B. TECH. PROJECT REPORT

On

Design and Development of FPGA based Power Quality Analyzer

BY

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DISCIPLINE OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

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Design and Development of FPGA Based Power Quality Analyzer

A PROJECT REPORT

Submitted in partial fulfillment of the
Requirement for the award of the degrees

of
BACHELOR OF TECHNOLOGY
in

ELECTRICAL ENGINEERING

Submitted by:
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Guided by:
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INDIAN INSTITUTE OF TECHNOLOGY INDORE
December 2017

CANDIDATE'S DECLARATION

We hereby declare that the project entitled **Design and Development of FPGA Based Power Quality Analyser** submitted in partial fulfillment for the award of the degree of Bachelor of Technology in **ELECTRICAL ENGINEERING** completed under the supervision of **Dr. Amod C. Umarikar, Associate Professor, Electrical Engineering Department,** IIT Indore is an authentic work.

Further, we declare that we have not submitted this work for the award of any other degree elsewhere.

Signature and name of the student(s) with date

_____

CERTIFICATE by BTP Guide

It is certified that the above statement made by the students is correct to the best of my/our knowledge.

Signature of BTP Guide with dates and their designation

Preface

This report on **Design and Development of FPGA Based Power Quality Analyser** is prepared under the guidance of **Dr. Amod C. Umarikar.**

The aims of the electric power system can be summarized as "to transport electrical energy from the generator units to the terminals of electrical equipment" and "to maintain the voltage at the equipment terminals within certain limits." For decades research and education have been concentrated on the first aim. Reliability and quality of supply were rarely an issue, the argument being that the reliability was sooner too high than too low. Overtime, It became clear that equipment regularly experienced spurious trips due to voltage disturbances, but also that equipment was responsible for many voltage and current disturbances. In order to improve the quality of service, electrical utilities must provide real-time monitoring systems that are able to identify the signatures of different disturbance events and thereby providing mitigation techniques to these power quality problems that will help practicing engineers and scientists to design better energy supply systems and mitigate existing ones.

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It is their help and support, due to which we became able to complete the design and technical report.

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Table of Contents

Abstract

Accurate and fast estimation of time-varying harmonics are essential requirements for online monitoring, analysis, and control of electrical power system. This report presents a fast algorithm based on Fast Fourier Transform (FFT) to estimate the amplitude of fundamental and harmonic components of stationary power signal. The robustness and accuracy of the proposed technique have been investigated on synthetic as well as experimental test signals using MATLAB tool. The FFT algorithm has been implemented using Xilinx Spartan-6 FPGA board, using ISE design suite 14.2.

Chapter 1

Introduction

The term power quality refers to a wide variety of electromagnetic phenomena that characterize the voltage and current at a given time and at a given location on the power system. PQ is the ability of power system to operate loads without damaging or disturbing them and, also the ability of loads to operate without disturbing or reducing efficiency of the power system. Institute of Electrical and Electronic Engineers (IEEE) Standard 1100 defines power quality as, “The concept of powering and grounding sensitive electronic equipment in a manner suitable for the equipment.” Ideally, the best electrical supply would be a sinusoidal voltage waveform with constant magnitude and constant frequency. The Power Quality of a system expresses to which degree a practical supply system resembles the ideal supply system. If the Power Quality of the network is good, then the loads connected to it will run satisfactorily and efficiently. If the Power Quality of the network is bad, then loads connected to it will fail or reduces the lifetime, and the efficiency of the electrical installation will reduce. Electrically-connected equipment is affected by power variations. Determining the exact problems requires sophisticated electronic test equipment.

Various sources use the term "power quality" with different meanings. Other sources use similar but slightly different terminology like "quality of power supply" or "voltage quality." What all these terms have in common is that they treat the interaction between the utility and the customer, or in technical terms between the power system and the load. Treatment of this interaction is in itself not new.

The aim of the power system has always been to supply electrical energy to the customers. What is new is the emphasis that is placed on this interaction, and the treatment of it as a separate area of power engineering. Utilities all over the world have for decades worked on the improvement of what is now known as power quality. The recent increased interest in power quality can be explained in a number of ways. Some of them are listed below:

1) Equipment has become more sensitive to voltage disturbances.

Electronic and power electronic equipment has especially become much more sensitive than its counterparts 10 or 20 years ago. Scientists have treated this increased sensitivity to voltage disturbances. Not only has equipment become more sensitive, companies have also become more sensitive to loss of production time due to their reduced profit margins. On the domestic market, electricity is more and more considered a basic right, which should simply always be present. The consequence is that an interruption of the supply and poor quality of power.

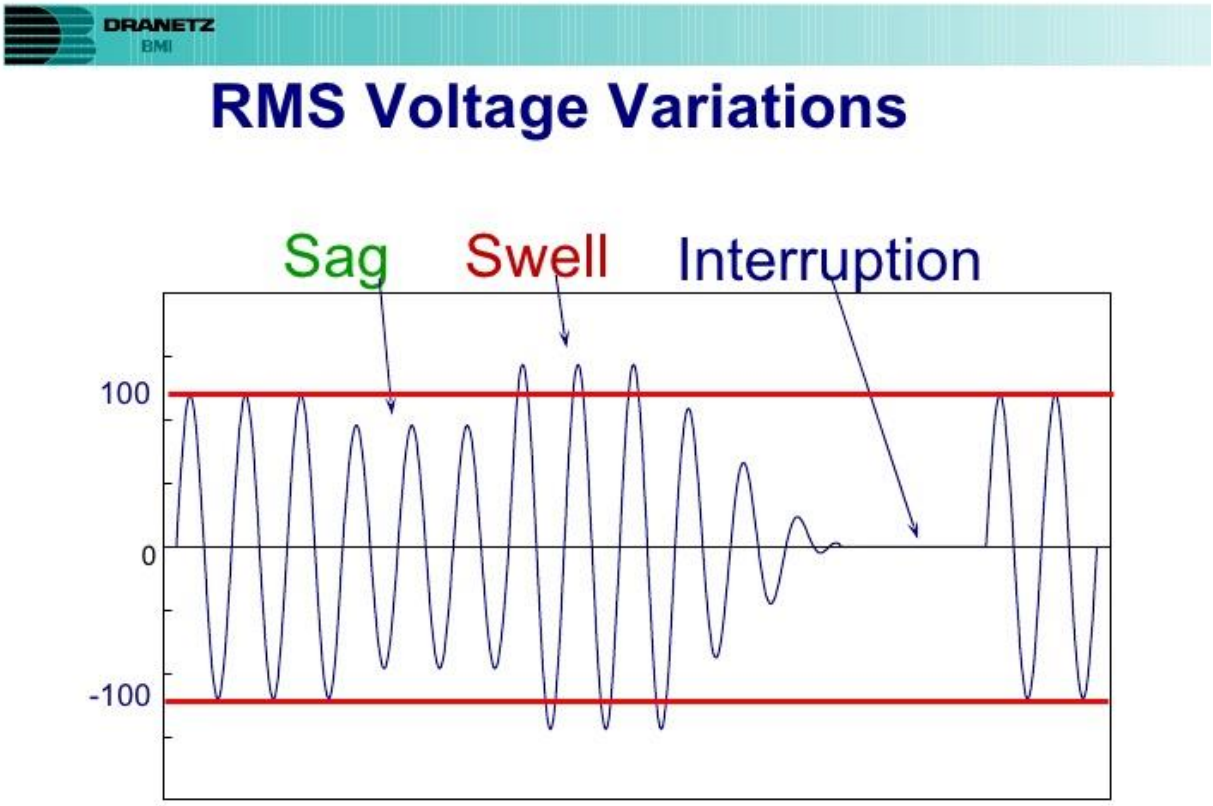
2) Equipment causes voltage disturbances.

Tripping of equipment due to disturbances in the supply voltage is often described by customers as "bad power quality." Utilities on the other side, often view disturbances due to end-user equipment as the main power quality problem. Modern (power) electronic equipment is not only sensitive to voltage disturbances, it also causes disturbances for other customers. The increased use of converter-driven equipment (from consumer electronics and computers, up to adjustable-speed drives) has led to a large growth of voltage disturbances, although fortunately not yet to a level where equipment becomes sensitive. The main issue here is the nonsinusoidal current of rectifiers and inverters. The input current not only ontains a power frequency component (50 Hz or 60 Hz) but also so-called harmonic components with frequencies equal to amultiple of the power frequency. The harmonic distortion of the current leads to harmonic components in the supply voltage.
Equipment has already produced harmonic distortion for a number of decades. But only recently has the amount of load fed via power electronic converters increased enormously: not only large adjustable-speed drives but also small consumer electronics equipment. The latter cause a large part of the harmonic voltage distortion: each individual device does not generate much harmonic currents but all of them together cause a serious distortion of the supply voltage.

3) A growing need for standardization and performance criteria.
The consumer of electrical energy used to be viewed by most utitiliessimply as a "load." Interruptions and other voltage disturbances were part of the deal, and the utility decided what was reasonable. Any customer who was not satisfied with the offered reliability and quality had to pay the utility for improving the supply.
Today the utilities have to treat the consumers as "customers." Even if theutility does not need to reduce the number of voltage disturbances, it does have to quantify them one 'way or the other. Electricity is viewed as a product with certain characteristics, which have to be measured, predicted, guaranteed, improved, etc. This is further triggered by the drive towards privatization and deregulation of the electricity industry.

4) Deregulation of market:

Open competition can make the situation even more complicated. In the past a consumer would have a contract with the local supplier who would deliver the electrical energy with a given reliability and quality. Nowadays the customer can buy electrical energy somewhere, the transport capacity somewhere else and pay the local utility, for the actual connection to the system. It is no longer clear who is responsible for reliability and power quality.
As long as the customer still has a connection agreement with the local utility, one can argue that the latter is responsible for the actual delivery and thus for reliability and quality. But what about voltage sags due to transmission system faults? In some cases the consumer only has a contract with a supplier who only generates the electricity and subcontracts transport and distribution. One could state that any responsibility should be defined by contract, so that the generation company with which the customer has a contractual agreement would be responsible for reliability and quality. The responsibility of the local distribution would only be towards the generation companies with whom they have a contract to deliver to given customers. No matter what the legal construction is, reliability and quality will need to be well defined.



5) Utilities want to deliver a good product.
Something that is often forgotten in the heat of the discussion is that many power quality developments are driven by the utilities. Most utilities simply want to deliver a good product, and have been committed to that for many decades. Designing a system with a high

reliability of supply, for a limited cost, is a technical challenge which appealed to many in the power industry, and hopefully still does in the future.

6) The power quality can be measured.
The availability of electronic devices to measure and show waveforms has certainly contributed to the interest in power quality. Harmonic currents and voltage sags were simply hard to measure on a large scale in the past. Measurements were restricted to rms voltage, frequency, and long interruptions; phenomena which are now considered part of power quality, but were simply part of power system operation in the past.

Signal Processing techniques

Various signal processing techniques can be used to break down the signal into various frequency components and hence estimate the power quality indices. To analyze the disturbances, present in the signal, data are often available as a form of sampled time function that is represented by a time series of amplitudes. When dealing with such data, the Fourier transform (FT)-based approach is most often used. FT provides the frequency information; however, it is not capable of providing time information about signal disturbances. For instance, time-frequency information related to disturbance waveforms can be obtained by using the STFT. Similarly, DWT can be used, however to make the filter more adaptive a new technique Adaptive Spectral Segmentation (AFSS) is proposed which segments the spectrum based on the boundaries calculated separately for each new signal.

System Generator

System Generator is a DSP design tool from Xilinx that enables the use of the MathWorksmodel-based Simulink design environment for FPGA design. Previous experience with Xilinx FPGAs or RTL design methodologies are not required when using System Generator. Designs are captured in the DSP friendly Simulink modeling environmentusing a Xilinx specific blockset. All of the downstream FPGA implementation stepsincluding synthesis and place and route are automatically performed to generate an FPGAprogramming file.

FPGAs

A field programmable gate array (FPGA) is a general-purpose integrated circuit that is“programmed” by the designer rather than the device manufacturer. Unlike an application-specific integrated circuit (ASIC), which can perform a similar function in an electronic system, an FPGA can be reprogrammed, even after it has been deployed into a system.

An FPGA is programmed by downloading a configuration program called a bitstream into static on-chip random-access memory. Much like the object code for a microprocessor, this bitstream is the product of compilation tools that translate the high-level abstractions produced by a designer into something equivalent but low-level and executable. Xilinx System Generator pioneered the idea of compiling an FPGA program from a high-level Simulink model.

An FPGA provides you with a two-dimensional array of configurable resources that can implement a wide range of arithmetic and logic functions. These resources include dedicated DSP blocks, multipliers, dual port memories, lookup tables (LUTs), registers, tristatebuffers, multiplexers, and digital clock managers. In addition, Xilinx FPGAs contain sophisticated I/O mechanisms that can handle a wide range of bandwidth and voltage requirements. The Virtex®-4 FPGAs include embedded microcontrollers (IBM PowerPC®405), and multi-gigabit serial transceivers. The compute and I/O resources are linked under the control of the bitstream by a programmable interconnect architecture that allows them to be wired together into systems.

Chapter 2

Harmonics Analysis

The **Cooley–Tukey algorithm**, named after J.W. Cooley and John Tukey, is the most common fast Fourier transform (FFT) algorithm. It re-expresses the discrete Fourier transform (DFT) of an arbitrary composite size $N = N_1N_2$ in terms of N_1 smaller DFTs of sizes N_2, recursively, to reduce the computation time to O(N log N) for highly composite N (smooth numbers). Because of the algorithm's importance, specific variants and implementation styles have become known by their own names, as described below.

Because the Cooley-Tukey algorithm breaks the DFT into smaller DFTs, it can be combined arbitrarily with any other algorithm for the DFT.

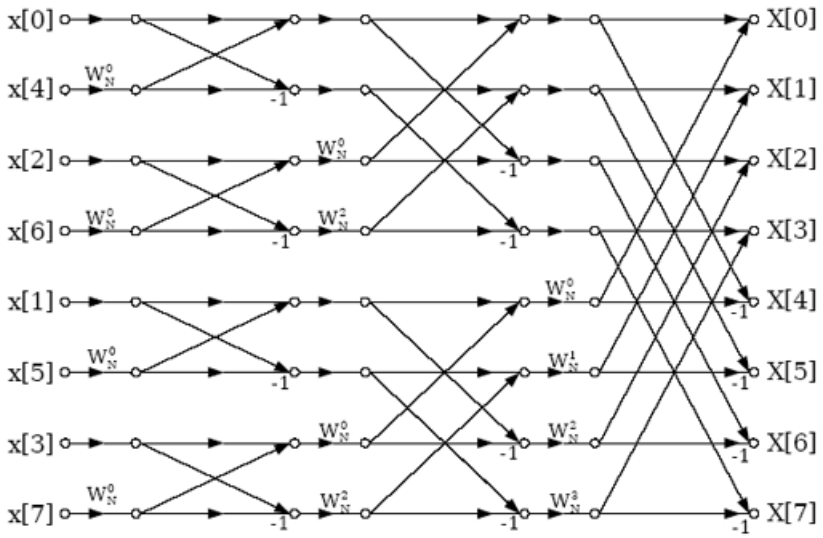
For example, Rader's or Bluestein's algorithm can be used to handle large prime factors that cannot be decomposed by Cooley–Tukey, or the prime-factor algorithm can be exploited for greater efficiency in separating out relatively prime factors.

The algorithm, along with its recursive application, was invented by Carl Friedrich Gauss. Cooley and Tukey independently rediscovered and popularized it 160 years later.

Here, radix-2 DIT form of Cooley- Tuckey algorithm was implemented.

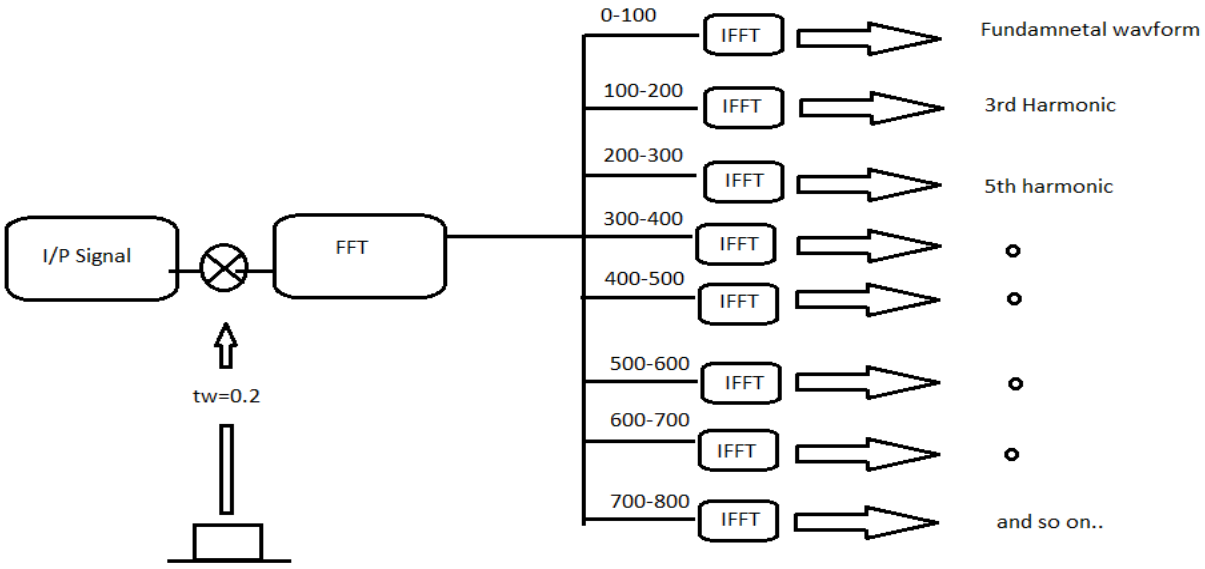
The radix-2 DIT

A **radix-2** decimation-in-time (**DIT**) FFT is the simplest and most common form of the Cooley–Tukey algorithm, although highly optimized Cooley–Tukey implementations typically use other forms of the algorithm as described below. Radix-2 DIT divides a DFT of size N into two interleaved DFTs (hence the name "radix-2") of size $N/2$ with each recursive



stage.

Logic



The input signal is extracted using the above mentioned windowing logic.

Calculations

No.of multiplications(m)= Nlog2N

No. of additions(n) = 2Nlog2N

Total no. of operations = 2*m + 2*n

Frequency=(location of frequency bin – 1)*sampling freq/no. of samples in an interval

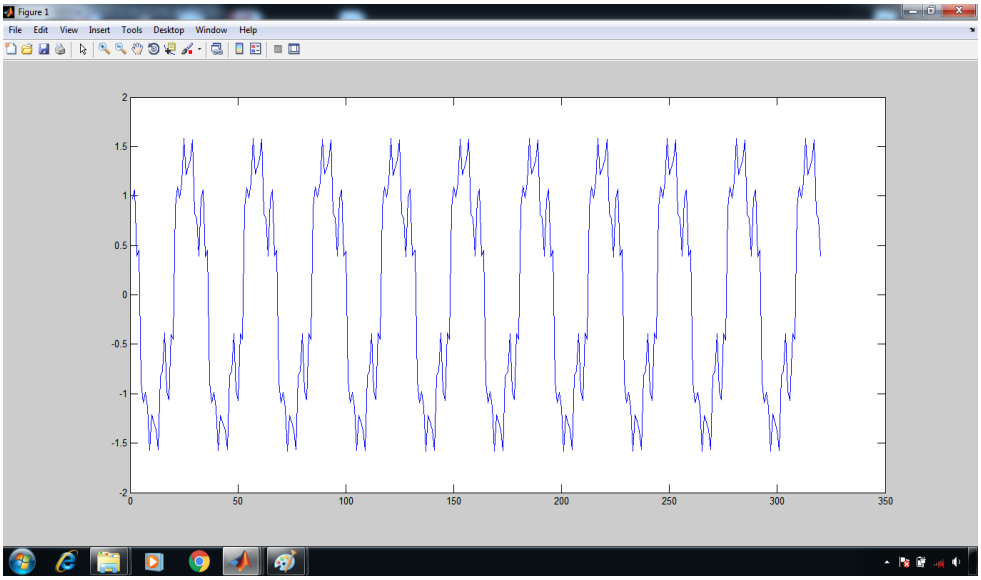
Sampling frequency=1600Hz

Fundamental frequency=50Hz

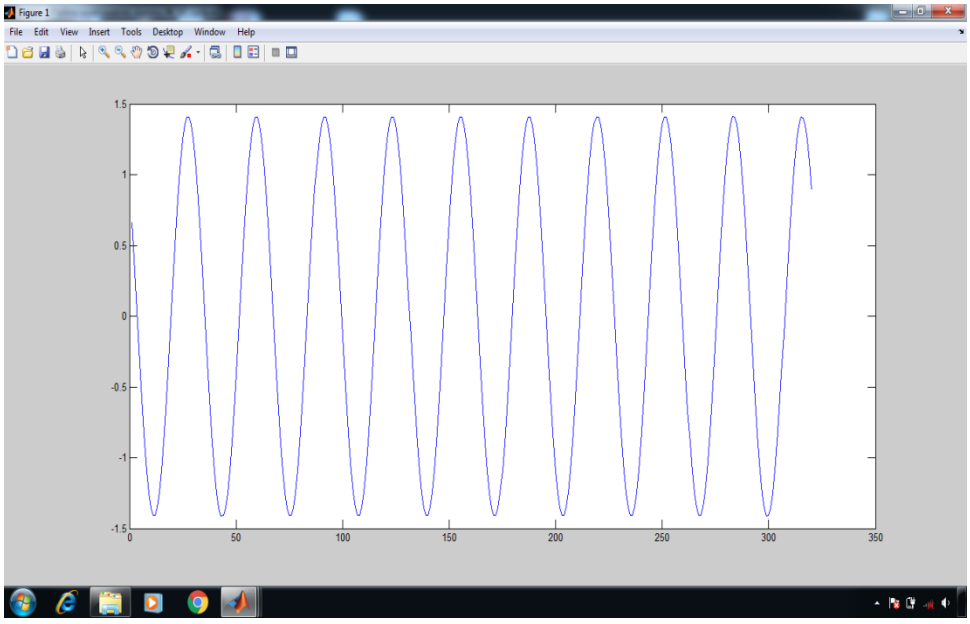
Observation

1. Stationary Signal

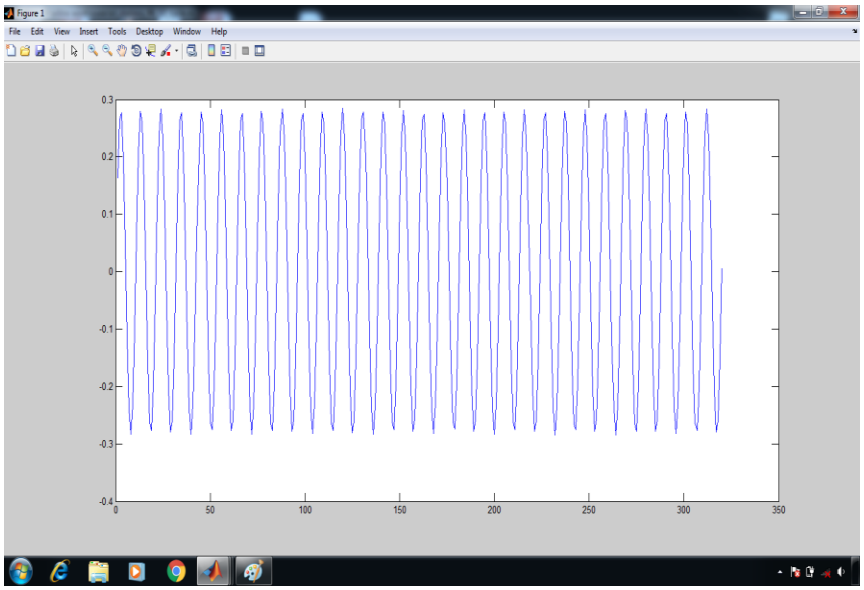
Original Waveworm



Fundamental waveworm



3rd harmonic



Standard deviation error

Variables - sd_err

per_rms_err | rmsfin | sd_err

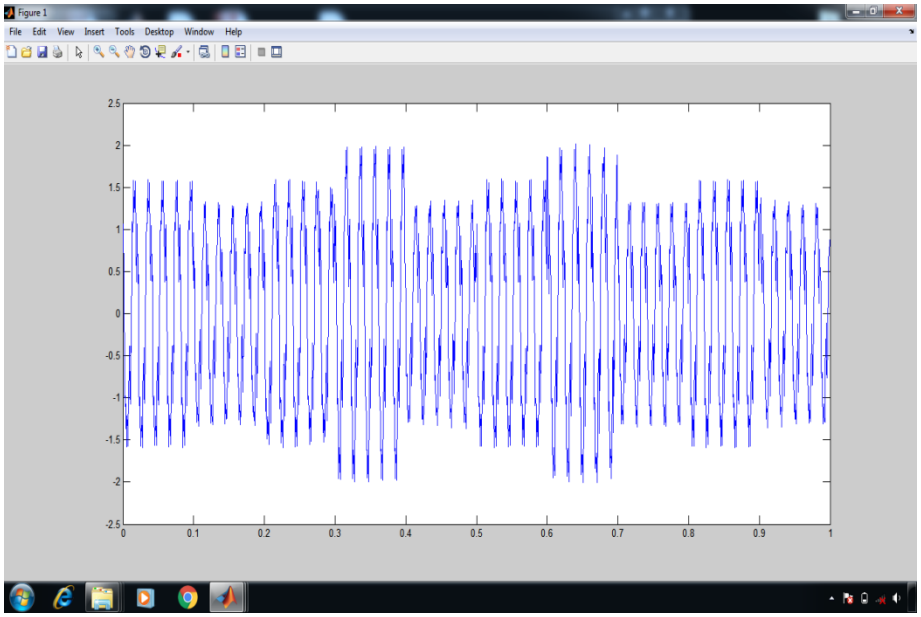
sd_err <1x8 double>

	1	2	3	4	5	6	7	8	9	10
1	1.2181e-04	4.9533e-05	1.2989e-04	7.4865e-05	6.1726e-05	9.5773e-05	7.2382e-05	7.6122e-05		
2										
3										
4										
5										
6										
7										
8										
9										

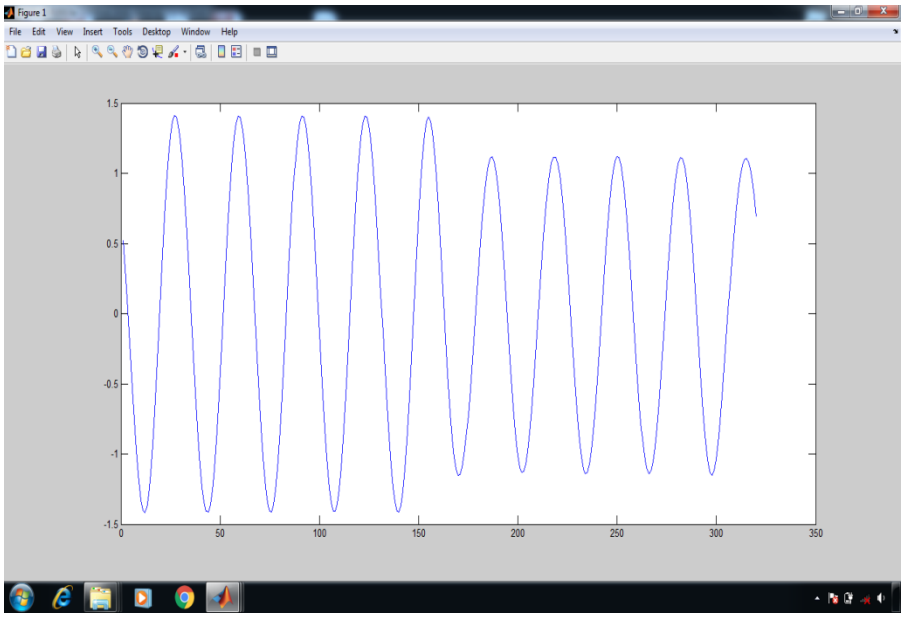
2. Time Varying Signal

Observation

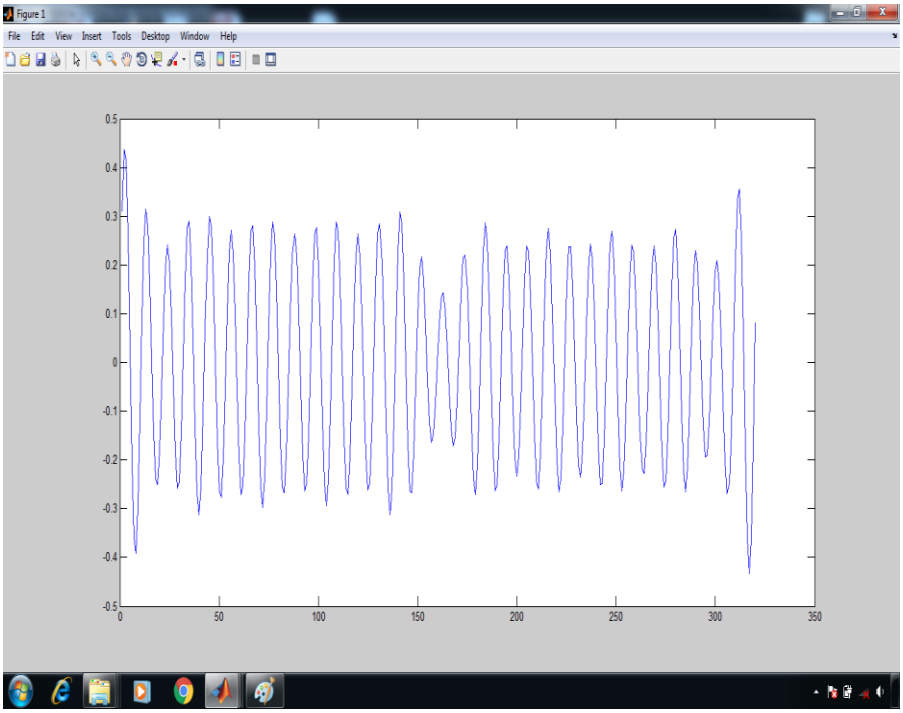
Original waveform



Fundamental Harmonic



3rd Harmonic



Chapter 3

Hardware Co-simulation

System Generator for DSP provides the functionality for performing Hardware Co-Simulation for designs that run both in hardware and in software. Hardware Co-Simulation can verify the operation of designated parts of a design in hardware to significantly decrease simulation runtimes. This is a powerful feature of System Generator for DSP, especially when considering the parallel nature of FPGA devices. Hardware Co-Simulation can make it possible to complete even very long simulations within a much shorter period of time.

System Generator DSP simulation performance results are analyzed by reviewing simulation run times. In addition, the way that a System Generator for DSP simulation fits into a Simulink simulation also affects performance. The following sections are included to provide background about how System Generator for DSP blocks fit into the Simulink simulation environment.

It is important to understand how a Hardware Co-Simulation fits into a Simulink simulation. There are two clocking schemes available: single-stepped, and free-running.

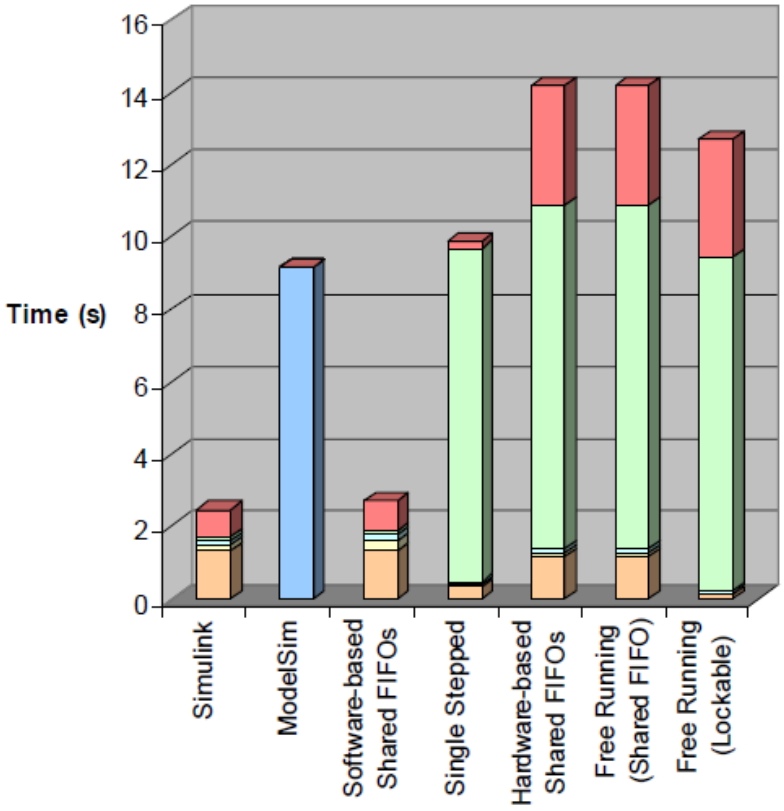
- In a **single-stepped** simulation, the clock from the System Generator solver is sent to the logic running in hardware over the Hardware Co-Simulation interface.
- In a **free-running** simulation, the part of the design that is running in software is not synchronized with the part running in hardware. The clock driving the logic in hardware is typically an onboard oscillator, which easily outperforms the single-stepped clock provided by Simulink.

Comparison of Implementations

A comparison of the results obtained for each implementation method is provided to show which method may produce the best results for different simulation times. Results are compared at three different simulation runtimes: 1,000, 10,000 and 100,000. This is followed by a comparison of the three fastest hardware implementations over very long simulation runtimes.

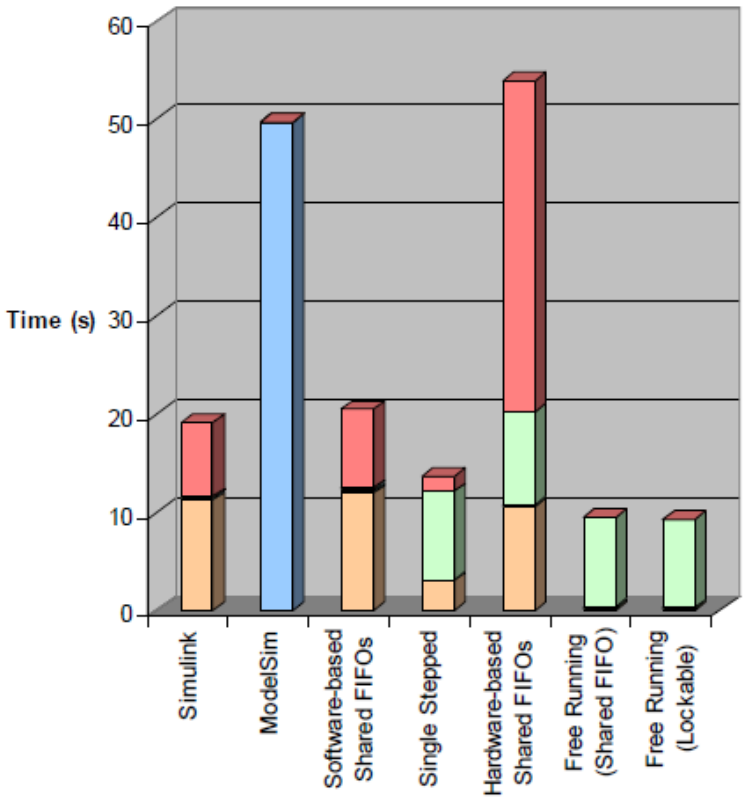
Short Runtime Comparison: 1000s

For short simulation times, comparison shows that a software implementation outperforms the hardware implementations. This is expected, as the Hardware Co-Simulation implementations must initialize the hardware (configure FPGAs, etc.) as indicated by the *Sysgen: Initialize Simulation* portions of Figure. This is not necessary for any software-only implementations.



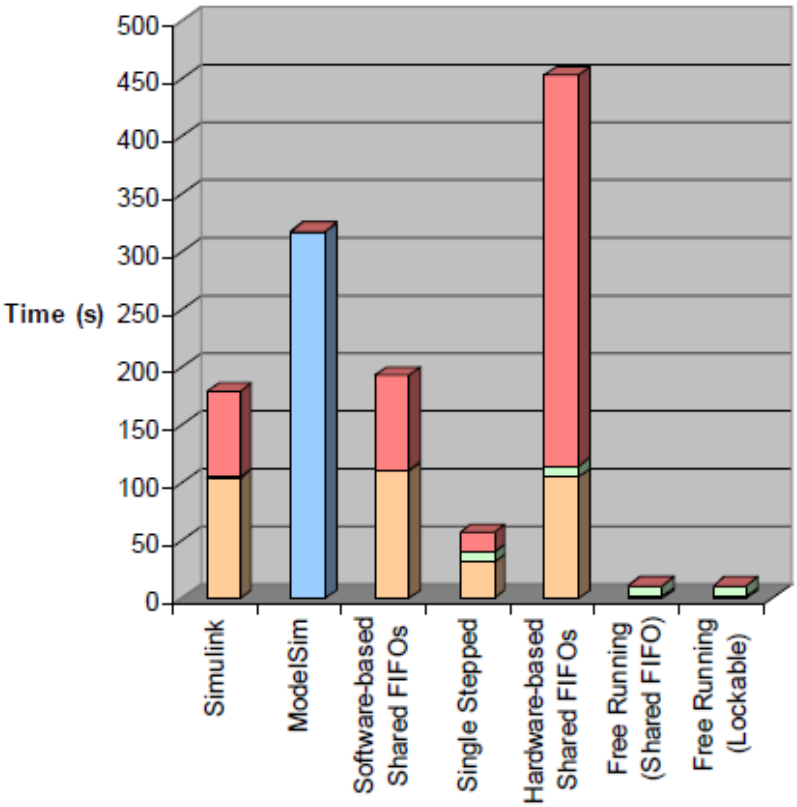
Intermediate Runtime Comparison: 10,000s

As shown, the runtimes of software and hardware implementations are fairly close to eachother. This is due to the time required to initialize the hardware simulations (program the FPGA,etc.) as that is fairly constant and independent of simulation runtime. This is the majordisadvantage of the hardware implementations with a short simulation.Figure illustrates the intermediate simulation times comparison.



Long Runtime Comparison: 100,000s

Figure shows the longer runtime comparison. As indicated, the Hardware Co-Simulation implementations clearly outperform the software implementations, with the frame-based free running simulations outperforming a single stepped Hardware Co-Simulation.


Time (s)
500
450
400
350
300
250
200
150
100
50
0
Simulink
ModelSim
Software-based Shared FIFOs
Single Stepped
Hardware-based Shared FIFOs
Free Running (Shared FIFO)
Free Running (Lockable)

Chapter 4

Fast Fourier Transform v7.1

Introduction

The Xilinx LogiCORE™ IP Fast Fourier Transform (FFT) implements the Cooley-Tukey FFT algorithm, a computationally efficient method for calculating the Discrete Fourier Transform (DFT).

Features

- Drop-in module for Kintex™-7, Virtex®-7, Virtex®-6, Virtex-5, Virtex-4, Spartan®-6, Spartan-3/XA,Spartan-3E/XA and Spartan-3A/XA/AN/3A DSPFPGAs
- Forward and inverse complex FFT, run-time configurable
- Transform sizes $N = 2m$, $m = 3 – 16$
- Data sample precision $bx = 8 – 34$
- Phase factor precision $bw = 8 – 34$
- Arithmetic types:
  ¨ Unscaled (full-precision) fixed-point
  ¨ Scaled fixed-point
  ¨ Block floating-point
- Fixed-point or floating-point interface
- Rounding or truncation after the butterfly
- Block RAM or Distributed RAM for data and phase-factor storage
- Optional run-time configurable transform point size
- Run-time configurable scaling schedule for scaled fixed-point cores
- Bit/digit reversed or natural output order
- Optional cyclic prefix insertion for digital communications systems
- Four architectures offer a trade-off between coresize and transform time
- Bit-accurate C model and MEX function for systemmodeling available for download
- For use with Xilinx CORE Generator™ softwareand Xilinx System Generator for DSP v13.1

Overview

The FFT core computes an N-point forward DFT or inverse DFT (IDFT) where N can be 2m, m = 3–16. For fixed-point inputs, the input data is a vector of N complex values represented

as dual bx-bit two's-complementnumbers, that is, bx bits for each of the real and imaginary components of the data sample, where bx is in the range8 to 34 bits inclusive. Similarly, the phase factors bw can be 8 to 34 bits wide.For single-precision floating-point inputs, the input data is a vector of N complex values represented as dual 32-bitfloating-point numbers with the phase factors represented as 24- or 25-bit fixed-point numbers.

All memory is on-chip using either block RAM or distributed RAM. The N element output vector is represented using by bits for each of the real and imaginary components of the output data. Input data is presented in natural order and the output data can be in either natural or bit/digit reversed order. The complex nature of data input and output is intrinsic to the FFT algorithm, not the implementation.

Three arithmetic options are available for computing the FFT:

- Full-precision unscaled arithmetic
- Scaled fixed-point, where the user provides the scaling schedule
- Block floating-point (run-time adjusted scaling)

The point size N, the choice of forward or inverse transform, the scaling schedule and the cyclic prefix length arerun-time configurable. Transform type (forward or inverse), scaling schedule and cyclic prefix length can bechanged on a frame-by-frame basis. Changing the point size resets the core.Four architecture options are available: Pipelined, Streaming I/O, Radix-4, Burst I/O, Radix-2, Burst I/O, andRadix-2 Lite, Burst I/O. For detailed information about each architecture

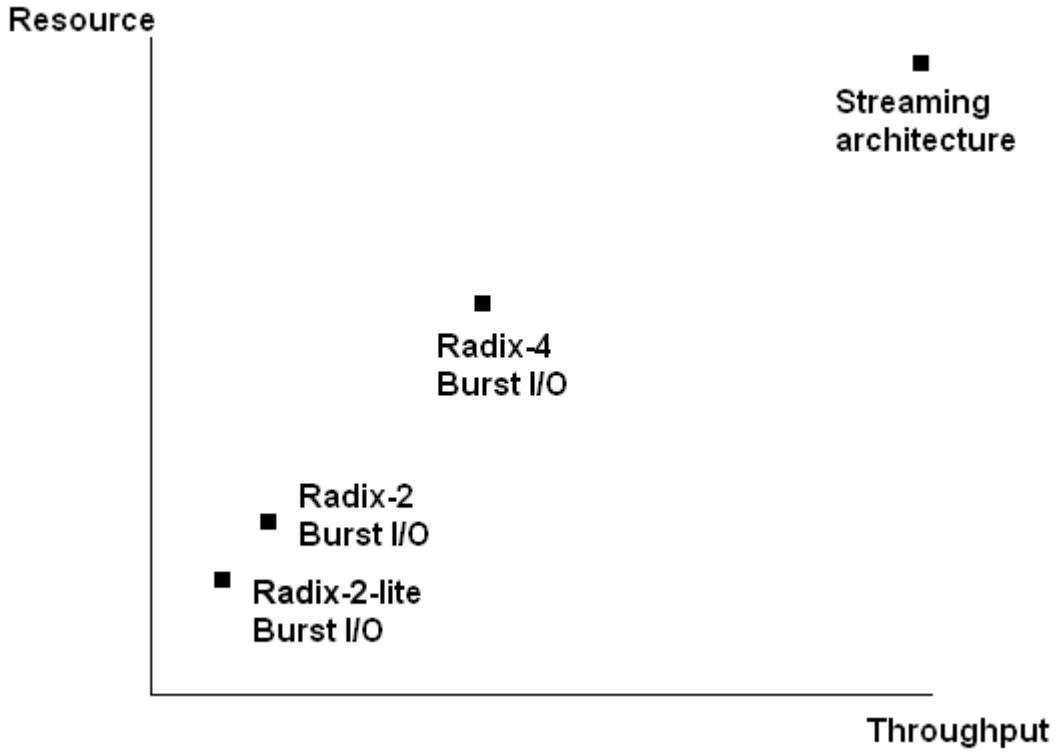
Architecture

The FFT core provides four architecture options to offer a trade-off between core size and transform time.

- **Pipelined, Streaming I/O –** Allows continuous data processing.
- **Radix-4, Burst I/O –** Loads and processes data separately, using an iterative approach. It is smaller in size thanthe pipelined solution, but has a longer transform time.
- **Radix-2, Burst I/O –** Uses the same iterative approach as Radix-4, but the butterfly is smaller. This means it is smaller in size than the Radix-4 solution, but the transform time is longer.
- **Radix-2 Lite, Burst I/O –** Based on the Radix-2 architecture, this variant uses a time-multiplexed approach tothe butterfly for an even smaller core, at the cost of longer transform time.

Figure illustrates the trade-off of throughput versus resource use for the four architectures. As a rule of thumb,each architecture offers a factor of 2 difference in resource from the next architecture. The example is for an evenpower of 2 point size. This does not require the Radix-4 architecture to have an additional Radix-2 stage.

All four architectures may be configured to use a fixed-point interface with one of three fixed-point arithmeticmethods (unscaled, scaled or block floating-point) or may instead use a floating-point interface.



Pipelined, Streaming I/O

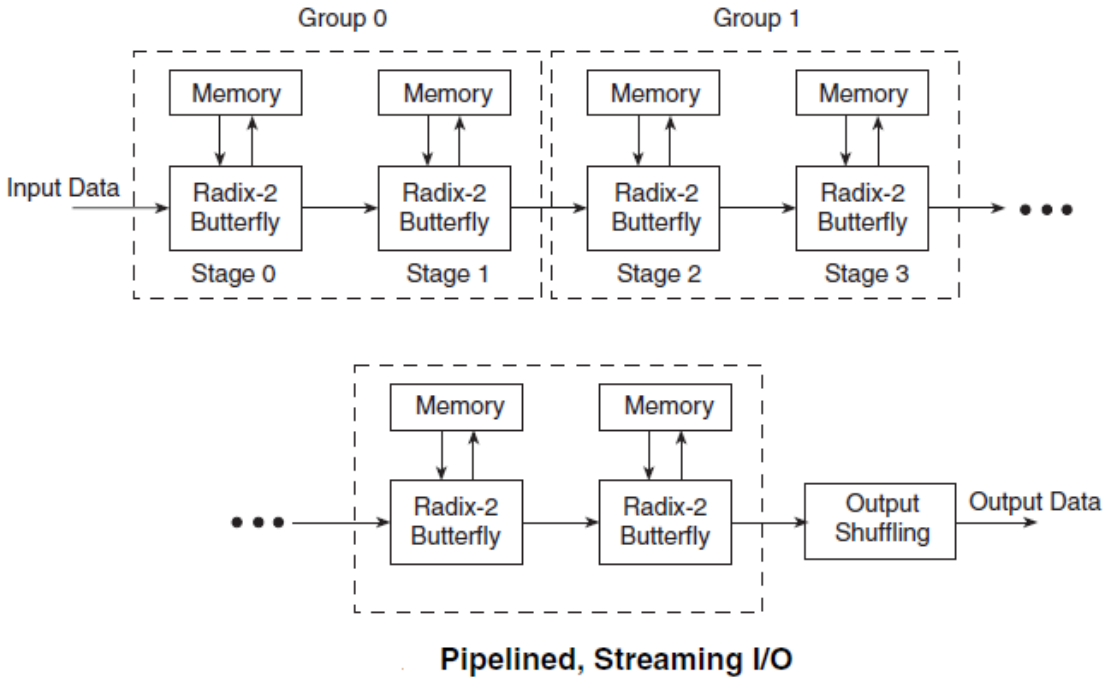
The Pipelined, Streaming I/O solution pipelines several Radix-2 butterfly processing engines to offer continuousdata processing. Each processing engine has its own memory banks to store the input and intermediate data(Figure). The core has the ability to simultaneously perform transform calculations on the current frame of data,load input data for the next frame of data, and unload the results of the previous frame of data. The user can continuouslystream in data and, after the calculation latency, can continuously unload the results. If preferred, thisdesign can also calculate one frame by itself or frames with gaps in between.

In the scaled fixed-point mode, the data is scaled after every pair of Radix-2 stages. The block floating-point modemay use significantly more resources than the scaled mode, as it must maintain extra bits of precision to allowdynamic scaling without impacting

performance. Therefore, if the input data is well understood and is unlikely toexhibit large amplitude fluctuation, using scaled arithmetic (with a suitable scaling schedule to avoid overflow inthe known worst case) is sufficient, and resources may be saved.

The input data is presented in natural order. The unloaded output data can either be in bit reversed order or in naturalorder. When natural order output data is selected, additional memory resource is utilized.

This architecture covers point sizes from 8 to 65536. The user has flexibility to select the number of stages to useblock RAM for data and phase factor storage. The remaining stages use distributed memory.



ADAPTIVE FOURIER SPECTRAL SEGMENTATION (AFSS)

Owing to the limitations of FFT and DWT, a new method of AFSS is proposed.

In FFT, the time information of the signal is lost. We can find out what frequencies are present in a signal but we cannot locate them, we cannot find out what frequencies are

present at what time. Though this information is quite represented in DWT owing to the localized and short duration of mother wavelet which is able to represent localised features but the DWT is not adaptive. In DWT, once we fix the sampling frequency, the filter design is fixed that is the segmentation becomes predefined for the signal. As a result, it may suit quite well for some signals but may not be quite for another. Now, AFSS overcomes these limitations by restructuring the filter design each time for every new signal. The boundaries or the segmentations in the spectrum are calculated separately each time for new signal which accounts for minimum spectral leakage and minimum overlapping of two frequencies on each other. Consequently, the error in the estimation in the PQIs reduces and hence the term ADAPTIVE.

The procedure followed by Adaptive Fourier Spectral Segmentation is as follows:

Step 1) Determine the frequency components of the applied signal using FFT. 20

Step 2) Calculate the number of peaks (maxima) occurring by applying constraints of magnitude threshold (3% of the fundamental frequency magnitude) and frequency distance threshold.

Step 3) Now, find out the minima between these peaks and the location of these minima.

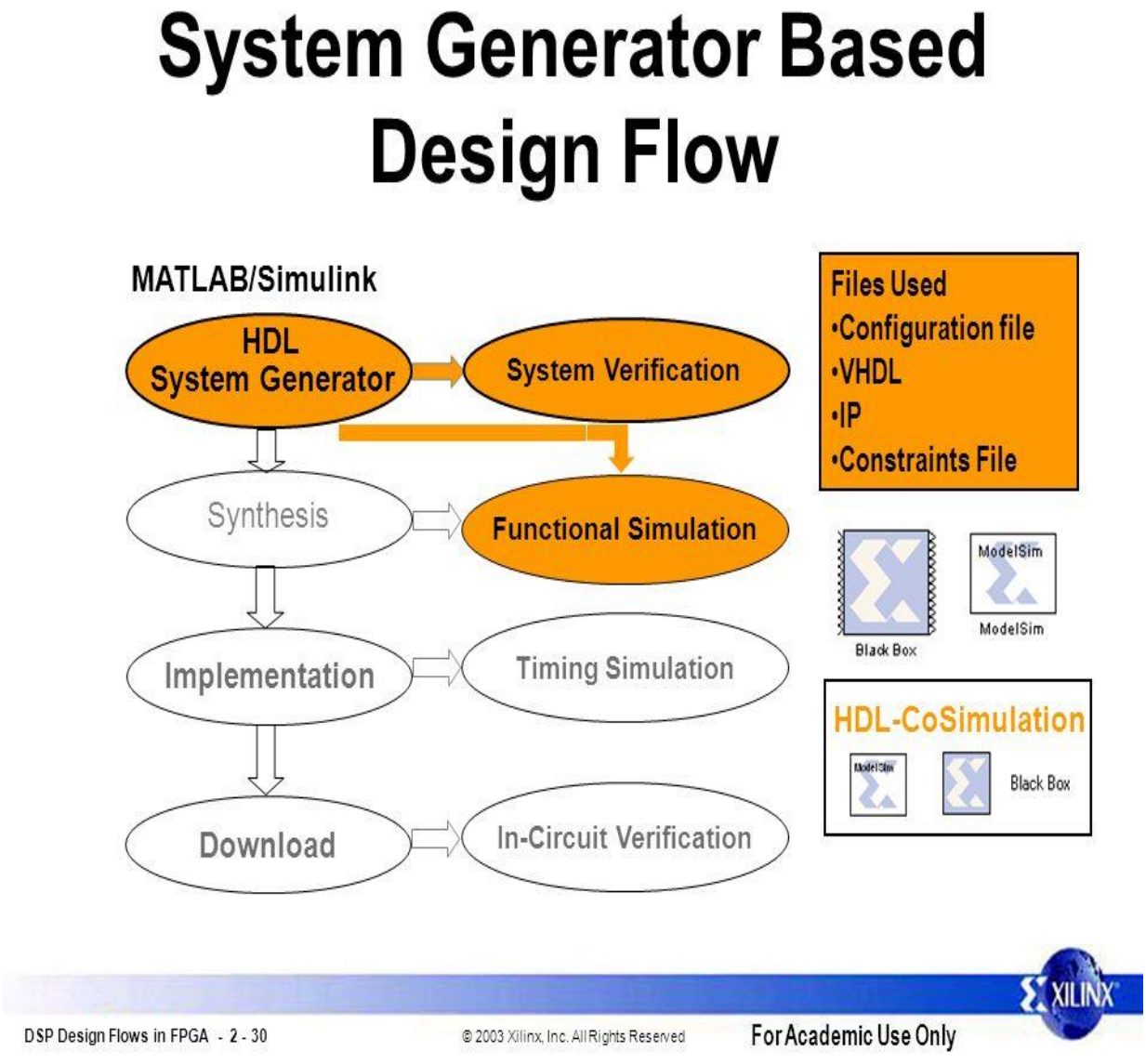
Step 4) Segment the spectrum on the lines of these frequencies at which minima occurs.

Step 5) Now, calculate the PQIs from this segmented spectrum. FFT-based indices can be used as calculations are done in frequency domain itself.

Chapter 5

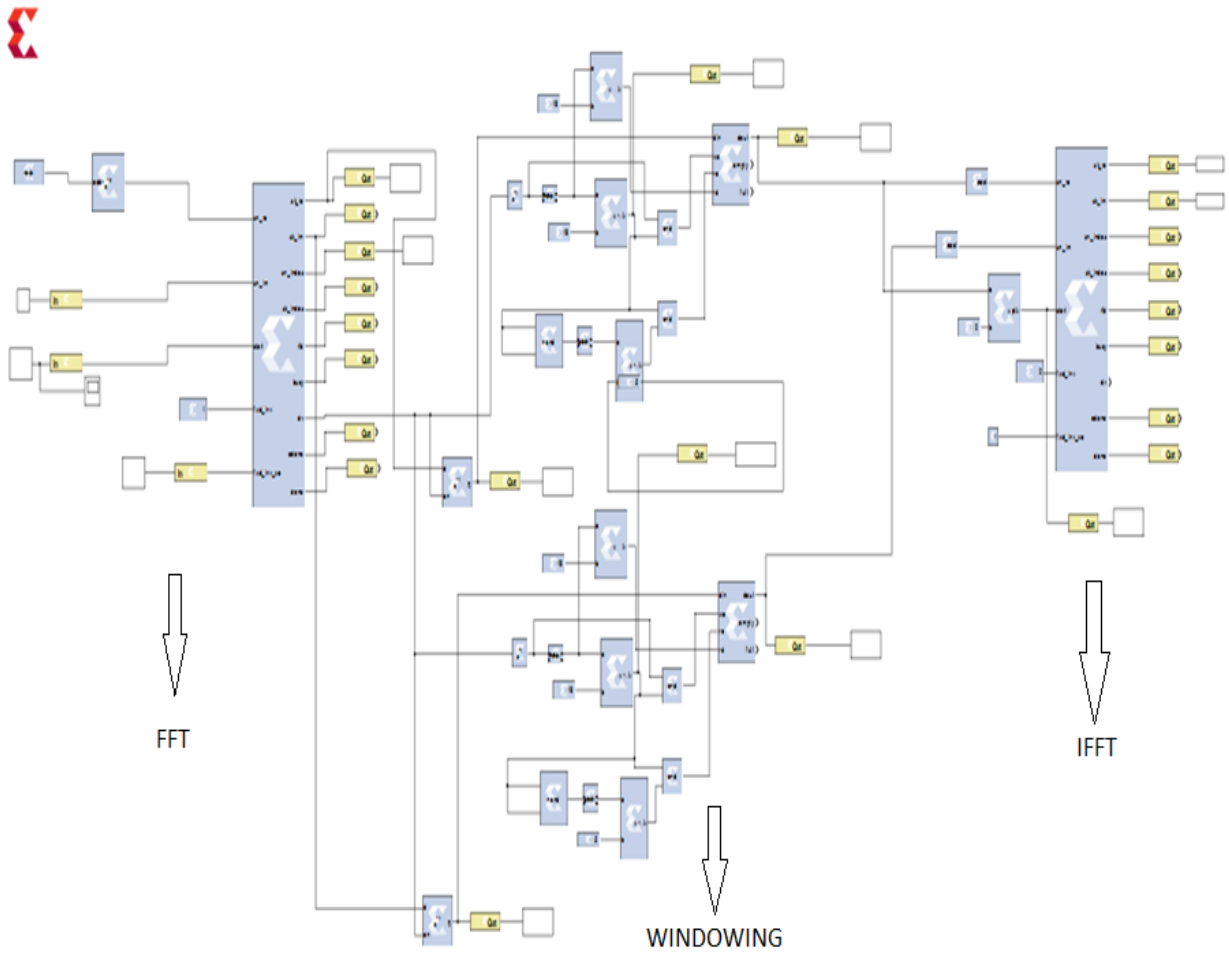
Design

This section of the document gives the detailed description of the model(fig-3), which is both Online and Real Time, designed to implement IEC-61000-4-7 standards using FFT The design uses FFT v 7.1 block configured for our requirements.



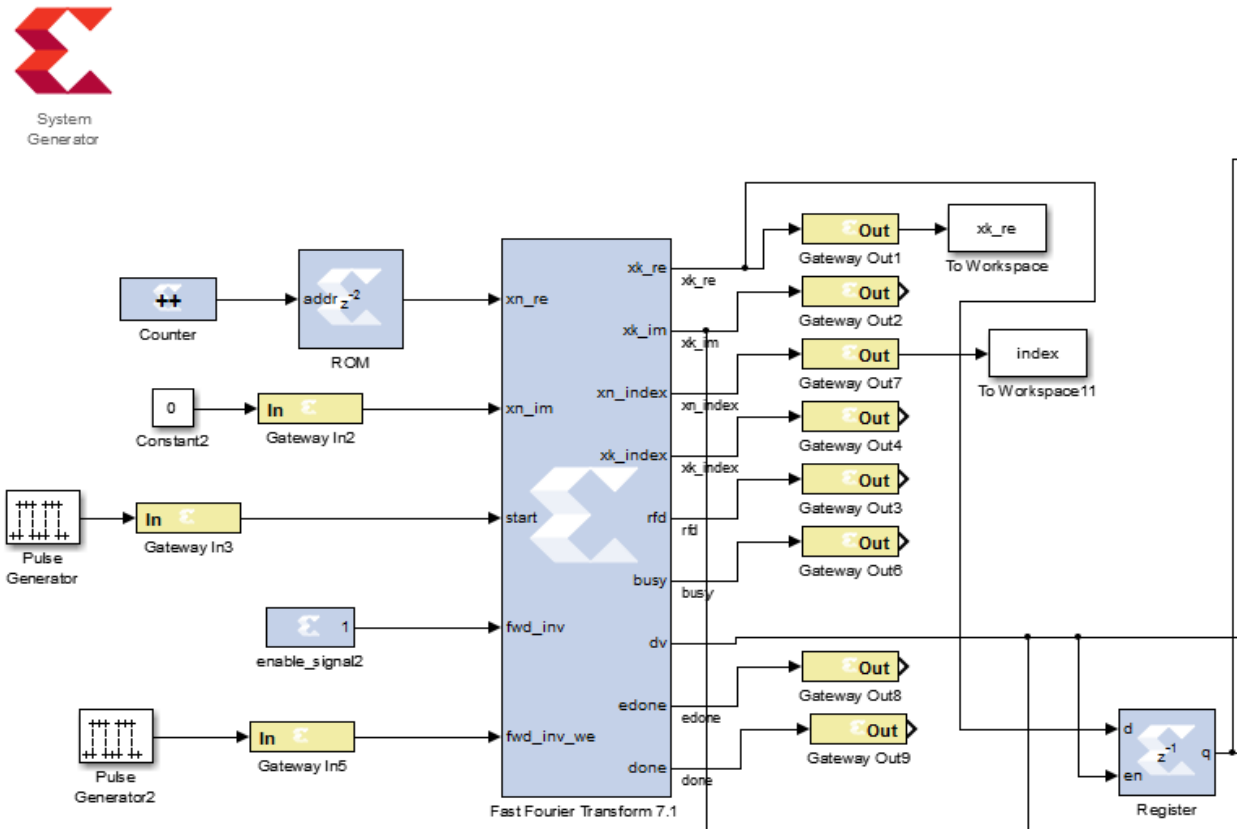
The model is developed in three phases:

1. Fast Fourier Transform
2. Windowing
3. Inverse FFT



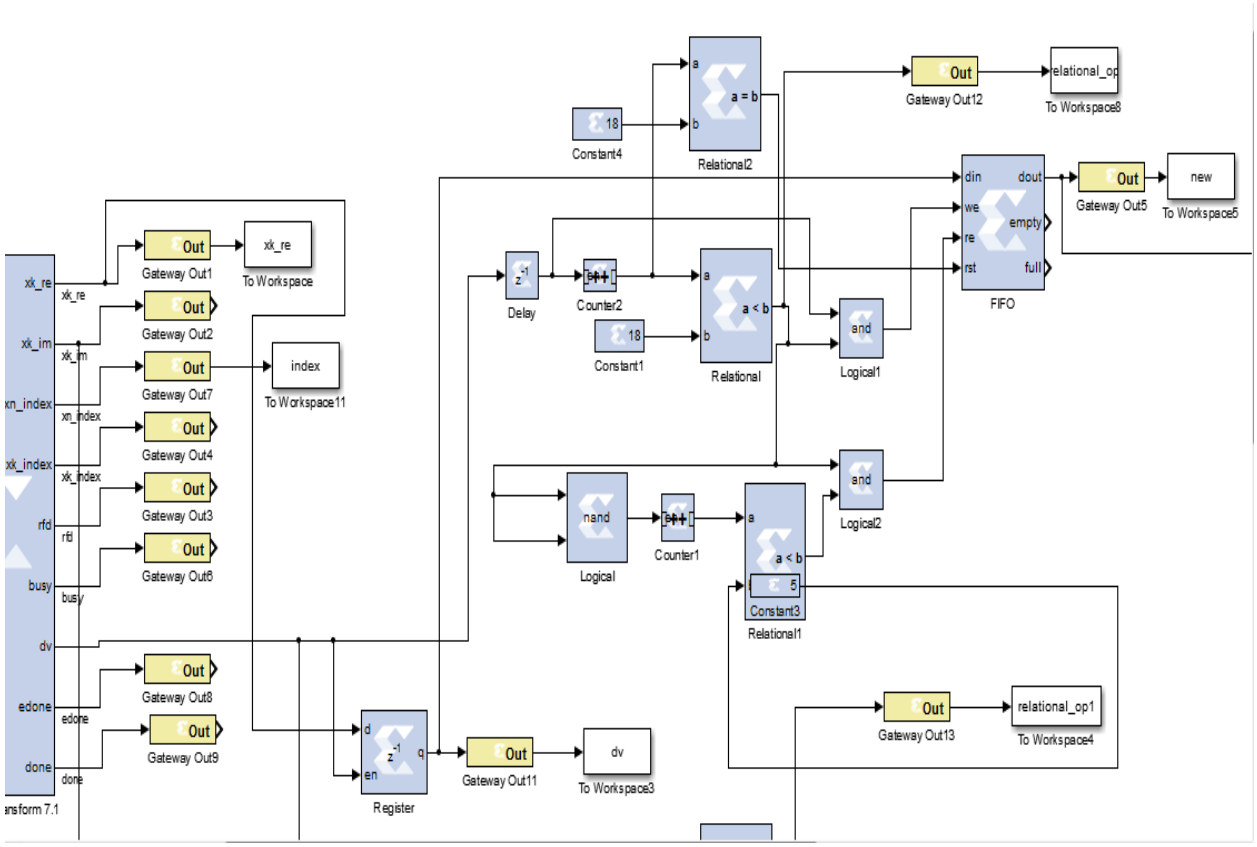
1. FFT

256-point FFT is implemented as shown below. The stationary signal is uploaded from workspace and FFT is computed.



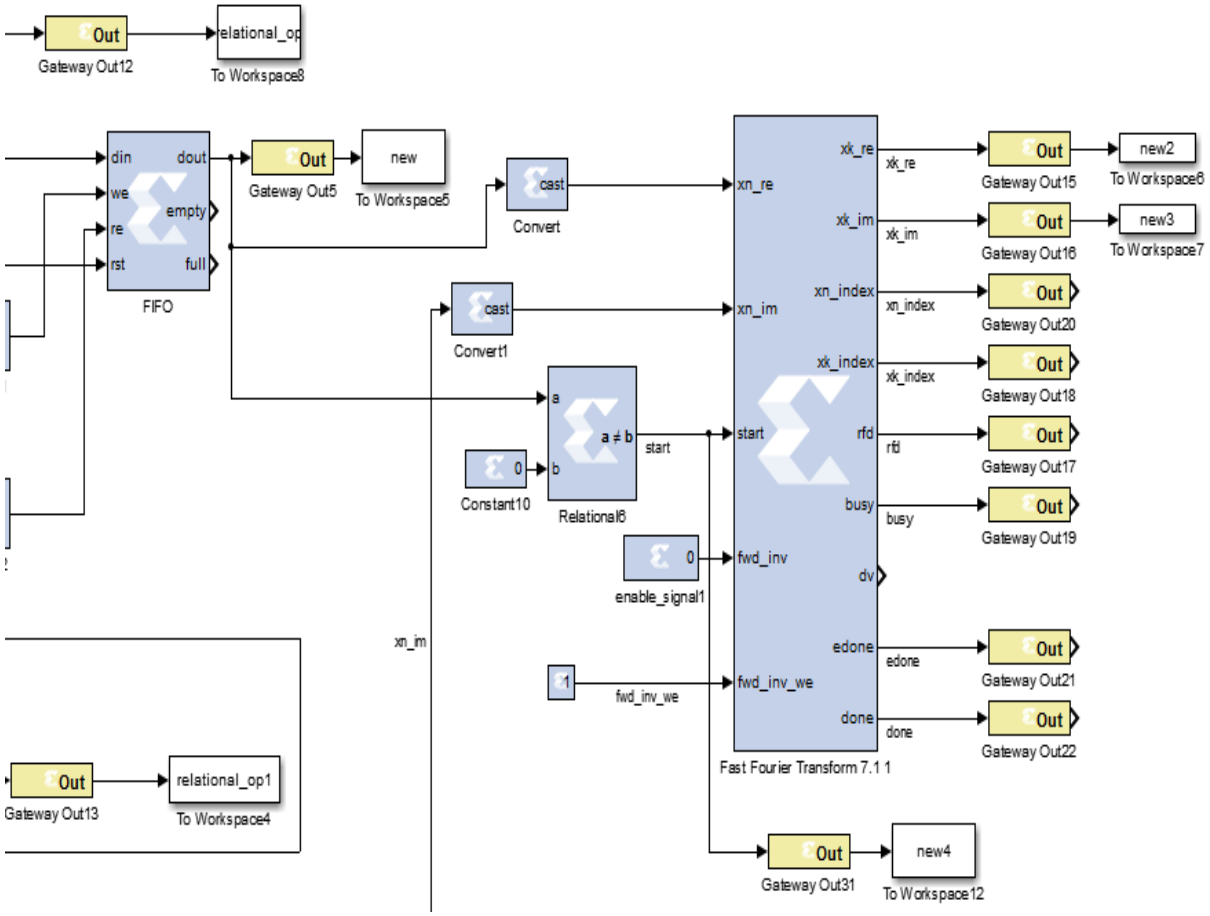
2. Windowing

The output of FFT contains delay which is caused by the time taken by the FFT block to take all the input values. A window of width 18 was applied for the index interval 610-627 and the last value was reset to get zero after the window. The output of logic was fed to the FIFO and perfect windowing was observed.



3. IFFT

The output of windowing was fed to the IFFT block as shown below.



Conclusion

- Harmonics analysis was completed and verified on MATLAB.
- Partial completion of hardware implementation.

Future Scope

The simulation can be completed and and the hardware can be successfully designed on FPGA.

Once the fundamental frequency and harmonics are extracted the power quality indices can be calculated.

Power quality indices gives the complete information of power quality in the power system.

Once the analysis is complete the necessary measure can be taken.

References

[1] V. E. Wagner *et al.*, “Effects of harmonics on equipment,” *IEEE Trans. Power Del.*, vol. 8, no. 2, pp. 672–680, Apr. 1993.

[2] M. Bollen and I. Gu, *Signal Processing of Power Quality Disturbances*. Hoboken, NJ, USA: Wiley, 2006.

[3] *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, IEEE Standard 519-2014 (Revision IEEE Std 519-1992), 2014, pp. 1–29.

[4] *Testing and Measurement Techniques—General Guide on Harmonics and Interharmonics Measurements and Instrumentation, for Power Supply Systems and Equipment Connected Thereto*, IEC Standard 61000-4-7, 2002.

[5] G. D’Antona, C. Muscas, P. A. Pegoraro, and S. Sulis, “Harmonic source estimation in distribution systems,” *IEEE Trans. Instrum. Meas.*, vol. 60, no. 10, pp. 3351–3359, Oct. 2011.

[6] M. S. Hamad, M. I. Masoud, K. H. Ahmed, and B. W. Williams, “A shunt active power filter for a medium-voltage 12-pulse current source converter using open loop control compensation,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5840–5850, Nov. 2014.

[7] M. A. M. Radzi and N. A. Rahim, “Neural network and bandless hysteresis approach to control switched capacitor active power filter for reduction of harmonics,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1477–1484, May 2009.

[8] N. Locci, C. Muscas, and S. Sulis, “Investigation on the accuracy of harmonic pollution metering techniques,” *IEEE Trans. Instrum. Meas.*, vol. 53, no. 4, pp. 1140–1145, Aug. 2004.

[9] G. W. Chang, C.-I. Chen, and Y.-F. Teng, “Radial-basis-function-based neural network for harmonic detection,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2171–2179, Jun. 2010.

[10] J. Barros and R. I. Diego, “On the use of the Hanning window for harmonic analysis in the standard framework,” *IEEE Trans. Power Del.*, vol. 21, no. 1, pp. 538–539, Jan. 2006.