Scaling Limits of Capacitorless DRAM Implemented Through Twin-gate Reconfigurable Transistor

M.Tech Thesis

By

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A THESIS

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **Scaling Limits of Capacitorless DRAM Implemented Through Twin-gate Reconfigurable Transistor** in the partial fulfillment of the requirements for the award of the degree of **MASTER OF TECHNOLOGY** and submitted in the **DEPARTMENT OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from July, 2021 to June, 2022 under the supervision of Dr. Abhinav Kranti, Professor, Discipline of Electrical Engineering, Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Arghya Singha Roy

30/05/2022

Signature of the student with date
(ARGHYA SINGHA ROY)

This is to certify that the above statement made by the candidate is correct to the best of my/~~our~~ knowledge.

30/05/2022

Signature of the Supervisor of M.Tech. thesis (with date)
(Prof. ABHINAV KRANTI)

ARGHYA SINGHA ROY has successfully given his/~~her~~ M.Tech. Oral Examination held on **6th June, 2022.**

Signature of Supervisor of M.Tech. thesis
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Signature of PSPC Member 2
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Dedicated to my family

Abstract

SCALING LIMITS OF CAPACITORLESS DRAM IMPLEMENTED THROUGH TWIN-GATE RECONFIGURABLE TRANSISTOR

As we moved through the age of machine learning, big data and Artificial Intelligence (AI), the requirements for computations have increased drastically. So has the requirement of memory. As per Moore's law and Dennard's scaling theory, number of transistors per unit chip has been doubled every 18 months with the advantages of low power as well as high speed. However, the overall system performance which depends on the interaction between the processor and memory did not improve at the same speed due to a lack of innovation in the memory segment. So, in recent decades, a lot of research has been done on the improvement of speed and density of memory for high power as well as low power applications. Although the conventional 1T-1C Dynamic Random Access Memory has dominated the market for a sufficiently long time, the unscalable nature of the capacitor along with the short channel effects, dielectric leakage, gate induced drain leakage, diode leakage affect the performance of the device significantly. This begs to look into the possibilities of using different device architectures such as using the body of transistor itself (1T) to store the charges in order to overcome the difficulties faced by 1T-1C DRAM. The conventional partially depleted and fully depleted structures have been studied and shown promises as 1T-DRAM. However, integration of processor along with memory on the same chip for low power and high-speed application requires devices that can offer more than simple logic implementation. Thus, the thesis work focuses on an energy-efficient device, Reconfigurable Field Effect Transistor Tunnel (RFET) as 1T-DRAM, which can also be used for logic implementation with a lesser no of transistors due to its inherent reconfigurable nature.

RFET, which consists of Schottky Barrier (SB) at source/drain ends, utilizes tunneling phenomenon for its functioning. The difference with respect to SB-MOSFET is an extra gate, which controls the Schottky barrier width and also

suppresses the ambipolar behavior. The other gate i.e. control gate (CG), is manages the injection of carriers into the body. The higher values of on-current to off-current ratio coupled with reversible operation are some of the benefits of RFET vis-à-vis conventional MOSFET.

This work focuses on the use of twin gate (2G) RFET for 1T-DRAM purpose. Although a 2G-RFET can be utilized for implementing logic with reduced transistor count, the dynamic memory operation is not feasible as the storage region (potential well) is positioned near to the Schottky barrier. Through structural improvisations (through intentional gate misalignment) without degrading the current drive and retaining polarity control, the thesis work reports feasible dynamic memory operation in 2G-RFET for embedded (eDRAM) as well as standalone applications. The analysis presented in this work consists of device operation and physics of using 2G-RFET as 1T-DRAM highlights the feasibility of capacitorless dynamic memory operation for embedded applications with impressive performance indicators: sense margin ≥ 6 µA/µm, retention time ≥ 16 ms at 85 °C, current ratio of nearly 4 orders along with a low write (~1 ns) and read (~2 ns) time. Scalability of biases and total source-to-drain length are also examined and presented to highlight the design guidelines for implementing eDRAM cell with 2G-RFET.

LIST OF PUBLICATIONS

A. Peer-reviewed Journals:

1. **A. S. Roy**, S. Semwal and A. Kranti, "An Insightful Assessment of 1T-DRAM With Misaligned Polarity Gate in RFET," *IEEE Transactions on Electron Devices*, 69, no. 6, pp. 3163-3168 (2022).

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NOMENCLATURE

L_G	*Gate length*	*nm*
L_T	*Total length*	*nm*
T_{box}	*Buried oxide thickness*	*nm*
I_{ON}	*On-current*	*mA*
I_{OFF}	*Off-current*	*nA*
I_{ON}/I_{OFF}	*On-current to off-current ratio*	*Unitless*
C_S	*Storage capacitor*	*F*
C_B	*Bit-line parasitic capacitor*	*F*
V_{REF}	*Reference voltage*	*V*
V_{Th}	*Threshold voltage*	*V*
V_{DD}	*Supply voltage*	*V*
V_{CB}	*Bit-line voltage*	*V*
V_G	*Gate voltage*	*V*
V_D	*Drain voltage*	*V*
E_0	*Energy of free space*	*eV*
E_F	*Energy of Fermi level*	*eV*
E_g	*Bandgap of the semiconductor*	*eV*
Φ_s	*Work function of semiconductor*	*eV*
Φ_m	*Work function of metal*	*eV*
Φ_n	*Work function of n-type semiconductor*	*eV*
Φ_p	*Work function of p-type semiconductor*	*eV*
χ_s	*Electron affinity of semiconductor*	*eV*
$\chi_{s,n}$	*Electron affinity of n-type semiconductor*	*eV*
$\chi_{s,p}$	*Electron affinity of p-type semiconductor*	*eV*
q	*Electronic charge*	*C*
V_{bi}	*Built-in potential*	*V*
$\Phi_{B,n}$	*Schottky barrier height in the n-type semiconductor*	*eV*
$\Phi_{B,p}$	*Schottky barrier height in the p-type semiconductor*	*eV*

V_{AP}	*Applied forward bias*	*V*
J_{TE}	Current density of thermionic emission	$\mu A/m^2$
T	*Temperature*	*K*
*m**	*Effective mass of carrier*	*kg*
m_o	*Unit effective mass*	*kg*
m_n*	*Effective mass of electron*	*kg*
m_p*	*Effective mass of hole*	*kg*
h	*Planck's constant*	m^2kg/s
k	*Boltzmann's constant*	*J/K*
V_{FB}	*Flatband voltage*	*V*
T_{ox}	*Gate oxide thickness*	*nm*
T_{Si}	*Silicon body thickness*	*nm*
V_{DS}	*Drain to source voltage*	*V*
V_{PG}	*Polarity gate voltage*	*V*
V_{CG}	*Control gate voltage*	*V*
V_{BG}	*Back gate voltage*	*V*
V_S	*Source voltage*	*V*
L_{PG}	*Length of polarity gate*	*nm*
L_{CG}	*Length of control gate*	*nm*
L_{GAP}	*Length of ungated gap region between PG and CG*	*nm*
L_{SP}	*Spacing of back gate from drain*	*nm*
L_S	*Source metal length*	*nm*
L_D	*Drain metal length*	*nm*
L_{BG}	*Back gate length*	*nm*
L_{FGAP}	*Ungated gap length between PG and CG at top*	*nm*
L_{BGAP}	*Ungated gap length between BG and CG at bottom*	*nm*
L_T	*Length of Silicon between source and drain*	*nm*
$T_{n,p}$	*Tunneling probability*	*Unitless*
I_D	*Drain to source current*	*μA*
I_1	*Read '1' state current*	*μA*
I_0	*Read '0' state current*	*μA*

t_W	*Write time*	*ns*
t_R	*Read time*	*ns*
$V_{BG,read}$	*Back gate voltage in Read operation*	*V*
$V_{BG,hold}$	*Back gate voltage in Hold operation*	*V*
$V_{PG,hold}$	*Program gate voltage in Hold operation*	*V*
$V_{CG,hold}$	*Control gate voltage in Hold operation*	*V*
$V_{S,D,hold}$	*Source and Drain voltage in Hold operation*	*V*
S	*Sensitivity*	*Unitless*
D_{it}	*Interface trap density*	$cm^{-2}\ eV^{-1}$

ACRONYMS

SOI	*Silicon-on-insulator*
MOSFETs	*Metal Oxide Semiconductor Field-Effect Transistors*
FET	*Field-Effect Transistor*
MOS	*Metal Oxide Semiconductor*
n-MOS	*n-type MOS structure*
p-MOS	*p-type MOS structure*
ICs	*Integrated Circuits*
SCEs	*Short Channel Effects*
DIBL	*Drain Induced Barrier Lowering*
CMOS	*Complementary MOS*
RAM	*Random Access Memory*
SRAM	*Static RAM*
DRAM	*Dynamic RAM*
eDRAM	*Embedded DRAM*
WL	*Word Line*
BL	*Bit Line*
RT	*Retention Time*
SM	*Sense Margin*
CR	*Current Ratio*
BTBT	*Band-to-band-tunnelling mechanism*
PDSOI	*Partially Depleted SOI*
FDSOI	*Fully Depleted SOI*
SiO_2	*Silicon dioxide*
SB	*Schottky Barrier*
SB-MOSFET	*Schottky Barrier Metal Oxide Semiconductor Field-Effect Transistor*
SBH	*Schottky barrier height*
BH	*Barrier height*

n	*Donor type*
p	*Acceptor type*
n^+	*Heavily doped donor type*
p^+	*Heavily doped acceptor type*
S/D	*Source or Drain*
RFET	*Reconfigurable Field Effect Transistor*
PG	*Polarity Gate*
CG	*Control Gate*
n-RFET	*n-type Reconfigurable Field Effect Transistor*
p-RFET	*p-type Reconfigurable Field Effect Transistor*
2G-RFET	*Twin Gated Reconfigurable Field Effect Transistor Structure*
3G-RFET	*Three Gate Reconfigurable Field Effect Transistor Structure*
NiSi	*Nickel silicide*
DG	*Double Gate*
RDF	*Random Dopant Fluctuation*
Si	*Silicon*
TCAD	*Technology Computer-Aided Design*
VLSI	*Very Large Scale Integration*
VB	*Valence Band*
CB	*Conduction Band*
BG	*Back gate*
TUN	*Tunneling mechanism*
$T_{n,p}$	*Tunneling Probability*

Chapter 1

Introduction

1.1 Motivation for Memory

In the last few decades, the requirement for semiconductor devices has increased significantly owing to its vast inclusion in various industries. The devices have been scaled down to improve functionalities through an increase in speed and density, and decrease in power dissipation. This concept of scaling was guided by Moore's law [1-2] along with the scaling theory proposed by Dennard et al. [3]. Gordon Moore, in 1965, postulated that the no of transistors per unit chip would double every year, which, later was revised to 18 months [2]. This eventually became Moore's law. As per the proposed scaling theory by Dennard et al. [3], as the devices shrunk, they consume less power and run fast. Both of these laws have governed the scaling of semiconductor devices resulting in efficient and fast [4-9] transistors over the years.

Throughout the years, the processors have been improved in three specific metrics: speed, area and power. Thus, overall achievement of processors has enhanced multifold. However, the memory design has been aimed toward cost-effectiveness mainly. The improved designs of the processors have increased the burden on the memory designs as the number of controllers per processor core has decreased [10-11]. As a result, due to lack of innovation specifically in the area of interaction between the processor and memory, the overall performance of the system did not improve significantly at the same rate. That is why, in the last decade, much focus has been given towards the memory design and performance improvement.

As we have moved through the age of Artificial Intelligence (AI), Machine Learning and Big Data, the number of computations have increased significantly. Thus, the requirement of memory has also increased. These applications have encouraged the development of various memory technologies [12-21] in the past few years. To bridge the gap between speed of processor and access time of memory, the embedded applications where the

memory systems are incorporated along with logic devices on Integrated Circuits (ICs) chips are also gaining enough attention compared to standalone applications [22-25]. The typical performance parameters of memory are sense margin, retention time, endurance, reliability, current ratio, power consumption and stability [19]. Based on the requirements, the trade-offs are necessary among these metrics, and hence, optimization of the memory in all aspects is crucial to design.

Based on the retention of data, the solid-state memory can be grouped into two types – volatile memory and non-volatile memory. Volatile memories cannot retain data once the power is off. The Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM) come under this category. Non-Volatile Memory (NVM) can retain the data even the power is off. Non-volatile Random Access Memory (NVRAM), Electrically Erasable Programmable Read Only Memory (EEPROM), Flash Memory are representations of NVM. Apart from these, new emerging technologies such as Resistive RAM (RRAM), Ferroelectric RAM (FeRAM) etc. based devices are also becoming popular.

1.2 Motivation for DRAM

The first DRAM was introduced by Robert Dennard in 1967 where one access transistor (1T) was used to access the charge stored in the storage capacitor(1C) [3]. A patent was filed in 1967 for 1T-1C based DRAM and was issued in 1968 [26]. In early 70's, Intel introduced 3 transistors (3T) and 1 capacitor based 1KB DRAM for commercial use [27]. However, soon 1T-1C based DRAM became much popular and have been an integral part from then throughout the history in revolutionizing the use of computers and reduction in size from the size of a room to our palms.

DRAM is a cost-effective, high speed, robust memory which can attain high density with low power requirement [28-34]. However, due to significant innovation in the past decades, NAND flash memory dominates non-volatile memory segment. Hence, DRAM also needs to compete with cheap and low power NAND flash memory [25]. The continuous requirement of DRAM to be of much denser with low power have driven the innovation so far and the

DRAM technology itself has changed significantly [17]. The requirement of just main memory today has increased in multiple times compared to what it was just 10 years ago. This trend continues to shape the future of memory industry and thus architectural improvements are needed to counter that requirement.

1.3 Working of 1T-1C DRAM

Both SRAM and DRAM have seen tremendous growth [10-11, 16-17] in the last few decades due to innovation and rapid scaling. However, DRAMs have emerged as victorious in remaining at the top of memory hierarchy as its application in main memory in all computer systems apart from other vast applications [17]. The high density and thus, low cost per bit data have helped it to beat other type of memories. In DRAM, periodic refreshing is needed to retain the charge stored in the capacitor. That is why it is dynamic in nature. Each bit stored in DRAM can be accessed separately or randomly. That is why it is random access. SRAM also is random access but it does not need continuous refreshing to store the data. As long as the power is supplied, SRAM can retain the data [11, 16]. That is why the name 'static' comes. Both of these memories are volatile in nature i.e., when the power is turned-off, they lose the stored data. SRAM is generally used for high-speed applications and due to limited density, its use is mainly limited to on chip cache memory [11]. DRAM on the other hand found its application in main memory, and also in certain cases, as embedded cache memory [11, 24, 35]. Typical memory operation can be divided into 3 parts - write, hold and read. For DRAM, the operations are described below [36-38].

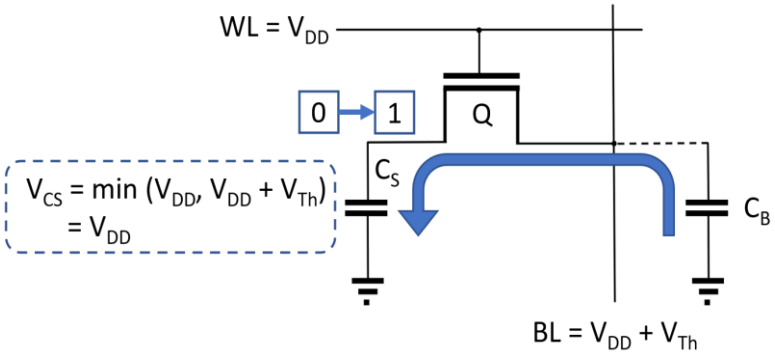


Fig. 1.1 Write '1' operation of 1T-1C DRAM.

For write ‘1’, charges are stored in the capacitor through access capacitor. For that, at first, the bit line (BL) is precharged up to V_{DD}, and then the word line (WL) is connected to V_{DD}. This facilitates the access transistor to be on, and the capacitor starts charging towards V_{DD}. However, due to weak pull up nature of nMOS, the capacitor can only be charged up to $V_{DD} – V_{Th}$ (min (V_{DD}, V_{DD} - V_{Th}) = V_{DD} - V_{Th}) where V_{Th} is the threshold voltage. Thus, to overcome this, the BL is precharged to V_{DD} + V_{Th}. Hence, the capacitor can charge up to V_{DD} and store the charges [36-38]. This is shown in Fig 1.1.

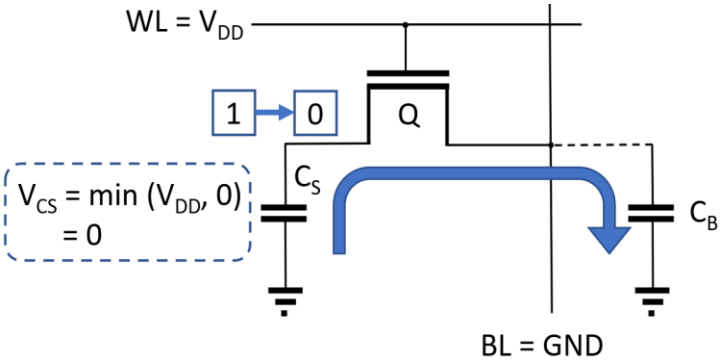


Fig. 1.2 Write ‘0’ operation of 1T-1C DRAM.

For write ‘0’ operation the charges stored in the capacitor, if any, are removed. That is why, here, at first the BL are first grounded and then the word line is activated through the application of a higher bias which is generally the supply voltage (V_{DD}) to WL [36-38]. Due to strong pull-down nature of nMOS, the capacitor is discharged to ground voltage (min (0, V_{DD} - V_{Th}) = 0) through the access transistor which is shown in Fig 1.2.

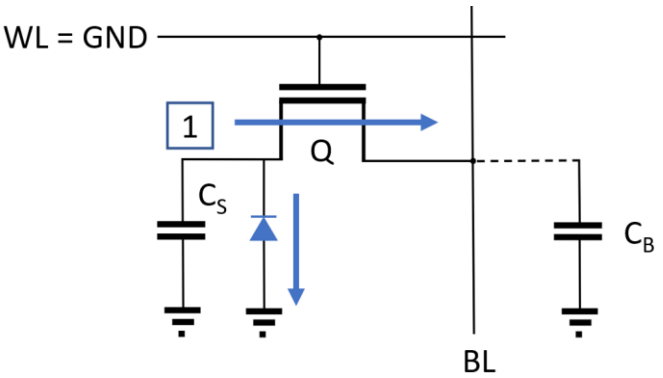


Fig. 1.3 Hold operation of 1T-1C DRAM. The arrows denote the leakage of charges.

In hold operation, irrespective of the bit line voltage the word line is kept grounded. As a result, the access transistor becomes off. Hence, ideally, the capacitor would retain the charges for infinite time. However, practically, due to leaky nature of the capacitor, n^+-p junction leakage current at the storage capacitor end and subthreshold current of the transistor, the charges are leaked away from the capacitor [36-38]. That is why the capacitor is periodically refreshed every 64 ms [9] i.e., the stored value in the capacitor is read and then written back. This is known as 'Refreshing'. The hold operation is shown in Fig 1.3.

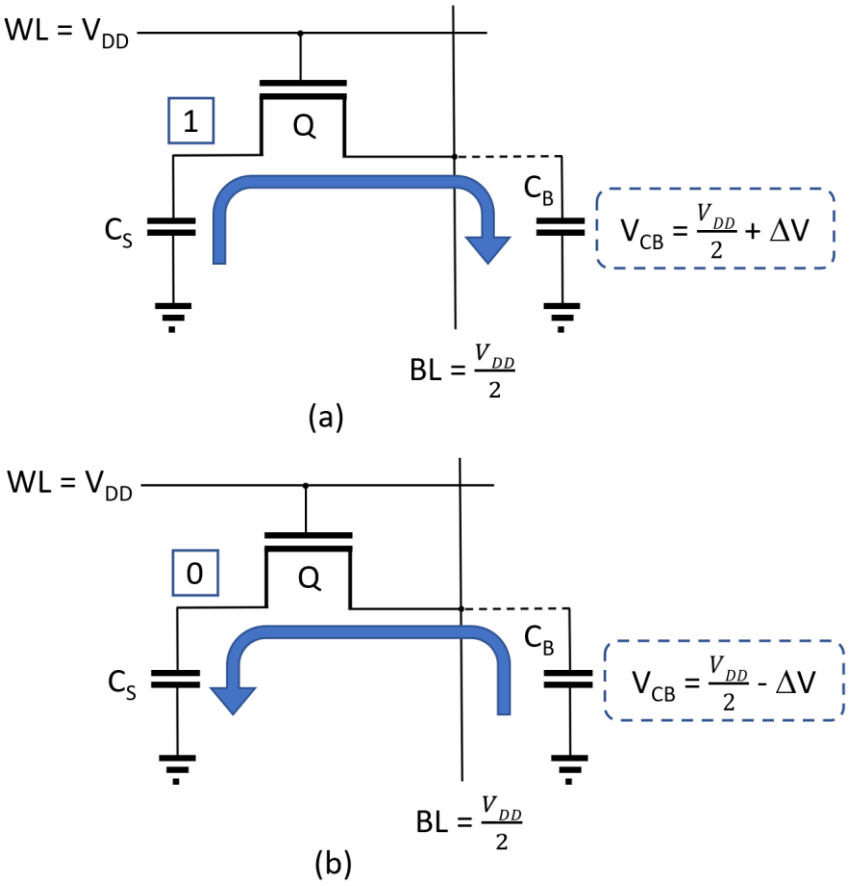


Fig. 1.4 (a) Read '1' and (b) Read '0' operation of 1T-1C DRAM.

The read operation is shown in Fig. 1.4 (a)-(b). Initially, the bit line is precharged to half of the supply voltage i.e. $V_{DD}/2$. Thereafter, WL is activated by connecting it to V_{DD}. Thus, if '1' is stored in the storage capacitor (C_S), bit line parasitic capacitor (C_B) starts getting charged through the access transistor and the voltage level of C_B increases (Fig. 1.4 (a)). However, if '0' is stored in storage capacitor, C_B gets discharged through the access transistor.

Hence, voltage level at the C_B decreases (Fig. 1.4 (b)). By using a sense amplifier, the changed voltage level of bit line is compared with reference voltage ($V_{REF} = V_{DD}/2$). If the bit line voltage is greater than $V_{DD}/2$ then it is decided that '1' was stored in C_S otherwise '0' was stored. During read, charges stored in the capacitor are lost due to the inherent mechanism of it. Thus, write back mechanism is used to impose the decided voltage level ('1' or '0') in the storage capacitor and restore the voltage level. That is why the read process is destructive in nature for 1T-1C DRAM [36-38].

1.4 1T-1C DRAM: Evolution

In order to increase the density of DRAM in chip, the access transistor as well as the storage capacitor has been scaled. However, as the scaling of capacitor continues, the storing capability also decreases. Hence, complex architecture for capacitor been introduced [10, 22, 39]. In the initial era, the planar capacitor used for storage was put at the adjacent of the access transistor and consumed 30% of the unit cell area. Thus, the scalability was a big problem [28]. Thus, instead of planar capacitor trench capacitor was introduced [40]. Here, the trench was formed in the substrate itself. However, the fabrication complexity also increased. Also, the high-k dielectric needed for better insulation in capacitor was hard to be formed using this process [10, 41]. Hence, the concept of stack capacitor was introduced [42]. The stack capacitor is fabricated above the substrate in way that reduces the overhead area to increase the device integrity. However, the increased fabrication complexity increases the cost [10]. Also, the dielectric leakage of the capacitor has always been an issue. As the transistors are scaled down to nanometer regime, different effects such as short channel effects and gate induced drain leakage can possibly increase leakage current in DRAM, and thus, operating speed is compromised [10-11, 30-33]. As a result, to improve reliability, in fact higher capacitor area is needed. That means, even though the access transistor is scalable, actually, for charge retention in the capacitor, a higher area and storage capability are needed. These drawbacks motivate the innovation in DRAM design by removing the capacitor altogether and store the charges in the body of the capacitor itself and thus conceptualizing 1T-capacitorless DRAM (1T-DRAM) [43].

1.5 1T-capacitorless DRAM

The use of storage capacitor (3D cell) and transistor arrangement in a vertical array can resolve the problems associated with 1T-1C DRAM. However, the fabrication complexity increases in that case. Hence, the body of the transistor (1T) itself can be used to store the charges. Since no capacitor is being used, the scalability issue is removed compared to conventional 1T-1C DRAM. As a result, the fabrication complexity and cost both can be reduced. The concept of 1T-capacitorless DRAM was proposed more than 20 years ago [44] and since then several architectures such as Partially-Depleted (PD) SOI MOSFET [45]–[56], Fully Depleted (FD) SOI [57]–[65], Advanced-RAM (A-RAM) [66]–[68], A2RAM [69]–[73], Zero-Slope and Zero-Impact Ionization FET (Z2-FET) [74]–[80], Field Effect Diode (FED) [81]–[85], Tunnel Field Effect Transistor (TFET) [86]–[96], Impact Ionization (IMOS) [97-98], Junctionless (JL) [99-100], Raised Source and Drain MOS [101], 3-Gated RFET [102] based 1T-capaciorless DRAM have been proposed.

In 1T-DRAM, the charges stored in the body of the transistor changes the threshold voltage of the device through floating-body effect [103-104]. Due to this change in threshold voltage, and hence, on-current changes in both conditions. As a result, a considerable difference between the currents of the two states is observed. This difference can distinguish between state ‘1’ and ‘0’. Also, the charges that are retained during hold operation are not lost during the read operation, and thus, the read operation is non-destructive in nature here. Other advantages associated with it are high density due to removal of capacitor, low cost of fabrication due to use typical SOI logic process [105], excellent delay-power trade-off along with advantages of use of multigate architectures [106-108].

Although the simple structure of 1T-capacitorless DRAM even though makes the fabrication much more easy, architectural and bias related optimizations are necessary for both applications, standalone and embedded. The retention time (RT) of memory is defined as the hold time at which the difference between state ‘1’ and state ‘0’ read currents become half of that of the difference value at very low hold time [64, 86-88, 101]. The sense margin (SM), on the other hand, is the difference between state ‘1’ and state ‘0’ read

currents at a very low hold time [64, 86-89, 100]. The current ratio (CR) of memory is the ratio of read currents for states ‘1’ and ‘0’. For better DRAM performance higher values of SM, RT and CR are desired. Requirements for RT are different for each application [109-110]. Although, static RAM dominates segments of on-chip memory, the eDRAMs are being developed for cheap, high density and low power applications. The 1T-capacitorless DRAM being a competitive candidate for that, requires additional attention.

1.6 Operation of 1T-capacitorless DRAM

1.6.1 Write ‘1’ Operation

In 1T-DRAM, the write ‘1’ operation is performed by generating holes in the body. The generation of holes can be done using different mechanisms such impact ionization [49,52,63-64,106,111-113], bipolar action [116-118], band-to-band tunneling [93-95] etc. Some of them are discussed below.

➢ **Impact Ionization Based:** The impact ionization based [49,54,67-64,106,111-113] hole generation depend on avalanche breakdown in which electron-hole pairs (EHPs) are generated upon applying enhanced field in the device [114]. The positive voltage at the drain attracts the generated electrons, while the holes are stored at the lower potential region. In order to invert the whole channel, a sufficient gate voltage needs to be applied here. Upon applying a high drain voltage at this condition, the electrons accelerate towards drain and causes collision and thus EHPs are generated. Even though this mechanism is fast and low power, the high applied drain bias may cause reliability issues [115]. The same is represented in Fig. 1.5.

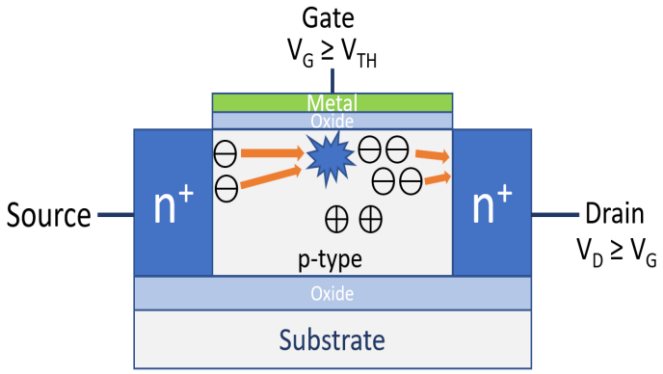


Fig. 1.5 Illustration of write ‘1’ operation through impact ionization.

➢ **Bipolar Action Based**: In this mechanism [116-118], impact ionization along with a positive feedback help to generate a lot of EHPs within a very short time which is shown in Fig. 1.6. Here, the parasitic BJT present in MOSFET configuration helps in generation. Due to impact ionization near the drain terminal, the EHPs are generated among which the holes accumulate at the lower potential region (back surface) which enhances the potential of the body and forward biases parasitic emitter (source) – base (body) junction. This reduces the energy barrier at the source-body region allowing more no of electrons to be injected in the body. Due to the applied field between source and drain, these electrons rush toward the drain and cause more impact ionization. This parasitic bipolar action improves the speed of the write operation. But still, we need sufficient drain bias to trigger impact ionization which may cause reliability issues [115] as before.

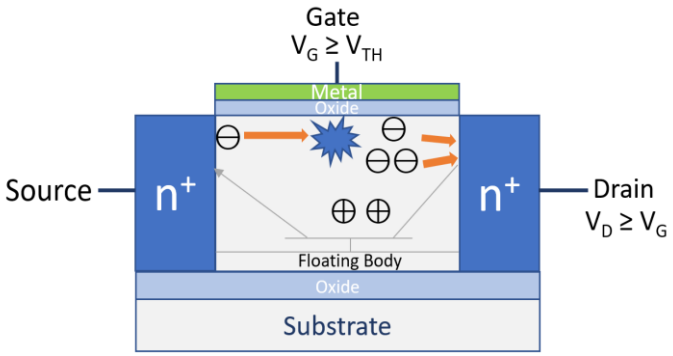
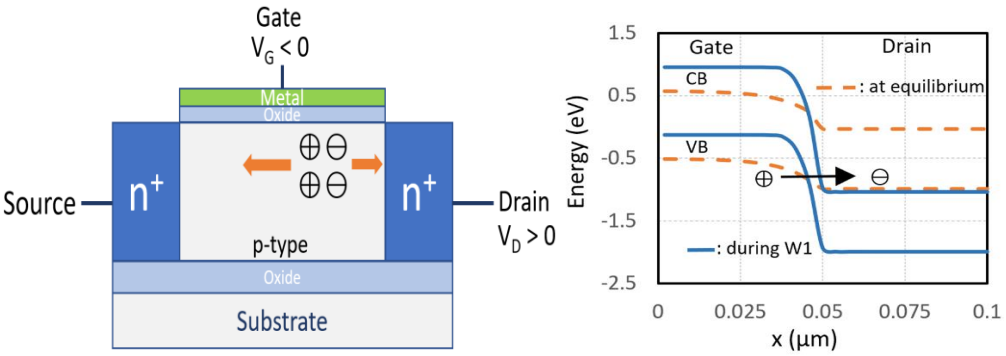


Fig. 1.6 Schematic diagram of write '1' operation through bipolar action.

➢ **Band-to-band Tunneling (BTBT) Based**: Band-to-band tunneling based devices operate by using a combination of positive drain bias and negative gate voltage. This creates a high electric field region and reduces the tunneling width between gate and drain by reverse biasing this region [89-91]. As a result, the tunnelling of electrons takes from channel valence band to drain conduction band. This creates holes in the channel region which are then accumulated in the potential well [91]. This tunneling can also be classified as Gate Induced Drain Leakage (GIDL) [56]. Due to very small current requirement, this process is much more power efficient and reliable than the previously discussed methods [92]. The process is represented in Fig. 1.7 (a)-(b).



(a) (b)

Fig. 1.7 (a) Schematic diagram of write '1' operation through BTBT mechanism and (b) EHP generation through BTBT in write '1' at gate-drain region.

1.6.2 Write '0' Operation

The removal of holes from the body takes place in write '0' operation. This is accomplished by applying a positive gate bias and negative drain voltage. This causes the body-drain and body-source regions to be forward biased, and thus, the holes are removed from the body [27]. This forward bias causes the electrons to enter from source/drain to the storage region and electron-hole recombination occurs depleting holes from the body. This is shown in Fig. 1.8.

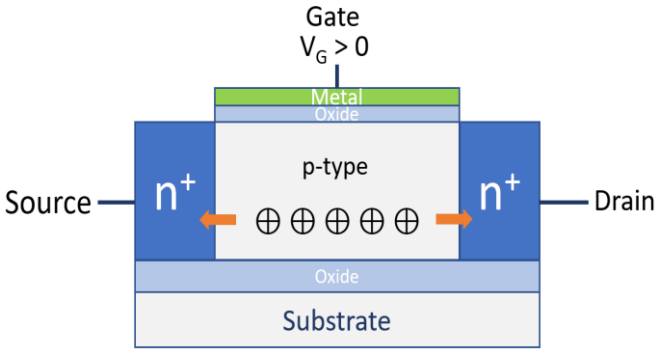


Fig. 1.8 Illustration of hole depletion in write '0' operation.

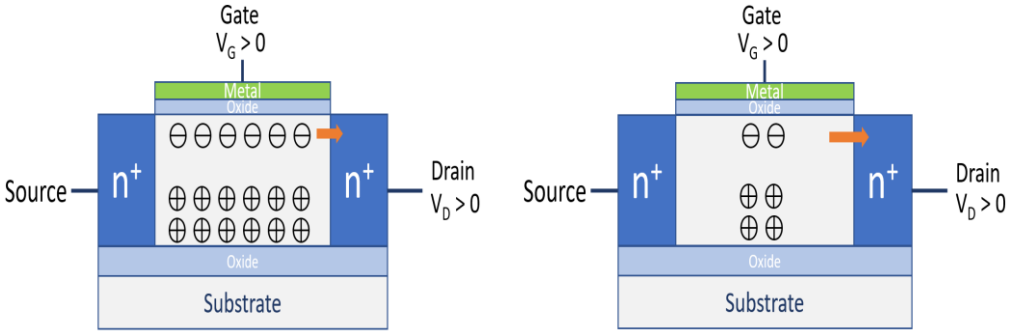
1.6.3 Hold Operation

In hold operation, the holes which are generated or depleted in the write operation are retained. This charge retention depends upon hole recombination and generation of holes which are function of device

architecture, bias and temperature [64, 86, 92]. The thermal generation, BTBT and weak impact ionization affect the hole generation, and thus, during the hold '0' the hole concentration stored in potential well increases [64, 86, 92]. On the contrary, with time, due to thermal recombination mainly, the hole concentration decreases during hold '1' [64, 86, 92]. Therefore, to maintain a high retention time along with high sense margin the bias along with device optimization are necessary to control hole generation and recombination.

1.6.4 Read Operation

In read operation, the holes that are stored in the body modify the body potential, and hence, alter the threshold voltage of the device. Therefore, when read operation is followed by hold '1' operation, excess holes present in the body increases the body potential and reduces the threshold voltage through body-effect. On the other hand, when read operation is followed by hold '0' operation, since holes were depleted, the threshold voltage is not impacted. As a result, when read current flows, we see clear difference between read '1' and read '0' currents which are then sensed by a sense amplifier to distinguish between state '1' and state '0' [64, 86-88, 102]. The read operations are illustrated in Fig. 1.9 (a)-(b).



(a) (b)

Fig. 1.9 Schematic representation of (a) read '1' and (b) read '0' operation in SOI devices.

The read current depends mainly upon read bias used and device architecture. Since the charges stored during hold operation are not lost during read operation (non-destructive read), the cell can be read multiple times after

programming. This capability reduces overall power requirement of 1T-DRAM compared to 1T-1C DRAM.

1.7 Conclusion

Research and innovation in the in the memory segment have introduced several devices [45-102] which are potential candidates for 1T-DRAM application. However, feasibility of the devices practically and integration have always been an issue. The SOI MOSFET based 1T-DRAM [45-65] have shown promise for standalone applications requiring a minimum retention time of 64 ms with sufficient sense margin. But for embedded applications, the devices need to support logic integration with improved scalability and operation. As the rapid growth of the semiconductor industry continues, we will need better architectures in that regards which can support highly dense, low power and fast operation. Thus, one can look into some other devices such as Reconfigurable (or Programmable or Polarity Controlled) Field Effect Transistor (RFET) which has already been proven to be a good alternative to traditional architectures, and look into the possibility of using it as 1T-DRAM.

1.8 Thesis Organization

The thesis organization is described as following:

Chapter 1 focuses on understanding of 1T-1C DRAM concepts and drawbacks associated with it. It provides an understanding of need of 1T-DRAM and concepts behind it. Finally, it emphasizes on the need of different architectures to obtain 1T-DRAM function.

Chapter 2 introduces the concepts of twin-gated reconfigurable field effect transistor and its operation. Associated advantages and disadvantages are also discussed in this chapter.

Chapter 3 presents the drawbacks of using conventional twin gated reconfigurable field effect transistor and proposes a novel structure to overcome the bottleneck of the issues. The operation of 1T-DRAM based on 2G-RFET is discussed here.

Chapter 4 provides detailed analysis of effects of different parameters such as read and write time scaling, bias variation, length scaling and use of different spacing lengths and traps at interfaces on device performance. A fair comparison of the device with the other reported devices is also discussed here.

Chapter 5 summarizes the conclusion of the research work and proposes the scope of the future work.

References

[1] Moore G. E. (1965), Cramming More Components onto Integrated Circuits, Electronics, 38, 114-116.

[2] Moore G. E. (1975), Progress in digital integrated electronics, IEEE Electron Devices Meeting, 21, 11-13.

[3] Dennard R. H., Gaensslen F. H., Rideout V. L., Bassous E. and LeBlanc A. R. (1974), Design of Ion-Implanted Small MOSFET‘s Dimensions with Very Small Physical Dimensions, IEEE Journal of Solid-State Circuits, 9, 256–268.

[4] Wong H.-S. P. (2002), Beyond the conventional transistor, IBM Journal of Research and Development, 46, 133-168.

[5] Chen T. C., (2006) Where CMOS is going: trendy hype vs. real technology, Proceedings of IEEE Solid-State Circuits Conference, pp. 1-18.

[6] Antoniadis D. A., Aberg I., Chleirigh C. N., Nayfeh O. M., Khakifirooz A., and Hoyt J. L. (2006), Continuous MOSFET performance increase with device scaling: The role of strain and channel material innovations, IBM Journal of Research and Development, 50, 363-376.

[7] Waldrop M. M. (2016), More than moore. Nature, 530, 144-148.

[8] Mandelman J. A., Dennard R. H., Bronner G. B., De Brosse J. K., Divakaruni R., Li Y., and Radens C. J. (2002), Challenges and future directions for the scaling of dynamic random-access memory (DRAM), IBM Journal of Research and Development, 46, 187-212.

[9] ITRS International Technology Working Groups. International Technology Roadmap for Semiconductors, http://www.itrs.net (2015).

[10] Joodaki, M., (2012) Selected advances in nanoelectronic devices: logic, memory and RF, Springer Science and Business Media, Heidelberg (ISBN- 978-3-642-31349-3).

[11] Keeth, B., Baker, J. R., Jacob, B., Lin, F., (2007) DRAM circuit design: fundamental and high-speed topics 2nd ed. John Wiley & Sons Inc., New Jersey (ISBN- 978-0-4701-8475-2).

[12] Fujisaki Y. (2013), Review of emerging new solid-state non-volatile memories, Japanese Journal of Applied Physics, 52, 040001.

[13] Freitas R. F., and Wilcke W. W. (2008), Storage-class memory: The next storage system technology, IBM Journal of Research and Development, 52, 439-447.

[14] Burr G. W., Kurdi B. N., Scott J. C., Lam C. H., Gopalakrishnan K., and Shenoy R. S. (2008), Overview of candidate device technologies for storageclass memory, IBM Journal of Research and Development, 52, 449-464.

[15] Brewer J. E., Zhirnov V. V., and Hutchby, J. A. (2005), Memory technology for post CMOS era, IEEE Circuits and Devices Magazine, 21, 13-20.

[16] Coughlin T. (2014), Thanks for the memories: Nonvolatile memory technology enables the age of spin [The art of storage], IEEE Consumer Electronics Magazine, 3, 85-92.

[17] Adee S. (2009), Thanks for the memories. IEEE Spectrum, 46.

[18] Endoh T., Koike H., Ikeda S., Hanyu T. and Ohno H. (2016), An Overview of Nonvolatile emerging memories—Spintronics for working memories, IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 6, 109-119.

[19] Chen A. (2016), A review of emerging non-volatile memory (NVM) technologies and applications, Solid-State Electronics, 125, 25-38.

[20] Sun G., Zhao J., Poremba M., Xu, C., and Xie, Y. (2017), Memory that Never Forgets: Emerging Non-volatile Memory and the implication for architecture design, National Science Review, 1-16.

[21] Kim H., Hwang S., Lee J. H., and Park B. G. (2017), Combination of volatile and non-volatile functions in a single memory cell and its scalability, Japanese Journal of Applied Physics, 56, 04CE06.

[22] Zhang, K., (2009) Embedded memories for nano-scale VLSIs, Springer Science and Business Media, Oregon (ISBN 978-0-387-88496-7).

[23] Ghosh S., (2014) Tutorial t6b: Embedded memory design for future technologies: Challenges and solutions, Proceedings of 27th International Conference on VLSI Design and 13th International Conference on Embedded Systems, pp. 14-15.

[24] Itoh K. (2011), Embedded memories: Progress and a look into the future, IEEE Design & Test of Computers, 28, 10-13.

[25] Kim K. (2005), Technology for sub-50nm DRAM and NAND flash manufacturing, IEEE Electron Devices Meeting, pp. 323-326.

[26] Dennard R. H. (1968), Field-effect transistor memory, U.S. Patent 3387286.

[27] Ohsawa, T., Hamamoto, T., (2012) A Novel Capacitor-less DRAM: Floating Body Cell, CRC Press, Taylor & Francis Group, Florida, (ISBN: 978-9-81430-308-8).

[28] Itoh K. (2008), The history of DRAM circuit designs–at the forefront of DRAM development, IEEE Solid-State Circuits Society Newsletter, 13, 27-31.

[29] Kim K. (2000), Perspectives on giga-bit scaled DRAM technology generation, Microelectronics reliability, 40, 191-206.

[30] Itoh K., Nakagome Y., Kimura S. I., and Watanabe T. (1997), Limitations and challenges of multigigabit DRAM chip design, IEEE Journal of Solid-State Circuits, 32, 624-634.

[31] Kim K., Hwang C. G., and Lee J.G., (1998), DRAM technology perspective for gigabit era, IEEE Transactions on Electron Devices, 45, 598-608.

[32] Itoh K., Sasaki K., and Nakagome Y., (1995) Trends in low-power RAM circuit technologies, Proceedings of the IEEE, 83, 524-543.

[33] Itoh K., Watanabe T., Kimura S. I., and Sakata, T., (2000), Reviews and prospects of high-density RAM technology, International Semiconductor Conference, pp. 13–22.

[34] Comfort J. H., (1999) DRAM Technology: outlook and challenges, Proceedings of IEEE International Conference on VLSI and CAD, 99, pp. 182–186.

[35] Kim K., and Lee S. Y., (2007) Memory technology in the future, Microelectronic Engineering, 84, 1976-1981.

[36] Sharroush S. M. (2016), Performance optimization of 1T-1C DRAMs: A quantitative study, Microelectronics Journal, 52, 147-164.

[37] Faul J. W., and Henke, D. (2005), Transistor challenges–A DRAM perspective. Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 237, 228-234.

[38] Sunami H. (2008), The role of the trench capacitor in DRAM innovation, IEEE Solid-State Circuits Society Newsletter, 13, 42-44.

[39] Kurinec, S.K. and Iniewski K., (2013) Nanoscale semiconductor memories: Technology and applications, CRC Press, Taylor & Francis Group, Florida (ISBN-978-1-4665-6061-1).

[40] Sunami H. (2008), The role of the trench capacitor in DRAM innovation, IEEE Solid-State Circuits Society Newsletter, 13, 42-44.

[41] Lee S. H., (2016) Technology scaling challenges and opportunities of memory devices, Proceedings of IEEE Electron Devices Meeting, pp. 1-8.

[42] Koyanagi M. and Hashimoto N. (1979), Novel high density, stacked capacitor MOS RAM, IEEE International Electron Devices Meeting, 24, pp. 348 - 351.

[43] Tack M. R., Gao M., Claeys C. L. and Declerck G. J. (1990), The multistable charge-controlled memory effect in SOI MOS transistors at low temperatures, IEEE Transaction on Electron Devices, 31, 1373–1382.

[44] H.-J. Wann. and C. Hu., (1993) A capacitorless DRAM cell on SOI substrate, Proceedings of IEEE International Electron Devices Meeting (IEDM), pp 635–638.

[45] Okhonin S., Nagoga M., Sallese J. M. and Fazan, P. C., (2001) A SOI capacitor-less 1T-DRAM concept, Proceedings of IEEE International SOI Conference, pp. 153-154.

[46] Blagojevic M., Kayal M., Pastre M., Harik L., Declercq M. J., Okhonin S., and Fazan P. C. (2006), Capacitorless 1T DRAM Sensing Scheme With Automatic Reference Generation, IEEE Journal of Solid-State Circuits, 41, 1463–1470.

[47] Ban I., Avci U. E., Shah U., Barns C. E., Kencke D. L., and Chang P., (2006) Floating Body Cell with Independently-Controlled Double Gates for High Density Memory, Proceedings of IEEE International Electron Devices Meeting (IEDM), pp 1–4.

[48] Bae D. Il., Kim S., and Choi Y. K. (2009), Low-cost and highly heat controllable capacitorless PiFET (Partially insulated FET) 1T DRAM for embedded memory, IEEE Transactions on Nanotechnology, 8, 100–105.

[49] Cao C.-W., Zang S.-G., Lin X., Sun Q.-Q., Xing C., Wang P.-F., and Zhang D. W. (2012), A Novel 1T-1D DRAM Cell for Embedded Application IEEE Transaction on Electron Devices, 59, 1304–1310.

[50] Yoshida E., and Tanaka T. (2006), A capacitorless 1T-DRAM technology using gate-induced drain-leakage (GIDL) current for low-power and high-speed embedded memory, IEEE Transactions on Electron Devices, 53, 692–697.

[51] Kuo C., King T. J., and Hu C. (2003), A capacitorless double gate DRAM technology for sub-100-nm embedded and stand-alone memory applications, IEEE Transactions on Electron Devices, 50, 2408-2416.

[52] Ohsawa T., Fujita K., Hatsuda K., Higashi T., Shino T., Minami Y., Nakajima H., Morikado M., Inoh K., Hamamoto T., Watanabe S., Fujii S., and Furuyama T. (2006), Design of a 128-Mb SOI DRAM Using the Floating Body Cell (FBC), IEEE Journal of Solid-State Circuits, 41, 135–145.

[53] Ohsawa T., Fujita K., Higashi T., Iwata Y., Kajiyama T., Asao Y., and Sunouchi K. (2002), Memory design using a one-transistor gain cell on SOI, IEEE Journal of Solid-State Circuits, 37, 1510–1522.

[54] Fossum J. G., Lu Z. and Trivedi V. P. (2007), New insights on “capacitorless” floating-body DRAM cells, IEEE electron device letters, 28, 513-516.

[55] Ryu S.-W., Han J.-W., Kim C.-J., Kim S., and Choi Y.-K. (2009), Unified random access memory (URAM) by integration of a nanocrystal floating gate for nonvolatile memory and a partially depleted floating body for capacitorless 1T-DRAM, Solid. State. Electron., 53, 389–391.

[56] Okhonin S., Nagoga M., Sallese J. M., and Fazan P. C. (2002), A capacitor-less 1T-DRAM cell, IEEE Electron Device Letters, 23, 85–87.

[57] Shin J. S., Bae H., Jang J, Yun D., Lee J., Hong E., Kim D. H., and Kim D. M. (2011), A Novel Double HBT-Based Capacitorless 1T DRAM Cell With Si/SiGe Heterojunctions, IEEE Electron Device Letters, 32, 850–852.

[58] Moon D. I., Choi S. J., Han J. W., Kim S., and Choi Y. K. (2010), Fin-width dependence of BJT-based 1T-DRAM implemented on FinFET, IEEE Electron Device Letters, 31, 909-911.

[59] Kim S., Choi S. J., Moon D. I., and Choi Y. K. (2012), Carrier lifetime engineering for floating-body cell memory, IEEE Transactions on Electron Devices, 59, 367-373

[60] Han J.-W., Ryu S.-W., Kim D.-H., Kim C.-J., Kim S., Moon D.-I., Choi S.-J., and Choi Y.-K. (2009), Fully depleted polysilicon TFTs for capacitorless 1T-DRAM IEEE Electron Device Letters, 30, 742–744.

[61] Zhou Z., Fossum J. G., and Lu Z. (2009), Physical insights on BJT-based 1T DRAM cells, IEEE Electron Device Letters, 30, 565-567.

[62] Lu Z., Fossum J. G., and Zhou Z. (2011), A floating-body/gate DRAM cell upgraded for long retention time, IEEE Electron Device Letters, 32, 731-733.

[63] Zhichao L., Fossum J. G., Ji-Woon Y., Harris H. R., Trivedi V. P., Min C., and Thompson S. E. (2009), A Simplified Superior Floating-Body/Gate DRAM Cell, IEEE Electron Device Letters, 30, 282–384.

[64] Butt N. Z., and Alam M. A. (2007), Scaling limits of double-gate and surround-gate Z-RAM cells, IEEE Transactions on Electron Devices, 54, 2255-2262.

[65] Giusi G., Alam M. A., Crupi F., and Pierro S. (2010), Bipolar mode operation and scalability of double-gate capacitorless 1T-DRAM cells, IEEE Transactions on Electron Devices, 57, 1743-1750.

[66] Rodriguez N., Gamiz F., and Cristoloveanu S. (2010), A-RAM memory cell: Concept and operation, IEEE Electron Device Letters, 31, 972-974.

[67] Rodriguez N., Cristoloveanu S., and Gamiz F. (2011), Capacitor-less A-RAM SOI memory: Principles, scaling and expected performance, Solid. State. Electron., 59, 44–49.

[68] Gamiz F., Rodriguez N., and Cristoloveanu S. (2012), 3D Trigate 1T-DRAM Memory Cell for 2x nm Nodes, In IEEE International Memory Workshop (IMW), pp 1–4.

[69] Rodriguez N., Navarro C., Gamiz F., Andrieu F., Faynot O., and Cristoloveanu S. (2012), Experimental Demonstration of Capacitorless A2RAM Cells on Silicon-on-Insulator, IEEE Electron Device Letters, 33, 1717–1719.

[70] Rodriguez N., Gamiz F., Navarro C., Marquez C., Andrieu F., Faynot O., and Cristoloveanu S. (2015), Experimental developments of A2RAM memory cells on SOI and bulk substrates, Solid. State. Electron., 103, 7–14.

[71] Wakam F. T., Lacord J., Martinie S., Barbe J.-C., Bawedin M., and Cristoloveanu S., (2017) Optimization guidelines of A2RAM cell performance through TCAD simulations, Proceedings of IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), pp 329–332.

[72] Gamiz F., Rodriguez N., Marquez C., Navarro C., and Cristoloveanu S., (2014) A2RAM: Low-power 1T-DRAM memory cells compatible with planar and 3D SOI substrates, Proceedings of IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp 1–2.

[73] Rodriguez N., Andrieu F., Navarro C., Faynot O., Gamiz F., and Cristoloveanu S., (2011) Properties of 22nm node extremely-thin-SOI MOSFETs, Proceedings of IEEE International SOI Conference (SOI), pp 1–2.

[74] Dirani H. El., Solaro Y., Fonteneau P., Legrand C. A., Marin-Cudraz D., Golanski D., Ferrari P., and Cristoloveanu S. (2016), A band-modulation device in advanced FDSOI technology: Sharp switching characteristics, Solid. State. Electron., 125, 103–110.

[75] Duan M., Adam-Lema F., Cheng B., Navarro C., Wang X., Georgiev V. P., Gamiz F., Millar C., and Asenov A., (2017) 2D-TCAD simulation

on retention time of Z2FET for DRAM application, Proceedings of IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), pp 325–328.

[76] Wan J., Royer C. Le., Zaslavsky A., and Cristoloveanu S. (2013), A systematic study of the sharp-switching Z2-FET device: From mechanism to modeling and compact memory applications, Solid. State. Electron., 90, 2–11.

[77] Navarro C., Duan M., Parihar M. S., Adamu-Lema F., Coseman S., Lacord J., Lee K., Sampedro C., Cheng B., Dirani H. El., Barbe J.-C., Fonteneau P., Kim S.-I., Cristoloveanu S., Bawedin M., Millar C., Galy P., Le Royer C., Karg S., Riel H., Wells P., Kim Y.-T., Asenov A., and Gamiz F. (2017), Z2 -FET as Capacitor-Less eDRAM Cell For High-Density Integration IEEE Transactions on Electron Devices, 64, 4904–4909.

[78] Parihar M. S., Lee K. H., Park H. J., Navarro C., Lacord J., Gamiz F., Galy P., Cristoloveanu S., and Bawedin M., (2018) Z2-FET memory matrix in 28 nm FDSOI technology, Proceedings of Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), pp 1–4.

[79] Navarro C., Lacord J., Parihar M. S., Adamu-Lema F., Duan M., Rodriguez N., Cheng B., Dirani H. El., Barbe J.-C., Fonteneau P., Bawedin M., Millar C., Galy P., Le Royer C., Karg S., Wells P., Kim Y.-T., Asenov A., Cristoloveanu S., and Gamiz F. (2017), Extended Analysis of the Z2-FET: Operation as Capacitorless eDRAM IEEE Transactions on Electron Devices, 64, 4486–4491.

[80] Jeon Y., Kim M., Lim D., and Kim S. (2015), Steep Subthreshold Swing n- and p-Channel Operation of Bendable Feedback Field-Effect Transistors with p+–i–n+ Nanowires by Dual-Top-Gate Voltage Modulation, Nano Letters, 15, 4905–4913.

[81] Avci U. E., Kencke D. L., and Chang P. L. D. (2012), Floating-Body Diode—A Novel DRAM Device, IEEE Electron Device Letters, 33, 161–163.

[82] Badwan A. Z., Chbili Z., Yang Y., Salman A. A., Li Q., and Ioannou D. E. (2013), SOI field-effect diode DRAM cell: Design and operation, IEEE Electron Device Letters, 34,1002-1004.

[83] Yang Y., Gangopadhyay A., Qiliang L., and Ioannou D. E., (2009) Scaling of the SOI field effect diode (FED) for memory application, Proceedings of IEEE International Semiconductor Device Research Symposium (SDRS), pp 1–2.

[84] Imamoto T., and Endoh T. (2014), Excellent scalability including self-heating phenomena of vertical-channel field-effect-diode type capacitor-less one transistor dynamic random access memory cell, Japanese Journal of Applied Physics, 53, 04ED05.

[85] Ma T. P., (2008) FEDRAM: A capacitor-less DRAM based on ferroelectric-gated field-effect transistor, Proceedings of IEEE International Conference on Solid-State and Integrated-Circuit Technology (ICSICT), pp 850–852.

[86] Navlakha N., Lin J.-T., and Kranti A. (2016), Improving retention time in tunnel field effect transistor based dynamic memory by back gate engineering, Journal of Applied Physics, 119, 214501.

[87] Navlakha N., and Kranti A. (2017), Overcoming the drawback of lower sense margin in tunnel FET based dynamic memory along with enhanced charge retention and scalability, Nanotechnology, 28, 445203.

[88] Biswas A., Dagtekin N., Grabinski W., Bazigos A., Le Royer C., Hartmann J. M., Tabone C., Vinet M., and Ionescu A. M. (2014), Investigation of tunnel field-effect transistors as a capacitor-less memory cell, Applied Physics Letters, 104, 092108.

[89] Navlakha N., Kranti A., and Lin J.-T., (2017) Optimization of back gate workfunction, alignment and bias for charge retention in TFET based DRAM, Proceedings of IEEE International Conference on Emerging Electronics (ICEE), pp 3–6.

[90] Navlakha N., and Kranti A. (2017), Insights into operation of planar tri-gate tunnel field effect transistor for dynamic memory application, Journal of Applied Physics, 122, 044502.

[91] Navlakha N., Lin J.-T., and Kranti A. (2016), Improved Retention Time in Twin Gate 1T DRAM with Tunneling based Read Mechanism, IEEE Electron Device Letters, 37, 1127-1130.

[92] Navlakha N., Lin J.-T., and Kranti A., (2017) Twin gate Tunnel FET based capacitorless dynamic memory, Proceedings of IEEE International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), pp 1–2.

[93] Navlakha N., Lin J.-T., and Kranti A., (2017) Retention and Scalability Perspective of sub-100-nm Double Gate Tunnel FET DRAM, IEEE Transactions on Electron Devices, 64, 1561-1567.

[94] Navlakha N., and Kranti A., (2018) Physical Insights on Junction Controllability for Improved Performance of Planar Trigate Tunnel FET as Capacitorless Dynamic Memory, Proceedings of IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), pp 129–132.

[95] Navlakha N., Lin J.-T., and Kranti A., (2017) Design optimization of tunnel FET for dynamic memory applications, Proceedings of IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), pp 1–3.

[96] Biswas A., and Ionescu A. M. (2015), 1T capacitor-less DRAM cell based on asymmetric tunnel FET design, IEEE Journal of the Electron Devices Society, 3, 217-222.

[97] Lahgere A., and Kumar M. J. (2017), 1-T Capacitorless DRAM Using Bandgap-Engineered Silicon-Germanium Bipolar I-MOS, IEEE Transactions Electron Devices, 64, 1583–1590.

[98] Lahgere A, and Kumar M. J. (2018), 1-T Capacitorless DRAM Using Laterally Bandgap Engineered Si-Si:C Heterostructure Bipolar I-MOS for Improved Sensing Margin and Retention Time, IEEE Transactions on Nanotechnology, 17, 543–551.

[99] Giusi G., and Iannaccone G. (2013), Junction Engineering of 1T-DRAMs. IEEE Electron Device Letters, 34, 408-410.

[100] Yoon Y.-J., Seo J.-H., Cho M.-S., Kim B.-G., Lee S.-H., and Kang I.-M. (2017), Capacitorless one-transistor dynamic random access

memory based on double-gate GaAs junctionless transistor, Japanese Journal of Applied Physics, 56, 06GF01.

[101] Ansari M. H. R. and Cho S. (2021), Performance Improvement of 1T DRAM by Raised Source and Drain Engineering, IEEE Transactions on Electron Devices, 68, 1577-1584.

[102] Bhuvaneshwari Y. V., and Kranti A. (2021), Enhancing multi-functionality of reconfigurable transistors by implementing high retention capacitorless dynamic memory, Semiconductor Science and Technology, 36, 115003.

[103] Shahidi G. G., Ajmera A., Assaderaghi F., Bolam R. J., Leobandung E., Rausch W., Sankus D., Schepis D., Wagner L. F., Kun W., and Davari B., (1999) Partially-depleted SOI technology for digital logic, Proceedings of IEEE International Solid-State Circuits Conference. Digest of Technical Papers (ISSCC), pp 426–427.

[104] Shahidi G. G., (2001) SOI technology for the GHz era, International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers, 46, 121–131.

[105] Almeida L. M., Sasaki K. R. A., Caillat C., Aoulaiche M., Collaert N., Jurczak M., Simoen E., Claeys C., and Martino J. A. (2013), Optimizing the front and back biases for the best sense margin and retention time in UTBOX FBRAM, Solid-State Electronics, 90, 149-154.

[106] Kuo C., King T. J., and Hu C. (2002), A capacitorless double-gate DRAM cell, IEEE Electron Device Letters, 23, 345-347.

[107] Yoshida E., Miyashita T., and Tanaka T. (2005), A study of highly scalable DG-FinDRAM, IEEE Electron Device Letters, 26, 655–657.

[108] Bawedin M., Cristoloveanu S., and Flandre D. (2008), A capacitorless 1T-DRAM on SOI based on dynamic coupling and double-gate operation, IEEE Electron Device Letters, 29, 795-798.

[109] Yang H.-Y., Chang C.-M., Chao M. C.-T., Huang R.-F., and Lin S.-C. (2012), Testing Methodology of Embedded DRAMs, IEEE Transactions on Very Large Scale Integration Systems, 20, 1715–1728.

[110] Ghosh S. (2014), Modeling of Retention Time for High-Speed Embedded Dynamic Random Access Memories, IEEE Transactions on Circuits Systems I: Regular Paper, 61, 2596–2604.

[111] Fazan P. C., Okhonin S., Nagoga M., and Sallese J. M., (2002) A simple 1-transistor capacitor-less memory cell for high performance embedded DRAMs, Proceedings of IEEE Custom Integrated Circuits Conference, pp. 99-102.

[112] Song K. W., Jeong H., Lee J. W., Hong S. I., Tak N. K., Kim Y. T., Choi Y. L., Joo H. S., Kim S. H., Song H. J., and Oh Y. C., (2008) 55 nm capacitor-less 1T DRAM cell transistor with non-overlap structure, Proceedings of IEEE Electron Devices Meeting, pp. 1-4.

[113] Almeida L. M., Aoulaiche M., Sasaki K. R. A., Nicoletti T., de Andrade M. G. C., Collaert N., Simoen E., Claeys C., Martino J. A., and Jurczak M., (2012) Comparison between low and high read bias in FB-RAM on UTBOX FDSOI devices, Proceedings of IEEE International Conference on Ultimate Integration on Silicon, pp. 61-64.

[114] Streetman, B. G., and Banerjee, S. K., (2009) Solid State Electronic Devices, sixth ed. Pearson Education Inc., New Jersey 07458, (ISBN-978-81 -203-3020-7).

[115] J.-P. Colinge, (1997) Silicon-on-Insulator Technology: Materials to VLSI. Boston, MA: Springer US (ISBN- 9781461347958).

[116] Okhonin S., Nagoga M., Carman E., Beffa, R., and Faraoni, E., (2007) New generation of Z-RAM, Proceedings of IEEE Electron Devices Meeting, pp. 925-928.

[117] Giusi G. (2014), Physical insights of body effect and charge degradation in floating-body DRAMs, Solid-State Electronics, 95, 1-7.

[118] Moon D. I., Choi S. J., Han J. W., Kim S., and Choi Y. K. (2010), Fin-width dependence of BJT-based 1T-DRAM implemented on FinFET, IEEE Electron Device Letters, 31, 909-911.

Chapter 2

Twin Gate Reconfigurable Transistor

2.1 Metal-Semiconductor Contacts

A junction formed by metal and semiconductor (M-S junction) can lead to a Schottky contact (rectifying) or Ohmic contact (non-rectifying) based on the work function difference and electron affinity of the materials used [1]. The energy required to move an electron from Fermi level (E_F) to vacuum level (E_0) is defined as the work function (Φ) of any material [1]. On the other hand, electron affinity of semiconductor (χ_s) is the energy difference between the conduction band edge (E_C) and vacuum level [1]. For metal, as the conduction band and Fermi energy level (Φ_m) overlap, the work function is same as the electron affinity. However, for semiconductor the location of Fermi energy level depends on doping. Therefore, the work function of semiconductor (Φ_s) also changes. However, as the electron affinity of semiconductor (χ_s) depends on the conduction band only, it remains fixed. To understand the behavior of RFET, it is essential to understand the carrier conduction through M-S junction specifically for Schottky contacts.

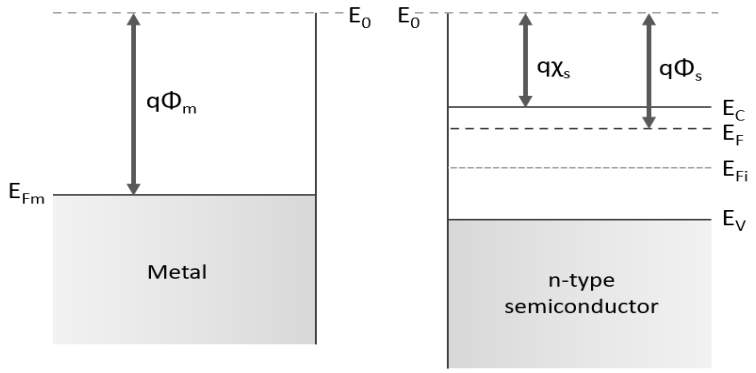


Fig. 2.1 Band diagram of metal and semiconductor [1].

2.1.1 Schottky Contact

Based on the type of semiconductor, the Schottky contact can be formed in two cases:

a) n-type semiconductor with $\Phi_m > \Phi_n$

Prior to the contact formation, Fermi level of semiconductor is positioned above that of metal. At equilibrium, electrons from the n-type semiconductor will move towards the lower energy levels of metal resulting in a depletion or space charge region at the junction.

The potential barrier height for electrons as seen from the metal side to move to E_C is known as Schottky Barrier Height (SBH) for electrons and is given by [1],

$$q\Phi_{B,n} = q(\Phi_m - \chi_{s,n}) \tag{2.1}$$

On the other hand, the potential energy barrier as seen from the semiconductor side for an electron to move to the metal side is known as built-in potential (V_{bi}) and is given by [1],

$$qV_{bi} = q(\Phi_{B,n} - \Phi_n) \tag{2.2}$$

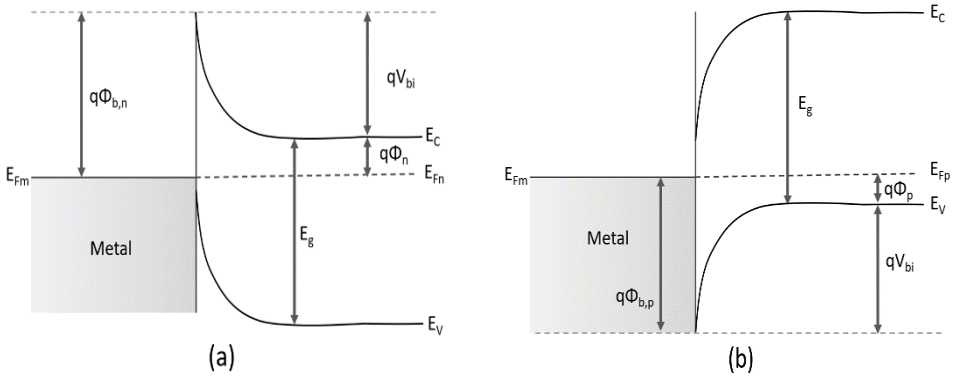


Fig. 2.2 M-S contact band diagram with (a) n-type and (b) p-type semiconductor [1].

b) p-type semiconductor with $\Phi_m < \Phi_p$

Similar to that of the n-type, at equilibrium, here the depletion region is formed at M-S junction by the uncovered acceptor ions when holes from the p-type move to the energy level of the metal. The SBH [1] for holes is,

$$q\Phi_{B,p} = E_g - q(\Phi_m - \chi_{s,p}) \tag{2.3}$$

where, E_g is the bandgap of semiconductor.

Conduction through Schottky Barrier

For simplicity, the conduction is explained for n-type semiconductor ($\Phi_m > \Phi_n$). For conduction at M-S junction, three possible mechanisms are responsible [1]. These are described below.

a) Thermionic Emission

It refers to the flow of carriers when they have sufficient energy to cross the barrier at the M-S junction. When a forward bias (V_{AP}) is applied i.e. $V_{AP} > 0$, the barrier height for electrons in the n-type semiconductor reduces. As a result, the electrons can now move from the higher energy levels of conduction band (E_C) to the lower energy levels of metal resulting flow of current in the device. However, when a reverse bias is applied with $V_{AP} < 0$, the potential energy barrier at the junction increases. As a result, the current decreases. However, the applied bias does not affect the SBH. Hence, there is always a very small amount of current because of tunnelling of electrons (metal to semiconductor) under reverse bias condition.

The 1-D equation of Thermionic Emission (J_{TE}) at temperature (T) is given as [2],

$$J_{TE} = A^* T^2 exp\left(-\frac{q\Phi_{B,n}}{kT}\right) \tag{2.4}$$

where A* is Richardson's Constant and is given by,

$$A^* = \frac{4\Pi q m^* k^2}{h^3} \tag{2.5}$$

The overall current density in the Schottky diode is almost similar to that of p-n junction counterpart and is expressed as [2],

$$J_n = J_{TE}\left[exp\left(\frac{qV_{AP}}{kT}\right) - 1\right] \tag{2.6}$$

b) Field Emission

Due to the applied field, some of the electrons get sufficient energy to tunnel through barrier around the conduction band edge. This phenomenon is referred as field emission.

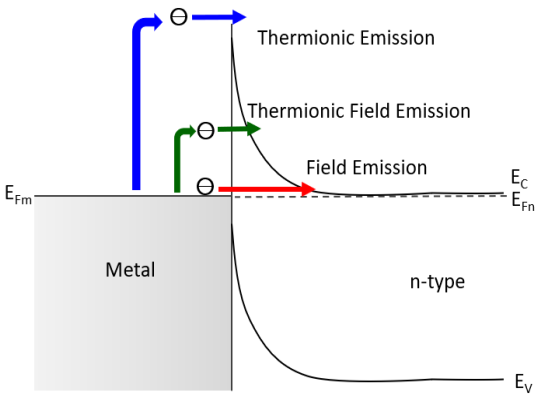


Fig. 2.3 Different mechanism responsible for conduction at M-S junction.

c) Thermionic-field Emission

Some of the thermally excited electrons which have higher energy than the conduction band but not enough to cross the barrier can also tunnel through the barrier due to the electric field. This is referred to as thermionic-field emission.

Both field-emission and thermionic-field emission are strongly functions of thickness of the barrier at the M-S junction. In a heavily doped semiconductor, the barrier becomes very thin, and current flows due to these two phenomena [1]. For the same reason, for low doped semiconductor the effects of field-emission and thermionic-field emission are very negligible compared to thermionic emission.

2.1.2 Ohmic Contact

Similar to the Schottky contacts, the Ohmic contacts can also be formed in two ways at M-S junctions [2]. For n-type semiconductor with $\Phi_m < \Phi_n$, results in flow of electrons from the higher energy states of metal to the lower energy states of semiconductor at equilibrium making the junction more n-type. At equilibrium, a p-type semiconductor with $\Phi_m > \Phi_p$ results in flow of electrons from semiconductor to metal generating more holes at the junction making it more p-type. Upon applying biases, the carriers can easily flow from metal to semiconductor or vice versa owing to very small barrier or no barrier at all at the junction resulting flow of current in direction according to applied voltages. That is why these junctions act like non-rectifying or ohmic contact.

Another way to create ohmic contact at M-S junction is simply by doping the semiconductor heavily [2]. Because of this high doping, the depletion width at the junction becomes very narrow resulting reduction in the tunnelling width and thus carriers can easily tunnel through this barrier and reach either side based on the applied bias.

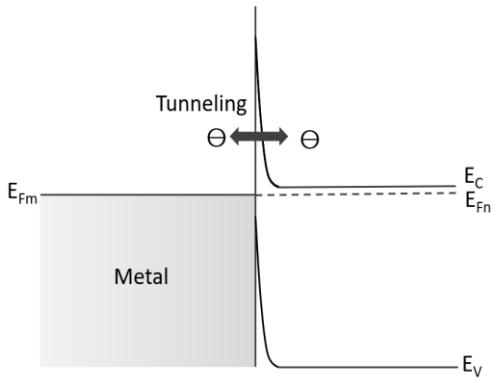


Fig. 2.4 Tunnelling mechanism through ohmic M-S contact for conduction.

2.2 Reconfigurable Field Effect Transistor (RFET)

The idea of Reconfigurable Field Effect Transistor (RFET) [5-16] comes from Schottky Barrier Field Effect Transistor (SBFET). SBFET employs two M-S junctions at source and drain. Here, a single gate used for current flow. However, it suffers from ambipolar behaviour of the current. To suppress the ambipolarity another gate is employed at the source side. Later, these two gates were separated and controlled independently to achieve reconfigurability. As the scaling continued over the years according to Moore's Law [3], in the nanoscale regime many effects such as short channel effects (SCEs), random dopant fluctuations become more dominant. As a result, not only the fabrication process becomes more complex [4] but the reliability of the MOSFET operation is also challenged. The RFET, being intrinsic and the use of simple M-S junctions at source and drain counter the issues of fabrication process complexity and cost (low thermal budget). On the other hand, just by changing the polarity of the biases, same transistor can be operated as both n-type and p-type. Therefore, the separate need of fabricating p-type device like CMOS counterpart is not needed at all. In the logic

implementation level, this decreases number of transistors to be used compared to standard CMOS logic [5-16].

Typical RFET configuration consists of two effective gates: control gate (CG) and polarity gate (PG). To enable carrier injection at the source and drain side through tunnelling, two M-S Schottky junctions are needed. For that Ni-Si are used at source and drain. Since RFET supports both n-type and p-type on the same device, the Si-body is essentially intrinsic or lightly p-doped.

Based on the position of the gates, RFET can be broadly classified into types: two gate or 2G-RFET and three gate or 3G-RFET [5-14]. The corresponding figures are shown in Fig. 2.5 and Fig. 2.6. 3G-RFET consists of three gates, two polarity gates at the source and drain side and one control gate in the middle. On the other hand, 2G-RFET employs one control gate at the source while another is at the drain. In both the cases, the injection of carriers is done by polarity gate and the flow of carriers is controlled by control gate by applying biases. In 3G-RFET, this flow of carriers is controlled at the middle of structure whereas the same is done at the drain end in 2G-RFET. A positive bias at the polarity gate enables the injection of electrons in the body making it n-type and a negative bias enables the injection of holes making the device p-type, thus achieving reconfigurable nature. The polarity gates in the 3G-RFET can be shorted and operated with a single bias.

Due of the use of more number of gates, the controllability in 3G-RFET is higher than that of 2G-RFET. This provides better subthreshold swing in 3G-RFET than 2G-RFET. However, the use of more number of gates requires more fabrication complexity and cost [5]. Also the use more number of gates lead to higher capacitance, and thus, increase intrinsic delay of device [17]. That is why in this analysis 2G-RFET has been the primary concern. Nickel silicide has been used in both source and drain region for M-S junction as it has been proven an excellent material for forming Schottky junction avoiding defects or taps at the interface causing Fermi level pinning at the M-S junction [18].

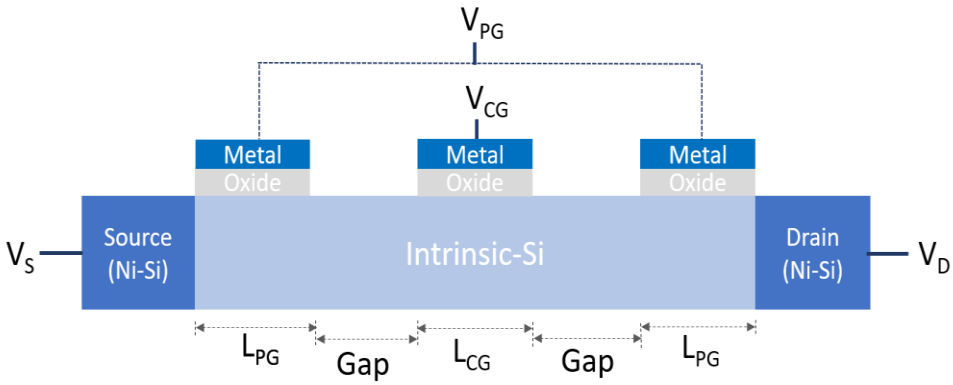


Fig. 2.5 Schematic illustration of a three gate RFET.

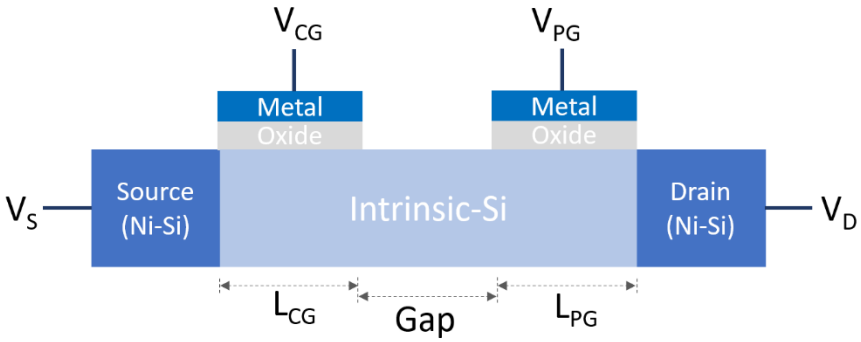


Fig. 2.6 Schematic illustration of a two gate RFET.

2.2.1 Working of Twin Gate RFET

The entire analysis of 2G-RFET (throughout the thesis) has been done on Silvaco ATLAS TCAD tool [19]. The Universal Schottky Tunneling (UST) model has been used to capture conduction at the Schottky Barrier junction. The effective masses of electrons (m_n^*) and holes (m_p^*) are taken to be $0.3m_o$ and $0.2m_o$ respectively [6], where m_o is the rest mass of electron. Other physical models used for simulation include temperature and concentration dependent carrier lifetime, generation-recombination models, impact ionization, and concentration and field dependent mobility [19].

To explain the working principle through the band diagrams, the control gate length (L_{CG}) is same as the length of the polarity gate (L_{PG}) i.e. 25 nm along with gap/separation of 90 nm. The source and drain metal length are equal and of 30 nm. The Si body thickness (T_{Si}) and the oxide (SiO_2) thickness

(T_{ox}) are 10 nm and 2 nm respectively. The work function of all gates as well as source/drain are taken to be 4.71 eV.

When no voltages are applied at any of the terminals, the bands are essentially flat as there is no work function difference between gates, S/D region with the Si-body as seen in Fig. 2.7.

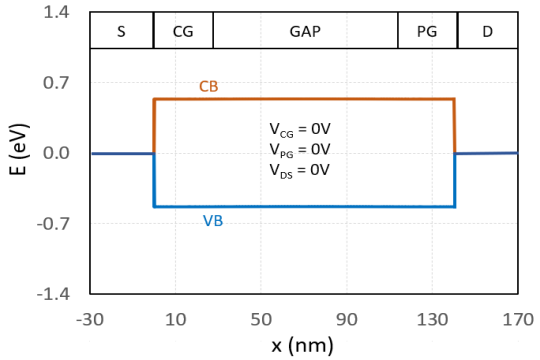


Fig. 2.7 RFET at equilibrium/flat band condition (zero bias).

To make this device as n-type, a positive voltage at the polarity gate causes electrons to accumulate below it and the surface becomes more n-type (field induced doping). Hence, bands bend in downwards. However, as V_{CG} = 0 at this point, electrons which are present at the source side see a high energy barrier and cannot cross it. Hence, no current flows through the body even at the application of drain bias. Hence, the device is OFF. To make this device ON, a positive bias has to be applied at control gate terminal. Hence, bands (corresponding to the control gate region) bend in downward direction. Under this condition, a positive bias at the drain allows electrons to tunnel through the reduced barrier width at the source and reaches drain under the influence of electric field. Thus, current flows in the device in n-type configuration.

Similar to the n-type, the device can be made to function as p-type by changing the polarity gate bias to negative. As a result, holes will be accumulated below the polarity gate bending the bands in the upward direction. However, even at the application of a negative bias at drain, holes from source cannot cross the energy barrier in the body as V_{CG} = 0 V. This is the OFF condition in p-type configuration. To turn the device ON, a negative voltage at the control gate causes bands to bend upwards resulting a narrow barrier width. Thus, holes from the source side tunnel through this narrow

width and reach drain because of the applied horizontal field constituting the hole current. The band diagrams for n-RFET and p-RFET ON and OFF conditions are shown in Fig. 2.8.

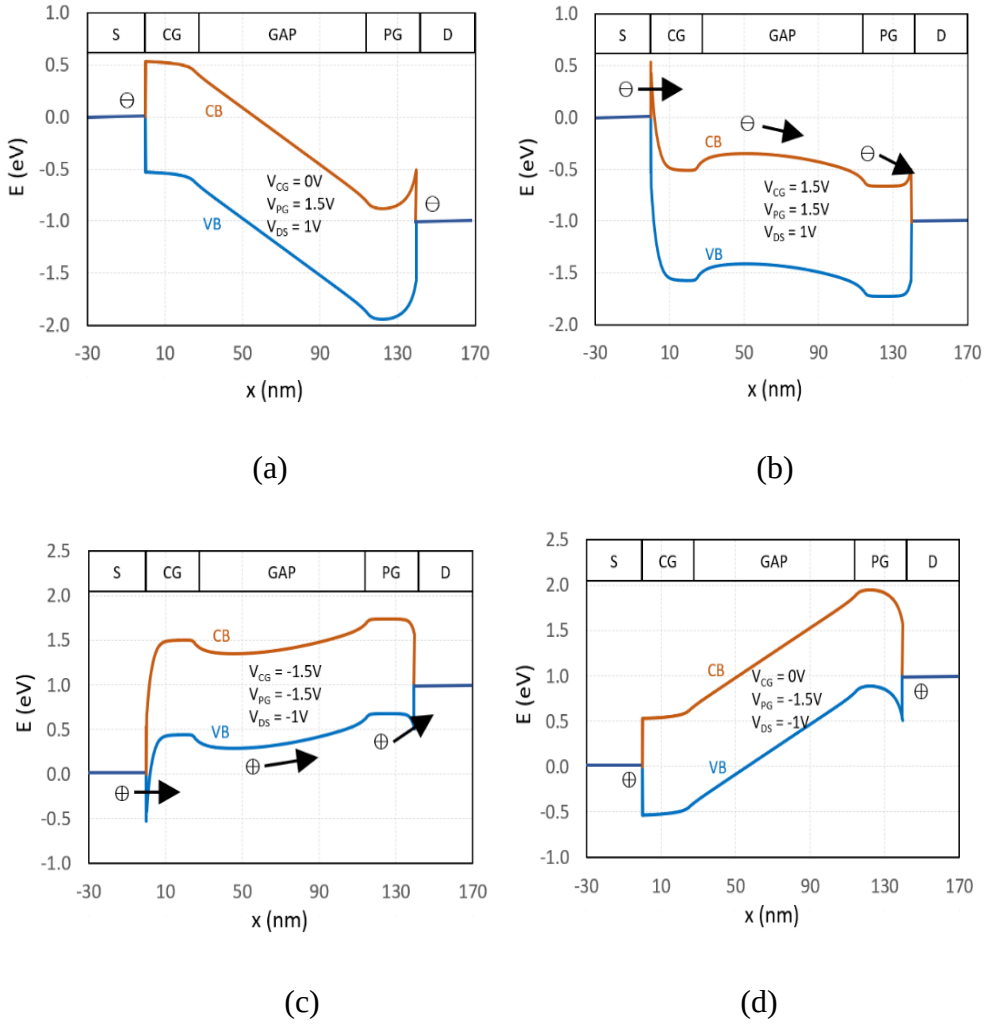


Fig. 2.8 Band diagram for (a) n-RFET OFF, (b) n-RFET ON, (c) p-RFET ON and (d) p-RFET OFF conditions.

2.2.2 Characteristics of 2G-RFET

The characteristics of 2G-RFET can be divided into two parts – transfer characteristics and drain or output characteristics. Again, as there are two separate gates present, we have two separate transfer curves – I_D vs V_{CG} curve and I_D vs V_{PG} curve.

The width of tunneling at Schottky barrier (SB) depends on the applied bias at the polarity gate and control gate. The intrinsic spacer region (the ungated region) between the control and polarity gate causes a high resistance

in the body region and thus limiting the drive current. That is why in RFET the drive current is small compared to conventional MOSFET device.

For the characteristics here, L_{PG} and L_{CG} are taken to be 25 nm with an ungated gap region, L_{GAP} of 50 nm. L_S and L_D are taken as 25 nm each. The t_{ox} and t_{Si} are 1.5 nm and 10 nm respectively. All the gates along with source-drain work function are taken to be 4.71 eV at 85 °C.

The tunneling probability, $T_{n,p}$, through a barrier can be expressed with the help of Wentzel–Kramers–Brillouin (WKB) approximation for a triangular barrier [20] as,

$$T_{n,p} \propto e^{\frac{-4\sqrt{2\,m^*_{n,p}}\,\Phi^{\frac{3}{2}}_{B,n,p}}{3q\hbar E}} \tag{2.6}$$

where E is the applied field the across the barrier and ħ is the reduced Planck's constant.

For a fixed V_D of 1.5 V, when I_D vs V_{CG} graph is plotted in Fig. – 2.9 (a) for different V_{PG} it can be seen that, for a higher V_{PG} we have a higher current in the device. For a low V_{CG}, the barrier thickness at the source region is sufficiently high causing a very low current in the device. On the other hand, a high V_{CG} causes the bands to bend in the downward direction significantly resulting a very narrow tunneling width. Thus, more electrons can now get injected in the device through tunneling. However, if V_{PG} is low, at the drain region the tunneling width becomes high. Hence, thermionic emission becomes more dominant than tunneling mechanism and only a few electrons can cross the barrier and reach the drain terminal. However, upon applying a high V_{PG}, the tunneling becomes more dominant than thermionic emission and we get a higher current due to combining effect of them.

However, for a fixed V_{PG}, when I_D vs V_{CG} characteristics is plotted for different drain bias a similar trend to that for V_{PG} can be seen. This trend is followed because the barrier height decreases at drain terminal as V_D increases. As a result, when V_D is made high, a greater number of electrons can cross the barrier due to thermionic emission as well as tunnel through the barrier. Hence, drain current increases which is reflected in Fig. 2.9 (b).

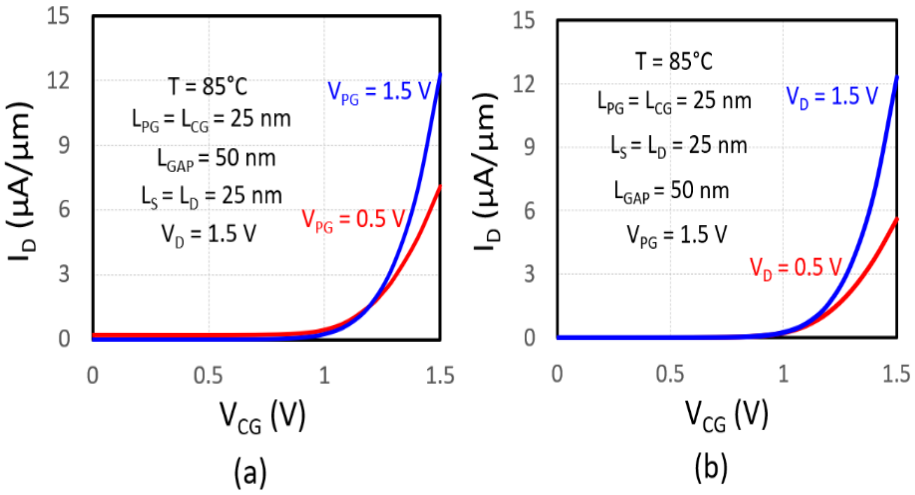


Fig. 2.9 I_D vs V_{CG} characteristics for (a) different V_{PG} and (b) different V_D.

The typical I_D-V_{PG} characteristics for different PG biases and a fixed drain bias of V_D = 1V is shown in Fig.- 2.10. For a given V_D and V_{CG}, when V_{PG} is varied, initially the current increases almost linearly due to the fact that upon increasing V_{PG} at the beginning the conduction and the valence bands near the drain terminal bend in the downward direction in a linear fashion. As a result, the energy barrier decreases enabling more thermionic emission into the drain terminal causing more current to flow. At a higher V_{PG}, this bending is more compared to that for lower V_{PG}. That is why the energy barrier decrease is also very high for a higher V_{PG}. Hence, we get a higher degree of current for a higher V_{PG}. However, at a given V_{CG} and V_D, at higher V_{PG} we can only see a very small slope in the current. This is due to the reason that, at this point the thermionic emission saturates and the tunneling of carriers at the Schottky barrier at the drain region comes into play. Due to the high V_{PG}, the tunneling width at the drain region becomes sufficiently narrower causing electrons to tunnel into drain. As a result, the current increases. A higher V_{CG} results in more injection of carriers in the source region causing a higher current to flow. One interesting aspect to note here is that, at the beginning when V_{PG} increases slightly the current actually decreases and then increases. When V_{PG} = 0V (say for V_{CG} = 1.5V and V_D = 1V), because of the high energy barrier at the middle only a very few holes (tunneling from drain side) and electrons (tunneling from source side) can flow due to thermionic emission and low rate of tunneling. Now, when V_{PG} increases slightly,

thermionic emission hardly gets affected, but as the band move slightly in the downward direction at drain side, the tunneling width also increases, reducing carrier tunning at the drain side. That is why we see a negative slope in the graph at the beginning. However, after a certain point, when barrier starts reducing significantly, the thermionic emission become more dominant over tunneling and we see a linear variation of the current with V_{CG}.

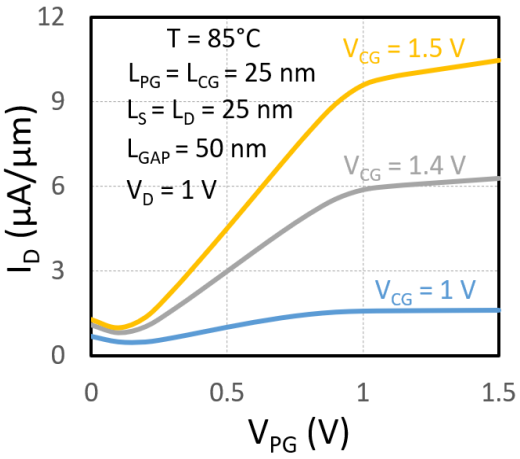


Fig. 2.10 I_D vs V_{PG} characteristics for different V_{PG}.

The output or I_D vs V_D characteristics for different values of V_{PG} and V_{CG} (both are kept at same voltage) are shown in Fig.- 2.11. It can be seen that, it follows a similar kind of pattern to that of I_D vs V_{PG} characteristics. At the beginning as V_D increases, the energy barrier for the carriers (here, electrons) at the drain region as well as at the ungated region move in the downward direction. As a result, the barrier height at these areas decreases allowing more electrons to flow from source and ultimately because of tunneling and thermionic emission at the drain region current increases linearly. However, after a certain voltage, the Schottky barrier height at the drain region becomes negligible because of the higher voltage at the drain causing the metal Fermi level to move downward significantly. At this point only thermionic emission exist and the current increases at a very slower rate due to applied field for a given V_{CG} and V_{PG}. If V_{CG} and V_{PG} are lowered, the tunneling width at both source and drain becomes higher and less carriers get injected through tunneling process. Hence, a lower current is attained.

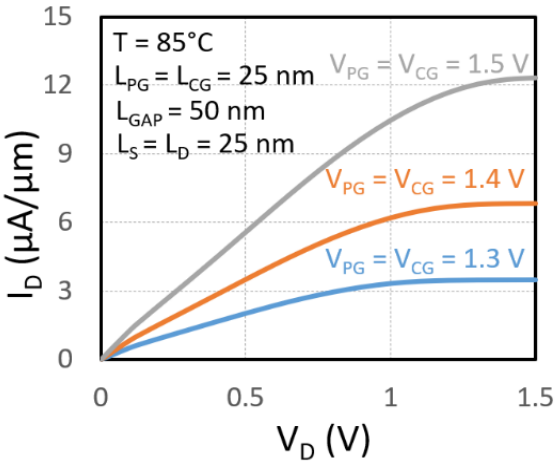


Fig. 2.11 I_D vs V_D characteristics for different V_{PG} = V_{CG}.

Similar type of characteristics curves can be obtained for p-type also just by changing biases. However, if the same device is used with all gates and source-drain work function of 4.71 eV, the drive current for p-type will be less than that of n-type. This is because, in Si, the intrinsic Fermi level does not exist exactly at the middle due to the effective mass difference between holes and electrons. As result, a higher Schottky barrier exist for holes when M-S junctions are formed for a work function of 4.71 eV. Therefore, to decrease the Schottky barrier height for holes, a slightly higher work function at the source and drain metal can be used. But as this increases the Schottky barrier height for electrons, a comparatively low n-type current than previous case is observed.

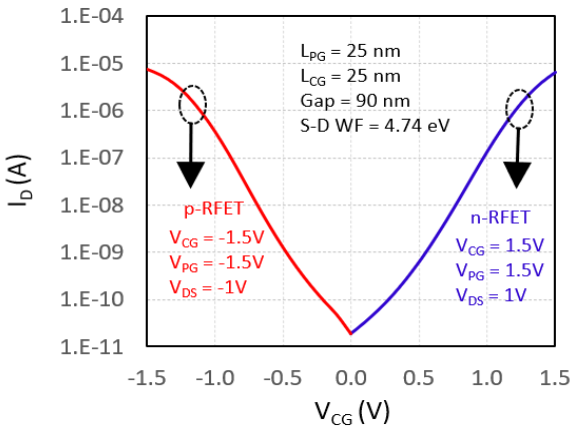


Fig. 2.12 Reconfigurability of 2G-RFET shown through nMOS and pMOS device characteristics.

In the Fig. 2.12, which actually is the I_D vs V_{CG} characteristics of both p-type and n-type configuration, a slightly higher work function (4.74 eV) at source and drain region is used to get symmetric p-type and n-type current which proves the reconfigurability feature of the RFET. Here, L_{GAP} is taken as 90 nm with all other parameters same as previously stated.

2.3 Conclusion

The RFET, being an extension of SBMOSFET, has all the advantages of it along with the improved properties such as suppressing the ambipolar behaviour and reconfigurability. Here, in fact the ambipolarity nature is modified to provide unipolar n-type and p-type configuration by using two separate gates. Even though the small drive current is a concern, the I_{ON}/I_{OFF} ratio being in the order of ~10^5 and the gate capacitance was relatively lower [21] than that exhibited by MOSFET. This makes it suitable for logic applications. RFET, upon achieving maturity, can be used to implement multifunctional complementary logic circuits with same design.

References

[1] Taur Y., and Ning T. H., (2009) MOSFET devices. In: Fundamentals of modern VLSI devices, 2nd edn., Cambridge University Press, pp. 108-122 (ISBN 978-0-521-83294-6).

[2] Neamen D. A., (2012) Semiconductor Physics and Devices: Basic Principles, 4th edn. McGraw-Hill, New York (ISBN 9780073529585).

[3] Moore G. E., (1998) Cramming More Components Onto Integrated Circuits, Proceedings of the IEEE, 86, pp. 82-85.

[4] Xiong, W. (W.) (2008). Multigate MOSFET Technology. In: Colinge, JP. (eds) FinFETs and Other Multi-Gate Transistors. Springer, Boston, pp. 49-111 (ISBN 9780387717524).

[5] Trommer J., Heinzig A., Baldauf T., Slesazeck S., Mikolajick T. and Weber W. M. (2015), Functionality-enhanced logic gate design enabled by symmetrical reconfigurable silicon nanowire transistors, IEEE Transactions on Nanotechnology, 14, 689-698.

[6] Navarro C., Barraud S., Martinie S., Lacord J., Jaud M. and Vinet M. (2017), Reconfigurable field effect transistor for advanced CMOS: Advantages and limitations, Solid-State Electronics, 128, 155-162.

[7] Marchi M. D., Zhang J., Frache S., Sacchetto D., Gaillardon P.-E., Leblebici Y., and Micheli G. D. (2014), Top–down fabrication of gate-all-around vertically stacked silicon nanowire FETs with controllable polarity, IEEE Transactions on Nanotechnology, 13, 1029–1038.

[8] Marchi M. D., Zhang J., Frache S., Sacchetto D., Gaillardon P.-E., Leblebici Y., and Micheli G. D. (2014), Configurable logic gates using polarity controlled silicon nanowire gate-all-around FETs, IEEE Electron Device Lett., 35, 880–882.

[9] Zhang J., Marchi M. D., Sacchetto D., Gaillardon P., Leblebici Y. and Micheli G. D. (2014), Polarity-Controllable Silicon Nanowire Transistors With Dual Threshold Voltages, IEEE Transactions on Electron Devices, 61, 3654-3660.

[10] Böckle, R., Sistani, M., Lipovec, B., Pohl, D., Rellinghaus, B., Lugstein, A., Weber, W. M. (2022), A Top-Down Platform Enabling Ge Based Reconfigurable Transistors, Adv. Mater. Technol., 7, 2100647.

[11] Simon M., Liang B., Fischer D., Knaut M., Than A., Mikolajick T. and Weber W. M. (2020), Top-Down Fabricated Reconfigurable FET With Two Symmetric and High-Current On-States, IEEE Electron Device Letters, 41, 1110-1113.

[12] Sistani M., Böckle R., Falkensteiner D., Luong M. A., Hertog M. I. D., Lugstein A. and Weber W. M. (2021), Nanometer-Scale Ge-Based Adaptable Transistors Providing Programmable Negative Differential Resistance Enabling Multivalued Logic, ACS Nano, 15, 18135-18141.

[13] Simon M., Heinzig A., Trommer J., Baldauf T., Mikolajick T. and Weber W. M. (2017), Top-Down Technology for Reconfigurable Nanowire FETs With Symmetric On-Currents, IEEE Transactions on Nanotechnology, 16, 812-819.

[14] Heinzig A., Slesazeck S., Kreupl F., Mikolajick T. and Weber W. M. (2012), Reconfigurable Silicon Nanowire Transistors, Nano Letters, 12, 119-124.

[15] Gaillardon P., Hasan M., Saha A., Amarú L., Walker R. and Rodriguez B. S., (2016) Digital, analog and RF design opportunities of three-independent-gate transistors, Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), pp. 405-408.

[16] Gaillardon P., Amaru L., Zhang J. and Micheli G. D. (2014), Advanced system on a chip design based on controllable-polarity FETs, Proceedings of Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 1-6.

[17] Manoj C. R., Mangal A., Rao V. R., Tsutsui K. and Iwai H., (2006) Parasitics effects in multi gate MOSFETs, Proceedings of International Workshop on Nano CMOS, pp. 255-260.

[18] Tung R., (2014) The physics and chemistry of the Schottky barrier height, Applied Physics Reviews, 1(1), p.011304.

[19] Silvaco, (2015) ATLAS User Manual, Santa Clara, CA, USA.

[20] Sze, S. M., Li, Y., & Ng, K. K. (2021). Physics of semiconductor devices. John wiley & sons. (ISBN 978-0-470-06832-8).

[21] Weber W.M., Heinzig A., Trommer J., Martin D., Grube M. and Mikolajick T. (2014), Reconfigurable nanowire electronics–a review. Solid-State Electronics, 102, 12-24.

Chapter 3

Twin gated RFET as 1T-DRAM

3.1 Introduction

The advantages of Silicon-on-Insulator (SOI) over bulk technology [1-5] makes it an ideal technology to be widely used in emerging transistors. Out of the two options within SOI i.e. partially depleted (PD) and fully depleted (FD), the device miniaturization has lead to the utilization of FD SOI in scaled devices. The development of eDRAM cell in SOI technology allows the transistors to be integrated onto the same chip as devices for logic applications. The overall system performance shall be benefitted if the same devices can be utilized for logic as well as for memory applications [6-8]. The present CMOS technology needs different fabrication steps for nMOS or pMOS transistors which limits logic circuit density. However, RFET which can be electrically tuned as nMOS or pMOS via applied bias [9-10], allows logic function realization with lower transistor count [9-19].

The re-configurability of RFET has the advantage of using the same structure as NAND and NOR when programmed dynamically using only 6-RFETs [15] as well as the implementation of XOR and NAND on the same 4-RFET layout [10], thus allowing room to implement different set of functionalities and providing new approach for logic synthesis. The use of dual-threshold RFET has also been demonstrated to highlight a significant reduction in leakage power [17]. Technology mapping with the help of new algorithm has been proposed to improve area and delay using RFET [16]. The implementation of full adder [19], 4T pseudo-SRAM cell [19] and embedded power gating techniques have also been demonstrated to achieve faster and energy efficient System-on-Chip [19]. Apart from digital applications, RFETs have also been used for analog/rf designs [18]. All of the above indicate to numerous advantages of RFETs. Apart from the above-mentioned advantages, it is a great interest to explore 1T-DRAM possibilities through 2G-RFET. The primary asset of converging RFET based eDRAM with logic is to enhance bandwidth i.e. minimize delay in data transfer [20]. In this context, the design

optimization and benchmarking of eDRAM and standalone DRAM finds relevance in futuristic programmable technologies.

3.2 Limitation of using double gate conventional 2G-RFET as 1T-DRAM

Here, to analyse conventional double gate 2G-RFET as 1T-DRAM, the workfunction of Nickel Silicide (NiSi) at source/drain region is 4.6 eV, which correlates to a Schottky barrier (SB) height (SBH) of 0.43 eV. The tunneling through SB is incorporated through the universal Schottky tunneling (UST) module with different effective masses of electrons ($0.3m_o$) and holes ($0.2m_o$), respectively, where m_o is the rest mass of electron [21]. A fixed silicon film thickness (T_{Si}) of 10 nm, and SiO_2 layer thickness (T_{ox}) of 1.5 nm is used for the analysis throughout this chapter. Other models have already been described in chapter 2.

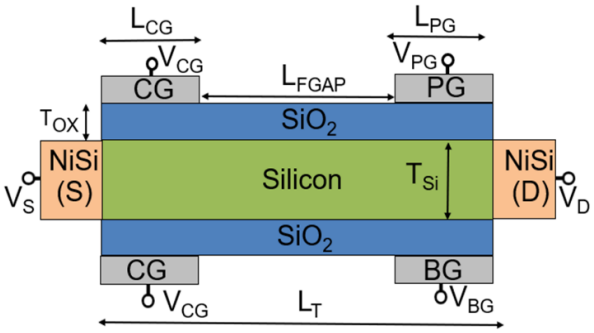


Fig. 3.1 Conventional double gate 2G-RFET structure.

To analyse the conventional double gate 2G-RFET, the structure shown in the Fig. 3.1 has been considered. For logic operation the top and back polarity gates as well as the top and back control gates are short circuited. However, for 1T-DRAM application the back polarity gate, also known as back gate (BG) is operated independently to store the charges in the body of RFET. Here, for operation, all the gate lengths are taken to be 25 nm ($L_{PG} = L_{CG} = L_{BG} = 25$ nm) along with spacing (L_{FGAP}) of 50 nm.

In a 2G-RFET, to enable the tunneling of holes a negative voltage is applied at the PG, as it bends the energy bands in PG region in the upward direction and thereby reducing the tunneling width. Here, the storage region is present at the back surface in the back gate region which is biased

independently to store the holes. For write ‘1’ operation the excess holes are needed to be generated in the body. The impact ionization and tunneling mechanism are used to generate these excess carriers. To facilitate that, -1.5 V is applied at PG and 1.5 V at the drain as shown in Fig. 3.2 (a) and Fig. 3.3 (a). During write ‘0’ the holes from the storage region are needed to be depleted. Hence, barrier height as seen by electrons is reduced at drain by the application of positive BG bias (Fig. 3.2 (b) and Fig. 3.3 (b)). When write ‘1’ is followed by hold process, the positively charged holes increase the potential at the back gate region facilitating tunneling of electrons from drain region causing recombination of the stored holes with electrons. As a result, the hole concentration is significantly reduced. On the other hand, during hold ‘0’ operation, since the holes are depleted during write ‘0’ operation, the potential

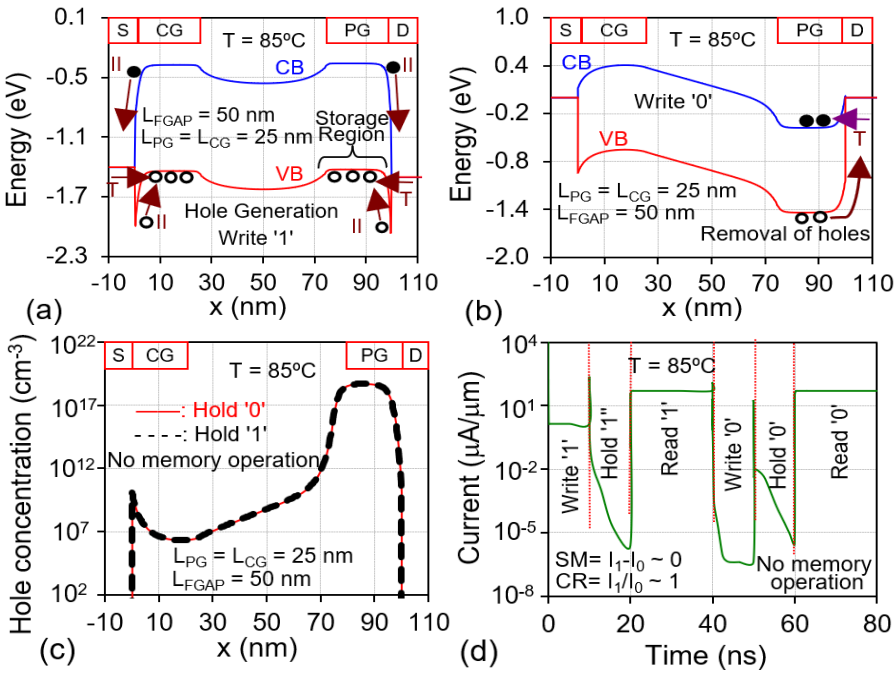


Fig. 3.2 The absence of memory functionality in a conventional 2G-RFET is exhibited through the variation of conduction and valance bands for (a) write ‘1’, and (b) write ‘0’ operations. Correlation of the same is shown through the (c) variation of hole concentration during hold operation and (d) drain current transient. The cutline in the semiconductor for (a), (b) and (c) is taken to be 0.5 nm above the back surface. Biases are mentioned in Table 3.1.

at the back gate region decreases. As a result, holes tunnel from source and drain region to the body, and increase the hole concentration significantly.

Thus, hole concentration at the time of hold ‘1’ and hold ‘0’ states essentially remain same as shown in Fig. 3.2 (c) and Fig. 3.3 (c)-(d).

Therefore, when the read current flows, both the read ‘1’ and read ‘0’ hole concentration at BG region impacts the top surface barrier by exactly the same amount as the concentration is the same. Thus, read ‘1’ and read ‘0’ current essentially become same and cannot be distinguished as shown in Fig. 3.2 (d). Therefore, the memory operation cannot be achieved in this architecture. This problem cannot be resolved by selecting appropriate bias as a higher negative voltage at the PG results in more tunneling of holes causing a sharp degradation in hold ‘0’ state and a lower negative PG bias facilitates tunneling of electrons causing degradation in hold ‘1’ state. Hence, 1T-DRAM operation cannot be achieved in conventional double gate 2G-RFET with bias selection. Therefore, the architecture improvisation is needed. To resolve this issue, the back gate can be misaligned and move away from the drain Schottky region through intentional back gate misalignment [22].

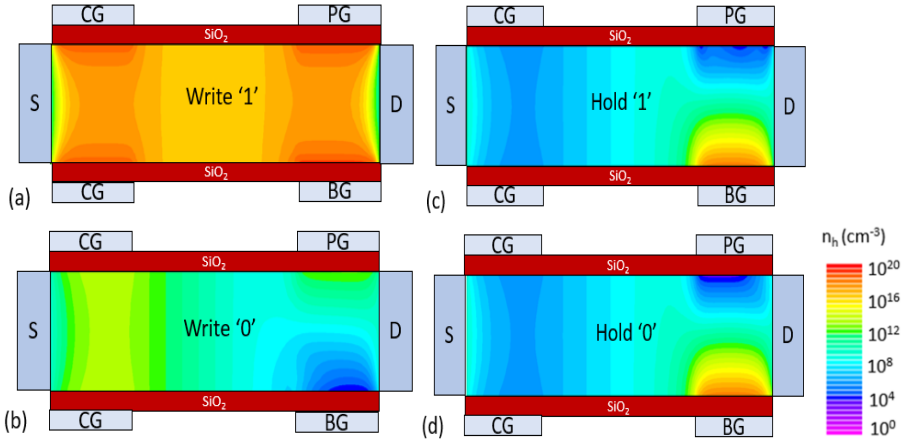


Fig. 3.3 Contour plots for hole concentration (n_h) during (a) write ‘1’, (b) write ‘0’, (a) hold ‘1’ and (b) hold ‘0’ operations of conventional double gate 2G-RFET at 85°C. at 85°C. Parameters: L_{CG} = L_{PG} = L_{BG} = 25 nm and L_{FGAP} = L_{BGAP} = 50 nm. Biases are mentioned in Table 3.1.

3.3 Proposed misaligned 2G-RFET as 1T-DRAM

The proposed structure has one PG at the front surface, one CG each at front and back surfaces, and one intentionally misaligned PG (referred as back

gate, BG) as shown in Fig. 3.4 (a). The ungated region (L_{FGAP}) separates front CG and PG as shown in Fig. 3.4 (a).

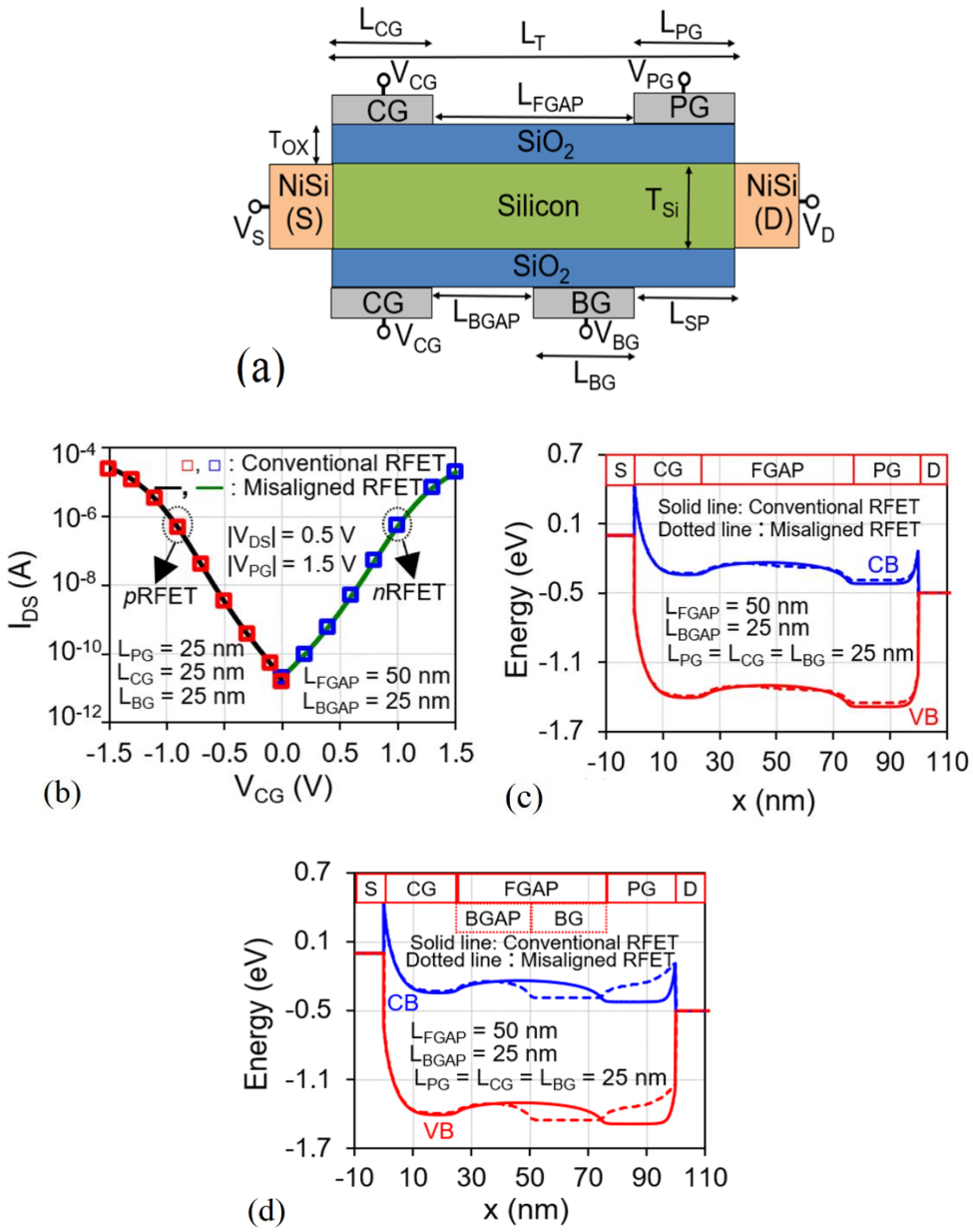


Fig. 3.4 Schematic diagram of (a) proposed misaligned twin-gate (2G) RFET. (b) Comparison of I_{DS}-V_{CG} characteristics of conventional and misaligned (proposed) RFET. Energy bands diagrams extracted at (c) front and (d) bottom surfaces of conventional and proposed 2G-RFET. Biases: V_S = 0V, V_D = 0.5 V, V_{PG} = V_{BG} = 1.5 V.

Similarly, an ungated region (L_{SP}) separates BG from the drain. SB and ungated region primarily affect the resistance of the RFET. The application of bias at the PG can reduce the resistive component of SB. In the proposed structure, front gate barriers remain unaffected (Fig. 3.4 (c)). However, intentional BG misalignment enhances the SB resistive component (Fig. 3.4 (d)) as the BG is away from the SB. The benefit of this is derived through a lowering of the resistance associated with L_{FGAP} due to better BG control. Hence, the current drive of the misaligned 2G-RFET essentially becomes similar to the current drive of a traditional 2G-RFET structure as shown in Fig. 3.4 (b). Also, a key aspect of RFET i.e. multi-functionality is preserved as both nMOS and pMOS operations can be implemented (by electrically connecting the PG and BG) with the misaligned topology. Thus, the proposed misaligned structure facilitates the use of BG (independently biased) for creating an electrostatic potential well without compromising re-configurability.

3.4 Integration flow

RFETs have already been fabricated in different geometries such as nanowire [9-10, 23-30], and Fin shape [31-32] in SOI technology. In literature, there are two possible ways to fabricate the RFET devices: (1) top to bottom [9-10, 25-28] and (2) bottom-up [29-30] approach. Initially, a bottom-up approach [33] was used in the fabrication of RFETs. However, due to several issues in the approach, researchers have utilized top-down approach, which is compatible with CMOS fabrication process [9-10, 25-28].

The possible integration flow (Fig. 3.5) of the proposed structure is based on the top to bottom approach as follows:

Fabrication steps start with an undoped SOI layer. Channel can be patterned into the desired fin shape with electron beam lithography [31]. SiO_2 layer is formed using dry oxidation [31]. After SiO_2 formation, a polysilicon layer is deposited over the oxide layer using the conformal deposition. After that, the Schottky-Barrier (SB) region is patterned through electron beam lithography by lifting off the metal and oxide in that region. All the above-mentioned steps are very same as used in the fabrication of the Fin-shaped

RFET. Now, again using the electron beam lithography, CG and PG can be patterned with different length i.e., $L_{PG}=2\times L_{CG}$. After the above-mentioned steps results in a twin gate RFET with polarity gate length equal to the twice of control gate length.

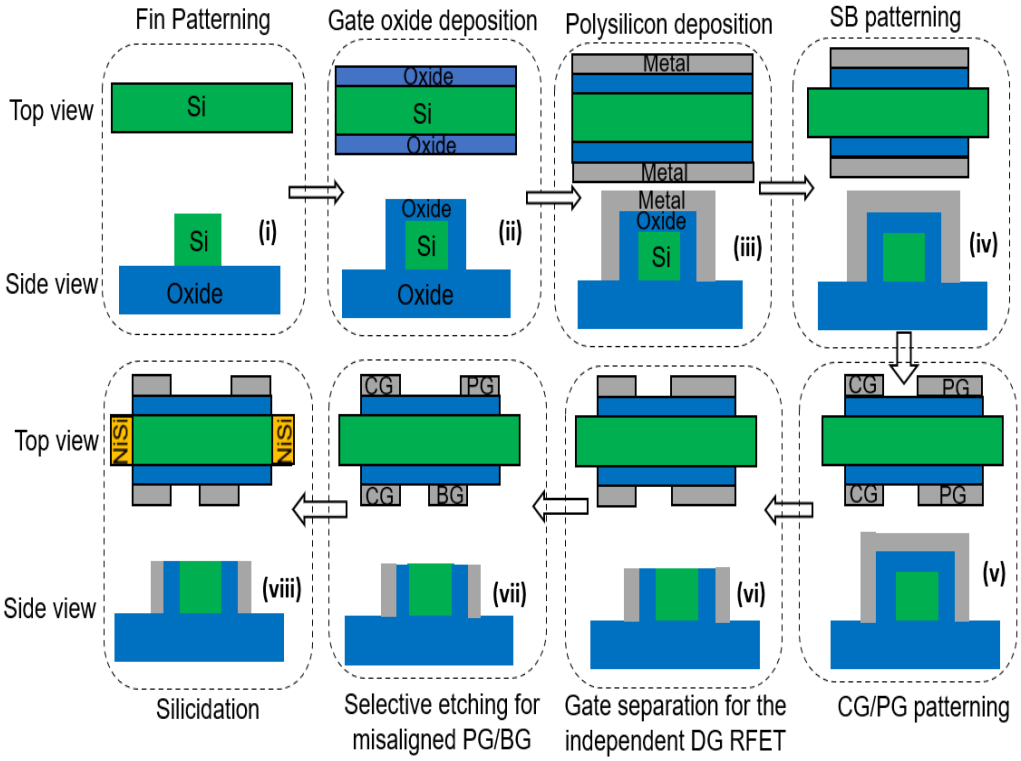


Fig. 3.5 Possible integration flow to realize the proposed structure through well-known fabrication steps [31-35].

The gates can be separated for independent gate operation by using Chemical Mechanical Polishing (CMP) [34], stopping at the SiON layer protecting the fin. The slurry with a high Si/SiON selectivity enabled a self-stopping mechanism once the SiON Hard mask (HM) on top of the fin is reached, eliminating the risk of damage [34-35]. After the CMP process results in an independent polarity and control gate double gate RFET with $L_{PG}=2\times L_{CG}$. After that, the backside and front side of the polysilicon layer can be selectively etched using dry etching followed by a chemical etching to obtain misaligned PG and BG, respectively. At the end, by using sputtering method the nickel layer is and a specific annealing process is done to create NiSi at the S/D and gate contacts [31].

The process and flow mentioned above are based on well-known technologies, which have already been used in literature to implement fin shape RFET [31-32], gate misalignment [34] and independent gate [34] operation. Thus, it is possible to integrate the proposed structure in the RFET fabrication flow, which will enable the use as a capacitorless DRAM while retaining reconfigurability.

3.5 1T-DRAM Operation

Optimal functioning of 1T-DRAM requires optimal biases at different terminals to perform various operations. These biases are shown in Table 3.1. The analysis is commenced considering 10 ns of write time and 20 ns of read time. The functionality of 1T-DRAM is primarily governed by generation and distribution of holes during write operation, and maintaining the concentration in hold operation which are shown through the contour plots in Fig. 3.6 (a)-(d).

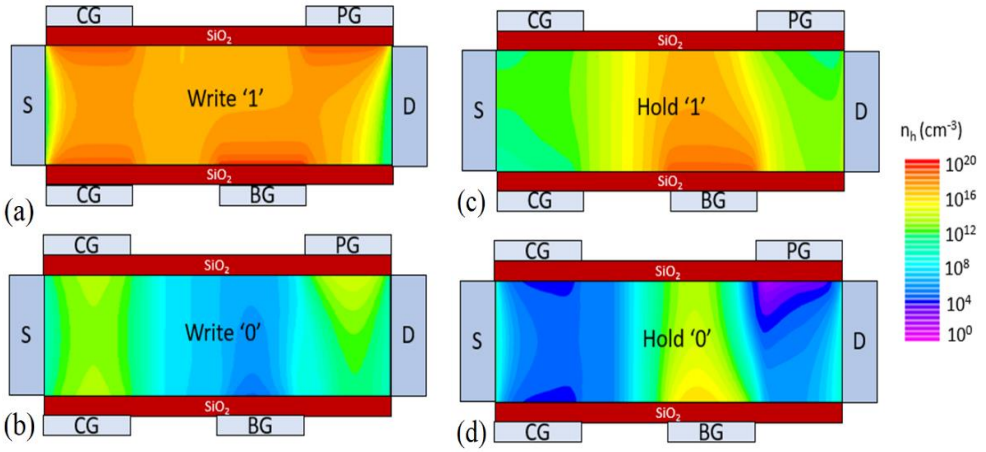


Fig. 3.6 Contour plots for hole concentration (n_h) during (a) write '1', (b) write '0', (c) hold '1' and (d) hold '0' operations of proposed (misaligned) 2G-RFET at 85°C. Parameters: $L_{CG} = L_{PG} = L_{BGAP} = L_{BG} = 25$ nm and $L_{FGAP} = 50$ nm. Biases are mentioned in Table 3.1.

The working principle of proposed (intentionally misaligned back gate) 1T-DRAM is explained in Fig. 3.7 (a)–(f) via band diagrams for various operations. Fig. 3.7 (a) shows the reference energy for zero applied bias. Excess carriers (holes) are generated during write '1' operation through impact ionization (II) and tunneling (Tun) through SB as shown in Fig. 3.7 (b). The

application of source (1.4 V) and drain (1.5 V) biases along with a negative BG bias (-1.5 V) results in a high electric field facilitating impact ionization. Also, a negative polarity gate bias (-0.2 V) is applied to lower the barrier for holes at SB to enable tunneling (Tun) as shown in Fig. 3.7 (b). The negative BG bias of -1.5 V is sufficient to create a potential well which can store excess holes. The write '0' mechanism involves removal of holes through the application of 1.5 V at BG as depicted shown in Fig. 3.7 (c).

Table 3.1

Biases and Time for Operation of Misaligned 2G RFET 1T-DRAM

	V_S (V)	V_D (V)	V_{PG} (V)	V_{CG} (V)	V_{BG} (V)	Time (ns)
write '1'	1.4	1.5	-0.2	0V	-1.5	10
write '0'	0.3	0.4	0	0.1	1.5	10
hold	-0.3	-0.3	1.5	0.4	-1.2	-
read	0	1	1.5	1.5	-0.26	20

To maintain excess carriers in hold operation after write '1', a negative BG bias (-1.2 V) is used. To prevent the tunneling of carriers to the source/drain Schottky junctions, a negative bias (-0.3V) is applied at source/drain which increases the tunneling width at the barrier. Also, front PG (1.5 V) and CG (0.4 V) voltages are maintained positive to decrease tunneling of hole from S/D to semiconductor (Fig. 3.7 (d)-(e)). As the storage region (at back surface) is moved away from the metal-semiconductor junction, it is not affected by the tunneling. Thus, hold '0' is degraded by the thermal generation while hold '1' is degraded by the thermal recombination. As the impact ionization and tunneling generate sufficient carrier concentration, the hold concentration during hold '1' is not affected by recombination. Therefore, the retention time of the structure is mainly limited by hold '0'.

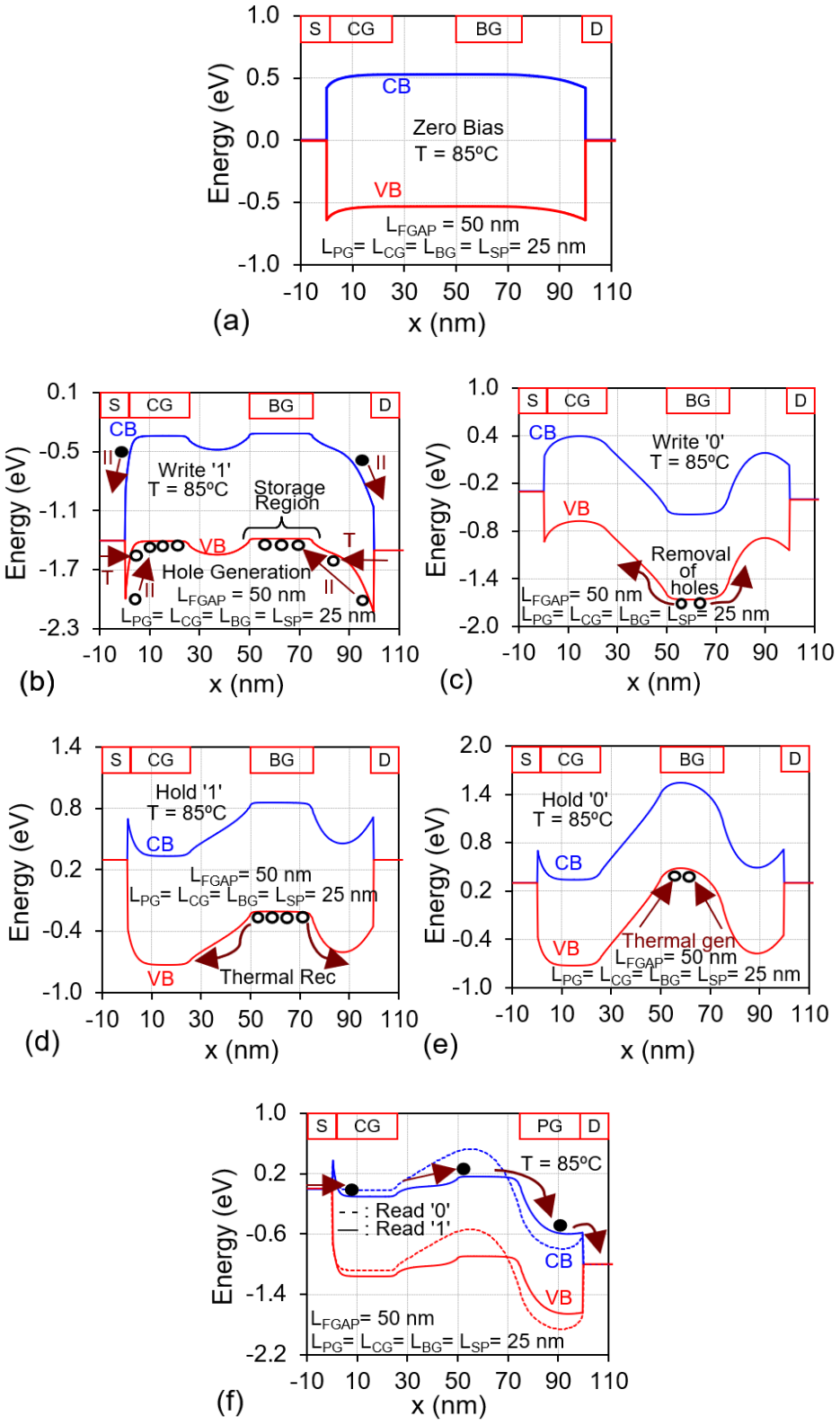


Fig. 3.7 1T-DRAM functionality through the variation of conduction and valance bands for (a) reference (zero bias), (b) write '1', (c) write '0', (d) hold '1', (e) hold '0' and (f) read operations. Band diagrams are extracted at 0.5 nm above the back surface in (a)–(e) and 0.5 nm below the front surface in (f).

The different levels of current i.e. I_1 and I_0 can be used can be used to separate states '1' and '0'. At the time of read operation, drain bias is made high (1 V) along with high polarity gate (1.5 V) and control gate (1.5 V) biases to decrease the barrier for electrons. The resistance to the current flow is mainly due to the ungated region. If the read follows hold '1', the positively charged excess holes at the back surface increases the potential at front surface and thus, decrease the energy barrier formed by ungated region (Fig. 3.7 (f)), causing a high read current (I_1) as shown in Fig. 3.6 (a). Similarly, if read operation follows hold '0', the omission of excess holes at the back surface does not affect the BH at the front surface (Fig. 3.6 (f)), producing a sufficient lower read current (I_0)

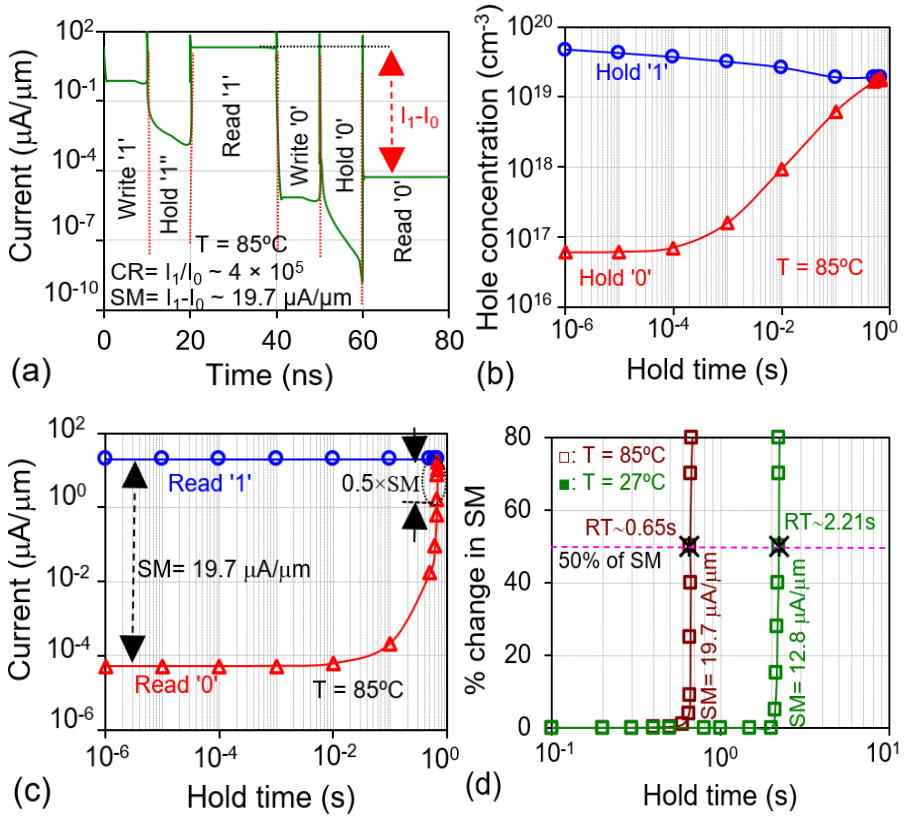


Fig. 3.8 (a) Variation of drain current transient for the proposed 1T-DRAM. (b) Variation of hole concentration in storage region with hold time during hold '1' and '0' operations. (c) Variation of read '1', read '0' currents with hold time. (d) Variation of percentage change in SM with hold time for 85°C and 27°C. All biases are same as mentioned in Table 3.1.

(Fig. 3.8 (a)). The proposed 2G-RFET showcases a high SM [36] of 19.7 µA/µm along with an impressive current ratio (CR = I_1/ I_0) of ~3×10^5 at 85ºC. As hold time increases, hold '0' concentration increases because of the thermal generation (Fig. 3.8 (b)) which decreases the front gate barrier formed by ungated region for read '0', and hence, I_0 increases (Fig. 3.8 (c)).

Hole concentration for hold '1' decreases with a minimal rate due to thermal recombination but I_1 does not change significantly with hold time due to subdued impact ionization during read '1', which prevents the degradation of I_1 (Fig. 3.8 (c)). Thus, SM and CR both decrease with the hold time as shown in Fig. 3.8 (c). The hold time value at which the difference (I_1–I_0) reaches 50% of its maximum value is termed as retention time (RT) [36]. At room temperature (27 ºC), the generation and recombination rates are low, which results in a smaller change in (I_1–I_0) as compared that exhibited at higher temperature (85 ºC). Thus, a retention time of 2.21 s and 665 ms achieved at 27 ºC and 85 ºC respectively (Fig. 3.8 (d)).

3.6 Conclusion

2G-RFET being intrinsic, of low fabrication complexity, and reconfigurable in nature can offer highly dense chip for logic operation. This chapter shows the excellent capability of RFET to be used as 1T-DRAM. It can be used as embedded DRAM which can bridge the gap between processor and DRAM technology. It also provides sufficient retention time (> 64 ms) and sense margin to be used for standalone application.

References

[1] Kim K. and Lee S. Y. (2007), Memory technology in the future, Microelectronics Engineering, 84, 1976-81.

[2] Lee S. H., (2016) Technology scaling challenges and opportunities of memory devices, Proceedings of IEEE International Electron Devices Meeting (IEDM), pp. 1-1.

[3] Wan J. Le Royer C., Zaslavsky A. and Cristoloveanu S. (2011), A compact capacitor-less high-speed DRAM using field effect-controlled charge regeneration, IEEE Electron Device Letters, 33, 179-181.

[4] Bawedin M., Cristoloveanu S. and Flandre D. (2007), Innovating SOI memory devices based on floating-Body effects, Solid-State Electronics, 51, 1252-1262.

[5] Fossum J. G., Lu Z. and Trivedi V. P. (2007), New insights on capacitorless floating-body DRAM cells, IEEE Electron Device Letters, 28, 513-516.

[6] Park Y.-H., Kook J. and Yoo H.-J., (2002) Embedded DRAM (eDRAM) power-energy estimation for system-on-a-chip (SoC) applications, Proceedings of ASP-DAC/VLSI Design 7th Asia and South Pacific Design Automation Conference and 15h International Conference on VLSI Design, pp. 625-630.

[7] Takato H., Koike H., Yoshida T. and Ishiuchi H., (1999) Embedded DRAM technology: past, present and future, Proceedings of International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers. (Cat. No.99TH8453), pp. 239-242.

[8] Furusawa H., Nogami S., Ogawa T., Kumazaki M., Okada N. and Yamamoto H. (2011), High-performance transistor evaluation for low-cost embedded DRAM, IEEE Workshop on Microelectronics and Electron Devices, 1-4.

[9] Marchi M. D., Zhang J., Frache S., Sacchetto D., Gaillardon P.-E., Leblebici Y. and Micheli G. D. (2014), Top–down fabrication of gate-all-around vertically stacked silicon nanowire FETs with controllable polarity (2014), IEEE Transactions Nanotechnology, 13, 1029–1038.

[10] Marchi M. D., Zhang J., Frache S., Sacchetto D., Gaillardon P.-E., Leblebici Y. and Micheli G. D. (2014), Configurable logic gates using polarity controlled silicon nanowire gate-all-around FETs, IEEE Electron Device Letters, 35, 880–882.

[11] Rai S., Trommer J., Raitza M., Mikolajick T., Weber W. M. and Kumar A. (2019), Designing Efficient Circuits Based on Runtime-Reconfigurable Field-Effect Transistors, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 27, 560-572.

[12] Sun B., Richstein B., Liebisch P., Frahm T., Scholz S., Trommer J., Mikolajick T., Knoch J. (2021), On the Operation Modes of Dual-Gate

Reconfigurable Nanowire Transistors, IEEE Transactions on Electron Devices, 68, 3684-3689.

[13] Sun Y., Shao J., Liu Z., Li X., Liu Y. and Shi Y. (2021), Evaluation of Single-Event-Transient Effects in Reconfigurable Field Effect Transistor Beyond 3 nm Technology Node, IEEE Transactions on Electron Devices, 68, 6001-6006.

[14] Cadareanu P. and Gaillardon P. -E. (2021), A TCAD Simulation Study of Three-Independent-Gate Field-Effect Transistors at the 10-nm Node, IEEE Transactions on Electron Devices, 68, 4129-4135.

[15] Trommer J., Heinzig A., Slesazeck S., Mikolajick T. and Weber W. M. (2014), Elementary Aspects for Circuit Implementation of Reconfigurable Nanowire Transistors, IEEE Electron Device Letters, 5, 141-143.

[16] Rai S., Raitza M., Sahoo S. S. and Kumar A. (2014), DiSCERN: Distilling Standard-Cells for Emerging Reconfigurable Nanotechnologies, 2020 Design, Reconfigurable Nanowire Transistors, IEEE Electron Device Letters, 35, 141-143.

[17] Zhang J., Gaillardon P. and Micheli G. D., (2013) Dual-threshold-voltage configurable circuits with three-independent-gate silicon nanowire FETs, Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2111-2114.

[18] Gaillardon P., Hasan M., Saha A., Amarú L., Walker R. and Rodriguez B. S., (2016) Digital, analog and RF design opportunities of three-independent-gate transistors, Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), pp. 405-408.

[19] Gaillardon P., Amaru L., Zhang J. and Micheli G. D., (2014) Advanced system on a chip design based on controllable-polarity FETs, Proceedings of Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 1-6.

[20] Matick R. E., and Schuster S. E. (2005), Logic-based eDRAM: Origins and rationale for use, IBM Journal of Research and Development, 49, 145-165.

[21] Navarro C., Barraud S., Martinie S., Lacord J., Jaud M. and Vinet M. (2017), Reconfigurable field effect transistor for advanced CMOS: Advantages and limitations, Solid-State Electronics, 128, 155-162.

[22] Widiez J., Jérôme L., Maud V., Thierry P., Bernard P., Frédéric D., Mireille M. and D. Simon (2005), Experimental evaluation of gate architecture influence on DG SOI MOSFETs performance, IEEE Transactions on Electron Devices, 52, 1772-1779.

[23] Trommer J., André H., Tim B., Stefan S., Thomas M. and Weber W. M. (2015), Functionality-enhanced logic gate design enabled by symmetrical reconfigurable silicon nanowire transistors, IEEE Transactions on Nanotechnology, 14, 689-698.

[24] Zhang J., Marchi M D., Sacchetto D., Gaillardon P., Leblebici Y. and De Micheli G. (2014), Polarity-Controllable Silicon Nanowire Transistors With Dual Threshold Voltages, IEEE Transactions on Electron Devices, 61, 3654-3660.

[25] Böckle R., Sistani M., Lipovec B., Pohl D., Rellinghaus B., Lugstein A., Weber W. M. (2022), A Top-Down Platform Enabling Ge Based Reconfigurable Transistors, Advanced Materials Technologies, 7, 2100647, 2022.

[26] Simon M., Liang B., Fischer D., Knaut M., Tahn A., Mikolajick T. and Weber W. M. (2020), Top-Down Fabricated Reconfigurable FET With Two Symmetric and High-Current On-States, IEEE Electron Device Letters, 41, 1110-1113.

[27] Marchi M. D., Sacchetto D., Zhang J., Frache S., Gaillardon P., Leblebici Y. and Micheli G. D. (2014), Top–Down Fabrication of Gate-All-Around Vertically Stacked Silicon Nanowire FETs With Controllable Polarity, IEEE Transactions on Nanotechnology, 13, 1029-1038.

[28] Sistani M., Böckle R., Falkensteiner D., Luong M. A., Hertog M. I. d., Lugstein A. and Weber W. M. (2021), Nanometer-Scale Ge-Based Adaptable Transistors Providing Programmable Negative Differential Resistance Enabling Multivalued Logic, ACS Nano, 15, 18135-18141.

[29] Heinzig A., Slesazeck S., Kreupl F., Mikolajick T. and Weber W. M. (2012), Reconfigurable Silicon Nanowire Transistors, Nano Letters, 12, 119-124.

[30] Heinzig A., Mikolajick T., Trommer J., Grimm D. and Weber W. M. (2013), Dually Active Silicon Nanowire Transistors and Circuits with Equal Electron and Hole Transport, Nano Letters, 13, 4176-4181.

[31] Zhang J., Trommer J., Weber W. M., Gaillardon P.-E. and Micheli G. D. (2015), On Temperature Dependency of Steep Subthreshold Slope in Dual-Independent-Gate FinFET, IEEE Journal of the Electron Devices Society, 3, 452-456.

[32] Zhang J., Marchi M. D., Gaillardon P. -E. and Micheli G. D., (2014) A Schottky-barrier silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 decades of current, Proceedings of IEEE International Electron Devices Meeting, pp. 13.4.1-13.4.4.

[33] Choi H. (2012), Vapor–Liquid–Solid Growth of Semiconductor Nanowires, In: Semiconductor Nanostructures for Optoelectronic Devices: Processing, Characterization and Applications, Springer, Berlin.

[34] Liu Y., Matsukawa T., Endo K., Masahara M., O'uchi S. -I., Ishii K., Yamauchi H., Tsukada J., Ishikawa Y. and Suzuki E. (2007), Cointegration of High-Performance Tied-Gate Three-Terminal FinFETs and Variable Threshold-Voltage Independent-Gate Four-Terminal FinFETs With Asymmetric Gate-Oxide Thicknesses, IEEE Electron Device Letters, 28, 517-519.

[35] Endo K., O'uchi S.-I., Ishikawa Y., Liu Y., Matsukawa T., Sakamoto K., Masahara M., Tsukada J., Ishii K., Yamauchi H. and Suzuki E. (2009), Independent-double-gate FinFET SRAM for leakage current reduction, IEEE electron device letters, 30, 757-759.

[36] Bhuvaneshwari Y. V., and Kranti A. (2021), Enhancing multi-functionality of reconfigurable transistors by implementing high retention capacitorless dynamic memory, Semiconductor Science and Technology, 36, 115003.

Chapter 4

Scalability and Sensitivity Assessment Twin Gated Reconfigurable Field Effect Transistor based 1T-DRAM

4.1 Introduction

An embedded 1T-DRAM (eDRAM) can favourably assist in speeding up the performance of a system [1]. Hence, the requirement of access time in eDRAM is different from a standalone 1T-DRAM. The access time write as well as read time is relatively lower which necessities a lower RT (~ 4 ms to 16 ms [2]) as compared to 64 ms for standalone applications [3]. In this chapter, we evaluate eDRAM cell operation through a 2G-RFET in a double gate (DG) configuration. As SM and RT offered by the proposed structure exceeds the requirement for 1T-DRAM (retention time > 64 ms [3]) even at lower access time, this device is also feasible for standalone applications.

To operate at high frequency and have high chip density, the major concerns of 1T-eDRAM are access time and scalability [2-9]. This chapter aims to discuss the effect of different parameters such as read and write time scaling, bias variation, length scaling and use of different spacing lengths (L_{SP}) and traps at interfaces on device performance and also provide a fair comparison of the device with the other reported devices.

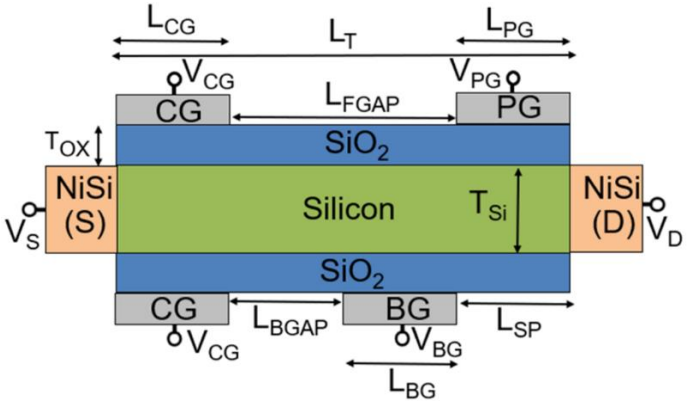


Fig. 4.1 Proposed misaligned 2G-RFET for 1T-DRAM.

4.2 Structure Optimization through change in back gate position and polarity gate length

The proposed structure shown in Fig. 4.1 overcomes the drawback of using traditional RFET for 1T-DRAM purpose through the misalignment of back gate as discussed in previous chapter. In this subsection, the effect of shifting of the position of back gate from the drain region i.e., spacing of storage region from the drain (L_{SP}) and polarity gate length (L_{PG}) is discussed.

For the given structure, as the BG position is moved towards the drain end, the resistance offered by the Schottky barrier near the back surface decreases. As a result, sense margin (SM) increases from 20 µA/µm to 28 µA/µm as L_{SP} decreases from 25 nm to 15 nm, respectively. On the other hand, if the L_{SP} increases i.e., the back gate is shifted towards the source end, the resistance offered by the ungated region increases. Thus, eventually the sense margin decreases from 20 µA/µm to 6 µA/µm as L_{SP} increases from 25 nm to 35 nm respectively which is observed in Fig. 4.2 (b). Similar to the effect of conventional RFET structure as 1T-DRAM, here, as the BG shifts closer to the drain, tunneling also increases. Therefore, it becomes difficult for the polarity gate and drain voltage alone to maintain the hole concentration at the storage region in hold operation. Hence, the retention time (RT) decreases from 565 ms to 8 ms as the L_{SP} decreases from 25 nm to 15 nm (Fig. 4.2 (a)). However, moving BG towards the source end increases retention time (up to 1400 ms at L_{SP} of 35 nm) as it decreases the effect of tunneling, and thus increasing the retention of carriers in the body region for longer duration which can be seen in Fig. 4.2 (a). Thus, to achieve retention time greater than 16 ms for eDRAM application [2], at least 16 nm of L_{SP} is required at 85 °C. However, for appreciable values of RT and SM, the optimal spacing of back gate from drain should be same as the polarity gate length i.e., the back gate should start from the point where polarity gate ends ($L_{SP} = L_{PG}$).

The effect of changing polarity gate length is shown in Fig. 4.2 (c)-(d). When the polarity gate length is increased keeping the starting point of polarity gate as the endpoint of BG, the back gate shifts away from the drain end. Hence, the effect of tunneling at the drain end decreases. Also, as the PG

length increases, the control over the Schottky barrier width by the polarity gate voltage increases due to existence of higher area. Thus, the carriers can be held for longer duration at the storage region. That is why when L_{PG} increases from 20 nm to 30 nm, the retention time increases from 165 ms to 1150 ms as shown in Fig. 4.2 (c). Decreasing the BG length causes the storage region to move towards the drain end. Thus, the resistance offered by the ungated region at the middle increases. Also, the control over the barrier by the polarity gate decreases. As a combining effect, the SM decreases which can be seen in Fig. 4.2 (d).

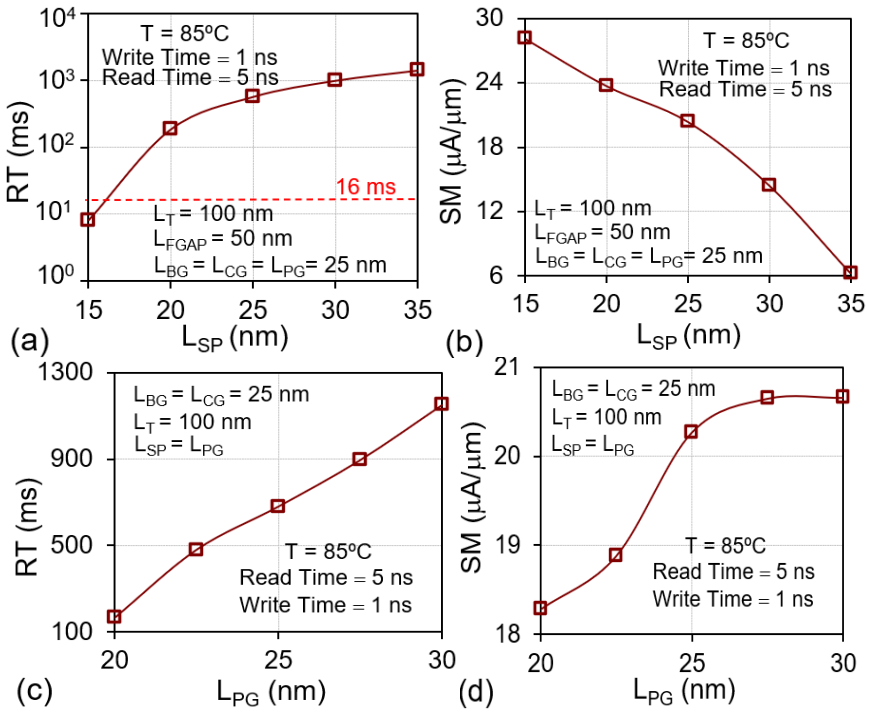


Fig. 4.2 Variation of (a) retention time (RT), and (b) Sense margin (SM), with spacing between storage region from drain side (L_{SP}) for a fixed polarity gate length (L_{PG}) of 25 nm. Variation of (c) RT, and (d) SM, with polarity gate length (L_{PG}) for $L_{SP} = L_{PG}$. Parameters: L_{CG} = 25 nm, L_{BG} = 25 nm, T_{Si} = 10 nm, T_{ox} = 1.5 nm, at 85°C.

4.3 Effect of read and write time scaling on device performance

An efficient and fast 1T-eDRAM must operate at lower values of write time and read time. Write operation, which involves generation of holes, can

be realized through impact ionization and tunneling at source/drain regions. These essentially limit the lowering of write time.

The write ‘1’ process is dependent on both impact ionization and tunneling. Because of the combining effect of both, the generation of excess holes at the body takes very low time. As a result, even if the write time (t_W) is scaled down from 10 ns to 1 ns, the excess hole concentration remains same throughout the write ‘1’ process for the same write ‘1’ bias as shown in Fig. 4.3.

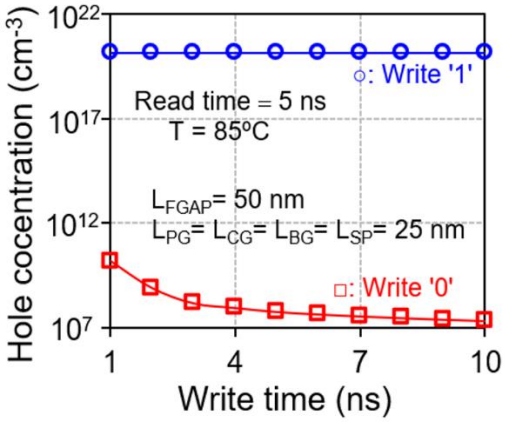


Fig. 4.3 Variation of Hole concentration during write ‘1’ and write ‘0’ for different write time.

In write ‘0’ process, the holes from the storage region are depleted through a positive bias at the BG and this process takes finite amount of time. It is observed from Fig. 4.3 that for a lower write time, BG is unable to deplete the body region sufficiently and as a result, the hole concentration increases at the storage region. Therefore, the minimum write time is mainly limited by the time taken to deplete the holes in write ‘0’ configuration. However, a very low write time of 1 ns can be used where the hole concentration is sufficient for both write operations to be followed by hold operations without compromising RT and SM. Thus, SM and RT both remain almost constant throughout the scaling of write time from 10 ns to 1 ns.

In read operation, a slight negative BG bias is applied to retain the carriers of hold configuration and affect the current at the top gate region. A high hole concentration at the storage region increases the body potential and thus reduces the barrier offered by ungated region at front surface. As a result,

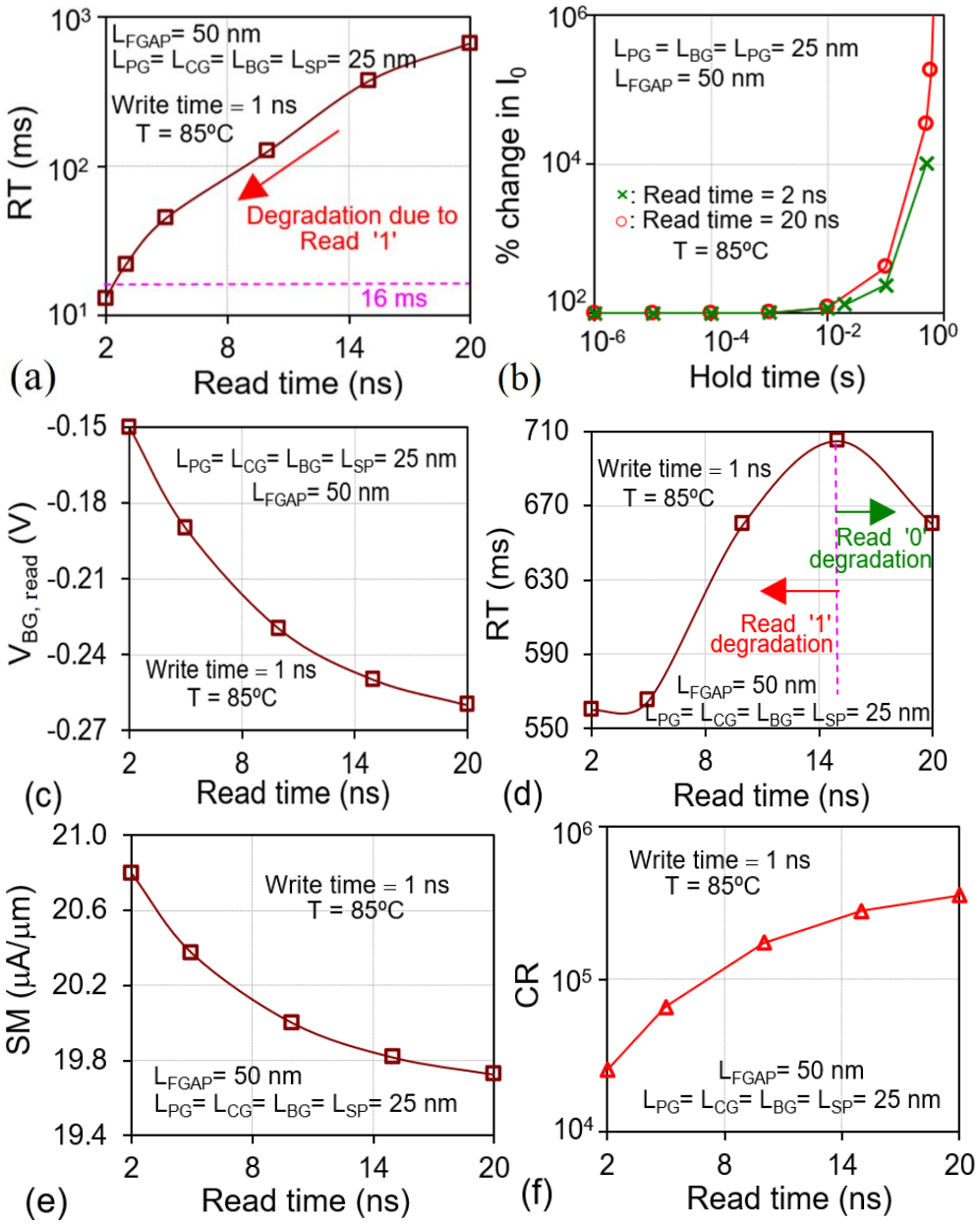


Fig. 4.4 (a) Variation of retention time (RT) with read time for the same set of biases as shown in Table 3.1 in previous chapter. (b) Variation of read '0' currents with hold time for read time of 2 ns and 20 ns. (c) Variation of back gate read bias ($V_{BG,read}$) needed for different read time for memory operation. Variation of (d) RT, (e) SM, and (f) CR with read time for individual optimized $V_{BG,read}$ at 85°C. All the parameters are same as mentioned in figures.

a high read '1' current (I_1) flows. On the other hand, low hole concentration at the storage region is hardly able to increase the body potential, and thus, cannot affect the barrier at the ungated region resulting in a very low read '0'

current (I_0). In read '1' operation if this barrier is low, the current (I_1) rises sharply and saturates to its maximum value at a very low time. If the hold time is of high duration, due to thermal recombination the excess hole concentration during hold '1' reduces, causing the barrier to not decrease significantly during read '1'. As a result, read '1' current degrades. However, a lower excess hole concentration during read '0' results in a very low and nearly constant I_0 current level. But, during hold '0', due to thermal generation, the hole concentration increases with time. Therefore, when read '0' is followed by hold for longer duration, due to a higher hole concentration at the storage region, I_0 increases and the degradation of read '0' current is observed. Thus, read operation time significantly affects the fall of I_1 and rise of I_0. That is why when read time is reduced by 10 times starting from 20 ns, the retention time decreases from 660 ms to 13 ms due to degradation in read '1' as shown in Fig. 4.4 (a) as at lower read time, the operation does not allow the current to rise to its saturation value for that hold time. For the same reason, the smaller read time also does not allow I0 to rise at higher rate which is observed in Fig. 4.4 (b).

However, the lowering of RT can be checked by using a lower negative back gate bias at low read time as shown in Fig. 4.4 (c). At less negative $V_{BG,read}$, the energy barrier for the electrons is already decreased which causes current I_1 to increase at a faster rate to sufficient level even when the read time has low values. Thus, read current depends on both excess hole concentration and BG bias during read operation. An optimum negative BG bias during read operation is necessary to obtain an RT of 560 ms even at 2 ns of read time as shown in Fig. 4.4 (d).

A lower read time also prevents the increment of I_0 at higher hold time. As a result, when the read time is reduced from 20 ns to 15 ns, the retention time increases from 665 ms to 705 ms as shown in Fig. 4.4 (d). Reducing the read time even further ceases the increment of I_0 as well as I_1. Hence, a lower read time (< 15 ns) contributes to lowering of RT due to the degradation in I_1 at higher hold time. Fig. 4.4 (d)-(f) show that a high retention time of 560 ms can be achieved along with a sufficient sense margin (~19.7 µA/ µm) and current ratio (~2.5×10^4). A higher sense margin is obtained at lower read time

because of a less negative $V_{BG,read}$. At the same time, as I_0 also increases, the current ratio decreases to ~4 orders.

4.4 Effect of bias variation on device performance

The hold and read biases are most important to analyse here as they directly affect the key performance parameters of 1T-DRAM, sense margin and retention time. An optimized set of hold and read biases are necessary to have a high retention time.

In hold operation, to retain the generated or depleted holes of write operation for a longer duration, appropriate bias is necessary. In the proposed twin-gated RFET, the degradation of state '0' is more dominant than that of state '1' due to thermal generation. Hence, proper biasing is necessary at both polarity and control gate sides to modulate the Schottky barrier width to avoid tunneling of any additional carrier to improve retention. A higher positive control gate bias ($V_{CG,hold}$) increases barrier width for holes at the source side which prevents the degradation of state '0' through source end. Similarly, a higher positive voltage at the polarity gate ($V_{PG,hold}$) increases the SB width for holes at drain end, and thus, prevents the degradation of state '0' from drain side. From Fig. 4.5 (a)-(b) it can be understood that to prevent the degradation of state '0' a bias greater than 0.3 V is necessary at both polarity and control gates. For back gate region, a sufficient negative voltage is necessary to retain the excess holes of write '1'. A low negative back gate voltage ($V_{BG,hold}$) causes the recombination holes as it cannot retain all the holes, and thus, state '1' degrades. A high negative BG voltage increases the electric field between back gate and polarity gate region which causes the hole generation due to impact ionization during hold '0' and state '0' degrades. Thus, an optimal bias at back gate is also necessary (Fig. 4.5 (c)). The Schottky barrier width at the source and drain region are also affected by source and drain biases. High negative source and drain biases reduce the barrier width for electrons, which causes degradation of state '1' through the recombination process during state '1' (Fig. 4.5 (c)). However, a less negative bias at source and drain reduces the barrier width for holes causing degradation of state '0' through the generation of holes by tunneling during state '0' (Fig. 4.5 (c)).

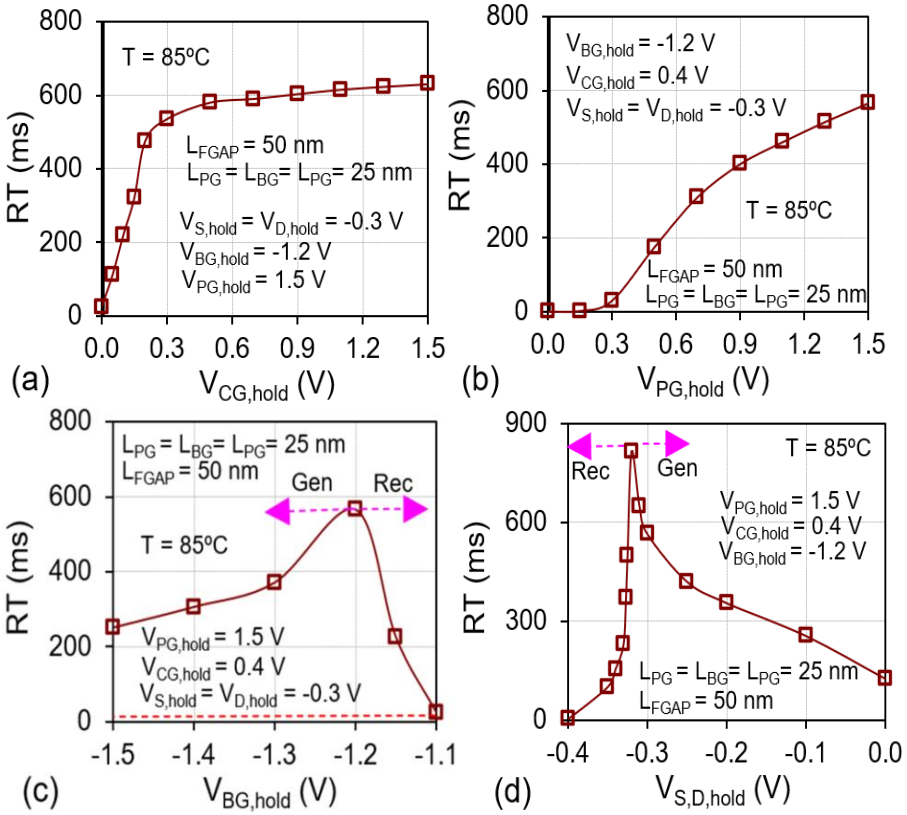


Fig. 4.5 Variation of retention time (RT) with (a) control gate bias, (b) polarity gate bias, (c) back gate bias, and (d) drain/source bias during hold operation. Parameters: L_{CG} = 25 nm, L_{BG} = 25 nm, T_{Si} = 10 nm, T_{ox} = 1.5 nm, at 85°C.

In read configuration, the hole concentration after hold configuration has to be retained at the storage region to affect the on current flowing at the top gate region. For that, a low negative bias ($V_{BG,read}$) can be used. If the back gate voltage is very high, the barrier at the ungated region becomes so high that the holes stored at the back gate are hardly able to decrease the barrier at high hold duration (as the hole concentration of hold '1' state reduces over hold time). However, for low hold duration, the holes are able to reduce this barrier because of presence of high hole concentration. As a result, the retention time decreases. On the other hand, for a low negative BG voltage, the barriers are lowered by read '0' stored hole concentration at the back gate. As a result, the difference between read '1' and read '0' currents decrease sharply over hold time. As a result, the retention time decreases. Thus, at high negative back gate bias retention time decreases due to read '1' state degradation and at low negative back gate bias retention time decreases due to read '0' state degradation. An optimal back gate bias is thus necessary to have

high retention time which is found to be around -0.25 V from Fig. 4.6. However, the sense margin remains the same as it is obtained at very low hold time when the hole concentration is very high in hold '1' state, and thus, the barrier in read '1' configuration is reduced sufficiently.

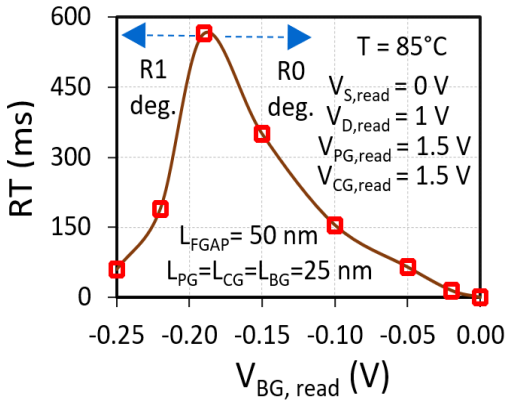


Fig. 4.6 Variation of RT with BG bias during read operation.

4.5 Effect of length scaling on device performance

To increase the density of 1T-eDRAM, the downscaling of total length ($L_T = L_{CG} + L_{PG} + L_{FGAP}$) is required. The variation of RT and SM with the total length is shown in Fig. 4.7. To scale the device, the length of control gate and polarity gate are considered to be 1/4th of total length i.e., $L_{CG} = L_{BG} = 0.25 \times L_T$. The spacing of back gate from drain end (L_{SP}) is kept equal to the polarity gate length to overcome the trade-off between SM and RT as described in section 4.2. As the total device length is scaled down from 120 nm to 80 nm, all the gate lengths and spacing are also decreased. As a result, the control over the carrier leakage by the polarity gate and control gate also decreases. Also, the back gate becomes closer to the drain region. Hence the retention time decreases from 1550 ms to 135 ms as shown in Fig. 4.7 (a). On the other hand, with decreasing length the resistance at the ungated middle region decreases, causing current to increase at lower device length. Hence a high sense margin of 20.3 µA/µm can be obtained at L_T of 80 nm which can be seen in Fig. 4.7 (b). For L_T = 60 nm and $L_{PG} = L_T/4$, the retention time decreases to 3 ms due to the dominant contribution of Schottky barrier tunneling at the drain on the storage region because of the shorter PG length (15 nm) and close position of the back gate to drain end. Hence a higher

polarity gate length (L_{PG} = 20 nm) can be used in total length 60 nm device keeping all other gate lengths to 15 nm and reducing the front gap to 25 nm. This improves the retention time to 50 ms (> 16 ms at 85 °C) and also attains a high sense margin of 30 µA/µm as the ungated spacing region length is decreased.

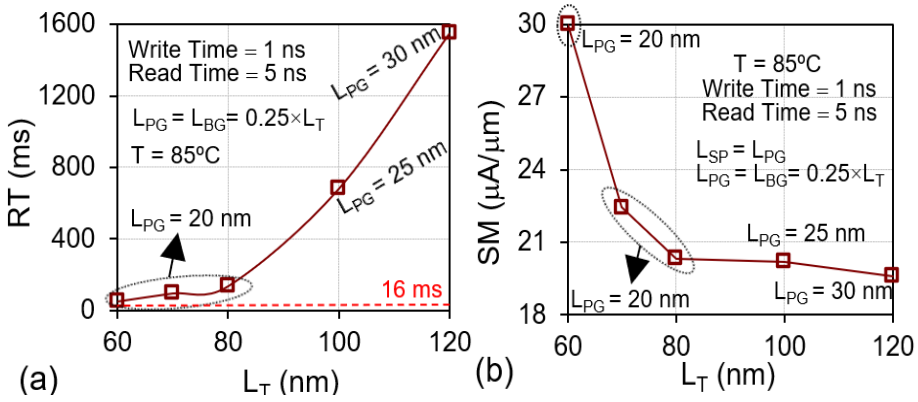


Fig. 4.7 Variation of (a) Retention time (RT), and (b) Sense margin (SM), with total silicon film length (L_T). Parameters: $L_{CG} = L_{BG} = 0.25 \times L_T$, read time = 5 ns, write time = 1 ns, T_{Si} = 10 nm, T_{ox} = 1.5 nm, at 85°C.

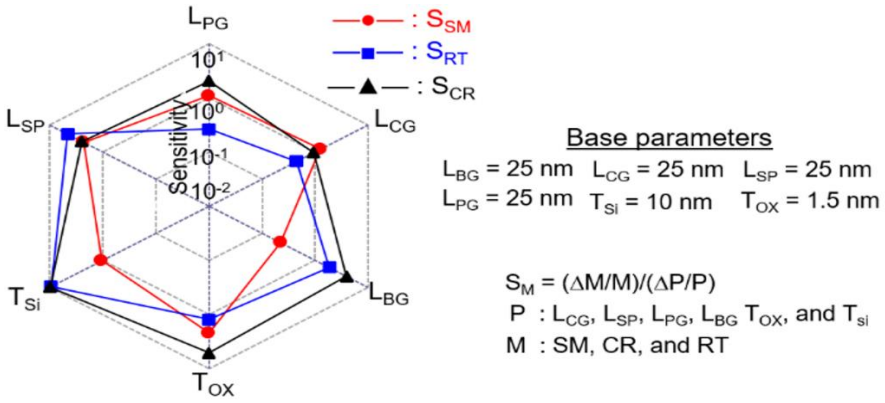


Fig. 4.8 Sensitivity of sense margin (S_{SM}), retention time (S_{RT}), and current ratio (S_{CR}) for ±5% variation in dimensions around their mean values at 85°C [10]. Parameters: $L_{CG} = L_{PG} = L_{BG} = L_{SP}$ = 25 nm, T_{Si} = 10 nm and T_{ox} = 1.5 nm.

4.6 Performance sensitivity of the proposed 2G-RFET

The sensitivity of a metric (M) to a parameter (P) has been evaluated by considering a total 10% (±5%) variation in P around their optimum values (Fig. 4.8) [10]. Among all the parameters, current ratio and retention time are more sensitive to T_{Si} as it governs the gate controllability of the storage region.

As the length and position of the storage region are governed by L_{BG} and L_{SP}, retention time is more sensitive to these parameters. Read currents depend on the gate field, which is a strong function of T_{OX}. Thus, sense margin and current ratio are more sensitive to T_{OX}. The position of BG strongly influences 1T-DRAM performance, which results in high sensitivity to L_{SP} on all the metrics. As the read current flows through the front surface, the sensitivity of sense margin on L_{BG} is low. However, both retention time and current ratio are very sensitive to L_{BG} as it governs the length of the storage region. Among all the parameters L_{PG} has the least sensitivity to all metrics for a fixed L_{SP}.

4.7 Effect of traps at a metal-semiconductor junction

The traps or the defects which are present at the M-S interface [11] strongly affect the Schottky barrier-based devices. Here, the interfacial layers create traps in the bandgap which pins the Fermi level at a particular position irrespective of the work function of the metal. This phenomenon is called the Fermi Level Pinning [12]. This causes an increase in Schottky barrier height for a particular type of carrier. An increase in barrier height because of Fermi level pinning depends on metal work function as well as interface trap charge density at M-S junction [11]. For the taken metal work function at source and drain region of 4.6 eV and typical interface charge density (D_{it}) of 10^{12} $cm^{-2}eV^{-1}$, the barrier height foe electrons increases to 0.51 eV from 0.43 eV. Therefore, if this is modelled in terms of increased barrier height at source and drain end, the sense margin decreases from ~20.37 µA/µm to ~9.46 µA/µm as shown in Fig. 4.9. Poor fabrication process results in traps at semiconductor-oxide (Si-SiO_2) interface also, which affects the lifetime of the carriers [13] specifically which are stored at the interface region (back gate storage region). In order to model the effects of traps at Si/SiO_2 interface, a lower lifetime of the carriers such as 10 ns is considered [13]. Lower lifetime of carriers significantly affects the retention time. This can be seen in Fig. 4.9 where due to this reduced lifetime (10 ns at 85 °C) the retention time decreases to 175 ms from 565 ms (for 76 ns lifetime at 85 °C [14]). However, since the retention time is still higher than 64 ms at 85 °C, it is still eligible for 1T-DRAM purpose. In the planar SOI process, the mean interface trap density (D_{it}) is less that that observed in non-planar geometries, and D_{it} lies in the order of

10^{10}~10^{11} cm^{-2} eV^{-1} [15]. The interface trap density can be reduced by growing the gate oxide thermally [16]. Due to a less mature fabrication process, higher trap density may exist in the device which may cause severe degradation in the performance of 1T-DRAM. The maturing of silicon fabrication and processing technology [16] over the years is expected to minimize traps at Si/SiO_2 interface through the high-temperature annealing processes.

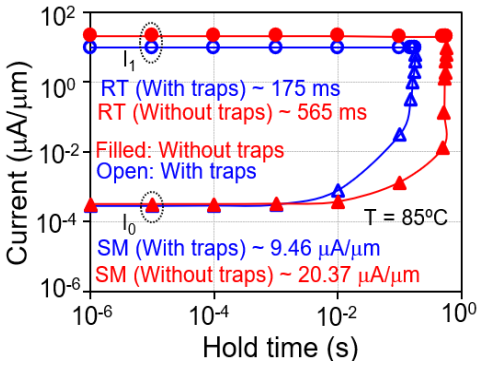


Fig. 4.9 Comparison of read current with hold time for a device with and without traps at 85°C

4.8 Performance Comparison of 2G-RFET based devices with other devices

For eDRAM, the typical SM needed for detection through current mode sense amplifier is 5 uA/um [17] and the RT required is 4-16 ms [2]. The standalone 1T-DRAM has similar requirements as that of the 1T-eDRAM [3]. However, a lower access time is mandatory for eDRAM compared to standalone application to operate at higher frequency. The comparison of different devices regarding retention time, sense margin, read time, write time and body length are shown in Table 4.1. The 1T-DRAM devices based on Ga-As JLFET [22], ARAM [23], A2RAM [24], SISOI [25] and IMOS [26] may provide sufficient sense margin, but the access times are comparatively higher than the 2G-RFET based 1T-DRAM. The retention time of 1T-Bulk [17] and GIDL based FDSOI [18] 1T-DRAM devices are also lower than the RFET based device reported here with the corresponding comparable length. DG-FinFET [19], DG nMOSFET [21] and Z^2FET [28] are comparable to 2G-RFET in terms of write time. But both DG-FinFET and DG-nMOSFET suffer

from low RT and SM. In case of Z^2FET, the absence of the reconfigurability feature makes RFET more suitable for eDRAM along with logic implementation. Hence, overall, RFET based 1T-DRAM has great advantage of lower access time along with high sense margin and retention time to be implemented as 1T-eDRAM compared to other devices.

Table 4.1

Performance comparison among reported devices for 1T-DRAM

Architecture	T°C	L_T (nm)	RT (ms)	SM (µA/µm)	Read Time(ns)	Write Time(ns)
1T-Bulk[17]	85	65	10	40	5	5
FDSOI (GIDL)[18]	85	350	100	12	5	5
DG FinFET[19]	85	60	10	5	2	1
JLFET[20]	85	420	0.2	2.76	-	10
DG nMOSFET[21]	27	10	Few ms	2	-	1
Ga-As JLFET[22]	27	45	100	50	10	10
ARAM[23]	85	28	30	16.5	-	10
A2RAM[24]	85	100	20	60	-	10
SISOI[25]	27	100	1600	65	10	10
IMOS[26]	85	150	320	3	10	10
TFET[27]	85	245	600	0.18	50	5
Z^2FET[28]	75	60	150		1	1
RSD MOSFET[29]	85	30	15	3.3	10	5
2G-RFET (this work)	85	100 60	560 60	20.8 30.8	2 2	1 1

4.9 Conclusion

In this chapter we have discussed effect of different parameters on device performance metrics (sense margin and retention time mainly). Also, the feasibility of the device to work at low write and read time have been discussed which makes the device suitable for 1T-DRAM as well as 1T-eDRAM purpose. Finally, the device has been compared to some other well-known as well as newly reported devices to get a fair idea of 1T-DRAM trends.

References

[1]. Matick R. E. and Schuster S. E. (2005), Logic-based eDRAM: Origins and rationale for use, IBM Journal of Research and Development, 49, 145-165.

[2]. Yang H., Chang C., Chao M. C. -T., Huang R. and Lin S. (2012), Testing Methodology of Embedded DRAMs, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 20, 1715-1728.

[3]. International Technology Roadmap for Device and System (IDRS), 2020.

[4]. Gong Y.-H., Jang H. B. and Chung S. W., (2013) Performance and cache access time of SRAM-eDRAM hybrid caches considering wire delay, Proceedings of International Symposium on Quality Electronic Design (ISQED), pp. 524-530.

[5]. Park Y.-H., Kook J. and Yoo H.-J. (2002), Embedded DRAM (eDRAM) power-energy estimation for system-on-a-chip (SoC) applications, (2002) Proceedings of ASP-DAC/VLSI Design 7th Asia and South Pacific Design Automation Conference and 15h International Conference on VLSI Design, pp. 625-630.

[6]. Takato H., Koike H., Yoshida T. and Ishiuchi H., (1999) Embedded DRAM technology: past, present and future, Proceedings of International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers. (Cat. No.99TH8453), pp. 239-242.

[7]. Furusawa H., Nogami S., Ogawa T., Kumazaki M., Okada N. and Yamamoto H. (2011), High-performance transistor evaluation for low-cost embedded DRAM, IEEE Workshop on Microelectronics and Electron Devices,1-4.

[8]. Park K., Park C. M., Kong S. H. and Lee J. (2010), Novel Double-Gate 1T-DRAM Cell Using Nonvolatile Memory Functionality for High-Performance and Highly Scalable Embedded DRAMs, IEEE Transactions on Electron Devices, 57, 614-619.

[9]. Okhonin S., Fazan P. and Jones M. -E., (2005) Zero capacitor embedded memory technology for system on chip, Proceedings of IEEE International Workshop on Memory Technology, Design, and Testing (MTDT'05), pp. xxi-xxv.

[10].Lim T. C. and Armstrong G. A. (2005), Parameter sensitivity for optimal design of 65 nm node double gate SOI transistors, Solid-state electronics, 49, 1034-1043.

[11].Tung R. T. (2014), The physics and chemistry of the Schottky barrier height, Applied Physics Reviews, 1.

[12].Streetman, B. G., Banerjee, S., (2015) Solid State Electronic Devices. seventh ed. Upper Saddle River, New Jersey (9780133356649).

[13].Wan J., Royer C. L., Zaslavsky A. and Cristoloveanu S. (2013), Progress in Z2-FET 1T-DRAM: Retention time, writing modes, selective array operation, and dual bit storage, Solid-State Electronics, 84, 147-154.

[14].Bhuvaneshwari Y. V., and Kranti A. (2021), Enhancing multi-functionality of reconfigurable transistors by implementing high retention capacitorless dynamic memory, Semiconductor Science and Technology, 36, 115003.

[15].Weber W. M. and Mikolajick T. (2017), Silicon and Germanium Nanowire Electronics: Physics of Conventional and Unconventional Transistors, Reports on Progress in Physics, 80.

[16].Deal B. E., Sklar M., Grove A. S. and Snow E. H. (1967), Characteristics of the surface-state charge (Q_{ss}) of thermally oxidized silicon, Journal of the Electrochemical Society, 114, 266.

[17].Ranica R., Villaret A., Malinge P., Mazoyer P., Lenoble D., Candelier P., Jacquet F., Masson P., Bouchakour R., Fournel R., Schoellkopf J. P. and Skotnicki T., (2004) A one transistor cell on bulk substrate (1T-Bulk) for low-cost and high density eDRAM, Digest of Technical Papers, Proceedings of Symposium on VLSI Technology, pp. 128-129.

[18].Puget S., Bossu G., Fenouiller-Beranger C., Perreau P., Masson P., Mazoyer P., Lorenzini P., Portal J. M., Bouchakour R. and Skotnicki T., (2009) FDSOI floating body cell eDRAM using gate-induced drain-leakage (GIDL) write current for high speed and low power applications, Proceedings of IEEE International Memory Workshop, pp. 1-2.

[19].Hou J., Shao Z. and Miao X., (2009) A High speed low power capacitorless SOI-DRAM cell using impact ionization and GIDL effect,

Proceedings of IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), pp. 517-520.

[20].Ansari M. H. R., Navlakha N., Lin J.-T. and Kranti A. (2018), Doping dependent assessment of accumulation mode and junctionless FET for 1T DRAM, IEEE Transactions on Electron Devices, 65, 1205–1210.

[21].Giusi G. and Iannaccone G. (2013), Junction engineering of 1T-DRAMs, IEEE Electron Device Letters, 34, 408–410.

[22].Yoon Y. J., Seo J. H., Cho M. S., Kim B. G., Lee S. H. and Kang I. M. (2017), Capacitorless one-transistor dynamic random access memory based on double-gate GaAs junctionless transistor, Japanese Journal of Applied Physics, 56.

[23].Rodriguez N., Cristoloveanu S. and Gamiz F. (2011), Capacitor-less A-RAM SOI memory: Principles, scaling and expected performance, Solid-State Electronics, 59, 44–49.

[24].Rodriguez N., Cristoloveanu S. and Gamiz F. (2011), Novel Capacitorless 1T-DRAM Cell for 22-nm Node Compatible With Bulk and SOI Substrates, IEEE Transactions on Electron Devices, 58, 2371-2377.

[25].Lee W. and Choi W. Y. (2011), A Novel Capacitorless 1T DRAM Cell for Data Retention Time Improvement, IEEE Transactions on Nanotechnology, 10, 462-466.

[26].Lahgere A. and Kumar M. J. (2017), 1-T Capacitorless DRAM Using Bandgap-Engineered Silicon-Germanium Bipolar I-MOS, IEEE Transactions on Electron Devices, 64, 1583-1590.

[27].Navlakha N., Ansari M. H. R., Lin J. -T. and Kranti A., (2018) Performance Assessment of TFET Architectures as 1T-DRAM, Proceedings of IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp. 1-3.

[28].Wan J., Royer C. L., Zaslavsky A. and Cristoloveanu S., (2012) Z2-FET used as 1-transistor high-speed DRAM, Proceedings of the European Solid-State Device Research Conference (ESSDERC), pp. 197-200.

[29].Ansari M. H. R. and Cho S. (2021), Performance Improvement of 1T DRAM by Raised Source and Drain Engineering, IEEE Transactions on Electron Devices, 68, 1577-1584.

Chapter 5

Conclusion and Scope for Future Work

5.1 Conclusion

This chapter aims to provide summary of different features corresponding to use of twin-gated RFET for 1T-DRAM purpose. The idea of Reconfigurable Field Effect Transistor (RFET) [1-12] has been derived from Schottky Barrier Field Effect Transistor (SBFET) structure which employs two M-S junctions at source and drain. In, SBFET, a single gate is employed to control the current in the device. However, it suffers from ambipolar behavior of the current. To suppress that ambipolarity, another gate is employed at the source side. These two gates are separated and controlled independently to achieve reconfigurability. The RFET, being intrinsic and the use of simple M-S junctions at source and drain counter the issues of fabrication process complexity and cost (low thermal budget) are reduced. On the other hand, due to reconfigurable nature the separate need of fabricating p-type device like CMOS counterpart is not needed at all. At the logic implementation level, this decreases number of transistors to be used compared to standard CMOS logic.

The research work presented in the thesis first describes the non-usability of conventional 2G-RFET as 1T-DRAM. It is seen that as the back gate region was at the drain end, the charges at the back gate are depleted or generated in the hold condition at a very higher rate which resulted in no difference between ‘1’ or ‘0’ state. Hence, a new structure is proposed where the back gate is misaligned from the polarity gate. Here, as the back gate is moved away from the drain end, a high speed (1 ns read time and 2 ns write time), high RT (660 ms at 85°C for 100 nm body) standalone DRAM performance is achieved. Other aspects of DRAM, such scalability and access time scaling are also discussed. As, for write ‘1’ operation, this device uses both impact ionization and tunneling methods, the device is very fast in charge generation. However, as charge depletion takes a higher time, the write time is limited by write ‘0’ process. The read time is sensitive to bias and detailed

analysis corresponding to it is given. A low read time (2 ns) is also proven to be sufficient to attain a high retention time (~ 560 ms) along with high sense margin (20.8 µA/µm). The scalability analysis is done to provide a clear picture of the parameters which affect the performance of the device most. It is found that spacing of back gate from drain end, silicon body thickness and back gate length have the highest sensitivity on retention time. To achieve a high RT, the back gate can be moved further away from the drain (1400 ms retention time), but at the cost of reducing sense margin (6.2 µA/µm). In order to investigate the effect of traps at the Si-SiO_2 interface as well as the Schottky barriers, the modelling is done in two ways. The effect traps at Schottky barrier is modelled through an increase in barrier height for electrons which has a detrimental effect mainly on sense margin (9.46 µA/µm). On the other hand, the traps at the Si-SiO_2 interface are expected to reduce the lifetime of carriers [13], and thus, DRAM performance is measured at low lifetime (10 ns) which has resulted a low retention time (175 ms). Even though for these analysis, different level of biases are necessary, simplified bias levels can also be used to attain a high degree of performance [14]. Therefore, overall, this thesis presents the RFET a suitable candidate not only for logic operation but also for low power memory applications.

5.2 Scope for future work

Different devices which have been reported in the past few decades along with the RFET could be a great replacement of conventional 1T-1C DRAM but are still not viable for commercial use. However, significant research in the past decade has shown a great deal of interest in using RFET [1-12] for processor applications. Hence, along with that, RFET for memory application is expected to attract a lot of attention.

Today, eDRAMs are attracting a lot of attention for cheaper, faster and low voltage embedded applications. The fabrication cost associated with capacitor in 1T-1C for embedded applications can be reduced through use of RFET as the same structure can be used for logic and memory operations, which have been demonstrated in this thesis as reliable, low power and high speed DRAM device. However, further investigations are necessary at circuit

level as well as the implementation (fabrication) level in order to analyse bit line and word line disturbance as well as some other effects to which 1T-DRAM performances are sensitive such as Random Dopant Fluctuations (RDFs), radiation effects [15-16], row-hammering [17], etc. This would serve as a guideline to device and circuit engineers and be useful to semiconductor society to develop dynamic memories.

References

[1] Trommer J., Heinzig A., Baldauf T., Slesazeck S., Mikolajick T. and Weber W. M. (2015), Functionality-enhanced logic gate design enabled by symmetrical reconfigurable silicon nanowire transistors, IEEE Transactions on Nanotechnology, 14, 689-698.

[2] Navarro C., Barraud S., Martinie S., Lacord J., Jaud M. and Vinet M. (2017), Reconfigurable field effect transistor for advanced CMOS: Advantages and limitations, Solid-State Electronics, 128, 155-162.

[3] Marchi M. D., Zhang J., Frache S., Sacchetto D., Gaillardon P.-E., Leblebici Y., and Micheli G. D. (2014), Top–down fabrication of gate-all-around vertically stacked silicon nanowire FETs with controllable polarity, IEEE Transactions on Nanotechnology, 13, 1029–1038.

[4] Marchi M. D., Zhang J., Frache S., Sacchetto D., Gaillardon P.-E., Leblebici Y., and Micheli G. D. (2014), Configurable logic gates using polarity controlled silicon nanowire gate-all-around FETs, IEEE Electron Device Lett., 35, 880–882.

[5] Zhang J., Marchi M. D., Sacchetto D., Gaillardon P., Leblebici Y. and Micheli G. D. (2014), Polarity-Controllable Silicon Nanowire Transistors With Dual Threshold Voltages, IEEE Transactions on Electron Devices, 61, 3654-3660.

[6] Böckle, R., Sistani, M., Lipovec, B., Pohl, D., Rellinghaus, B., Lugstein, A., Weber, W. M. (2022), A Top-Down Platform Enabling Ge Based Reconfigurable Transistors, Adv. Mater. Technol., 7, 2100647.

[7] Simon M., Liang B., Fischer D., Knaut M., Than A., Mikolajick T. and Weber W. M. (2020), Top-Down Fabricated Reconfigurable FET With Two Symmetric and High-Current On-States, IEEE Electron Device Letters, 41, 1110-1113.

[8] Sistani M., Böckle R., Falkensteiner D., Luong M. A., Hertog M. I. D., Lugstein A. and Weber W. M. (2021), Nanometer-Scale Ge-Based Adaptable Transistors Providing Programmable Negative Differential Resistance Enabling Multivalued Logic, ACS Nano, 15, 18135-18141.

[9] Simon M., Heinzig A., Trommer J., Baldauf T., Mikolajick T. and Weber W. M. (2017), Top-Down Technology for Reconfigurable Nanowire FETs With Symmetric On-Currents, IEEE Transactions on Nanotechnology, 16, 812-819.

[10] Heinzig A., Slesazeck S., Kreupl F., Mikolajick T. and Weber W. M. (2012), Reconfigurable Silicon Nanowire Transistors, Nano Letters, 12, 119-124.

[11] Gaillardon P., Hasan M., Saha A., Amarú L., Walker R. and Rodriguez B. S., (2016) Digital, analog and RF design opportunities of three-independent-gate transistors, Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), pp. 405-408.

[12] Gaillardon P., Amaru L., Zhang J. and Micheli G. D., (2014) Advanced system on a chip design based on controllable-polarity FETs, Proceedings of Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 1-6.

[13] Sze, S. M., Li, Y., & Ng, K. K. (2021). Physics of semiconductor devices. John wiley & sons. (ISBN 978-0-470-06832-8).

[14] Roy A. S., Semwal S. and Kranti A. (2022), An Insightful Assessment of 1T-DRAM With Misaligned Polarity Gate in RFET, IEEE Transactions on Electron Devices, 69, 3163-3168.

[15] Butt N. Z., and Alam M. A. (2007), Scaling limits of double-gate and surround-gate Z-RAM cells, IEEE Transactions on Electron Devices, 54, 2255-2262.

[16] Cho M. H. (2012), Thin-Body SOI Capacitorless DRAM Cell Design Optimization and Scaling. University of California, Berkeley, Technical Report No. UCB/EECS-2012-176.

[17] Kim Y., Daly R., Kim J., Fallin C., Lee J. H., Lee D., Wilkerson C., Lai K., and Mutlu O., (2014) Flipping bits in memory without accessing them: An experimental study of DRAM disturbance errors, Proceedings of the International Symposium on Computer Architecture, pp. 361-372.