Enabling sub-Boltzmann On-to-Off Switching Through Metal-Ferroelectric-Metal-Insulator-Semiconductor Architecture

M.Tech. Thesis

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DEPARTMENT OF ELECTRICAL ENGINEERING
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A THESIS

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DEPARTMENT OF ELECTRICAL ENGINEERING
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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **Enabling sub-Boltzmann On-to-Off Switching Through Metal-Ferroelectric-Metal-Insulator-Semiconductor Architecture** in the partial fulfillment of the requirements for the award of the degree of **MASTER OF TECHNOLOGY** and submitted in the **DEPARTMENT OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from July 2021 to June 2022 under the supervision of Dr. Abhinav Kranti, Professor, Department of Electrical Engineering, Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

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Date: June 06, 2022

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Dedicated to my mother

Abstract

ENABLING SUB-BOLTZMANN ON-TO-OFF SWITCHING THROUGH METAL-FERROELECTRIC-METAL-INSULATOR-SEMICONDUCTOR ARCHITECTURE

In order to meet the computational demands, high-density chips are required. A larger number of transistors on a single integrated chip allows greater functionality to be packed in a given module and also lowers the cost for the chip manufacturers. The way to achieve such high-density chips is by downscaling or reducing the dimensions of the transistors. However, reducing the dimension affects the transistor performance i.e, formation of an ultra-sharp *p-n* junction, Short channel effects (SCEs), static power dissipation, and poor on to off current ratio,. In order to meet the high on to off current ratio requirement at lower supply voltages, several transistor architectures such as Impact ionization MOS (IMOS), Tunnel FET (TFET), Feedback FET, and Negative capacitance FET have been proposed in the literature. These structures have different conduction mechanisms and involve p-n junction formation which makes the fabrication process very complex and costly as lower technology nodes. The formation of *p-n* junction can be avoided using the junctionless (JL) topology, which consists of the entire film doped with the same type of dopants. Although it provides better subthreshold characteristics and scalability. However, it has some limitations such as the requirement for high work function to deplete the heavily doped film in the off state. These limitations can be overcome by stacking the ferroelectric (FE) layer over the gate terminal of the JLFET. the with the negative capacitance (NC) phenomenon of FE materials. A FE layer with negative capacitance results in a negative internal gate voltage at zero control gate bias, which results in depletion of heavily doped film at a midgap work function. Also, utilizing the negative capacitance phenomena of the FE layer, a sub-60 mV/dec subthreshold swing can be attained with the suppressed short channel, which makes an NC JLFET a potential candidate for ultralow-power and high-density applications.

This work presents a closed-form analytical model for NC JLFET, operating in the subthreshold region. The model is developed by solving the 2D-Poisson's equation with the 1D L-K model to get the closed-form relation between internal gate voltage and terminal voltages (Gate and drain voltage). The model successfully predicts the unconventional effect of channel doping, gate length, drain bias, and ferroelectric thickness in NC JLFET. Because of the equipotential internal gate layer, the validation of the model is done separately for JLFET and ferroelectric layer (LK model), which matched well with the simulation and experimental results, respectively.

In addition, the model is utilized to investigate the performance of subthreshold inverters for ultralow voltages (< 400 mV). Results show that the by proper optimization of ferroelectric thickness, the figure of merits (nominal and low and high output level, gain, and noise margin) of the inverter can be improved. However, for thicker ferroelectric, hysteresis can be observed in the voltage transfer characteristic because of negative differential resistance. Results obtained from the model were also benchmarked with the conventional JLFET and a significant improvement can be observed for NC JLFET than conventional JLFET.

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NOMENCLATURE

SS	*Subthreshold Swing*	*mV/decade*
L_G	*Gate length*	*nm*
I_{ON}	*On-current*	*mA*
I_{OFF}	*Off-current*	*nA*
I_{ON}/I_{OFF}	*On-current to off-current ratio*	*Unitless*
E_{CB}	*Energy of conduction band*	*eV*
Φ_M	*Work function of metal*	*eV*
Φ_{Si}	*Work function of semiconductor*	*eV*
q	*Electronic charge*	*C*
T	*Temperature*	*K*
V_{TH}	*Threshold voltage*	*V*
V_{FB}	*Flatband voltage*	*V*
T_{OX}	*Gate oxide thickness*	*nm*
T_{FE}	*Ferrelectric layer thickness*	*nm*
V_{DS}	*Drain to source voltage*	*V*
V_{IG}	*Internal gate to source voltage*	*V*
V_{GS}	*External gate to source voltage*	*V*
I_{DS}	*Drain to source current*	*μA*
Ψ_S	*Surface potential*	*V*
Ψ_C	*Centre potential*	*V*
V_{FE}	*Voltage across the ferroelectric layer*	*V*
N_{CH}	*Doping concentration of channel region*	cm^{-3}
ε_{Si}	*Permitivity of semiconductor*	*F/cm*
ε_{OX}	*Permitivity of* SiO_2	*F/cm*

ACRONYMS

MOSFETs	*Metal Oxide Semiconductor Field-Effect Transistors*
FET	*Field-Effect Transistor*
JLFET	*Junctionless Field-Effect Transistor*
MOS	*Metal Oxide Semiconductor*
NC	*Negative Capacitance*
ICs	*Integrated Circuits*
SCEs	*Short Channel Effects*
DIBL	*Drain Induced Barrier Lowering*
CMOS	*Complementary MOS*
FinFET	*Fin Field Effect Transistor*
FBFET	*Feedback Fiekd Effect Transistor*
TFET	*Tunnel Field Effect Transistor*
GAAFET	*Gate All Around Field Effect Transistor*
SiO_2	*Silicon dioxide*
n	*Donor type*
p	*Acceptor type*
n^+	*Heavily doped donor type*
p^+	*Heavily doped acceptor type*
S/D	*Source or Drain*
DG	*Double Gate*
RDF	*Random Dopant Fluctuation*
Si	*Silicon*
BTBT	*Band-to-Band Tunneling*
TCAD	*Technology Computer-Aided Design*
VLSI	*Very Large Scale Integration*
VB	*Valence Band*
CB	*Conduction Band*

Chapter 1

Introduction

1.1Transistor Scaling

Metal Oxide Semiconductor (MOS) Field Effect Transistors (FETs) are the basic building block to drive the semiconductor industry. In order to meet the computational demands, high-density chips are required [1]. A larger number of transistors on a single integrated chip allows greater functionality to be packed in a given module and also lowers the cost for the chip manufacturers [1]. The way to achieve such high-density chips is by downscaling or reducing the dimensions of the transistors. The electronics industry has survived on the foundation of Moore's law [1], which stated that the number of devices in a chip doubles every two years. Evaluation of integrated circuit (IC) based on the number of transistors count per chip over the years is shown in fig. 1.1. International Roadmap for device and system (IRDS) evolved its technology node (TN) from 120 nm (IRDS, 1999) to 100 nm (IRDS, 2001, 2002). The specified gate length of a MOSFETS evolved from 85 nm (IRDS, 1999) to 45 nm (IRDS, 2001) [2].

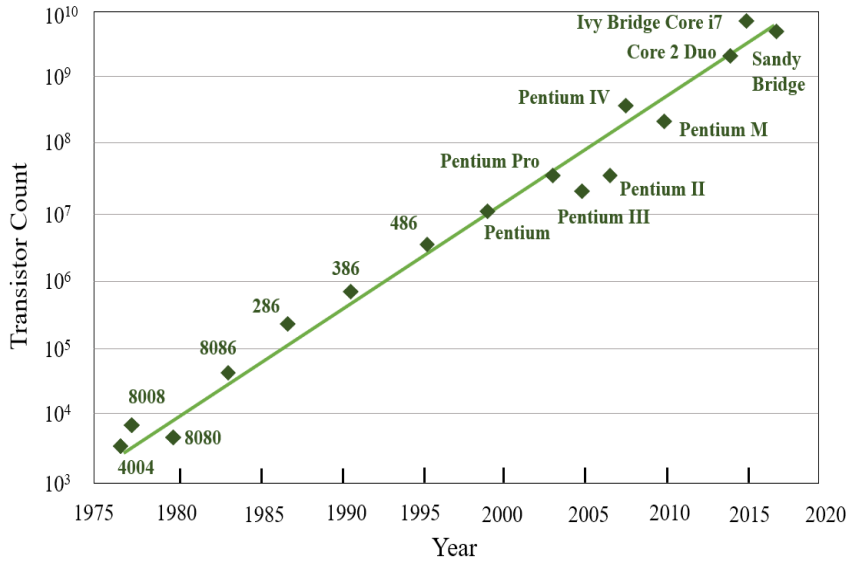


Fig. 1.1: Trend for the transistors count per chip as predicted by Moore's law [1].

Initially, the fabrication of the integrated circuits was implemented with a lesser number of devices, which eventually lead to an increase in the number of transistors, and the need towards efficient hardware to achieve better functionality. Therefore, to fabricate a greater number of functional devices on a limited size chip, downscaling of transistors was the only approach. Downscaling refers to reducing the dimensions and modifying the device parameters by a factor [3], as follows.

1) **Constant field scaling** [2]**:** In Constant field scaling, the electric field inside the transistor is maintained the same while scaling down the voltages and the dimensions by a scaling factor 'S'

2) **Constant voltage scaling** [2]: In Constant voltage scaling, the terminal voltages and operating power supply voltage are maintained the same while the device dimensions are scaled by a scaling factor 'S'.

1.2 Challenges in Transistor Scaling

Transistor downscaling has several challenges associated such as degradation in off-current, poor of gate controllability over the channel, higher static power consumption, higher parasitic capacitance, and device reliability [6]. A poor controllability of gate over the channel arises due to effect of a high lateral electric field from drain side on the channel. This results in a higher short channel effects (SCEs) like Threshold Voltage degradation wih length (dV_{TH}), Subthreshold Swing (SS) degradation, band-to-band tunneling at drain side, and drain induced source to channel barrier lowering i.e. Drain Induced Barrier Lowering (DIBL) [2].

1.2.1 Short channel effects

Short channel effects (SCEs) are the undesired effects that arise in MOSFETs with lower gate lengths [2]. In a long channel device, the drain and source terminals are far apart from each other, and hence, the lateral electric field induced by the drain side does not affect the minimum channel potential or does not affect the source to channel barrier [2]. However, at lower gate lengths, the electric field between drain and source influences the electrostatics under the gate which affects weakens the effect of the gate

electric field on the channel. This lowers the gate controllability and leads to several SCEs [2] as discussed below.

(a) **Drain Induced Barrier Lowering (DIBL)** [2]**:** This effect occurs at a shorter gate length where a high drain voltage reduces the energy barrier formed between source to channel, which results in the overall reduction in gate controllability. As a result, even at low gate voltage, the transistor starts conducting, and a higher off-current is observed.

(b) **Threshold Voltage roll-off** [2]**:** In the nanoscale regime, the depletion width at the drain and source side becomes comparable to the gate-controlled depletion width. Therefore, when the channel length is scaled down while maintaining the same doping, the threshold voltage decreases as shown in fig 1.2(b).

(c) **Subthreshold swing** [2]**:** As an effect of DIBL, due to proximity of drain, the channel is not controlled by the gate. So, the change in gate voltage does not affect the current flow as strongly as that in long-channel. Therefore, the subthreshold swing of the device increases. Fig 1.2(b) shows increased subthreshold swing for lower gate length.

(d) **Hot carrier injection** [2]**:** In a short channel device, due to the high electric field near the drain side, some of the electrons near the drain side acquire more energy compared to thermal energy. These carriers possess high energies and can tunnel through the thin gate dielectric which leads to gate leakage currents or may get trapped at the Si-SiO_2 interface which can cause threshold voltage shift.

(e) **Gate Induced Drain Lowering (GIDL)** [2]: For a zero or negative gate voltage, if the drain voltage is kept very high, the energy bands at the overlapped region at the drain end bend significantly due to higher reverse bias. It can cause

avalanche multiplication due to the high electric field and band-to-band tunnelling because of very thin depletion width. The minority carriers present underneath the gate can also be moved away to the substrate leading to an increase of the leakage current. This effect is described in fig 1.2(c)-(d) which shows the band-to-band tunnelling and an increase in the current for more negative gate voltage.

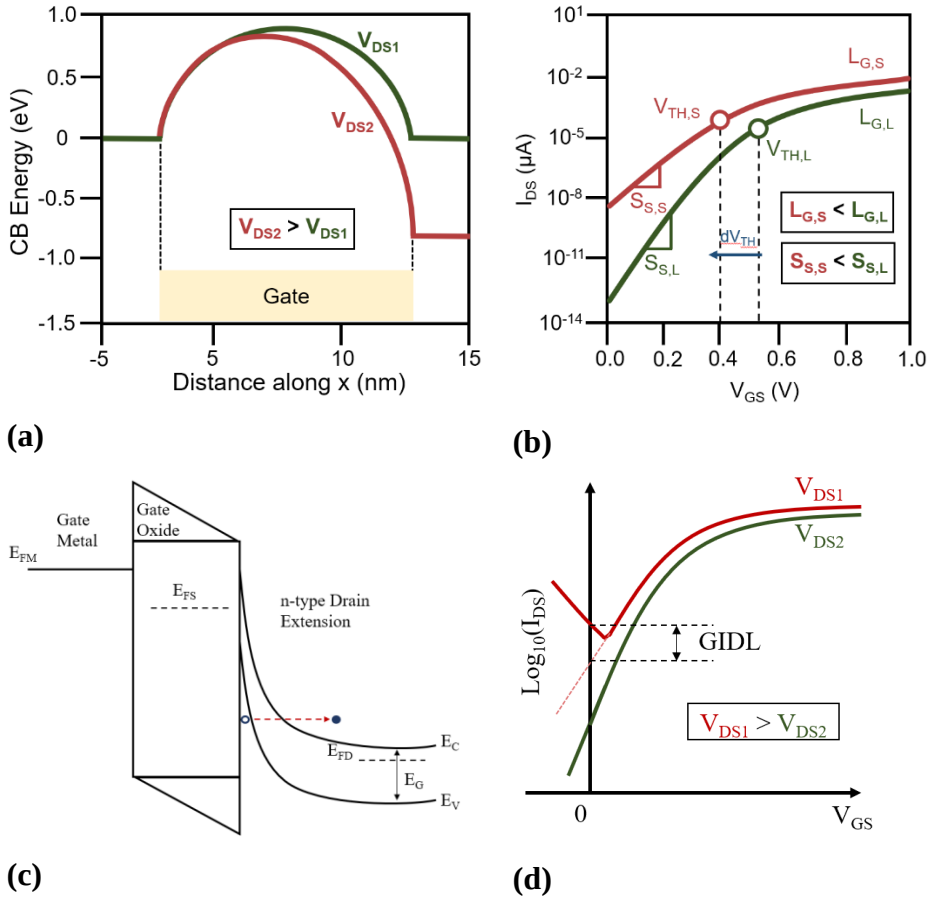


Fig. 1.2: (a) Variation of conduction band energy along the channel length for different drain biases ($V_{DS2} > V_{DS1}$) showing drain induced barrier lowering (DIBL). (b) Variation of drain current (I_{DS}) at different gate lengths ($L_{G,S} < L_{G,L}$) showing degradation of subthreshold swing and threshold voltage roll-off ($V_{TH,S} < V_{TH,L}$). Variation of (c) conduction and valance band showing electron tunnelling through the barrier, and (d) and the corresponding effect on drain current due to gate induced drain leakage (GIDL) [2].

1.2.2 Process

Patterning smaller features in nanoscale devices is carried out using optical lithography, which requires a very high precision that increases in the cost of fabrication. Also, at the nanoscale regime, the source and drain junctions need abrupt doping concentration, which again increases the complexity of the process [4],[5].

1.2.3 Power

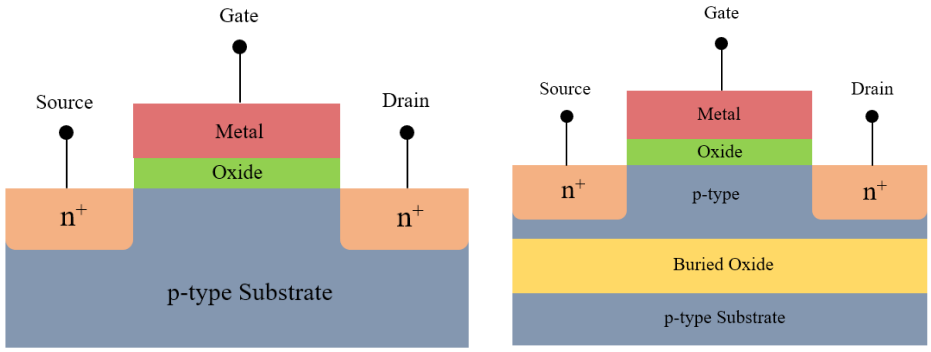
In Complementary Metal Oxide Semiconductor (CMOS) logic, total power is consumption depends on the static power and dynamic power [6]. Switching power or dynamic power varies proportionally with the operating frequency, load capacitance and operating supply voltage. The static power or the leakage power, on the other hand, depends on the static leakage current and supply voltage in the off-state of the transistor [6].

1.3 Evolution of transistor architecture to overcome SCEs

To enable further scaling of transistors and to improve the device performance several architectures can be used, which enhanced the gate controllability.

1. **Bulk MOSFET** [7]**:** The schematic diagram of the bulk MOSFET is shown in fig 1.3(a). Bulk MOSFETs with long channel technology were proven to be much more effective to meet the speed and power requirements. However, downscaling the device leads to various SCEs such as an increase in off current (I_{OFF}), subthreshold swing (SS) degradation, DIBL, threshold voltage (V_{TH}) degradation [7]. Therefore, to meet the low power requirement with a scaled device becomes extremely difficult while maintaining the desired speed of operation.
2. **Silicon-on-Insulator (SOI)** [8]**:** The improvement over bulk technology was achieved by reducing leakage paths by using Silicon-on-Insulator (SOI) [8] technology. Here, an oxide layer is

grown on a bulk substrate and then the body (silicon) layer is deposited on which the channel is formed (fig 1.3(b)). Such a structure can be divided into two categories: (1) if the silicon film thickness (T_{CH}) is larger than the maximum depletion width in the channel region, then the silicon body will only be partially depleted i.e. Partially Depleted SOI (PD SOI), and (2) if T_{CH} is less than the depletion width, the channel can be fully depleted at zero gate voltage i.e. Fully Depleted SOI (FD SOI).



(a) **(b)**

Fig. 1.3: Schematic diagram showing (a) Bulk MOSFET, and (b) SOI MOSFET.

1.3.1 Advantages of SOI technology over bulk technology [9],[10],[11]:

i) In SOI transistors, the drive current is higher than bulk MOSFET [9] due to higher mobility.

ii) The parasitic n^+p junction capacitances can be reduced in the SOI devices, which results in high-speed operation [10] in SOI devices.

iii) SCEs can be significantly reduced in a MOSFET fabricated on an SOI technology and can further be suppressed as the film thickness becomes thinner [11].

1.3.2 Multiple Gate Architectures

SOI MOSFETs can be operated at low power due to the lower off-current as compared to traditional bulk MOSFETs. It exhibits a lower subthreshold swing than that of bulk CMOS technology with a higher threshold voltage [11]. Hence, the static power consumption is greatly reduced. While learning a few

ways to reduce the off-current and control the SCEs, SOI topology has witnessed the change in device architecture from planar with a single gate to 3-D devices with multi-gate structures to improve gate control (electrostatics).

a) **Double-Gate MOSFET (DG MOSFET) [12]:** A FDSOI device integrated between two electrically shorted (connected) gates can significantly reduce SCEs [12] (Fig. 1.4 (a)). As gates are present at top and at the bottom of the film, this structure provides superior control over the channel region than SOI MOSFET. Also, in DG architecture the effect of the drain electric field on channel potential can be reduced significantly, which results in reduced SCEs.
b) **FinFET [13]:** A FinFET was introduced as a lean-channel transistor [13] which is entirely depleted. A tall and narrow fin-shaped silicon film is used as a channel (fig 1.4(b)). Because of the vertical tri-gate structure, FinFET provides better SCEs performance and high packing density [14]. Therefore, FinFET is widely used in the semiconductor industry.
c) **Gate-All-Around Nanowire structure (GAA-NW) [15],[16]:** The gate controllability of the transistor can be further improved using the Gate-All-Around nanowire (fig 1.4(c)) configuration, in which the channel region of the device is surrounded by the gate electrode to provide enhanced gate controllability [15],[16]. It provides excellent gate electrostatics (controllability) over other structures, and thus SCEs are suppressed.
d) **Nanosheet [17],[18],[19]:** It is a structure similar to a FinFET but in this case the gate completely surrounds the nanowire which is wider and thicker as shown in fig 1.4(d) [17]. It was first proposed by Samsung [17]. Nanosheet FETs can include vertical stacking which can improve the drive current [18]. It overcomes the issues of vertical stacking with higher effective width and lower parasitic capacitances [19].

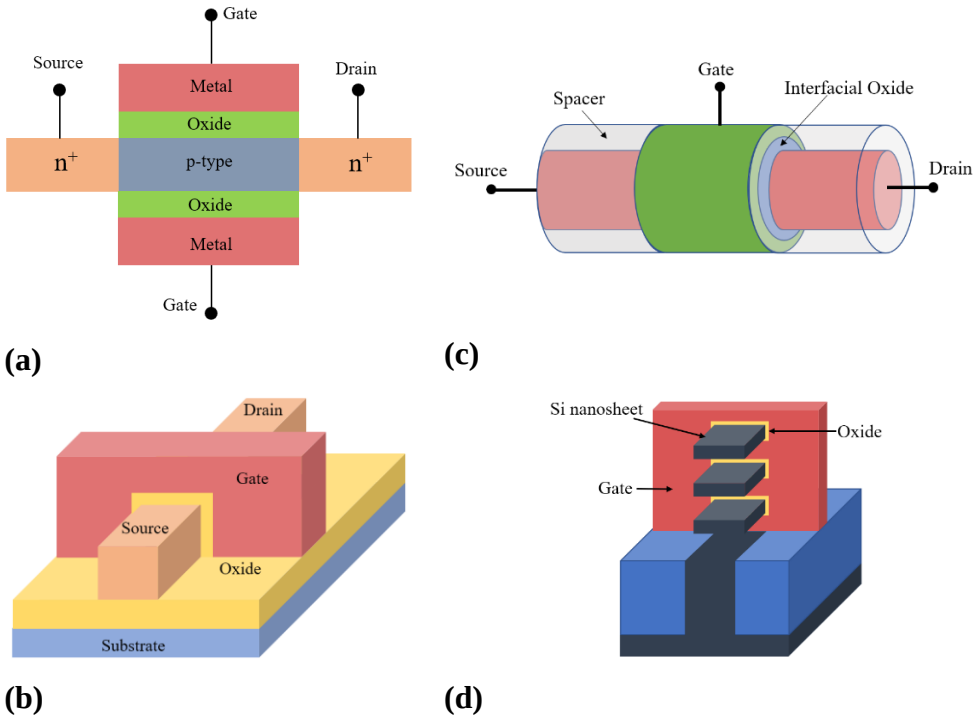


Fig. 1.4: Schematic representation of (a) Double Gate (DG) MOSFET, (b) FinFET, (c) GAA MOSFET, and (d) Nanosheet FET

1.4 Evolution of transistor architecture to overcome nanoscale process challenges

One of the most suitable approaches is to simplify the process technology is to avoid ultra-steep p-n junctions in the nanoscale regime. A junctionless (JL) topology [20] can be useful for the same. JL transistor consists of a heavily doped silicon film either p-type or n-type and a gate to modulate the channel concentration. Since there are no junctions, the conduction mechanism is different in these devices. Compared to conventional inversion mode MOS, a junctionless device suppresses the SCEs compared to inversion mode MOSFET, and more importantly, a simpler fabrication methodology as it completely avoids the formation of junctions. Due to this, it enables further scalability of the device into the nanometre regime [20]. However, a junctionless device faces several challenges such as the possibility of high source/drain resistance, random dopant fluctuations for higher doping,

and high metal work function required to deplete the entire film at zero gate bias [21].

1.5 Evolution of transistor architecture for ultra-low power application

Ultra-low Power (ULP) devices have attracted a lot of attention due to the ever-increasing demands of energy efficient circuits in modern and portable electronics. Fermi-Dirac carrier distribution and the drift-diffusion transport mechanism have limited the scalability of sub-threshold swing to 60 mV/decade i.e. Boltzmann limit [22]. Thus, the on-to-off current ratio is also limited by the subthreshold swing at lower supply voltage (V_{DD}). This causes challenges to implement UPL circuits with scaled devices. Whereas a sharp transition is necessary from off state to on state for switching devices, the gradual transition of the same makes it very difficult to achieve a high on-current to off-current at shorter dimension devices.

There have been multiple studies to improve the subthreshold swing and reduce the static power dissipation by making modifications to the conduction mechanism which leads to devices such as Impact-ionization MOS (I-MOS) [24], Tunnel-FET (TFET) [26], feedback FET [27]. Also, by modifying gate controllability of baseline transistor through the insertion of ferroelectric material, a sub-60 swing can be achieved [32],[33] i.e. through the use of Negative Capacitance FET (NC-FET).

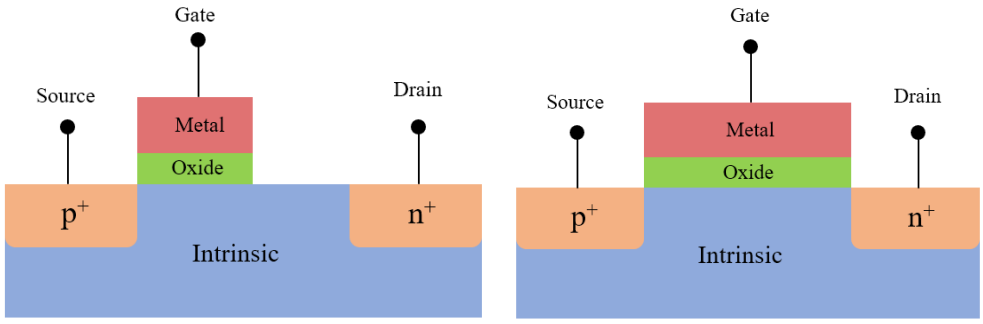
1.5.1 Impact-ionization MOS (I-MOS)

The structure of the device is similar to p-i-n configuration [24] as shown in fig. 1.5(a), where the intrinsic region is partially gated so as the ungated region is towards the p region for n-type IMOS and towards n-region for p-type IMOS. It works on the principle of avalanche breakdown. If the gate voltage is low, then the inversion charge is less and the entire intrinsic region

acts as effective channel length. The electric field is not enough to achieve breakdown and the device remains off. In IMOS, the off-current is reduced because of the inherent nature of p-i-n configuration. As the gate voltage increases, an inversion layer starts forming, and as a result, the effective channel length reduces and electric fields increases. When the electric field has increased beyond a certain voltage, the impact ionization is triggered [24]. IMOS has some reliability issues such as the generation of hot carriers which degrades the device performance [25], and it also requires a high negative voltage at the source which increases the source to body leakage [25].

1.5.2 Tunnel FET (TFET)

The schematic structure of TFET is shown in fig 1.5(b), where the doping of the drain and source region are opposite in nature which forms p-i-n like structure along source to drain. The conduction mechanism in TFET depends on Band-to-Band tunnelling (BTBT) which leads to a sub-60 mV/dec subthreshold swing at 300 K [26]. However, the fabrication of TFETs has several challenges such as fabrication of steep tunnel junctions, low interface-trap-density, and contacts with lower resistance [26].



(a) **(b)**

Fig. 1.5: Structure of (a) impact-ionization MOSFET (I-MOS) and (b) Tunnel field-effect transistor (TFET) [26].

1.5.3 Feedback FET (FBFET)

The feedback FET is also a p-i-n structure with undoped channel partially covered by the front gate (fig 1.6) [27]. The difference comes from the biasing in forward mode and operating mechanism which is band modulation by injected carriers. As compared to conventional MOSFETs they can have

steep sub-threshold swing and high I_{ON}/I_{OFF} ratio [27]. Although it addressed the power consumption issue, the fabrication is not cost-effective because of the formation of steep p-n junctions [28].

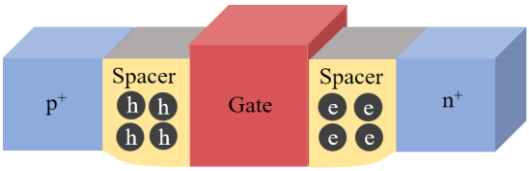


Fig 1.6: Structure of feedback field-effect transistor (FBFET).

1.5.4 Negative Capacitance FET (NC-FET)

A ferroelectric material can have any of the two distinct polarization states even in absence of an electric field, which can be switched from one to another by an external electric field. During the polarization switching, a negative capacitance phenomenon is observed in the ferroelectric devices [31]. Replacing the dielectric gate oxide of a conventional MOSFET with the ferroelectric material can possibly enhance the rate of change of channel potential with the gate voltage because of negative capacitance. This can enable ultra-low-power operation by reducing the supply voltage requirement via a sub-60 mV/decade subthreshold swing [32].

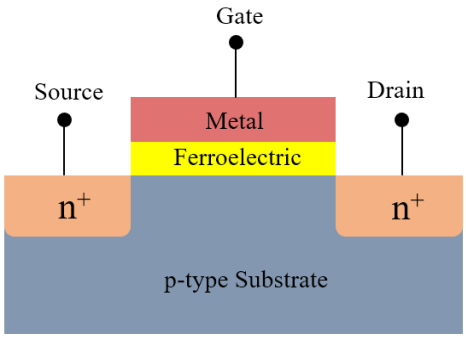


Fig 1.7: Structure of bulk negative capacitance FET (NC-FET)

1.6 Organization of Thesis

The thesis presents an elaborated approach to model the subthreshold characteristics of a negative capacitance (NC) junctionless field effect (JLFET) transistor, and analyse the impact of the ferroelectric layer on the terminal gate charge in relation to the external gate voltage and short channel effects. The developed model is also utilized in ultra-low power (ULP) CMOS subthreshold inverter to analyse its figure-of-merit (FoM) and benchmarking.

Chapter 1 discusses the recent advancements in MOS technology, downscaling and techniques to reduce SCEs, different MOS architectures, multiple gate topologies and architectures facilitating steep switching action.

Chapter 2 explains the different material properties and significance of ferroelectric materials for semiconductor technology, its modelling using the Landau equation and related negative capacitance phenomena. Further, the chapter discusses the junctionless topology, its advantages over conventional MOS devices, and its fundamental limitations. In later part of the chapter, the use of ferroelectric material as a replacement for an insulator is described.

Chapter 3 consists of a detailed discussion of the model developed for a negative capacitance junctionless field effect transistor, and its applicability with the respective numerical (simulation) data is shown.

Chapter 4 extends the model to subthreshold logic applications in which a CMOS inverter is analysed with the application of the developed model and observation of its performance parameters.

Chapter 5 presents a summary of the research work and also mentions the possibility of future work.

1.7 Conclusion

For technology scaling and reliable operation in ultra-low power regimes, various device architectures and conduction mechanisms have been studied to keep up with scaling projections of Moore's law. To meet demands on modern computation and performance there is a need to develop or modify conventional MOS structures which could enable further scaling of the device as well as improve the performance. Along with the advancement in structure, the fabrication process which needs to be cost-effective. As per the current trend for ULP operation, reducing the static power dissipation is a new challenge which can be reduced by introducing different materials into MOS structure enabling further optimization in circuit applications.

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Chapter 2

Negative Capacitance Junctionless Transistor

2.1 Material Overview

2.1.1 Piezoelectricity and Pyroelectricity

Piezoelectric material releases electric charges under the application of mechanical stress [1]. This phenomenon is observed in non-centrosymmetric materials. When the charge is released due to a change in temperature of the material, the phenomenon is known as pyroelectricity [1], and the same occurs in materials with crystal symmetric. All pyroelectric crystals are piezoelectric [1].

2.1.2 Ferroelectricity

A Ferroelectric material possesses a permanent dipole moment or spontaneous polarization in absence of an electric field. Ferroelectric material was first discovered in Rochelle salts [4][5]. Later, ferroelectricity was also found in Barium Titanate in 1944 [6]. Ferroelectric materials can be a subset of the set of pyroelectrics due to their polar nature. They are known to exhibit spontaneous polarisation which can be reversed along with the direction of the polar axis through an external electric field [1][2][3].

The spontaneous polarization is exhibited below a specific temperature called Curie temperature [4]. The positioning of the centre ion of material governs the orientation of spontaneous polarisation. By applying the electric field, the direction of the spontaneous polarization can be switched. A non-linear relationship is exhibited by the ferroelectric materials between polarization, P, and electric field, E, as given by a hysteresis loop (fig. 2.1) [9].

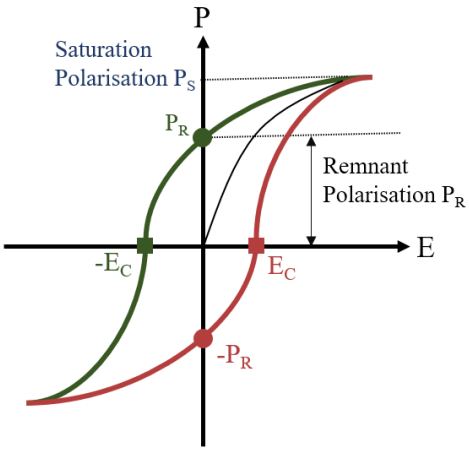


Fig 2.1: Schematic representation of hysteresis in ferroelectric materials [9].

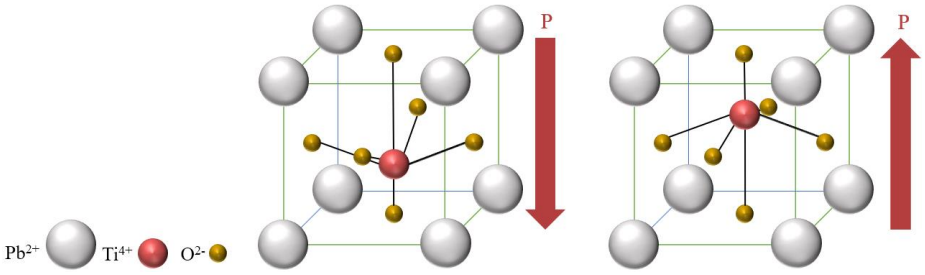


Fig 2.2: Representation of two different polarization states of ferroelectric $PbTiO_3$ due to asymmetric positioning of the central Ti ion [7].

A ferroelectric crystal lattice shows spontaneous polarisation because of crystal asymmetry (Fig. 2.2). These crystal lattices form multiple domains, which are orientated in different directions. Thus, the net polarization remains zero in absence of an electric field. Applying an external electric field, the direction of the domain can be changed [8], which results in a nonlinear increment in polarization with the electric field. Further increment in the electric field maximum polarization can be attained, which is known as saturation polarization (P_S) where all the domains are oriented in the direction of the electric field [9]. Similarly, by reversing the direction of the electric field, the direction of domains can be switched. The expansion of existing antiparallel domains causes the growth of new antiparallel domains, which leads to hysteresis [2][7][8]. The polarization which exists in the device when the electric field is set to zero is known as remanent polarization (P_R) [9]. However, the external electric field needed to depolarise ($P = 0$) the ferroelectric material is known as coercive field (E_C).

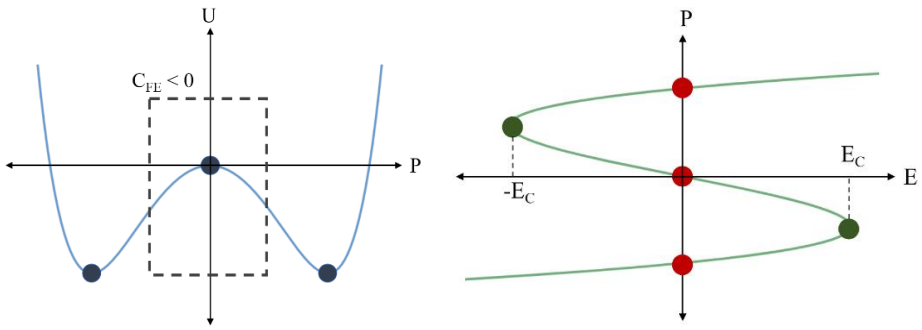
2.2 Landau Theory of Ferroelectric

The Landau theory was founded on symmetry phenomenology, which acts as a theoretical link between macroscopic and microscopic models [10]. Landau emphasised that a ferroelectric system cannot smoothly switch between two stable phases with distinct symmetries. Thus, an unstable phase must exist between the two stable states [10].

Landau defined the free energy (U) in terms of power series of polarization (P) [11]. The two stable spontaneous polarisation states i.e. stable energy states must correspond to the minimum free energy state (Fig. 2.3a) [11]. The free energy ($U(P)$) of a ferroelectric can be expressed in terms of polarization and applied electric field [11], as shown below

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \tag{2.1}$$

where $E\left(=\frac{V}{d}\right)$, is the external electric field, V is the applied voltage across the ferroelectric and d is the ferroelectric thickness. α, β, γ, are Landau's parameters, where α is negative and temperature-dependent, β and γ are remains independent of temperature. Also, γ always remains positive while β may have positive or negative depends on the phase transition. Below the Curie temperature, α is less than zero, which results in a double well energy landscape characterised by the negative curvature around $P = 0$ (Fig. 2.3a).



(a) **(b)**

Fig 2.3: (a) A double well energy landscape, and (b) E-P Curve obtained from the L-K Model [10] as shown in Eq. (2.1).

2.3 Negative Capacitance in Ferroelectric

The capacitance (C) can be obtained in terms of free energy (U) as

$$C = \left(\frac{d^2U}{dQ^2}\right)^{-1}$$

The region that separates the two stable polarization states (two energy minima), is the region of interest for this work where ferroelectric material shows negative capacitance [12],[13]. The negative capacitance region of the ferroelectric lies in an unstable region which occurs during the transition from one stable state to another. The unstable NC region can be stabilized by stacking the ferroelectric over the dielectric capacitor such that the total energy of ferroelectric-dielectric stack becomes minimum in the NC region of the FE [15]. This configuration is known to provide internal voltage amplification [12],[13],[14] which results in steep current rise, and hence, the subthreshold swing can be lowered than the theoretical limit of 60 mV/decade at room temperature. Also, the ferroelectric material shows hysteresis which is not suitable for logic applications, which can be avoided by choosing the appropriate ferroelectric and dielectric thickness as part of the gate stack [15].

2.4 Junctionless MOSFET (JL MOSFET)

Scalability to nanoscale dimensions while maintaining the performance of the device is the need of the current semiconductor industry. For a scaled device, a simpler and cost-effective fabrication process is essential. Conventional inversion mode SOI MOSFET consists a p-n junctions at drain and source side, which becomes increasingly difficult to obtain steep junctions in the nanoscale regime [17]. The fabrication processes for doping (ion-implantation) with high temperature annealing become increasingly difficult to control to form such junctions. Also, the inversion mode device must be heavily doped to achieve an optimum current drive. Thus, it imposes two constraints in inversion mode device, (1) formation of ultra-sharp p-n junction in nanoscale dimensions, and (2) high doping [17].

Julius Edgar Lilienfield, an Austrian-Hungarian physicist conceptualized and patented conductivity modulation with the help of an electric field in MOS configuration in 1933 [18]. The device consisted of two metal electrodes and the current could be modulated by the applied electric field. It didn't have any metallurgical junctions which makes it quite relevant for current technology trends. Based on the above mention mechanism, a junctionless transistor was first fabricated in nanowire architecture by Colinge *et al.* [18].

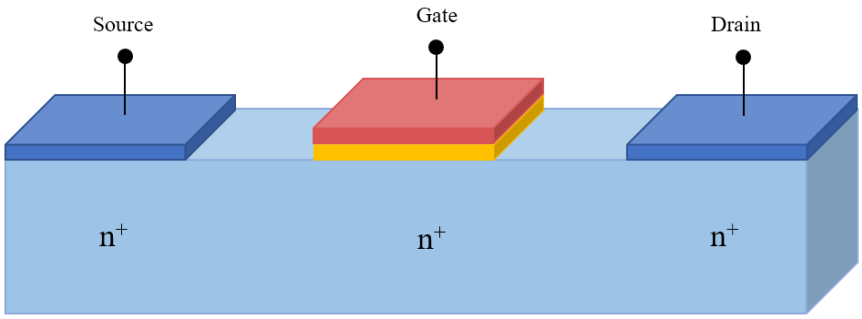


Fig 2.4: Structure of JL MOSFET [19].

The structure of a JL MOSFET is shown in fig. 2.4. It consists of a highly doped (single dopant type) semiconductor film without any separately doped regions for the source and drain. Heavy doping is required to form an ohmic contact at drain and source. As it does not have any p-n junctions, the conduction mechanism is different from that of a conventional inversion mode device [17]. Depending on the doping configurations there can be three types viz. junctionless (JL) mode FET ($n^+n^+n^+$) FET, inversion mode (IM) FET (n^+pn^+), and accumulation mode (AM) FET (n^+nn^+) [17]. The current-voltage characteristics of these configurations shown in fig. 2.5 indicate that the difference in the three configurations is the location of the flatband voltage (V_{FB}) [18]. In the case of junctionless, the current characteristics are similar to that of IM device except the flatband voltage is higher than the threshold voltage.

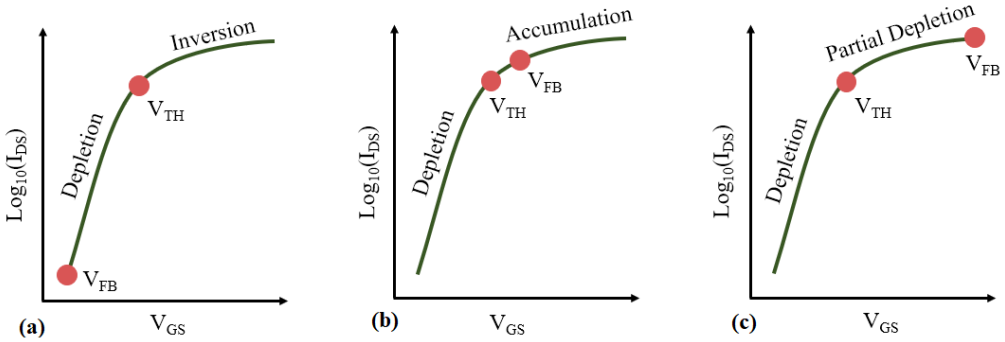


Fig 2.5: Comparison of transfer characteristics [18] of (a) inversion mode (IM) FET, (b) accumulation mode (AM) FET, and (c) junctionless (JL) FET.

2.4.1 Operation

A junctionless device is operated in a similar manner as an inversion mode MOSFET. At zero gate bias (V_{GS}), the entire silicon channel is depleted of charge carriers, hence no conduction path forms, and the device is in the off-state (fig. 2.6a) [18]. As V_{GS} increases, the depletion starts to reduce from the centre of the film and the current increases in the subthreshold region (fig. 2.6b). When V_{GS} is equal to threshold voltage V_{TH}, a neutral channel starts forming in the centre from source to drain [18]. In the case of junctionless device, the conduction starts from bulk and not from the surface. Hence, the device turns on but the channel remains partially depleted, and the current conduction takes place through the bulk [18]. Above threshold, the device shows identical behaviour like saturation region and pinch-off as that of conventional inversion mode MOSFETs. The working of junctionless MOSFET can be summarized in the figure 2.6.

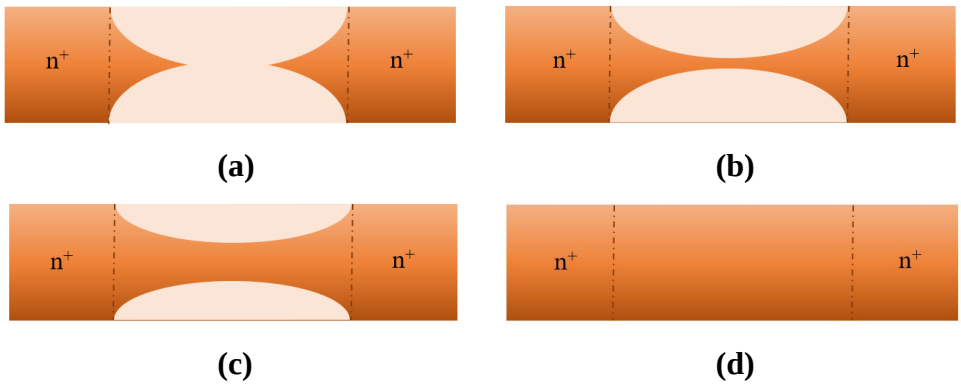


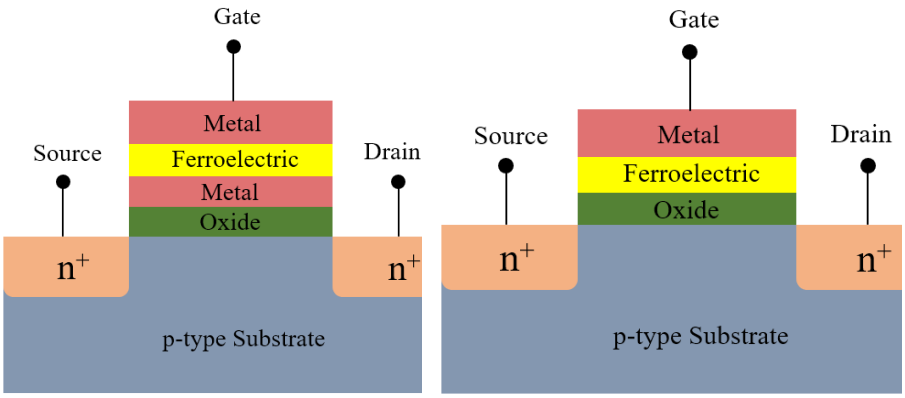
Fig 2.6: Operation of JL MOSFET for (a) $V_{GS} < V_{TH}$, (b) $V_{GS} = V_{TH}$, (c) $V_{GS} > V_{TH}$, and (d) $V_{GS} = V_{FB}$.

2.4.2 Limitations of Junctionless transistor

i. The entire film is heavily doped to achieve better on-current, this requires a high gate work function for the depletion of silicon film in the off-state [17]. Such higher values of work function can cause problems in fabricating the device due to poor adhesion with the gate oxide [17].

ii. As the doping requirement of the film is high for higher on-current, the device requires an ultrathin semiconductor film for volume depletion at zero gate bias. Also, a heavy doping causes mobility degradation and increased impurity scattering [17].

iii. The doping is done via ion implantation which doesn't ensure uniform placement of impurity atoms. Hence, in the case of heavy doping, the random placement of impurity atoms (random dopant fluctuations) can cause variations in surface potential which affects the carrier flow [20].



(a) **(b)**

Fig 2.7: Structure of (a) MFMIS [21] and (b) MFIS topology of NC FET [21]

2.5 Negative Capacitance (NC) FET

An NC-FET is realized by stacking a ferroelectric layer over the conventional MOSFET [21]. There are two possible NCFET configurations were exist in the literature as shown in Fig 2.7 i.e. metal ferroelectric insulator semiconductor (MFIS) and metal ferroelectric metal insulator semiconductor (MFMIS) [21].

The fabrication of a silicon junctionless transistor with ferroelectric gate oxide [22],[23] had shown various improvements such as suppressed off-

current, reduced sub-threshold swing and increased on-current [23]. The performance of JL transistors degrades significantly at lower gate lengths. By making use of the ferroelectric layer, the device can be turned-off with a significantly lower-off current [23],[24]. Also, the channel can be depleted at the midgap gate work function. Also, a JL MOSFET with a ferroelectric layer provides a better on-to-off current ratio (I_{ON}/I_{OFF}) ratio with lower off-current as compared to its inversion mode counterpart [23],[24].

The gate voltage needed for the one-decade current change is known as subthreshold swing [25] of the device, which strongly depends on the gate to channel coupling and current transport mechanism, and can be expressed as

$$S_{swing} = \left(\frac{\partial V_{GS}}{\partial \psi_S}\right)\left(\frac{\partial \psi_S}{\partial(\log_{10} I_{DS})}\right) = m\left(\frac{\partial \psi_S}{\partial(\log_{10} I_{DS})}\right) \qquad (2.1)$$

where $\frac{\partial \psi_S}{\partial(\log_{10} I_{DS})}$ the term depends on the current transport mechanism of the device while the term m is the body factor, which depends on the gate to channel coupling of the device [25]. The current transport factor has a Boltzmann limit (60 mV/decade) at 300 K for barrier modulated transport while the term, m is always greater than unity in case of conventional MOSFET [25]. In case of ferroelectric layer at gate stack, the transport mechanism is remains unaffected but the insulator capacitance, C_{INS}, gets modified as the series combination ferroelectric and dielectric capacitor. If the ferroelectric capacitor operates in the negative capacitance region, then m may become less than unity which makes the sub-threshold swing less than 60 mV/decade [25].

The negative capacitance can be used to amplify the internal gate voltage [25],[26]. Therefore, a minor change in gate voltage may results in a larger change in internal gate voltage, which can result in steeper current transition and a higher on-current. Thus, it can also reduce supply voltage requirement for ultralow power application.

In off-state, the channel is depleted of majority charge carriers. In case of n-channel the depleted channel has positive charge [25],[26]. This induces a negative charge on internal gate electrode. Based on the charge voltage relationship of ferroelectric layer, a voltage drop across the ferroelectric is

attained. Therefore, the resultant internal gate voltage which is the difference between the external gate voltage and the voltage across the ferroelectric layer becomes negative. Hence, the negative internal gate voltage further depletes the channel, and off-current is reduced [23],[25],[26].

Use of ferroelectric layer also makes the device more resilient to variations caused by RDF which is a major concern for nanoscale JL MOSFET [30].

2.6 Conclusion

The chapter provides an insight into the working of negative capacitance transistors, especially with regards to voltage gain in a transistor through the use of a ferroelectric layer. The ferroelectric layer in the gate stack of a JL MOSFET can achieve sub-60 mV/dec SS at 300 K along with supressed SCEs. The negative capacitance phenomenon also counters the limitations of JL MOSFET such that it reduces the metal work function requirements [17], better SCEs immunity (negative DIBL) [23],[24] and variations due to random dopant fluctuations [30]. Also, the supply voltage scalability is possible due to internal voltage amplification.

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Chapter 3

Modelling of Negative Capacitance Double Gate Junctionless Transistor

3.1 Device Modelling

A device model captures electrical and physical behaviour of semiconductor devices [1]-[5]. A device model can be used to understand how a device operates, primarily internal mechanisms or terminal behaviour [2]. These mathematical models broadly can be classified into different types as discussed below.

1) Physical device models [3]-[4]: These kind of models helps to understand the physics inside the device in terms of non-measurable quantities and electrical behaviour associated with the device. These models allow to user to choose the appropriate device geometry, materials, doping distribution, dimensions, and carrier transport mechanism. These models are often employed in commercial numerical device simulators because they offer a complete understanding of physics inside the device along with device operation.
2) Compact model [3]-[4]: Physical device models discussed earlier are accurate but require a large computation, which makes them unsuitable for faster and large circuit simulations [3][4]. Compact models are made up of interconnected segments that recreate the electrical terminal behaviour. Thus, these models are widely utilised in circuit simulators due to their compact and quick computational nature. Berkeley Short-channel Insulated Gate FET Model (BSIM) [6] is a series of a compact models developed by the University of California, Berkeley, for integrated circuit simulation, which is extensively used by the semiconductor industry.
3) Analytical models [3]-[4]: They are based on device physics and commonly used in circuit simulators, consisting of closed-form solutions for physical parameters such as charge density and surface

potential. Due to the complexity of MOSFET behaviour, in some cases, it becomes difficult to achieve a continuous and compact closed-form analytical model which would be applicable to all operating regions.

3.1.1 Modelling Framework

The multi-gate JL architecture has opened up new avenues for extending the downscaling limits of traditional MOSFETs. The absence of abrupt p-n junctions, easy fabrication techniques, lower thermal budget, effective gate controllability over the channel with multiple gates, and enhanced SCEs immunity are all significant aspects of these transistors [8]-[12]. As the source, drain and channel have the same kind of doping, which results in the depletion region can extend outside the gated part in subthreshold operation [13]. This increases the effective channel length, which could suppress the SCEs in JL transistors [14][15].

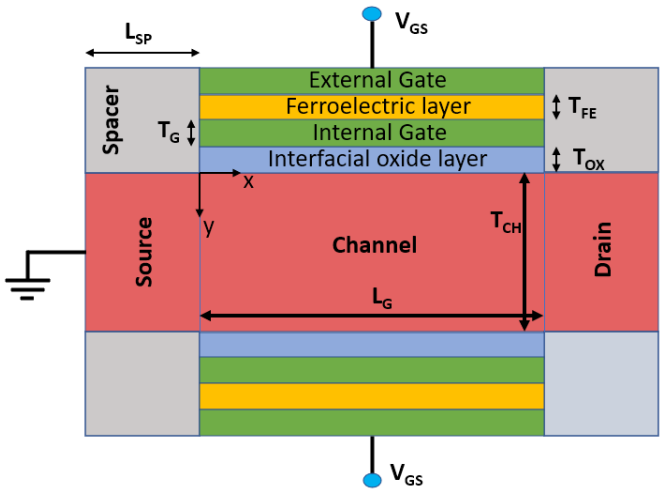

Fig 3.1: Schematic of double gate (DG) negative capacitance (NC) junctionless (JL) FET.

To further enhance the subthreshold characteristics there have been studies on the use of ferroelectric materials and their negative capacitance phenomena to achieve performance improvements. Generally, the ferroelectric layer is included in the gate stack along with the interfacial oxide [16]. The presence of an interfacial oxide provides better control over the thickness of the ferroelectric layer. Such a configuration leads to a voltage drop across the ferroelectric layer which influences the gate charge

by modulating the internal gate voltage. Several models of junctionless transistors have been proposed for subthreshold behaviour and threshold voltage. This chapter investigates the closed form model for potential and current which captures the behaviour of the internal gate voltage with external gate and drain voltage.

The analytical framework to model development for NC JL FET is represented in fig 3.2. First, the 2D Poisson's equation in subthreshold region can be solved to estimate surface potential in terms of internal gate voltage (V_{IG}). Then, integrating the space charge density along the channel length, the internal gate charge density due to inner coupling can be evaluated. The intrinsic gate charge and charge due to fringing fields together represent the total charge density on internal gate. Next, the total internal charge density (or polarization charge density) and Landau's model [17] can be used to evaluate the voltage across the ferroelectric film. Finally, by combining the baseline JL FET model with Landau's model a closed-form relationship can be obtained between internal gate voltage and external gate voltage.

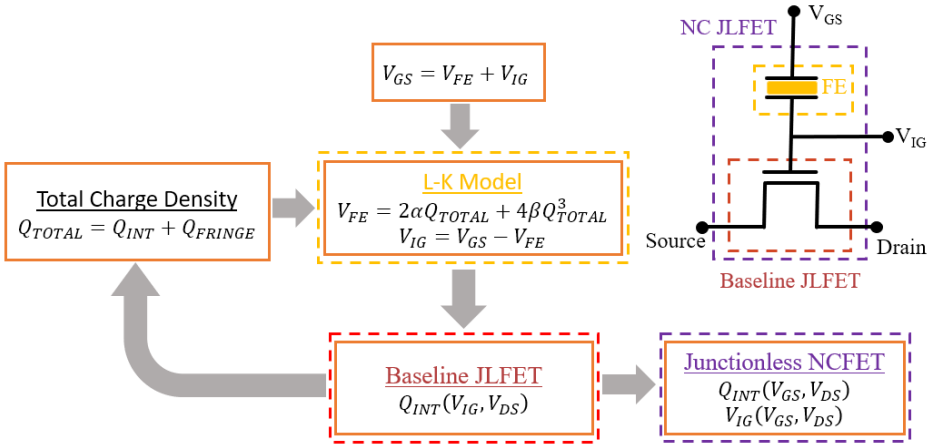

Fig 3.2: Analytical framework adopted in this work to model the NC JL FET.

3.1.2 Potential Distribution in the channel

Figure 3.1 shows the schematic of DG NC junctionless FET analysed in this work. In the depletion region, the mobile charge term can be neglected in the Poisson's equation. Thus, the potential distribution ($\psi(x, y)$) through 2D Poisson's equation can be written as

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{qN_{CH}}{\epsilon_{Si}} \tag{3.1}$$

where x is the distance from the source side, y is the distance along channel width, q is the elementary charge, N_{CH} is the channel doping, and ε_{Si} is the silicon permittivity. A parabolic approximation of potential along the channel thickness can be used [18] to yield results with reasonable accuracy as

$$\psi(x,y)=c_1(x)+c_2(x)y+c_3(x)y^2 \tag{3.2}$$

where the coefficients $c_3(x)$, $c_2(x)$ and $c_1(x)$, can be calculated using following boundary conditions as

(i) Surface potential, $\psi_s(x)$, for symmetric mode operation, at front ($y=0$) and back ($y=T_{CH}$) surface can be evaluated as

$$\psi(x,y=0)=\psi(x,y=T_{CH})=\psi_S(x) \tag{3.3}$$

(ii) Electric fields at front and back surface are given by

$$\left.\frac{\partial\psi(x,y)}{\partial y}\right|_{y=0}=-\frac{\epsilon_{OX}}{\epsilon_{Si}T_{CH}}(\psi_S(x)-\phi_{GS}) \tag{3.4}$$

$$\left.\frac{\partial\psi(x,y)}{\partial y}\right|_{y=T_{CH}}=-\frac{\epsilon_{OX}}{\epsilon_{Si}T_{CH}}\left(\phi_{GS}-\psi_S(x)\right) \tag{3.5}$$

where, V_{GS} is the gate bias, $\phi_{GS}=V_{GS}-V_{FB}$, ϵ_{OX} is the permittivity of Silicon Dioxide (SiO_2), T_{OX} is the thickness of SiO_2, and V_{FB} is the the flatband voltage. From the equations (3.3) - (3.5), coefficients $c_1(x)$, $c_2(x)$ and $c_3(x)$, can be calculated and the equation (3.2) can be written as

$$\psi(x,y)=\psi_S(x)+\frac{\epsilon_{OX}(\psi_s(x)-\phi_{GS})}{\epsilon_{Si}T_{OX}}y-\frac{\epsilon_{OX}(\psi_s(x)-\phi_{GS})}{\epsilon_{Si}T_{CH}T_{OX}}y^2 \tag{3.6}$$

The conduction in the subthreshold region occurs at the centre of the silicon film i.e. $y=\frac{T_{CH}}{2}$. Thus, Poisson's equation can be solved at the centre of the film using equations (3.1) and (3.6), and the centre potential ($\psi_C(x)$) can be written as

$$\frac{\partial^2\psi_C(x,y)}{\partial x^2}-\frac{1}{\lambda_C^2}\psi_C(x)-\frac{1}{\lambda_C^2}\left(\phi_{GS}+\frac{q\lambda_C^2N_{CH}}{\epsilon_{Si}}\right)=0 \tag{3.7}$$

where, λ_C is the natural length at the centre of the channel and can be written as

$$\lambda_C = \sqrt{\left(\frac{\epsilon_{Si} T_{CH} T_{OX}}{2\epsilon_{OX}}\right)\left(1 + \frac{\epsilon_{OX} T_{CH}}{4\epsilon_{Si} T_{OX}}\right)} \tag{3.8}$$

The equation (3.7) reveals that the term $(\phi_{GS} + qN_{CH}\lambda_C^2/\epsilon_{OX})$ represents the long channel potential.

The general solution for equation (3.7) is represented by

$$\psi_C(x) = A_C e^{\frac{x}{\lambda_C}} + B_C e^{\frac{-x}{\lambda_C}} + V_{LC} \tag{3.9}$$

where, $V_{LC} = \phi_{GS} + \frac{qN_{CH}\lambda_C^2}{\epsilon_{Si}}$ is the long channel potential

The drain $(\psi_C(x = L_G) = V_{Bi} + V_{DS})$ and source $(\psi_C(x = 0) = V_{Bi})$ side boundary conditions can be used to evaluate the unknown coefficients, A_C and B_C as

$$A_C = \frac{(V_{Bi} - V_{LC})\left(1 - e^{-\frac{L_G}{\lambda_C}}\right) + V_{DS}}{2\sinh\left(\frac{L_G}{\lambda_C}\right)} \tag{3.10}$$

$$B_C = V_{Bi} - V_{LC} - \frac{(V_{Bi} - V_{LC})\left(1 - e^{-\frac{L_G}{\lambda_C}}\right) + V_{DS}}{2\sinh\left(\frac{L_G}{\lambda_C}\right)} \tag{3.11}$$

Solving equation 3.1 and 3.6 at the surface of the semiconductor ($y = 0$ and $y = T_{CH}$), the surface potential ($\psi_S(x)$) can be obtained as

$$\psi_S(x) = A_S e^{\frac{x}{\lambda_S}} + B_S e^{\frac{-x}{\lambda_S}} + V_{LS} \tag{3.12}$$

where, λ_S is the natural length at the surface of the channel and can be written as

$$\lambda_S = \sqrt{\frac{\epsilon_{Si} T_{CH} T_{OX}}{2\epsilon_{OX}}} \tag{3.13}$$

The long channel surface potential is given as $V_{LS} = \phi_{GS} + \frac{qN_{CH}\lambda_S^2}{\epsilon_{Si}}$, and the coefficients, A_S and B_S, can be evaluated by using the appropriate boundary conditions at drain $(\psi_S(x = L_G) = V_{Bi} + V_{DS})$ and source $(\psi_S(x = 0) = V_{Bi})$ as

$$A_S = \frac{(V_{Bi}-V_{LS})\left(1-e^{-\frac{L_G}{\lambda_S}}\right)+V_{DS}}{2\sinh\left(\frac{L_G}{\lambda_S}\right)} \tag{3.14}$$

$$B_S = V_{Bi} - V_{LS} - \frac{(V_{Bi}-V_{LS})\left(1-e^{-\frac{L_G}{\lambda_S}}\right)+V_{DS}}{2\sinh\left(\frac{L_G}{\lambda_S}\right)} \tag{3.15}$$

The sub-threshold current model [19] can be evaluated through

$$I_{DS} = \frac{2\pi kT\, n_i\, \mu_n \left(1-e^{\frac{-qV_{DS}}{kT}}\right)}{\int_0^{L_G} \frac{dx}{\int_0^{T_{CH}} e^{\frac{q\phi_c(x,y)}{kT}} dy}} \tag{3.16}$$

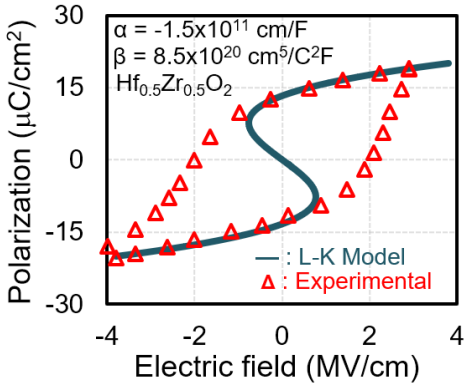

Fig 3.3: Calibration of Landau curve with the experimental polarization (Q_P) - Electric field (E_{FE}) [23] curve for α = -1.5×10^{11} cm/F and β = 8.5×10^{20} cm^5/C^{2}F corresponding to $Hf_{0.5}Zr_{0.5}O_2$.

3.1.3 Modelling of total internal gate charge density

The total internal gate charge, Q_{TOTAL}, consists of two components, (i) intrinsic internal gate charge due to space charge density (Q_{INT}), and (ii) fringing fields induced charge (Q_{FRINGE}).

i) The intrinsic gate charge can be expressed as

$$Q_{INT} = W_G C_{OX} \int_0^{L_G} (V_{IG} - V_{FB} - \psi_S(x))\, dx \tag{3.17}$$

where, W_G is the gate width, L_G is the gate length, V_{IG} is the internal gate voltage.

By integrating (3.13), total intrinsic gate charge due to space charge density can be obtained as

$$Q_{INT} = WC_{OX}\left[L_G(V_{IG} - V_{FB} - V_{LS}) - A_S\lambda_S\left(e^{\frac{L_G}{\lambda_S}} - 1\right) + B_S\lambda_S\left(e^{-\frac{L_G}{\lambda_S}} - 1\right)\right] \quad (3.18)$$

Rearranging the terms, equations (3.14) can be expressed in terms of V_{IG} and V_{DS} as

$$A_S = M_1 - C_2V_{IG} + SV_{DS} \quad (3.19)$$

$$B_S = M_2 + (C_2 - 1)V_{IG} - SV_{DS} \quad (3.20)$$

where, the coefficients can be expressed as

$$M_1 = C_2(V_{Bi} - C_1) \quad (3.21)$$

$$M_2 = V_{Bi} - C_1 - M_1 \quad (3.22)$$

$$C_1 = \frac{qN_{CH}\lambda_S^2}{\epsilon_{Si}} - V_{FB} \quad (3.23)$$

$$C_2 = \frac{\left(1 - e^{-\frac{L_G}{\lambda_S}}\right)}{\left(2\sinh\left(\frac{L_G}{\lambda_S}\right)\right)} \quad (3.24)$$

$$S = \frac{1}{2\sinh\left(\frac{L_G}{\lambda_S}\right)} \quad (3.25)$$

From equations (3.19) and (3.20), internal gate charge can be expressed as

$$Q_{INT} = W_GC_{OX}\left[L_G(V_{IG} - V_{FB} - V_{LS}) - (M_1 - C_2V_{IG} + SV_{DS})\lambda_S\left(e^{\frac{L_G}{\lambda_S}} - 1\right) + (M_2 + (C_2 - 1)V_{IG} - SV_{DS})\lambda_S\left(e^{-\frac{L_G}{\lambda_S}} - 1\right)\right] \quad (3.26)$$

$$Q_{INT} = W_GC_{OX}\left[L_G(-V_{FB} - C_1) - M_1\lambda_S\left(e^{\frac{L_G}{\lambda_S}} - 1\right) + C_2\lambda_S\left(e^{\frac{L_G}{\lambda_S}} - 1\right)V_{IG} - S\lambda_S\left(e^{\frac{L_G}{\lambda_S}} - 1\right)V_{DS} + M_2\lambda_S\left(e^{-\frac{L_G}{\lambda_S}} - 1\right) + (C_2 - 1)\lambda_S\left(e^{-\frac{L_G}{\lambda_S}} - 1\right)V_{IG} - S\lambda_S\left(e^{-\frac{L_G}{\lambda_S}} - 1\right)V_{DS}\right] \quad (3.27)$$

$$Q_{INT} = W_GC_{OX}[C_3 + C_4V_{IG} - C_5V_{DS}] \quad (3.28)$$

where, the coefficients can be expressed as

$$C_3 = L_G(-V_{FB} - C_1) - M_1\lambda_S\left(e^{\frac{L_G}{\lambda_S}} - 1\right) + M_2\lambda_S\left(e^{-\frac{L_G}{\lambda_S}} - 1\right) \quad (3.29)$$

$$C_4 = C_2\lambda_S\left(e^{\frac{L_G}{\lambda_S}} - 1\right) + (C_2 - 1)\lambda_S\left(e^{-\frac{L_G}{\lambda_S}} - 1\right) \quad (3.30)$$

$$C_5 = S\lambda_S\left(e^{\frac{L_G}{\lambda_S}} - 1\right) + S\lambda_S\left(e^{\frac{-L_G}{\lambda_S}} - 1\right) \quad (3.31)$$

ii) The charge due fringing fields can be modelled as [20]

$$Q_{FRINGE} = C_{OF}(2V_{IG} - V_{DS}) \quad (3.32)$$

where C_{OF} is the parasitic capacitance which is estimated using the ATLAS TCAD tool.

Therefore, the total internal gate charge density form equations (3.26) and (3.30) can be expressed as

$$Q_{TOTAL} = Q_{INT} + Q_{FRINGE} \quad (3.33)$$

$$Q_{TOTAL} = W_G C_3 + (2C_{OF} + W_G C_{OX} C_4)V_{IG} - (C_{OF} + W_G C_{OX} C_5)V_{DS} \quad (3.34)$$

$$Q_{TOTAL} = X + YV_{IG} - ZV_{DS} \quad (3.35)$$

where, the coefficients can be expressed as

$$X = \frac{W_G C_{OX} C_3}{W_G L_G} \quad (3.36a)$$

$$Y = \frac{(2C_{OF} + W_G C_{OX} C_4)}{W_G L_G} \quad (3.36b)$$

$$Z = \frac{(C_{OF} + W_G C_{OX} C_5)}{W_G L_G} \quad (3.36c)$$

The 1-D Landau-Khalatnikov (L-K) equation can be used for determining the electric field across the ferroelectric (E_{FE}), in terms of ferroelectric polarization charge density (Q_P) [17] as

$$E_{FE} = 2\alpha Q_P + 4\beta Q_P^3 + 6\gamma Q_P^5 \quad (3.37)$$

where α, β, and γ are Landau's parameters [17]. The potential across the ferroelectric layer (V_{FE}) can be represented as

$$V_{FE} = \alpha_0 Q_P + \beta_0 Q_P^3 + \gamma_0 Q_P^5 \quad (3.38)$$

The coefficients, α_0, β_0, and γ_0, depend on the Landau's parameters as well as ferroelectric layer, are given as

$$\alpha_0 = 2\alpha T_{FE} \tag{3.39a}$$

$$\beta_0 = 4\beta T_{FE} \tag{3.39b}$$

$$\gamma_0 = 6\gamma T_{FE} \tag{3.39c}$$

In subthreshold region since the terminal charge is much lower, the higher order terms in the equation (3.38) can be ignored [21] and the voltage drop across ferroelectric layer can be obtained as

$$V_{FE} = \alpha_0 Q_P \tag{3.40}$$

Finally, the total internal charge density Q_{TOTAL}, from equation (3.35) can be used in the equation (3.40) as follows.

$$V_{FE} = \alpha_0 X + \alpha_0 Y V_{IG} - \alpha_0 Z V_{DS} \tag{3.41}$$

In a MFMIS structure of NC JLFET, the relation between terminal voltages is

$$V_{GS} = V_{IG} + V_{FE} \tag{3.42}$$

Combining equations (3.41) and (3.42) and rearranging the terms, we can obtain a closed form relation as

$$V_{IG} = A_1 V_{GS} + A_2 V_{DS} + A_3 \tag{3.43}$$

where, the coefficients can be expressed as

$$A_1 = \frac{1}{1+\alpha_0 Y} \tag{3.44a}$$

$$A_2 = \frac{Z a_0}{1+\alpha_0 Y} \tag{3.44b}$$

$$A_3 = -\frac{X \alpha_0}{1+\alpha_0 Y} \tag{3.44c}$$

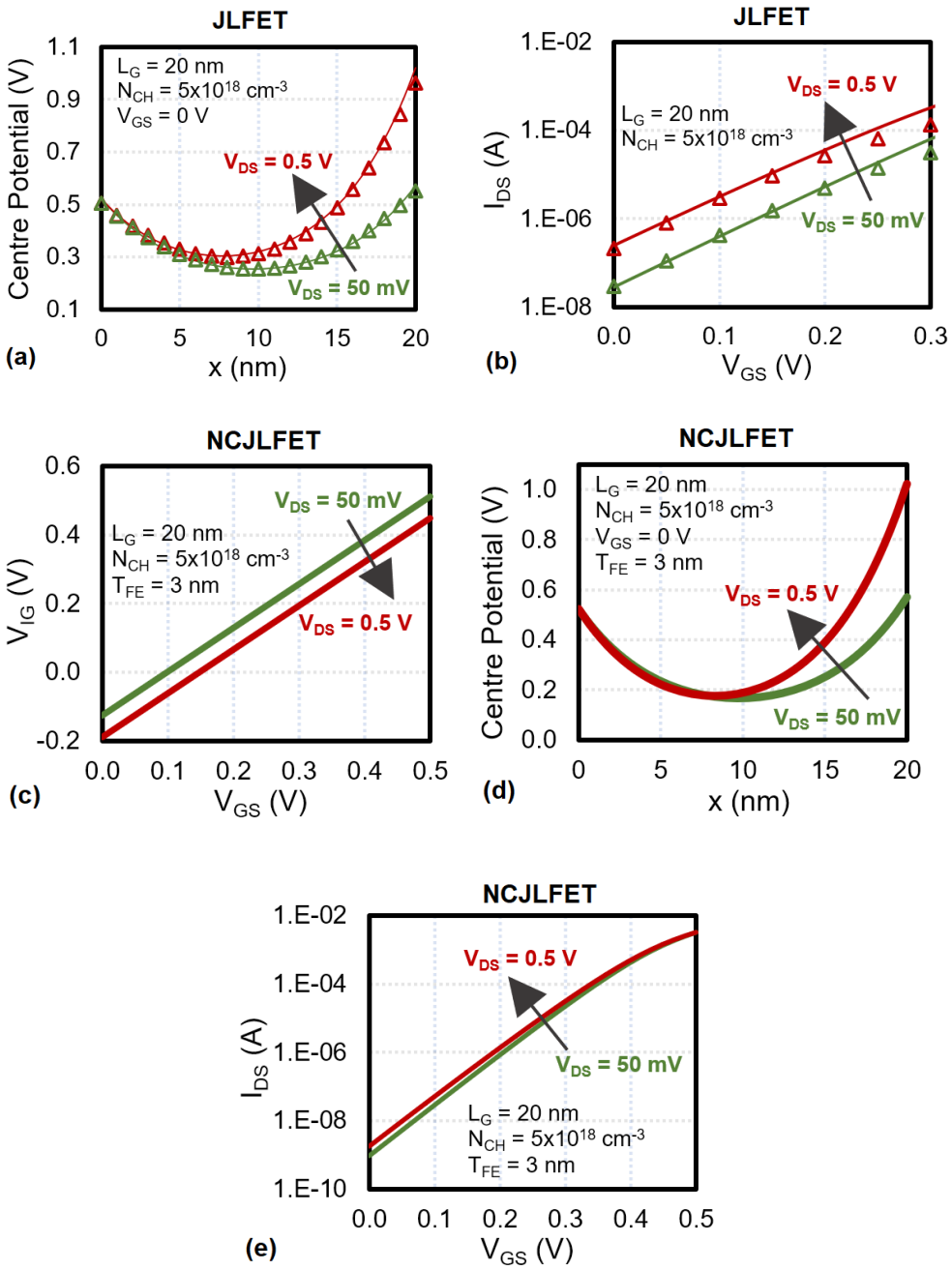

Fig 3.4: Variation of (a) centre potential (ψ_C) and (b) drain current (I_{DS}) of JLFET at V_{DS} = 50 mV and 500 mV. Variation of (c) internal gate voltage (V_{IG}), (d) ψ_C and, (e) I_{DS} of the NC JLFET at V_{DS} = 50 mV and 500 mV. Symbol represents the simulation data while the lines represent the model data.

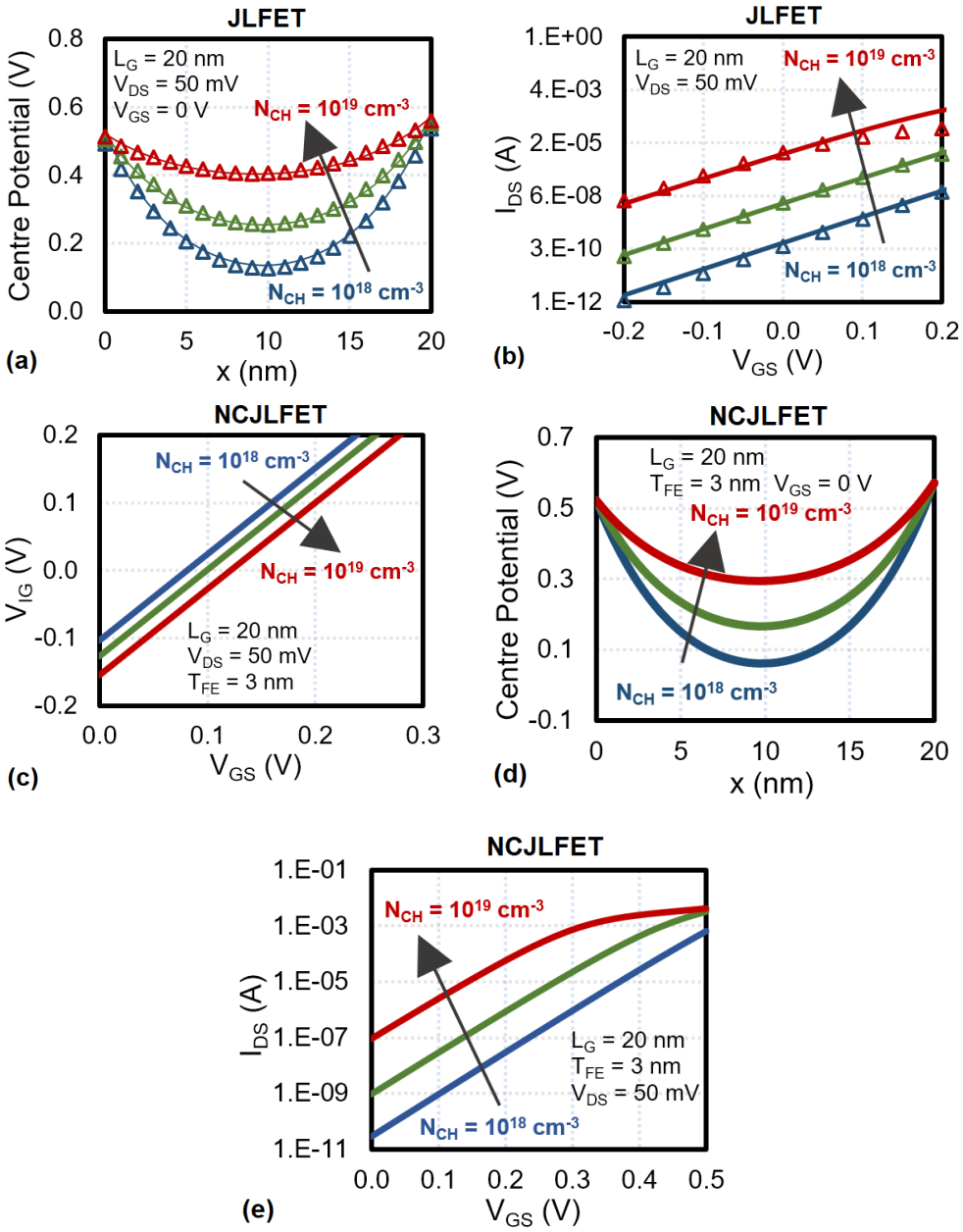

Fig 3.5: (a) Variation of centre potential (ψ_C) of baseline JLFET along the channel length (x) for various channel doping concentration (N_{CH}). (b) Variation of I_{DS} with V_{GS} of the baseline JLFET for various channel doping concentration, (c) Variation of V_{IG} in NC JLFET with V_{GS} for various channel doping concentration, (d) Variation of ψ_C of NC JLFET along the channel length for various channel doping concentration, (e) Variation of I_{DS} with V_{GS} of the NC JLFET for various channel doping concentration. Symbol represents the simulation data while the lines represent the model data.

3.2 Results and Model Validation

Fig. 3.1 shows the schematic of a DG NC JLFET analysed in this work, which has an internal oxide thickness (T_{OX}) of 1 nm, source/drain doping of 10^{20} cm^{-3}, silicon film thickness (T_{CH}) of 10 nm, and gate width (W_G) of 1000 nm. However, other parameters such drain bias (V_{DS}) is varied from 50 mV to 0.5 V, channel doping (N_{CH}) varied from 10^{18} cm^{-3} to 10^{19} cm^{-3}, gate length (L_G) length varied from 14 nm to 20 nm and ferroelectric thickness (T_{FE}) varied from 2 nm to 4 nm. The results obtained from the model for baseline JLFET are validated against the simulation results obtained from ATLAS TCAD simulator [24].

DG NC JL transistors have been analysed with $Hf_{0.5}Zr_{0.5}O_2$ (HZO) as the ferroelectric layer. Landau's parameters used in this work are extracted from the experimentally reported P-E curve of HZO [23]. The parameters of ferroelectric material in L-K equation can be extracted as shown in fig 3.3. This work is focused on the subthreshold operation; thus, the analysis is restricted to 0.5 V for V_{GS} and V_{DS}

Fig 3.4(a)-(b) represents the variation in centre potential and drain current of baseline JLFET for different drain voltages. Increasing the drain bias a rise in centre potential barrier is observed i.e. drain induced barrier lowering (DIBL) (Fig. 3.4(a)). Also, because of DIBL, a degradation in off current can be observed as shown in Fig. 3.4(b). The developed model for the baseline JL FET shows good agreement with the simulation data obtained from ATLAS tool [24]. Fig 3.4(c) represents the relation between internal (V_{IG}) and external (V_{GS}) gate voltage. Due to the presence of the ferroelectric layer and its negative capacitance phenomenon, the internal gate voltage become negative at zero external gate voltage, and the internal gate voltage become more negative as the drain voltage increases. Because of more the negative internal gate voltage, a less degradation in minimum potential is observed in NC JLFET at higher drain bias (fig 3.4(d)). The effect can also be observed in the drain current variation, where a less degradation in threshold voltage is observed as the drain bias increases compared to JLFET (fig 3.4(e)). Therefore, a lower degree of DIBL is observed in the NC JLFET compared to JLFE

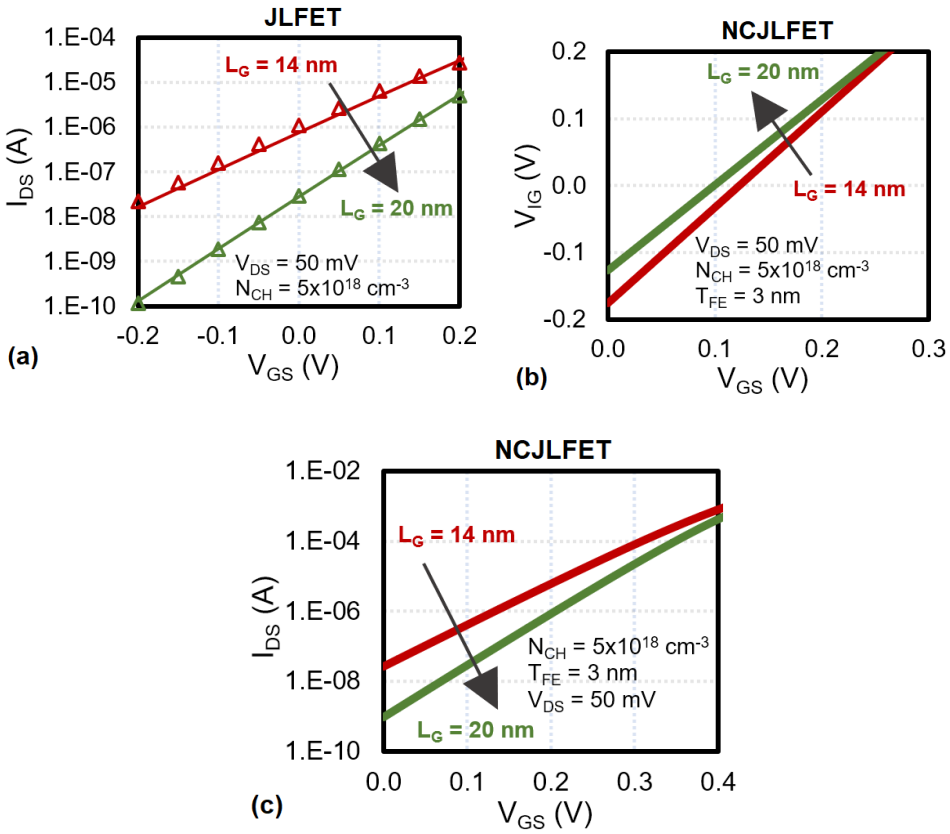

Fig 3.6: (a) Variation of drain current (I_{DS}) with gate to source voltage (V_{GS}) of the baseline JLFET for gate length of 14 nm and 20 nm, (b) Variation of internal gate voltage (V_{IG}) in NC JLFET with gate to source voltage (V_{GS}) for gate length of 14 nm and 20 nm, (c) Variation of drain current (I_{DS}) with gate to source voltage (V_{GS}) of the NC JLFET for gate length of 14 nm and 20 nm. Symbol represents the simulation data while the lines represent the model data.

Fig 3.5(a)-(b) represents the variation in centre potential and drain current for different channel doping concentration. Results indicate that for higher channel doping concentration it becomes difficult to deplete the channel, which results in higher channel potential (Fig. 3.5(a)) and a higher off-current (Fig. 3.5(b)). Fig 3.5(c) represents the relation between internal and external gate voltage for various doping. As doping in channel increases, the charge coupled with the ferroelectric layer also increases which leads to a further reduction in the internal gate voltage. Thus, a more negative internal gate voltage prevents the degradation of potential barrier compared to JLFET (fig 3.5(d)). Therefore, an improved subthreshold characteristic (fig 3.5(e)) is observed in NC JLFET. Hence, the degradation in subthreshold characteristics

is much lower in NC JLFET as compared to the baseline JL FET characteristics for higher channel doping.

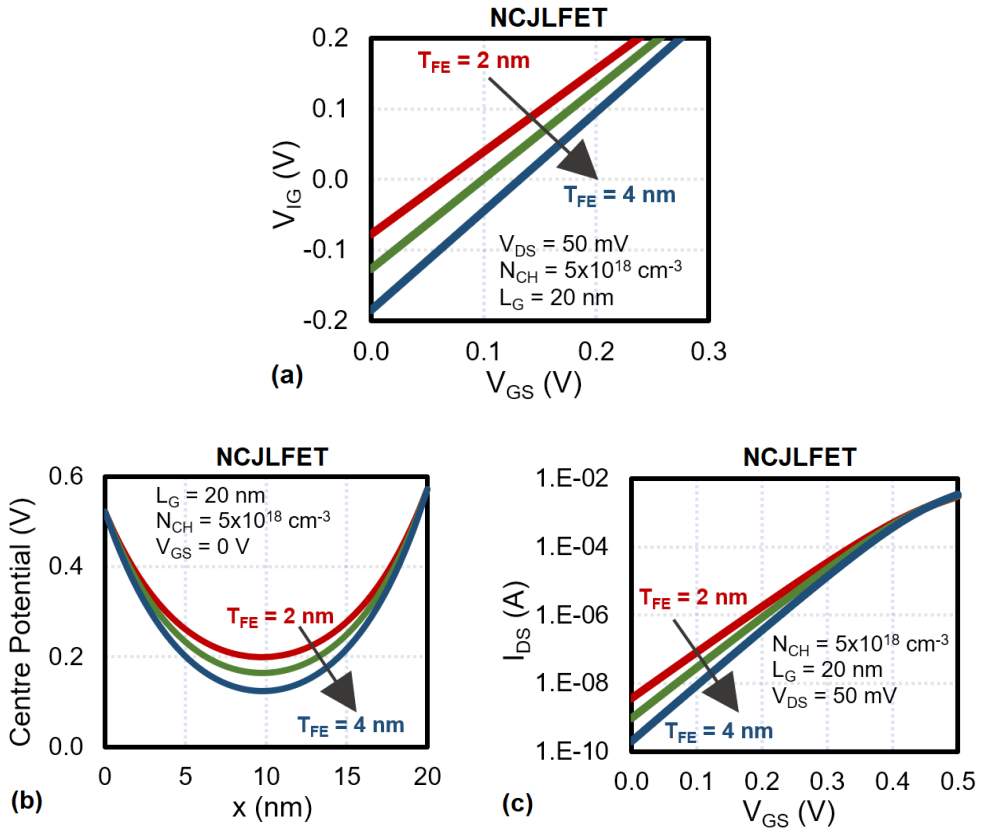

Fig 3.7: (a) Variation of internal gate voltage (V_{IG}) in NC JLFET with gate to source voltage (V_{GS}) for different ferroelectric thickness, (b) Variation of centre potential (ψ_C) of NC JLFET along the channel length (x) for different ferroelectric thickness, (c) Variation of drain current (I_{DS}) with gate to source voltage (V_{GS}) of the baseline JLFET for different ferroelectric thickness.

Fig 3.6(a) represents the variation in drain current of baseline JLFET for different gate lengths (14 nm and 20 nm). Results also indicate that at lower gate lengths, the subthreshold characteristics degrade due to SCEs. However, at shorter gate length, the fringing coupling become stronger, which results in more negative internal gate voltage at shorter gate length (Fig 3.6(b)). A negative internal gate voltage prevents the degradation of subthreshold characteristics as shown in Fig 3.6(c). Hence, the degradation in subthreshold characteristics is much lower as compared to baseline JL FET characteristics at lower gate length. This shows the potential for further scaling of the device.

Fig 3.7(a)-(c) shows the effect of ferroelectric thickness on the performance of NC JLFET. For a thicker ferroelectric layer, the internal voltage amplification enhances, thus providing more negative internal gate voltage at zero external gate voltage, which is due to improved capacitance matching. For a higher ferroelectric thickness, the capacitance matching between ferroelectric capacitor (C_{FE}) and internal capacitance (C_{INT}) (which is the parallel combination of oxide capacitance (C_{OX}) and MOS capacitance (C_{MOS}), improves which results in a higher internal gain [25]. A more negative internal gate voltage at thicker ferroelectric thickness, further increases the centre potential barrier (Fig 3.7(b)), which causes an improved subthreshold characteristics (fig 3.7(c)), Therefore, for higher ferroelectric thickness, an enhanced channel depletion is possible at zero gate bias, which results in a lower off-current.

3.3 Conclusion

This chapter provides a detailed analysis of the subthreshold characteristics of DG NC JL MOSFETs. The proposed closed form model predicts the effect of drain bias, channel doping, length scaling, and ferroelectric thickness on the NC JLFET through the variation of internal gate voltage, channel potential and drain current. The internal gate provides an equipotential surface, as a result both devices (baseline JLFET and ferroelectric layer) can be treated separately. Thus, the calibration baseline JLFET device is done with TCAD simulation and the calibration of Landau parameters is done with the experimental data. The evaluation of subthreshold swing and SCEs related parameters is been carried out using a simplified analytical solution for subthreshold drain current. The results shows that inclusion of the ferroelectric layer improves the subthreshold characteristics, which shows a good potential for further downscaling of the device and suitability for ULP subthreshold operation.

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Chapter 4

Ultralow Power Subthreshold Inverter with NC JLFET

4.1 Introduction

Ultralow power devices are widely used to reduce power consumption in several areas such as computing, portable electronics, smart sensors, networking and communication [1]. Historically, different digital logic families such as Transistor-Transistor Logic (TTL) [1]-[3], Resistor-Transistor Logic (RTL) [1]-[3], Emitter-Coupled Logic (ECL) [1]-[3], Complementary MOS (CMOS) logic [1]-[6], and Metal-Oxide-Semiconductor (MOS) logic [1]-[3] were considered to implement integrated circuits (ICs). Out of these logic families, CMOS logic is the widely implemented logic for ULP integrated circuits because of its low power consumption and high noise margin [1]-[3].

Input Voltage (V_{IN})	**Region of Operation (nMOS)**	**Region of Operation (pMOS)**
$0 < V_{IN} < V_{TH,N}$	Cut-off region	Linear region
$V_{TH,N} < V_{IN} < \frac{V_{DD}}{2}$	Saturation region	Linear region
$V_{IN} = \frac{V_{DD}}{2}$	Saturation region	Saturation region
$\frac{V_{DD}}{2} < V_{IN} < V_{DD} - \lvert V_{TH.P} \rvert$	Linear region	Saturation region
$V_{DD} - \lvert V_{TH,P} \rvert < V_{IN} < V_{DD}$	Linear region	Cut-off region

Table 4.1: Various operating regions of pMOS and nMOS transistor in a CMOS inverter for different input voltage (V_{IN}) ranges. $V_{TH,N}$ and $V_{TH,P}$ represents the threshold voltages for n and p-type MOSFET, respectively [2].

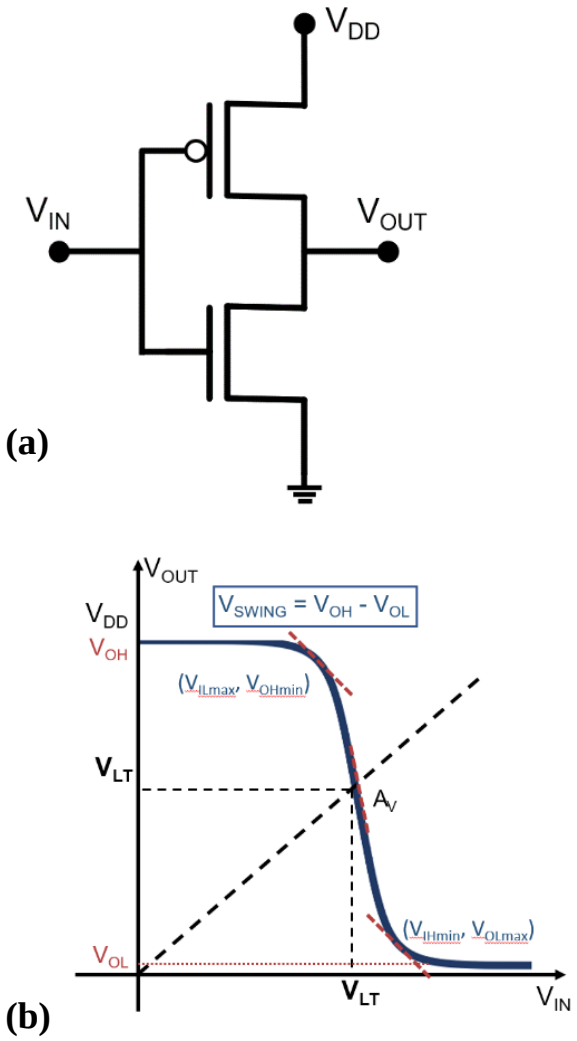

Fig 4.1: Schematic representation of (a) ULP NC JLFET inverter, and its (b) voltage transfer characteristics (VTC) showing the DC figure of merits.

4.1.1 CMOS Inverter

CMOS logic is a basic building block to realize complex logic circuits, which consists of a pMOS and nMOS transistor fabricated on the same substrate or SOI layer [3]. Figure 4.1(a) shows the schematic of a ULP NC JLFET inverter which has an input (V_{IN}) applied to the gate of p-type and n-type NC JLFET devices, a supply voltage (V_{DD}) and an output terminal (V_{OUT}). Figure 4.1(a) shows the voltage transfer characteristics (VTC) of ULP NC JLFET inverter, where output changes from V_{OH} to V_{OL} when the input voltage varies from 0 to V_{DD}. During this transition, nMOS and the pMOS devices go through several regions of operation as shown in the table 4.1.

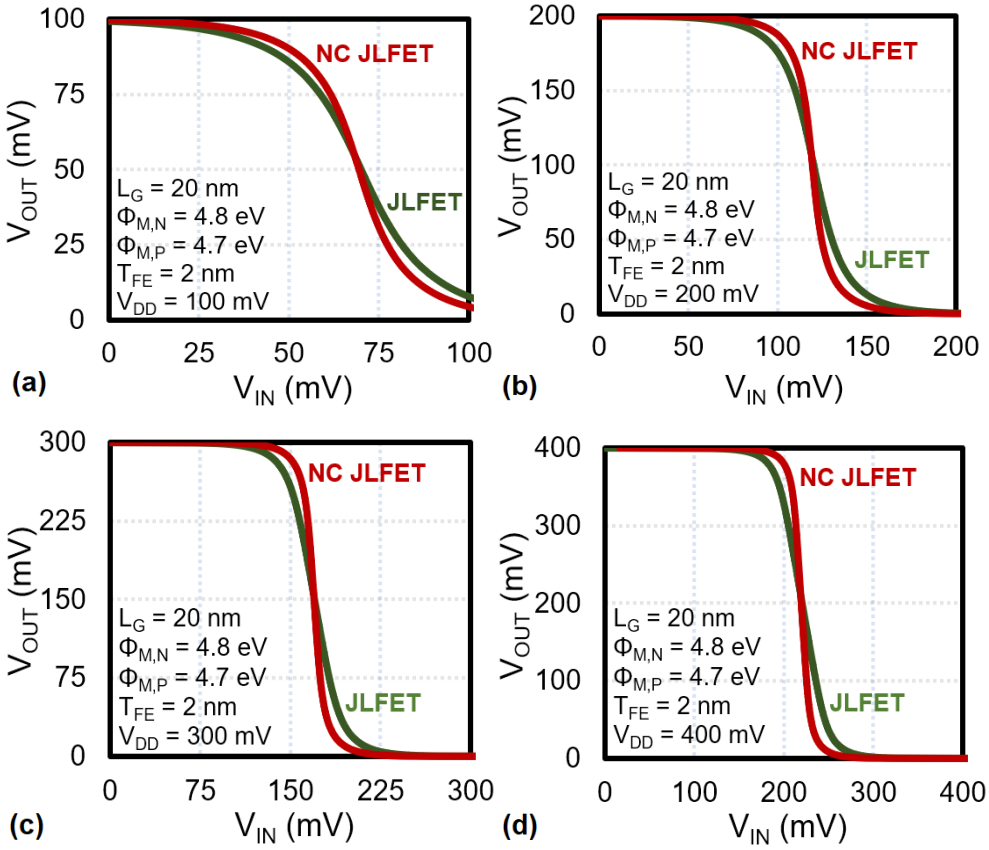

Fig 4.2: Comparison of VTC of CMOS inverter with JLFET and NC JLFET with a ferroelectric layer thickness of 2 nm for a supply voltage of (a) 0.1 V, (b) 0.2 V, (c) 0.3 V and (d) 0.4 V.

Figure 4.1(b) shows the schematic representation of the DC voltage transfer characteristics of a subthreshold inverter, where V_{IN} is the input voltage, V_{OUT} is the output voltages, respectively, and V_{DD} is the supply voltage. V_{OH} and V_{OL} represent the higher and lower output voltage level attained in VTC for a full input voltage swing, respectively. Ideally, V_{OH} should be V_{DD} while V_{OL} should be 0 V. V_{LT} represents the logic threshold (V_{LT} = V_{IN} = V_{OUT}) which should be V_{DD}/2 for a balanced CMOS inverter (fig 4.1(b)). V_{SWING} represents an output swing for a full input swing from 0 to V_{DD}, and A_V is the DC voltage gain at logic threshold.

In ULP subthreshold operation, the CMOS characteristics degrade because of poor on-to-off current ratio, lower supply voltage, higher parasitic capacitances and SCEs [7]-[9]. This makes a degraded voltage transfer characteristics (VTC) and the figure of merits deviate from their nominal values,

which affects applicability and robustness of the circuit. Using a negative capacitance transistor, the performance of ULP inverter can be improved, because of a potentially higher on-to-off current ratio in a negative capacitance transistor, and that too, at lower supply voltage which results from sub-60 mV/dec subthreshold swing [10].

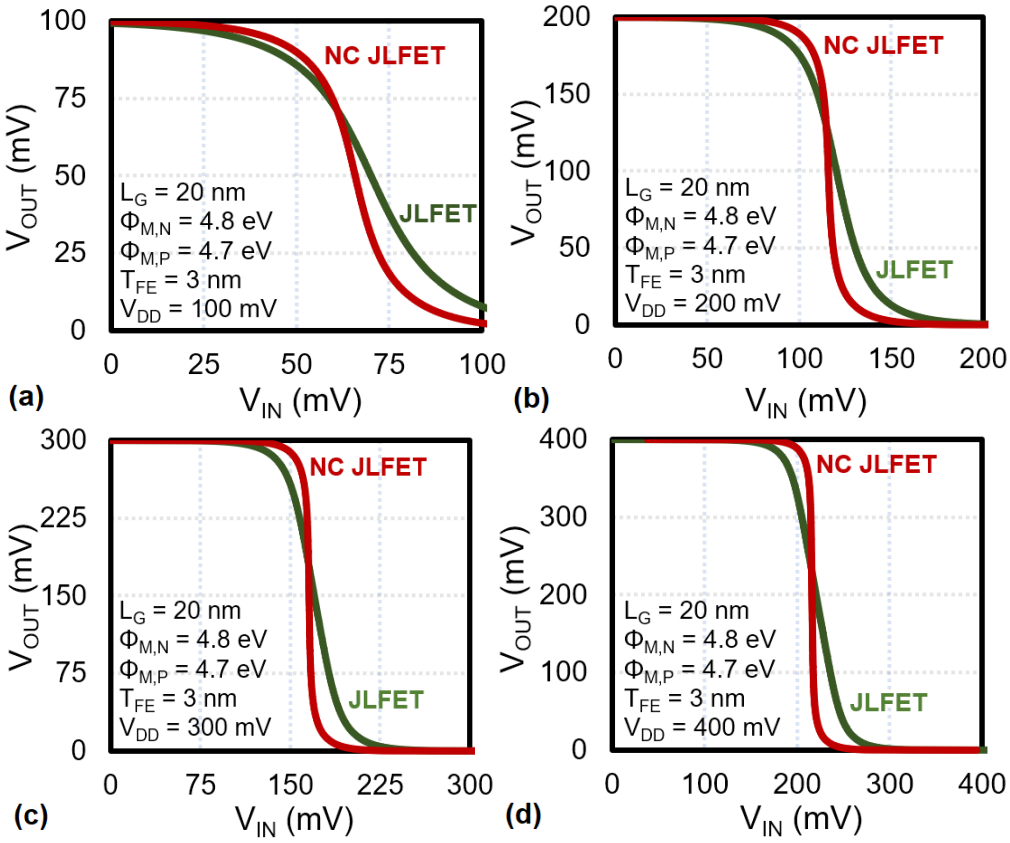

Fig 4.3: Comparison of VTC of CMOS inverter with JLFET and NC JLFET with a ferroelectric layer thickness of 3 nm for supply voltage of (a) 0.1 V, (b) 0.2 V, (c) 0.3 V and (d) 0.4 V.

4.2 Results and Discussion

The CMOS inverter analysed here consists of a double gate (DG) device with gate length (L_G) of 20 nm, silicon channel thickness (T_{CH}) of 10 nm, SiO_2 thickness (T_{OX}) of 1 nm FE thickness (T_{FE}) of 2 nm, 3 nm and 6 nm, channel doping of 10^{19} cm^{-3}, and gate workfunction of 4.8 eV (for nMOS) and 4.7 eV (for pMOS). To check the suitability of the device for ULP subthreshold

applications, the VTC have been analysed for V_{DD} varying from 100 mV to 400 mV.

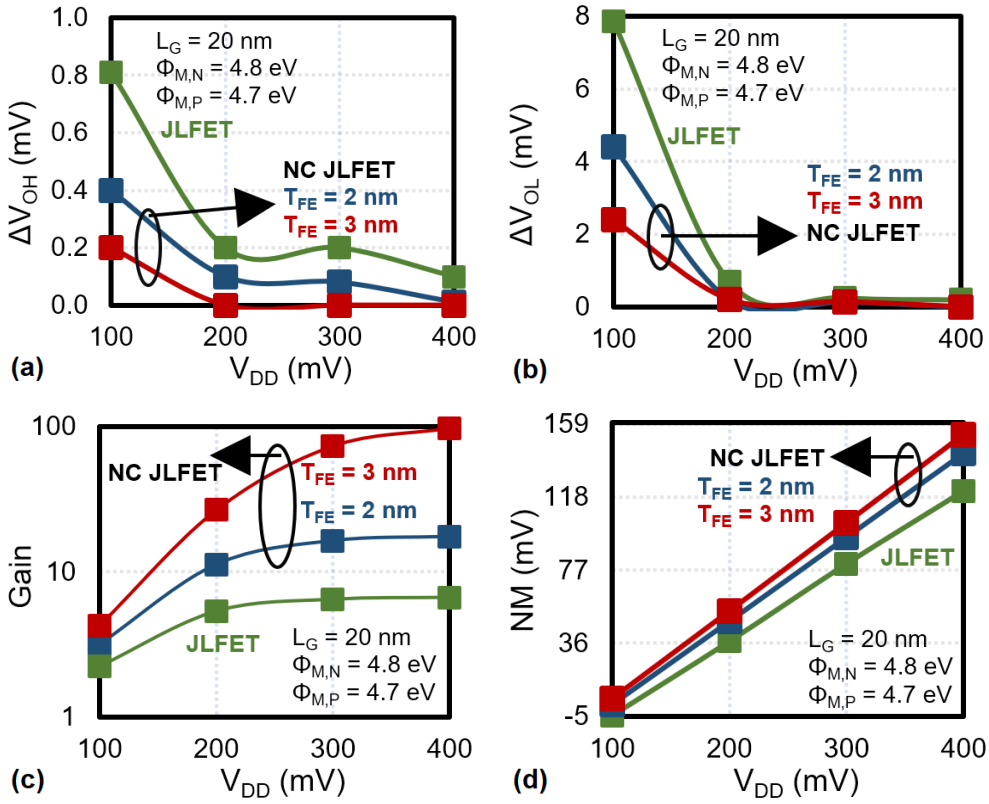

Fig 4.4: Variation of deviation in (a) higher output level (ΔV_{OH}), and (b) lower output level (ΔV_{OL}) from ideal value with supply voltage. Variation of (c) Gain, and (d) Noise margin of JLFET and NC JLFET (T_{FE} = 2 nm and 3 nm) with supply voltage.

Fig 4.2 (a)-(d) shows the comparison of voltage transfer characteristics of JLFET and NC JLFET ULP subthreshold inverter for a ferroelectric thickness of 2 nm. For ULP application, the supply voltage is kept lower than the device threshold (< 400 mV). Figure 4.2 (a)-(d) shows that by decreasing the supply voltage from 400 mV to 100 mV, the transition becomes smoother in both JLFET and NC JLFET. Also, at a lower supply voltage (100 mV), a clear deviation of minimum and maximum output voltage levels from their ideal values can be observed in both JLFET and NC JLFET (Fig. 4.2 (a)). However, NC JLFET clearly shows a better DC gain (a sharper transition) along with the improved minimum and maximum output voltage levels because of suppressed SCEs and higher on-to-off current ratio.

Similarly, Fig 4.3 (a)-(d) shows the comparison of voltage transfer characteristics of JLFET and NC JLFET subthreshold inverter for a ferroelectric thickness of 3 nm. Increasing the ferroelectric thickness, improves the capacitance matching, which leads to a steeper current transition or higher on-to-off current ratio [11]. An improvement in minimum and maximum output voltage levels, and gain is observed with a ferroelectric thickness of 3 nm compared to 2 nm (Fig. 4.2 (a)-(d)). Also, for a supply voltage of 400 mV, a nearly ideal VTC can be observed for T_{FE} = 3 nm because of improved subthreshold swing and DIBL.

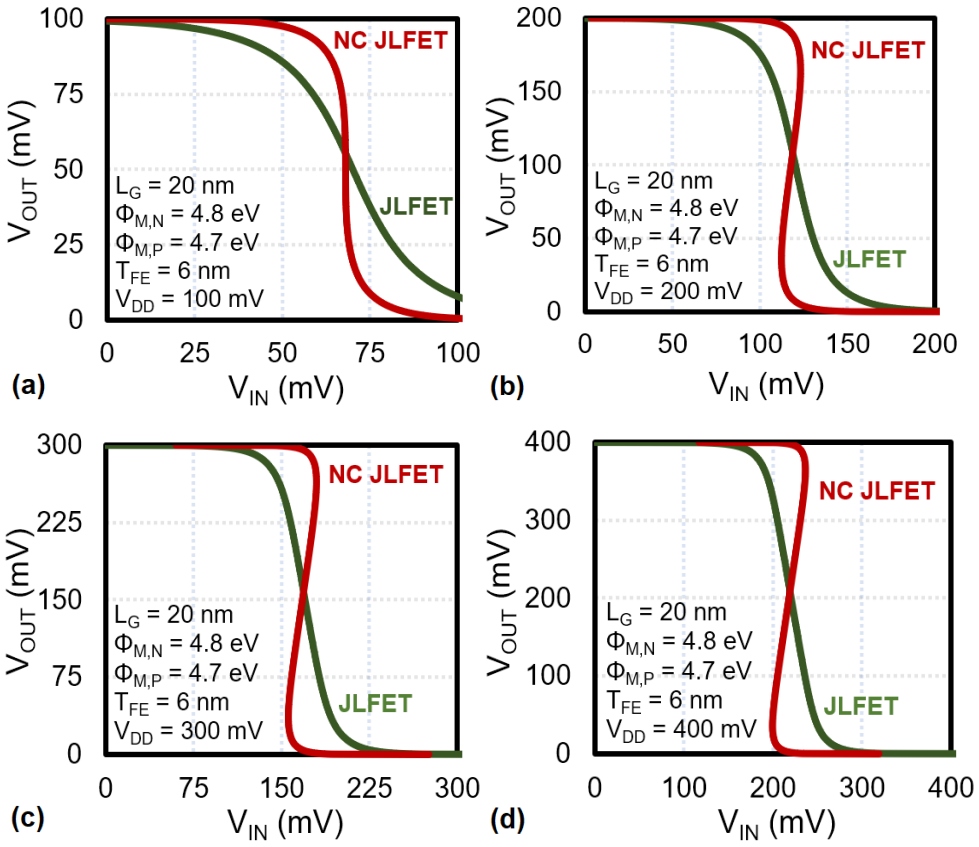

Fig 4.5: Comparison of VTC of CMOS inverter with JLFET and NC JLFET with a ferroelectric layer thickness of 6 nm for supply voltage of (a) 0.1 V, (b) 0.2 V, (c) 0.3 V and (d) 0.4 V.

Figure 4.4 (a)-(d) shows the comparison of the figure of merits of JLFET and NC JLFET subthreshold inverters for different supply voltages. Fig. 4.4 (a)-(b) shows the deviation of high and low output voltage levels from their ideal values i.e $\Delta V_{OH} = V_{DD} - V_{OH}$ and $\Delta V_{OL} = V_{OL}$ [12]. A lower deviation in V_{OH}

(< 1 mV) is observed compared to V_{OL}. At higher supply voltages (> 200 mV), the deviation in V_{OH} and V_{OL} in both JLFET and NC JLFET inverter remains the same. However, for a supply voltage of 100 mV a significant improvement can be observed in ΔV_{OL} with NC JLFET i.e ~8 mV in JLFET, ~4.5 mV in NC JLFET with T_{FE} = 2 nm and ~2.5 mV in NC JLFET with T_{FE} = 3 nm. A significant improvement in gain can be observed in NC JLFET, which can be further improved by increasing the ferroelectric thickness from 2 nm to 3 nm. Unlike the V_{OH} and V_{OL}, a significant difference in gain is observed at a higher supply voltage i.e. ~7 in JLFET, ~20 in NC JLFET with T_{FE} = 2 nm and ~100 in NC JLFET with T_{FE} = 3 nm. Noise margin (NM) is defined as a maximum noise from an external source that can be added to the input voltage level without causing any deviation in output voltage from actual logic level [13]. Reducing the supply voltage, a degradation in NM can be observed (Fig. 4.4 d)) because of smoother transition of VTC [14]. However, by using NC JLFET, NM can be improved i.e ~120 mV in JLFET, ~142 mV in NC JLFET with T_{FE} = 2 nm and ~153 mV in NC JLFET with T_{FE} = 3 nm.

Similarly, Fig. 4.5 (a)-(d) shows the comparison of voltage transfer characteristics of JLFET and NC JLFET subthreshold inverter for a relatively higher ferroelectric thickness (6 nm). Increasing the FE thickness to 6 nm, NDR in the output characteristics increases which results in multiple current intersections around logic threshold and results a hysteresis in the VTC (Fig 4.5 (b)-(d)). For a smaller supply voltage (100 mV), NDR become very insignificant, which results in a hysteresis free VTC (Fig. 4.5(a)). Therefore, to avoid the hysteresis, ferroelectric thickness and supply voltage can be optimized.

4.3 Conclusion

Among all logic families, the CMOS logic family is widely used in low power applications because of low static power dissipation, and high noise margin. However, for ultralow supply voltage (less than the threshold voltage of the device), because of poor on-to-off current ratio, circuit robustness is challenging. A subthreshold inverter is the most important building block for ULP memory. Therefore, the subthreshold inverter implemented through JLFET and NC JLFET is analysed in this work. The degradation in figure of merits of subthreshold inverter at very low supply voltage (100 mV) is highlighted in this chapter.

In NC JLFET the subthreshold characteristics such as I_{ON}/I_{OFF} ratio drain induced barrier lowering, and subthreshold swing can be improved which can enhance the inverter characteristics for ultralow voltages. The effect of lower supply voltage on degradation in inverter characteristics is significantly reduced in case of NC JLFET transistors. The nominal high and low output voltage levels, DC gain, and noise margin can be improved significantly in NC JLFET compared to JLFET. At higher ferroelectric thickness the performance of the subthreshold inverter can further improve. However, for a thicker ferroelectric thickness, a hysteresis is observed in the voltage transfer characteristics because of the negative differential resistance in the output characteristics.

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Chapter 5

Conclusions and Scope for Future Work

5.1 Conclusion

Junctionless FET can be a potential alternative for next generation low power transistors [1]-[3]. They offer several advantages such as no p-n junction formation, which makes the fabrication process simple and cost effective, reduced SCEs and enhanced scalability than the conventional inversion mode FET [4][5]. Since a JL FET is expected to have better subthreshold characteristics with reduced SCEs, the architecture exhibits potential for ULP applications [6][7]. Apart from the above-mentioned improvements, there are some challenges in JL topology. As the entire film is heavily doped with a single dopant type, which increases the off current of the device Heavily doping makes it very difficult to entirely deplete the channel which increases the value of the metal work function. A metal with workfunction higher than the mid-gap workfunction (4.71 eV) has poor thermal stabilization and poor adhesion with the gate oxide [8]. High doping concentration also requires the film to be ultrathin to achieve desired volume depletion and also causes effects such as RDFs, impurity scattering and mobility degradation [8].

Further, ferroelectric (FE) materials were studied to show a negative capacitance (NC) phenomenon which can exhibit potential for steep switching when used with inversion mode or junctionless FET [9]-[12]. By adding a dielectric (DE) layer in series with the FE layer, the NC region can be stabilized. Such a configuration can be formed by stacking the ferroelectric layer over the gate and gate oxide of a JL FET [10]-[12]. The effects of JL FET due to heavily doped film are significantly reduced such as the internal voltage amplification which makes it possible to achieve volume depletion at a lower metal gate work function (midgap workfunction) by providing negative voltage at the internal gate for a zero value of control gate voltage. The other parameters such as drain bias, channel doping, gate length, and the FE layer have several positive effects on the subthreshold characteristics of NC JLFET, which have been analysed in this work.

The derived closed form relation between internal gate voltage terms of terminal voltages is utilized to analyse the subthreshold behaviour of DG NC JL FET. The proposed model describes the dependence of SCEs on channel doping, gate length, ferroelectric layer thickness and drain voltage. The improvements such as negative DIBL and reduced subthreshold swing have also been observed.

The CMOS logic family offers very low static power dissipation as compared to others which makes it suitable for ULP operation. A subthreshold CMOS inverter with NC JL FET is analysed. I_{ON}/I_{OFF} and subthreshold swing are the performance parameters of a ULP subthreshold CMOS inverter. In chapter 4, the application of the derived model is extended for subthreshold CMOS inverter implemented using NC JL FET. The effect of negative capacitance of FE layer on inverter parameters such as V_{OH}, V_{OL}, V_{IH}, V_{IL} and V_{LT} is observed. The FE layer thickness has strong impact on the subthreshold characteristics. As the FE layer is made thicker, the capacitance matching can improve and the inverter characteristics can be improved. However, for a very high ferroelectric thickness, because of NDR, hysteresis is observed in the VTC.

5.2 Future Work

The proposed model can be used to derive closed form analytical expressions for determining the DC figure of merits of a hysteresis free ULP NC JLFET-inverter such as lower and higher output voltage swing level, voltage swing, logic threshold, gain, and noise margin. Also, the model can be adapted to find the conditions for hysteresis free VTC in subthreshold operation. Also, at nanoscale dimensions, quantum confinement effects are expected to affect the device performance. Thus, the consideration of quantum effects is also essential and can be added to the analytical model.

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