Optical Guidance and Control in FINFET Structure

M.Tech. Thesis

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **OPTICAL GUIDANCE AND CONTROL IN FINFET LIKE STRUCTURE** in the partial fulfillment of the requirements for the award of the degree of **MASTER OF TECHNOLOGY** and submitted in the **DISCIPLINE OF ELECTRICAL ENGINEERING , INDIAN INSTITUTE OF TECHNOLOGY INDORE**, is an authentic record of my own work carried out during the time period from June 2021 to June 2022 under the supervision of **Dr. Mukesh Kumar**, Professor, department of Electrical Engineering.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

06/06/2022

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This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

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Date: **06-06-2022**

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DEDICATION

To my Parents, Niksa & my Supervisor

Abstract

Silicon photonics is a promising platform which provides the highly scalable, low-cost on-chip photonic devices. Ideally, photonics miniaturization is limited due to the diffraction limit, which has been conveyed through the development of novel guiding of mechanisms. In a metal-dielectric interface, light can be coupled with collective oscillations of free electrons at nanoscales that exceed the limit of diffraction. Such waveguides with surface plasmon polariton (SPP) modes abide from excessive metal losses, so its practically they are limited.

In a plasmonic waveguide for nanoscale devices, leaky mode confinement in a high refractive index layer beneath the Hybrid Plasmonic boundary layer can reduce further losses and control propagation Properties. Optical signals can be electrically controlled due to the large light-matter interaction. Recent advances in the field of Nano-photonics have become more capable of controlling the structure and properties of devices with high levels of precision. FinFET Structure is proposed as a nanophotonic platform to guide and control light. The hybrid plasmonic mode is made to guide in the dielectric layer around the silicon fin (channel). We are able to guide and control both TE and TM modes in the proposed structure which provides improved electrostatic control over the channel where the gate is wrapped around the Fin. The hybrid plasmonic mode is controlled through modulation of charge carriers' conductivity in the channel by varying the gate voltage. By utilizing the gate and drain-source voltages we can control the charge carriers in the channel thereby realizing phase tuning. In addition, a voltage tunable absorption is also reported through the voltage variable imaginary part of the effective refractive index. The proposed device can be well suited for applications in photonic devices at real nanoscales. The proposed concept can pave the way to build other nano-scale functions like optical modulator, optical switch, optical filter, polarization converter etc. Photonic devices are quickly gaining traction as a way to fulfill bandwidth demands in communication networks and high-performance computing

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NOMENCLATURE

ε	Dielectric Constant
λ	Wavelength
η	Refractive Index
η_{eff}	Effective Refractive Index
$\emptyset$	Phase of the electro-magnetic wave
q	Electronic Charge
α	Attenuation Coefficient
β	Phase Constant
ω	Angular Frequency
c	Speed of light
k	Wavenumber
hv	Photon Energy
μ_e	Electron Mobility
L_π	Phase shifter length
Ec	Conduction Band Energy
Ev	Valance Band Energy
n_e	Electron Density

ACRONYMS

CMOS	Complimentary metal oxide semiconductor
MIM	Metal Insulator Metal
MIS	Metal Insulator Semiconductor
SPP	Surface Plasmon Polariton
PIC	Photonic Integrated Circuit
SOI	Silicon on Insulator
I-V	Current-Voltage
Au	Gold
Si	Silicon
SiO_2	Silicon Dioxide
MOSFET	Metal-Oxide Field Effect Transistor
TFET	Tunneling Field Effect Transistor
FinFET	Fin Field Effect Transistor
HPW	Hybrid Plasmonic Waveguide
FDE	Finite Difference Eigenmode (FDE) solver

Chapter 1

Introduction to Integrated Photonics

An integrated photonics is a emerging branch of photonics that fabricates devices and waveguides as a integrated structure that are embedded on the surface of a flat substrate. The integration of complex photonic circuits allows for the processing and transmission of light in similar to how electronic integrated circuits handle and transmit electronic signals. In this chapter we examine the fundamental limitations of electronic structures and the advancements in integrated photonics to enhance the computational capabilities of the system. In addition, we discuss the guiding mechanisms of the light signal in multiple silicon-based optical structures and the significance of optical modulation in photonic electronic integrated circuits.

1.1 Background and Motivation:

In a modern electronic system, large number transistors are being incorporated into a single chip in order to enhance more computational power. One of the top research topics of recent years has been progress towards finding the smallest features size on the chip [1], [2]. In this regard, VLSI industries are continuously looking forward to the lower technology node. A dense integrated circuit has greatly improved the performance of electronic chips. With highly dense CMOS circuitry, however, it is more challenging to increase the computational capabilities, especially when the feature size is less than 100 nm [3] - [5]. This occurs because of two major factors: the power dissipation and the Bandwidth thus it becomes difficult to achieve high performance integrated circuits [6]. Additionally, CMOS fabrication platforms are well-developed with a lot of market penetration due to their cost-effectiveness and large-scale production capabilities. With each advanced technology node, leakage power in the chip increases rapidly compared to the active power [7] as shown in Fig. 1.1. The real motivation behind this work is to overcome the issue of Bandwidth and

power dissipation on the same CMOS compatible fabrication platform. It can be done with the use of photonics.

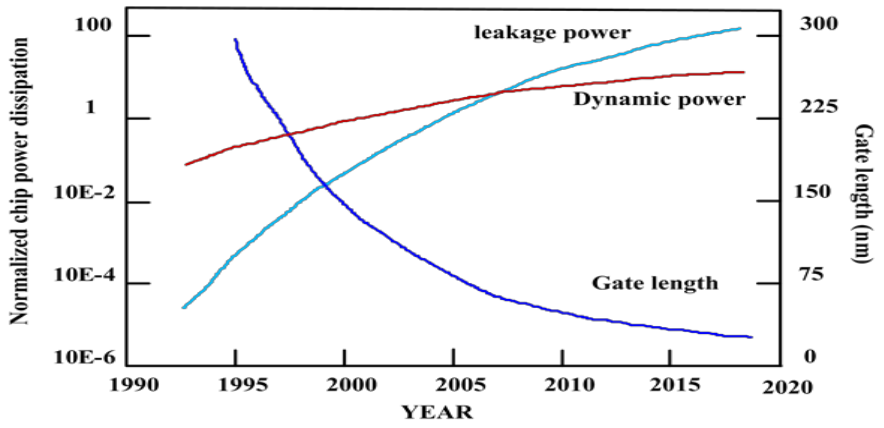

Figure 1.1 International Technology Roadmap for Semiconductor (ITRS) based static and dynamic power dissipation trends in chip [2].

Photonics is the science and technology; the generation and control of photons are studied with an electronic medium [8] - [10]. Photon-based devices have inherently high bandwidth due to the high-frequency range of light (in THz). High-performance applications enabled by this technology are being used in a variety of places, such as telecommunication, aerospace, and environmental monitoring [11].

1.1.1. Silicon Photonics:

The evolution of photonic-based devices has resulted in a wide range of materials in realization of multiple aspects of technology. In contrast, most of these materials are incompatible with CMOS technology, which makes it highly difficult to integrate devices made from them on highly dense integrated circuits [12]. Silica was able to induce low optical loss with wavelengths near 850 nm, 1310 nm, and 1550 nm, leading to the concept of silicon photonics. It opens the opportunity to utilize the same material in the optical regime [13], [14]. Fig. 1.2 shows the loss spectra of the silica fiber, the main cause of optical losses is Rayleigh scattering, absorption through various metallic impurities, tiny water droplets in the fiber, and silica molecule itself. Rayleigh scattering losses are minimum for longer wavelength since they decrease with free-space wavelength ($1/\lambda^4$) [15].

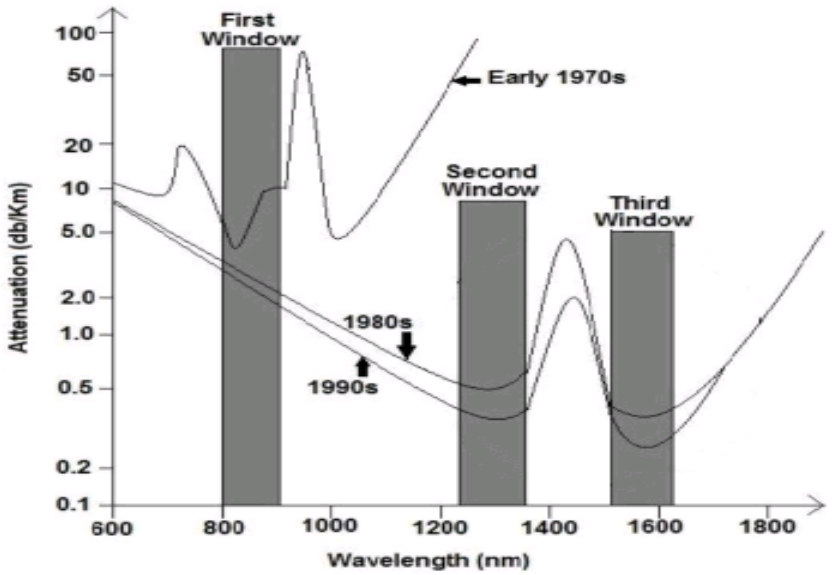

Figure 1.2 Transmission Spectra of early 1970s, 1980s, 1990s silica fibers. Three low-loss communication windows are shaded [8].

Additionally, improved fabrication technology for silica fibers governs a drastic reduction in transmission losses when compared to silica fibers used earlier. In spite of the zero-group velocity dispersion at 1310 nm, 1550 nm is the wavelength considered to be the telecommunication window [15]. The invention of components such as EDFA has given this window an edge and given it an edge in 1530-1610 nm, so 1550 nm is believed to be acknowledged as a telecommunication window worldwide [16]. By enhancing transmission speed through an optical domain, silicon photonics can complement existing microelectronics by improving the transmission speed currently limited by electrical traces (heat generation) [17]. In light of the vastly improved bandwidth and reduced power dissipation of photonic devices, any optical solution must be cost-efficient for mass production. In this regard, silicon photonics has been a hot topic in both scholastics and industry. Si photonics, named by Soref, in the earlier to the mid-1980s, and began trading by the Bookham Technology Limited [18]. In 1989 Si is the moment most (after O_2) inexhaustible component on the earth [19]. With a straight forward cubic and the crystal structure, Si can be utilized to create wafers with purity without any defects. Due to Si

hardness, high thermal carriers, and low density, semiconductor gadgets are remarkably useful [20] - [25]. At 1550 nm, Si has a refractive index of 3.476, which is a low-loss optical communication window, and it is transparent over 1100 nm. Furthermore, silicon's high-quality oxide, SiO_2, has a unique optical property, which makes it ideal as a natural substrate for silicon waveguide cladding [26], [27]. With its moderately low refractive index (nSiO2=1.35 at 1550 nm) and its optical transparency, this oxide might make a great silicon waveguide cladding. A large index difference between Si and SiO2 furthermore enables a strong optical intensity within silicon waveguides, which resolves nonlinear effects [28].

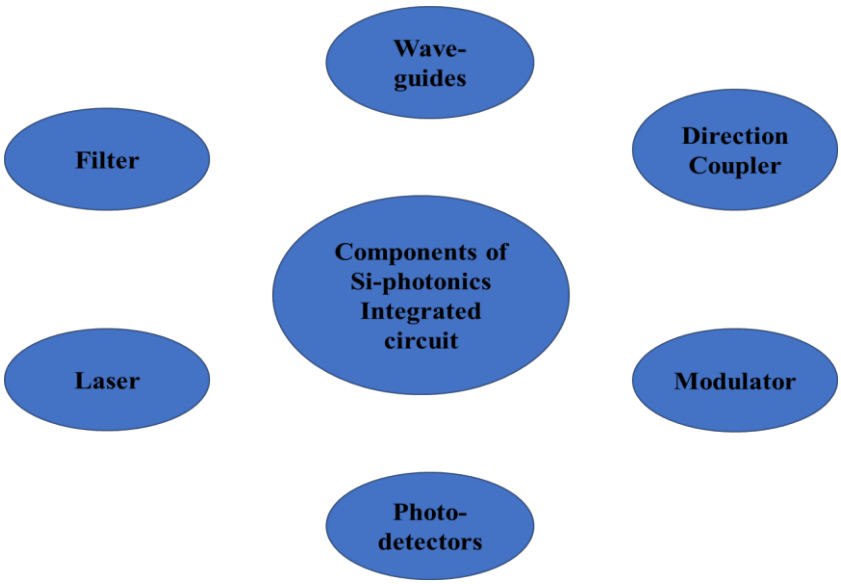

Figure 1.3 Main components of Silicon integrated photonic circuits.

Figure 1.3 depicts the main components of the Si photonic integrated circuit. Due to the advantages of silicon, many fundamental optical devices, including waveguides, filters, modulators, photodetectors, Direction Coupler, Optical Filter, and lasers, can be realized on the silicon photonics integration platform [29]. Using this prototype, the optical and electronic components can be integrated seamlessly into a chip to provide dynamic system-level optical functions, and these components can be

produced and packaged using a single CMOS process [30],[31]. These Si-based optoelectronic integrated circuits have considerable potential for future low-cost and high-volume tera-scale data transmission.

1.2 Nanophotonic Optical Guiding Structures:

A novel contactless technology that uses nanometric particles to make contact and interact with one another is known as nano-photonics. As a result of novel optical phenomena and functions, nano-photonics gives a crucial part in the development of fabrication technologies as well as qualitative advances in photonic systems and devices. In recent decades, photonic crystals, plasmonics, quantum dots, Si photonics, and meta structures have been increasingly well known. But they are based on waves that are diffraction-limited.

1.2.1. Photonics Crystals:

Optical nanostructures arranged in a periodical arrangement that allow or prevent a specific frequency band are called photonic crystals. Yablonovich [32] and John [33] proposed a one-dimensional period structure which is an optical analogy to semiconductor bands. Authors in 1997 proposed the concept of photonic crystal in which the atoms in a material are arranged in such a way that they allow or prohibit certain frequencies. The photonic crystal can be one, two, or three-dimensional, as shown in Figure 1.4, depending upon the direction of periodicity.

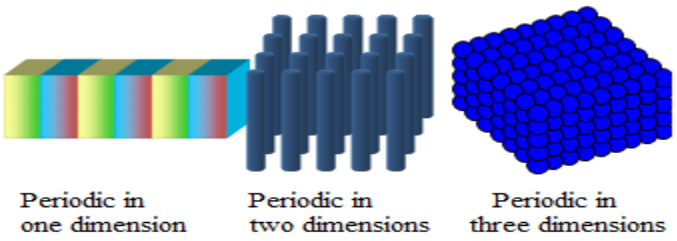

Figure 1.4 Photonic crystal for nanophotonic waveguiding and optical applications [32].

Photonic structures confine a high intensity field within the nanostructured structure, and have a unique-properties which have been demonstrated to be useful in applications such as biosensing and optical modulation. Periodicity in the waveguide slows down the light to a large degree, and these devices are useful in memory devices and optical delay lines. In spite of their difficulty in fabrication, these devices have been used for delay lines, optical memory, optical interconnects, optical data manipulation, bio-sensing using light etc.

1.2.2 Photonic Crystal Slabs:

The figure 1.5 shows the photonic crystal slabs consist of 2 Dimensionally periodic index contrasts that are usually used as guiding layers in high-index semiconductor devices [34]. At wavelength scale, the guided modes cannot be controlled by external radiation since they are totally confined by the slab. This means that the structures supporting in plane line guided modes are totally confined by the slab [35]. By using a slab structure as a substrate, huge-scale circuits, on-chip components, and photonic components can all be integrated. It is also feasible for photonic crystal slabs to interact with external radiation using in-plane waveguide.

(a) (b)

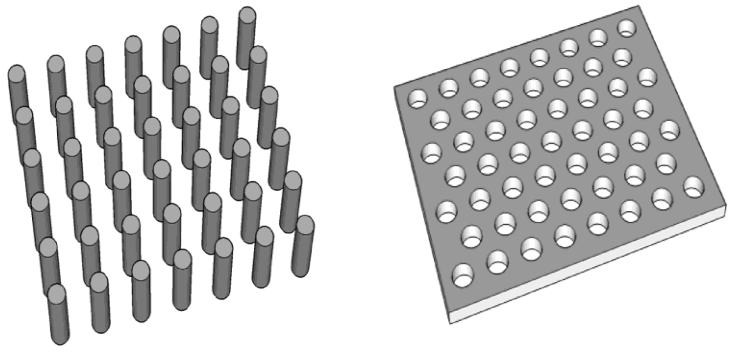

Figure 1.5 2-D periodicity and index-guiding Photonic-crystal slabs (a) A square grid of dielectric plains in air of the rod slab (b) A triangular grid of air space in a dielectric of the hole slab [35].

Like the guided mode, guided resonances take place in the structures, and electromagnetic power which is strongly confined inside the slab is combined with external radiation by using the guided resonances [36]. Light can be transported from inside the slab to the outside environment through guided resonances because, contrary to the guided mode, the resonance can be coupled to external radiation. A photonic crystal slab can be used to implement number of photonic applications, including band pass filters, super prism effects, waveguides and cavities, communication, biosensors, light extraction from light emitting diodes (LEDs), spontaneous emission control and sensors [37].

1.2 Types of Plasmonic Waveguides:

The optical circuit consists of an optical waveguide that allows light propagation over a variety of separations, from a few meters to thousands of kilometers for fiber optic transmission, thus enabling low-loss transmission of various components and gadgets. As optical waveguides are resistant to electromagnetic interference, actuated crosstalk, and offset diffraction, they are indispensable for computing applications and communication [38]. The geometry, mode structure, index distribution, and materials of optical waveguides are all used to classify them. Multiple total internal reflections from the surfaces of the high index material positioned parallel to the optical route of propagation are used to create the optical waveguides. The important group of optical waveguides include ridge waveguide, rib waveguide, slot waveguide, MIM, IMI, Dielectric loaded plasmonic waveguide, V-groove MIM [39].

The optical wave propagating in the of a rect waveguide structure can be analyzed according to the scalar wave of equation given as

$$\frac{\delta^2 E}{\delta x^2} + \frac{\delta^2 E}{\delta y^2} + [K_o^2 n^2(x,y) - \beta^2]\, E \qquad (1.1)$$

Where the total number of optical modes are related to V number as

$$V = \frac{2\pi a}{\lambda}\sqrt{n_{core}^2 - n_{clad}^2} \qquad (1.2)$$

Where λ is the wavelength, n_{clad} and n_{core} represent the refractive index of cladding and core r, a is waveguide core dimension, and β is the optical wave's phase constant.

Ridge Waveguide:

The three-dimensional schematic representation of the Si photonic ridge waveguide is shown in Fig. 1.6 (a), The ridge waveguides has a Si core with cladding made of SiO_2. The waveguide must only accommodate a single mode in order to manufacture useful devices [40]. The dimensions of the waveguide's core play an essential role in achieving fundamental TE and TM modes. When an optical mode's eff. refractive index (η_{eff}) is larger than the cladding but less than the core index, the mode will only propagate in the waveguide's and will not leak out [41]. The optical mode confinement in the core region will be stronger as the effective refractive index increases.

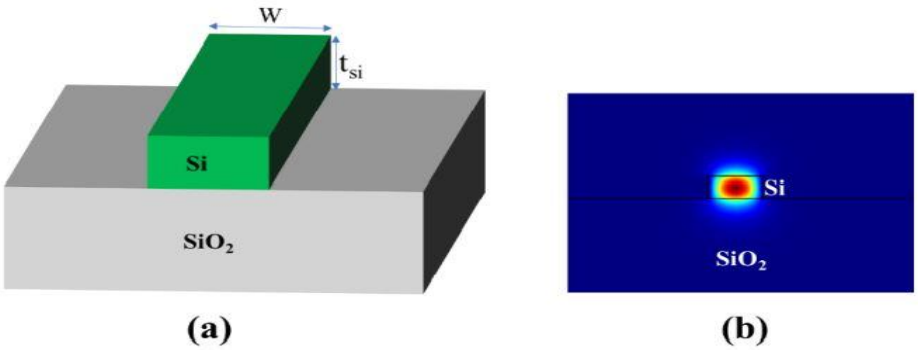

Figure 1.6 (a) Schematic view of Ridge waveguide, w=450nm, t_{Si} = 220 nm on top of 2 μm thick SiO_2. (b) E.F distribution of the TE mode in core of Si waveguide [13].

It should be noted that the phase velocity (V_p) of each mode is determined by the value of neff ($V_p=c/\eta_{eff}$), therefore all modes in the waveguide travel at different velocities [42]. Another factor to consider is mode confinement in the core region; as previously stated, the mode with the highest η_{eff} value will have the strongest confinement in the waveguide. The n_{eff} of higher-order modes weakens, and the mode begins to leak out of the core region. This phenomenon is significant for a vast area of applications such as sensing, modulation, absorption and so on [43].

Slot Waveguide:

Slot waveguides can be created with the optimum structural geometry shown in Fig. 1.7 (a) so that the optical mode carrying a very high electric field intensity is restricted to the low-index region, also known as the slot region [44]. The electrical boundary condition of the electrical signal at the interface of the low index and high index regions can be easily comprehended.

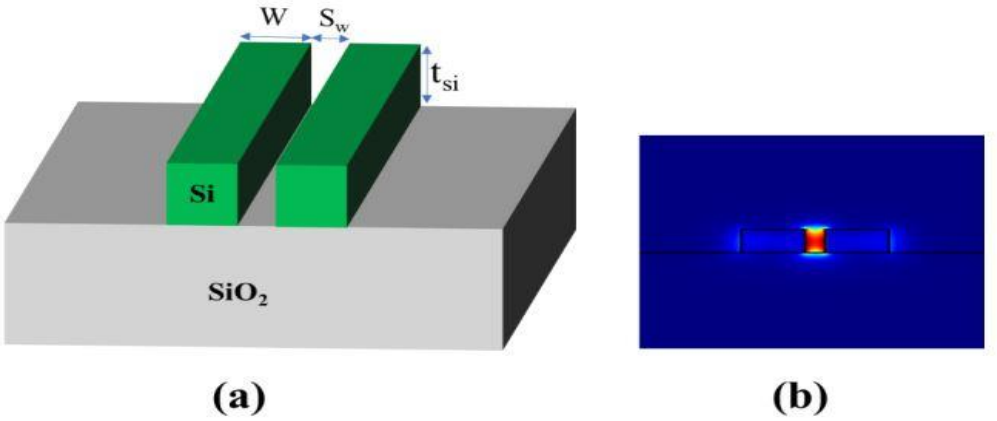

Figure 1.7(a) Schematic view of slot waveguide, w=300 nm, t_{Si} = 220 nm, S_w = 100 nm on top of 2 µm thick SiO2. (b) Electric field distribution of quasi TE mode in slot area region [44].

The tangential component of the E.F can be given as

$$E_{t_1} = E_{t_2} \tag{1.3}$$

Similarly, Normal component of E.F can be written as

$$D_{n_1} - D_{n_2} = \rho_s \tag{1.4}$$

$D_{n_1} - D_{n_2} = 0$ for dielectric material (σ=0)

$$\mathcal{E}_1 E_{n_1} = \mathcal{E}_2 E_{n_2} \tag{1.5}$$

Thus, for our case where $\in_1$ and $\in_2$ are the permittivity of silicon and slot region respectively.

$$E_{n_1} = \frac{\mathcal{E}_2}{\mathcal{E}_1} E_{n_2} = \frac{n_{Si}^2}{n_{Slot}^2} E_{n_2} \tag{1.6}$$

High discontinuity at the boundary creates a high electric field in the slot region, which is directly proportional to the rectangular of the refractive indices' ratio of the high-index material to the low-index material, as shown in Eq. 1.6. The maximum confinement of the optical signal in the slot region can be achieved when the width of the slot area region is equal to the decaying component of the electric field across the slot region, whereas this effect is minimal for the quasi-TM mode because the magnetic boundary is continuous at the boundary [45]. A slot waveguide's main benefit is a very strong E.F in the slot region, which is useful in a variety of applications such as nonlinear optics and sensing. Another advantage of slot structure over ridge waveguide is the high phase velocity of optical mode (owing to low n_{eff}) for high bandwidth applications in travelling wave-based modulators.

Various configuration of plasmonic waveguide:

Plasmonic waveguide usually suffers from large ohmic losses. Researchers devised many techniques to address this, including MIM metal-insulator-metal, V grove MIM, MIS metal insulator semiconductor, IMI, and others, as shown in Figure 1.8. At NIR wavelengths, the noble metals Au, Ag, and Cu have demonstrated a significant low loss [46]. This system has a direct relationship between material property and incident light, making it easier to control and alter. Because of these features, plasmonic waveguides are a better possibility for on-chip nanophotonic devices in optical modulation and photodetection.

The plasmonic waveguide's large light-matter interaction also makes it suitable for sensing applications [47]. In 2007, researchers presented a hybrid device that compensates for plasmonic losses by linking the optical and plasmonic modes, resulting in a hybrid plasmonic mode, to overcome various losses in the plasmonic waveguide which is covered in the next sections of this chapter.

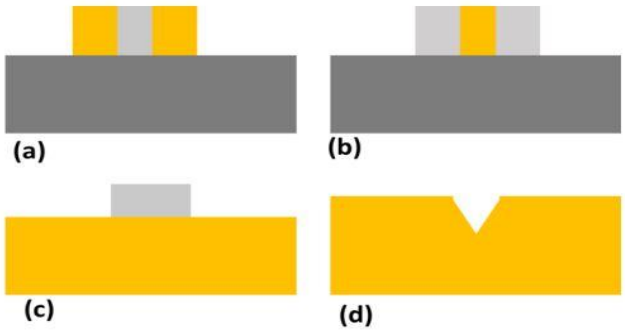

Fig 1.8 Different configuration of the plasmonic waveguides are (a) MIM (b) IMI (c) dielectric-loaded plasmonic waveguide (d) V grove MIM [47]

1.2.4 Surface Plasma Polariton:

When light interacts significantly with a dielectric media, the resulting wave can frequently be considered a coupled mode forming from the interaction of light with the medium's normal modes to a decent approximation. [Hopfield 1965, Kittel 1993] The word 'polariton' was first used to characterize the quantized states of such excitations [48]. The wave number grows as the resonance frequency approaches, and propagation slows. Away from the band gap, the wave is predominantly "Photon-like," with light-like velocity and wavelength. Electromagnetic waves can link to spin waves in ferromagnetic materials, excitons in semiconductors, phonons in crystals, or electrons in metals, producing magnon, exciton, phonon, and plasmon polaritons, respectively [49]. Surface plasmon polariton (SP) is a form of surface wave that can exist at a metal-dielectric contact interference. The concept of SP is depicted in Figure 1.9. It depicts a metal-dielectric interface, with the material filling the space for y > 0 having permittivity 1 and the material filling the area for y 0 having permittivity 2. The transverse magnetic TM mode of SP

propagating in the x direction is also depicted in Fig. 1.9. he SP mode supported by such an interface is TM in nature, The electric field profile and surface charge distribution of Surface plasmonic propagates in the direction of x-axis are shown in Fig. 1.9 [50].

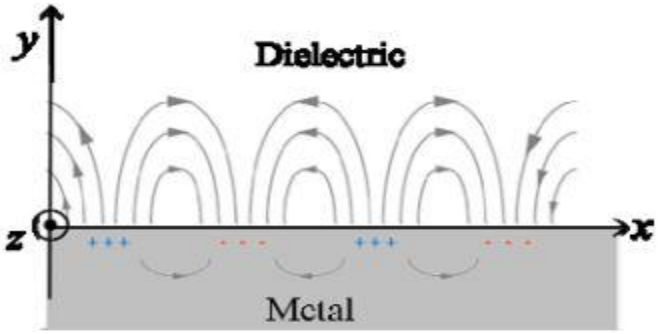

Fig. 1.9. Single metal-dielectric interface and field profile of SP mode [50]

The expression for the dispersion relation of the SP mode for the metal-dielectric interface shown in Fig. 1.9 is

$$\beta = K_o \sqrt{\frac{\varepsilon_1 \varepsilon_2}{\varepsilon_1 + \varepsilon_2}} \tag{1.7}$$

Here β is the propagation constant in the x direction and the free space wave number is given by $k0=2\pi/\lambda_0$; λ_0 is wavelength in free space. The permittivity of a lossless metal in the optical regime can be expressed by the Drude model [Maier 2007].

$$\varepsilon_2 = 1 - \frac{\omega_p^2}{\omega^2} \tag{1.8}$$

Here ω_p is the plasma frequency of the gold and ω is the angular freq of light. Substituting the expression of (1.7) for ε_2 in (1.8), we get the dispersion relation of SP supported by a lossless Drude metal-dielectric interface.

$$\beta = K_o \sqrt{\frac{\varepsilon_1 \left(1 - \frac{\omega_p^2}{\omega^2}\right)}{\varepsilon_1 + \left(1 - \frac{\omega_p^2}{\omega^2}\right)}} \tag{1.9}$$

Due to the metal's complex permittivity at optical wavelength, the propagation losses in the surface plasma polaritons became quite challenging and the corresponding losses affect the optical mode confinement [51]. Dielectric waveguides are lossless, but the confinement of mode size is limited to the diffraction limit whereas SPP waveguides can guide the light far less than the diffraction limit but there is a huge propagation loss.

1.3 Hybrid Plasmonic Waveguide:

Large losses in the plasmonic waveguide can be overcome by linking the guided SPP with the leaky optical mode, resulting in a hybrid plasmonic waveguide. A HPWG is a combination of two waveguides - dielectric and plasmonic [52]-[54]. In order to allow leaky modes to travel through the high index layer coupled to plasmonic waveguides, the waveguides are stacked with high index layers. Fig 1.10. depicts the typical configuration for the HPWG, which is a layer of low index semiconductor between a metal layer and a high index semiconductor layer.

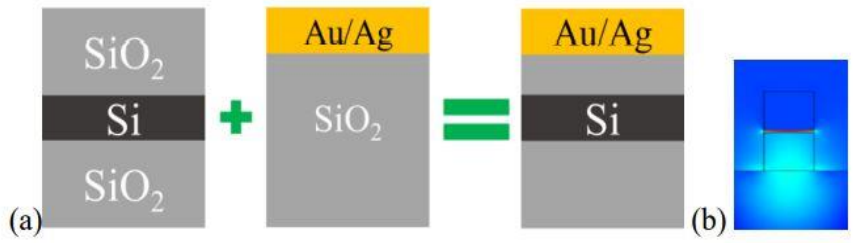

Figure 1.10. (a) Hybridization of Si photonics waveguide and plasmonic waveguide resulting in the hybrid plasmonic waveguide. For the wavelength 1550-nm the Au and Ag are the best choices of metal (b) Maximum intensity of the Mode profile of hybrid plasmonic mode in the dielectric layer [53].

It also provides the benefit of low-loss propagation of the signal in the waveguide and high confinement in nano-low index materials [54]. Because of these advantages, the hybrid plasmonic configuration has attracted the attention of researchers and scientists in the field of integrated photonics [55]-[57]. Plasmonic waveguides have also been found to have coupling problems with light from the source in the waveguide to the HPW. This problem has also been solved in many configurations of this type of hybrid plasmonic waveguide [58]. The high light-matter interaction also facilitates the use of this waveguide for optical modulation through the external electric field.

1.3.1 Introduction to Hybrid Plasmonic Waveguide:

By combining optical and plasmonic modes, a hybrid mode is produced. The waveguide has a low loss and high confinement of the electromagnetic field, as well as a small confinement area. This concept was introduced by M.Z. Alam et.al. [37] at a conference in 2007. In 2008, R. F. et.al Oulton published a detailed analysis of it in Nature Photonics where they have taken a cylindrical layer of high index material, divided from the metal layer by a gap filled with a low index insulator material [41]. The high index layer should might be small enough that it allows only leaky optical modes to pass through when the gap between it and the metal is reduced significantly enough. They also demonstrated that when the high index layer is small enough, an electromagnetic field forms between the two [42].

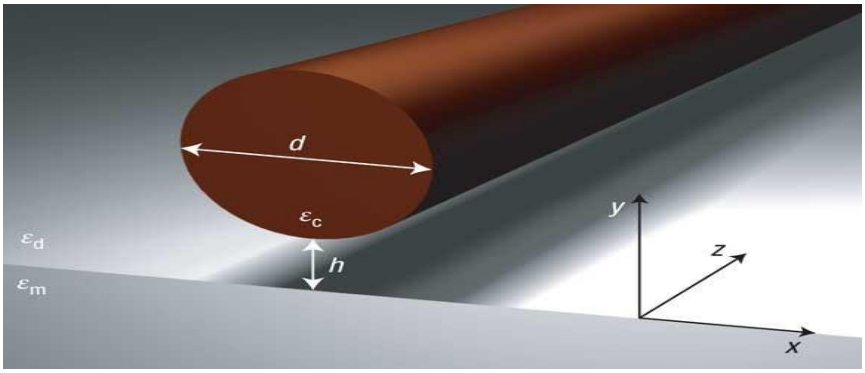

Figure 1.11 Schematic view of the introduced concept of HPWG [5]

Moreover, they demonstrated that the high index layer should be small enough to permit only leaky optical modes to pass through it. Since this concept has improved upon the major drawbacks of the plasmonic waveguide while maintaining the nano-dimensional confinement of the field, researchers have begun appreciating its applications in on-chip devices [45], [47]. The mode factor is a metric of quality of the hybrid mode, describing how much SPP and optical energy couples with one another. Equation (8) provides the mode factor, which is the marginal quality of hybrid mode.

$$| a(d,h) |^2 \frac{n_{hyb}(d,h)-n_{spp}}{(n_{hyb}(d,h)-n_{cyl}(d))+(n_{hyb}(d,h)-n_{spp})} \tag{1.10}$$

|a| is the mode factor for hybrid plasmonic waveguide n_{hyb}, n_{spp} and n_{cyl} are the eff. refractive index of the hybrid of the mode, metal-insulator plasmonic mode and optical mode respectively.

$$A = \frac{1}{\max\{W(r)\}} \int W(r) dA \tag{1.11}$$

A mode of plasmonics has the following characteristics: effective mode area is determined by equation (11), and its area is proportional to its maximum energy density. W(r) is the energy carrier density per unit length of a mode, and the true figure of merit is determined by the length of the mode and the confinement strength, The FOM is defined by equation (1.11).

$$FOM = \frac{L}{\sqrt{A_{eff}}} \tag{1.12}$$

1.3.2 Electrical control of optical signal in hybrid plasmonic waveguide:

Using light to control electrically at nanoscale is still an essential element for on-chip optical devices [48]. The optical switch and the electro-optical

modulator constitute the main components of any photonic integrated circuit. Silicon has very low transmission and low absorption, so modulating light is generally difficult in silicon-based electro-optic modulators. While increasing the length of silicon-based modulators can increase modulation, the device size will not be suitable for on-chip devices, micro-ring resonators, MZI, and silicon hybrid material-based modulators can be used as possible solutions for reducing the modulator size [59]. These schemes have the disadvantages of low fabrication tolerance, working in a narrow bandwidth of operation, and being temperature sensitive. In order to fix this problem, plasmonic waveguides are an attractive solution comparing the advantages of plasmonics and silicon, which is various optical modulators and switches are designed based on hybrid waveguides. A hybrid plasmonic waveguide-based modulator is experimentally demonstrated by Sorger et. al. [60]. They have demonstrated phase and intensity modulation by plasma dispersion effect and by varying the refractive index of the layered ITO. When the E.F is applied to the top metal, an accumulation of charges form in the silicon layer. The modulators under this type of technology exhibit a substantial depth of field. Being that the materials change over time, the modulation speed is very slow [61].

1.4 Electro Optical Modulators:

Researchers have been exploring electro-optical modulation in different materials and structures for electrical control of optical properties. In this section, electro-optic modulation based on various physical effects like Pockels and Kerr effects, Franz Keldysh effect, Quantum Confined Stark Effect.

1.4.1 Pockels and Kerr effects:

Any material in which E.F is applied undergoes a variation in its refractive index. The Pockels effect occurs when the variation is relative to the static E.F and the Kerr effect occurs when the change is quadratic [31]. The alteration in the refractive index as a work of the applied static electric field is given by:

$$\Delta\eta = -r_{33}n_{33}\frac{E_3}{2} \tag{1.13}$$

where n_{33} is the refractive index in the regulation of the applied E.F and E_3 is the applied E.F.

As a purpose of the quadratic electric field, the refractive index changes is given by

$$\Delta\eta = s_{33}n_0\frac{E^2}{2} \tag{1.14}$$

where E is the applied E.F, n_0 is the unperturbed refractive index, and s_{33} is the Kerr coefficient. Pockels effect shows good effect on materials of Indium Phosphide, Gallium Arsenide, and Lithium Niobate whereas Kerr effect can measure the Si, but it is powerless [33].

1.4.1 Franz-Keldysh Effect:

When a static E.F is not applied to the bulk material, the Franz Keldysh effect changes the optical absorption of the different materialS for wavelengths near its direct energy band gap (e.g., Si or Ge) [35]. With no static E.F applied into the material, the conduction band would be as shown in Figure 1.12(a).

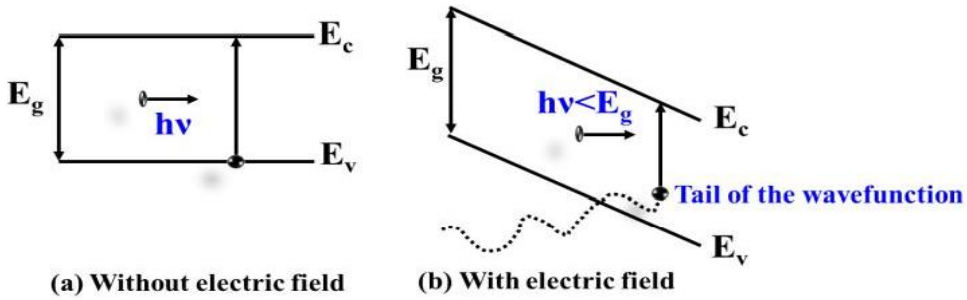

Figure 1.12 FKE Energy diagraM. In (a) there is no applied static E.F (b) a static E.F is applied [6].

As shown in Figure 1.12(a), at this point an electron can be moved from the VB to CB when the energy of a photon exceeds Eg (energy bandgap). When an E.F

is applied into the material, both the VB and CB is shifted as shown in Figure 1.12(b). This may occurs for electrons in the valence band (crystalline shell) that tunnel into the forbidden conduction band (colloid shell) [36],[37]. Since the electrons cannot tunnel through this process, a photon with smaller energy than the band gap of the element Eg can vitality an electron and can be excited from VB to the CB, which causes light to be absorbed [38]. As a result, this improves the optical absorption of the substance beneath the energy bandgap Eg.

1.4.3 Quantum-confined Stark Effect:

When a static E.F is applied to a s.c, the QCSE changes its absorption properties of materials near the bandgap. This effect happens in quantum wells [39]. In the no apperance of a static E.F, the wave-function for holes and electrons is symmetrical when the quantum well is at equilibrium [40].

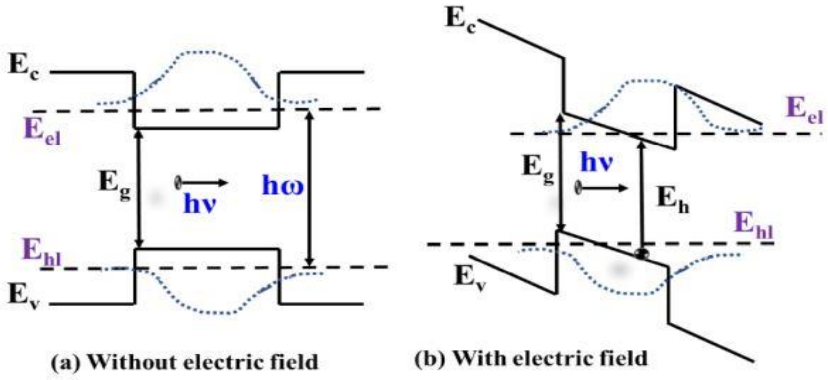

Figure 1.13 Energy diagram of the Quantum confined stark effect. (a) No E.F applied (b) an E.F is applied [8].

Electric fields tilt the energy bands when it is perpendicular to the quantum well, as illustrated in Figure 1.13.b Furthermore, due to the quantum mode confinement holes and electrons are related to the forces of the coloumb and form excitiment of the holes and electrons [27]. The energy is given by:

$$h_w = E_g + E_{el} - E_{hl} - E_{ex} \qquad (1.15)$$

E_g is the energy of the material with the bandgap, E_{ex} is energy binding of the exciton, E_{el} is the electrons and E_{hl} is the holes energy of sub-band. As a result, the electric field pushes hole and electron wave functions to the edges of the quantum dot well, reducing the overlap the integral between their wave functions in conduction band and valence band [41]. Thus, the energy bandgap and recombination efficiency are reduced. Therefore, the band-edge of the absorption spectrum is more susceptible to absorption.

1.5 Electronics- photonics convergence:

Due to inherent limitations in the platforms available, electronic and photonic devices have been challenging to integrate on a single basic platform for a long-lasting time. While the Si platform is capable of producing high performance electronic structure devices, photonic functions are restricted by the lack of active photonic structures [48]. The III-V platform, on the other side, cannot integrate electronic devices at high density while supporting active photonic structures. Since the beginning of the last decade, intensive research has led to the possibility of integrating electronics and photonics convergence. Two separate ways have been followed for the integral combination. In one process, III-V materials are either grown directly on silicon to produce active photonics structural devices or are combined in a hybrid approach [49].

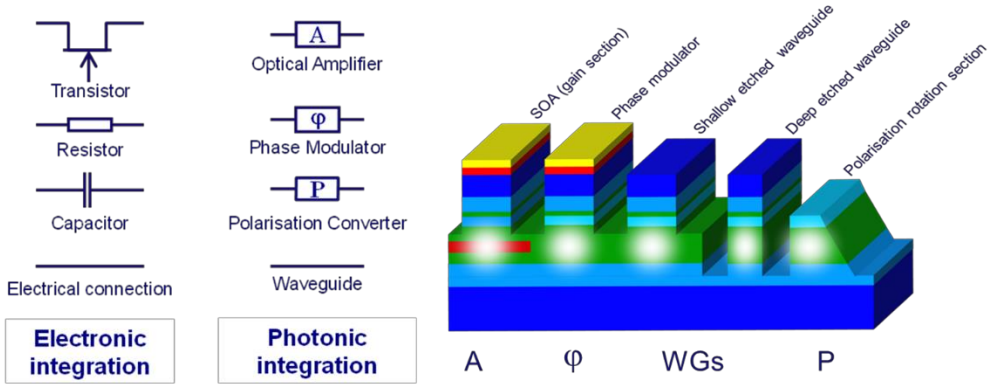

Figure 1.13 Electronics and photonics convergence [16]

The other approach involves fabricating both passive and active photonics structural by using silicon CMOS compatible materials within an IC process flow using mask levels. In general, "CMOS integration" is used to describe a process followed by photonic devices which, in general, uses materials and processes typically found in CMOS [50]. The most common limitations in the fabrication of photonic devices involve the thermal budgets and thickness of material layers determined by the design of planarization and the interconnection schemes. In contrast to PIN diodes with isolation trenches, the MOSFET configuration has the advantage of negligible dc power consumption as well as the ability to localize refractive index change under the gate electrode. However, due to continuous scaling of MOSFET, several challenges like it short channel effects (SCE) arise, which results in the leakage of current in the device, reduction of subthreshold swing, and increase in OFF current [51]. To overcome this problem and reduce these effects, FinFET was proposed which offers better control over SCE and good gate control over the channel (Fin) which gives better results in optical phase modulation and absorption. Over time, as signal speeds and transmission capacities increase, electrical interconnections are replaced with optical interconnections, and light flows from the rack to the board and even into it [52]. In order to develop photonics-electronics converged devices, power consumption can be reduced, cost can be reduced, and density of carrier can be increased [53].

1.6 Organization of the Thesis:

The thesis is organized into five chapters starting with an introduction to integrated photonics, literature review of past work and problem formulation, theory of research followed by the chapter on original research work done and the final chapter on conclusion and the future scope.

Chapter 2. Literature Review: The second chapter consists of brief literature review of the dielectric, plasmonic, hybrid plasmonic waveguides and its applications and also a review on the significant contributions in optical modulation and absorption based on hybrid materials, which includes the many

current reported works. Followed by this, the chapter highlights the problem formulation.

Chapter 3. Integrated CMOS photonics: The chapter consists of the theoretical of the CMOS photonics technology which includes about the optical modulator, optical waveguide, photodetector which is described under the photonics technology. In this chapter we also described about the CMOS photonic layer integration which includes about the plasmonic dispersion effect. Finally, we also investigated theoretical analysis on the various type of CMOS photonic devices which includes various type of structure, in that we have described about the electrical analysis of the FinFET that it is a multi-gate transistor where the gate is wrapped around the Fin channel and also described about the optical properties of the FinFET structure.

Chapter 4. Guiding and controlling light at Nanoscale in FinFET: The chapter introduces the nanoscale optical guidance of light in the FinFET structure and control it electrically at a wavelength of 1550 nm. Here the HPM is made to guide in a 10 nm dielectric thin layer, where the mode confinement exists in both TE and TM polarization. The variation in the complex effective refractive index is observed by varying the gate voltage in this structure. The Finite-Difference Eigenmode (FDE) using LUMERICAL software is used to analyze and design the device structure. The structure is used to create a plasma dispersion effect, which in turn modulates the light in nanoconfinement with a very small mode area. Efficient phase modulation and Absorption change are observed by varying the gate voltage.

Chapter 5. Summary and Future Scope: In this chapter, all the contributions are summarized, and the relevant future scope of the work is briefly discussed.

Chapter 2

Literature Review

2.1 Introduction:

There is a conflict between these two technologies, namely electronic and photonic devices/circuits, in relation to their size for large density integration. This chapter provides an overview of recent literature on dielectric, plasmonic, and hybrid waveguides and their applications in high density integration circuits or devices in section 2.2 followed by objectives and contribution and in the final on the Methodology.

2.2 Literature Review:

2.2.1 Review on the Hybrid plasmonic waveguide:

This concept was introduced by **M.Z. Alam et.al. [17]** at a conference in 2007. In 2008, R. F. et.al Oulton published a detailed analysis of it in Nature Photonics where they have taken a cylindrical layer of high index material, divided from the metal layer by a gap filled with a low index insulator material. The high index layer should be small enough that it allows only leaky optical modes to pass through when the gap between it and the metal is reduced significantly enough. They also demonstrated that when the high index layer is small enough, an electromagnetic field forms between the two. Moreover, they demonstrated that the high index layer should be small enough to permit only leaky optical modes to pass through it. Since this concept has improved upon the major drawbacks of the plasmonic waveguide while maintaining the nano-dimensional confinement of the field, researchers have begun appreciating its applications in on-chip devices. The mode factor is a metric of the quality of the hybrid of the mode, describing how much SPP and optical energy couples with one another. **P. Berini 2009 [18]** has presented the long-range surface plasmon polaritons (LRSPPs), which are the surface of the fundamental waves, propagate along with a thin metal stripe. The authors looked at a variety of optical qualities such as modal characteristics, field enhancement, and so on.

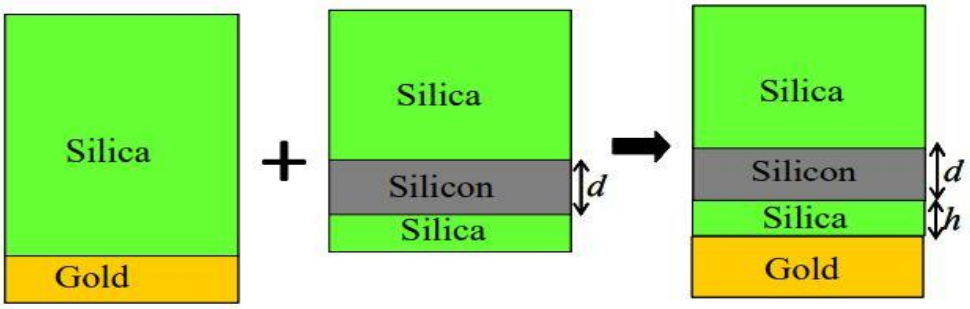

Figure 2.1 Formation of hybrid mode from coupling of dielectric and SP mode (a) Waveguide structure [17].

According to **Xiaodong Yang and colleagues [19]**, the optical force acting on a high index waveguide is stronger than that on a dielectric photonic waveguide due to the strong coupling between the two modes. Additionally, they showed an effective optical trapping force at the nanoscale on a single particle, which can be used for light manipulations and biosensing.

Yao Kou et al -2011 [20], introduced a HPWG with very large order of combined plasmonic modes of gold nano waves by integrating the photonic mode profiles of a silicon waveguidal dimension. When compared to typical dielectric modes, the generated HP modes have smaller mode areas and longer propagation lengths, resulting in a 90 percent efficiency.

2.2.2 Review on CMOS photonics devices:

In their novel MOSFET and Tunnel FET nanophotonic devices, **Lalit Singh et. al.2019 [21]** have included an optical waveguide based on hybrid plasmonic principles and an electrically modulated guided mode using the proposed MOSFET. According to the free carrier plasma dispersion effect, conductivity modulations in the FETs are employed in order to electrically modify the optical characteristics. An efficient modulation of phase is observed in the Hybrid Plasmonic mode and it is observed in the proposed devices. By varying the drain potential and source voltages in the channel, conductivity modulations of the channel are used to manipulate the guided light. At a wavelength of 1550 nm, an $\lambda^2/96$ quantum well transistor is shown to have a length of propagation

of 74µm and a very less mode area in the figure 2.2. These advantages can be used to compact optical devices with low loss.

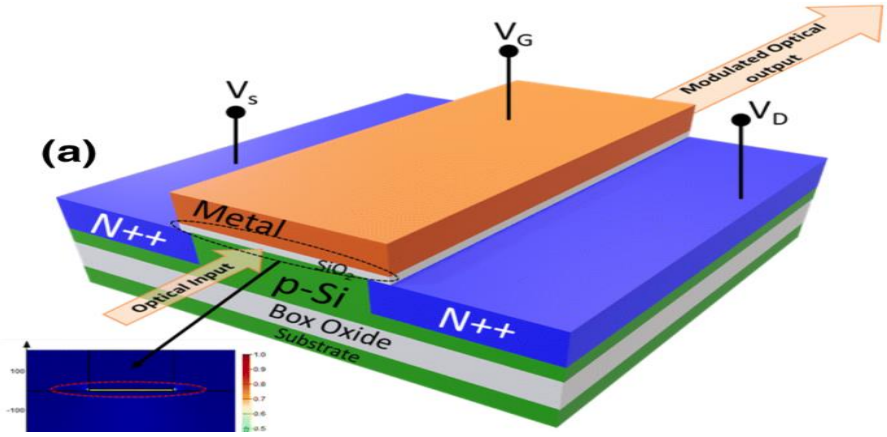

Figure 2.2 Schematic waveguide structure based on concept of HP using a MOSFET.

Optimal optimization of the device dimensions may further improve the efficiency of optical coupling. For illustration, improving the insulator thickness will lessees the losses of optical, but it will be consuming a larger amount of energy to achieve a larger shift in phase of the optical signal. Additionally, optimizing the horizontal dimensions will result in a more significant variation in the real of the eff. refractive index of the proposed structure.

D. Dai et al. 2009 [22] have proposed the double low index nano-slots based HPW structure. The theoretical study shows that the HPW guide has a small loss. It has been observed that the index nano-slots contains more power confinement for a smaller core width and hence, the power density in the nano region slots area is very high. This kind of analysis is essentially beneficial for the realization of PIC with ultra-high integration capabilities.

Debajit Bhattacharya et.al 2014 [23] they have proposed the impact of FinFETs from the structure to device level. FinFETs prove to be a better alternative to MOSFETs in today's scaled technologies since they have learned about their shortcomings in today's scaled technologies. In addition, they examined issues related to FinFET device characteristics, such as interconnect

lengths, insulator thickness, and fin height, along with other FinFET asymmetries.

2.2.2 Review on Optical modulators:

Liu et al. [24] demonstrated the first Silicon-based optical modulator, which used Mach Zehnder configuration for operating in large bandwidth areas across Ghz 62, mingbo et al. reported a data rate of >100 Gbit/s demonstrating compact footprint, low power consumption, high modulation efficiency, and power-efficient design all in a single device. As pure Si does not have linear electrical-optic effect, and quadratical of electrical-optical effect is poor at communication wavelength, Si-based optical modulators must have large area or, in other words, low modulating efficiency. The plasma dispersion effect is the most common modulation utilized in pure-Si; yet the devices are hampered by slow carrier diffusion times of nanoseconds and short carrier lifetimes of many hundreds and thousands picoseconds. This raised the need to investigate new alternative active materials.

A.P. Vasudev et.al-2013 [25] implemented an idea for a silicon waveguide modulator that controls the transmission of a waveguided plasmonic mode by electrically producing an epsilon-near-zero in barrier adjacent SiO_2 layer. This is accomplished by increasing mode overlap with the lossy area where free carrier absorption occurs while causing loss owing to free carrier plasmonic absorption in the SiO_2 layer.

G.R. Bhatt et al 2012 [26] was investigated the polarization sensitivity of the SOI waveguide device. He demonstrates surface plasmonic-induced at TM polarizer light is attenuated in the gold covered also investigated the extinction ratio of TE vs TM Using the concept of super-mode, Rahul Dev Mishra et.al formed a Si-based waveguide structure with very-low dispersion. It exhibits reasonably optical tunable properties activated by the plasma dispersion effect in Si. According to the proposed concept, there can be new fields of applications

for the FETs. In the study, FETs are used in integrated photonics in a novel way, which offers a broader range of application possibilities.

2.3 Research Objectives:

The below objectives are taken on the understanding gained from the initial study and literature review:

1. Optimization of mode confinement in FinFET device based on the hybrid plasmonic concept.
2. To analyze the effect of electrical characteristics and parameters like (V-I characteristics, charge carriers, bandwidth) on the proposed structure.
3. To introduce an efficient design of HPWG photonic structure with Improvement in mode characteristics, absorption and phase modulation.

2.4 Methodology:

1. Integrated CMOS photonic device based on hybrid plasmonic will be designed in the LUMERICAL software.
2. Optimization of HPWG Properties like different modal characteristics (mode area, propagation loss and eff. mode index) will be analyzed on FDE (Finite difference eigen mode solver) based on LUMERICAL software.
3. The effect of electrical parameters like (V-I characteristics, charge carriers, bandwidth) on the waveguide characteristics (optical power, Propagation length, mode area) will be done initially CHARGE solver then transported to FDE based on LUMERICAL software.

Chapter 3

Integrated CMOS Photonics

3.1 Introduction:

Recent efforts to integrate Si photonics and electronics (the EPIC, or photonic-electronic integrated circuit) are emblematic of a decades-long movement towards greater functional integration [63]. Analyzing the history of electronic systems-on-a-chip (SoC) that features memory, logic, and output-input drivers monolithically combined or integrated on a simple single chip can be instructive [64]. SoC integration, like EPIC integration, was driven by simpler physical interfaces, higher subsystem reliability, higher speed, reduced packaging costs, and lower power consumption.

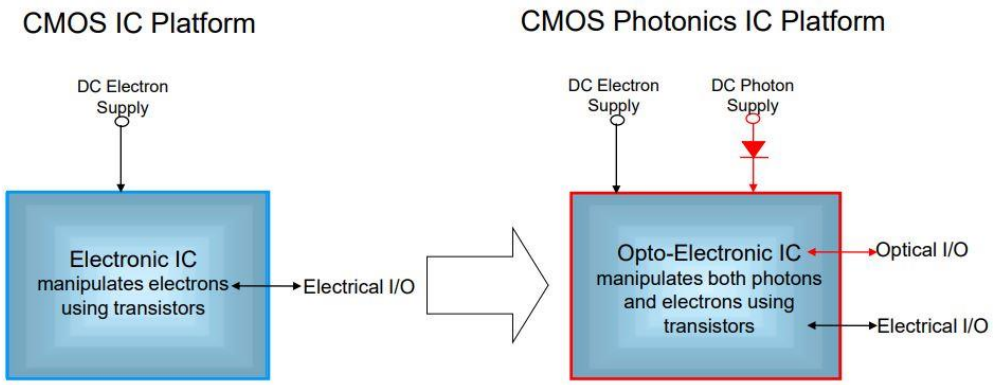

Figure 3.1 depicts the CMOS IC platform and CMOS photonics IC platform

The MOS Transistor controls the flow of electrons from source to drain by controlling the voltages at its terminals. Today, millions of MOS transistors can be placed on a single semiconductor chip but a modulator controls the flow of photons from source to drain by adjusting the voltages of the two arms. However, one important difference is that no photon can be stopped, so all unwanted ones go to drain. Many of these modulators can be stacked on a single chip. Luxtera [64] has built a platform using Freescale Semiconductor's standard CMOS (complementary metal oxide semiconductor) line to enable monolithic combination of photonic devices, such as grating couplers, detectors with electronic circuits, and modulators such as transimpedance amplifiers and modulator drivers.

3.2 CMOS Photonics Technology:

To build Integrated CMOS photonics, system designers need to have several basic building blocks at their disposal. Hence, the basic components of an CMOS photonics optical device consist of the following: optical modulator, optical waveguides, optical detectors, light sources and fiber coupling. It is clear that each of these components is capable of providing practical solutions in the near future, thus CMOS photonics is ready for use in mainstream applications [65].

3.2.1 Optical Modulator:

Optical waveguide is a device that changes or modulates the amplitude of an optical signal in a controlled manner. The plasma dispersion effect based on optical modulation in this paragraph. Since its full CMOS compatibility, the plasma dispersion effect has been investigated extensively over the past two decades. In 1987, Soref [66] and a colleague demonstrated that with an E.F applied, the refractive index and absorption coefficient of c-Si changes.

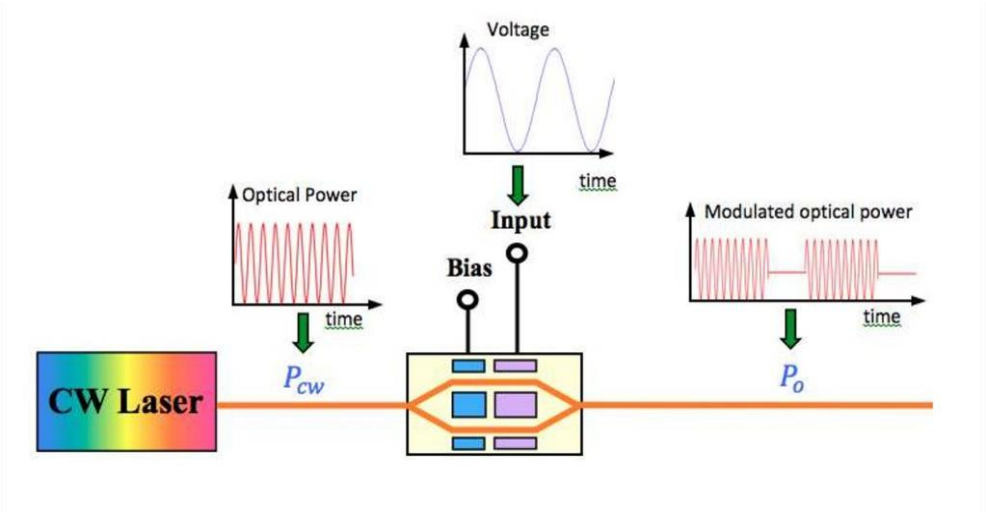

Figure 3.2 Schematic view of the Optical modulator [66].

The variation in carrier concentration with applied bias modulates the local eff. refractive index of the substance or any material that causes variation in the phase of the guided optical wave. A carrier injection optical modulator

is usually realized with an embedded p-i-n junction inside the waveguiding region of a spectrum. When a positive bias is applied to the junction via ohmic contact, a large number of electrons and holes will be injected into the intrinsic region, thereby causing a change in the real and imaginary parts of an effective refractive index [67]. An accumulation type modulator is characterized by an insulating layer (a barrier layer is also known as) that is formed into a waveguiding region, so that free carriers accumulate on both sides of the insulating layer under the influence of an electric field. In this category of modulation process, the device is not limited by the lifetime of the minority carrier [68].

3.2.2 Optical Waveguide:

Waveguides are constructed by enclosing a longitudinally extended high-index optical medium, called the core, by a low-index optical medium, called the cladding. In the waveguide, a guided optical wave propagates along its longitudinal direction.

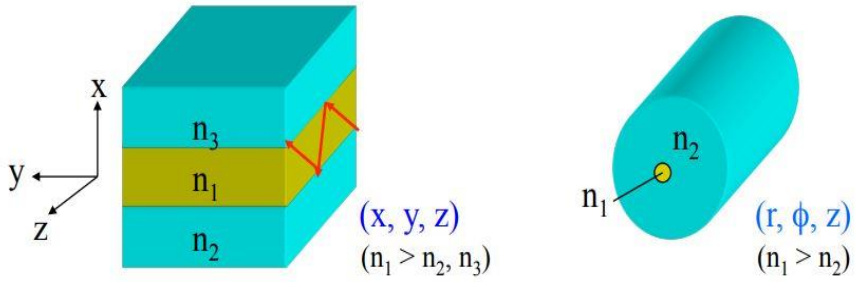

Figure 3.3 shows the (a) planar Waveguide (b) Optical Waveguide [68]

The core of a planar waveguide is sandwiched between upper and lower cladding layers, with an index profile n(x), in only one transverse direction. The lower cladding layer is called the cover, and the upper cladding layer is called the substrate. In fiber-optic transmission, optical waveguides are a key part of the design of waveguide couplers and modulators, as well as key elements in semiconductor lasers[69]. Optical waveguides are used as passive and active waveguides for expressing light across different displacements, varying from

tens or hundreds of meters in PIC to hundred's or thousand's of km in broad-band distance optic fiber transmission. The modes exist only at that are properties of a particular waveguide structure [69]. A mode is a perpendicular field pattern where the polarization and amplitude profiles remains constant with the latitudinal z-axis coordinate. Hence, the E.F and M.F of a mode can be written as follows

$$E_v(r,t) = E_v(x,y)expi(\beta_v - wt) \quad (3.1)$$

$$H_v(r,t) = H_v(x,y)expi(\beta_v - wt) \quad (3.2)$$

here υ is the mode index, $H_\upsilon(x, y)$ & $E_\upsilon(x, y)$ are the mode area region profiles, and βυ is the propagational constant of the certain mode.

3.2.3 Photodetector:

In a photonic link, photodiodes, also called photodetectors, convert incident optical radiation into electrical signals, either voltage or current. They transform optical power levels to electrical bits. Its working principle is based on the photon absorption process. At first, a photon with enough energy is absorbed by an electron in the valence band. Once this electron has absorbed the photon's energy, it jumps to the conduction band, resulting in the creation of a pair of electrons and holes [32]-[34]. It is possible to design a photodetector in several different ways, the most straightforward one is to build the sensing part directly into the input waveguide, This allows the light to reach the detector and generate current. The electronics process of the generated current is to determine the wave of the input light [35].

3.3 Plasma dispersion effect:

A device can increase the modulation efficiency based on plasma-dispersion effect [36]. This enhancement in the modulating efficiency arises from the decreased effective conductivity mass of dielectric with respect to

pure Si devices. there is a deep theoretical analysis of Soref's eq. from Drude's model [30].

$$\Delta\eta = \left(\frac{q^2\lambda^2}{8\pi^2 c^3 \varepsilon_o n}\right)\left(\frac{\Delta N_e}{m^*_{ce}} + \frac{\Delta N_h}{m^*_{ch}}\right) \tag{3.3}$$

It can be seen from the graph that all constant variables are being fixed exceptional to the area of refractive index Δn and both electrons and holes effective conductivity mass m^*_c. The variation in refractive index from the plasmonic-dispersion effect may have inversely proportional to m^*_c.

3.4 CMOS Photonic devices:

Due to inherent limitations in the platforms available, electronic and photonic devices have been challenging to integrate on a single basic platform for a long-lasting time [69]. The MOS Transistor controls the flow of electrons from source to drain by controlling the voltages at its terminals. Today, millions of MOS transistors can be placed on a single semiconductor chip but a modulator controls the flow of photons from source to drain by adjusting the voltages of the two arms. Some of photonic devices are discussed below

3.4.1 Optical MOSFET:

Silicon CMOS technology has progressed to the nanometer scale. The key to sustained performance improvement is the continued miniaturization of transistors [70]. As a result of this aggressive scaling, higher order effects have also been observed, which adversely impact the device's functions. A CMOS and optoelectronic integration offers all the benefits such as immunity to interference of electromagnetic fields, greater reliability, etc. In the presence of light that falls on a semiconductor, photons which have a greater energy than that of the bandgap energy of the semiconductor are absorbed [71]. By coupling an electron to the conduction band, a hole is created in the valence band. All electrons and holes in the conduction band

move freely beneath an electric field that is generated intrinsically or externally.

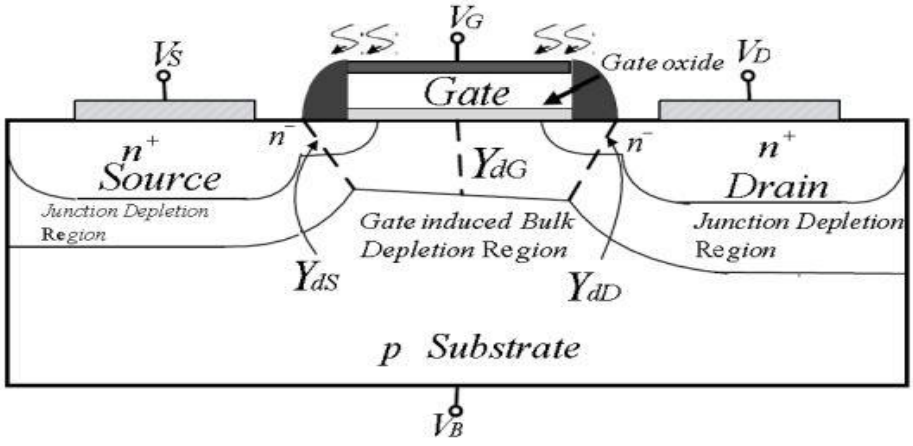

Figure 3.4 Schematic of MOSFET under the illumination [29].

As a result of the absorption of photons, the separation of electron-hole pairs enhances the conductivity, and this photocurrent increases with the intensity of the incident light. In figure 3.4, we see an illumination schematic for an MOSFET. The Aluminum electrodes stop the incoming incident light, but the EM wave is absorbed by the gate potential [72]. Due to the emphasis on low-voltage, low-power, and high-speed design, threshold voltage V, and subthreshold swing S have become increasingly important. The threshold voltage of the MOSFET can be calculated by

$$V_t = \Delta + \frac{\sqrt{2\mathcal{E}_s q N_{sub}(2\emptyset_b + V_{sb})}}{C_{ox}} \tag{3.4}$$

$$\Delta = V_{fb} + 2\emptyset_b \tag{3.5}$$

However, due to continuous scaling of MOSFET, several challenges like it short channel effects (SCE) arise, which results in the leakage of current in the device, reduction of subthreshold swing, and increase in OFF current. To overcome this problem and reduce these effects, FinFET was proposed which offers better control over SCE [73]. FinFET improves the sub-threshold swing degradation, it rolls off the threshold voltage by reducing

the drain-induced barrier lowering (DIBL), increases On-current with high carrier mobility, and improves the subthreshold swing and better optical phase modulation and absorption.

3.4.2 The FinFET- Multi-gate Transistor:

The continuous downscale the channel in the MOSFET technology following Moore's law trend, new challenges arise in device fabrication and performance [74]. However, due to continuous scaling of MOSFET, several challenges like it short channel effects (SCE) arise, which results in the leakage of current in the device, reduction of subthreshold swing, and increase in OFF current. TFET is proposed to reduce the SCE based on band-to-band tunneling, however, it can be problematic due to drawbacks like low On-current and ambipolarity [75]. Planar MOSFETs based on bulk Si wafers (also known as bulk MOSFETs) have previously been used as planar MOSFETs. By eliminating the extra substrate beneath the channel, fully depleted silicon-on-insulator (FDSOI) MOSFETs (planar MOSFETs built atop SOI wafers) eliminate extra leakage routes from the drain to source. Their performance characteristics are comparable to those of MGFETs with two gates, known as double-gate FETs (DGFETs). Both have lower junction capacitance, a greater Ion/Ioff ratio, better subthreshold performance, and superior robustness against random dopant fluctuation (RDF). Due to their simple architecture and ease of production, FinFETs (a form of DGFET) and Trigate FETs (another common MGFET with three gates) have emerged as the most sought MOSFET replacements [76]. Two or three gates wrapped around a vertical channel enable easy alignment of gates and compatibility with the standard CMOS fabrication process. To construct the third gate on top of the channel in Trigate FETs, an additional selective etching step of the hard mask is required. Although the third gate increases process complexity, it also provides benefits such as lower fringe capacitances and increased transistor width [65]. To overcome all this problem and reduce these effects, FinFET was better device which offers

better control over SCE. FinFET improves the sub-threshold swing degradation, it rolls off the threshold voltage by reducing the drain-induced barrier lowering (DIBL), increases On-current with high carrier mobility, and improves the subthreshold swing [66].

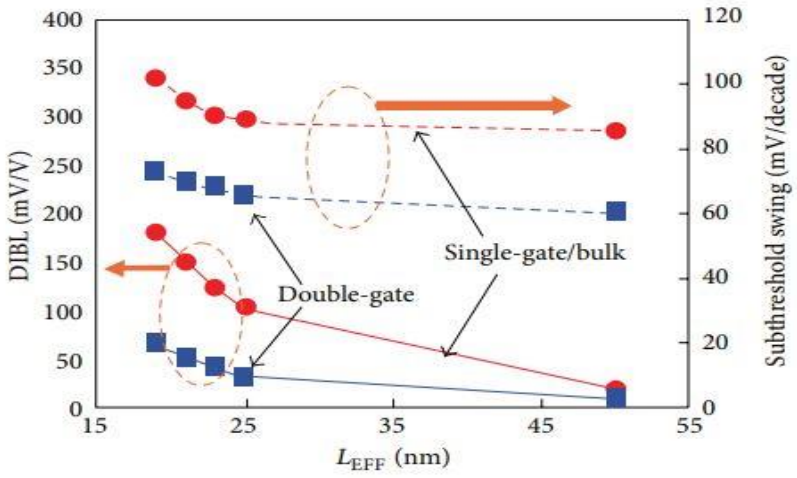

Figure 3.5 DIBL and subthreshold swing (*S*) vs eff. Length of channel for bulk-silicon n FETs and double-gate (DG) [66].

The electrostatic field of the potential in the subthreshold area region can be described by 3-D Laplace's equational if the potential perturbation due to the charge carriers and concentration of doping can be removed, which is the case for fin with undoped.

$$\frac{\partial^2 \Psi}{\partial x^2} + \frac{\partial^2 \Psi}{\partial y^2} + \frac{\partial^2 \Psi}{\partial z^2} = 0 \qquad (3.4)$$

The buried substance oxide is analyzed to be large enough that any limited potential voltage across the buried material oxide or substance leads to a negligible E.F [67]. The boundaries between gate oxide and silicon fin are eliminated by replacing the physical dimensions with effective dimensions. The whole region is treated as homogeneous silicon with effective thickness (T_{eff}), effective channel length (L_{eff}) and effective height (H_{eff}) [68].

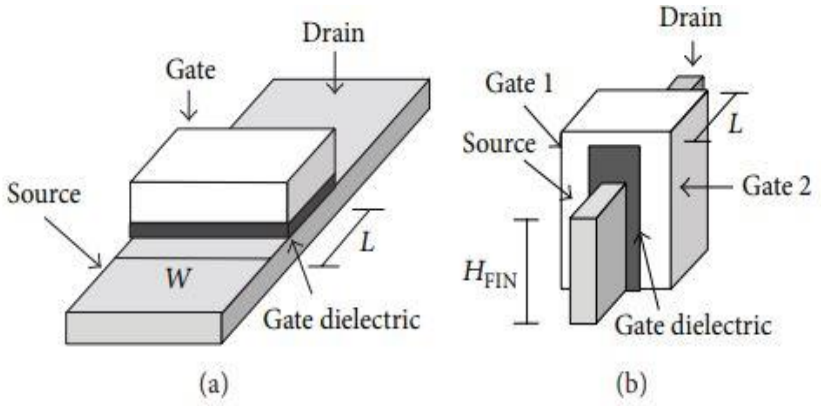

Figure 3.6 Device comparison between (a) MOSFET and (b) FinFET.

To define T_{eff} and H_{eff} is to replace the amount of insulator area with an equivalent region with thickness of the parametric oxide region modified by $\frac{\varepsilon_{Si}}{\varepsilon_{ox}}$.

$$T_{eff} = T_{fin} + \frac{2\varepsilon_{Si}}{\varepsilon_{ox}} T_{fin} \tag{3.5}$$

$$H_{eff} = H_{fin} + \frac{2\varepsilon_{Si}}{\varepsilon_{ox}} H_{fin} \tag{3.6}$$

FinFETs are less susceptible to dopant-induced fluctuations, and reduced channel doping provides higher carrier mobility within the channel. This enables lower threshold voltages to be used, resulting in improved performance and decreased power dissipation [69], [70]. The drive current of the FinFET can be improved by improving the thickness of the fin, thereby increasing the width of the Fin. Based on the graphical device, the fin dimension of the height of a single-channel FinFET might be half of the eff. channel width (electrical width), W_{eff}.

$$W_{eff} = 2H_{fin} + T_{fin} \tag{3.7}$$

Considering FinFET may soon become an industry standard it is also introduced in the silicon photonics where the device is analyzed when the optical light is passed across the structure [71].

3.4.3 Optical properties of FinFET structure:

Electrically control of light at nanoscale is an absolute necessity for on-chip optical devices. The optical switches and electro-optic modulators are the main components of any photonic integrated circuits [72]. Silicon has a week nonlinear effect and at 1550-nm the silicon has high transmission and low absorption hence difficult to modulate light in silicon-based electro-optic modulators. The FinFET is a symmetric three gate structure, which means that all its three gates have the same work function and also at the same potential [73]. The three-dimensional (3-D) structure requires 3-D analysis. The electrostatic potential with non-uniform channel doping in the vertical direction can be described by the 3-D Poisson's equation.

$$\Delta^2 U = \frac{q[N_b(x,y,z) - n(z,y,z) + p(x,y,z)}{\mathcal{E}_s} + \Delta n \qquad (3.8)$$

where $N_b(x, y, z)$ is the doping concentration of the channel in non-uniform in the longitudinal direction, U(x, y, z) is the surface potential point at a particular region (x, y, z), q is the charge of the device, ε_s is the permittivity of Si, p(x, y, z) is the concentration of hole, n(x, y, z) is the concentration of electron, Δn is the amount of extra charge carriers generated per unit volume because of illumination [74]-[76]. The amount of extra carriers created per unit of the volume because of the absorption of incoming optical power charge density are given by

$$\Delta n = \frac{1}{W_m} \int_0^{W_m} G_{op}(x) T_L \, d_y \qquad (3.9)$$

Where W_m is the maximum width of the layer in the depletion and is given by

$$W_m = \left[\frac{4\mathcal{E}_s \ln (N_a/n_i}{q\beta N_a}\right] \qquad (3.10)$$

where Na is the concentration of the acceptor.

The number of carriers created by a photodetector per incident photon is known as quantum efficiency and dots [77]. The active couple of pairs generated divided by the number of active photons may be absorbed that is called the internal quantum efficiency, and it is generally quite large in defect-free materials. Because it represents the useful fraction of signal created by the cross section of light and photodetector, the external quantum efficiency only particular number for photon generated charge carriers gathered as a result of light absorption. For photodetector characterization, external quantum dot mechanical efficiency is a high important metric than internal quantum efficiency [79]. The particular number of carriers captured divided by the amount of incident electrons and photons is known as external quantum dot efficiency. The absorption coefficient of the particular material and the amount of the thickness of the engross material determine the external quantum efficiency. If the photo flux carrier density at the surface is zero and there is no reflection of electromagnetic wave from the surface of the active photodetection material, Beer's law gives the photon flux at depth x [62].

$$\emptyset(x) = \emptyset_o(e^{-\alpha x}) \tag{3.11}$$

The drain current properties of FinFET structure for broad range V_{gs} values is taken. The drain current increases constantly with applied in the gate-to-source voltages, while the channel (Fin) width is varied by the applied gate-to-source potential. The charge carriers across the channel region and hence the conduction may occur [63]. When the drain voltage is improved, extra amount of charge carriers' density passes through the fin, resulting in an I_d. These charge carriers' density passes across the Fin width area that was created previously. Therefore, even if the drain voltage is further improved, the I_d will saturate after a certain point. Many factors can affect the optical phase modulation, the charge carrier injection and the high-frequency capacitor may reduce its speed [65]. Electric contact points and increased doping levels also affect it.

Chapter 4

Guiding and controlling light at Nanoscale in FinFET

Transistors are the basic building block for semiconductor electronics. Controlling optical signals can be done with MOS-based matured electronic technology. Another problem to solve is controlling light at the nanoscale. The leaky optical mode from the plasma dispersion effect can be exploited to modulate the optical signal in a hybrid plasmonic waveguide. The FinFET device is proposed is made to guide and electrically tune the EM wave at nano dimensional scale using the hybrid of plasmonics waveguide and optical mode profiles. The HP mode is confined in the insulator that is SiO_2 is compromised in between metal Au and s.c (Si) Fin channel which is formed from the adjoining of SPP mode at the metal-insulator interface with the optical guided mode in the insulator. A hybrid plasmonic waveguide can effectively overcome the propagation losses with better mode confinement by confining the optical mode in the dielectric (SiO_2) and far away from the dielectric-metal surface interface thus it achieves better propagation length. HPWG has an added advantage of Polarization diversity compared to plasmonic waveguides where it exhibits both TE and TM mode profiles [42]. An electromagnetic field with the TE component, couples to a metal-dielectric interface resulting in a hybrid plasmonic mode present in the low index layer whereas TM resides in the high index layer. The charge-carrier density along with the dispersion effect in the Fin channel, through potential applied on the gate and source-drain, result in the phase modulation in FinFET. The change in the complex eff. refractive index is observed by varying the gate voltage in this structure [45]. The Finite-Difference Eigenmode (FDE) using LUMERICAL software is made to analyze and design the device structure. In order to utilize the full potential of the introduced hybrid plasmonic waveguide for the on-chip practical applications electrical control is to be incorporated. It has been achieved that a number of optical functions can be implemented on-chip to guide the light across a variety of materials and then to control it for varying applications.

3.1 Device design and Optical guidance:

Fig. 1(a) shows the proposed design of the FinFET structure at a nanoscale of the optical waveguide. FinFET is a multi-gate transistor where the channel is vertical, unless in the MOSFET the channel is in the lateral direction. In the FinFET device, the channel is surrounded by the gate on the three sides, due to these multiple gates, the charge carriers can deplete more in the channel, thus gate has much better control over the channel by diminishing the short channel effects and leakage of current.

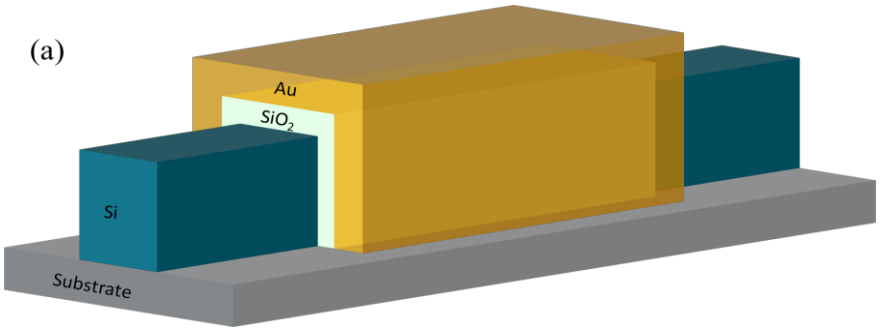

Figure 4.1 Schematic three-dimensional view of FinFET, gate wrapped over the Fin on 3 sides, where the gate is Gold (Au), Silicon dioxide (SiO_2), and Silicon (Si).

When the fin height is smaller, there is more pliability to the multiple fins and leads to more silicon area but fins with a taller height take less silicon area. When we shine the light perpendicular to the channel (Fin), the light is excited with the charge carriers at the metal surfaces, that the hybrid plasmonic mode is squeezed much more in the dielectric layer, which enables the confinement of two-mode polarizers, i.e., TE and TM mode can be observed in the SiO_2 layer. TE mode is confined in the two vertical slots regions formed in between the Si layer and metal whereas TM mode is confined in the horizontal slot region of the dielectric layer that is in between the bottom of the metal and the top of the silicon. The optimized dimension of the Silicon width (w_{si}) and thickness (t_{si}) is 200 nm and 300 nm. The geometrical dimensions of the SiO_2 layer width (w_h) and thickness

(t_h) are 10 and 10 nm and the dimensions of gold, width (w_m) and thickness (t_m) are 100 and 100 nm. Gold (Au) is the most promising material for the plasmonic with low losses at the surface roughness and also in the Infrared and visible ranges.

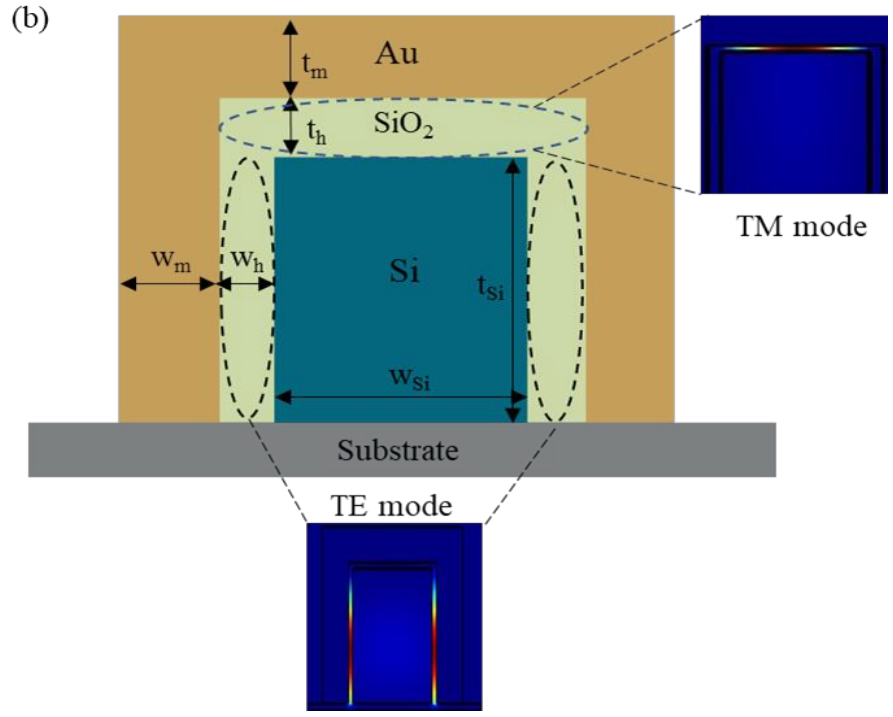

Figure 4.2 depicts Cross-sectional view of FinFET, it shows TM mode in the lateral direction of the SiO_2 and the vertical direction of the SiO_2, mode confinement exists in the TE mode.

Gold has better temperature stability, oxide resistance and is chemically stable. Figure 4.2 depicts the representation view of the FinFET, where the hybrid plasmonic mode is guided in the SiO_2. For simulation, the Lumerical Eigenmode solver is used to conceptualize about the field confinement of the mode, which supports both TM and TE, and this Eigenmode solver is used to calculate the different modes in the HPWG [52]. In the fundamental mode wave, the TE mode profile is confined in the two vertical directions of the SiO_2 layer that has a very high-power density due to the field confined in the SiO_2 layer in the lateral direction that is sandwiched in between the Si and the metal surface where the field area of the enhancement exists due

to the strong discontinuity of the applied E.F in the normal component. This kind of phenomenon occurs only if the SiO_2 thickness is less than evanescent wave's penetration depth, results in the optical and surface plasmonic modes overlapping each other.

3.2 Electrical Characteristics:

In an N-type FinFET when we apply the positive voltage at the gate, an electric field starts moving downwards and the holes are repelled away from the surface of the channel, where the negative ions are left in the channel that forms an inversion layer. The source and drain potential are connected to the opposite side of the fin and when the drain potential improved the current conduction takes place in the Fin. When the drain to gate voltage improved there a large number of minority carriers (holes) are repelled away from the surface of the channel which results in a large variation in eff. refractive index ($\Delta\eta_{eff}$), and in the channel initially the current is in the triode region after it reaches to saturation as the drain potential increases [54]. The Drude model hypothesis says that $\Delta\eta=\frac{\Delta\varepsilon}{2\sqrt{\varepsilon}}$, that the complex permittivity is changed with the variation in the charge carrier density which leads to the variation in the complex eff. refractive index. The eff. refractive index of electrons is three times smaller than the holes for the same charge carries. The Lumerical device simulation tools introduce the charge carrier density into the Lumerical mode solution through the index perturbation for examination of changes in the light characteristics owing to the applied bias [58]. In the simulation, a fixed wavelength of 1550nm is used and the refractive index of Silicon and SiO_2 is 3.48 and 1.44, for the metal (Gold) is =-115.13+111.259. Figure 4.3 (a) depicts the transfer characteristics of the V_{GS} vs I_D graph, where the drain current is constant up to the gate voltage of 0.6V, after the gate voltage higher drain current also higher exponentially. Figure 4.4(b) shows the output characteristics of the V_{GS} vs I_D graph for the V_{GS}=0.4V and 0.8V, initially, the drain current is in the

triode region after the V_{DS}=0.7V the drain current becomes saturation, as V_{DS} increases the drain current becomes constant.

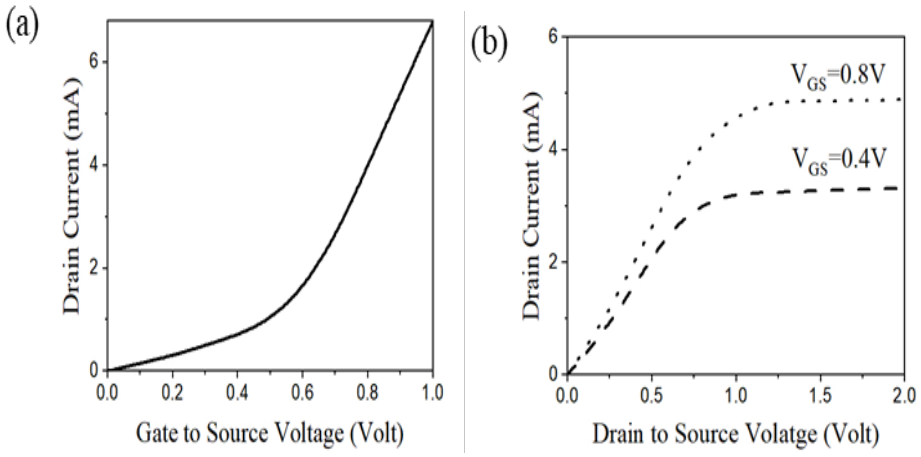

Figure 4.3 shows the simulated characteristics of N-type FinFET structure, (a) The transfer characteristics of V_{GS} vs I_D graph for a fixed voltage of V_D=0.5V, and (b) shows the output characteristics of V_{DS} vs I_D for fixed gate voltages of V_{GS}=0.4V, 0.8V.

This kind of phenomenon occurs only if the SiO_2 thickness is less than the evanescent wave's penetration depth, which results in the optical and surface plasmonic modes overlapping each other. Here, the lateral and vertical dimensions of the Si are decided in such a way that only the leaky mode should travel in it [65] . Grading the doping profile and the interaction of the light and carrier concentration of the charge density made a pathway to the electro-optic phase modulation Many factors influence the device modulation speed. The injection of charge carriers in the fin and the transistor's high freq capacitance limit the device's optical phase modulation speed. Concentration of doping increases in the drain/source region also creates a problematic to the device's modulation speed. Physical contact pads, as well as their selection and positioning, play a role in reducing the device's phase modulation speed and the absorption of the material.

3.3 Optical parameters of the FinFET structure:

Lumerical CHARGE and MODE solver software are used for performing the simulation. Lumerical charge is used to examine the electrical characteristics and to obtain the charge distribution with the applied gate voltage is performed on the FinFET structure. Then using a drift-diffusion transport solver obtained in CHARGE is transported to the MODE solver for simulation to extract the phase response, variation in eff. refractive index with the variation in gate voltage, and to observe the fundamental mode of TE and TM mode.

3.3.1 Change in Real of effective refractive index:

When we shine the light perpendicular to the channel (Fin), the light is excited with the charge carriers at the metal surfaces, that the hybrid plasmonic mode is squeezed much more in the dielectric layer, which enables the confinement of two-mode polarizers, i.e., TE and TM mode can be observed in the SiO_2 layer. TE mode is confined in the two longitudinal slot regions formed in between the Si layer and metal whereas TM mode is confined in the lateral slot region of the dielectric layer that is in between the bottom of the metal and the top of the silicon. Figure 4.4 and Fig. 4.5 depicts the variation in the real of the η_{eff} with the applied gate voltage for

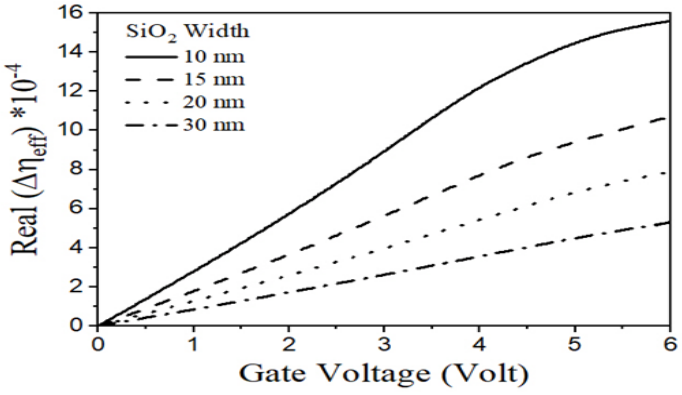

Figure 4.4 depicts the variation in the real part of the eff. refractive index ($\Delta\eta_{effreal}$) vs gate voltage(V) graph in TE mode

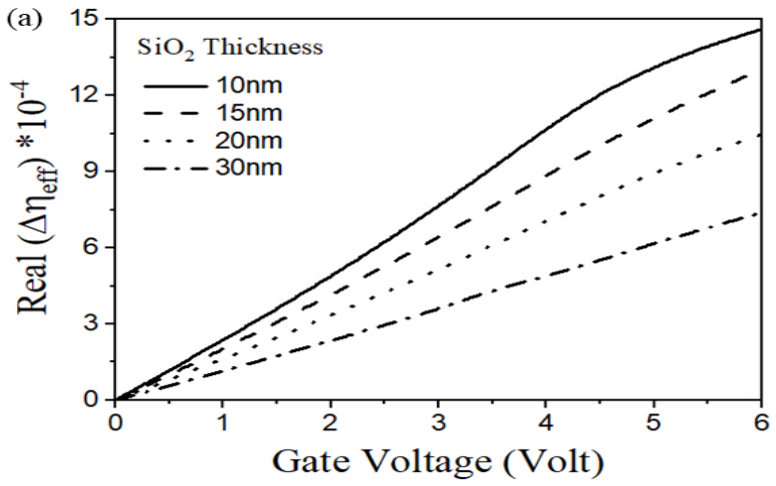

Figure 4.5 depicts the variation in the real part of the eff. refractive index ($\Delta\eta_{effreal}$) vs gate voltage(V) graph in TM mode.

the different SiO_2 thicknesses of 10, 15, 20 and 30 nm for the transported gate voltage in the TE and TM mode. The variation in the real part of the η_{eff} is in the order of 10^{-4} and the maximum change in the real part of the η_{eff} for the 10 nm SiO_2 layer thickness is 15.8×10^{-4} in the TE mode and for TM mode change is in order of 10^{-4}, the maximum change in the real part of η_{eff} is 14.7×10^{-4} for $10\ nm$ thickness of SiO_2. As SiO_2 layer thickness increases the change in the real of η_{eff} decreases for the TE and TM mode and the intensity of mode confinement also reduces.

3.3.2 Change in imaginary of effective refractive index:

Figure 4.6 (a) and Fig. 4.6 (b) depicts the variation in the Img part of the η_{eff} with the applied gate voltage for the different SiO_2 thicknesses of 10, 15, 20 and 30 nm for the transported gate voltage in the TE and TM mode. The variation in the imaginary part of the η_{eff} is in the order of 10^{-5} and the maximum variation in the imaginary part of the η_{eff} for the 10 nm SiO_2 layer thickness is 15.8×10^{-4} in the TE mode region and for TM mode region varies in order of 10^{-4}, the maximum variation in the imaginary of η_{eff} is 14.7×10^{-4} for $10\ nm$ thickness of SiO_2. As SiO_2 layer thickness

increases the change in the imaginary part of η_{eff} decreases for the TM and TE mode and the intensity of mode confinement also reduces

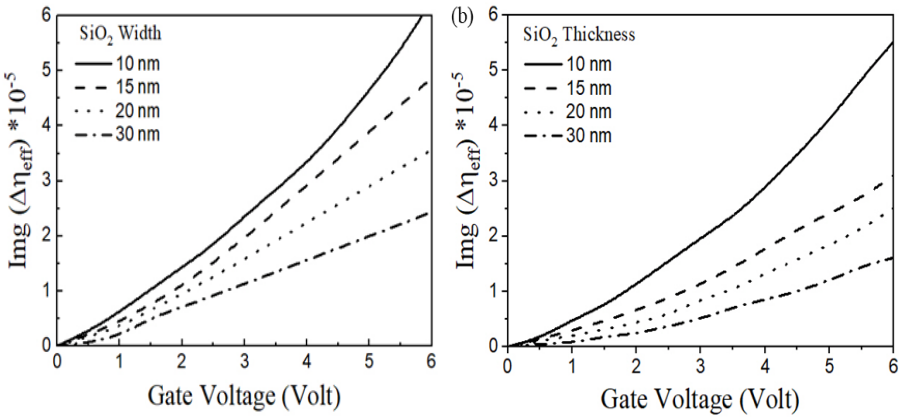

Figure 4.6 (a) and (b) depicts the variation in the imaginary part of the eff. refractive index ($\Delta\eta_{effimg}$) vs gate voltage (V) graph in TE and TM mode.

Length of propagtion of the guided mode mathematically can be defined as,

$$L_P = \frac{\lambda}{4\pi Img(\Delta\eta_{eff})} \tag{3.14}$$

Img ($\Delta\eta_{eff}$) is variation in imaginary of the eff. refractive index, propagation length of hybrid plasmonic mode for 10nm SiO_2 is 187µm.

3.4 Optical Modulation and Absorption:

A perfect Matched Layer (PML) is designed in such a way that it absorbs the radiating waves from the compute domain area by preventing reflections back into the active region and the boundaries of this PML are placed two times bigger than the dimensions of the device for the simulation in the axis of x and z [64]. We examine the phase modulation by the electrical characteristics using the drift-diffusion transport model by analyzing the charge carriers with respect to the applied potential.

Si (w*h) (nm)	SiO_2 (h) (nm)	Real($\Delta\eta_{eff}$) (10^{-4})	Phaseshift ($\Delta\emptyset$)	Img(η_{eff}) (10^{-5})	Absorption ($\Delta\alpha$)
100*100	10	12.162	170.9804	24.141	97.80
	15	2.39	179.953	11.169	45.25
	20	0.386	179.9935	0.4911	19.87
	30	0.295	179.5876	1.928	7.811
100*300	10	20.491	179.659	8.579	34.75879
	15	13.31	179.9426	9.4173	36.47431
	20	8.91	179.8325	3.941	15.96741
	30	5.27	179.928	2.3002	9.31952
200*100	10	14.2	179.7445	17.411	70.54263
	15	9.77	179.4906	9.755	39.52348
	20	6.15	179.9768	4.85	19.65032
	30	3.55	210.1692	4.39	15.46262
200*300	10	15.19	179.9986	6.5901	26.70053
	15	10.71	126.9114	4.8657	19.71393
	20	7.89	179.9531	3.571	14.46831
	30	5.3	62.28697	2.4339	9.861221
300*100	10	15.33	108.5957	6.445	25.41758
	15	8.63	178.3904	10.443	42.31099
	20	7.64	179.9294	2.973	12.04545
	30	4.97	179.9557	4.4979	18.22375
300*300	10	11.65	179.9362	4.9125	19.904
	15	11.71	150.82	3.7765	15.30092
	20	7.26	120.62	3.2756	13.27146
	30	5.2	92.32	2.3838	9.658256

Table 4.1 shows the change in phase shift, real and img $\eta_{eff,}$ absorption for various dimesnions of Si, SiO_2.

In the device, when the flow of current is perpendicular to the propagation of light, then the modulation occurs in the devices [80]. The change in the real part of η_{eff} results in phase shift ($\Delta\Phi$) and it is calculated

$$\Delta\Phi = \frac{2\pi L_\pi \Delta\eta_{eff}}{\lambda} \tag{4.2}$$

where L_π is the phase shifter of the length and $\Delta\eta_{eff}$ is the variation in real of eff. refractive index on the applied gate voltage and λ is a wavelength (1550 nm). Fig. 3(b) depicts the optical phase shift of structure on the applied gate voltage from 0 to 6 V. Maximum phase change of 180° is obtained at the gate voltage of 6V in 10 nm SiO_2 width and for 15, 20, 30 nm the phase change is 150°, 123°, and 65°.

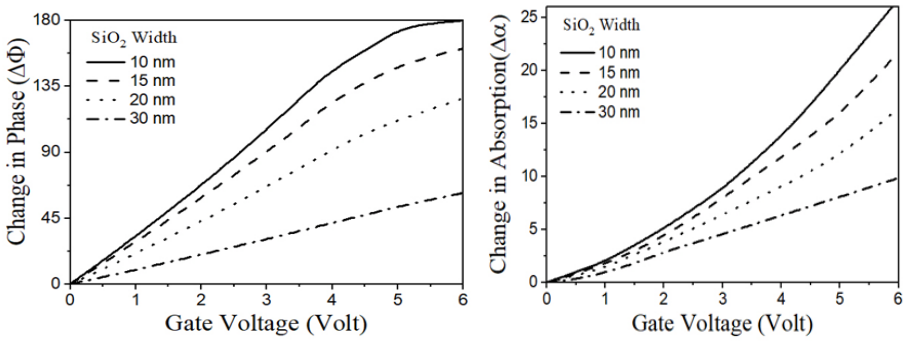

Figure 4.7 (a) shows the phase change ($\Delta\Phi$) vs gate voltage(V) (b) show the change absorption ($\Delta\alpha$) vs gate voltage(V)graph, in TE mode.

Variation in the imaginary of the eff. refractive index leads to Absorption, when the charge carriers are larger in the channel it results to high optical absorption. The change in Absorption can be calculated by the

$$\Delta\alpha = \frac{2\pi K_{eff}}{\lambda} \tag{4.3}$$

where K_{eff} is the change in the imaginary part, and λ is the wavelength. Fig. 3(d) shows the change in Absorption with the applied gate voltage from 0 to 6 V and the maximum change in Absorption is 25 for 10 nm SiO_2 width in TE mode. As the SiO_2 width increases from 10 nm to 30 nm the change in absorption decreases, for the applied gate voltage of 0 to 6 V and the minimum change in absorption is 10.5 for 30 nm SiO_2 width.

Chapter 5

Conclusions and Scope for Future Work

Summary:

A nanophotonic device based on the FinFET structure is proposed which utilizes the concept of a hybrid plasmonic waveguide. The guided optical mode is electrically controlled to realize variable phase and optical absorption. The proposed device is an able to guide both the TM and TE modes at a wavelength of 1550 nm implying that polarization independence can be achieved by altering the dimensions of the appropriate layer. The maximum variation in the real of the eff. refractive index in TE and TM modes observed are 0.00158 and 0.00147. The intensity of the mode confinement decreases as the thickness of the di-electric layer increases. A maximum phase shift of 180^{o} is achieved by a voltage swing of 0 to $6\,V$. A significant absorption change is realized in the device by tuning the voltage range from 0 to $6\,V$. By utilizing the gate and drain-source potential we can control the charge carriers in the channel thereby realizing phase tuning. In addition, a voltage tunable absorption is also reported through the voltage variable imaginary of the eff. refractive index. The proposed device can be well suited for applications in photonic devices at real nanoscales. This kind of phenomenon occurs only if the SiO_2 thickness is less than the evanescent wave's penetration depth, which results in the optical and surface plasmonic modes overlapping each other. The hybrid plasmonic mode is controlled through modulation of charge carriers' conductivity in the channel by varying the gate voltage. Here, the lateral and vertical dimensions of the Si are decided in such a way that only the leaky mode should travel in it. Grading the doping profile and the interaction of the light and carrier concentration of the charge density made a pathway to the electro-optic phase modulation The proposed FinFET structure allows a stronger impact of voltage variation on the optical properties of the guided hybrid plasmonic mode. Modulation efficiency can be further improved by increasing the doping concentration of silicon. In electronic photonic integrated circuits (EPICs), the on-chip silicon photonics

technology is emerging due to its mass production, low cost, and large-scale integration capabilities enabled by CMOS-compatible fabrication flow. The proposed concept can pave the way to build other nano-scale functions like optical modulator, optical switch, optical filter, polarization converter etc.

Future Scope:

- The thickness of Si and SiO_2 layer in the proposed device can be optimized in the FinFET structure to study the effect on mode confinement which might be result in better phase modulation.
- Introducing dark current (Optical charge carriers) in Si (Fin channel) in order to realize the change in phase shift and change in absorption, and compared with electrical charge carriers.
- The dielectric material can be replaced with a material having high dielectric permittivity for optical phase and change in absorption.
- The design of a new plasmonic material can reduce metallic losses. A highly doped semiconductor can be a good alternative to metal.

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