Analytical and Physical Modelling of Y_2O_3-based Memristive Devices for Neuromorphic Computation

M.Tech. Thesis

By

Mohit Kumar Gautam

(2002102023)

DISCIPLINE OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

JUNE 2022

Analytical and Physical Modelling of Y_2O_3-based Memristive Devices for Neuromorphic Computation

A THESIS

Submitted in partial fulfillment of the

requirements for the award of the degree

of

Master of Technology

by

Mohit Kumar Gautam

DISCIPLINE OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

JUNE 2022

INDIAN INSTITUTE OF TECHNOLOGY INDORE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **Analytical and Physical Modelling of Y_2O_3-based Memristive Devices for Neuromorphic Computation** in the partial fulfillment of the requirements for the award of the degree of **MASTER OF TECHNOLOGY** and submitted in the **DISCIPLINE OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from August 2020 to June 2022 under the supervision of Prof. Shaibal Mukherjee, Professor, Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

30/05/2022

Signature of the student

(Mohit Kumar Gautam)

This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

30/5/2022

Signature of the Supervisor

(Prof. Shaibal Mukherjee)

Mohit Kumar Gautam has successfully given his M.Tech. Oral Examination held on 07/06/2022.

Signature(s) of Supervisor(s) of M.Tech. thesis

Date: 07/06/2022

Convener, DPGC

Date: 07/06/2022

Signature of PSPC Member #1

Date: 09/06/2022

Signature of PSPC Member #1

Date: 07/06/2022

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my thesis supervisor **Prof. Shaibal Mukherjee**, for his constant support, encouragement and guidance during my Master's study and thesis work. Furthermore, I would like to express my deep gratitude to my PSPC members **Prof. Mukesh Kumar** and **Prof. Apurba K. Das** for their valuable suggestions and feedback.

I would also like to specially thank **Mr. Sanjay Kumar** for giving me valuable comments regarding the problem related to modeling and coding. Also, he helps me in critical technical discussion throughout my master research work.

I would also like to thank **Hybrid Nanodevice Research Group** for a friendly and supporting environment in the laboratory. I would also like to thank **Indian Science Technology and Engineering Facilities Map (I-STEM), IISc**, Bengaluru, India for providing license for COMSOL® Multiphysics.

IIT Indore played a vital role in providing me with the facilities, teaching assistantship, hostel accommodation and lab computer and library resource that added to my knowledge and my project. All this was made possible by incredible support and blessings of my parents who blessed me all the time, it would not have been possible without their love and support.

DEDICATION

Dedicated to my family, who have been my constant support source of inspiration. Without their love and care I would not have been made it possible ever.

Abstract

This work is the amalgamation of analytical and physical modelling of Y_2O_3-based memristor crossbar array for neuromorphic computation. Firstly, in the case of analytical modelling, the advancement has been implemented in the existing analytical model and remove the limitations to make the new memristive device more dedicated towards the neuromorphic applications by introducing two novel internal state variables namely as forgetting rate and retention. The newly introduced parameters greatly helped in investigation of the working of the system and improved the synaptic behavior in terms of potentiation and depression processes by enabling re-stimulation process effectively.

The developed analytical model is fully capable to emulate the highly dense memristive crossbar array-based neural network of biological synapses and can implement the learning capability of the neurons. These biological synapses control the communication efficiency between neurons by varying the synaptic weight between to neurons during effective communication process. During electrical stimulation of the memristive devices, the memory transition is exhibited along with the number of applied voltage pulses, which is analogous to the real human brain functionality. Further, to obtain the forgetting and retention behaviors of the memristive devices, a modified window function is proposed by incorporating two novel internal state variables. The obtained results confirm that the effect of variation in electrical stimuli on forgetting and retention is similar to that of the biological brain. The modelled data is well fitted with the fabricated Y_2O_3-based memristive crossbar array to evaluate the performance of the memristive array system and helps to understand the synaptic behavior in the neuromorphic computation. The developed analytical memristive model can further be utilized in the memristive system to develop real-world applications in neuromorphic domains.

On the other hand, a physical electro-thermal modelling of nanoscale Y_2O_3-based memristor devices has also been carried out to understand and analyze the effect of symmetric and asymmetric electrodes variation on the resistive switching (RS) properties and device synaptic properties. The physical modelling of memristor device is carried out in a semiconductor physics-based tool i.e., COMSOL Multiphysics and MATLAB Livelink with a well-defined MATLAB script. The RS responses for the reported physical model show low values of coefficient of variability (C_V) i.e., 6.69 and 7.11% in SET and RESET voltages, respectively, during cycle-to-cycle variation which eventually confirms the stability of the modelled device.

The physics-based simulation is carried out by considering minimum free energy of the materials at an applied certain voltage. The simulated results also exhibit a stable pinched hysteresis loop in the RS responses in symmetric and asymmetric electrodes combinations with an efficient ON/OFF ratio. Moreover, the simulated devices show the synaptic plasticity functionalities in terms of potentiation and depression processes with almost ideal linearity factor for symmetric and asymmetric electrodes combinations. Therefore, the presented work efficiently depicted the electrode material's suitability with the Y_2O_3 switching layer which shows better device performance and can also help the researchers to develop a perfect Y_2O_3-based memristor device for neuromorphic, digital, and logic applications.

LIST OF PUBLICATIONS

Peer-reviewed Journal Papers:

1. **Mohit Kumar Gautam**, Sanjay Kumar, and Shaibal Mukherjee, "Y_2O_3-based Memristive Crossbar Array Synaptic Learning", Journal of Physics D: Applied Physics, vol. 55, no. 20, 2022. **(IF: 3.2)**

2. Sanjay Kumar, **Mohit Kumar Gautam**, Gurpreet Singh Gill and Shaibal Mukherjee, "3-D Physical Electro-Thermal Modeling of Nanoscale Y_2O_3-based Memristive Devices for Synaptic Application", IEEE Transaction on Electron Devices, vol. 69, no. 6, 2022. **(IF: 2.9)**

3. Kumari Jyoti, **Mohit Kumar Gautam**, Sanjay Kumar, Sushma Sai, Ram Bilas Pachori, and Shaibal Mukherjee, "Memristive Crossbar Array-based Computing Framework for DWT with Application in Medical Image Processing" IEEE Transactions on Emerging Topics in Computing. (**IF: 7.6)** (Under Communication).

4. Sanjay Kumar, Mayank Dubey, **Mohit Kumar Gautam**, Saurabh Yadav, Shaibal Mukherjee, "Transition from Memcapacitive to Memristive Behavior in Al/Y_2O_3/GZO-based Crossbar Array", IEEE Transaction on Electron Devices. **(IF: 2.9)** (Under Communication)

5. **Mohit Kumar Gautam**, Sanjay Kumar, Mayank Dubey, and Shaibal Mukherjee, "Investigation of Electrodes Variation on Nanoscale Y_2O_3-based Memristors via Physical Electro-Thermal Modelling", Nano Futures. **(IF: 3.3)** (Under Communication)

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBERIVIATION

RRAM	Resistive Random Access Memory
STM	Short Term Memory
LTM	Long Term Memory
LRS	Low Resistive State
HRS	High Resistive State
CF	Conductive Filament
LTP	Long Term Potentiation
STP	Short Term Potentiation

Chapter 1

Introduction

1.1 Background

Artificial neural networks are inspired by the remarkable efficacy of biological systems, and can be practically realized by utilizing two-terminal memristive devices [1]. Further, the emulation of the synapse is a promising step toward the enhancement of efficiency of artificial neural networks [2]. The synapse is one of the fundamental cellular units of the biological neural unit [3]. More specifically, in the biological nervous system, neurons are interconnected with one another through synapses, and information gets transferred from presynaptic to post-synaptic neurons via synapses [3, 4]. During this transfer, the synaptic weight of the synapse, which is analogous to the memristive device conductance, can be modulated under the application of electrical stimuli [5]. The synaptic weight is strengthened under the application of positive electrical stimuli, while in the case of negative electrical stimuli, the synaptic weight is debilitated [4].

In neuromorphic computation, the strengthened and debilitated processes are termed as the potentiation and depression mechanism, respectively [4, 5]. The synaptic weight of the memristive device can be dynamically varied according to the use of electrical pulse excitations [6, 7]. Synaptic plasticity is the fundamental functionality of the biological brain to change and receive new information, and plays vital role in the learning and forgetting process in the human brain [8].

Neuromorphic computation requires ultralow power, high-density networks, remarkable efficiency and complementary metal oxide semiconductor-compatible devices and systems [7, 9]. A memristive system fulfilling all these requirements would make it a highly suitable candidate for neuromorphic computation [5], synaptic functionality [10] and data storage applications [11]. Besides these, memristive systems are able to show various synaptic functionalities, such as nonlinear

transmission characteristics [12], spike-rate-dependent plasticity [2], spike-timing-dependent plasticity [2], long-term potentiation (LTP) [13], short-term plasticity (STP) [13], learning behavior [14] and forgetting behavior [14], and short-term memory (STM) [15] and long-term memory (LTM) [15] behaviors of the real biological synapse.

Due to the versatile nature and competent characteristics of memristive devices, it is the need of new era to do the comprehensive study and modelling of the memristors which could eventually leads to tackle the substantial challenges in the new world of nanotechnology i.e., Moore's Law.

1.2 Motivation

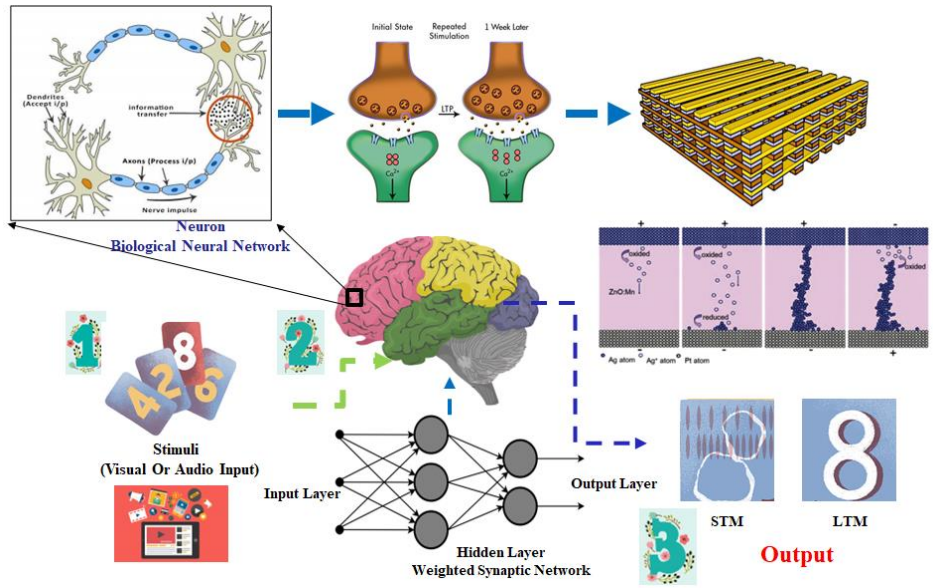


Figure 1.1: Detailed Schematic illustration in the process form of a Biological Synapse and the ion channels neuron membrane. In an extremely simplified model, the signal transmission strength from the presynaptic neuron to the postsynaptic neuron.

Memory is a vital fundamental building block in learning and decision-making process in biological systems. Human memory is not permanent, not like semiconductor memories. Forgetfulness is the key characteristic of learning behavior; it is not always seen as a disadvantage since it free up space memory storage for more valuable or more often approached data and necessary to adjust to new condition. Eventually, only memories that

are important enough are transformed from short-term memory (STM) into long-term memory (LTM) through continual stimulation. Stimulus could be anything that could be sensed by our senses. In the neuromorphic computation applications, on the essential basis device must be ideal to the human brain which possess characteristics as the human brain does. Through incorporating the forgetting behavior in the existing device models, leads to the advancement in the endeavor to successfully achieve the milestone of silicon brain. Retention loss in a nanoscale memristor device bear striking resemblance to memory loss in biological systems. Conventional models of the memristor attempted to bring the characteristics of the device closer to the ideal brain but suffered due to synaptic bottlenecks till now higher ideality hasn't achieved yet. To overcome the bottleneck and to bring closer to the human biological system, retention and forgetting ability must be incorporated in the memristive systems. Memristive devices with forgetting and retention effect support artificial neural network structures with the potential to support application in neuromorphic in-memory computation.

1.3 Memristor

Memristors can be used in extensive range of applications due to its versatile and characteristic properties. For each different application, memristor should possess different characteristics. For an instance, memory design, an element that have the ability to compute, control and store the data after computation is needed. They need to have fast read and write times. The reading mechanism shouldn't change the data while reading. The difference between stored data should be large enough to avoid bad noise margins and have better sensitivity. Needed high loop areas in order to achieve larger window for multiple levels so that number of bits can be stored. Also, for storing Boolean data or design logic in a memristor, the ratio between Ron and Roff or Ion and Ioff resistances should be high enough. There are other characteristics that are important for memristor applications, such as good scalability, switching speed, retention, ON/OFF

ratio, endurance, low power consumption, flexibility and compatibility with conventional CMOS.

Memristor, the fourth fundamental two-terminal element other than resistor, capacitor and inductor, was first described by Leon Chua in 1971 element when combining the fundamental physical quantities in electromagnetism i.e., current (I), charge (Q), flux (Φ), voltage (V) and time (t). Figure 1.2 shows the relation between each pair formed from these quantities. Out of the possible six combinations, three elements were already known prior to his work; i.e., capacitor, inductor and resistor and two are based on well-established Ampere and Lens law. The relation between flux (Φ) and charge (Q) was identified as the missing element as pointed out in Figure 1.2. This implies that this missing element keeps track of not only the amount and direction but also, the history of charge flown through that element Regardless of the discovery, memristive device technology underwent a long period of silence due to strong dominance of CMOS technology in computing systems. However, since the successful demonstration of TiO2-based memristor device by HP labs in 2008, amid recent stagnation faced by CMOS technology, memristive device technology is considered as a potential to replace/- complement CMOS technology. Some of the attractive attributes offered by memristive device technology are non-volatility, high scalability and good compatibility with CMOS technology. The shared characteristics of the family of memristive devices include the property to switch between stable resistance states and retain the state even without any voltage supply (non-volatility). Some of the well-known memristor-based memories are phase change memories (PCM), spin-torque transfer magnetic RAM (STT-MRAM), conductive bridge RAM (CB-RAM), redox oxide-based RAM (ReRAM).

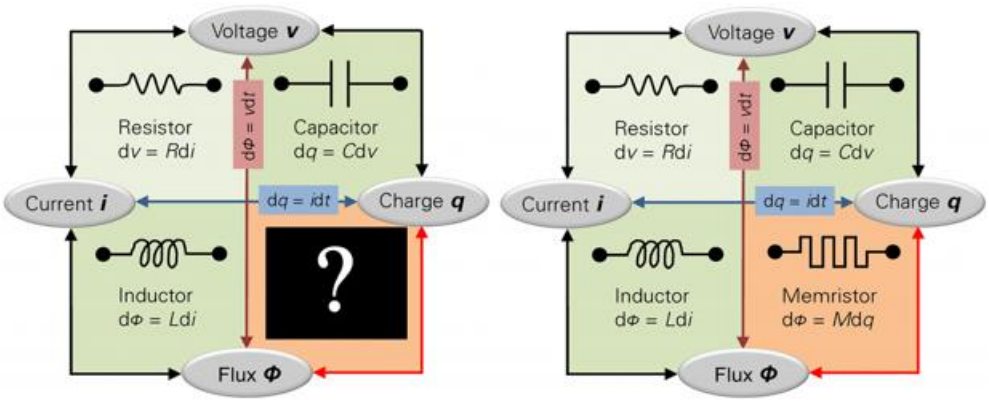


Figure 1.2: Linkage among four fundamental elements and basic circuit parameter [16].

Memristor-based applications require an appropriate model for analysis and simulation of the system. Going through the literature, we can see that HP memristor model works on the principle of the drift of oxygen vacancies. The HP Lab memristor model composed of Pt/TiO_2/Pt structure, as shown in Figure 1.3. In HP labs model, a positively charged oxygen vacancies are present at one side of the TiO_2 oxide layer, which is sandwiched between the two noble metallic layers, i.e., platinum [16].

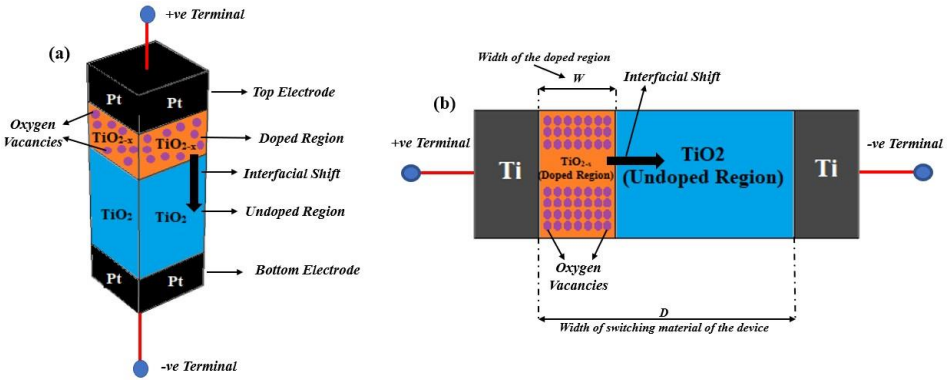


Figure 1.3: The structure of TiO2-based memristor developed by HP Labs.

The doped part of oxide layer shows the low resistance behavior while the high resistance behavior is demonstrated by an undoped portion of the oxide layer. On an application of appropriate supply, the ionic drift between the doped portion and therefore the undoped portion leads to a change in

the width of the doped region. Here the width of the doped region is taken as a state variable. Also, when the width of the doped region approaches zero, the memristor goes to a high resistance state (HRS). When the width of the doped region approaches a boundary, the memristor goes to a low resistance state (LRS). Since the dimensions of memristor are very small (~nm), a low excitation in the supply can cause a change in the doped region. Thus, the resistance of the memristor varies between HRS and LRS [17]. Negative bias electroforming drives O^{2-} ions to the lower electrode, where they discharge to form O_2. The conducting channel thus formed is the Magneli phase Ti_4O_7, which acts as a source/sink of oxygen vacancies in TiO_2. TiO_2 is an insulator TiO_4 is a conductor. Initial cell resistance is high (e.g., bit =0). Voltage causes TiO_4 to migrate, producing lower cell resistance. This state is stable when voltage removed. (e.g., bit =1). Reverse voltage cause TiO_4 to migrate back, causing higher cell resistance. This state is stable when voltage is removed. (e.g., bit =0)

The relationship between voltage, current, charge, and flux for the memristor is given by:

$$v(t) = M(q(t))\, i(t) \qquad (1)$$

$$M(q) = \frac{d\phi(q)}{dq} \qquad (2)$$

$$i(t) = W(\phi(t))\, v(t) \qquad (3)$$

$$W(\phi) = \frac{dq(\phi)}{d\phi} \qquad (4)$$

where $W(\phi)$ has the unit of conductance and $M(q)$ has the unit of resistance.

Memristor shows different properties compared from other fundamental circuit elements that are pinched hysteresis loop, passivity, and non-volatile memory effect.

When Equation (1) and (2) are analyzed, Equation (5) and (6) can be written as follows:

$$v(\mathrm{t}) = M\left(\int_{-\infty}^{t} i(t)dt\right) i(t) \quad (5)$$

$$i(\mathrm{t}) = M\left(\int_{-\infty}^{t} v(t)dt\right) v(t) \quad (6)$$

The current passing through the memristor tells about the Memristance value. That means, when the current flow through memristor is off, it retains the value of the Memristance, and when the current flow through the memristor is passed again, Memristance value will change from the last retained value, i.e., before the cutoff. That shows the non-volatile property of memristor and also tells about that, the memristor is not an energy storage element [17, 18]. Memristor is analogous to a resistor with memory [19]. The I-V curve of memristor shows the pinched hysteresis loop characteristic.

If a bipolar signal periodic in nature is applied to a memristor it shows a pinched hysteresis I-V characteristic that always crosses the origin. As the frequency of the applied signal increases the pinched hysteresis loop shows the singled valued function and behaves as a linear resistor. When the frequency reaches to infinity, the pinched hysteresis loop behaves as a single-valued function which has resemblance with resistor following ohms law [20, 21].

The memristor is a passive circuit element which can remember the state of resistance because of the voltage-current integral relationship. Because of these features, they are used soft computing, in resistive memories, neurocomputing, etc.

Resistive random-access memory (RRAM) or memristor has been widely investigated as one of the promising and leading candidates for scale limits of typical electron storage-based memories [22-25]. Based on its resistive

switching mechanisms, the memristor can be simply categorized into two types: filamentary-type and interfacial-type [24,26]. The filamentary-type memristor device can be operated in a local region and due to this, it shows a high switching speed as well as higher device scalability as compared to interfacial-type memristor [26]. However, to fulfill the desired requirements for the synaptic device, the interfacial-type memristor is comparatively more suitable than the filamentary-type memristor [27,28]. The interfacial-type memristor has extremely stable and analog resistance change as it comes from electrochemical reactions between the reactive metal layer and resistive switching layer. The resistive synaptic devices need to be evaluated in different ways with the non-volatile memories (NVMs). To implement the hardware for the neuro-inspired computing system, millions of resistive synaptic devices are necessarily required to integrate with other complementary metal oxide semiconductor (CMOS) device components. Therefore, the device scalability is one of the most critical factors for hardware implementation. From the scalability point of view, the Y_2O_3-based synaptic device offers numerous advantages such as it is simple metal-insulator-metal (MIM) structure which can be highly stable and efficiently integrated into the crossbar array architecture.

1.3.1 Resistive Switching (RS) Mechanisms of RRAM Devices

To provide a comprehensive overview of RRAM devices, it is necessary to implement and study in-depth survey on different RS mechanisms. The current investigation of RS mechanisms for RRAM devices is linked to not only materials selection of electrode/RS medium but also utilized operation modes. Now, profoundly opted switching mechanism is established on conductive filaments (CFs). This section is focused on the research of several working mechanisms related to anion/cation migration and thermal-chemical reaction, including thermal-chemical mechanism (TCM), valance change mechanism (VCM) and electrochemical metallization (ECM).

1.3.1.1 Thermal-Chemical Mechanism (TCM)

TCM can be applied to explain the formation and rupture of CFs resulted from ions (oxygen or metal ion) migration induced by thermal-chemical reaction (Joule heating), which is independent of the switching mode (unipolar and bipolar) for RRAM devices [29–31]. Zhang et al. explained the working principle of their Pt/Al/AlO_x/ITO RRAM device with TCM theory [29]. As illustrated in Figure 3, oxygen ions driven by Joule heating effect drifted to TE and left oxygen vacancies in the AlO_x layer; CFs based on the accumulation of oxygen vacancies set the device to LRS. For the RESET process of unipolar device, the current steadily increased with the increasing positive voltage bias, the formed CFs finally broke when it reached the critical temperature induced by Joule heating, which made the device switch back to HRS. Similarly, for the RESET process of bipolar device, the oxygen ions drifted back to the AlOx layer due to the melting of CFs and switched the device to HRS again. TCM based on Joule heating reaction is related to the formation and rupture of CFs. The filament based on metal Ag played a dominating role during the RS process. The formation of Ag CF made the device from HRS to LRS during the SET process. Due to the Joule-heating-based oxidation, the Ag CF ruptured by the thermal dissolution and completed the RESET operation. In general, with the SET/Forming operation, the thermal decomposition process that occurs in the RS medium generates the ions migration in the RRAM device and the resulting formation process of CFs transforms the device from HRS to LRS. With the reversed voltage bias applied onto the electrode, the existing CFs rupture due to the thermal melting reaction, which transforms the device back to HRS and completes the RESET process accordingly.

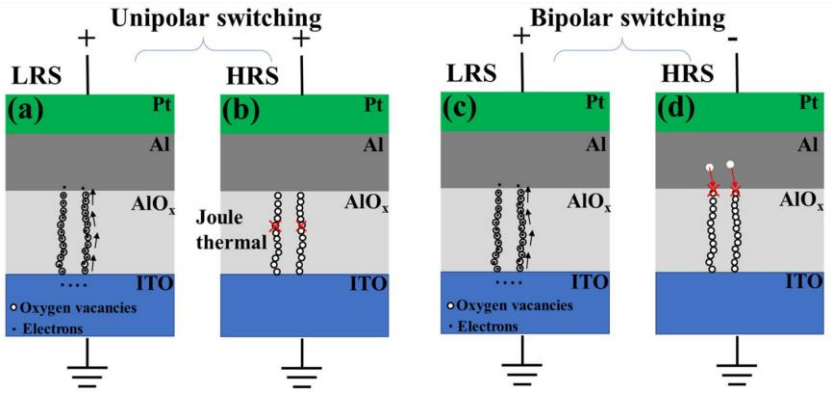


Figure 1.4: Switching mechanism of unipolar (a, b) and (c, d) AlO_x-based RRAM devices, reproduced from [39], with the permission from Springer Nature, 2020.

1.3.1.2 Valence Change Mechanism (VCM)

VCM has oxygen-related defects/vacancies and their electrochemical reaction occurred in the RS medium [32-37]. In addition, it is not necessary for an RRAM device to operate with the structure that consists of an active electrode and an inert electrode, namely, the activity difference between TE and BE is not required [38]. Chen et al. researched the unipolar performance of Pt/SiO_x/Pt RRAM device with VCM and dangling bond (DB) [33]. With the effect of ternal electric field, the strength of the polar covalent Si-O bond was weakened and finally broken. With the much higher concentration of DB near the middle of the silicon band gap, the hopping process could make the transportation of the electron through the discontinuation of DB, which was similar to the initial state (HRS) of their devices. If the DB concentration arose up to the threshold value of the percolation path, the electron transport could occur in the mini-band of DBs and the device switched into LRS, which accordingly indicated the SET process. Munjal also initiated the analysis process of $CoFe_2O_4$-based RRAM devices with the VCM theory [37]. In most cases, for VCM RRAM devices, the resistance change performance is attributed to the formation and rupture process of CF based on oxygen vacancies in the RS layer [32–37]. With the positive voltage bias applied onto the inert electrode, oxygen ions drift from where they stayed before with the effect of external electric

field and oxygen vacancies left in the RS medium. The consequent CF path made up of leftover oxygen vacancies connects TE and BE through the functional layer, which increases the electric conductivity of the RS thin film and switches the device from HRS to LRS. Whereas, with the reversed voltage bias onto the same electrode, oxygen ions drift back to the RS layer and result in the rupture of formed CF, which makes the device switch back to HRS again. Therefore, oxygen defects/vacancies and oxygen may be the dominating aspect during the growth and destruction of CF in the functional layer.

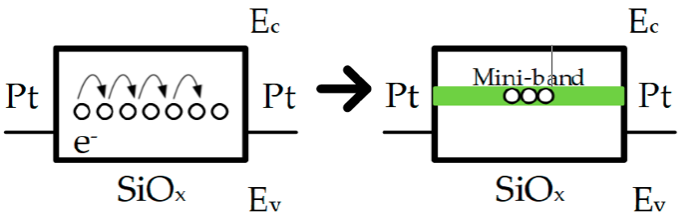


Figure 1.5: Schematic of discontinuous and continuous states of mini-band DBs, reproduced from [], with permission.

1.3.1.3 Electrochemical Metallization (ECM)

Compared with TCM and VCM, ECM based on electrochemical reaction and cation migration, as

the most recognized mechanism, is always used to explain the working principle of RRAM device with an active electrode, which is similar to VCM [39–45]. Generally, most active electrodes for ECM devices are active metal such as Cu [40–42] and Ag [39,43–45]. Tsuruoka et al. investigated Cu/Ta_2O_5/Pt RRAM device based on Cu filaments [40]. With a positive voltage bias applied onto Cu TE, Cu atoms near the interface between Cu layer and Ta_2O_5 layer were dissolved into Cu ions (Cu^{2+}) and electron (e^-) due to the electrochemical reaction. These Cu^{2+} ions drifted towards the RS layer with the effect of external electric field, which induced the Cu^{2+} ions supersaturation near the Ta_2O_5/Pt interface. Then continuous cathodic deposition reaction occurred between Cu^{2+} and e^- led the formation of Cu-based filament and switched the device into ON state.

Yu et al. also confirmed that multiple Ag filaments attributed to the multilevel RESET behavior of RRAM device with a switching layer based on nonmetal materials ($Ag/SiO_2/Pt$) [39]. With a small negative voltage bias, the $Ag/SiO_2/Pt$ device exhibited gradual resistance increasement. When the voltage bias continued to increase beyond a threshold value, the resistance of device was increased to a higher state sharply, which suggested that multiple Ag filaments were effective as predicted. As demonstrated in Figure 1.6, in the SET process, Ag CFs with different sizes existed under a big CC after several switching cycles. During the RESET process, Ag from Ag CFs transferred into Ag^+ due to the dissolution reaction, which resulted in a gradual resistance increase of device. When these smaller CFs were broken, the resistance changed significantly. After that, CFs with larger sizes were getting thinner until they ruptured, which further induced the multilevel performance of RESET process. Long et al. also used ECM based on Ag filament to explain the switching mechanism of Ag/ZrO_2: Cu/Pt RRAM device [43]. With the effect of external electric field induced by voltage bias applied onto TE Ag, the oxidation process occurred on Ag atoms and Ag atoms transferred into Ag ions ($Ag \rightarrow Ag^+ + e^-$). Then Ag+ migrated gradually to BE Pt as the electric field increased in the ZrO_2 thin film and ions were reduced back to atoms ($Ag^+ + e^- \rightarrow Ag$). Finally, the formed Ag filament switched the device into LRS when the voltage reached VSET, which showed the related metallic transportation behavior. However, for the RESET process, when the voltage bias with reversed polarity was applied onto the active electrode, the existing Ag filament was broken within the oxide layer due to the electrochemical reaction w/o Joule heat assistance. Similarly, research reported by Tsuruoka et al. also presented the same perspective, which indicated that the RESET process related to formed metallic filaments might be related to electrochemical reaction w/o Joule heat assistance [40].

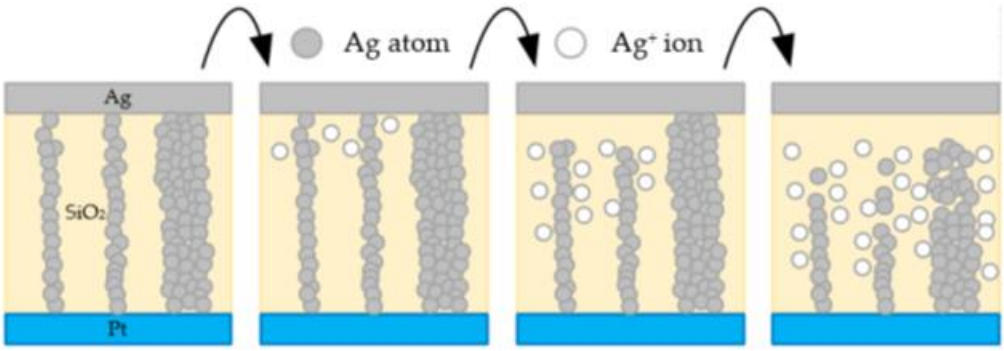


Figure 1.6: Illustration of multilevel RESET process of Ag/SiO_2/Pt RRAM device.

1.4 Organization

This chapter has introduced the background, motivation of the thesis and introduction of the memristive devices including device switching mechanism and its interrelation with other circuit parameters. The remainder of this thesis report is organized as follows:

In Chapter 2, we have discussed the analytical modelling, physical modelling and experimental demonstration for the Y_2O_3-based memristive crossbar array, in detail. Analytical model consists two internal state variables introduced in time derivative of the internal state variable ($w(t)$) and according formulated the differential equations of forgetting rate and retention. 3-D electrothermal physical model has been created and studied the switching response of symmetric and asymmetric electrodes combinations along with the synaptic behavior. Obtained experimental data fitted with analytically generated.

In Chapter 3, we have discussed results of proposed analytical model which involves study of effect of newly introduced internal state variable, namely *viz* the forgetting rate (τ) and retention (t_r) and results exhibit a stable pinched hysteresis loop in the resistive switching (RS) responses in symmetric and asymmetric electrodes combinations with an efficient ON/OFF current ratio of numerical model RRAM.

In Chapter 4, Conclusion and Future Work.

References

[1] Naous R, AlShedivat M, Neftci E, Cauwenberghs G and Salama K N 2016 Memristor-based neural networks: synaptic versus neuronal stochasticity AIP Adv. 6 111304

[2] Thomas A 2013 Memristor-based neural networks J. Phys. D: Appl. Phys. 46 093001

[3] Citri A and Malenka R C 2008 Synaptic plasticity: multiple forms, functions, and mechanisms Neuropsychopharmacol. Rev. 33 18–41

[4] Chang T, Jo S-H, Kim K-H, Sheridan P, Gaba S and Lu W 2011 Synaptic behaviors and modeling of a metal oxide memristive device Appl. Phys. A 102 857–63

[5] Jo S H, Chang T, Ebong I, Bhadviya B, Mazumder P and Lu W 2010 Nanoscale memristor device as synapse in neuromorphic systems Nano Lett. 10 1297–301

[6] Kim S, Lim M, Kim Y, Kim H-D and Choi S-J 2018 Impact of synaptic device variations on pattern recognition accuracy in a hardware neural network Sci. Rep. 8 2638

[7] Hwang H-G, Woo J-U, Lee T-H, Park S-M, Lee T-G, Lee W-H and Nahm S 2020 Synaptic plasticity and preliminary-spike-enhanced plasticity in a CMOS compatible Ta2O5 memristor Mater. Des. 187 108400

[8] Covi E, Brivio S, Serb A, Prodromakis T, Fanciulli M and Spiga S 2016 HfO2-based memristors for neuromorphic applications IEEE Int. Symp. On Circuits and Systems (ISCAS) vol 16226481 pp 393–6

[9] Chang T 2012 Tungsten oxide memristive devices for neuromorphic applications PhD Thesis University of Michigan

[10] Snider G S 2008 Cortical computing with memristive nanodevices SciDAC Rev. 10 58–65 [11] Jo S H, Kim K-H and Lu W 2009 High-density crossbar arrays based on a Si memristive system Nano Lett. 9 870–4

[12] Tan T, Du Y, Cao A, Sun Y, Zhang H and Zha G 2018 Resistive switching of the HfOx/HfO2 bilayer heterostructure and its transmission characteristics as a synapse RSC Adv. 8 41884–91

[13] Wu Q, Wang H, Luo Q, Banerjee W, Cao J, Zhang X, Wu F, Liu Q, Li L and Liu M 2018 Full imitation of synaptic metaplasticity based on memristor devices Nanoscale 10 5875–81

[14] Chen L, Zhou W, Li C and Huang J 2021 Forgetting memristors and memristor bridge synapses with long-and short-term memories Neurocomputing 456 126–35

[15] Chen L, Li C, Huang T, Chen Y, Wen S and Qi J 2013 A memristor model with forgetting effect Phys. Lett. A 377 3260–5

[16] Strukov, D., Snider, G., Stewart, D. et al. The missing memristor found. Nature 453, 80–83 (2008). https://doi.org/10.1038/nature06932.

[17] Dongale TD. Development of High Performance Memristor for Resistive Random Access Memory Application [Thesis]. Kolhapur Maharashtra, India: Shivaji University; 2015

[18] Georgiou PS. A Mathematical Framework for the Analysis and Modelling of Memristor Nanodevices [Thesis]. London: Chemistry of Imperial College London; 2013

[19] Kavehei O. Memristive Devices and Circuits for Computing, Memory, and Neuromorphic Applications [Thesis]. Australia: The University of Adelaide; 2011

[20] Adhikari S, Sah M, Kim H, Chua L. Three fingerprints of memristor. IEEE Transactions on Circuits and Systems I: Regular Papers. 2013;60(11):3008-3021. DOI: 10.1109/TCSI.2013. 2256171

[21] Chua LO. Resistance switching memories are memristors. Applied Physics A. 2011;102:765-783. DOI: 10.1007/s00339-011-6264-9

[22] R. Waser, and M. Aono, "Nanoionics-based resistive switching memories", Nature Materials, vol. 6, no. 11, 2007, DOI: 10.1038/nmat2023.

[23] K. Szot, W. Speier, G. Bihlmayer, and R. Waser, "Switching the electrical resistance of individual dislocations in single-crystalline $SrTiO_3$", Nature Materials, vol. 5, no. 4, 2006, DOI: 10.1038/nmat1614.

[24] International Technology Roadmap for Semiconductor (ITRS), 2015, Source: https://www.semiconductors.org/resources/2015-international-technology-roadmap-for-semiconductors-itrs/

[25] H. Y. Chen, S. Yu, B. Gao, P. Huang, J. Kang, and H. S. P. Wong, "HfO_x based vertical resistive random-access memory for cost-effective 3D cross-point architecture without cell selector", IEEE International Electron Devices Meeting (IEDM, 2012, San Francisco, CA, USA, DOI: 10.1109/IEDM.2012.6479083.

[26] H. Akinaga, and H. Shima, "Resistive random-access memory (ReRAM) based on metal oxides", Proc. IEEE vol. 98, no. 12, 2010, DOI: 10.1109/JPROC.2010.2070830

[27] S. Park, H. Kim, M. Choo, J. Noh, A. Sheri, S. Jung, K. Seo, J. Park, S. Kim, W. Lee, J. Shin, D. Lee, G. Choi, J. Woo, E. Cha, J. Jang, C. Park, M. Jeon, B. Lee, B. H. Lee, and H. Hwang, "RRAM-based synapse for neuromorphic system with pattern recognition function", IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2012, DOI: 10.1109/IEDM.2012.6479016.

[28] S. Park, A. Sheri, J. Kim, J. Noh, J. Jang, M. Jeon, B. Lee, B. R. Lee, B. H. Lee, and H. Hwang, "Neuromorphic speech systems using advanced RRAM-based synapse", IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 2013, DOI: 10.1109/IEDM.2013.6724692.

[29] Zhang, X.; Xu, L.; Zhang, H.; Liu, J.; Tan, D.; Chen, L.; Ma, Z.; Li, W. E_ect of Joule Heating on Resistive Switching Characteristic in AlOx Cells Made by Thermal Oxidation Formation. Nanoscale Res. Lett. 2020, 19, 3229-1–3229-19.

[30]. Tsuruoka, T.; Hasegawa, T.; Terabe, K.; Aono, M. Conductance quantization and synaptic behavior in a Ta2O5-based atomic switch. Nanotechnology 2012, 23, 435705–435711.

[31] Sun, P.; Li, L.; Lu, N.; Li, Y.; Wang, M.; Xie, H.; Liu, S.; Liu, M. Physical model of dynamic Joule heating e_ect for reset process in conductive-bridge random access memory. J. Comput. Electron. 2014, 13, 432–438.

[32] Zhang, T.; Ou, X.; Zhang, W.; Yin, J.; Xia, Y.; Liu, Z. High-k-rare-earth-oxide Eu2O3 films for transparent resistive random access memory (RRAM) devices. J. Phys. D Appl. Phys. 2014, 47, 065302–065308.

[33] Chen, K.J.; Liu, J.; Wang, Y.; Yang, H.; Ma, Z.; Huang, X. VCM Conductive defect states based filament in MOM structure RRAM. IEEE Electron. Device Lett. 2018, 9, 1–4.

[34] Kwon, D.H.; Kim, K.M.; Jang, J.H.; Jeon, J.M.; Lee, M.H.; Kim, G.H.; Li, X.S.; Park, G.S.; Lee, B.; Han, S.; et al. Atomic structure of conducting nanofilaments in TiO2 resistive switching memory. Nat. Nanotechnol 2010, 5, 148–153.

[35] Xue, W.; Liu, G.; Zhong, Z.; Dai, Y.; Shang, J.; Liu, Y.; Yang, H.; Yi, X.; Tan, H.; Pan, L.; et al. A 1D Vanadium Dioxide Nanochannel Constructed via Electric-Field-Induced Ion Transport and its Superior Metal-Insulator Transition. Adv. Mater. 2017, 29, 1702162(1)–1702162(9).

[36] Lee, S.; Sohn, J.; Jiang, Z.; Chen, H.Y.; Philip Wong, H.S. Metal oxide-resistive memory using graphene-edge electrodes. Nat. Commun. 2015, 6, 8407–8413.

[37] Munjal, S.; Khare, N. Valence Change Bipolar Resistive Switching Accompanied With Magnetization Switching in CoFe2O4 Thin Film. Sci. Rep. 2017, 7, 12427–12436.

[38]. Ye, C.;Wu, J.; He, G.; Zhang, J.; Deng, T.; He, P.; Wang, H. Physical Mechanism and Performance Factors of Metal Oxide Based Resistive Switching Memory: A Review. J. Mater. Sci. Technol. 2016, 32, 1–11.

[39] Yu, D.; Liu, L.F.; Chen, B.; Zhang, F.F.; Gao, B.; Fu, Y.H.; Liu, X.Y.; Kang, J.F.; Zhang, X. Multilevel resistive switching characteristics in Ag/SiO2/Pt RRAM devices. IEEE Electron. Device Lett. 2011, 11, 1–4.

[40] Tsuruoka, T.; Terabe, K.; Hasegawa, T.; Aono, M. Forming and switching mechanisms of a cation-migrationbased oxide resistive memory. Nanotechnology 2010, 21, 425205–425213.

[41] Guo, T.; Sun, B.; Zhou, Y.; Zhao, H.; Lei, M.; Zhao, Y. Overwhelming coexistence of negative di_erential resistance e_ect and RRAM. Phys. Chem Chem Phys. 2018, 20, 20635–20640.

[42]. Long, S.B.; Liu, Q.; Lv, H.B.; Li, Y.T.; Wang, Y.; Zhang, S.; Lian, W.-T.; Liu, M. Resistive switching mechanism of Cu doped ZrO2-based RRAM. IEEE Electron. Device Lett 2010, 5, 1–4.

[43] Long, S.; Liu, Q.; Lv, H.; Li, Y.;Wang, Y.; Zhang, S.; Lian,W.; Zhang, K.;Wang, M.; Xie, H.; et al. Resistive switching mechanism of Ag/ZrO2:Cu/Pt memory cell. Appl. Phys. A 2011, 102, 915–919.

[44] Yuan, F.; Shen, S.; Zhang, Z.; Pan, L.; Xu, J. Interface-induced two-step RESET for filament-based multi-level resistive memory. Superlattices Microstruct. 2016, 91, 90–97.

[45] Gao, S.; Zeng, F.; Chen, C.; Tang, G.; Lin, Y.; Zheng, Z.; Song, C.; Pan, F. Conductance quantization in a Ag filament-based polymer resistive memory. Nanotechnology 2013, 24, 335201–335208.

Chapter 2

Analytical, Physical and Experimental Demonstration

In this chapter, we discussed Analytical, physical and experimental demonstration in detail. Firstly, discussed the detailed description of already existing, non-linear analytical memristive model, which is based on interfacial switching mechanism and confabulate the current-voltage equation, its effect on the V-I characteristics and other part includes the proposed modified analytical model in which 2 novel the internal state variable ($w(t)$) and two important parameters, namely *viz* the forgetting rate (τ) and retention (t_r) to emulate the retention and forgetting behavior of the memristive crossbar array. Next section, discussed the developed physical model of memristor which was modelled on physics-based software i.e., COMSOL Multiphysics with a defined MATLAB script and effect of symmetric and asymmetric electrode variation on the resistive switching properties of the nanoscale Y_2O_3-based memristor devices is also investigated. Lastly, experimental section is discussed in detail in which fabrication process to realize the Y_2O_3-based memristive crossbar array using the DIBS system is weighed up and done the R^2-fitting accuracy of 99.2% with corresponding experimentally obtained data of the fabricated crossbar array with analytically obtained data from the model.

2.1 Analytical Model for Memristive Systems for Neuromorphic Computation

2.1.1 Current-Voltage Equation

Equation (1) describes the current-voltage (I-V) relationship for the Non-Linear Analytical model which is nearly related to the equations of the model reported by Yang at al [3].

$$I(t) = \begin{Bmatrix} b_1 w^{a_1} \left(e^{\alpha_1 V_i(t)} - 1\right) + \chi\left(e^{\gamma V_i(t)} - 1\right), V_i(t) \geq 0 \\ b_2 w^{a_2} \left(e^{\alpha_2 V_i(t)} - 1\right) + \chi\left(e^{\gamma V_i(t)} - 1\right), V_i(t) < 0 \end{Bmatrix} \quad (1)$$

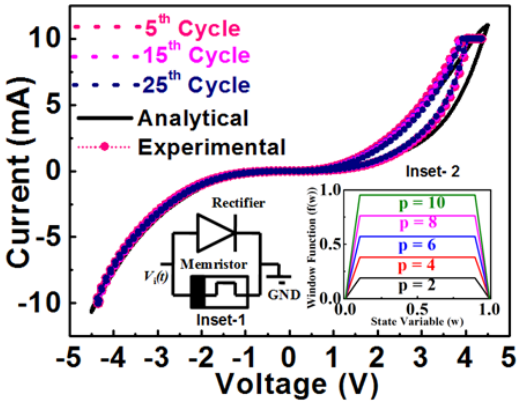


Figure 2.1: Resistive switching characteristic of a memristive device (sweep rate: 1.042 V s−1). Inset-1 and inset-2 show parallel connection of rectifier and memristor and piecewise window function, respectively.

The first term on the right side of equation (1) describes the flux-controlled memristive behavior and it is dominated by the interfacial switching mechanism which is not incorporated by various previously reported models [1, 3, 4]. The parameters a_1 and a_2 are the degrees of influence of the state variable on current for positive and negative voltage biases, respectively and also contribute in the control of loop area of the hysteresis loop. b_1 and b_2 are the experimental fitting parameters which define the slope of conductivity in I–V characteristics, w is the state variable,

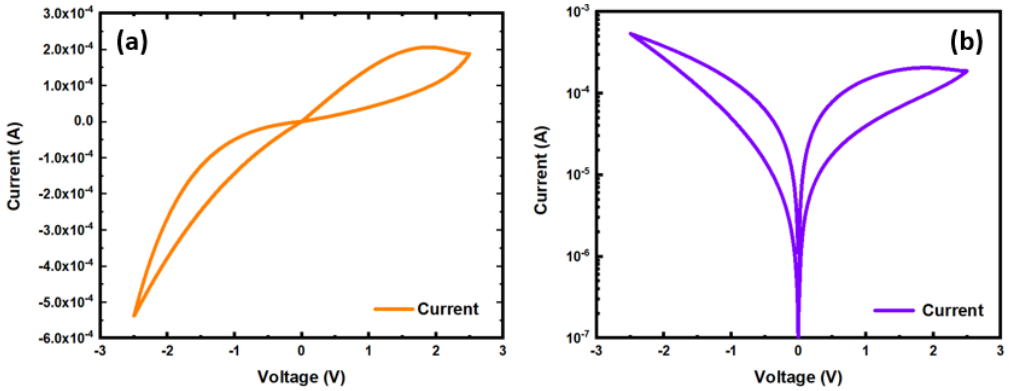


Figure 2.2: (a) I-V Characteristics (b) Log(I) -V Characteristics.

α_1 and α_2 are the major hysteresis loop area controlling parameters. The second term on the right side of equation (1) is linked with the ideal diode behavior in I–V characteristics which plays a vital role when the state variable (w) approaches zero i.e., non-conducting state or OFF state and parameters χ and γ denote the net electronic barrier of the memristive device. $V_i(t)$ is the applied input voltage and in the case of I–V characteristics, a triangular waveform and while in the case of synaptic functionality, rectangular voltage pulses are used. Analytical model is applicable for both unipolar and bipolar memristive systems while previously reported models [2, 3] are utilized only for bipolar memristive system.

2.1.2 Window Function

A new piecewise window function, f (w) is described by equation (2), as shown in the inset of Figure 1, which ensures that the state variable (w) is limited between 0 and 1. In the analytical modeling, a constant value of p=2 is used. The range of parameter p defines the limit of the f (w) $\in$ {0, 1} (seen in Figure 2.3) and if the value of p > 10, the upper limit of the f (w) is beyond 1 thus violating the essential conditions reported by Prodromakis et al [2]:

$$f(w) = log\begin{Bmatrix}(1+w)^P,\ 0 \le w \le 0.1\\ (1.1)^P,\ 0.1 < w \le 0.9\\ (2-w)^P, 0.9 < w \le 1\end{Bmatrix} (2)$$

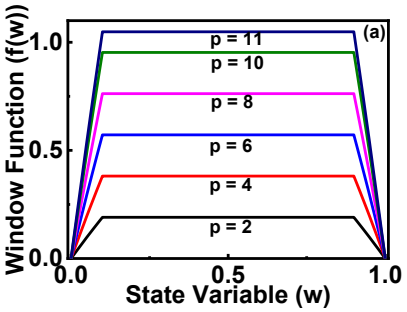


Figure 2.3: Piecewise window function.

2.1.3 Time-Derivative Equation of State Variable

The time derivative of the state variable (w(t)) is governed by the equation (3) in which it depicts the rate of variation of the state variable with respect to time in the memristive devices and depends upon the nature of input voltage and window function.

$$\frac{dw}{dt} = A \times V_i^m(t) \times f(w) \qquad (3)$$

where, A and m are the parameters that determine the dependence of the state variable on the input voltage and m is always an odd integer to ensure that the opposite polarity of the applied voltage leads to opposite change in the rate of change of state variable. Table 1 presents the physical significance and numerical values of all parameters used in analytical modeling.

Table 1. Physical interpretation and values of parameters for analytical modeling.

Parameters	**Values for Y_2O_3**	**Physical Significance**
b_1	1.59×10^{-3}	Experimental fitting parameters
b_2	-6.2	Experimental fitting parameters
a_1	1.2	Degrees of influence of the state variable under positive bias
a_2	0.3	Degrees of influence of the state variable under negative bias
α_1	0.60	Hysteresis loop area controlling parameters under positive bias
α_2	-0.68	Hysteresis loop area controlling parameters under negative bias

χ	1 x 10^{-11}	Magnitude of ideal diode behavior
γ	1	Diode parameters like thermal voltage and ideality factor
A	5 x 10^{-4}	Control the effect of the window function
m	5	Control the effect of input on the state variable
P	0<P≤10	Bounding parameter for window function between 0 and 1

2.2 Analysis of the Proposed Analytical Model Synaptic Learning

2.2.1 Current-Voltage Equation

Equation (4) describes the current–voltage (*I–V*) relationship that governs the switching characteristics of the augmented Y_2O_3-based memristor [9]:

$$I(t) = \begin{Bmatrix} b_1 w^{a_1} \left(e^{\alpha_1 V_i(t)} - 1\right) + \chi\left(e^{\gamma V_i(t)} - 1\right), V_i(t) \geq 0 \\ b_2 w^{a_2} \left(e^{\alpha_2 V_i(t)} - 1\right) + \chi\left(e^{\gamma V_i(t)} - 1\right), V_i(t) < 0 \end{Bmatrix} \quad (4)$$

Here, the first term described on the right-hand side of (4) is associated with the flux-controlled memristive behavior due to the interfacial switching mechanism and is not reported in previously reported models [14–15]. Here, the parameters a_1 and a_2 determine the degrees of influence of the state variable on the device current for positive and negative polarities of the applied bias voltage, respectively. b_1 and b_2 are designated as the experimental fitting parameters, which describe the conductivity slope in resistive switching characteristics. w is the internal state variable, and α_1 and α_2 are the pinched hysteresis loop area controlling parameters. The second term on the right-hand side of (4) stands for the ideal diode behavior

in resistive switching characteristics and plays a key role when the internal state variable (w) approaches zero, and parameters χ and γ denote the net electronic barrier of the memristive device. Vi(t) is the applied input bias voltage.

2.2.2 Window Function

A piecewise window function $f(w)$ is utilized as described in equation (5) [9]. The window function ensures that w is restricted between 0 and 1. In the analytical modeling, a constant value of $p = 2$ is used. The value of the parameter p helps one to limit the value of $f(w)\varepsilon\ \{0, 1\}$. However, for $p >$ 10, the upper limit of $f(w)$ is beyond 1, and thus violates the essential conditions for $f(w)$, which is defined between 0 and 1, as reported by Kumar *et al* [7] and Prodromakis *et al* [10]:

$$f(w) = log\begin{Bmatrix}(1+w)^P,\ \ 0 \le w \le 0.1\\ (1.1)^P,\ \ 0.1 < w \le 0.9\\ (2-w)^P, 0.9 < w \le 1\end{Bmatrix} \qquad (5)$$

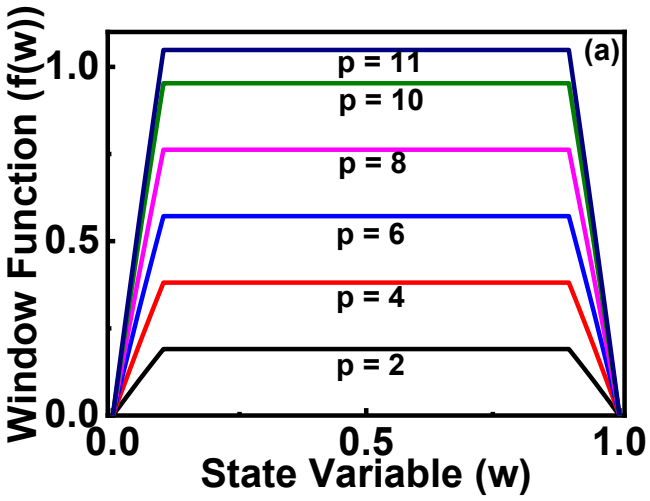


Figure 2.4: Piecewise window function.

2.2.3 Modified Time-Derivative Equation of State Variable

Equation (6) describes the time derivative of the internal state variable ($w(t)$) [9] and is further modified by incorporating two important parameters, namely *viz* the forgetting rate (τ) and retention (t_r) to emulate the retention and forgetting behavior of the memristive crossbar array. The time derivative of the ($w(t)$) is dependent on the nature of the input voltage, window function and forgetting and retention terms of the memristive crossbar model. However, the previously reported model [6] has not been experimentally validated for the switching response of the memristive crossbar array:

$$\frac{dw}{dt} = \left\{A \times V_i^m(t) \times f(w) - \left(\frac{w-t_r}{\tau}\right)\right\} \quad (6)$$

where A and m are the parameters that define the dependence of the state variable on the input voltage, and m ensures that the opposite polarity of the applied voltage leads to an opposite change in the rate of change of the state variable. The last term on the right-hand side of (6) is associated with the memory forgetting rate (τ) and retention (tr) behavior of the memristive device.

2.2.3 Proposed Internal State Variables

The voltage derivative of forgetting rate and retention can be defined by (7) and (8), respectively:

$$\frac{d\tau}{dt} = \theta(e^{\eta 1v} - e^{-\eta 2v}) \quad (7)$$

$$\frac{dt_r}{dt} = \sigma(e^{\eta 1v} - e^{-\eta 2v}) \times f(w) \quad (8)$$

where η_1 expresses the interface effect with positive and negative voltage and is considered as positive-valued fitting parameter, and η_2 represents the material properties, such as activation energy [5]. The value of t_r is limited between 0 and 1, i.e., $t_r \in [0, 1]$, and σ and ϑ are the corresponding

parameters for tr and τ and are considered as constants during the analytical modeling.

Equations (7) and (8) are used to accurately model the synaptic plasticity; more specifically, the STM and LTM properties. The value of τ denotes the forgetting rate, which is greater than 0 ($\tau > 0$), and ϑ and σ are always positive-valued parameters to analyze the forgetting rate and the retention behavior of the memristive crossbar array systems. Table 2 presents the physical interpretation and numerical values of all parameters used in the analytical modeling.

Table 2. Modeling parameter values and their physical interpretation.

Parameters	**Values**	**Physical interpretation**
b_1	1.59×10^{-3}	Experimental fitting parameters
b_2	-6.2×10^{-4}	Experimental fitting parameters
a_1	1.2	Degrees of influence of the state variable under positive bias
a_2	0.3	Degrees of influence of the state variable under negative bias
α_1	0.60	Hysteresis loop area controlling parameters under positive bias
α_2	-0.68	Hysteresis loop area controlling parameters under negative bias
χ	10^{-11}	Magnitude of ideal diode behavior
γ	1	Diode parameters such as thermal voltage and ideality factor

A	5×10^{-4}	Control the effect of the window function
m	5	Control the effect of input on the state variable
p	$0 < p \leqslant 10$	Bounding parameter for window function between 0 and 1
τ	0.15	Forgetting rate
t_r	0.1	Retention; *t*r ε [0,1]z
σ	10^{-6}	Corresponding parameters for *t*r and τ
θ	10^{-7}	Corresponding parameters for *t*r and τ
η_1	4	Interface effect with positive and negative voltage and independent of *w*
η_2	2	Interface effect with positive and negative voltage with positive-valued parameters and determined by the SL material properties and independent of *w*

2.3 Analysis of the Physical Electro-Thermal Modelling

2.3.1 Numerical Electro-Thermal Model and Specification

As Figure 2.5 (a-b) represents the 2D axisymmetric model of the memristor in COMSOL for RESET (or OFF) and SET (or ON) processes,

respectively. The 2D geometry of memristive device in COMSOL helps to reduce the volume integrals in equation (9) to area integrals.

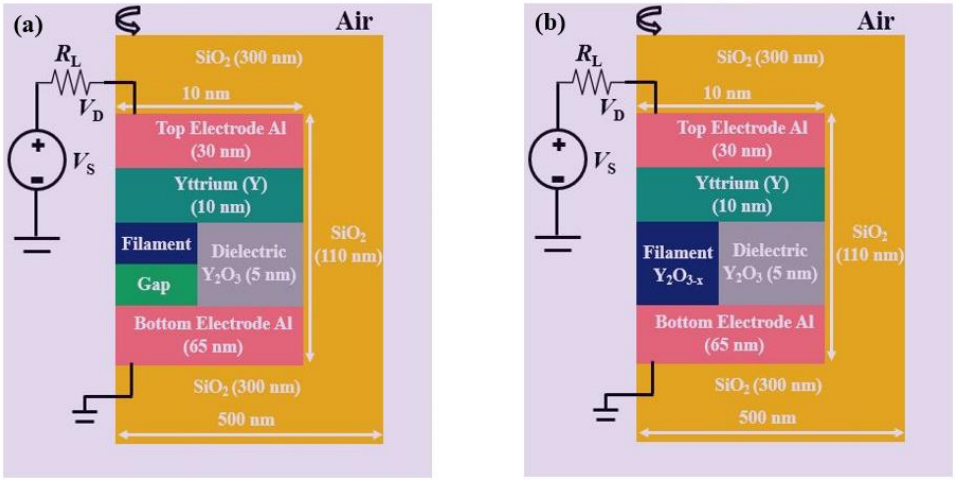


Figure 2.5: (a) 2D structure of memristive device under SET operation, and (b) 2D structure of memristive device under RESET operation. In addition, the sketches indicate number of boundary conditions, materials, and regular parameters. (Figures are not sketched to their true scales)

Resistive Switching equivalent to the SET process is an amalgamation of 2 processes:

- Formation of filament between the electrodes.
    - Nucleation and
    - Longitudinal growth of CFs due to their probabilistic nature [15]
- Radial development of Conducting Filament.

Equivalently, Resistive Switching for RESET process is also formed of 2 processes:

- Nucleation and
- Growth of the gap (or rupturing of the CFs). Nature of the growth of the gap is also of stochastic nature [15].

As seen from Fig. 1(a-b), a layer of SiO_2 is used as a thermally insulated layer surrounding the memristor device. The yttrium metal used as an

oxygen reservoir layer and enhance the formation of stable CFs during the SET process. The numerical analysis is rooted on the concept of minimum free energy (FE) of memristive device which increases on the application of external voltage. At the same time, the device evolves in such a way to minimize its free energy due to phase transition in oxide material by braking chemical bonds. The free energy in a memristive device can be expressed as [16]:

$$F = \int \rho C_{\mathrm{P}}\, \delta T dx^3 + \frac{1}{2}\int \varepsilon |E|^2 dx^3 + 2\pi r h \sigma_{\mathrm{S}} + \pi r^2 h \delta \mu \qquad (9)$$

The area integrals associated with SET and RESET processes in COMSOL are expressed as [16-17]:

$$F_{\mathrm{SET}} = \iint \rho C_P \delta T dr dz + \frac{1}{2}\iint \varepsilon |E|^2 dr dz + 2\pi r h \sigma_S + \pi r^2 h \delta \mu_1 \quad (10)$$

$$F_{\mathrm{RESET}} = \iint \rho C_P \delta T dr dz + \frac{1}{2}\iint \varepsilon |E|^2 dr dz + 2\pi r h \sigma_S + \pi r^2 l \delta \mu_2 \quad (11)$$

where, ρ is the mass density, C_{p} is the specific heat capacity at constant pressure, δT is the change in temperature, ε is the permittivity, E is the electric field, r is the radius of conducting filament, h is the conducting filament height in SET process (referred as: l is gap length in the case of RESET process), σ_{s} is the interfacial energy, and δ_μ is the difference in chemical potential between unstable conductive phase and insulating phase during SET process ($\delta_{\mu 1}$) and between unstable conductive phase and metastable conductive phase during RESET process ($\delta_{\mu 2}$) [16-17].The first and second terms of equation (9) describe the thermal and electrostatic energy, respectively, while the last two terms of equation (9) can be correlated to the phase transformation energy.

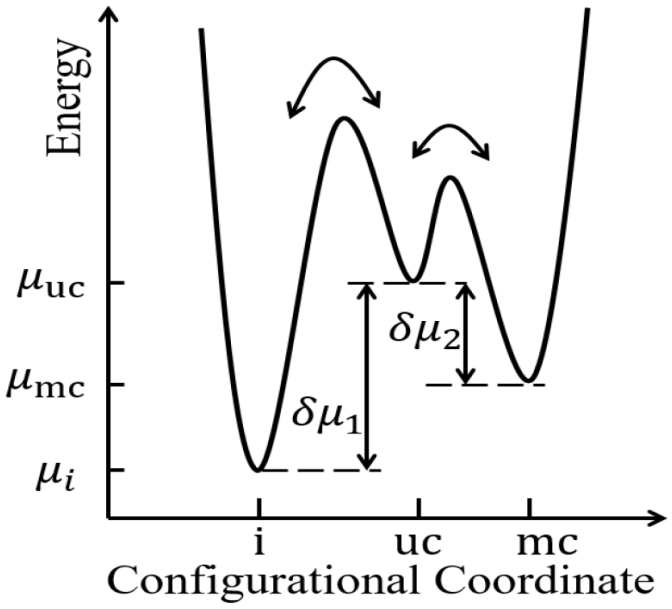


Figure 2.6: One dimensional (1D) presentation of the system where chemical potentials in unspecified configurational coordinates showing three distinct minima corresponding to the insulating (i), unstable conductive (uc), and metastable conductive (mc) phases and their related barriers. Arrows represent transformations between mc and uc and the uc and i phases where energy barriers are relatively low [18].

2.3.2 Implementation in COMSOL Multiphysics:

2.3.2.1 COMSOL Algorithm:

1. Open the COMSOL Model Wizard.
2. Select 2D Axisymmetric in Space Dimension section.
3. Select AC/DC module
    - add Electric Currents submodule.
    - electrical Circuit submodules.
4. Select Heat Transfer Module
    - add Heat Transfer in Solids submodule.
5. Select Done.
6. Create Geometry of the device from schematic as shown in Figure 2.5.
7. Add Blank Materials in the Materials junction and add material properties from Table 3.
8. Add the temperature-dependent electric conductivity,

- In Definitions junction, select Functions then Interpolation, and then insert temperature and corresponding conductivity values in the given Table 3.
- Select Linear for both Interpolation and Extrapolation option.

9. Add the temperature and voltage dependent hopping conductivity,
    - In Definitions junction, select Variables, add the formula from Table 3, and then select the corresponding domain.
10. Select the materials to the respective domains.
11. In Electric Currents submodule
    - add Terminal boundary condition.
    - select the top boundary of the top electrode.
    - select Circuit as the Terminal type.
    - add Ground boundary condition.
    - select the bottom boundary of the bottom electrode.
12. In Electric Circuit submodule,
    - add Resistor and value of load resistance,
    - add External I Vs. U from External Coupling.
    - select Terminal voltage from Electric potential option.
    - add Voltage Source for OFF and ON modules.
    - select Pulse source as Source type for ON and OFF modules and define the pulse length according to the different ramp-rate as listed in Table. III
    - Add Current Source for RESET and SET modules.
    - select DC-Source as Source type for SET and RESET modules.
13. In Heat Transfer in Solids submodule,
    - add Temperature boundary condition.
    - select the top of the SiO2 superstrate and bottom boundary of the SiO2 substrate.
    - add Diffusive Surface boundary condition.
    - select all the inner boundaries, and then choose 298K in the user defined temperature section and 0.9 Surface emissivity for the user defined value.

14. In Multiphysics node, to couple the Electric Currents and Heat Transfer in Solids submodule,
    - select all the domains and boundaries in Electromagnetic Heating sub-node.
    - select Heat Transfer in Solid as Source and Electric Currents as Destination in Temperature sub-node
15. Create Mesh
    - select Build All
16. Select Study type
    - select Time Dependent study for ON and OFF modules.
    - add Times corresponding to the pulse lengths.
    - select Stationary study for SET and RESET modules.
17. Select Compute
18. Obtain results from the Results node as shown in Figure (2.7-2.10)

The following sections describe the modules that are considered during the model's process in COMSOL:

[i] Electric Current Module:

$$\nabla . J = 0 \qquad (12)$$

$$J = \sigma E \qquad (13)$$

$$E = -\nabla V \qquad (14)$$

where E represents the electric field, J depicts the electric current density, ∇. shows the divergence operator, ∇ defines the three-dimensional gradient operator, and V denotes the electric potential.

[ii] Heat Transfer Module (solids):

$$-\kappa \nabla^2 T = Q_S \qquad (15)$$

$$\rho C_P \frac{\partial T}{\partial t} - \kappa \nabla^2 T = Q_S \qquad (16)$$

where absolute temperature in Kelvin is given by T, k is the thermal conductivity, the specific heat capacity is depicted by C_P, the

electromagnetic heat source is given by Q_S, and the density is represented by ρ.

[iii] Multiphysics Module:

$$Q_S = J.E \qquad (17)$$

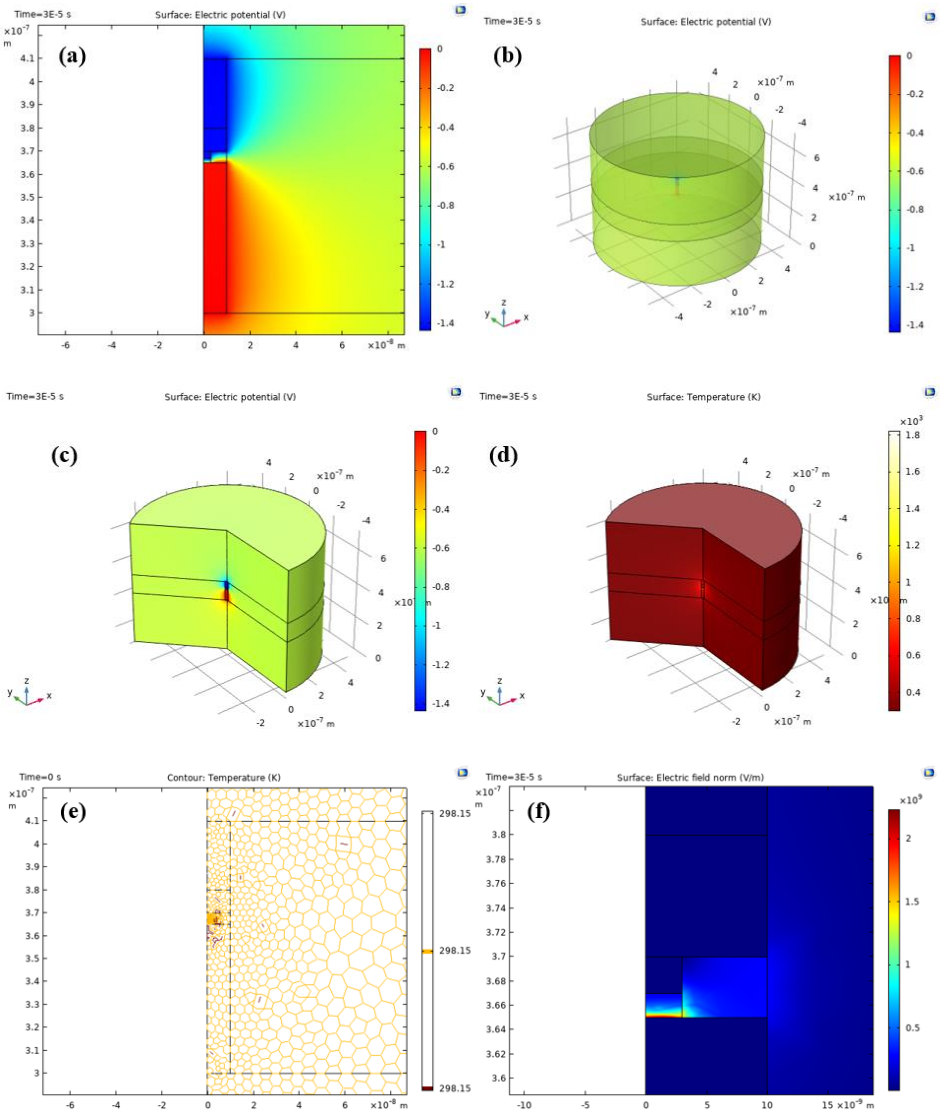


Figure 2.7: (a) 2-D Electric Potential Plot. (b) 3-D Electric Potential Plot. (c) 3-D Electric Potential Plot of Cutout section. (d) 3-D Temperature Plot. (e) Temperature Contour Plot. (f) 2-D Electric Field Plot. For the OFF Process.

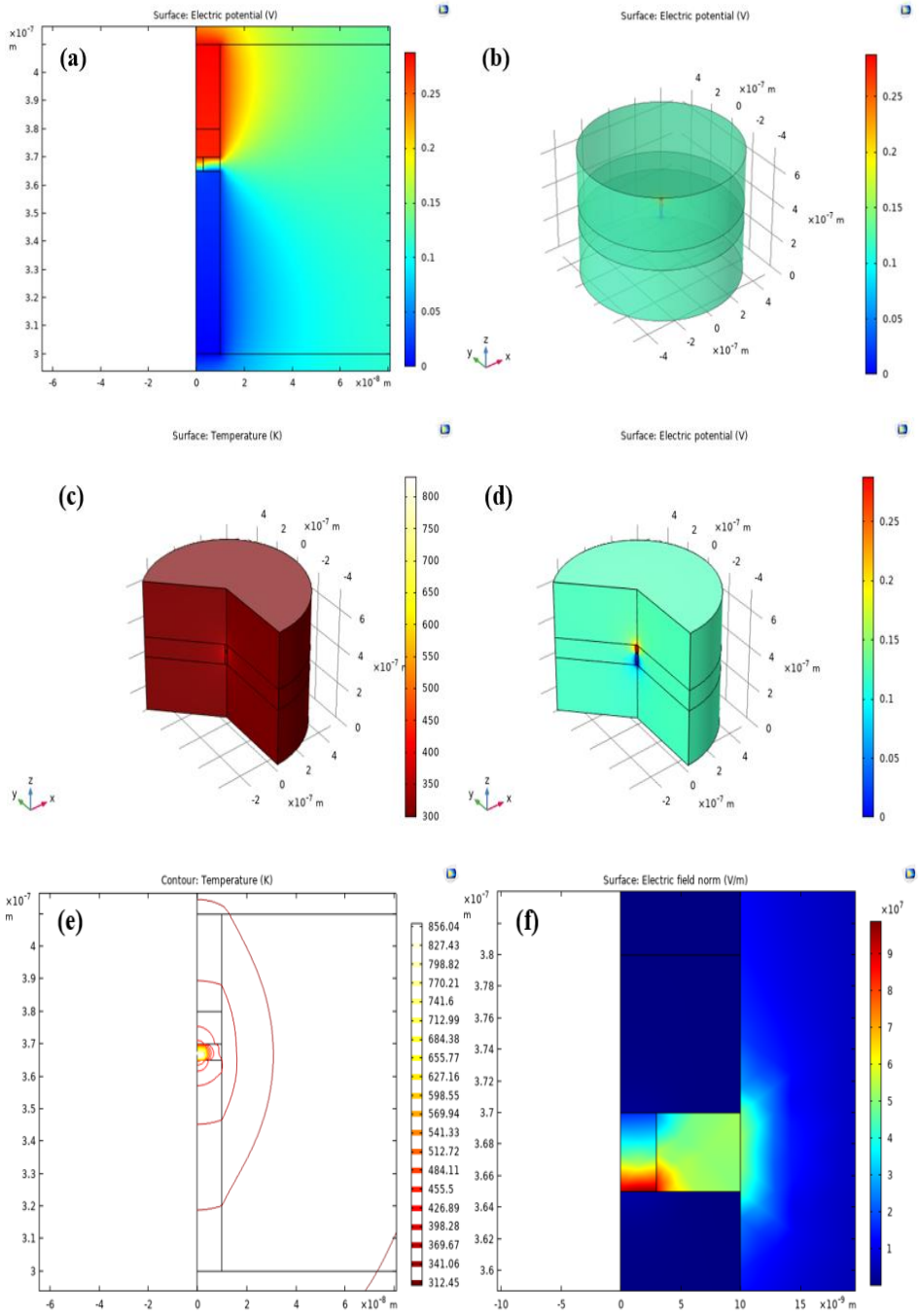


Figure 2.8: (a) 2-D Electric Potential Plot. (b) 3-D Electric Potential Plot. (c) 3-D Electric Potential Plot of Cutout section. (d) 3-D Temperature Plot. (e) Temperature Contour Plot. (f) 2-D Electric Field Plot. For the SET Process.

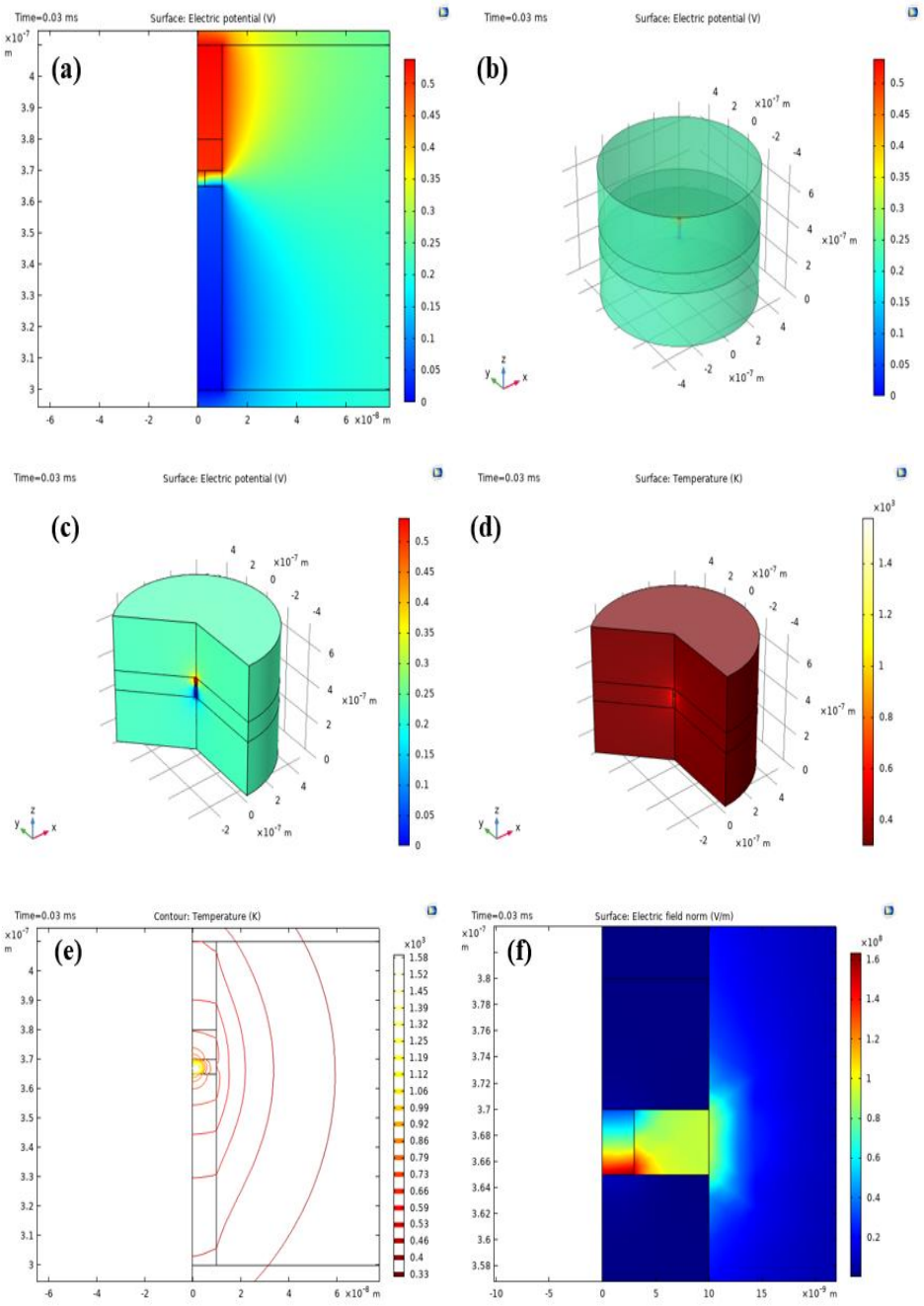


Figure 2.9: (a) 2-D Electric Potential Plot. (b) 3-D Electric Potential Plot. (c) 3-D Electric Potential Plot of Cutout section. (d) 3-D Temperature Plot. (e) Temperature Contour Plot. (f) 2-D Electric Field Plot. For the ON Process.

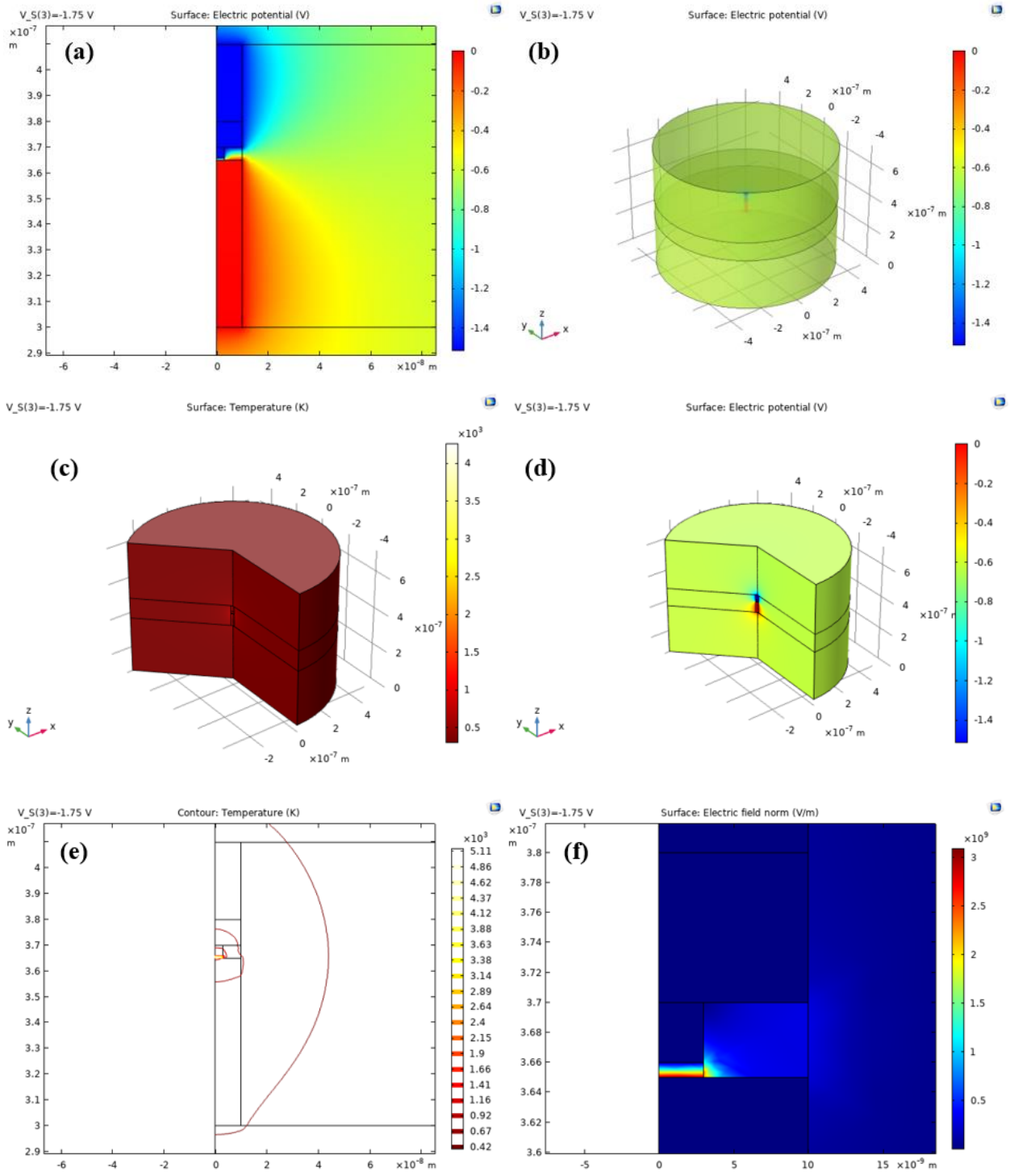


Figure 2.10: (a) 2-D Electric Potential Plot. (b) 3-D Electric Potential Plot. (c) 3-D Electric Potential Plot of Cutout section. (d) 3-D Temperature Plot. (e) Temperature Contour Plot. (f) 2-D Electric Field Plot. For the RESET Process.

Table 3: Values of the coefficients of the differential equations and FE used in electro-thermal modelling

Materials	Electrical Conductivity (σ) [S/m]		Thermal Conductivity (κ) [W/K.m]	Specific Heat Capacity [J/kg. K]	Relative Permittivity ($\boldsymbol{\varepsilon_r}$)	Mass Density (ρ) [kg/m^3]
SiO_2	1×10^3		1.38	703	3.9	2.20×10^3
Al	3.8×10^7		235	904	-∞[1]	2.70×10^3
Y	1.8×10^6		17	298	-∞[1]	4.47×10^3
Y_2O_3	10^{-11}		0.3	440	15	5.01×10^3
Y_2O_{3-x}	$\sigma_{if}\exp\left(\sigma_f \ln\left(\frac{t}{t_i}\right)\right)\exp\left(\sqrt{\frac{eV}{kT}}\right)$		$\sigma_c(T,V)TL$	528	-∞[1]	6.01×10^3
Gap	$\sigma_{ig} exp\left(-\sigma_g ln\left(\frac{t}{t_i}\right)\right) exp\left(\sqrt{\frac{eV}{kT}}\right)$		$k_{eff}\sigma_c(T,V)TL$	440	15	5.01×10^3
TiN	1.00×10^6		11.9	543.33	-∞[1]	5.22×10^3
Cu	5.90×10^7		400	386	-∞[1]	8.96×10^3
Au	4.50×10^7		320	126	-∞[1]	1.93×10^4
Pd	9.49×10^6		71.2	240	-∞[1]	1.20×10^4
Ag	6.20×10^7		430	233	-∞[1]	1.05×10^4
Al	3.80×10^7		235	921	-∞[1]	2.70×10^4
Pt	9.40×10^6		71	125	-∞[1]	2.15×10^4
Mo	2.00×10^7		139	251	-∞[1]	1.03×10^4
Ta	7.70×10^6		57	140	-∞[1]	1.67×10^4
Electrical Conductivity	**Parameters**	**Values**	Circuitry	**Parameters**	**Values**	
	σ_{if}	5 kS/m		R_L	3.1 kΩ	
	σ_{ig}	3 kS/m		$V_{(+)}$	1.5 V	
	α_f	-0.05		$V_{(-)}$	-1.5 V	
	α_g	0.05		$\Lambda(V/s)$	10^2, 10^3,10^6	
	t	V/ λ	Thermal Conductivity (Gap)	k_{eff}	10	
	t_i	0.1ps				

[1]10^6 was used for practical purpose as an alternative to $-\infty$.

2.4 Memristor Device Structure and Modelling

To simulate the Y_2O_3-based memristor structure, symmetric and asymmetric top and bottom electrodes have been utilized, as depicted in Figure 2.11 (a) shows the various symmetric electrodes combinations with Y_2O_3 as a resistive switching layer while Figure 2.11 (b) shows the asymmetric electrodes combinations with Y_2O_3 as a switching layer. The cross-sectional area of the simulated device structure is 314 nm^2. As seen in Figure 2.11, a thick layer of SiO_2 insulating layer is used in which the width of the SiO_2 layer is 490 nm, and top and bottom thickness of 300 nm. The thick layer of SiO_2 acts as a heat shield layer surrounding the memristor device to prevent the uncontrollable heat flow from the device to outside ambient (i.e., air) during the device switching operation [19]. Also, this passivation layer helps to maintain a stable temperature all around the device [20] which is advantageous to achieve the stable resistive switching response of the device. Further, the effective thickness of the memristor device is 100 nm, in which 65 nm thickness is of the bottom electrode (BE),

5 nm thickness of Y_2O_3 which acts as the switching layer, and 30 nm thickness of the top electrode (TE). It should be noted that, in the case of symmetric electrodes combinations, the same metal is used for TE and BE, as depicted in Figure 2.11 (a) while in the case of asymmetric electrodes combinations, active metal Ag is used as a TE and different metals such as Al, Au, Mo, Pd, Ta, and TiN have been used as a BE of the simulated memristor structure, as depicted in Figure 2.11 (b).

On the other hand, the resistive switching (RS) process in the memristor device is majorly categorized into two sections such as 'SET' process and 'RESET' process. The SET process is the combination of two sub-processes such as fast shunting of electrodes and the radial growth of conductive filaments (CFs), as depicted in Figure 2.12 (a) The shunting process can be further divided into two ways such as nucleation and longitudinal growth of CFs due to their stochastic nature [21]. While the RESET process is also categorized into two sub-processes such as nucleation and growth of the gap. The growth of the gap originated due to rupturing of the CFs, as shown in Figure 2.12 (b) The formation of the gap in the RESET process is also of stochastic nature [21].

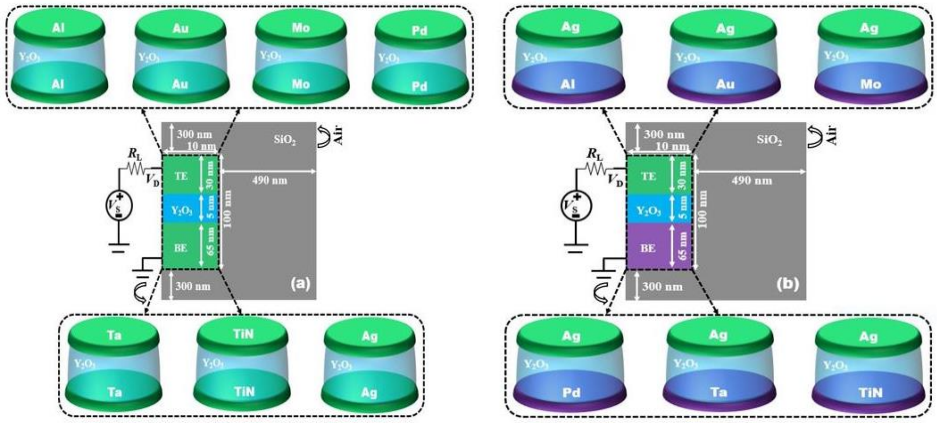


Figure 2.11: Y_2O_3-based memristor device with (a) Symmetric electrodes (similar metal is used for the top and bottom electrodes), (a) Asymmetric electrodes (different metal is used for top and bottom electrodes).

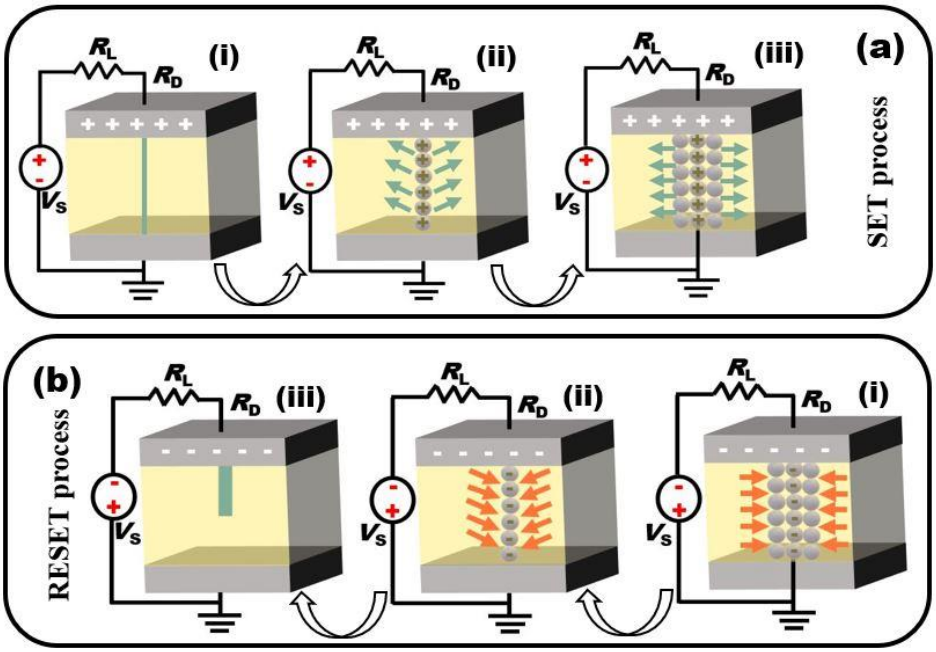


Figure 2.12: Formation and rupture of the CFs in a generic metal-insulator-metal (MIM) memristor device where (a) SET and (b) RESET process.

Here, under the positive applied voltage, step a(i) shows the initial stage of the device and in stage a (ii and iii) the nucleation process is started with radial growth of the CFs and device switches into SET state. On the other hand, under the negative applied voltage, step b(i) shows the shrinkage of CFs and in stage b(ii and iii) the dissolution of CFs is started and due to which the device switches into RESET state. The V_S, R_L and R_D shows the applied input voltage, load resistance and device resistance, respectively.

The simulation of the memristor device is based on the thermodynamic numerical analysis which is further related to the principle of minimum free energy (FE) of the memristor device. The minimum FE increases due to an applied external voltage. However, at the same time, the device evolves in such a way to minimize its free energy due to phase transition in oxide material by breaking chemical bonds. The free energy in a memristor device can be expressed by equation (18) [22].

$$F = \int \rho C_P \, \delta T dx^3 + \frac{1}{2}\int \varepsilon |E|^2 dx^3 + 2\pi r h \sigma_S + \pi r^2 h \delta \mu \qquad (18)$$

where, ρ = mass density, C_p = specific heat capacity at constant pressure, δT = change in temperature, ε = permittivity, E = electric field, r = radius of CF, h = CF height in SET process (l is gap length in the case of RESET

process), σ_s = interfacial energy, and $\delta\mu$ = difference in chemical potential between unstable conductive phase and insulating phase during the SET process ($\delta\mu_1$) and between unstable conductive phase and metastable conductive phase during RESET process ($\delta\mu_2$) [22-23]. The first and second terms of equation (18) are associated with the thermal and electrostatic energies, respectively, while the last two terms of equation (18) can be correlated to the phase transformation energy. The electrostatic energy of the conductive components such as electrodes and filaments are negligible, as compared to that of the insulating layer, which is the dominant candidate for higher capacitance in the memristor device. Hence, the electrostatic energy contribution in the overall value of FE is typically dominated by the insulator layer and the thermal contribution is dominated by the conducting filament that helps in the flow of current through insulating placed between the top and bottom electrodes. A detailed explanation of adopted simulation steps, an algorithm for the device design and the various partial differential equations and their boundary conditions have already been reported in our previous report [24].

2.5 Experimental Demonstration

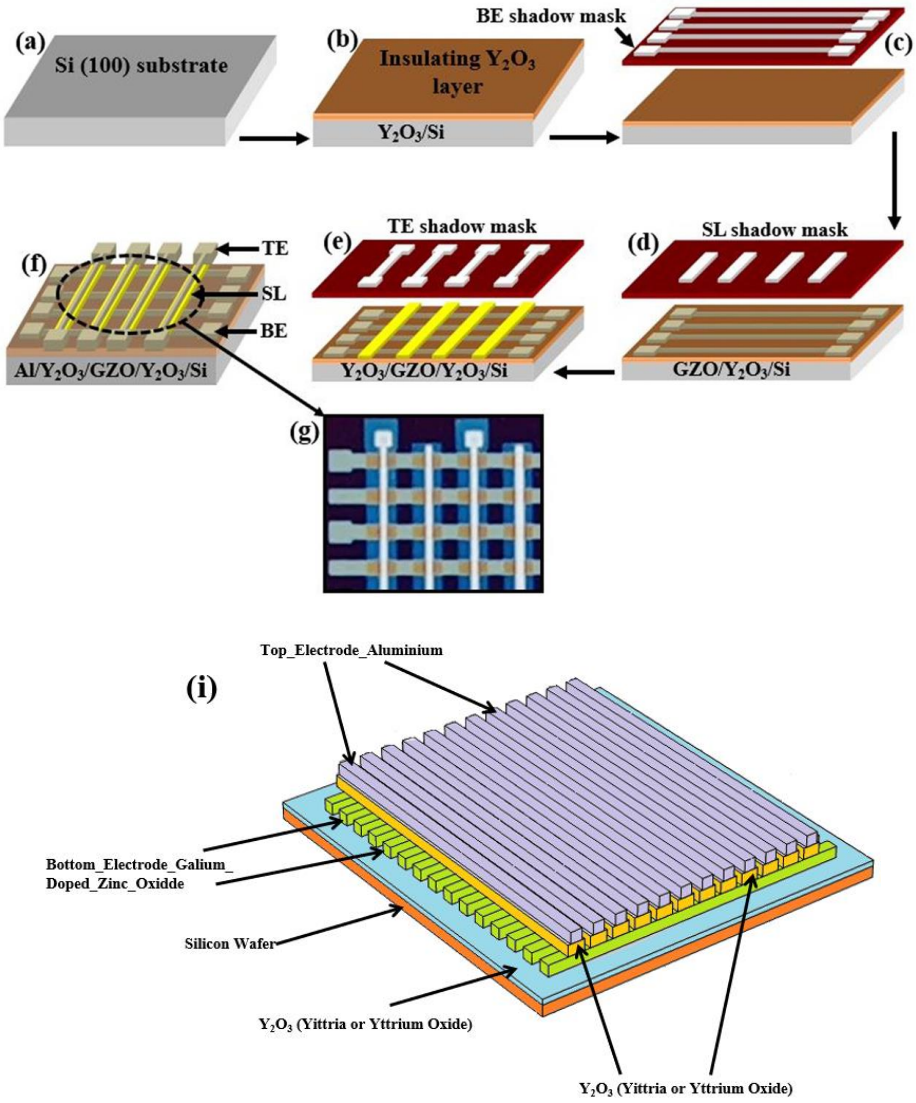
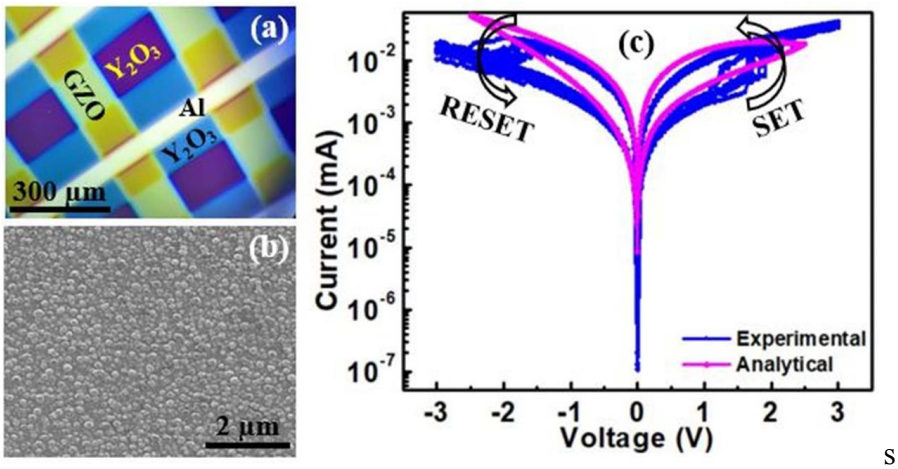


Figure 2.13: Schematic diagram of (a) cleaned Si substrate, (b) deposition of insulating Y2O3 layer on top of Si, (c) BE deposition via DIBS system, (d) SL deposition via DIBS system, (e) TE deposition via DC magnetron sputtering. (f) A schematic, digital camera photograph of the finally fabricated 4 × 4 crossbar array architecture and (g) schematic diagram of finally fabricated 4×4 crossbar array architecture.



s

Figure 2.14: (a) Magnified optical microscopy images of developed memristive crossbar array architecture, (b) FESEM images of top surface of Y_2O_3 SL, (c) resistive switching response of the fabricated memristive crossbar array fitted with the analytical model.

Experimental Figure 2.13 describes the detailed fabrication process to realize the Y_2O_3-based memristive crossbar array using the DIBS system [7, 8]. During the fabrication process, metal shadow masks are used to pattern the bottom electrode (BE), switching layer (SL) and top electrode (TE) of the crossbar array. For the (4 × 4) crossbar array fabrication, a 3-inch cleaned Si (100) substrate is utilized, as shown in Figure 2.13 (a) Further, an Ar^+ plasma etching process is performed for 15 min by the secondary ion assist source in the DIBS system to remove the native ultrathin SiO_2 layer on top of Si [7]. After the removal of native oxide, 150 nm thick polycrystalline Y_2O_3 is grown over the Si substrate as an insulating layer [8], as shown in Figure 2.13(b) at 100 ˚C in a pure Ar (5 sccm) environment in the assist ion source of the DIBS system. The deposited insulating layer has a remarkable surface morphology and smoothness due to the similar lattice constants of Si (2aSi = 10.86 Å) and Y_2O_3 (a Y_2O_3 = 10.60 Å), as reported elsewhere [20, 21]. Furthermore, a low resistive (5.3×10^{-4} Ω·cm) [13] Ga doped ZnO (GZO) with 100 nm thickness is grown over the insulating Y_2O_3 layer at 100 ˚C in a pure Ar (5 sccm) environment in the assist ion source. The deposited GZO acts as the BE and is patterned via a shadow mask with a width of 800 µm, as shown in Figure 2.13 (c). Subsequently, a 50 nm amorphous Y_2O_3 layer is

deposited as a resistive SL, as shown in Figure 2.13 (d). The SL is deposited at 300 ◦C at a fixed ratio of Ar to O_2 gas flow of 2:3 in the assist ion source of the DIBS system [25]. At the end, a 70 nm Al TE is deposited via a direct-current (DC) magnetron sputtering system, as presented in Figure 2.13(e). The line width of the TE shadow mask is 300 μm. Figures 1(f) and (g) show a schematic and digital camera photograph of the finally fabricated 4 × 4 crossbar memristive array. To investigate the resistive switching performance of the fabricated crossbar array architecture, a semiconductor parameter analyzer (SCS-4200A) system is utilized. Further, optical microscopy is performed to visualize the realistic view of the fabricated crossbar array, and field emission scanning electron microscopy (FESEM, Carl Zeiss) is used to assist in the surface morphological analysis. Subsequent to the fabrication and performance measurement of the memristive device, it is essential to analyze the performance to understand the underlying physics, and analytical modeling is essential. Previously, several analytical [15, 23–25] and circuit models [4] have been reported; however, none of the reported models have been validated with respect to the memristive crossbar array response. Some of the earlier reported models [15, 24, 25] have not been validated with the experimental results. Here, a memristive crossbar analytical model with experimental validation has been formulated to emulate the various memristive device properties.

Figure 2.14 (a) shows optical microscopy image of the developed memristive crossbar array, which clearly shows that the deposited layers are perfectly aligned to form a cross point structure in the array. Figure 2.14 (b) exhibits a continuous Y_2O_3 SL layer with compact grains, which is also described in our earlier report [7]. To analyze the resistive switching response of the fabricated crossbar array, the TE is connected to the positive/negative voltage terminal of the SCS-4200A while the BE is fixed to the ground. To examine the switching response, a triangular voltage waveform is applied to the device with an amplitude of ±3 V and a pulse width of 100 ms, and captures the resistive switching performance of the device as shown in Figure 2.14 (c). Further, when a positive voltage (0 to

+3 V) is imposed on the TE, the device switches from a high resistance state (HRS) to a low resistance state (LRS) and this process is termed the 'SET' process, as shown in Figure 2.14 (c). The detailed switching mechanism of the Y_2O_3-based memristor is described in our previous report [27]. For a negative voltage bias (from 0 to −3 V) applied on TE, the device switches from LRS to HRS [27], and this process is known as the RESET process, as depicted in Figure 2.14(c). Figure 2.14 (c) also reveals that the developed crossbar array shows a consistent resistive switching response in multiple switching cycles, and toggles between HRS and LRS and back without any noticeable change in the SET and RESET voltages. The negligible variation in the SET and RESET voltages signifies that the DIBS system is extremely promising to develop a reliable and stable memristive crossbar array. The analytical model, as discussed above, also captures the resistive switching behavior with an R^2-fitting accuracy of 99.2% with corresponding experimentally obtained data of the fabricated crossbar array. The accuracy of the model is comparatively higher than that observed in our previous reports [9, 14], in which ∼98% [9] and ∼96% [14] accuracy levels were reported. Besides that, the presented model has also shown better accuracy as compared to previously reported models [6, 26, 15] in terms of the stable switching response, with a better hysteresis loop area in multiple cycles. The presence of a pinched hysteresis loop in the resistive switching characteristics of the device is a footprint of the memristive system [28], and the pinched hysteresis loop can be collapsed into a single-valued function as described by Chua [29].

2.6 References:

[1] Kumar S, Agrawal R, Das M, Kumar P and Mukherjee S 2020 Analytical modeling of Y2O3-based memristive system for synaptic applications J. Phys. D: Appl. Phys. 53 1–6

[2] Prodromakis T, Peh B P, Papavassiliou C and Toumazou C 2011 A versatile memristor model with nonlinear dopant kinetics IEEE Trans. Electron Devices 58 3099–105

[3] Yang J J, Pickett M D, Li X, Ohlberg D A A, Stewart D R and Williams R S 2008 Memristive switching mechanism for metal/oxide/metal nanodevices Nat. Nanotechnol. 3 429–33

[4] Yakopcic C, Taha T M, Subramanyam G, Pino R E and Rogers S 2011 A memristor device model IEEE Electron Device Lett. 32 1436–8

[4] Chang T, Jo S-H, Kim K-H, Sheridan P, Gaba S and Lu W 2011 Synaptic behaviors and modeling of a metal oxide memristive device Appl. Phys. A 102 857–63

[5] Chen L, Li C, Huang T, Chen Y, Wen S and Qi J 2013 A memristor model with forgetting effect Phys. Lett. A 377 3260–5

[6] Das M, Kumar A, Kumar S, Mandal B, Khan M A and Mukherjee S 2018 Effect of surface variations on the performance of yttria based memristive system IEEE Electron Devices Lett. 39 1852–5

[7] Das M, Kumar A, Singh R, Htay M T and Mukherjee S 2018 Realization of synaptic learning and memory functions in Y2O3 based memristive device fabricated by dual ion beam sputtering Nanotechnology 29 055203

[8] Kumar S, Agrawal R, Das M, Jyoti K, Kumar P and Mukherjee S 2021 Analytical model for memristive systems for neuromorphic computation J. Phys. D: Appl. Phys. 54 355101

[9] Prodromakis T, Peh B P, Papavassiliou C and Toumazou C 2011 A versatile memristor model with nonlinear dopant kinetics IEEE Trans. Electron Devices 58 3099–105

[10] Khan M A, Kumar P, Das M, Htay M T, Agarwal A and Mukherjee S 2020 Drain current optimization in DIBS-grown MgZnO/CdZnO HFET IEEE Trans. Electron Devices 67 2276–81

[11] Das M, Kumar A, Kumar S, Mandal B, Siddharth G, Kumar P, Htay M T and Mukherjee S 2020 Impact of interfacial SiO2 on dual ion beam sputtered Y2O3-based memristive system IEEE Trans. Nanotechnology. 19 153134

[12] Sharma P, Singh R, Awasthi V, Pandey S K, Garg V and Mukherjee S 2015 Detection of a high photo response at zero bias from a highly conducting ZnO:Ga based UV photodetector RSC Adv. 5 85523

[13] Kumar S, Agrawal R, Das M, Kumar P and Mukherjee S 2020 Analytical modeling of Y2O3-based memristive system for synaptic applications J. Phys. D: Appl. Phys. 53 305101

[14] Yakopcic C, Taha T M, Subramanyam G, Pino R E and Rogers S 2011 A memristor device model IEEE Electron Device Lett. 32 1436–8

[15] S. Gaba, P. Sheridan, J. Zhou, S. Choi, and W. Lu, "Stochastic memristive devices for computing and neuromorphic applications," Nanoscale, vol. 5, no. 13, p. 5872, 2013, doi: 10.1039/C3NR01176C.

[16] D. Niraula and V. Karpov, "Numerical modeling of resistive switching in RRAM device," in Proc. COMSOL Conf. Boston, 2017, pp. 1–7.

[17] D. Niraula and V. Karpov, "Comprehensive numerical modeling of filamentary RRAM devices including voltage ramp-rate and cycle-to-cycle variations," J. Appl. Phys., vol. 124, no. 17, 2018, Art. no. 174502, doi: 10.1063/1.5042789.

[18] D. Niraula, and V. Karpov, "Comprehensive numerical modeling of filamentary RRAM devices including voltage ramp-rate and cycle-to-cycle variations", J. Appl. Phys., vol. 124, no. 17, 2018, DOI: 10.1063/1.5042789.

[19] R. Waser, and M. Aono, "Nanoionics-based resistive switching memories", Nature Materials, vol. 6, no. 11, 2007, DOI: 10.1038/nmat2023.

[20] K. Szot, W. Speier, G. Bihlmayer, and R. Waser, "Switching the electrical resistance of individual dislocations in single-crystalline $SrTiO_3$", Nature Materials, vol. 5, no. 4, 2006, DOI: 10.1038/nmat1614.

[21] Y. Wang, F. Wu, X. Liu, J. Lin, J. Y. Chen, W. W. Wu, J. Wei, Y. Liu, Q. Liu, and L. Liao, "High on/off ratio black phosphorus based memristor with ultra-thin phosphorus oxide layer", Appl. Phys. Lett., vol. 115, no. 193503, 2019, DOI: 10.1063/1.5115531.

[22] M. Das, A. Kumar, R. Singh, M. T. Htay and S. Mukherjee, "Realization of synaptic learning and memory functions in Y_2O_3 based memristive device fabricated by dual ion beam sputtering", Nanotechnology, vol. 29, no. 055203, pp. 1-9, 2018, DOI: 10.1088/1361-6528/aaa0eb.

[23] S. H. Jo, T. Chang, I. Ebong, B. Bhadviya, P. Mazumder and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems", Nano Lett., vol. 10, no. 4, 2010, DOI: 10.1021/nl904092h.

[24] Sanjay Kumar, Mohit Kumar Gautam, G. S. Gill and Shaibal Mukherjee, "3-D Physical Electro-Thermal Modeling of Nanoscale Y_2O_3-based Memristors for Synaptic Application," in IEEE Transactions on Electron Devices, vol. 69, no. 6, pp. 3124-3129, June 2022, doi: 10.1109/TED.2022.3166858.

[25] Snider G S 2008 Cortical computing with memristive nanodevices SciDAC Rev. 10 58–65

[26] Yang J J, Pickett M D, Li X, Ohlberg D A A, Stewart D R and Williams R S 2008 Memristive switching mechanism for metal/oxide/metal nanodevices Nat. Nanotechnol. 3 429–33

[27] Das M, Kumar A, Mandal B, Htay M T and Mukherjee S 2018 Impact of Schottky junctions in the transformation of switching modes in amorphous Y2O3-based memristive system J. Phys. D: Appl. Phys. 51 315102

[28] Chua L and Yang L 1988 Cellular neural networks: theory IEEE Trans. Circuits Syst. 35 1257–72

[29] Chua L 2011 Resistance switching memories are memristors Appl. Phys. A 102 765–83

Chapter 3

Results and Discussion

In this chapter, Firstly, we have discussed results of proposed time derivative of the internal state variable ($w(t)$) and two important parameters, namely *viz* the forgetting rate (τ) and retention (t_r) to emulate the retention and forgetting behavior of the memristive crossbar array. Synaptic behavior of memristive device on the application of consecutive positive and negative pulses with different amplitude and duration. Lastly, we discussed the simulated results exhibit a stable pinched hysteresis loop in the resistive switching (RS) responses in symmetric and asymmetric electrodes combinations with an efficient ON/OFF current ratio. Moreover, the simulated devices show the synaptic plasticity functionalities in terms of potentiation and depression processes with almost ideal linearity factor for both electrode combinations.

3.1 Analytical Modelling

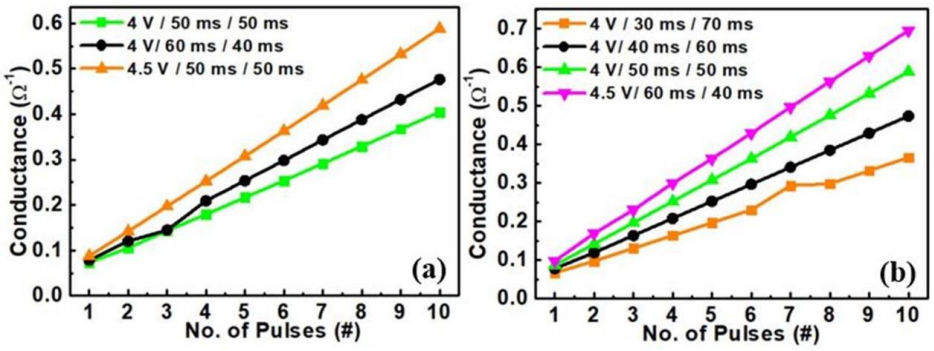


Figure 3.1: The plasticity of memristive crossbar using (a) pulses with different amplitude and duration, (b) pulses with different interval with constant amplitude. Here, the format of the labels, i.e., 4 V/50 ms/50 ms, shows the pulse amplitude, pulse width and interval between two consecutive pulses, respectively.

It is known that the conductance of memristive systems is dependent on various parameters, such as the input pulse amplitude, pulse time duration and time interval between two consecutive pulses. Here, Figure 3.1 (a) analytically shows the variation in the memristive device conductance with

respect to the number of pulses, in which ten consecutive voltage pulses with different amplitude and time duration are imposed on the memristive crossbar. It is observed that the pulses with larger voltage amplitude and longer time duration trigger a larger change in the device conductance, while on the other hand, the pulses with smaller amplitude and shorter time duration result in a negligible or no change in the device conductance, which is associated with the device activation state.

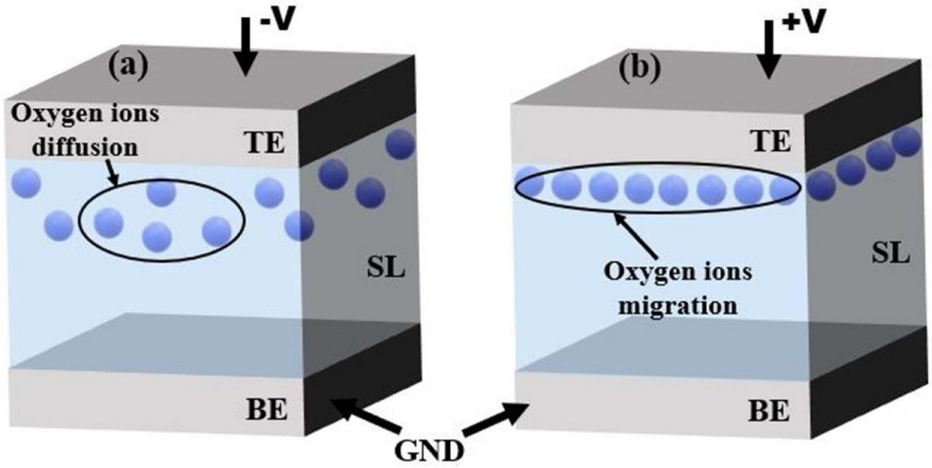


Figure 3.2: (a) Ion diffusion and (b) ion migration at the memristive device interface.

However, the relentless competition between ion diffusion and ion migration, as shown in Figure 3, at the device interface decides the net conductance of the memristive device. The ion diffusion decreases the device conductance while ion migration increases the device conductance [3, 8, 9]. Figure 3.2 (a) shows the ion diffusion process under the application of negative applied voltage at the TE, in which the net concentration of oxygen ions is less at the interface, which affects the interface conduction and further leads to a decrement in the device conductance [10–14]. On the other hand, under the application of applied positive voltage at the TE, the oxygen ion migration process takes place at the interface and the concentration of oxygen ions is higher at the device interface, which leads to an increment in device conductance at the interface [10–14], as shown in Figure 3.2 (b). Further, the time duration and interval have a significant impact on the device conductance [15, 16]. For this analysis, ten consecutive voltage pulses with the same amplitude and

different time duration and interval are applied on the memristive crossbar, and it is observed that the pulses with shorter intervals induce a larger change in the device conductance as compared to pulses with longer time intervals. This is because, in general, the longer time interval leads to ion diffusion, which substantially reduces the device conductance [3]. Similar memory plasticity is experimentally demonstrated by Das et al [4] in a DIBS-grown Y_2O_3-based single memristive device. In that work, the memristive device conductance is varied with the number of input pulses, and the impact of the conductance is investigated by the variation of pulse amplitude and duration. The experimental results reported by Das et al [4] are analytically verified by Kumar et al [5].

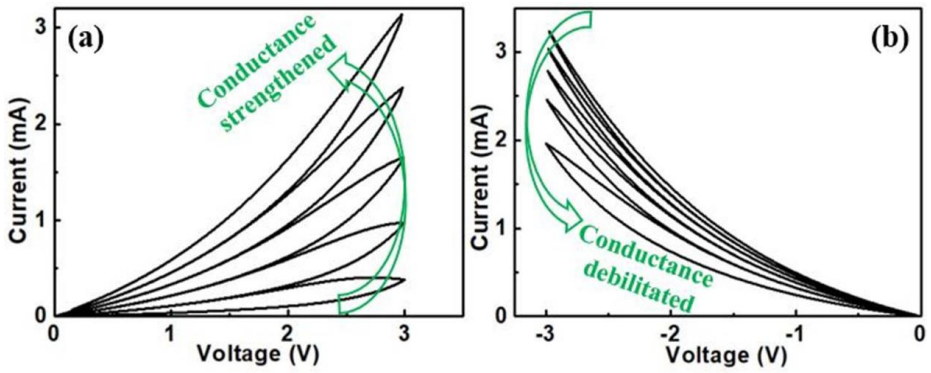


Figure 3.3: I–V curves of memristive systems under consecutive (a) positive voltage pulses of +3 V and (b) negative voltage pulses of −3 V. The change in device current/conductance is the basis of synaptic plasticity in memristive systems.

Further, the proposed model also captures the change in device current under the application of successive voltage sweeps, as shown in Figure 3.3. Figure 3.3 (a) represents a continuous enhancement of the device current (or conductance) under the application of successive positive voltage sweeps, and this phenomenon is analogous to the potentiation mechanism of memristive systems [1, 2]. On the other hand, for successive negative voltage sweeps, the device current (or conductance) continuously declines, as presented in Figure 3.3 (b), which is analogous to the depression mechanism of memristive systems [1, 2].

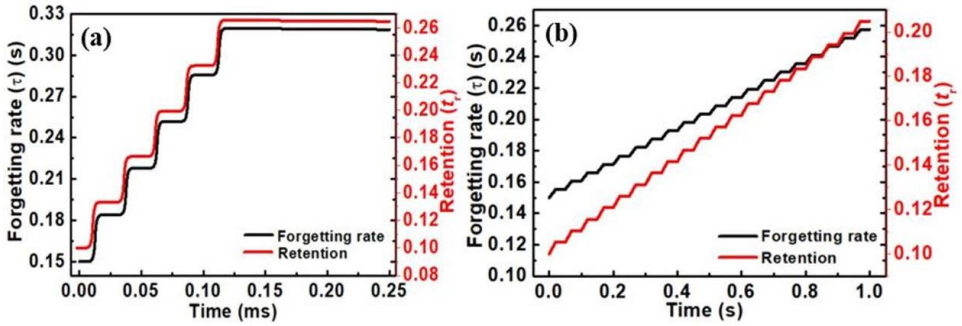


Figure 3.4 (a) and (b) τ –t and tr–t curves.

Figure 3.4 shows the retention and forgetting rate in the improved diffusion term and it is varied along with the time for which the electric field is applied. The direction of the ion diffusion is determined by the comparative result of the conductance and the retention. When $w > t_r$, the positive electrical field is overlapped, while an overlapping negative electric field is observed when $w < t_r$. In other cases, the ion diffusion mechanism promotes the increment or decrement in the device conductance, i.e., the ion diffusion process has the same direction as the ion migration [3]. Moreover, the asymmetric variation in the positive and negative electric field, τ and t_r, vary more rapidly under a positive electric field as compared to the case for a negative electric field, as shown in Figure 3.4 (a). From Figure 3.4 (b), it is clear that the forgetting rate and the retention are improved significantly under the application of repeated electrical stimulation. The forgetting rate increases from 0.15 to 0.26 s along with the increasing input stimuli number. At the same time, as shown in Figure 3.4 (b), the retention also increases from 10% to 20.1%, which is comparatively better than the previously reported data [3], 6 and the increment in forgetting rate and retention indicate a clear transition from STM to LTM [3]. Another important behavior of a memristive system is the transition from STM to LTM, which is captured by the proposed analytical model.

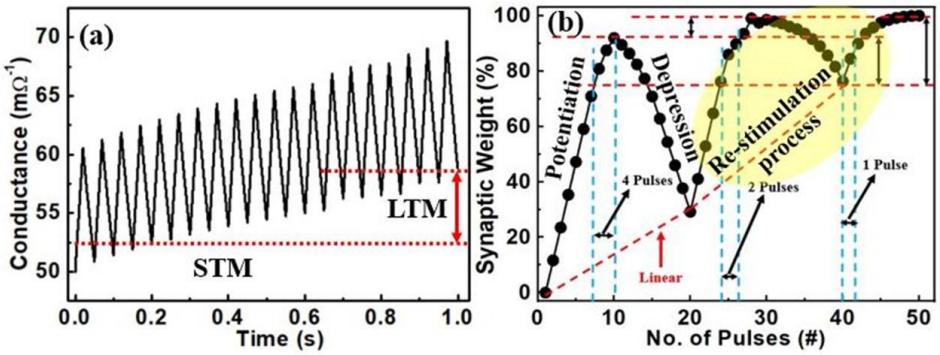


Figure 3.5: (a) Transition from STM to LTM in which conductance varies along with stimulation pulses, (b) potentiation and depression processes along with restimulation process.

As shown in Figure 3.5 (a), 20 consecutive input pulses of +4 V amplitude and 40% duty cycle are imposed on the memristive device. Under the application of each electrical stimulation, the device conductivity is first increased, followed by a decay due to spontaneous diffusion, as mentioned earlier. However, when the time interval between the successive stimulation is relatively short, in the range of 5–30 ms, an overall increment in the conductance is observed despite the spontaneous decay, as shown in Figure 3.5 (a). This phenomenon is caused by the competing process between diffusion and ion migration [3, 8, 9, 15]. Moreover, the stabilization in the switching process and persistence of LTM are evidence of the growth of new synaptic connections and a change in the shape and size of the pulse, adding more pathways for synaptic transmission. LTM fades with time, showing that the synaptic connections revoke with time, but at a much slower speed compared to the decay in STM [15].

Figure 3.5 (b) shows the synaptic plasticity behavior in terms of the potentiation and depression processes of the memristive device [1, 2, 4]. During a positive electrical stimulus, the synaptic weight or the normalized conductance of the memristive device is continuously strengthened, while under a negative electrical stimulus, the synaptic weight is gradually debilitated. Figure 3.5 (b) further displays the re-stimulation process followed by the first stage of the potentiation and depression processes, in

which a comparatively smaller number of electrical input stimuli are required to achieve the same stage of memory learning process. This phenomenon is similar to the learning behavior of biological systems, which allows relearning of the elapsed information to be at a much faster rate [4, 15].

The extensive benefits of the discussed analytical model are that it is able to emulate the forgetting and retention behavior and STM-to-LTM transition precisely, which was not captured by earlier reported models [5, 6, 7]. Further, the proposed model also has the ability to capture the realistic behavior of biological systems, which helps engineers and researchers to analyze the various functionalities of biological systems. Moreover, the developed analytical memristive model is also able to compute the diverse real-time neuromorphic characteristics.

3.2 Physical Modelling

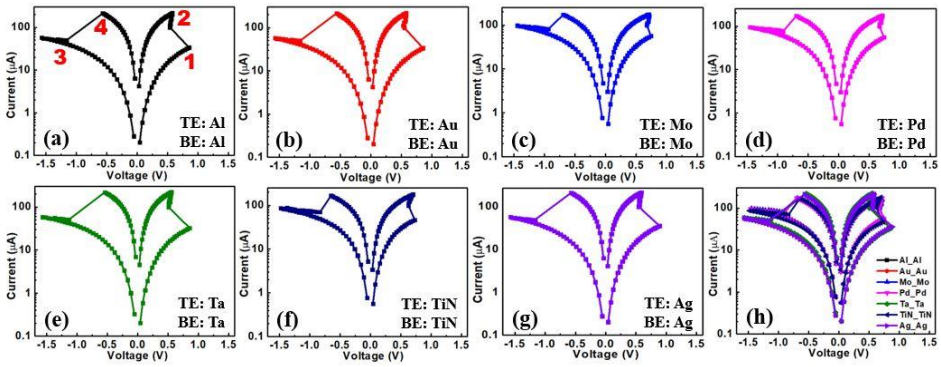


Figure 3.6: Resistive switching response of symmetric electrodes-based memristor structure: (a) Al/Y_2O_3/Al (V_{SET}: +0.5788 V and V_{RESET}: -0.5654 V), (b) Au/Y_2O_3/Au (V_{SET}: +0.5684 V and V_{RESET}: -0.5641 V), (c) Mo/Y_2O_3/Mo (V_{SET}: +0.7002 V and V_{RESET}: -0.6907 V), (d) Pd/Y_2O_3/Pd (V_{SET}: +0.7123 V and V_{RESET}: -0.6957 V), (e) Ta/Y_2O_3/Ta (V_{SET}: +0.5554 V and V_{RESET}: -0.5428 V), (f) TiN/Y_2O_3/TiN (V_{SET}: +0.6988 V and V_{RESET}: -0.6494 V), (g) Ag/Y_2O_3/Ag (V_{SET}: +0.5844 V and V_{RESET}: -0.5709 V), and (h) combined switching response of (a-g).

Figure 3.6: shows the simulated RS response of the various symmetric electrodes-based Y_2O_3 memristive devices. To evaluate the switching

response, the amplitude of an input voltage is ±1.5 V with a pulse width of ~10 ms has been imposed on the top electrode via a load resistance. As seen from Figure 3.6 (a), the RS response can be categorized into four parts namely as: (1) positive forming voltage ($+V_F$), (2) positive SET voltage (V_{SET}), (3) negative rupture voltage ($-V_R$), and (4) negative RESET voltage (V_{RESET}). During the positive voltage supply, all the CFs are formed inside the resistive switching medium of Y_2O_3 layer and memristive device is switched into the SET position from the forming position (V_F) and the process is termed as "SET process". The amplitude of V_{SET} is $\leq V_F$, as depicted in Figure 3.7 Also, it is observed that the hysteresis loop area in the resistive switching behaviors is dependent on the used metal combinations. On the other hand, when negative polarity voltage is applied on the top electrode all the formed CFs are ruptured and the memristive device is switched into RESET position and process is termed as "RESET process" where voltage amplitude $\leq -V_R$, as shown in Figure 3.7 The values of V_{SET} and V_{RESET} for all the symmetric device structures in which these are varied from one metal combination to the other. Figure 3.7 shows the RS response of the various asymmetric electrode-based Y_2O_3 memristive devices.

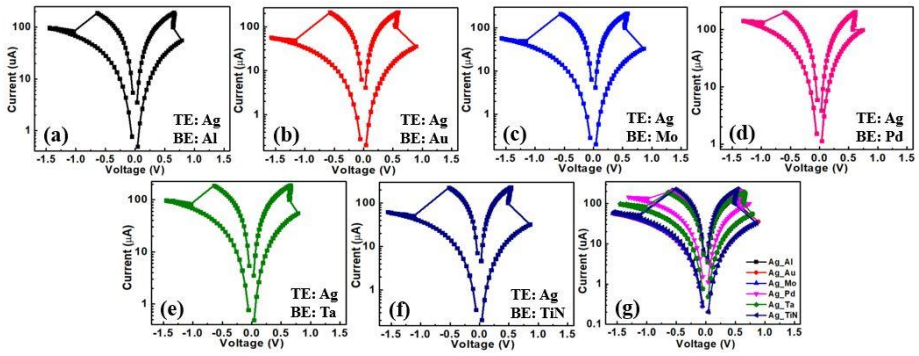


Figure 3.7: Resistive switching response of asymmetric electrode-based memristor structure: (a) Ag/Y_2O_3/Al (V_{SET}: +0.6537 V and V_{RESET}: -0.6399 V), (b) Ag/Y_2O_3/Au (V_{SET}: +0.5819 V and V_{RESET}: -0.5711 V), (c) Ag/Y_2O_3/Mo (V_{SET}: +0.5687 V and V_{RESET}: -0.5632 V), (d) Ag/Y_2O_3/Pd (V_{SET}: +0.6049 V and V_{RESET}: -0.5966 V), (e) Ag/Y_2O_3/Ta (V_{SET}: +0.6537 V and V_{RESET}: -0.6399 V), (f) Ag/Y_2O_3/TiN (V_{SET}: +0.5359 V and V_{RESET}: -0.5187 V), and (g) combined switching response of (a-f).

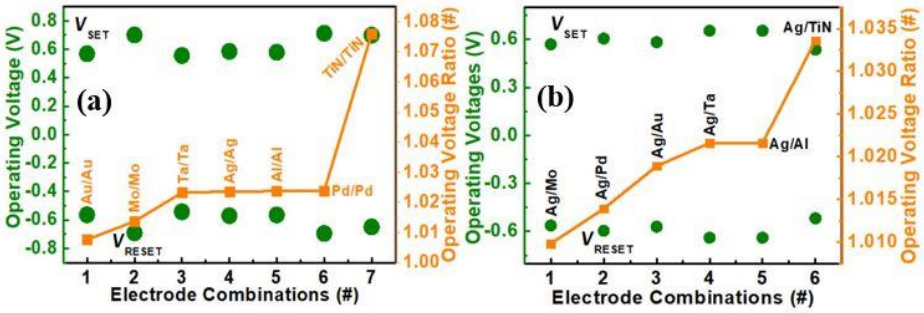


Figure 3.8: Operating voltages (V_{SET} and V_{RESET}) and operating voltage ratio (= $V_{SET}/|V_{RESET}|$) of Y_2O_3-based memristor with (a) symmetric electrodes, and (b) asymmetric electrodes.

Figure 3.8 shows the different operating voltages such as SET voltage (V_{SET}) and RESET voltage (V_{RESET}). Figure 3.8 (a) depicts the V_{SET} and V_{RESET} for the symmetric electrode-based Y_2O_3 memristor device while Figure 3.8 (b) shows the V_{SET} and V_{RESET} for the asymmetric electrode-based Y_2O_3 memristor device. Here, it is noticed that the operating voltages for each device structure combination are identical and had slight variations from one device structure to another. Further, to compare the differences between V_{SET} and V_{RESET} for all the simulated structures, we defined operating voltage ratio (= V_{SET}/V_{RESET}). As seen from Figure 3.8 (a), in the case of symmetric electrode-based memristor device, when the device electrode combination shift from Au/Au to Ta/Ta to TiN/TiN, the operating voltage ratio is increased. While on the other hand, in case of an asymmetric electrode-based memristor device, when device electrode combination shifts from Ag/Mo to Ag/Ta to Ag/TiN, the operating voltage ratio is also increased, as shown in Figure 3.8 (b). That means the optimized bias condition is necessary for each device structure to obtain the proper change in the device conductance.

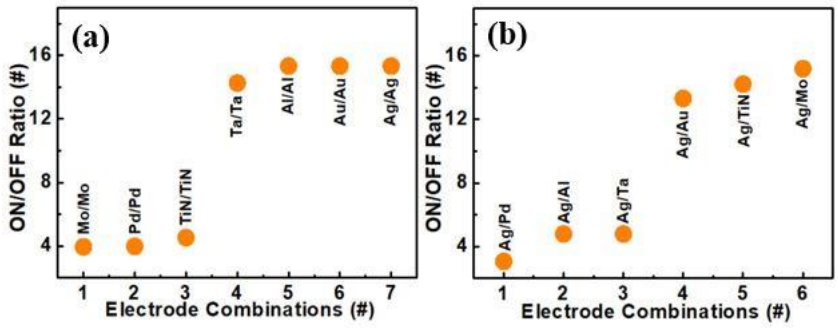


Figure 3.9: ON/OFF ratio of (a) symmetric electrodes, and (b) asymmetric electrodes-based Y_2O_3 memristor.

Figure 3.9 shows the ON/OFF ratio of current for both symmetric and asymmetric electrodes-based Y_2O_3 memristor devices. The simulated results show that when Ag, Au, and Al are considered as top and bottom electrode in Y_2O_3 memristor device, the ON/OFF ratio of current is highest, as compared to the other symmetric electrode combinations. On the other hand, the ON/OFF ratio is highest when Mo is considered as a bottom electrode in case of the asymmetric electrode where Ag acts as a top electrode. The ON/OFF ratio of the memristor device is associated with the memory window of the device and higher values of the ON/OFF ratio lead to the better stability in the switching response along with cyclic operations and time scale which is further useful in digital and logic applications.

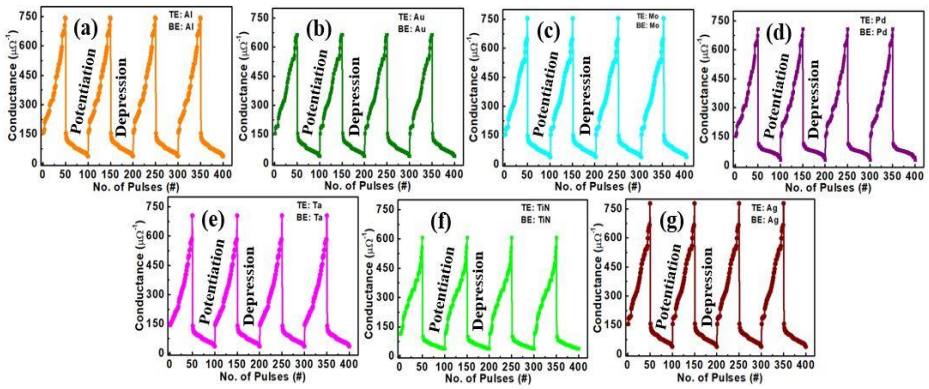


Figure 3.10: Potentiation and depression processes of symmetric electrodes-based Y_2O_3 memristor: (a) Al/Y_2O_3/Al, (b) Au/Y_2O_3/Au, (c) Mo/Y_2O_3/Mo, (d) Pd/Y_2O_3/Pd, (e) Ta/Y_2O_3/Ta, (f) TiN/Y_2O_3/TiN, and (g) Ag/Y_2O_3/Ag.

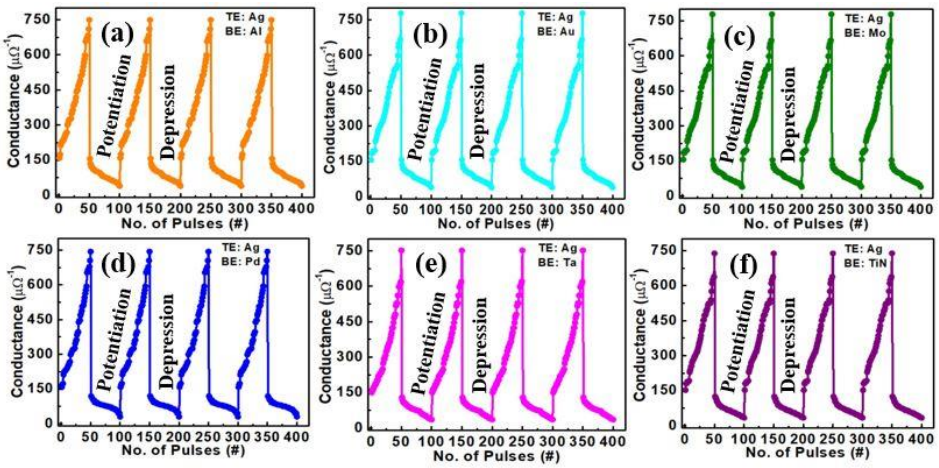


Figure 3.11: Potentiation and depression processes of asymmetric electrodes-based Y_2O_3 memristor: (a) Ag/Y_2O_3/Al, (b) Ag/Y_2O_3/Au, (c) Ag/Y_2O_3/Mo, (d) Ag/Y_2O_3/Pd, (e) Ag/Y_2O_3/Ta, and (f) Ag/Y_2O_3/TiN.

Further, to evaluate the synaptic plasticity behavior of the memristive device in terms of potentiation and depression, a train of 50 positive and 50 negative triangular voltage pulses with amplitude of +1.5 and -1.5 V, respectively, with voltage ramp rate (V_{RR}) of 100 V/s are imposed on the memristive device. Figure 3.11 shows the synaptic plasticity characteristics for symmetric electrode-based while Figure 3.11shows the asymmetric electrode-based Y_2O_3 memristor device. As seen from Figure 3.10 and 3.11, under the application of positive voltage pulses, the synaptic weight or the normalized device conductance of the memristive device is continuously strengthened. The continued strengthening in the synaptic weight is analogous to the 'learning behavior' of the human brain functionality and this process is termed as 'potentiation'. While, in the case of negative electrical pulses, the synaptic weight is gradually weakened, as shown in Figure 3.10 and 3.11. The continuous weakening in the synaptic weight is familiar with the 'forgetting behavior' of the human brain functionality and this process is termed as 'depression'. Also, the continuous strengthening and weakening of the synaptic weight are analogous to the synaptic plasticity functionality of the human brain [17-18, 21-25]. Here, a chain of consecutive 100 (50 positive and 50 negative) identical pulses with an amplitude of ±1.5 V and pulse width of 15 ms are imposed on the device to compute the synaptic characteristics. As seen from Figure 3.10 and 3.11, under the identical pulses, the metal/insulator

interfaces are observed to exhibit gradual potentiation and abrupt depression process [26-29]. The abrupt change in the depression process is associated with the difference in metal-oxide free energy [30]. Moreover, considering the metal-oxide free energy, induced oxide layer and non-identical spikes pulses which have different pulse amplitude or duration can be an efficient solution to overcome the high asymmetry ratio [18] in potentiation and depression processes. However, the non-identical spike may enhance the complexity of the peripheral circuits and the neuro-inspired computing system [18].

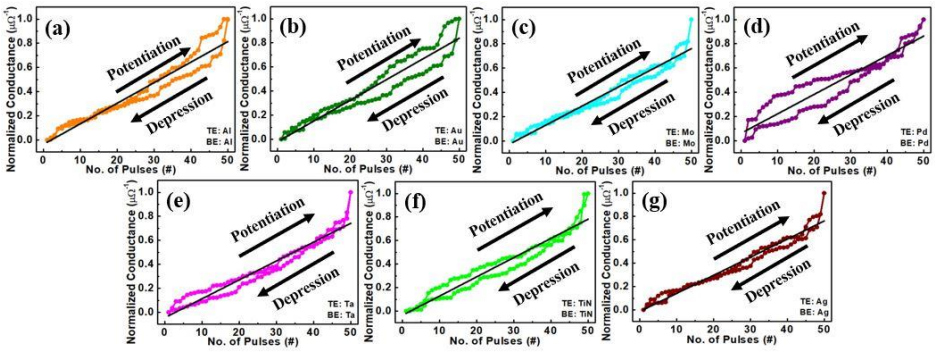


Figure 3.12: Evaluation of asymmetric ratio in potentiation (0 to 50 pulses) and depression (50 to 0 pulses) processes of symmetric electrodes-based Y_2O_3 memristor: (a) Al/Y_2O_3/Al, (b) Au/Y_2O_3/Au, (c) Mo/Y_2O_3/Mo, (d) Pd/Y_2O_3/Pd, (e) Ta/Y_2O_3/Ta, (f) TiN/Y_2O_3/TiN, and (g) Ag/Y_2O_3/Ag.

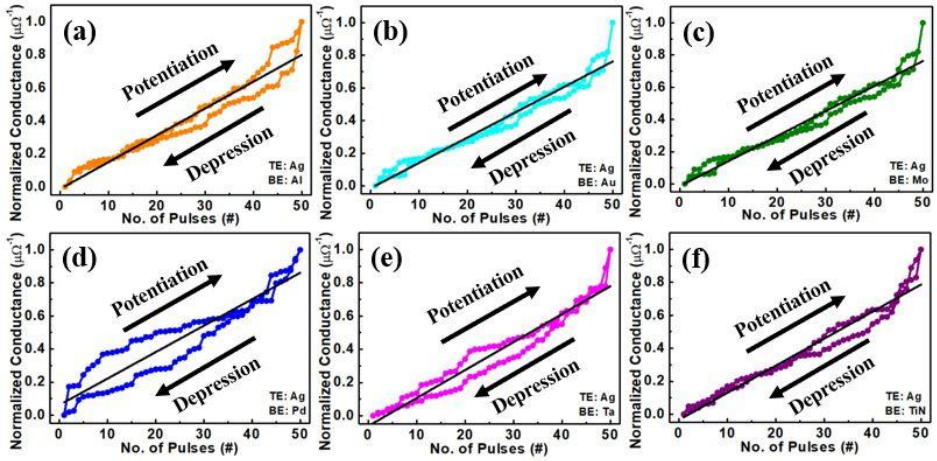


Figure 3.13: Evaluation of asymmetric ratio in potentiation (0 to 50 pulses) and depression (50 to 0 pulses) processes of asymmetric electrodes-based Y_2O_3 memristor: (a) Ag/Y_2O_3/Al, (b) Ag/Y_2O_3/Au, (c) Ag/Y_2O_3/Mo, (d) Ag/Y_2O_3/Pd, (e) Ag/Y_2O_3/Ta, and (f) Ag/Y_2O_3/TiN.

Here, in Figure 3.12 and 3.13, the potentiation and depression processes are plotted for symmetric electrodes and asymmetric electrodes-based memristor with the same number of applied pulses. For the potentiation, the number of pulses is expressed from 0 to 50, while in case of the depression, the number of pulses is from 50 to 0. Hence, based on this bilateral symmetric superposition, the absolute conductance difference between the potentiation and depression can be calculated and defined as an asymmetry ratio (R_A). To compare the values of conductance (G) among these samples, normalized values of device conductance are considered. In case of the neuro-inspired computing system, it is required to be updated the synaptic weights and conductance of the synaptic device need to be changed with the same incremental value at any conductance value. In other words, at any certain conductance value, the potentiation and depression can be executed randomly [19, 20]. Thus, the increment in the conductance change (ΔG) needs to be the same during the potentiation and depression processes. For example, if the potentiation is processed for ten times at a certain conductance value, and sequentially the depression process is processed for ten times, then the final conductance value needs to be similar to the initial conductance value. However, sometimes, the final and initial conductance values are not similar and, in this case, a more complicated circuits and processes are required to make a target conductance of the synaptic device. The unreliable change in the device conductance (ΔG) can degrade the learning accuracy in the computation of neuro-inspired computing systems [19, 20]. Therefore, the similar change in the potentiation and depression is one of the important factors for designing and developing the synaptic device. Here, to compare all simulated device structures, asymmetry ratio has been utilized which can show the linearity in weight, indirectly. Based on the maximum and minimum G values (G_{max} and G_{min}), it is assumed that G is varied from G_{min} to G_{max} during the potentiation and from G_{max} to G_{min} during the depression. Thus, at a certain pulse number (N_x), the R_A can be defined as:

$$Asymmetric\ ratio\ (R_A) = \frac{G_{Pot}\ at\ N_x}{G_{Dep}\ at\ (N_{max} - N_x)} \quad (1)$$

where, G_{pot} is G value during the potentiation, G_{dep} is G value during the depression, and N_{max} is total pulse number between G_{min} and G_{max}. However, this R_A cannot be a direct indicator for the linearity in weight, it can show a difference of G between the potentiation and depression after a certain number of pulses.

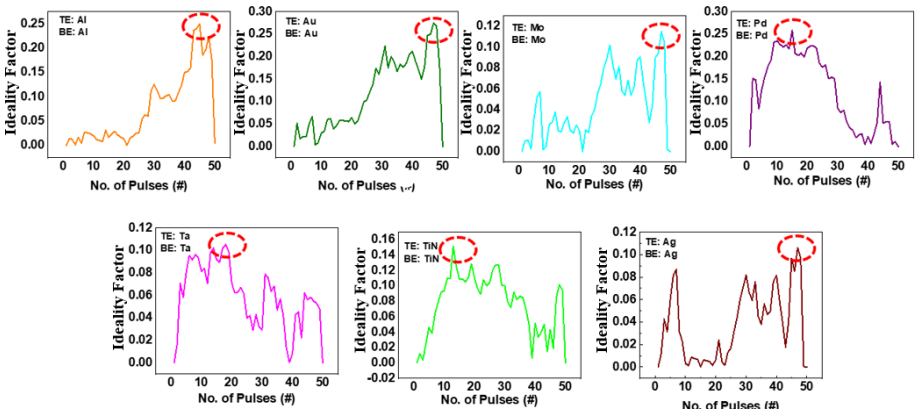


Figure 3.14: Evaluation of Non-Linearity in potentiation (0 to 50 pulses) and depression (50 to 0 pulses) processes of symmetric electrodes-based Y_2O_3 memristor: (a) Al/Y_2O_3/Al, (b) Au/Y_2O_3/Au, (c) Mo/Y_2O_3/Mo, (d) Pd/Y_2O_3/Pd, (e) Ta/Y_2O_3/Ta, (f) TiN/Y_2O_3/TiN, and (g) Ag/Y_2O_3/Ag.

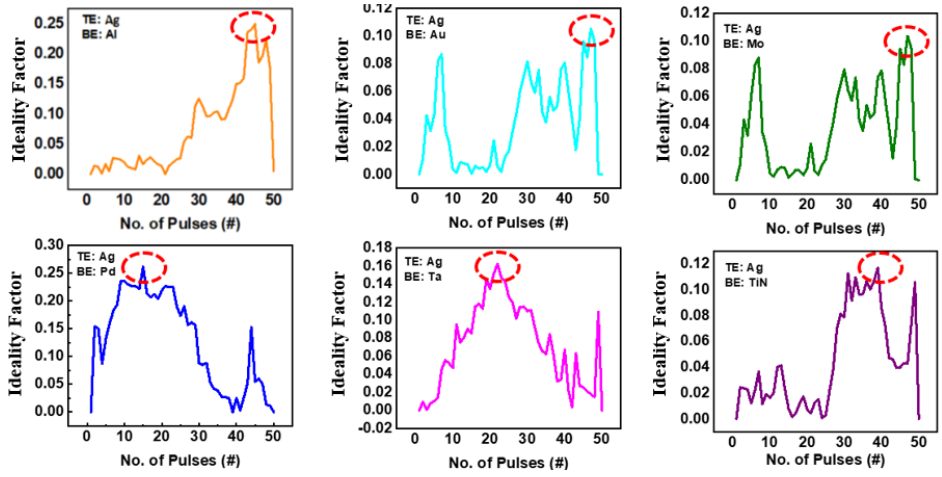


Figure 3.15: Evaluation of asymmetric ratio in potentiation (0 to 50 pulses) and depression (50 to 0 pulses) processes of asymmetric electrodes-based Y_2O_3 memristor: (a) Ag/Y_2O_3/Al, (b) Ag/Y_2O_3/Au, (c) Ag/Y_2O_3/Mo, (d) Ag/Y_2O_3/Pd, (e) Ag/Y_2O_3/Ta, and (f) Ag/Y_2O_3/TiN.

Here, in Figure 13 and 10, the NL i.e., non-Linearity curves are plotted for symmetric electrodes and asymmetric electrodes-based memristor with the

same number of applied pulses. Here, to compare the ideal learning behavior of all simulated device structures over the excitation, Ideality factor has been utilized which can show the behavior of ideality in weight with the applied pulses while potentiation and depression respectively. Based on the absolute difference of the conductance values IF i.e., ideality factor can be calculated. Thus, at a certain pulse number (N_x), the IF can be defined as:

$$Ideality\ Factor\ (\mathrm{IF}) = |GPx - GDx| \tag{2}$$

where, GP_x and GD_x are G value during the potentiation and depression at certain pulse number. However, this IF cannot be a direct indicator for the Ideality in synaptic weight updation while learning process. The value of IF for the ideal learning process must be zero, but as we can see in the reported IF values are nearly close to the zero and zero at the transition of P and D, where potentiation ends and depression begins. Number of maxima and minima can be observed in the in plots in which global maxima and global minima represents the maximum and minimum deviation from the ideal behavior, respectively. In the major number of plots global maxima occurs near the 50th pulse which means deviation is maximum almost at the end of process. The deviation in device conductance ($|\Delta G|$) can degrade the learning accuracy in the computation of neuro-inspired computing systems. Therefore, change in the GP and GD is one of the reliable factors for designing and developing the ideal synaptic device.

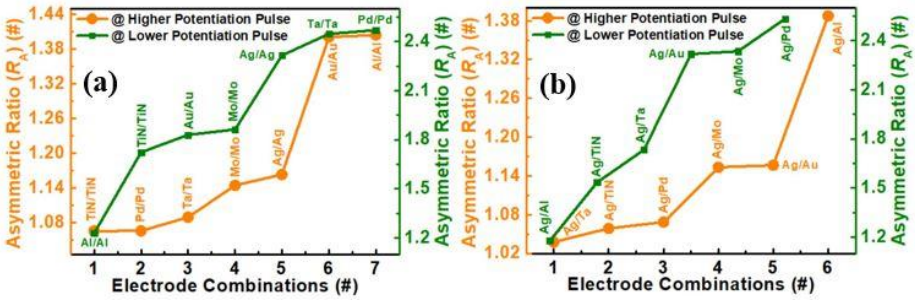


Figure 3.16: Asymmetric ratio of Y_2O_3-based memristor with (a) symmetric electrodes, and (b) asymmetric electrodes. Here, in both the cases, the asymmetric ratio is comparatively higher at the lower potentiation pulse as compared to higher potentiation pulse.

Figure 3.16: shows the values of R_A for symmetric electrodes-based (see Figure 3.11(a)) and asymmetric electrode-based (see Figure 3.11(b)) Y_2O_3 memristor. As seen from Figure 3.11, the values of R_A are nearly '1' at the higher potentiation pulse for both symmetric and asymmetric electrodes-based memristors which is the ideal case in synaptic characteristics. While for the lower potentiation pulse, the values of R_A are comparatively higher in comparison to the ideal value for both symmetric and asymmetric electrodes-based memristor. In case of lower potentiation pulse, the higher values of RA can be associated with the initially generated perturbations inside the memristive device.

3.3 References:

[1] Chang T, Jo S-H, Kim K-H, Sheridan P, Gaba S and Lu W 2011 Synaptic behaviors and modeling of a metal oxide memristive device Appl. Phys. A 102 857–63

[2] Jo S H, Chang T, Ebong I, Bhadviya B, Mazumder P and Lu W 2010 Nanoscale memristor device as synapse in neuromorphic systems Nano Lett. 10 1297–301

[3] Chen L, Li C, Huang T, Chen Y, Wen S and Qi J 2013 A memristor model with forgetting effect Phys. Lett. A 377 3260–5

[4] Das M, Kumar A, Singh R, Htay M T and Mukherjee S 2018 Realization of synaptic learning and memory functions in Y2O3 based memristive device fabricated by dual ion beam sputtering Nanotechnology 29 055203

[5] Kumar S, Agrawal R, Das M, Jyoti K, Kumar P and Mukherjee S 2021 Analytical model for memristive systems for neuromorphic computation J. Phys. D: Appl. Phys. 54 355101

[6] Kumar S, Agrawal R, Das M, Kumar P and Mukherjee S 2020 Analytical modeling of Y2O3-based memristive system for synaptic applications J. Phys. D: Appl. Phys. 53 305101

[7] Yakopcic C, Taha T M, Subramanyam G, Pino R E and Rogers S 2011 A memristor device model IEEE Electron Device Lett. 32 1436–8

[8] Sassine G, Barbera S L, Najjari N, Minvielle M, Dubourdieu C and Alibart F 2016 Interfacial versus filamentary resistive switching in TiO2 and HfO2 devices J. Vacuum Sci. Technol. B 34 012202

[9] Waser R, Dittmann R, Staikov G and Szot K 2009 Redox-based resistive switching memories-nanoionic mechanisms, prospects, and challenges Adv. Mater. 21 2632–63

[10] Sun W, Gao B, Chi M, Xia Q, Yang J J, Qian H and Wu H 2019 Understanding memristive switching via in situ characterization and device modeling Nat. Commun.10 3453

[11] Nikam R D, Kwak M and Hwang H 2021 All-solid-state oxygen ion electrochemical random-access memory for neuromorphic computing Adv. Electron. Mater. 7 2100142

[12] Kim S et al 2019 Metal-oxide based, CMOS-compatible ECRAM for deep learning accelerator 2019 IEEE Int. Electron Devices Meeting (IEDM) pp 35.7.1–35.7.4

[13] Li Y et al 2020 Filament-free bulk resistive memory enables deterministic analogue switching Adv. Mater. 32 2003984

[14] Lee J, Nikam R D, Kwak M, Kwak H, Kim S and Hwang H 2021 Improvement of synaptic properties in oxygen-based synaptic transistors due to the accelerated ion migration in sub-stoichiometric channels Adv. Electron. Mater.7 2100219

[15] Chang T, Jo S-H and Lu W 2011 Short-term memory to long-term memory transition in a nanoscale memristor ACS Nano 5 7669–76

[16] Wang Z Q, Xu H Y, Li X H, Yu H, Liu Y C and Zhu X J 2012 Synaptic learning and memory functions achieved using oxygen ion migration/diffusion in an amorphous InGaZnO memristor Adv. Funct. Mater. 22 2759–65

[17] H. Y. Chen, S. Yu, B. Gao, P. Huang, J. Kang, and H. S. P. Wong, "HfO_x based vertical resistive random-access memory for cost-effective 3D cross-point architecture without cell selector", IEEE International Electron Devices Meeting (IEDM, 2012, San Francisco, CA, USA, DOI: 10.1109/IEDM.2012.6479083.

[18] H. Akinaga, and H. Shima, "Resistive random-access memory (ReRAM) based on metal oxides", Proc. IEEE vol. 98, no. 12, 2010, DOI: 10.1109/JPROC.2010.2070830

[19] M. Das, A. Kumar, R. Singh, M. T. Htay and S. Mukherjee, "Realization of synaptic learning and memory functions in Y_2O_3 based memristive device fabricated by dual ion beam sputtering", Nanotechnology, vol. 29, no. 055203, pp. 1-9, 2018, DOI: 10.1088/1361-6528/aaa0eb.

[20] S. H. Jo, T. Chang, I. Ebong, B. Bhadviya, P. Mazumder and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems", Nano Lett., vol. 10, no. 4, 2010, DOI: 10.1021/nl904092h.

[21] R. D. Nikam, J. Lee, W. Choi, W. Banerjee, M. Kwak, M. Yadav, and H. Hwang, "Ionic Sieving Through One-Atom-Thick 2D Material Enables Analog Nonvolatile Memory for Neuromorphic Computing", Small, vol.17, no. 24, DOI: 10.1002/smll.202103543.

[22] W. Banerjee, "Challenges and Applications of Emerging Nonvolatile Memory Devices", Electronics, vo. 9, no. 1029, 2020, DOI:10.3390/electronics9061029.

[23] W. Banerjee, S. H. Kim, S. Lee, S. Lee, D. Lee, and H. Hwang, "Deep Insight into Steep-Slope Threshold Switching with Record Selectivity (> 4×10^{10}) Controlled by Metal-Ion Movement through Vacancy-Induced-Percolation Path: Quantum-Level Control of Hybrid-Filament", Adv. Funct. Mater., vol. 31, no. 37, 2021, DOI: 10.1002/adfm.202104054.

[24] J. W. Jang, S. Park, Y. H. Jeong and H. Hwang, "ReRAM-based Synaptic Device for Neuromorphic Computing", IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne, VIC, Australia, no. 14483574, 2014, DOI: 10.1109/ISCAS.2014.6865320.

[25] H. Liu, M. Wei and Y. Chen, "Optimization of non-linear conductance modulation based on metal oxide memristors", Nanotechnol Rev., vol. 5, no. 7, 2018, DOI: 10.1515/ntrev-2018-0045.

[26] K. Kim, S. Park, S. M. Hu, J. Song, W. Lim, Y. Jeong, J. Kim, S. Lee, J. Y. Kwak, J. Park, J. K. Park, B. K. Ju, D. S. Jeong, and I. Kim, "Enhanced analog synaptic behavior of SiNx/a-Si bilayer memristors through Ge

implantation", NPG Asia Materials, vol. 12, no. 77, 2020, DOI: 10.1038/s41427-020-00261-0.

[27] J. J. Zhang, H. J. Sun, Y. Li, Q. Wang, X. H. Xu, and X. S. Miao, "AgInSbTe memristor with gradual resistance tuning", Appl. Phys. Lett., vol. 102, no. 18,2013, DOI: 10.1063/1.4804983.

[28] S. Yu, "Neuro-inspired computing using resistive synaptic devices", Springer: Berlin, 2017, ISBN 978-3-319-54313-0, DOI: 10.1007/978-3-319-54313-0.

[39] G. W. Burr, R. M. Shelby, C. D. Nolfo, J. W. Jang, R. S. Shenoy, P. Narayanan, K. Virwani, E.U. Giacometti, B. Kurdi, and H. Hwang, "Experimental demonstration and tolerancing of a largescale neural network (165,000 synapses), using phase-change memory as the synaptic weight element", IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2014, DOI: 10.1109/IEDM.2014.7047135.

[30] J. W. Jang, S. Park, Y.H. Jeong, and H. Hwang, "ReRAM-based synaptic device for neuromorphic computing", IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne, VIC, Australia, 2014, DOI: 10.1109/ISCAS.2014.6865320.

Chapter 4

Conclusions and Future Work

4.1 Conclusions

We have reported the detailed fabrication process for an Y_2O_3-based memristive crossbar array architecture with its highly stable resistive switching response. Further, a nonlinear analytical model is also proposed, which is capable of simulating the resistive switching response of the fabricated crossbar array. Moreover, the developed analytical model shows various characteristics such as synaptic plasticity with learning behavior, the potentiation and depression processes, and the re-stimulation mechanism. These are essential properties for neuromorphic computation application. The developed analytical model also captures the new forgetting and retention functionality, including the memory transition between STM and LTM. Therefore, the described model can be further used in the design and modeling of memristive systems for in-memory computation, neuromorphic computation and artificial neural network applications.

Further, we have reported the resistive switching performance of the Y_2O_3-based memristor device with symmetric and asymmetric electrode combinations via COMSOL. The simulated results show the stable RS behavior in the pinched hysteresis resistive switching response with an efficient ON/OFF current ratio. The simulated outcomes suggest that, in the case of symmetric electrodes, Au/Au configuration shows a minimum operating voltage ratio while in the case of asymmetric electrodes, Ag/Mo configuration shows the minimum operating voltage ratio. Moreover, the highest ON/OFF current ratio is shown by Al/Al (Au/Au and Ag/Ag also shown the similar values in ON/OFF current ratio) electrodes configuration which is in case of symmetric while Ag/Mo in case of asymmetric electrodes configuration. The simulated memristor devices with symmetric and asymmetric electrodes configurations have also effectively established

the synaptic plasticity functionality with the almost ideal linearity factor which is analogous to the functionality of human brain. Therefore, the extensive benefit of the presented work is to be beneficial for the researchers to select the appropriate metal electrodes to develop Y_2O_3-based memristor devices which able to capture the realistic behavior of the biological synapse.

4.2 Future Work

- To explore the physical modelling of the memristive device with the stacked layer of MoS_2 and emulate the various Synaptic Properties like short term memory (STM), long term memory (LTM).
- To analysis the switching response of the Stacked-Layer MoS_2-based memristive device at nanoseconds or picosecond pulse width.
- To study the DAC behaviour of MoS_2-based memristive device.
- To explore and study the effect of perturbation at both interfaces (i.e., Top and bottom).

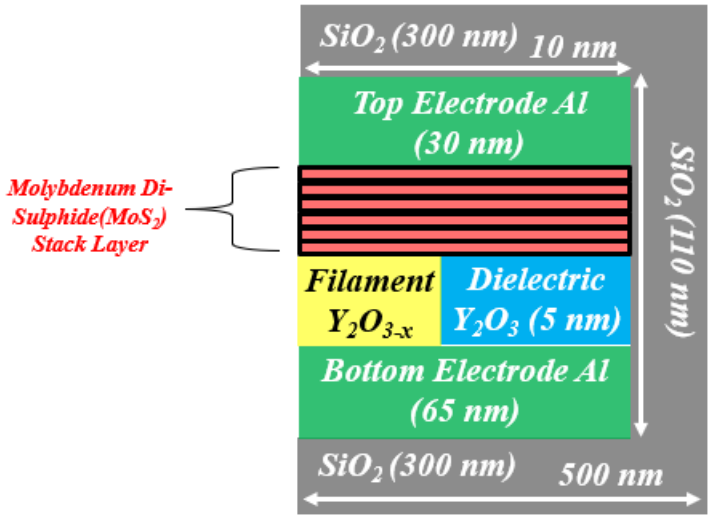


Figure 4.1: 2D structure of Stacked-Layer MoS_2 memristive device.