B. TECH. PROJECT REPORT

On

Impact of dopant location on the performance of nanoscale devices

BY

Rishikesh Meena

DISCIPLINE OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

December 2017

Impact of dopant location on the performance of nanoscale devices

A PROJECT REPORT

Submitted in partial fulfillment of the
requirements for the award of the degrees

of
BACHELOR OF TECHNOLOGY
in

ELECTRICAL ENGINEERING

Submitted by:
Rishikesh Meena

Guided by:
Dr. Abhinav Kranti, Faculty, Electrical Engineering

INDIAN INSTITUTE OF TECHNOLOGY INDORE
December 2017

CANDIDATE'S DECLARATION

We hereby declare that the project entitled **"Impact of dopant location on the performance of nanoscale devices"** submitted in partial fulfillment for the award of the degree of Bachelor of Technology in 'Electrical' completed under the supervision of **Dr. Abhinav Kranti, Professor, Electrical Engineering,** IIT Indore is an authentic work.

Further, I/we declare that I/we have not submitted this work for the award of any other degree elsewhere.

Signature and name of the student(s) with date

CERTIFICATE by BTP Guide(s)

It is certified that the above statement made by the students is correct to the best of my/our knowledge.

Signature of BTP Guide(s) with dates and their designation

Preface

This report on "Impact of dopant location on the performance of nanoscale devices" is prepared under the guidance of Dr. Abhinav Kranti, Professor, Electrical Engineering.

Through this report we have tried to gain a detailed knowledge about the functioning of various nanoscale semiconductor devices. We have tried study the changes these devices go through when subjected to different conditions.

We have tried to the best of our abilities and knowledge to explain the content in a lucid manner. We have also added figures and graphs to make it more illustrative.

Rishikesh Meena
B.Tech. IV Year
Discipline of Electrical Engineering
IIT Indore

Acknowledgements

I would like to express my sincere gratitude to my supervisors Dr. Abhinav Kranti for providing their invaluable guidance, comments, suggestions and kind support throughout the course of the project.

It is through their help and support, due to which we became able to complete the design and technical report.

Without their support this report would not have been possible

Rishikesh Meena
B.Tech. IV Year
Discipline of Electrical
IIT Indore

Abstract

The recent emergence of fabrication tools and techniques capable of constructing structures with dimensions ranging from 0.1 to 50 nm has opened up numerous possibilities for investigating new devices in a size domain heretofore inaccessible to experimental researchers. There is intense study around the world to determine the exact point in dimensional scaling where it becomes either physically unfeasible or financially impractical to continue the trend towards reducing the size while increasing the complexity of silicon chips. Although there are myriad questions involving electrical contacts, interconnections, reliability, and the like, one of the fundamental issues in the miniaturization/complexity debate concerns the Si MOSFET itself when the gate length is reduced to less than 50 nm. Does it behave like a long gate device or does the output conductance increase to impractical levels due to short-channel effects?

Table of Contents

List of Figures

Chapter 1 : INTRODUCTION

1.1. Nanoscale Devices

Nanoscale devices are devices that are one hundred to ten thousand times smaller than human cells and that can manipulate matter on atomic or molecular scales. Examples of nanoscale devices are synthetic molecular motors such as rotaxanes, graphene-based transistors and nanoelectromechanical oscillators. Devices that have been beyond the reach of engineers can now be fabricated in new ways. The crucial factor has been the development of a technique by which extremely narrow rods, or nanowires, of a semiconductor can be formed. The bottom-up, self-assembly process enables accurate control of dimension, location, composition, and other properties. The materials are the same semiconductors, like Si and GaAs, that we have, for the last forty or so years, been shaping into devices and circuits. But this process has relied on top-down fabrication techniques.

The top-down approach limits the dimensions of devices to what is technically achievable using lithography. This is the means by which patterns can be drawn, either in stone as the Vikings did when they carved messages into granite, or into Si as the electronics industry does today to build integrated circuits. Lithographic techniques can create device features as narrow as 130 nm and the industry sees the road ahead pretty well drawn up for line-widths down to ~50 nm. This continued progress does not come without a price; the cost of new fabs is growing extremely fast, at a pace that may limit continued progress, simply because devices and circuits become too expensive to be economically viable.

1.2. Simulation in ATLAS

Atlas is a 2D and 3D device simulator that performs DC, AC, and transient analysis for silicon, binary, ternary, and quaternary material-based devices. Atlas enables the characterization and optimization of semiconductor devices for a wide range of technologies. ATLAS is a physically-based two and three dimensional device simulator. It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation.

Device simulation helps users understand and depict the physical processes in a device and to make reliable predictions of the behavior of the next device generation. Two-dimensional device simulations with properly selected calibrated models and a very well-defined appropriate mesh structure are very useful for predictive parametric analysis of novel device structures. Two- and three-dimensional modeling and simulation processes help users

obtain a better understanding of the properties and behavior of new and current devices. This helps provide improved reliability and scalability, while also helping to increase development speed and reduce risks and uncertainties.

Chapter 2 : Study of nanoscale devices

2.1. PN Junction Diode

A *PN Junction Diode* is one of the simplest semiconductor devices around, and which has the characteristic of passing current in only one direction only. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage as the diode has an exponential current-voltage (I-V) relationship and therefore we can not described its operation by simply using an equation such as Ohm's law.

A simple pn junction diode simulated in ATLAS is shown below.

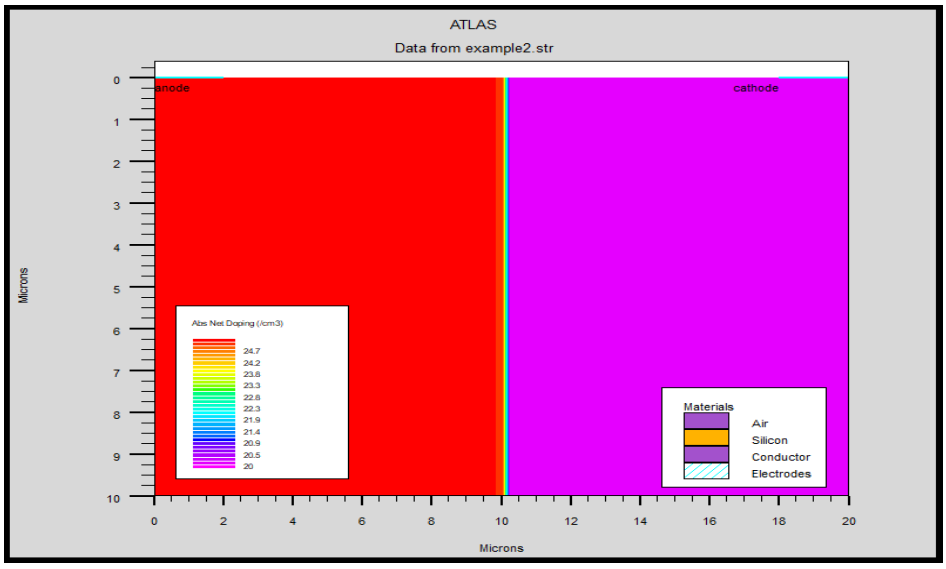

Fig. 2.1 (a) PN Junction Diode

The device structure is simulated with acceptor (N_a) and donor (N_d) doping concentration of $10^{19}cm^{-3}$ and $10^{17}cm^{-3}$, respectively. In order to forward bias the pn diode, the cathde terminal is fixed at zero baias whereas, the potential at the anode terminal varied from 0 V to 1 V.

If a suitable positive voltage (forward bias) is applied between the two ends of the PN junction, it can supply free electrons and holes with the extra energy they require to cross the junction as the width of the depletion layer around the PN junction is decreased.

Similarly, by applying a negative voltage (reverse bias) results in the free charges being pulled away from the junction resulting in the depletion layer width being increased. This has the effect of increasing or decreasing the effective resistance of the junction itself allowing or blocking current flow through the diode.

There are two operating regions and three possible "biasing" conditions for the standard **Junction Diode** and these are:

- 1. Zero Bias – No external voltage potential is applied to the PN junction diode.
- 2. Reverse Bias – The voltage potential is connected negative, (-ve) to the P-type material and positive, (+ve) to the N-type material across the diode which has the effect of **Increasing** the PN junction diode's width.
- 3. Forward Bias – The voltage potential is connected positive, (+ve) to the P-type material and negative, (-ve) to the N-type material across the diode which has the effect of **Decreasing** the PN junction diodes width.

1. Reverse Biased PN Junction Diode :

When a diode is connected in a **Reverse Bias** condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode.

The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

Fig. 2.1 (b) Reverse Characteristics Curve for a Junction Diode

This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small **leakage current** does flow through the junction which can be measured in micro-amperes, (μA).

One final point, if the reverse bias voltage Vr applied to the diode is increased to a sufficiently high enough value, it will cause the diode's PN junction to overheat and fail due to the avalanche effect around the junction. This may cause the diode to become shorted and will result in the flow of maximum circuit current, and this shown as a step downward slope in the reverse static characteristics curve above in fig. 2.1 (b).

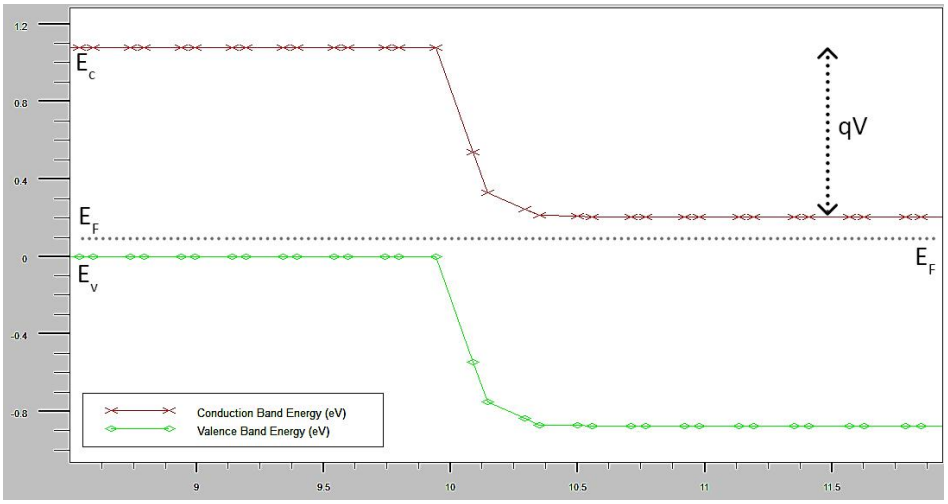

Fig. 2.1 (c) Energy band diagram in reverse bias condition

To reverse-bias the p-n junction, the p side is made more negative, making it "uphill" for electrons moving across the junction. The conduction direction for electrons in the diagram is right to left, and the upward direction represents increasing electron energy.

2. Forward Biased PN Junction Diode **:**

When a diode is connected in a **Forward Bias** condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow.

This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the

opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current flowing up to this voltage point, called the “knee” on the static curves and then a high current flow through the diode with little increase in the external voltage.

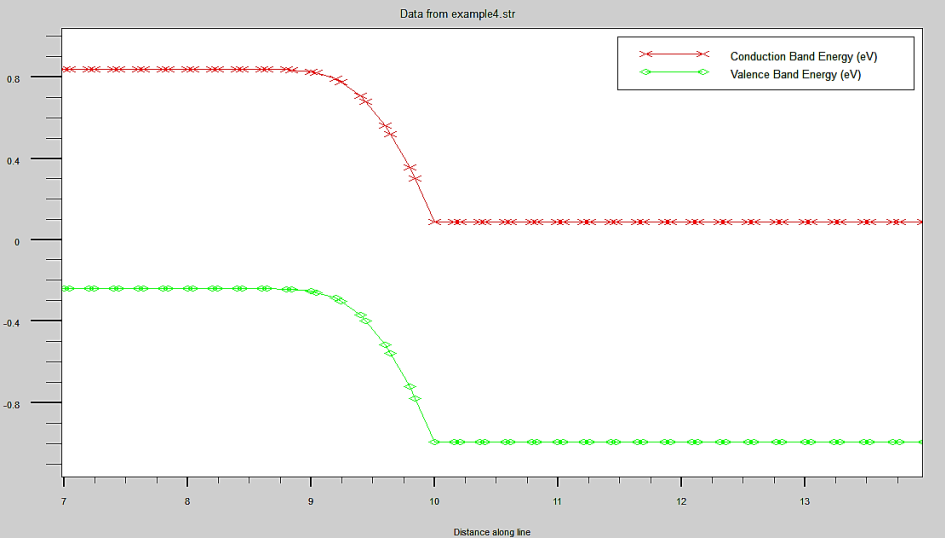

Fig. 2.1 (d) Energy band diagram in forward bias condition

To forward bias the p-n junction, the p side is made more positive, so that it is "downhill" for electron motion across the junction. An electron can move across the junction and fill a vacancy or "hole" near the junction. It can then move from vacancy to vacancy leftward toward the positive terminal, which could be described as the hole moving right. The conduction direction for electrons in the diagram is right to left, and the upward direction represents increasing electron energy.

2.2. MOSFET

The most common type of insulated gate FET which is used in many different types of electronic circuits is called the Metal Oxide Semiconductor Field Effect Transistor or MOSFET for short.

The MOSFET is a voltage controlled field effect transistor that differs from a JFET in that it has a “Metal Oxide” Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass. The gate material is often a layer of polysilicon(polycrystalline silicon). The MOSFET is by far the most common transistor in digital circuits, as hundreds of thousands or millions of them may be included in a memory chip or microprocessor.

MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:

- Depletion Type – the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "Normally Closed" switch.
- Enhancement Type – the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.

Basic MOSFET Structure :

The construction of the Metal Oxide Semiconductor FET is very different to that of the Junction FET. Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge carriers, electrons for n-channel or holes for P-channel, through the semiconductive drain-source channel. The gate electrode is placed on top of a very thin insulating layer and there are a pair of small n-type regions just under the drain and source electrodes. Such MOSFET simulated in ATLAS is shown below.

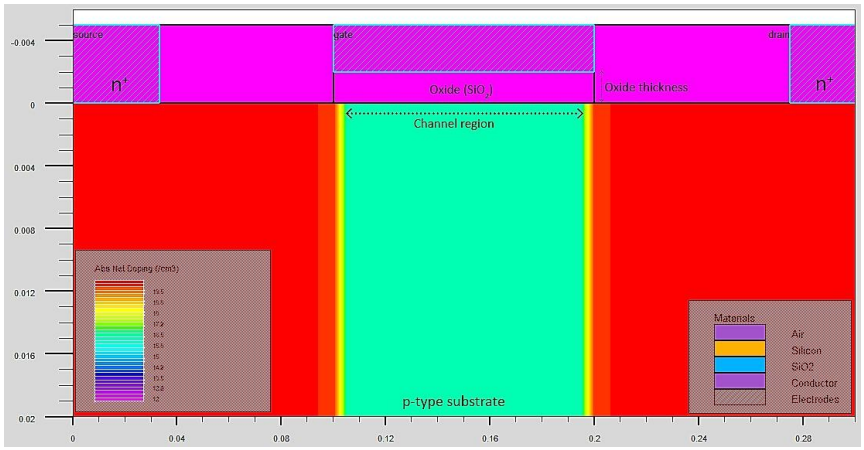

Fig.2.2 (a) Basic MOSFET structure

With a insulated gate MOSFET device no limitations apply on the biasing of the gate, so it is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve).This makes the MOSFET device especially valuable as electronic switches or to make logic gates because with no bias they are normally non-conducting and this high gate input resistance means that very little or no control current is needed as MOSFETs are voltage controlled devices. Both the p-channel and the n-channel MOSFETs are available in two basic forms, the Enhancement type and the Depletion type.

The I-V characteristics shown by an Enhancement type MOSFET is shown below.

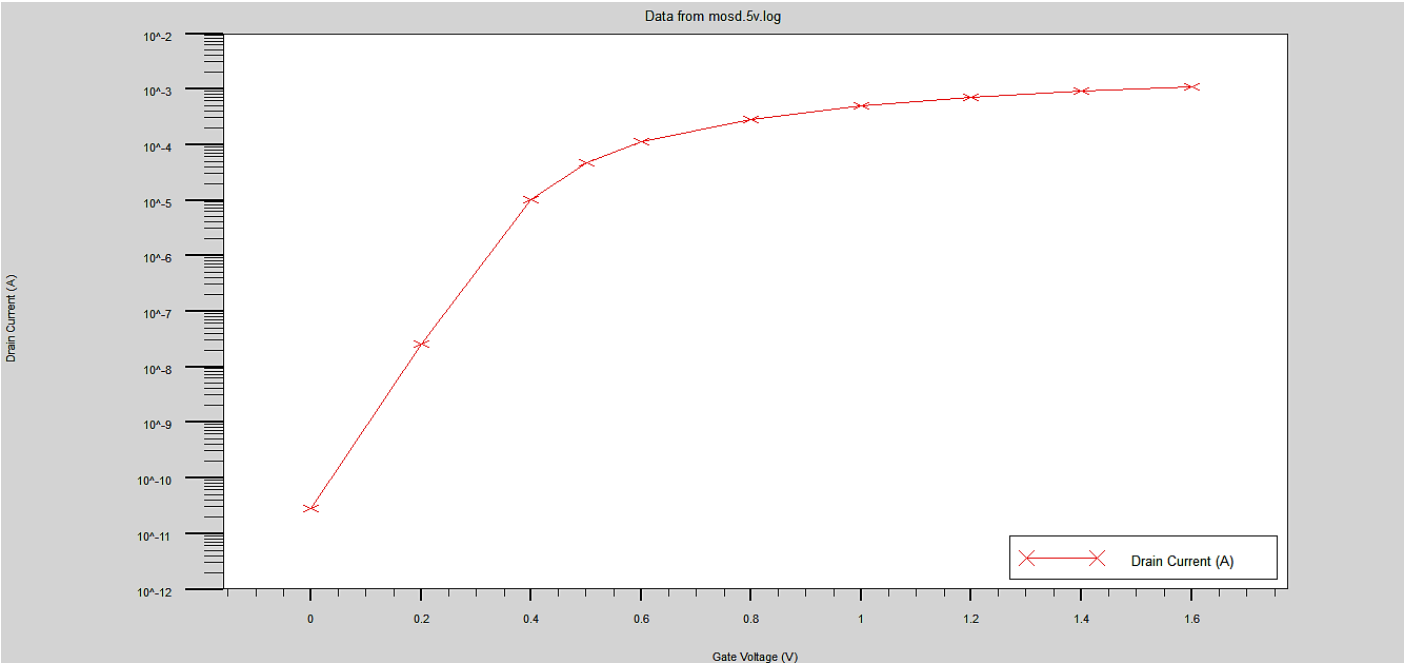

Fig.2.2 (b) I-V curve of MOSFET

If we keep the drain voltage (V_{DS}) constant and keep increasing the gate voltage (V_{GS}) then as a result the output current (I_D) will also increase. Enhancement-mode MOSFETs make excellent electronics switches due to their low "ON" resistance and extremely high "OFF" resistance as well as their infinitely high input resistance due to their isolated gate. Enhancement-mode MOSFETs are used in integrated circuits to produce CMOS type *Logic Gates* and power switching circuits in the form of as PMOS (P-channel) and NMOS (N-channel) gates. CMOS actually stands for *Complementary MOS* meaning that the logic device has both PMOS and NMOS within its design.

Variation in Oxide Thickness :

Similar to gate length if thickness of oxide layer is varied by taking the value of as 5 nm, 15 nm & 30 nm the variation of curve. It is useful to consider the impact of silicon thickness on the device current and performances. Thinner gate oxide are necessary is the drain current. Therefore for large current the oxide layer thickness should be less. If the t_{ox} is larger then drain current will increase which will shift threshold voltage of device to smaller values. The off state current is high with thick oxide layer and low with thin oxide layer. Devices with thick oxide layer have less control of gate on channel barrier height.

2.3. Ultra Thin Box (UTB) Body MOSFET :

These type of MOSFETs are made by adding just another body elctrode. This is also called SOI technology. By doing so we'll get a better performing device and also better control over SCE(short-channel effect). In addition to supressing the short channel effects, it also reduces the sub-threshold gate leakage current. With lower junction leakage we will be needing low switching energy for the device. Despite of all these advantages of using this device, this also have some critical drawback such as floating body effect.

There are two kinds of UTB SOI MOSFETs : PD-SOI(Partially depleted-SOI) and FD-SOI (Fully depleted-SOI). Of these fully depleted silicon on insulater is preferred because of its thin size, reduced leakage current and improved power consumption characteristics. A fully depleted SOI MOSFET is shown below.

Fig.2.3 (a) Fully depleted-SOI MOSFET

SOI MOSFETs are prone to self heating as the thermal conductivity of SiO_2 layer is lower than the silicon layer. There are two factors that are to be considered for the analysis of electrical characteristic for an UTB SOI : (a) The inversion electron- channel thickness of an MOSFET is less than 10nm. (b) If the top silicon layer is thinner than the inversion layer, the channel thickness is determined by the decrease in the top silicon layer thickness.

Effect of Silicon film thickness (Tsi) :

If we increase the silicon film thickness as 10nm, 15nm and 20nm then the value of off-current (the current at the beginning when the device is in off state, is the off current) will start to increase.The higher value of off-current is bad for device functioning.

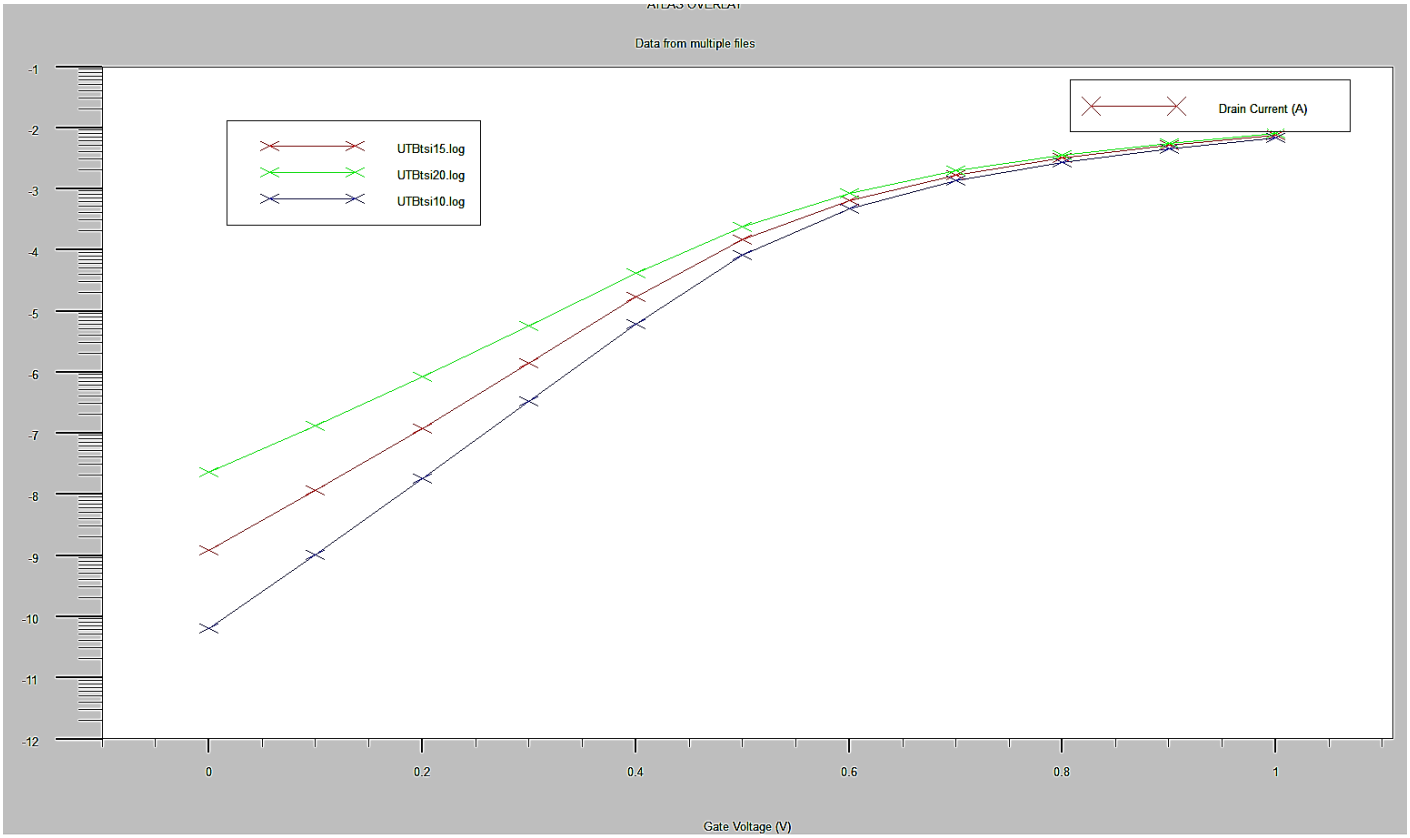

Fig. 2.3 (b) Effect of silicon film thickness(Tsi)

As you can see in above graph as we keep increasing the silicon film thickness the value of current at 0V is increasing. The value of off-current increases exponentially as the thickness of the insulating region decreases. Off-current is currently one of the main factors limiting increased computer processor performance. Off-current is generally measured in microamperes.

Effect of Gate Length :

With the increase of gate length, the distance between source and drain will increase. So now to more charge will be required to form a single layer of channel. So for a certain amount of gate voltage, drain current will decrease with the increase of gate length.

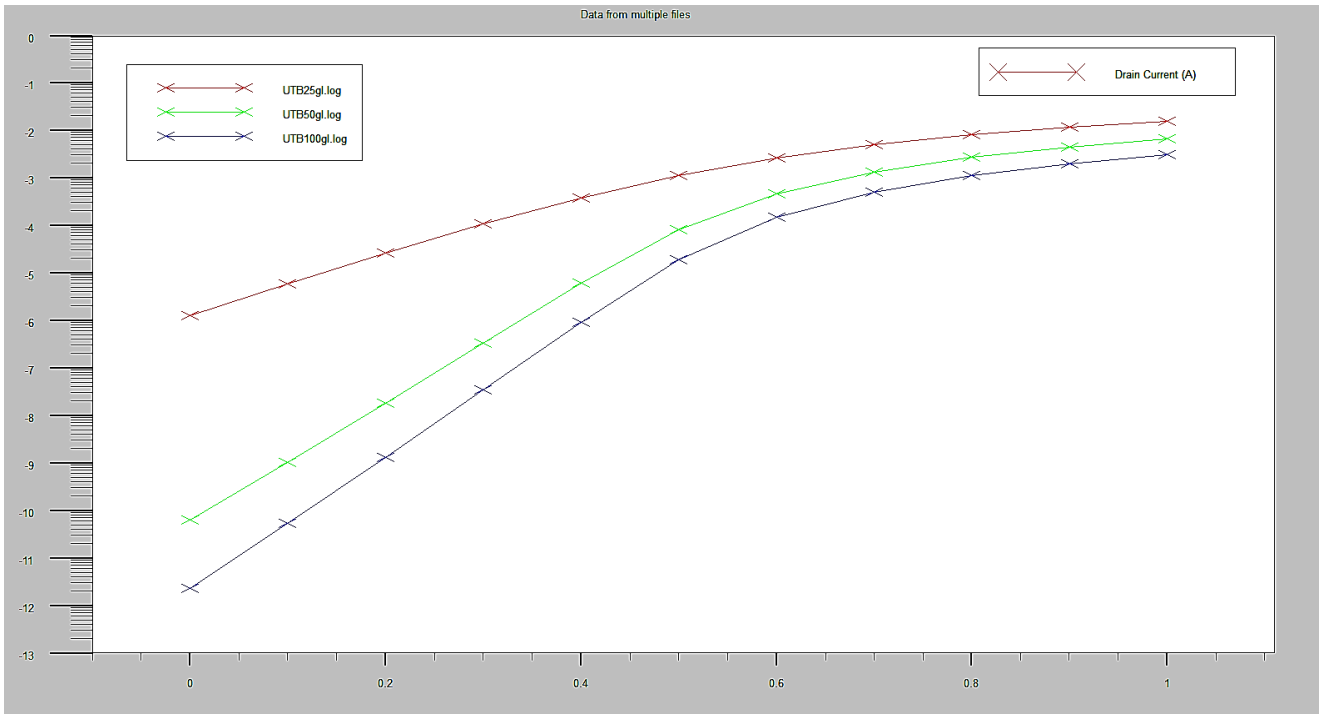

Fig.2.3 (c) Effect of gate length

Effect of Oxide thickness :

With the increase in oxide thickness the distance between gate electrode and channel keeps on increasing. So now more voltage will be required to accumulate that same amount of charge to form a channel. So with increase in thickness of oxide, the drain current decreases.

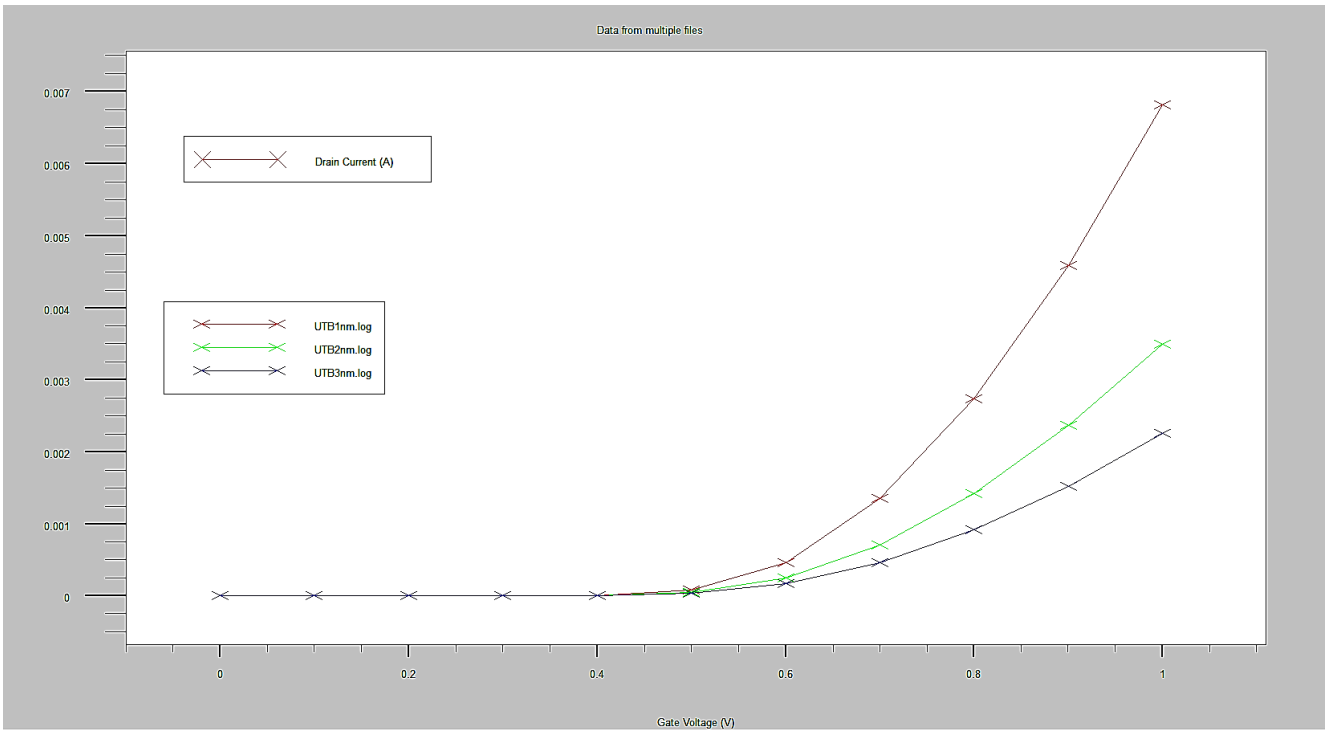

Fig.2.3 (d) Effect of Oxide thickness

Effect of Buried oxide (Tox2) :

If the body voltage is less than source voltage then body terminal is going to attract more holes. So to start the channel now more voltage is required.The floating body effect also comes in picture here which happens because of variation in size of buried oxide.

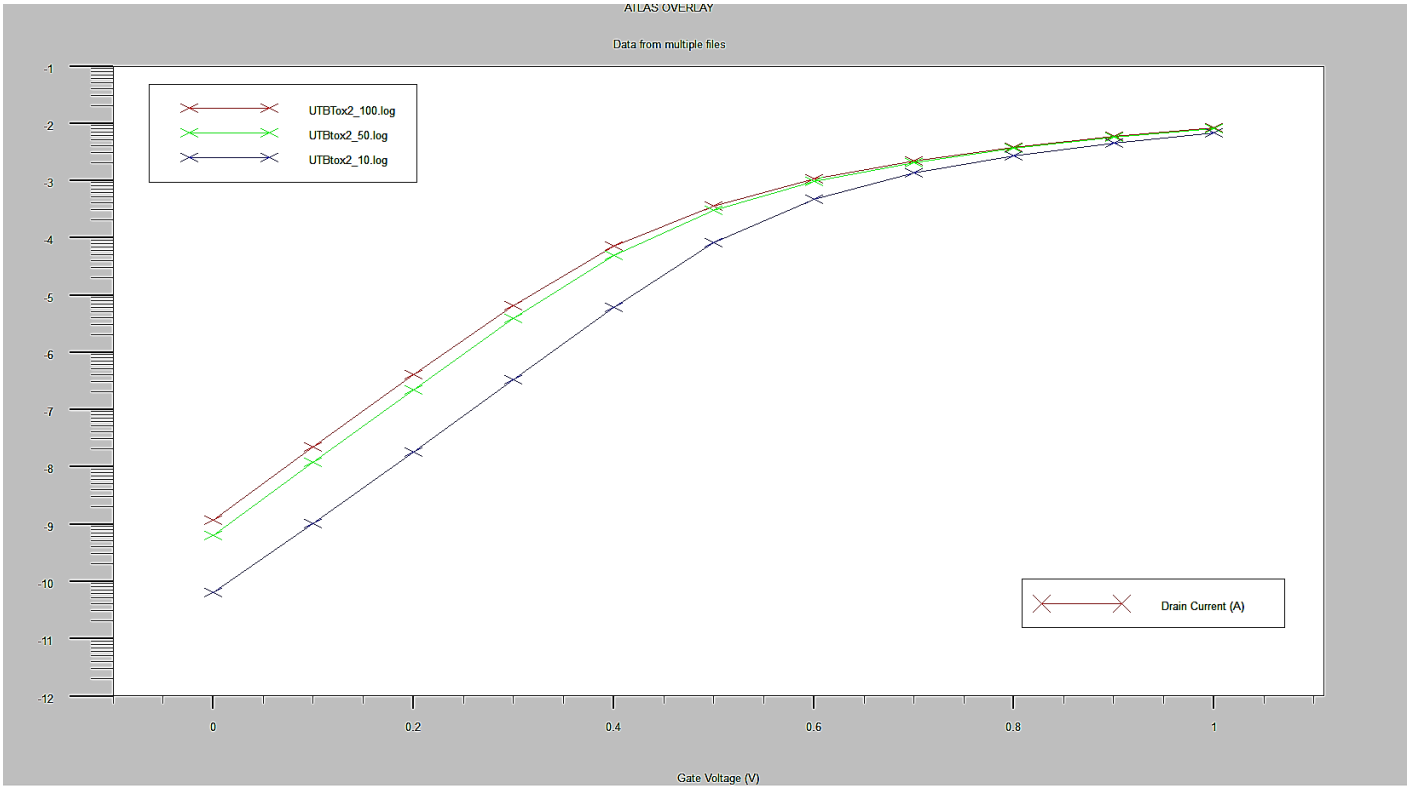

Fig. 2.3 (e) Effect of buried oxide thickness

The floating body effect is the effect of dependence of the body potential of a transistor realized by the silicon on insulator (SOI) MOSFETs. The transistor's body forms a capacitor against the insulated substrate. The charge accumulates on this capacitor and may cause adverse effects, for example, opening of parasitic transistors in the structure and causing off-state leakages, resulting in higher current consumption.

Chapter 3 : Conclusion and Scope for future work

As we have observed the characteristics of three nanoscale devices, which are PN Junction diode, MOSFET and Ultra Thin Body Body MOSFET. We have seen that all these nanoscale devices show thier different kind of I-V characteristics. And in chapter 2 we have briefly disscussed about the different types changes in chracter and functioning shown by these devices when subjected to some specific conditions or changes.

The evolution and revolution of semiconductor structures in recent years leading to micro-scale structures and nanoscale structures, have started revealing many new phenomena, such as quantum interference effects, tunneling effects, bandgap variations, for applications of new and novel functions. In concert with these efforts, we have conducted investigation on some of the nanostructures that bear potential for new functional devices leading to new applications in telecommunications and information technologies. These include formation of nanoscale semiconductor structures and measurements of their quantum mechanical properties. Nanoscale memories are used everywhere.The hunt is still on for universal memory that fits all the requirements of an "ideal memory" capable of high-density storage, low-power operation, unparalleled speed, high endurance**,** and low cost.