Large-area Y_2O_3-based Memristive Crossbar Array for Neuromorphic Computation

Ph.D. Thesis

By
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DEPARTMENT OF ELECTRICAL ENGINEERING
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A THESIS

Submitted in partial fulfillment of the
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DEPARTMENT OF ELECTRICAL ENGINEERING
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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **Large-area Y_2O_3-based Memristive Crossbar Array for Neuromorphic Computation,** in the partial fulfillment of the requirements for the award of the degree of **Doctor of Philosophy** and submitted in the **Department of Electrical Engineering, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from **December, 2017** to **September, 2022** under the supervision of **Prof. Shaibal Mukherjee**, Professor, Department of Electrical Engineering, IIT Indore and co-supervision of **Prof. Ajay Agarwal**, Professor, Department of Electrical Engineering, IIT Jodhpur.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

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Dedicated

to

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and

My Wife Dr. Shalu Rani

Specially Dedicated

to

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LIST OF PUBLICATIONS

A: Publications from Ph.D. thesis work

A1. List of Patents

1. *Silicon compatible yttria-based memristive crossbar array and a method of fabrication thereof*;
   Inventors: Shaibal Mukherjee, **Sanjay Kumar**, Mangal Das, Kumari Jyoti; Patent No. 202121013663, Published: June 25, 2021.

A2. In refereed journals

1. **Sanjay Kumar**, Rajan Agrawal, Mangal Das, Pawan Kumar, and Shaibal Mukherjee, "*Analytical Modeling of Y_2O_3-based Memristive System for Synaptic Applications*", Journal of Physics D: Applied Physics, vol. 53, no. 30, 2020. (**Impact Factor: 3.169**)
2. **Sanjay Kumar**, Rajan Agrawal, Mangal Das, Kumari Jyoti, Pawan Kumar, and Shaibal Mukherjee, "*Analytical Model for Memristive Systems for Neuromorphic Computation*", Journal of Physics D: Applied Physics, vol. 54, no. 35, 2021. (**Impact Factor: 3.169**)
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4. **Sanjay Kumar**, Ajay Agarwal, and Shaibal Mukherjee, *"Electrical Performance of Large-area Y_2O_3 Memristive Crossbar Array with Ultralow C2C Variability"*, IEEE Transactions on Electron Devices, vol. 69, no. 7, 2022. **(Impact Factor: 3.221)**
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A3. In refereed conferences

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2. **Sanjay Kumar**, Mangal Das, Rajan Agrawal and Shaibal Mukherjee, "*Impact of Grain Surface Area on the Performance of Yttria-based Memristive System*", 20th International Workshop on Physics of Semiconductor Device: IWPSD 2019, Kolkata, India, Dec. 17th-20th, 2019.
3. **Sanjay Kumar**, Mangal Das, Kumari Jyoti, Amit Shukla, Abhishek Kataria, and Shaibal Mukherjee, "*Analytical Modelling of Y_2O_3-based Memristive System for Artificial Neuron*", 5th International Conference on Emerging Electronics (ICEE 2020), IIT Delhi, India, Nov. 26th-28th, 2020.
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B1. In refereed journals

1. Mangal Das, Amitesh Kumar, **Sanjay Kumar**, Biswajit Mandal, Md. Arif Khan and Shaibal Mukherjee, "*Effect of Surface Variation on the Performance of Yttria based Memristive System*", IEEE Electron Device Letters, vol. 39, no. 12, 2018. (**Impact Factor: 4.221**)
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B2. In refereed conferences

1. Mangal Das, Amitesh Kumar, **Sanjay Kumar**, Biswajit Mandal and Shaibal Mukherjee, "*Effect of Schottky Junctions in Y_2O_3 Based Memristive Devices*", 4th International Conference on Emerging Electronics (ICEE), CeNSE, IISc, Bangalore, December-2018.
2. Amitesh Kumar, Mangal Das, **Sanjay Kumar**, Ritesh Bhardwaj, Md. Arif Khan, Abhinav Kranti and Shaibal Mukherjee, "*Role of interface anomalies in DIBS fabricated ZnO based RRAM exhibiting Quantum conductance*", 4th International Conference on Emerging Electronics (ICEE), CeNSE, IISc, Bangalore, December-2018.
3. Amitesh Kumar, Mangal Das, **Sanjay Kumar**, Ruchi Singh, Pawan Kumar, Abhinav Kranti and Shaibal Mukherjee, "*Role of interface modulation during resistive switching for ZnO based RRAMs*", 1st Indian Materials Conclave and 30th Annual General Meeting of MRSI (MRSI-AGM), IISc Bangalore, Feb-2019.
4. Mangal Das, Amitesh Kumar, **Sanjay Kumar**, Biswajit Mandal, Pawan Kumar and Shaibal Mukherjee, "*Impact of Schottky junction on the resistive*

switching of yttrium oxide", 9th International Conference on Key Engineering Materials, Oxford University, United Kingdom, March 29th-April 1st, 2019.

5. Amitesh Kumar, Mangal Das, **Sanjay Kumar**, Ruchi Singh, Pawan Kumar, Abhinav Kranti and Shaibal Mukherjee, "*Dual Ion Beam Sputtered RRAMs Exhibiting Quantum Conductance*", Materials Research Society (MRS) Spring Meeting, Phoenix, Arizona, USA, April 22th-26th, 2019.
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7. Mangal Das, Amitesh Kumar, **Sanjay Kumar**, Biswajit Mandal, Pawan Kumar and Shaibal Mukherjee, "*Impact of Metal/Semiconductor Junctions in the Resistive Switching of Yttria Based Memristive System*", Materials Research Society (MRS) Spring Meeting, Phoenix, Arizona, USA, April 22th-26th, 2019.
8. Mangal Das, **Sanjay Kumar**, Md. Arif Khan, Biswajit Mandal, Myo Than Htay, and Shaibal Mukherjee, "*Effect of roughness on the resistive switching of yttrium oxide-based system*," 7th International Symposium on Organic and Inorganic Electronic Material and Related Nanotechnologies (EM-NANO), Nagano, Japan, June 19th-22th, 2019.
9. Mangal Das, **Sanjay Kumar**, Amitesh Kumar, Biswajit Mandal, and Shaibal Mukherjee, "*Effect of roughness on the resistive switching of yttrium oxide-based system*", 10th International Conference on Materials for Advanced Technologies (ICMAT), Singapore, June 23th-28th, 2019.

B3. Book chapter:

NA

TABLE OF CONTENTS

Chapter 7 Conclusion and Future Perspective

LIST OF FIGURES

LIST OF TABLES

ACRONYMS

MCA	*Memristive Crossbar Array*
D2D	*Device-to-Device*
C2C	*Cycle-to-Cycle*
3D	*Three-Dimensional*
CMOS	*Complementary Metal Oxide Semiconductor*
AI	*Artificial Intelligence*
STP	*Short-Term Plasticity*
LTP	*Long-Term Plasticity*
ANNs	*Artificial Neural Networks*
RRAM	*Resistive Random-Access Memory*
RS	*Resistive Switching*
NVM	*Non-volatile Memory*
LRS	*Low Resistance State*
HRS	*High Resistance State*
TMO	*Transition Metal Oxide*
Y_2O_3	*Yttrium Oxide*
DIBS	*Dual Ion Beam Sputtering*
DC	*Direct Current*
I-V	*Current-Voltage*
HRTEM	*High Resolution Transmission Electron Microscopy*
FESEM	*Field Emission Scanning Electron Microscopy*
C-AFM	*Conductive-Atomic Force Microscopy*
PVD	*Physical Vapor Deposition*

LLC	*Load Lock Chamber*
MED	*Maximum Error Deviation*
SMU	*Source Measurement Unit*
CFs	*Conductive Filaments*
OBPU	*One Bit line Pull Up*
ABPU	*All Bit line Pull Up*
PBPU	*Partial Bit line Pull Up*

NOMENCLATURE

φ	*Flux*
q	*Electric charge*
$v(t)$	*Voltage*
$i(t)$	*Current*
$R(q)$	*Memristance*
ω	*Frequency*
V_{SET}	*SET Voltage*
V_{RESET}	*RESET Voltage*
$x(t)$	*State Variable*
$g(V(t))$	*Programming Threshold Voltage*
$f(w)$	*Window Function*
I_{CC}	*Compliance Current*

ABSTRACT

Large-area Y_2O_3-based Memristive Crossbar Array for Neuromorphic Computation

by

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In the last one decade, memristor which is also known as 'fourth fundamental circuit element' has attracted extensive attention as it offers numerous potentials applications in the next-generation non-volatile memory (NVM) technology. Memristor is the prominent candidate to replace conventional change-based flash memory technology in futuristic applications such as data storage and neuromorphic computation. Primarily, memristive devices offers several advantages as compared to conventional memories technologies such as its simple structure, ultrafast operational speed, energy efficient, high endurance and retention, high device production yield, three-dimensional (3D) integration capability to fabricate high density memory, low device-to-device (D2D), and ultralow cycle-to-cycle (C2C) variabilities. On the one hand, the design and validation of detailed non-linear analytical models for transition metal oxide (TMO) especially Y_2O_3 are extensively required to emulate the fundamental resistive switching response along with several neuromorphic characteristics of the memristive devices.

On the other hand, recent studies strongly suggest that Y_2O_3 can be an alternative option as a gate oxide material in thin-film transistor-based memory to replace SiO_2 as it offers numerous outstanding physical

properties such as: Y_2O_3 has high dielectric constant (~14-18) for frequencies (≤1 MHz) which is beneficial for applications in high-frequency oscillator, Chua's circuits, neuromorphic networks, and high-speed logical circuits. The lattice constant of the Y_2O_3 thin film is 10.60 Å which is very similar to that for Si substrate ($2\alpha_{Si}$ = 10.86 Å) that helps to achieve a smooth and uniform film surface which is highly desirable in case of memristive crossbar array fabrication. Y_2O_3 has a transparent nature over a broad spectral range (0.2-8 μm) which can be further used to fabricate transparent electronic memory for integrated transparent electronics. Moreover, Y_2O_3 shows the Schottky behavior with Al which plays a very crucial role in interfacial resistive switching mechanism.

However, a very few experimental reports are available on Y_2O_3-based memristive devices but the fabrication and detailed material and electrical investigation of Y_2O_3-based memristive crossbar array by utilizing dual ion beam sputtering (DIBS) system has not been reported to date. DIBS system offers several advantages such as produces high-quality thin films with reasonably better compositional stoichiometry, small surface roughness, excellent adhesion to the substrate even for films grown even at room temperature, and also offers large-area deposition for electronic device fabrication.

In this research work, the design of the non-linear memristive analytical models and further validation of these analytical models with experimental reported data are presented. These proposed models show better non-linear current profile at the device boundaries with least values of maximum error deviation (MED) i.e., 4.44% in the neuromorphic characteristics as corresponds to the experimental data which shows the robustness of the designed analytical models. The proposed model also has extendable capabilities to emulate the memory transition properties such as short-term memory (STM) to long term memory (LTM), and re-stimulation process in the artificial neurons. On the other hand, a three-dimension (3D) physical electro-thermal modeling has also been performed for the nanoscale Y_2O_3-based memristor device by considering internal Joule heating effect and

non-uniform distribution of electrical field inside the device by utilizing COMSOL Multiphysics. The simulated data show the perfect zero-crossing pinched hysteresis loop in its resistive switching characteristics which is purely dominated due to the formation and rupture of conductive filaments (CFs) inside the Y_2O_3-based resistive switching medium. The physical modeling also successfully depicted the impact of device switching speed (i.e., voltage ramp rate) over the cyclic variations, device switching parameters and synaptic characteristics of the memristor device.

Next, the detailed fabrication process, material, and electrical characterizations of the memristive crossbar arrays of (15×12) and (30×25) have been discussed. The fabrication of memristive crossbar arrays have been performed by utilizing DIBS systems which show better device interfaces as confirmed by high resolution-transmission electron microscopy (HR-TEM) outcome. Moreover, the fabricated crossbar arrays exhibit excellent resistive switching response with remarkable stability, repeatability, reproducibility in multiple switching cycles, high endurance up to 7.5×10^5 cycles, better retention (2.25×10^5 s), high production yield (92.67%), lower D2D (1.07%), and ultralow C2C (0.2%) variabilities in device switching voltages i.e., V_{SET} and V_{RESET}. The least values of D2D and C2C in V_{SET} and V_{RESET} are also favorable for the better thin film uniformity and smoothness which is also confirmed by HR-TEM analysis. The switching mechanism in the fabricated devices might be dominated due to device interfaces (mostly Al/Y_2O_3 Schottky interface) which is confirmed by conductive-atomic force microscopy (C-AFM) analysis. Furthermore, the fabricated devices in the crossbar array effectively show the device area scaling impact over the V_{SET} and V_{RESET} which further opens the way for fabrication of nanoscale device to increase the device density. Furthermore, the fabricated crossbar arrays have also exhibited the multi-level current programing states which further open the new way to store multi-bit data in a single memory cell as well as help to train the memory array with different set of alphabets digits. The fabricated array structures are also successfully demonstrated the synaptic and neuromorphic computation responses in terms of potentiation, depression and spike time

dependent plasticity (STDP) as analogous to the Hebbian learning rules of the biological system.

In the last chapter of this thesis, the read/write operational mechanism based on one bit line pull up (OBPU) scheme has been discussed which is performed on fabricated integrated 1S1R device configuration of (4×4) crossbar array. The fabricated devices in the crossbar array have effectively demonstrated read/write operation via device current mapping method in two different resistible states i.e., high resistance state (HRS) and low resistance state (LRS) which are represented as logic “0” and “1”, respectively, and write the name “HNRG” by considering current map in worst case scenario. Moreover, in this section of thesis, the training of memristive devices has also been demonstrated with multiple sets of alphabets by considering multilevel current programing scheme.

Chapter 1

Introduction: Basic Understanding of the Resistive Switching Phenomena in MCA Architecture

1.1 Background

In 1971, Chua [1] has postulated memristor as a fourth fundamental passive electrical circuit element in addition to resistor, capacitor and inductor which is established the physical link between flux (φ) and charge (q) as described in the later section of this chapter. Further, memristor element theory has been extended in 1976 [2] in which the memristor can store information in a form of resistance and the resistance history can be modulated by applying external electrical stimuli [1]. In 2008, Strukov *et al* [3] have physically realized the memristor device and established the strong link between memristor theory and physical resistive switching devices which is initially driven by the need for high-performance non-volatile memory and most recently accelerates the energy-efficient unconventional computing [4]. The typical structure of memristors is a two-terminal device and consisting resistive switching layer sandwiched between these two electrodes. For the resistive switching layer, various materials like semiconductor, inorganic insulator and organic materials have been utilized.

With the help of materials engineering, memristive devices can be categorised into two parts namely as; non-volatile or volatile memory. In the case of non-volatile memristor, the resistance state is maintained after the removal of the applied switching voltage or current while in the case of volatile memristor, its resistance state is not stable under the absence of external applied voltage or current. The stable resistance state is utilized to represent the stored information which makes memristive devices suitable for data storage applications [5]. The crossbar array architectures of the non-volatile memristive crossbar arrays are prominent candidates for future applications such as data storage [5], synaptic application [6], neuromorphic computation [7], hardware security [8] and analogous signal

and image processing application [9]. The aforementioned applications are only possible because memristive devices offer device area downscaling at the sub 2 nm scale [10] which open the new way to design and fabricate high density memristive crossbar array. The nanoscopic level memristive crossbar array possess many other desired properties, including high speed [11], high endurance and retention properties [12-13], high production yield [14], low energy consumption [15], low device-to-device (D2D) and ultralow cycle-to-cycle (C2C) variabilities [16], three-dimensional (3D) integration capability [13], and compatibility with complementary metal oxide semiconductor (CMOS) technologies [17].

Moreover, the non-volatile memristor are being developed to process the stored information for in-memory analog computation [18] which further offers an efficient and reconfigurable solution to process analog information in artificial intelligence (AI) applications [19]. While, the volatile memristor and its programable resistance state gradually relaxes toward a thermodynamically stable state under the absence of the programming voltage, offering desirable dynamics to mimic the biological synapses and neurons [10]. Furthermore, individual memristor has potential to show the short-term plasticity (STP) and long-term plasticity (LTP) as similar to the biological synapses [10, 20]. Artificial neural networks (ANNs) based on memristor crossbar array is also utilized to demonstrate brain-inspired functions [18].

In this chapter, we have comprehensively described the basic understandings of non-volatile memories, especially resistive random-access memory (RRAM) or Memristor [2]. The chapter also emphasizes the basic properties, operating principle, performance parameters, and advantages of the memristive crossbar array structure.

1.2 Resistive Random-Access Memory (RRAM) or Memristor

Currently, several non-volatile memories technologies such as phase-change random access memory (PCRAM) [21], magnetic random-access memory (MRAM) [22], ferroelectric random-access memory (FRAM)

[23], and resistive random-access memory (RRAM) [2] have been explored extensively to meet the current massive data storage and in-memory computation requirements. However, memory technologies like MRAM and FRAM face severe designing and technical obstacles during device downscaling. While, on the other hand, RRAM technology which is based on the resistive switching (RS) phenomena to alter the device resistance by modulating electrical bias has fascinated technical and commercial interests. Memristor is categorized under the broad category of RRAM as depicted in Figure 1.1.

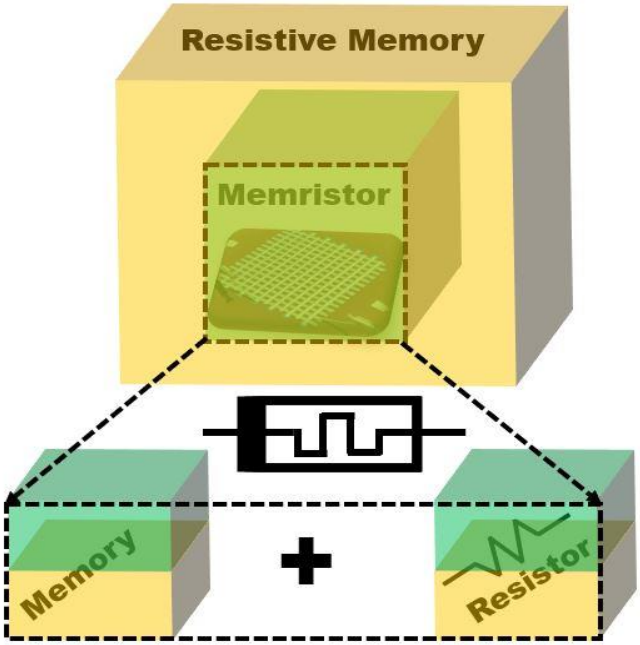

Figure 1.1: Schematic illustration of resistive memory and memristor.

Moreover, RRAM has attracted scientific attention from last one decade as a prominent candidate for non-volatile memory (NVM) due to its nanoscopic device size and simple device structure, energy efficient, fast operational speed (< 1 ns), and capability to offer 3D integration for high density [13, 24].

1.2.1 Mathematical Formulation for Memristor

In 1976, Chua [2] has proposed hypothesis for non-linear memristor [1] by establishing constitutive relationship between two mathematical variables

i.e., charge (*q)* and flux (*φ)* representing the time integral of the current, *i(t)*, and voltage, *v(t)* as described by equations (1) and (2).

$$q(t) \triangleq \int_{-\infty}^{t} i(\tau)d\tau \tag{1}$$

$$\varphi(t) \triangleq \int_{-\infty}^{t} v(\tau)d\tau \tag{2}$$

Here, it should be noted that the parameters 'q' and 'φ' are defined mathematically hence do not need to have any physical interpretations. It has considered that 'q' and 'φ' as a 'charge' and 'flux' of the memristor when equations (1) and (2) are associated with the formula related to the current, and flux to voltage, respectively. Assume that the memristor is charge-controlled or flux-controlled and if its constitutive relation can be defined by equations (3) and (4), respectively.

$$\varphi = \widehat{\varphi(q)} \tag{3}$$

$$q = \widehat{q(\varphi)} \tag{4}$$

where, $\varphi(q)$ and $q(\varphi)$ are continuous and piecewise-differentiable functions with bounded slopes. Next, differentiating equations (3) and (4) with respect to time *t*, and obtain the following equation (5).

$$v = \frac{d\varphi}{dt} = \frac{d\widehat{\varphi(q)}}{dq}\frac{dq}{dt} = R(q)i \tag{5}$$

where,

$$R(q) \triangleq \frac{d\widehat{\varphi(q)}}{dq} \tag{6}$$

Equation (6) represents the 'memristance' at *q*, and the unit of memristance is Ohms (Ω). A memristor shows pinched hysteresis loop in its resistive switching (RS) as depicted in Figure 1.2. Under the application of external voltage bias, a memristor shows resistive switching (RS) behavior in which device resistance switches between two distinct resistance states namely as: Low resistance state (LRS) and high resistance state (HRS) as illustrated in Figure 1.2.

1.2.2 Its Pinched Hysteresis Loop: 'Memristor Fingerprint'

An ideal memristor is a resistance state dependent device which shows perfect zero-crossing resistive switching response with pinched hysteresis loop [25]. The shape and hysteresis loop area of the resistive switching response are inversely proportional to operating frequency and decreases when operating frequency increases as depicted in Figure 1.2 which is the fingerprints of a memristive device. However, fast variation under excitation waveform cannot be responded due to device possesses some internal inertia hence, it settles at intermediate states which decreases the hysteresis loop area at higher sweep/ramp rates [25].

Figure 1.2 shows the pinched hysteresis loop in its resistive switching response. As seen from Figure 1.2, under the application of positive voltage bias memristive device switches from HRS to LRS and this process is termed as "SET process" and voltage defined at this stage is 'V_{SET}' [26]. On the other hand, under the negative voltage bias device turns back from LRS to HRS and this process is known as "RESET process" and voltage defined at this stage is 'V_{RESET}' [26].

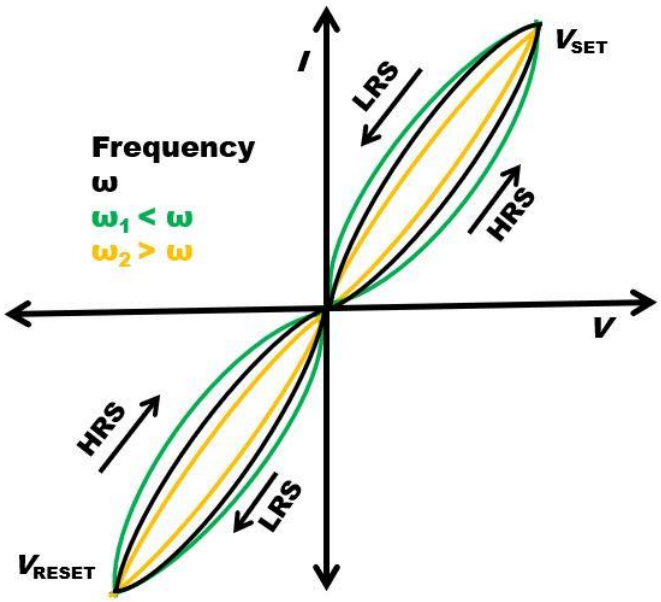

Figure 1.2: Memristive behavior in resistive switching response exhibiting pinched-hysteresis.

1.2.3 Resistive Switching Mechanisms

1.2.3.1 Electroforming

In the electroforming process, an electronically conductive path is formed throughout the dielectric layer (or resistive switching layer) under the application of a relatively high electric field [27]. The formed conductive path either based on metallic ions (in case of active metal electrode) or combination of oxygen vacancies or defects (in case of defect rich switching layer) [28]. It is widely accepted that the electroforming involves a defect-induced soft dielectric breakdown due to the heating and field accelerated bond rupturing [29] processes.

More specifically, under the application of external strong electric field the chemical bonds inside the dielectric layer are ruptured and this allows the formation of a conductive channel via vacancies flow towards opposite polarity according to the thermochemical dielectric breakdown theory [28]. The polarity of the applied electric field decides the orientation of the conductive channel. Hence, before commencing the resistive switching process in the memristive device, an electroforming process is performed to switch the pristine memory device to the high conductive state. Moreover, in electroforming process abrupt 'SET process' is happened which further increases the device variability.

1.2.3.2 Interfacial or Electroforming-free

The interfacial switching mechanism is also termed as 'homogeneous switching' which is based the modification of the Schottky barrier height between the metal electrode and the dielectric layer when oxygen vacancies (V_O^{2+}) are attracted or repealed from the metal contact under the application of an electric field [30]. Interfacial switching mechanism can be modelled as a one-dimensional (1D) problem in which V_O^{2+} concentration is modified along the vertical axis of the device. Moreover, interfacial switching mechanism-based devices have shown remarkable performances in terms of variability and controllability that make them prominent candidates for applications in analog or neuromorphic computing [31].

More specifically, under the influence of large electric voltage bias at the metal/oxide interface, large numbers of electrons are accumulated (extracted) into (from) the interface states under reverse (forward) bias. Accordingly, the net variation in charge at the interface states leads to a modification of a Schottky-like barrier width and/or height, because the degree of the band bending is dependent on a net charge in the interface states [26].

1.2.4 Types of Resistive Switching

The resistive switching (RS) process in the memristive device is directly underline by non-volatile and reversible change in resistance under the application of external electrical stimulus. The resistive switching behavior in memristive device can be categorized into two parts namely as: (i) bipolar and, (ii) unipolar**.** In the case of bipolar resisitve switching, the opposite voltage polarities are required for the SET and RESET processes, as depicted in Figure 1.3. While, in the case of nonpolar or unipolar resisitve switching, the SET and RESET processes are associated with either positve or negative polarity of the applied voltage bias [26], as shown in Figure 1.3.

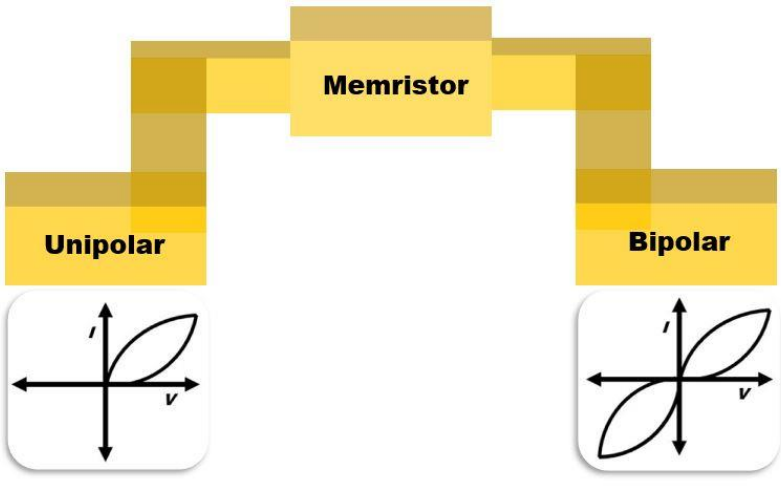

Figure 1.3: Types of resistive switching based on voltage polarities.

1.2.5 Performance Parameters for Resistive Switching

1.2.5.1 Resistance Ratio

It is the ratio of the resistance states i.e., HRS and LRS of the memristive device and defines as the high resistance state (HRS) to the low resistance state (LRS). It plays a very important role in memristive devices, as it directly affects the performance of the device during programming and erasing schemes [2, 24].

1.2.5.2 Endurance

Memristive devices have to be togged between HRS and LRS frequently during read/write processes and each read/write operations may initiate permanent damage or generally assumed as degradation. Endurance defines the number of SET/RESET cycles that can be sustained before the HRS and LRS are no longer defined separately. Therefore, a high value of endurance is more desirable for highly stable memristive devices [2].

1.2.5.3 Retention

It is the ability of the memristive device to retain a state over time. Further, it is the time duration in which memristive devices will stay in one stable state after programming or erasing [2, 32] which further denotes the intrinsic ability of a memristive device.

1.2.5.4 Variability

It is described by the coefficient of variation (C_V) and can be calculated by the ratio of standard deviation (σ) to mean value (μ) [33]. C_V can be evaluated by considering variations in the switching voltages i.e., V_{SET} and V_{RESET} and resistance values in HRS and LRS of the memristive devices. Further, it is associated with the D2D and C2C in the memristive crossbar array and the value of the coefficient of variation should be minimized for the highly stable memristive crossbar array [16].

1.2.5.5 Density

It is defined as the total number of devices in the single unit area. High-density memristive devices are more desirable for industry-scale applications. The memristive crossbar array offers 3D integration capability to ensure the high density and further, has the possibility of scalability to build a higher dense memory array [16, 33].

1.2.5.6 Device Production Yield

The device production yield, one of the crucial parameters in a crossbar array, describes the percentage of working devices on a wafer-scale in comparison to total fabricated devices during a single fabrication process [16]. It is important to note that the production device yield in the memristive crossbar array signifies an ambitious scientific importance to further decline the device manufacturing cost significantly.

1.2.6 Resistive Switching for Neuromorphic Applications

1.2.6.1 Synaptic Plasticity

Firstly, the idea of synaptic plasticity has proposed by psychologist Donald Hebb [30]. In general, the plasticity is the functionality of the brain to change and adapt to new information. Similarly, synaptic plasticity is the temporary change in the synapse between two neurons which allow neurons to communicate to each other and transfer the information from pre-synapse to post-synapse [22]. The strength of communication between two neurons can be dependent on synapse plasticity which further linked to other neurons for volumetric conversation. The volumetric conversation of the synapse is not static, but rather can change in both the short term and long term [22].

Synaptic plasticity refers to these changes in synaptic strength. The ability of change in synaptic weight is called synaptic plasticity and it is a key mechanism pursued by the human brain in learning process [23]. Figure 1.4 shows the critical components of a biological neural network, which

consists neurons and synapse alongside with numerous biological units. The synaptic plasticity can be divided into two parts such as:

1. Short-term plasticity (STP)
2. Long-term plasticity (LTP)

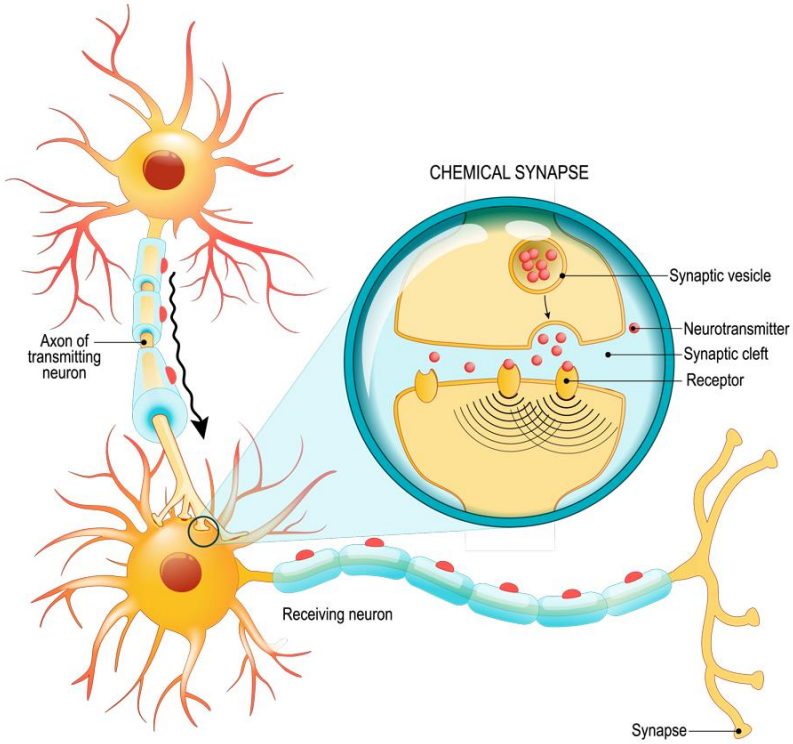

Figure 1.4: Biological neural network components for neural conversation. Credit: https://researchoutreach.org/articles/cryo-electron-tomography-synaptic-transmission-brain/.

1.2.6.1.1 Short-Term Plasticity (STP)

It is defined by the rapid changes (either increase or decrease) in synaptic strength over a minute. Specifically, STP shows a rapid, bidirectional and reversible change in synaptic strength and it is believed to serve as a key mechanism for modifying synaptic and circuit functions during computation.

1.2.6.1.1 Long-Term Plasticity (LTP)

Long-term plasticity is described by a long lasting (from minutes to hours), activity-dependent change in synaptic efficacy. LTP can be considered as

bidirectional and synaptic strength either strengthening in case of long-term potentiation (LTP) or debilitating in case of long-term depression (LTD). It defines how humans create and remember new memories.

1.3 Yttrium Oxide as Switching Material

In the past one decade, several transition metal oxides (TMOs) materials systems such as TiO_2 [34], HfO_2 [35], SiO_2 [36], ZnO [37] and Ta_2O_5 [38] have been extensively explored to design and fabricate memristive crossbar array. However, the aforementioned TMOs-based memristive device have several performance issues in terms of lower thermal stability, higher D2D (>15%) and C2C (>10%) variabilities, and poor retention data ($<10^5$) [34-37]. Ta_2O_5-based memristive device shows highest value of endurance cycles (10^{12}) in the case of all TMOs materials [38]. Most recently, Y_2O_3 has also been extensively considered [26, 39-41] to the memristive devices because it has some excellent physical properties which are outline below:

i. Y_2O_3 has high dielectric constant (~14-18) for frequencies (≤1 MHz) [39] which is beneficial for applications in a high-frequency oscillator, Chua's circuits, neuromorphic networks, and high-speed logical circuits [42].
ii. The lattice constant of the Y_2O_3 thin film is 10.60 Å which is very closed to that for Si substrate ($2\alpha_{Si}$ = 10.86 Å) [39]. The lower lattice mismatch between Y_2O_3 and Si is more favorable to achieve a smooth and uniform thin film surface [43] which is highly desirable in case of memristive crossbar array fabrication.
iii. Y_2O_3 has a transparent nature over a broad spectral range (0.2-8 μm) [44] which can be further used to fabricate transparent electronic memory for integrated transparent electronics [45].
iv. Moreover, Y_2O_3 shows the Schottky behavior with Al which is played a very crucial role in interfacial resistive switching mechanism [26, 39].

These aforementioned physical properties of Y_2O_3 makes it more suitable materials candidate to fabricate memristive crossbar array structure. Moreover, Y_2O_3 has also been investigated as a gate oxide material to

replace SiO_2 in thin-film transistor-based memory devices [39] because SiO_2 are highly unreliable due to high density of pinholes [39] and larger tunneling currents [39], which reduces device yield and low breakdown strength. Figure 1.5 depicts the cubic structure of the Y_2O_3 which has been utilized as a resistive switching material in this research work.

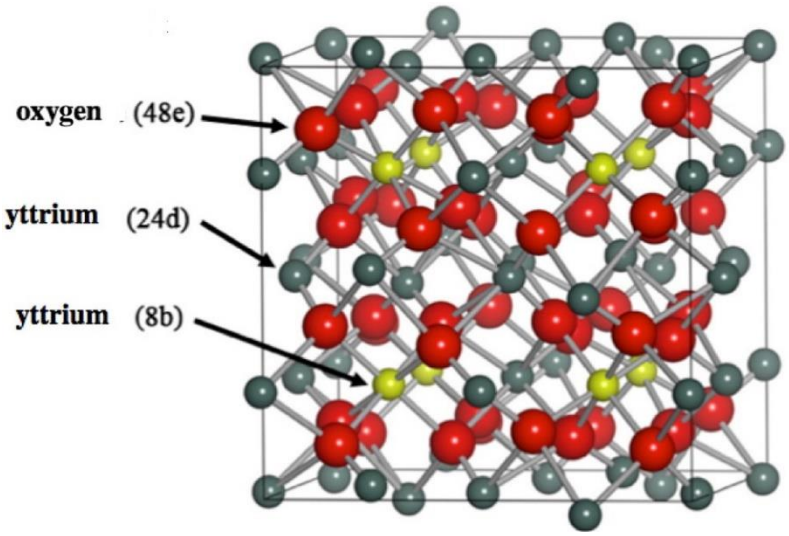

Figure 1.5: The cubic structure of yttrium oxide [46].

1.4 Aim and Objective

It is very difficult to fabricate memristive devices which shows interfacial (electroforming-free) resistive switching behavior as interfacial switching mechanism-based devices show remarkable performances in terms of variability and controllability that make them prominent candidates for applications in analog or neuromorphic computing. The design and validation of the analytical and physical modeling for neuromorphic computation and device fabrication parameters such as device production yield, endurance, resistance ratio, D2D and C2C variations in device V_{SET}, V_{RESET}, are the matter of concern in the case of the memristive crossbar array. To the best of our knowledge, the experimentally validated high accuracy analytical and physical memristive models and fabrication of yttria based memristive crossbar array by utilizing dual ion beam sputtering (DIBS) system has not been reported elsewhere to date. The main aim of this thesis is to design and validation of memristive analytical and physical models and realization of Y_2O_3-based memristive crossbar for non-volatile

memory and neuromorphic computing applications by utilizing MATLAB, COMSOL Multiphysics and sputtering techniques, respectively, and study the numerous memristive device characteristics. This research work includes the multiples objectives which are outlined below:

i. Extension of the previous reported studies on different yttria-based resistive switching devices and understand the various design methodologies of resistive switching device, which are related to memristive device performance parameters.

ii. Design and validation of memristor analytical models with remarkable accuracy and explores the various neuromorphic characteristics via these validated models.

iii. 3D physical electro-thermal modeling of nanoscale Y_2O_3-based memristor device for real synapse application by considering internal Joule heating and non-uniform electrical distribution via COMSOL Multiphysics.

iv. Fabrication of yttria based memristive crossbar array device by utilizing DIBS as it offers smooth, uniform and economically viable deposition which can be used for large-area fabrication.

v. Investigation of the various memristive characteristics such as stability in resistive switching response, endurance and retention properties, device production yield, and device area downscaling effect on device current on fabricated memristive devices.

vi. Analysis of multilevel current programming functionality, synaptic leaning, and spike time dependent plasticity (STDP) characteristics as analogous to the Hebbian learning rules similar to the biological system.

vii. Analysis of D2D and C2C variabilities in fabricated memristive crossbar array devices to investigate the performance of the crossbar array structure.

viii. Study of read/write scheme in fabricated crossbar array via device current mapping method and also discussed the writing of array for different alphabets digits by considering multilevel current programming functionality.

1.5 Organization of the Thesis

The research work reported in this thesis is focused on the design and validation of analytical and physical memristive device models and realization of yttria-based memristive crossbar array by utilizing DIBS system. The fabricated crossbar array has remarkable properties such as electroforming-free nature in the resistive switching responses, high stable, reproducible, repeatable, high endurance, better retention, multilevel current functionality, synaptic learning, spike time dependent plasticity (STDP), high production yield and low D2D and ultralow C2C variability in the switching voltages. The thesis is organized as follows:

Chapter 2 illustrates the various instruments and tools utilized for fabrication and characterizations of the memristive crossbar array.

Chapter 3 explains the detailed analytical and physical electro-thermal modeling of the Y_2O_3-based memristive devices. This chapter also outlined the device fabrication aspects as compared to previous studies in this field.

Chapter 4 provides the comprehensive details of various modeled results, various material and electrical characterizations of the fabricated memristive crossbar array by utilizing various external electrical stimuli. It also illustrates other characterization details concerning various aspects of RS response.

Chapter 5 explains the statistical distribution analysis and cumulative distribution function (CDF) for coefficient of variability in D2D and C2C.

Chapter 6 describes the read/write operation in the fabricated crossbar array structure as well as writing of the memristive array for alphabets digits by implementing multilevel current programing functionality.

Chapter 7 presents the conclusion and future perspective of the fabricated memristive crossbar array.

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Chapter 2

Fabrication and Characterization Systems for Y_2O_3-based MCA

In this chapter, the dual ion beam sputtering (DIBS) system and direct-current (DC) magnetron sputtering system which are primarily used for the oxide thin film and metal thin film deposition, respectively, and several characterization techniques, which are used to investigate the yttria-based memristive crossbar array, have been described in detail. Numerous characterization techniques are utilized to evaluate the structural, morphological, and electrical properties of the yttria resistive switching layer. The digital optical microscopy is utilized to investigate the alignment of each deposited layer in the fabricated crossbar array structure. The electrical properties of the memristive devices in the fabricated crossbar array is carried out by using the current-voltage (*I*-*V*) measurement system (Keithley 4200A-SCS semiconductor parameter analyzer). The quality of the various materials interfaces has been analyzed by utilizing the high resolution-transmission electron microscopy (HR-TEM) measurement. The quality of the surface morphology of the top surface of the yttria switching layer is investigated by field emission-scanning electron microscope (FE-SEM) images. The conductive-atomic force microscopy (C-AFM) is utilized to confirm the dominating resistive switching mechanism in the fabricated crossbar array via current distribution mapping under different voltage bias. Here, we have discussed all these utilized systems in detail.

2.1 Thin Film Deposition Tools

In this research work, the growth of the polycrystalline and amorphous Y_2O_3, and Ga-doped ZnO to fabricate yttria-based memristive crossbar array on Si substrate, Elettrorava-DIBS system is used. For the metal electrode deposition i.e., Aluminium (Al), DC-magnetron sputtering (Excel Instruments) is utilized. The following sub-sections are described the DIBS and DC-magnetron sputtering systems in detailed manner.

2.1.1 Dual Ion Beam Sputtering (DIBS) System

DIBS system is one of the most important physical vapor depositions (PVD) technique which is used to deposit either oxide or metal thin film under ultrahigh vacuum environment [1]. DIBS system is well equipped with a radio-frequency (RF) deposition ion beam source and a direct-coupled (DC) assist ion source, as depicted in Figure 2.1. The RF ion source is primarily utilized to sputter target materials, which is fixed in a four-target assembly. The DC assist ion source helps to clean the surface of the substrate prior to film deposition also can be utilized to remove the native oxide layer from the substrate prior thin film deposition. It also hinders the island formation and removes the weak dangling bonds during the thin film deposition [2]. The angle between the deposition ion source and the sputtering target is fixed at 45^{o} off normal while the angle between the assist ion source and the substrate assembly is maintained at 60^{o}. DIBS system offers the following numerous benefits as compared to other sputtering systems:

1. DIBS system produces high-quality thin films with reasonably better compositional stoichiometry, low surface roughness, provides excellent adhesion even at room temperature and better deposition quality for large-area electronic device fabrication [3].

The schematic of a whole DIBS system is shown in Figure 2.1, while Figure 2.2 depicts the digital camera image of the original DIBS assembly. The main components of this system include RF (deposition) ion source, assist ion source, a deposition chamber, load lock chamber, two vacuum turbopumps, different types of vacuum gauges, a substrate heater assembly, a water chiller and a controlling unit [2].

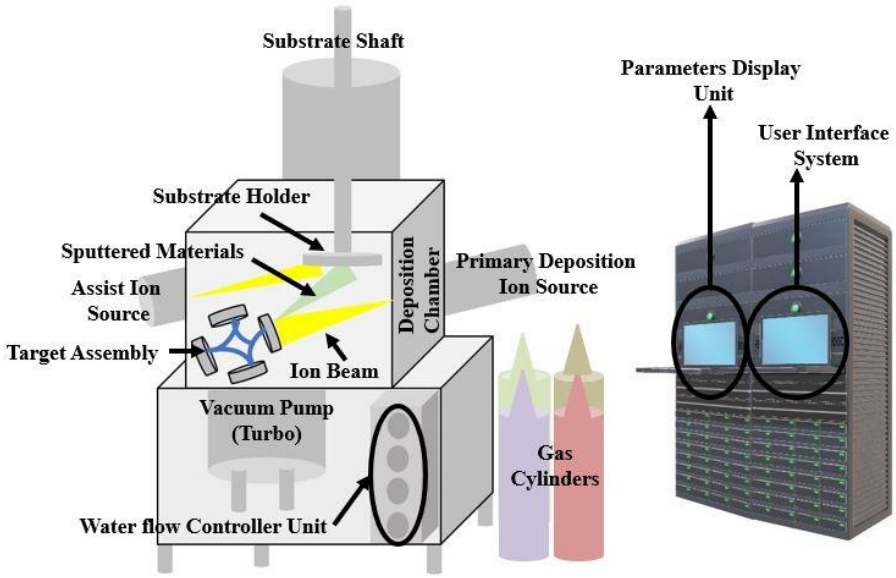

Figure 2.1: The schematic of dual ion beam sputtering (DIBS) system.

In the DIBS system, both ion sources are manufactured by Kaufman and Robinson which produce a cation ion beam. The produced ion beam is spatially well confined and mono-energetic [4]. Fundamentally, RF ion source creates a plasma of Ar gas which consists with the help of grids. The RF deposition ion source consists of three main parts namely as: (i) the discharge chamber, (ii) grids, and (iii) neutralizer. The Ar ions are generated inside the discharge chamber under the Ar gas environment subjected to an RF field. The ionization process starts when gas is reached into a small isolated quartz/alumina chamber, which is surrounded by an RF powered coil. The created RF field excites outermost electrons of Ar gas atoms until they gain sufficient energy to break away from gas atoms, and creates the plasma of cations and electrons; this process is termed as 'inductive coupling'.

Figure 2.2: Digital camera image of the DIBS system.

These ions are considered as a beam from the discharge chamber under the application of the various voltage biases on the grids. Usually, the deposition source consists of three grids to extract ions which help to reduce the chances of beam spread. The neutralizer also known as 'hollow cathode' is an electron source, which is utilized to neutralize the generated positive ion beam [4]. The schematic block diagram of the deposition ion source is depicted in Figure 2.3.

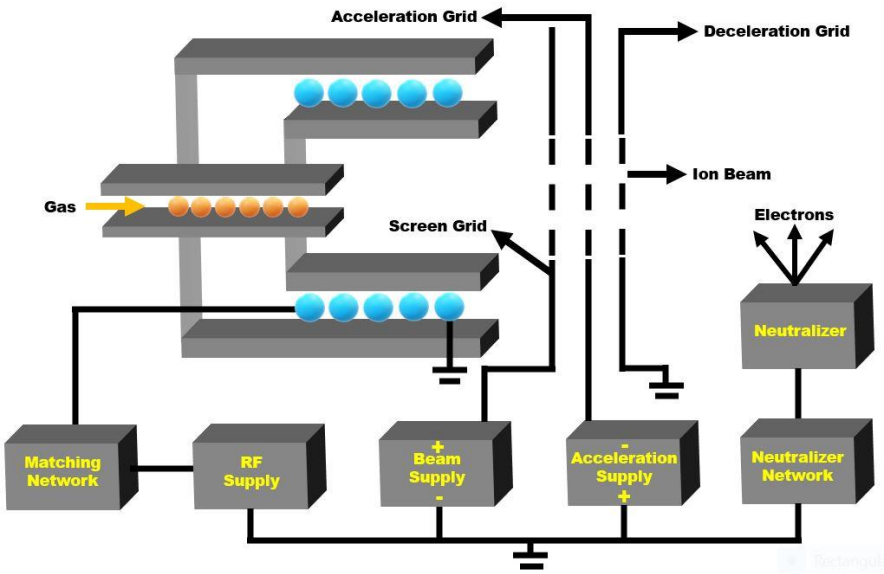

Figure 2.3: Schematic block diagram of ICP40 ion deposition source of DIBS system.

The assist ion source is also consisted of two main parts namely as; (i) End-Hall 400 ion source module and (ii) a neutralizer. This system has three types of power supplies which are mentioned below:

1. Keeper power supply
2. Emission power supply
3. Discharge power supply.

Keeper and emission power supplies are associated with the neutralizer while the discharge power supply is connected with the End-Hall 400 ion source module to provide voltage and current for generating a positive ion beam. This type of cost-effective assist ion source assembly offers some advantages like broad ion-beam coverage, large ion-current capabilities, and excellent reliability. The large ion-current capabilities of assist ion source allow sufficient etch rates [2] even at low ionic energy (≥ 200 eV). Here, Figure 2.4 depicts the schematic block diagram of the assist ion source assembly of the DIBS system. The keeper power supply is connected with hollow cathode neutralizer assembly to provide voltage and current and allows it for thermionic emission of electrons [2] from the keeper plate by igniting and keeping the keeper plate hot during the operation. The emission power supply starts after the keeper power supply

which ignited the hollow cathode and then the emission power supply provides a negative voltage to the hollow cathode unit to control the electron beam. The electron beam neutralizes the positive ions beam which are emitted from the End-Hall 400 ion source of the assist ion source.

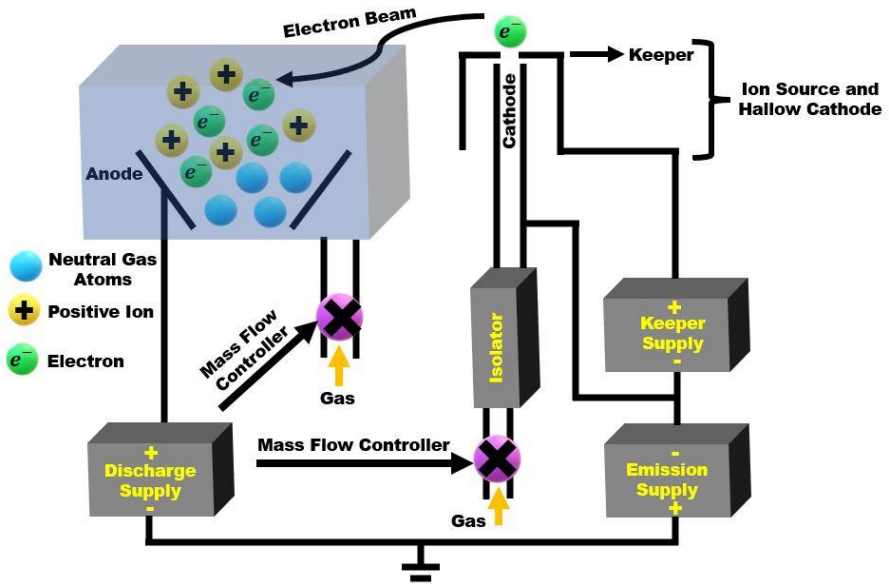

Figure 2.4: Schematic block diagram of EH400 assist ion source unit of DIBS deposition system.

The materials growth processes are performed inside the deposition chamber of the DIBS system which is mostly made up of stainless steel as it is non-corrosive, non-magnetic, easy to weld and clean, highly malleable, and has excellent outgassing characteristics [2]. The deposition chamber consists of a numerous port to perform different functions and small viewing windows of the Pyrex glass to visualize the realistic view of the generated plasma during operation. The load lock chamber (LLC) is a small vacuum enabled chamber which is directly connected with main deposition chamber that permits the loading of the substrate into the deposition chamber without perturbating the vacuum level of the deposition chamber. A robotic arm is used to load or unload the sample from the LLC to main deposition chamber. The DIBS system is also equipped with the sets of several rotary and turbomolecular vacuum pumps which are used to create an ultra-high vacuum inside the deposition chamber and load lock chamber. The level of vacuum is measured by different vacuum gauges. The heater

assembly is fixed over the substrate holder inside the main chamber which is used to heat the substrate up to 1000 °C. The heater assembly allows in-situ annealing of the deposited thin film at elevated temperatures during the material growth. A water chiller unit is also associated with the DIBS system to reduce the temperature inside the deposition chamber and target assembly and helps to prevent system overheating issues during the material growth. The several growth parameters such as deposition temperature, gas partial pressure, and RF power are controlled by a controlling unit [1-2].

2.1.2 Direct-Current (DC) Magnetron Sputtering System

DC-magnetron sputtering system is a one of the promising physical vapor deposition techniques which is primarily used for the metal electrode deposition. In DC-magnetron sputtering, Ar gas plasma is created under the application of a high DC electrical voltage, and positively charged ions (Ar^+) from the gas plasma are accelerated towards the negatively charged 'target' assembly. For these positively charged Ar ions, an acceleration voltage in the range of few hundred to a few thousand electron volts is required. The high acceleration voltage helps Ar^+ ions reach the target assembly and strike them with sufficient energy to remove atoms from the target materials [5]. The Ar^+ atoms are ejected in a typical line-of-sight cosine distribution on the target surface and highly condensed near to the target surface as the target assembly has a permanent magnet to bind them closely.

Moreover, the presence of a strong magnetic field at the target assembly helps to enhance the initial ionization process and creates the plasma at lower pressure. The lower pressure operation overcomes the problem of background gas incorporation in the growing film and energy losses of the sputtered atom during gas collisions which improves the quality of thin film with faster deposition rates [5]. The experimental setup of DC-magnetron sputtering is depicted in Figure 2.5.

Figure 2.5: Experimental setup of DC-magnetron sputtering system.

2.2 Characterization Techniques

The several characterization techniques are utilized to characterize the fabricated memristive crossbar array in this research work which are explained in the following sections.

2.2.1 Digital Optical Microscopy System

The digital optical microscopy manufactured by Leica (DM2700 M) has universal white light (4500 K) LED illumination in combination with premier high quality Leica optics which provides the ideal inspection and outstanding image quality of the samples. The Leica DM2700 M shows how simple and reliable microscopy which helps to improve your workflow so you can concentrate on the task at hand. The key points of the Leica DM 2700 M are outlined as follows: (i) Brilliance, (ii) Reliability, (iii) Flexibility, and (iv) Easy Documentation.

It is mandatory for the microscope to have good optics unit. Leica digital microscopies are innovative, cost-effective, and provide high-contrast, pin sharp images as seen via eyepieces and captured with digital cameras. The

digital camera unit offers brilliance and sharp contrast with high resolution and optimized image fields. The microscopy setup is user-friendly and easy to understand the functionality.

Figure 2.6: Digital camera image of Leica DM2700M microscopy. Credit: https://www.leica-microsystems.com/products/light-microscopes/p/leica-dm2700-m/.

The Leica DM2700 M is a flexible upright microscope system and can be useful for Brightfield (BF), Darkfield (DF), Differential Interference Contrast (DIC), Qualitative Polarization (POL), and Fluorescence (FLUO) applications. Moreover, it can also be equipped with transmitted light.

In this research work, digital optical microscopy (Leica DM2700M) is used to view the realistic view of the fabricated crossbar array devices which also helps to analyze the perfect crosspoint structure in the crossbar array. Figure 2.6 depicts the digital camera image of the digital optical microscopy (Leica DM2700M).

2.2.2 Current-Voltage (I-V) Measurement System

The Keithley 4200A-SCS semiconductor parameter analyzer (SPA) is a vital characterization system to investigate the resistive switching response in terms of current-voltage relationship. The SPA-4200A SCS can be

utilized to study several parameters such as electrode area dependent device current, endurance, retention, and resistance ratio of the fabricated memory devices. The SPA-4200A SCS is also facilized with pulse model operation which is more preferable during endurance and retention measurements of the memory device. Figure 2.7 shows the digital camera image of the *I-V* measurement setup. The *I-V* measurement setup is equipped with the Everbeing cryogenic probe station with the temperature range of 80 K to 450 K and a SPA 4200A-SCS.

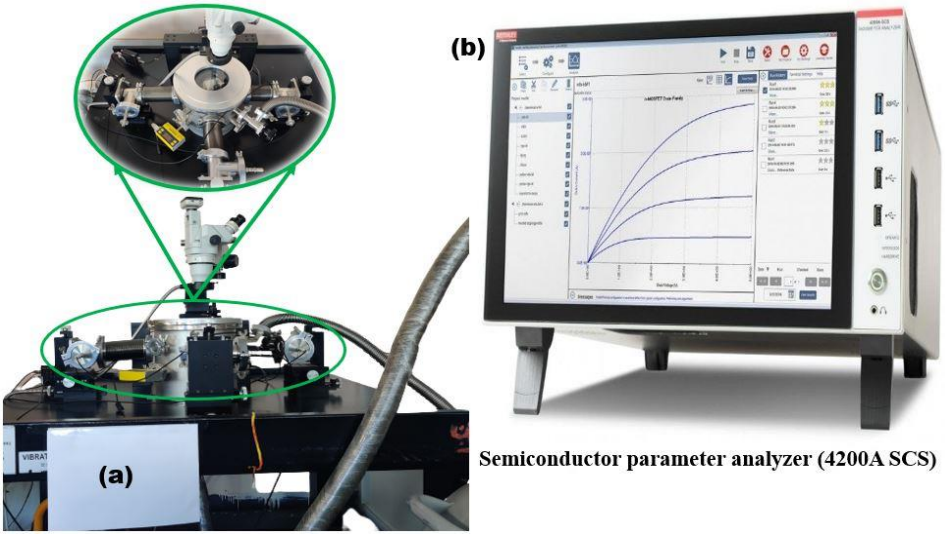

Figure 2.7: Photographs (a) Probe station and (b) Keithley 4200A-SCS semiconductor parameter analyzer.

The *I-V* measurement setup is fully capable to measure the thin-film samples with different sizes and shapes, but in our case, we have used complete 3-inch Si substrate for the crossbar array in which minimum and maximum device area is 0.24 mm^2 and 0.60 mm^2, respectively. The detailed utilization of *I-V* protocols is described in the later chapters of the thesis.

2.2.3 Field Emission-Scanning Electron Microscope (FE-SEM)

The field emission-scanning electron microscope (FE-SEM) creates high resolution images of the surface of any sample to scan the sample surface through focused high energy electron beam. The electron interaction with atoms present in the sample causes the emission of many secondary

electrons which can provide significant information about the topographical features of the surface and composition of the testing samples. In FE-SEM system, primary electrons are induced by a field emission source which is connected with the very high electrical field. FE-SEM creates clear and less electrostatically distorted images as compared to the conventional SEM. The electrons generated from the field emission gun are focused via a set of electronic lenses to produce a narrow beam of electrons which is bombarded on the samples in a random pattern. These uncountable collisions with sample induce the emission of secondary electrons from the surface of the samples. A FE-SEM system is equipped with a detector unit to detect these secondary electrons and generates an electronic signal. These electronic signals are further amplified and transformed into a video image.

Figure 2.8: Digital camera image of FE-SEM, Zeiss Supra 55. Credit: https://commons.wikimedia.org/wiki/File:SUPRA_55_(6908563989).jpg.

A FE-SEM can be used as a very high-resolution microscope, which can produce visualization of the topographic details below 100 nm scale on a sample. In this research work, the images of the top surface of Y_2O_3 switching layer are taken by FE-SEM, Supra55 Zeiss. The digital camera image of the actual system is depicted in Figure 2.8.

2.2.4 High Resolution-Transmission Electron Microscopy (HR-TEM)

High resolution-transmission electron microscopy (HR-TEM) is a specialized designed transmission electron microscope (TEM) which can be utilized for atomic level imaging of the sample. In TEM, an electron beam passes through a very thin (< 100 nm) sample. The passing electron beam interacts with the sample atoms to create the image of the sample. With the help of the TEM, we can get the morphological, compositional and crystallographic information of any sample. The created images by TEM have a very high resolution as compared to the light microscopes because it uses an electron beam that has a smaller De Broglie wavelength. The produced high-resolution images allow capturing very fine details such as a single column of atoms of the sample. TEM can be operated in several modes such as conventional imaging, scanning TEM imaging (STEM), diffraction, and spectroscopy. TEM is well equipped with many modules which are mentioned as follows:

1. A vacuum cavity system for traveling of the electrons beam.

2. Thermionic or field emission operatable electron emission source to generate electron beam into the vacuum.

3. A sets of electromagnetic lenses which are made of a solenoid coil, nearly surrounded by ferromagnetic materials.

In HR-TEM, the electrons are emitted from a filament and pass through the multiple electromagnetic lenses to form a beam shape. The electron speed is directly associated with the electron wavelength and determines the resolution of the created images. In HR-TEM, the interference pattern is utilized to create a phase-contrast image as an interference pattern is formed by the transmitted and the scattered beams. The captured image has a very high resolution which further helps to detect a single unit cell of the crystal. Moreover, HR-TEM is also utilized to investigate the crystal structures and several defects such as lattice deficiencies, point defects, stacking faults, dislocations, grain boundaries, and defect in different kinds of materials at atomic resolution [6].

In this research work, we have used HR-TEM to investigate the quality of various interfaces such as Y_2O_3/Si, BE GZO/insulating Y_2O_3, Y_2O_3 SL/GZO. Figure 2.9 depicts the digital camera image of HR-TEM system.

Figure 2.9: Digital camera image of HR-TEM system. Credit: https://jiam.utk.edu/core-facilities/microscopy/tem.

2.2.5 Conductive-Atomic Force Microscopy (C-AFM)

Conductive atomic force microscopy (C-AFM) is a widely accepted technique to investigate the topography of a thin film as well as the electric current distribution on thin film surface. The surface topography is investigated by sensing the deflection in the cantilever tip which is connected with the optical system (a combination of laser and photodiode). The current passing through the AFM tip is measured by using a current-to-voltage preamplifier unit because the tip current may be in pico-ampere level. In C-AFM, during surface topographical analysis, a conductive cantilever tip scans the thin film sample surface in contact mode to produce a surface topographical map, and the deviation in the electric current passing through the cantilever tip is measured to record the surface map. During C-AFM analysis, the testing sample is fixed on the sample-holder via conductive tape/paste.

In this research work, the quality of the Y_2O_3 thin film surface is investigated by utilizing C-AFM. The schematic of the C-AFM is presented in Figure 2.10. The conduction mechanism of our fabricated devices in the crossbar array has been verified using C-AFM. C-AFM is performed on the top surface of the resistive switching oxide layer of Y_2O_3 and the outcomes have been investigated to understand the switching behavior of the device under different amplitude of applied voltage. In this research work, Shimadzu, SPM-9500J3 C-AFM system with an Au coated Si_3N_4 probe has been utilized to study the surface morphology of the switching layer of Y_2O_3.

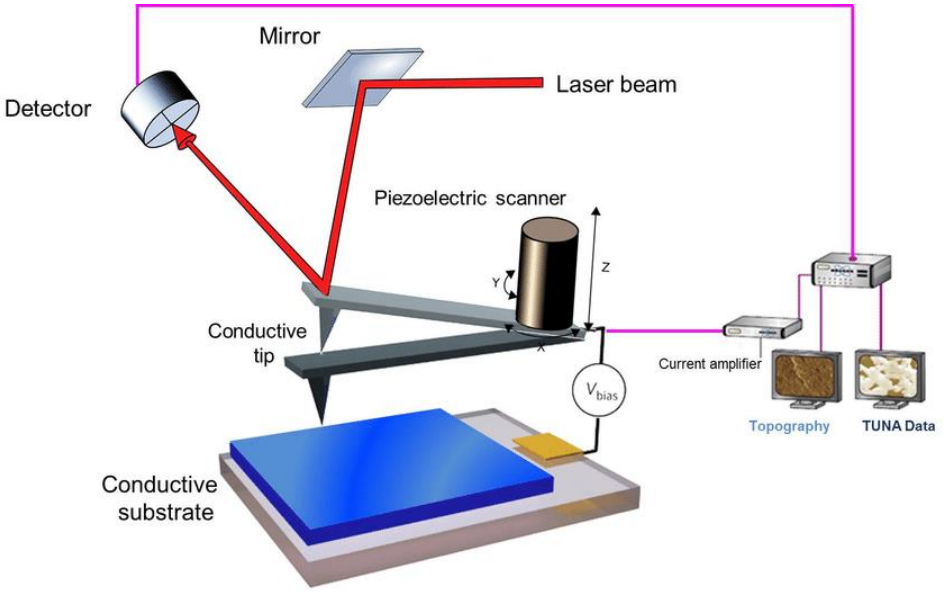

Figure 2.10: Schematic of conductive-atomic force microscopy (C-AFM). Credit: Valentina Castagnola, Implantable microelectrodes on soft substrate with nanostructured active surface for stimulation and recording of brain activities. Micro and nanotechnologies/Microelectronics, Universite Toulouse III Paul Sabatier, 2014. English. <tel-01137352>

2.3 References

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Chapter 3

Analytical and Physical Electro-Thermal Modeling with Crossbar Array Fabrication

3.1 Introduction

In 2008, Williams *et al* [1] have fabricated TiO_x-based memristive device and also designed an analytical model to capture the similar resistive switching response which was obtained through experimentally, for the first time in the world. Later, several analytical models [2-5] have been proposed which are based on different materials systems to replicate the resistive switching characteristics of the memristive devices. Further, a very few attempts have been performed to design and proposed the analytical models [3-4] and circuit simulators [2, 5] which are able to simulate the resistive switching response along with synaptic learning capabilities and neuromorphic characteristics in terms of potentiation and depression processes of the memristive systems. However, these previously reported analytical models [3-4] and circuit simulators [2, 5] have shown large maximum error deviation (MED) with the corresponding experimental data and some of these models [4-5] have not been validated experimentally. Therefore, we have designed and proposed generic analytical models that are able to capture the various memristive device characteristics with the realistic nature and show minimum error margin corresponding to experimental reports [2, 6]. Besides that, we have also performed the 3D physical electro-thermal modeling of nanoscale Y_2O_3-based memristor device wherein simulated outcomes exhibited the perfect zero-crossing resistive switching response under the application of the external electrical potential. The performed physical modeling is based on the free energy (FE) of the used materials at certain applied voltage and during the physical modeling, internal Joule heating and non-uniform distribution of electrical field have been considered as similar to the real memory devices which is not reported, till date in case of yttria-based memory device.

On the other hand, many oxide-based materials such TiO_x [7], InGaZnO

[8], ZnO [9], HfO_2 [10], Ta_2O_5 [11], and WO_x [2]) have been utilized to fabricate the memristive systems. There are very few attempts have reported to study Y_2O_3-based memristive systems [6, 12]. Yttria has widely been investigated as a gate oxide material in transistor-based applications [13]. Yttria has excellent physical properties such as low lattice mismatch ($a_{Y_2O_3}$ = 10.60 Å, $2a_{Si}$ = 10.86 Å) with Si substrate [6], large bandgap (~5.1 eV) [6], high dielectric constant (~15-18) [6], and shows Schottky contact with aluminium [12] for the resistive switching applications. In this chapter, we have comprehensively discussed the proposed analytical models and the device fabrication steps, which are utilized to fabricate memristive crossbar array structure based on yttria material system. Since, it is the first time to fabricate yttria-based memristive crossbar array with high device stability and higher device production yield by utilizing DIBS system or any other physical/chemical methods to fabricate memristive crossbar array.

3.2 Analytical Modeling of Y_2O_3-based Memristive System

The proposed analytical model provides a significant improvement (~16.66%) in device characteristics in terms of non-linear behavior of drift current at device boundaries by incorporating a modified window function and a newly incorporated state variable. The proposed model can also provide device characteristics for both sinusoidal and triangular input voltages. The memristive devices have structural variations as well as operational variations, and to cover these variations, several fitting parameters such as device conductivity and state variable on the device characteristics are used. The developed memristive device model fits well with the experimental reported data as shown elsewhere [6, 12], with an MED of ~20.1%. This work describes an in-depth analytical study of resistive switching response, conductance, actual power consumption, synaptic learning behavior, and a potentiation and depression mechanisms for a Y_2O_3-based memristive system.

3.2.1 Yakopcic Model

The current-voltage (*I-V)* relationship for the Yakopcic model [14] is described by equation (1).

$$I(t) = \begin{cases} a_1 x(t)\, sinh\big(bV(t)\big), & V(t) \geq 0 \\ a_2 x(t)\, sinh\big(bV(t)\big), & V(t) < 0 \end{cases} \quad (1)$$

In this model, several fitting parameters such as a_1, a_2 and b are used to fit the resistive switching response of memristive devices. To evaluate the current response under an externally applied voltage bias, the model requires various amplitude parameters that depend on the polarity of the applied voltage. The fitting parameter b is used to control the slope of electrical conductivity concerning the magnitude of the applied input voltage. In the case of the Yakopcic model, b is varied from 0.05 to 3 for TiO_2-based memristive system to reshape the resistive switching response. However, the value of b is dependent on the switching material. In our case, the value of b is considered to be 2.7 to achieve the maximum accuracy in comparison with the corresponding experimental data of Y_2O_3-based memristive system [6, 12]. *I-V* relationship also depends on the state variable *x(t)*, which provides a significant change in the device resistance. The range of *x(t)* is defined between 0 and 1 that directly affects the device conductivity.

The variation in *x(t)* is dependent on two different functions, such as *g(V(t))* and *f(x(t))*. The functions *g(V(t)* and *f(x(t))* are described as the programming threshold and state variable function, respectively, in the memristor model. Further, the programming threshold is governed by equation (2), which provides the different threshold voltage values on the different polarities of the applied input voltage. Equation (2) has some parameters such as positive and negative thresholds i.e., V_p and V_n, the magnitude of the exponentials i.e., A_p and A_n. The values of these aforementioned parameters represent how quickly the state of device is changed. Equations (2), (3) and (4) are described the mathematical expressions for the programming threshold voltage, *g(V(t))*, and window function, *f(x(t))*, which are given below:

$$g\big(V(t)\big) = \begin{cases} A_{\mathrm{p}}\big(e^{V(t)} - e^{V_{\mathrm{p}}}\big), & V(t) > V_{\mathrm{P}} \\ -A_{\mathrm{n}}\big(e^{-V(t)} - e^{V_{\mathrm{n}}}\big), & V(t) < -V_{\mathrm{n}} \\ 0, & -V_{\mathrm{n}} \le V(t) \le V_{\mathrm{p}} \end{cases} \quad (2)$$

$$f(x) = \begin{cases} e^{-\alpha_{\mathrm{p}}(x - x_{\mathrm{p}})} W_{\mathrm{p}}\big(x,\, x_{\mathrm{p}}\big), & x \ge x_{\mathrm{p}} \\ 1\,, & x < x_{\mathrm{p}} \end{cases} \quad (3)$$

$$f(x) = \begin{cases} e^{\alpha_{\mathrm{n}}(x + x_{\mathrm{n}} - 1)} W_{\mathrm{n}}(x,\, x_{\mathrm{n}}), & x \le 1 - x_{\mathrm{n}} \\ 1\,, & x > 1 - x_{\mathrm{n}} \end{cases} \quad (4)$$

When *V(t)* > 0, i.e., for the positive voltage polarity, the variation in the state variable is governed by equation (3), While, for *V(t)* < 0, i.e., for the negative voltage polarity, the variation is defined by equation (4). Here, W_{p} and W_{n} are the window functions and described by equations (5) and (6), respectively.

$$W_{\mathrm{p}}\big(x,\, x_{\mathrm{p}}\big) = \frac{x_{\mathrm{p}} - x}{1 - x_{\mathrm{p}}} + 1 \quad (5)$$

$$W_{\mathrm{n}}(x,\, x_{\mathrm{n}}) = \frac{x}{1 - x_{\mathrm{n}}} \quad (6)$$

Equation (7) is utilized to show the time derivative of the state variable in the memristive devices.

$$\frac{dx}{dt} = g\big(V(t)\big) \times f\big(x(t)\big) \quad (7)$$

3.2.2 Proposed Model

I-V relationship for the proposed model is governed by equation (8).

$$I(t) = \begin{cases} a_1 x(t)\, sinh\big(b_1 V(t)\big), & V(t) \ge 0 \\ a_2 x(t)\, sinh\big(b_2 V(t)\big), & V(t) < 0 \end{cases} \quad (8)$$

where, a_1 and a_2 are experimental fitting parameters, b_1 and b_2 are the conductivity slope controlling parameters under the positive and negative applied voltage, respectively. Equation (8) defines the individual conductivity control parameters for both the voltage polarities which provide better control on device hysteresis loop in the resistive switching

characteristics. On the other hand, equation (1) has single conductivity control parameter for both voltage polarities which is only applicable for bipolar memristive device. Here, it should also be noted that equation (8) is useful for both unipolar and bipolar memristive system.

In general, memristive devices show higher conductivity under positive voltage bias as compared to that under negative bias [2, 6, 12]. The higher conductivity under positive voltage bias is due to the migration of oxygen vacancies which takes place towards the interface between aluminum, used as the top electrode, and Y_2O_3 as in the case for Y_2O_3-based memristive system [6, 12]. These oxygen vacancies play important role in the resistive switching phenomena at the Al/Y_2O_3 interface in Y_2O_3-based memristive devices. Moreover, it is essential to note that the developed model is not dependent on threshold voltage while the Yakopcic model depends on the threshold voltage.

The time derivative of the state variable (*x(t)*) is governed by equation (9) where it depends on various parameters such as *G(V(t))*, α_p, α_n, W_p, W_n, *x* and *U(t)*. The physical interpretation and utilized numerical values of all modeling parameters are discussed in Table 3.1. In Yakopcic model, a specific range of numerical values for each parameter is given, and we have also used these values for analytical modeling.

$$\frac{dx}{dt} = \begin{cases} G\big(V(t)\big)e^{-\alpha_p U(x-x_p)(x-x_p)}\Big(1+\big(W_p-1\big)U\big(x-x_p\big)\Big), & V(t)>0 \\ G\big(V(t)\big)e^{\alpha_n U(x_p-x)(x-x_p)}\Big(1+(W_n-1)U\big(x_p-x\big)\Big), & V(t)<0 \end{cases} \quad (9)$$

where, *G(V(t))* is the programming voltage which depends on the several parameters such as magnitude of exponentials (A_p and A_n) and amplitude of applied input voltage *V(t)*, as described by equation (10). *U(t)* defines the unit step function.

$$G(V(t)) = \begin{cases} A_p\big(e^{V(t)}-1\big), & V(t)>0 \\ -A_n\big(e^{-V(t)}-1\big), & V(t)<0 \end{cases} \quad (10)$$

where, W_p and W_n are the window functions which bound the device state variable between 0 and 1. In the developed model, one more boundary condition has also been applied on window function, i.e., $x_p + x_n = 1$ and described by equations (11) and (12).

$$W_p = \frac{x_p - x}{x_n} + 1 \tag{11}$$

$$W_n = \frac{x}{x_p} \tag{12}$$

As described in equations (11 and 12), W_p controls the boundary of state variable when *x(t)* approaches 1 and W_n controls the boundary of state variable when *x(t)* approaches 0.

Table 3.1: Physical interpretation and numerical values of modeling parameters used in the analytical modeling.

Parameters	**Numerical Values**	**Physical Interpretation**
a_1	7×10^{-4}	Experimental fitting parameter
a_2	3.9×10^{-5}	Experimental fitting parameter
b_1	3.8	Conductivity slope controlling parameter for positive voltage polarity
b_2	1.5	Conductivity slope controlling parameter for negative voltage polarity
α_p, α_n	1.2	Control parameters for the rate of change of state variable
x_p	0.7	Constant for determining the boundedness of state variable
x_n	0.3	Constant for determining the boundedness of state variable
A_p, A_n	0.0021	Magnitude of exponentials

3.3 Generic Analytical Memristive Model for Neuromorphic Computation

In this generic analytical model, a non-linear *I-V* relationship along with a new piecewise window function has been proposed to investigate the performance of the memristive system. Recently, Kumar *et al* [15] have reported a semi-empirical model to overcome lacking in non-linear profile in the drift current at device boundaries by implementing certain mathematical modifications in several equations of the Yakopcic model. However, the reported model [15] does not capture the physics of a memristive system which is based on the interfacial switching mechanism and shows MED of ~20.1% in the neuromorphic computation characteristics, which is larger than the current generic non-linear developed model [16]. The developed non-linear analytical model is the parallel connection of rectifier and memristive device, as shown in Figure 3.1 which is able to capture the better non-linear profile in the device current along with non-ideal effects of the switching characteristics such as asymmetrical and non-zero crossing nature of switching and rectifying nature in the resistive switching response.

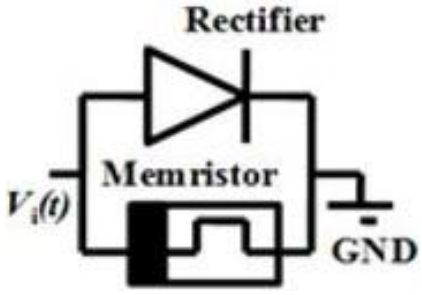

Figure 3.1: Parallel connection of rectifier and memristor.

The proposed non-linear analytical model is validated with the help of experimental results on Y_2O_3 [6] and WO_3 [2]-based memristive systems and the modelled data shows ~4.44% MED with the corresponding experimental results of Y_2O_3 [6] and ~4.50% MED in WO_3 [2]-based memristive device in the neuromorphic characteristics. The proposed newly piecewise window function fulfils all the necessary conditions as reported by Prodromakis *et al* [17]. This work describes the detailed non-linear analytical model with its resistive switching response, conductance

variations, synaptic learning behavior and synaptic plasticity functionality of Y_2O_3 and WO_3-based memristive systems.

3.3.1 Proposed Analytical Model

I-V relationship for the proposed non-linear analytical model is described by the equation (13) [16] which is closely related to the model equation reported by Yang *et al* [18].

$$I(t) = \begin{cases} b_1\, w^{a_1}\left(e^{\alpha_1 V_{\mathrm{i}}(t)} - 1\right) + \chi\left(e^{\gamma V_{\mathrm{i}}(t)} - 1\right), & V_{\mathrm{i}}(t) \geq 0 \\ b_2 w^{a_2}\left(e^{\alpha_2 V_{\mathrm{i}}(t)} - 1\right) + \chi\left(e^{\gamma V_{\mathrm{i}}(t)} - 1\right), & V_{\mathrm{i}}(t) < 0 \end{cases} \quad (13)$$

Here, the first term on the right-hand side of equation (13) defines the flux-controlled memristive behavior which is dominated by the interfacial switching mechanism as it is not included in previously reported analytical models [14-15, 18]. The newly introduced parameters a_1 and a_2 are related to the degrees of influence of the state variable on device current for positive and negative voltage biases, respectively. In this proposed model experimental fitting parameters are described in terms of b_1 and b_2 which define the slope of conductivity in *I-V* characteristics, *w* is the state variable, α_1 and α_2 are the hysteresis loop area controlling parameters. While, the second term on the right-hand side of equation (13) is related to the ideal diode behavior in *I-V* characteristics which plays a crucial role when the state variable (*w*) approaches zero i.e., the memristive device is near to the 'OFF' state and parameters χ and γ denote the net electronic barrier of the memristive device. V_{i}(t) is the applied input voltage and in the case of *I-V* characteristics, a triangular waveform and while in the case of synaptic functionality, rectangular voltage pulses are utilized as an input applied voltage. Here, it should be noted that during the I-V measurement, non-pulsing scheme is utilized to perform the switching response while, in the case of synaptic functionality analysis, pulsing scheme (i.e., rectangular) is the better way to capture the variations in the device conductance under a train of the consecutive pulses with positive and negative amplitude [6, 15-16].

The proposed non-linear analytical model can be utilized for both unipolar and bipolar memristive systems while previously reported models [2, 18] are utilized only for bipolar memristive system. Under the application of the positive bias condition, memristive devices generally show a larger hysteresis loop area due to the higher device conductivity as compared to that under the negative voltage bias [2, 6]. Because under the application of positive bias, oxygen vacancies move towards the interface between Al used as the top electrode and Y_2O_3 as switching oxide layer in the case for Y_2O_3-based memristive system [6]. The movements of these oxygen vacancies at the metal-insulator interface play a significant role in the resistive switching phenomena. Moreover, Chang *et al* [2] also have experimentally reported similar resistive switching phenomena for WO_3-based memristive system at the Pt/WO_3 interface. A new piecewise window function, *f(w)* is described by equation (14), as depicted in Figure 3.2 which ensures that the state variable (*w*) is limited between 0 and 1.

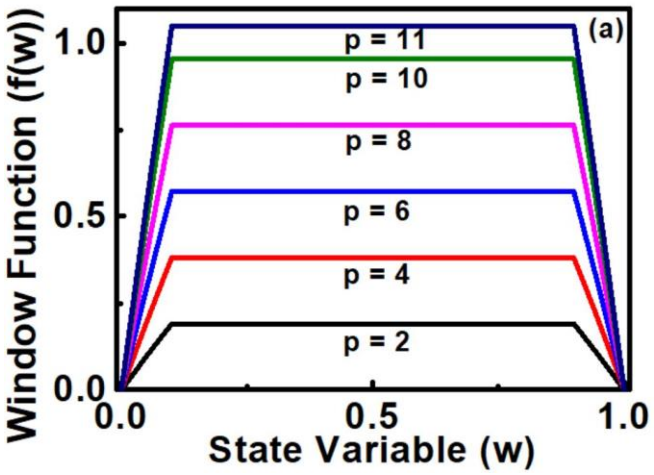

Figure 3.2: Proposed piecewise window function.

During the analytical modeling, a constant value of $p = 2$ (for Y_2O_3) and 1.5 (for WO_3) are used to capture the analytical data which are comparable to experimentally reported outcomes [2, 6]. The range of parameter '*p*' defines the limit of the *f(w)* ε {0, 1} and if the value of $p > 10$, the upper limit of the *f(w)* is beyond 1 thus violating the essential conditions as reported by Prodromakis *et al* [17].

$$f(w) = log\begin{Bmatrix}(1+w)^{\mathrm{P}}, & 0 \le w \le 0.1\\ (1.1)^{\mathrm{P}}, & 0.1 < w \le 0.9\\ (2-w)^{\mathrm{P}}, & 0.9 < w \le 1\end{Bmatrix} \quad (14)$$

The time derivative of the state variable *(w(t))* is described by the equation (15) where it depends on the nature of input applied voltage and window function.

$$\frac{dw}{dt} = A \times V_{\mathrm{i}}^{\mathrm{m}}(t) \times f(w) \quad (15)$$

where, *A* and *m* are the parameters that determine the dependence of the state variable on the applied input voltage and *m* is always an odd integer to ensure that the opposite polarity of the applied voltage leads to opposite change in the rate of change of state variable. Table 3.2 presents the physical interpretation and numerical values of all parameters used in analytical modeling.

Table 3.2: Physical interpretation and values of parameters for analytical modeling.

Parameters	**Values for Y_2O_3**	**Values for WO_3**	**Physical Significance**
b_1	1.59×10^{-3}	1.2×10^{-5}	Experimental fitting parameters
b_2	-6.2×10^{-4}	6.7×10^{-7}	Experimental fitting parameters
a_1	1.2	1.5	Degrees of influence of the state variable under positive bias
a_2	0.3	1.9	Degrees of influence of the state variable under negative bias
α_1	0.60	0.80	Hysteresis loop area controlling parameters under positive bias
α_2	-0.68	-1.5	Hysteresis loop area controlling parameters under negative bias
χ	1×10^{-11}	1×10^{-10}	Magnitude of ideal diode behavior

γ	1	1	Diode parameters like thermal voltage and ideality factor
A	5×10^{-4}	3×10^{-4}	Control the effect of the window function
m	5	5	Control the effect of input on the state variable
p	$0 < p \leq 10$; p = 2 (For result validation with the reported experimental data [6])	$0 < p \leq 10$; p = 1.5 (For result validation with the reported experimental data [2])	Bounding parameter for window function between 0 and 1

3.4 3D Physical Electro-Thermal Modeling for Nanoscale Memristor for Synaptic Application

In this section, the physical electro-thermal modeling of nanoscale Y_2O_3-based memristor devices for synaptic application has been presented. For the physical simulation, a combined software package of COMSOL Multiphysics and MATLAB has been utilized which is able to provide the realistic semiconductor device physics environment by considering several fundamental semiconductor physics equations. The performed physical modeling is based on the minimization of free energy at an applied voltage. The simulated results exhibit a stable pinched hysteresis loop in the resistive switching (RS) response in multiple switching cycles. The physical modeling is effectively shown the impact of voltage ramp rate (V_{RR}) on the device characteristics such as switching response and synaptic plasticity behavior of the device. The simulated outcomes significantly depict the impact of oxide layer thickness on the switching voltages in the nanoscale device. In this physical modeling work, for the first time in the literature, we proposed a 3D physical electro-thermal modeling of nanoscale Y_2O_3-based memristive devices with device size of 10 nm (radius of the top electrode of the device). The proposed model is based on the quantitative thermodynamic numerical model of the memristive

devices. The COMSOL [19] Multiphysics tool helps to solve the partial differential equations by utilizing Finite Element Method (FEM). The heat transfer and electrodynamic equations have solved for the defined structure by utilizing Y_2O_3 material parameters.

3.4.1 Numerical Analysis

RS corresponding to the SET process is a combination of two sub-processes such as fast shunting of electrodes and the radial growth of conductive filament (CF). The shunting process can be further classified as nucleation and longitudinal growth of CFs due to their stochastic nature [20]. Similarly, the RESET process is also composed of two sub-processes; nucleation and growth of the gap, as originated due to rupturing of the CFs. The growth of the gap in the RESET process is also of stochastic nature [20].

In the simulation process, Al/Y_2O_3/Al memristive structure is considered with a cross-sectional area of 314 nm^2. Figure 3.3(a-b) shows the simulated device geometry with corresponding layer thicknesses and description of various parameters. As seen from Figure 3.3(a-b), a SiO_2 insulating layer (with a width of 490 nm, and top and bottom thickness of 300 nm) is used as a heat shield layer surrounding the memristor structure. The effective thickness of the memristor is 110 nm including Al as bottom electrode (BE) of 65 nm, Y_2O_3 as switching layer of 5 nm, yttrium metal (Y) layer of 10 nm and Al as top electrode (TE) of 30 nm. The yttrium metal acts as an oxygen reservoir layer and helps to form the stable CFs during the device switching process and also controls the oxygen ion profile in the device. The thermodynamic numerical analysis is based on the principle of minimum free energy (FE) of memristive device and FE increases due to an applied external voltage. At the same time, the device evolves in such a way to minimize its free energy due to phase transition in oxide material by breaking chemical bonds. The free energy in a memristive device can be expressed as [21]:

$$F = \int \rho C_{\mathrm{P}}\, \delta T dx^3 + \frac{1}{2}\int \varepsilon |E|^2 dx^3 + 2\pi r h \sigma_{\mathrm{S}} + \pi r^2 h \delta \mu \qquad (16)$$

where, ρ is the mass density, C_p is the specific heat capacity at constant pressure, δT is the change in temperature, ε is the permittivity, E is the electric field, r is the radius of CF, h is the CF height in SET process (referred as: l is gap length in the case of RESET process), σ_s is the interfacial energy, and $\delta\mu$ is the difference in chemical potential between unstable conductive phase and insulating phase during SET process ($\delta\mu_1$) and between unstable conductive phase and metastable conductive phase during RESET process ($\delta\mu_2$) [21-22].

The first and second terms of equation (16) describe the thermal and electrostatic energies, respectively, while the last two terms of equation (16) can be correlated to the phase transformation energy. The electrostatic energy of the conductive components (electrodes and filament) is negligible, as compared to that of the insulating layer, which has higher capacitance. Hence, the electrostatic energy contribution in the overall value of FE is typically dominated by the insulator layer. On the other hand, the thermal contribution is dominated by the conducting filament that assists in the flow of current between the top and bottom electrodes. In this work, the following numerical algorithm steps have exploited to find the minimum FE configuration of the device and its corresponding current-voltage (*I-V)* characteristics:

(a) Construct a device;

(b) Apply the source voltage and calculate device FE for various values of filament radii;

(c) Calculate the variation in FE corresponding to the change in CF radius (∂F/∂r) and gap length (∂F/∂l) for a constant source voltage;

(d) Recalculate steps (b) and (c) for different source voltages;

(e) Capture the device voltage and current, CF radius and CF gap length, and their corresponding minimum FE for all source voltages;

(f) Finally, two sets of *I-V* are achieved in step (e) associated with the SET and RESET processes.

3.4.2 COMSOL Multiphysics Model

The 2D axisymmetric model of the memristive device in COMSOL for SET and RESET processes, is shown in Figure 3.3(a) and (b), respectively.

The 2D geometry of memristive device in COMSOL helps to reduce the volume integrals in equation (16) to area integrals.

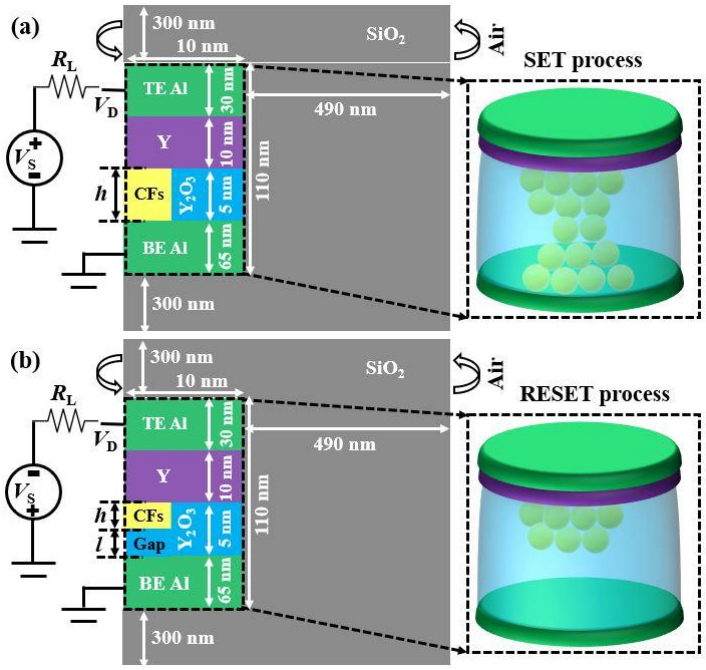

Figure 3.3: (a) 2D structure of memristive device under SET operation, and the inset shows the CF formation during the SET process, (b) 2D structure of memristive device under RESET operation, and the inset shows the CF rupturing during the RESET process.

The area integrals directly associated with SET and RESET processes in COMSOL are expressed as [21-22]:

$$F_{\text{SET}} = \iint \rho C_P \delta T dr dz + \frac{1}{2}\iint \varepsilon |E|^2 dr dz + 2\pi r h \sigma_S + \pi r^2 h \delta \mu_1 \quad (17)$$

$$F_{\text{RESET}} = \iint \rho C_P \delta T dr dz + \frac{1}{2}\iint \varepsilon |E|^2 dr dz + 2\pi r h \sigma_S + \pi r^2 l \delta \mu_2 \quad (18)$$

In case of COMSOL modeling, the values of E and T can be solved by utilizing several partial differential equations which are given below [21-22]:

[i] Electric current module formulations:

$$\nabla . J = 0 \quad (19.1)$$

$$J = \sigma E \quad (19.2)$$

$$E = -\nabla V \tag{19.3}$$

[ii] Heat transfer module formulation (in solid):

$$-\kappa \nabla^2 T = Q_S \tag{20}$$

[iii] Multiphysics module:

$$Q_S = J.E \tag{21}$$

where, J is the current density, σ is the electric conductivity, κ is the thermal conductivity and Q_s is the heat source. Typically, these equations are incorporated in the respective COMSOL modules and are extended to numerical modeling.

Here, equations (19.1 to 19.3) define the current conservation law, Ohm's law and the relation between electric field and electric potential due to Maxwell's law, respectively. Equation (20) is the Fourier heat law in which the heat source is provided by the Joule heat term given in equation (21). The boundary conditions and associated electrical configurations utilized during simulation have reported elsewhere [21-22]. Moreover, the C2C variability in the resistive switching parameters has been investigated after considering Joule heating and non-uniform electric field distribution inside the memristive device via physical electro-thermal modeling. The simulated memristive structure has also emulated the synaptic plasticity functionalities in terms of displaying of potentiation and depression processes. The simulation study also reveals the impact of voltage ramp rate (V_{RR}) on switching response which further significantly affects the synaptic functionality of the memristive device. The values of the coefficients of the differential equations such as (19.1)-to-(19.3), (20) and (21) and FE equation (17) and (18) used in this physical electro-thermal modeling are listed in Tables 3.3.

Table 3.3: Values of the coefficients of the differential equations and FE used in this physical electro-thermal modeling.

Materials	**Electrical Conductivity (σ) [S/m]**		**Thermal Conductivity (κ) [W/K.m]**	**Specific Heat Capacity [J/kg. K]**	**Relative Permittivity (ε_r)**	**Mass Density (ρ) [kg/m^3]**
SiO_2	1×10^3		1.38	703	3.9	2.20×10^3
Al	3.8×10^7		235	904	-∞	2.70×10^3
Y	1.8×10^6		17	298	-∞	4.47×10^3
Y_2O_3	10^{-11}		0.3	440	15	5.01×10^3
Y_2O_{3-x}	$\sigma_{if}\exp\left(\sigma_f \ln\left(\frac{t}{t_i}\right)\right)\exp\left(\sqrt{\frac{eV}{kT}}\right)$		$\sigma_c(T,V)TL$	528	-∞	6.01×10^3
Gap	$\sigma_{ig}exp\left(-\sigma_g ln\left(\frac{t}{t_i}\right)\right)exp\left(\sqrt{\frac{eV}{kT}}\right)$		$k_{eff}\sigma_c(T,V)TL$	440	15	5.01×10^3
Electrical Conductivity	**Parameters**	**Values**	**Circuitry**	**Parameters**	**Values**	
	σ_{if}	5 kS/m		R_L	3.1 kΩ	
	σ_{ig}	3 kS/m		$V_{(+)}$	1.5 V	
	α_f	-0.05		$V_{(-)}$	-1.5 V	
	α_g	0.05		λ	100 V/s, 10 kV/s, 1 MV/s	
	t	V/ λ	**Thermal Conductivity (Gap)**	k_{eff}	10	
	t_i		0.1ps			

3.5 Fabrication Process of MCA

For the fabrication of GZO/Y_2O_3/Al structure-based memristive crossbar array architecture a simple and feasible fabrication process is utilized as represented in Figure 3.4. During the fabrication of crossbar array, metal shadow masks are used to pattern the bottom electrode (BE), switching layer (SL), and top electrode (TE) of the crossbar array. For the (15×12) crossbar array fabrication, a 3-inch low-resistive (0.001-0.005 Ω.cm) *n*-type Silicon (100) substrate is used and cleaned in trichloroethylene (TCE), acetone, and isopropyl alcohol (IPA) for 15 minutes each under sonication to remove the unwanted residual impurities and dust particles from the substrate surface and subsequently rinsed thoroughly with de-ionized (DI) water. Further, Si substrate is purged by pure (99.999%) N_2 gas to remove the residual water droplets, as shown in step (a) of Figure 3.4.

After cleaning of Si substrate, Ar^+ plasma etching process is performed for 15 minutes by the secondary ion assist source in the DIBS system to remove the native ultrathin SiO_2 layer on top of Si substrate [23] as it may increase

the surface roughness of the deposited thin films which further affects the surface uniformity and smoothness of the films. Then, a 150-170 nm thick polycrystalline Y_2O_3 is deposited as an insulating layer [6], as shown in step (b) of Figure 3.4, on Si substrate at substrate temperature of 100 °C with pure Ar of 5 sccm environment used in the assist ion source of the DIBS system. The surface morphology and smoothness of as-deposited insulating Y_2O_3 is remarkable, as reported elsewhere [24].

As it is observed that the similar lattice constants of Si ($2\alpha_{Si}$ = 10.86 Å) and Y_2O_3 (10.60 Å) plays a very important role to provide better film uniformity and surface morphology of the Y_2O_3 insulating layer [25] on top of which BE is deposited. Low resistive (5.3×10^{-4} Ω.cm) [26] Gallium-doped Zinc Oxide (GZO) (3% Ga doping in ZnO) of 100-110 nm is deposited on top of the insulating Y_2O_3 layer at 100 °C substrate temperature with pure Ar flow of 5 sccm in the assist ion source of DIBS system. GZO acts as the BE and patterned via shadow mask with the line width of 800 μm, as depicted in steps (c and d) of Figure 3.4. Subsequently, 45-50 nm of amorphous Y_2O_3 layer is deposited as a resistive SL, as shown in steps (e and f) of Figure 3.4.

Here, it should be noted that, during the resistive SL deposition, a substrate temperature of 300 °C and the ratio of Ar and O_2 gas flow of 2:3 in the assist ion source of the DIBS system [6] which are completely different deposition conditions as opted during insulating layer deposition. Finally, a 70-80 nm Al TE is deposited via direct current (DC) magnetron sputtering system, as presented in steps (g and h) of Figure 3.4. The step (i) of Figure 3.4 shows a digital camera photograph of finally fabricated memristive crossbar array architecture of (15×12). It should be noted that during the fabrication of crossbar, the line width of the TE shadow mask is varied from 600 to 300 μm to investigate the impact of area on the device current.

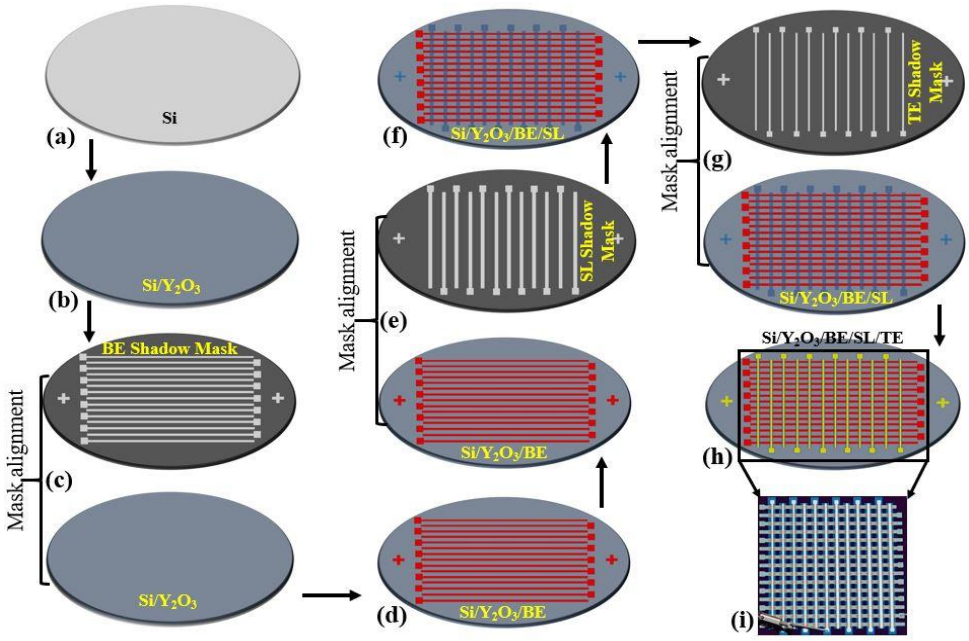

Figure 3.4: (a-h) Detailed fabrication process for the (15×12) memristive crossbar array via DIBS system: (a) Cleaned Si substrate, (b) Deposition of insulating Y_2O_3 layer, (c) Shadow mask alignment for BE deposition, (d) Deposited BE via DIBS system, (e) Shadow mask alignment for SL deposition, (f) Deposited SL via DIBS system, (g) Shadow mask alignment for TE deposition, (h) Deposited TE via DC magnetron sputtering, (i) A Photograph of the finally fabricated crossbar array architecture (top view).

3.6 Conclusion

In this chapter, we have discussed the developed analytical models, 3D physical electro-thermal modeling of nanoscale memristor and designed fabrication process flow for our fabricated memristive crossbar array which can prove our hypothesis of resistive switching in yttria-based memristive crossbar array. Also, in this chapter, we have comprehensively discussed the analytical models' parameters with its physical interpretation and numerical values used during the analytical modeling. This chapter comprehensively outlined the physical model and utilized FE equation with semiconductor modules equations in the COMSOL Multiphysics to simulate the memristor device at nanoscale level. Moreover, the chapter also discussed about the adopted fabrication process and contained the information about the materials used for the different layers of the crossbar array architecture such as BE, SL and TE, these deposition conditions,

utilized deposition systems and also discussed the device size in the crossbar array.

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Chapter 4

Analytical and Physical Models Analysis, Material and Electrical Characterizations of Fabricated MCA

4.1 Introduction

The comprehensive advantages of analytical modeling are that it has the ability to provide practical feedback to designers and practitioners to design memristive systems for the diverse real-time applications. The analytical models allow the designer to determine the correctness and efficacy of a memristive system. By utilizing the analytical modeling, the designer is able to better understand the behavior and interactions of the memristive system and, therefore, remains better equipped to counteract the complexity of the overall system.

Previously, several experimental reports have been published which are related to the different materials-based memristive systems [1-3]. These reported outcomes efficiently show synaptic learning behavior which is analogous to the biological synapses [4-6]. Among these transition metal oxides (TMOs) materials, Y_2O_3 is one of the most promising TMO material candidates for the memristive system for the neuromorphic applications [7-8] which has been carried out by utilizing a dual ion beam sputtering (DIBS) system. DIBS system offers plenty of advantages as compared to other conventional sputtering techniques, such as high-quality thin films with better compositional stoichiometry, small surface roughness, and good adhesion to the substrate [7]. However, no literature to date has reported on analytical modeling of a Y_2O_3-based memristive system for neuromorphic applications. Hence, it is essential to design and develop a generic model for the memristive system which can predict the experimental characteristics of a device for synaptic applications.

The proposed analytical model provides a significant improvement (~16.66%) in the device characteristics in terms of non-linear behavior of drift current at the device boundaries by incorporating a window function

and a newly introduced state variable. The developed model can also provide device characteristics for both sinusoidal and triangular input voltages. Since memristive devices have a significant variation in structure as well as in operation, the present model uses several fitting parameters to incorporate the effects of different parameters, such as device conductivity and state variable on the device characteristics. This work describes an in-depth analytical study of conductance, actual power consumption, and a potentiation and depression mechanism for a Y_2O_3-based memristive system.

Further, a 3D physical electro-thermal modeling is also performed to investigate the performance of real memristor device at nanoscopic level by considering several physical parameters such as internal Joule heating and non-uniform distribution of the electrical field. In this physical modeling, a thin layer (5 nm) of switching oxide layer is used as a resistive switching layer which allows filamentary based switching mechanism under the application of low input voltage and also emulated the various memristive properties under the ideal conditions. Therefore, the extensive benefit of the physical electro-thermal modeling includes the ability to capture the realistic behavior of the biological synapse which helps the researchers to analyze the various functionality of the artificial synapse.

Next, the chapter comprehensively describes the optical, materials, and electrical properties of the fabricated memristive crossbar arrays size of (15×12) and (30×25). These properties play a critical role in deciding the thin film properties such as resistivity, crystallinity, and surface roughness which will affect the resistive switching behavior of the fabricated memristive devices. After the device fabrication, we have performed current-voltage (*I-V*) measurement of the fabricated devices in pulse-mode using Keithley 4200A semiconductor parametric analyzer at room temperature in order to know the optimized values of these parameters. I-V measurements of samples have been performed under triangular waveform voltage excitation of ±3 V, compliance current of 20 μA) for the pinched hysteresis loop analysis.

4.2 Analytical Modeling of Y_2O_3-based Memristive System

An analytical model for Y_2O_3-based memristive systems is discussed, since a traditional model such as the Yakopcic model significantly deviates to capture the neuromorphic behavior for yttria-based memristive systems. On the one hand, the developed analytical model shows high correlation with the reported experimental data and removes the shortcomings of the Yakopcic model such as lack of non-linear behavior in the drift current at the device boundaries by incorporating a new window function and state variables. On the other hand, the Yakopcic model is based on the device threshold voltage parameters, while the developed model is generic and remains independent on threshold voltage parameters. As a result, the developed analytical model can be used in designing real-world applications based on the neuromorphic properties of yttria-based or any generic memristive systems.

4.2.1 Resistive Switching Characteristic

To investigate the resistive switching characteristics of the Y_2O_3-based memristive system, similar electrical conditions are utilized, which have been experimentally reported elsewhere [7-8]. For the switching characteristics and their memristive behavior, a triangular waveform is utilized as an input voltage with peak-to-peak voltages amplitude of ±5 V and a compliance current of 10 mA. Figure 4.1 depicts the resistive switching characteristics with pinched hysteresis loop property of the fabricated memristive system along with their substantial correlation with the analytical modeling data. The existence of the pinched hysteresis loop in the resistive switching is a footprint of the memristive system [9].

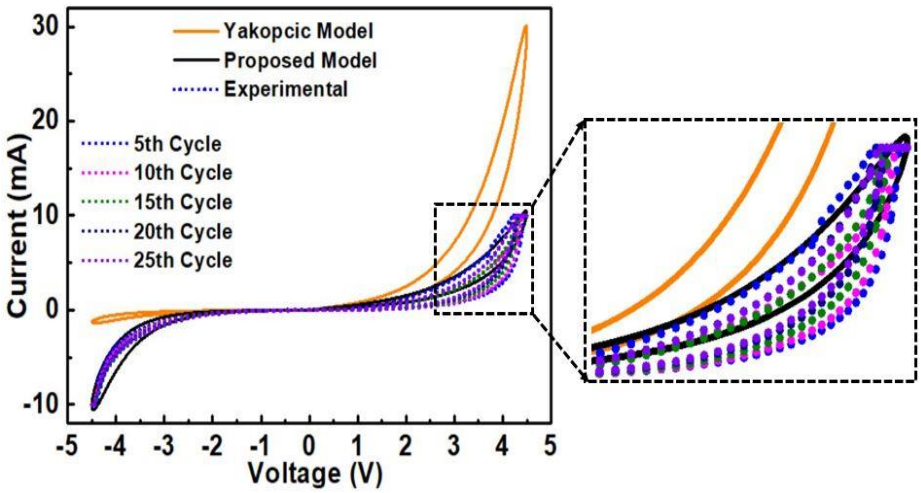

Figure 4.1: Nonlinear pinched hysteresis switching characteristics of the memristive device. Inset shows the enlarge view of the switching response.

Moreover, according to Chua [10], a device which shows a pinched hysteresis loop in its resistive switching response is the sufficient condition for resistive random-access memory to be considered under a broad category of memristive devices in which the pinched hysteresis loop can collapse into a single-valued function [10].

4.2.2 Variations in Device Conductance and Utilized Power

Figure 4.2(a) depicts the change in device conductance under the application of applied negative voltage bias from 0 to -5 V. In general, conductance is a positive electrical parameter; however, in this case, the negative direction of conductance under negative voltage bias shows the flow of device current in the opposite direction and the experimentally results show better agreement with the analytically modeled data. Figure 4.2(b) shows the actual power utilization when the memristive device under operation/test. The device utilized power is directly influenced by the applied voltage and corresponding generated device current. If one of the parameters such as applied input voltage or generated device current are varied, the corresponding utilized power by the device is also varied. Moreover, the device utilized power is associated with the device switching parameters such as switching voltages (V_{SET} and V_{RESET}) and device switching speed. The negative polarity of power shows that the applied

voltage direction is opposite (0 to -5 V). In this case, too, the presented analytical modeling fits perfectly with the experimentally obtained results [7-8].

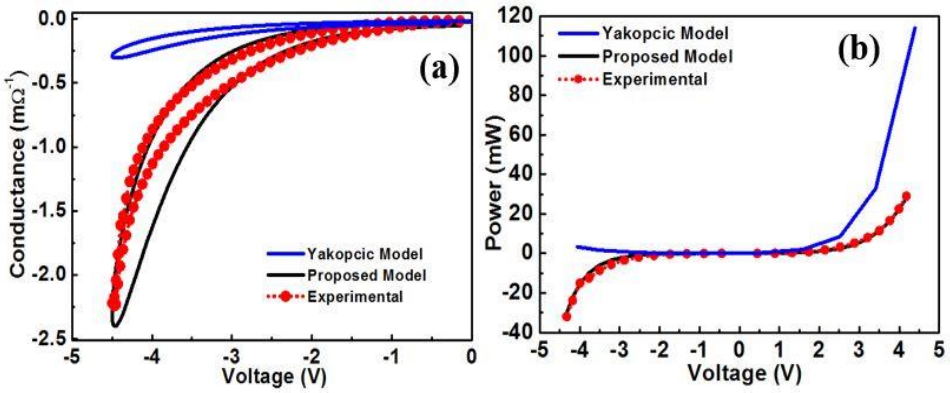

Figure 4.2: (a) Variation in device conductance under negative applied voltage, and (b) Actual power consumption by the device when in operation.

4.2.3 Variations in Synaptic Weight: "Learning Behavior"

For the analysis of the 'synaptic learning behavior' of the memristive device, a chain of 40 consecutive positive rectangular voltage pulses is imposed on the device with an amplitude of +4 V and a pulse width of 100 ms as reported elsewhere [7]. Under the consecutive pulses, the synaptic weight (or normalized device conductance) is continuously increased with the number of pulses. The learning behavior of the memristive system is shown in Figure 4.3.

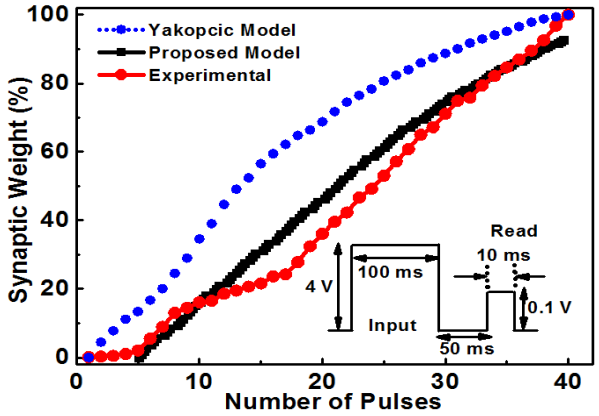

Figure 4.3: "Learning behavior": variation in synaptic weight under positive voltage pulses. Inset shows the applied rectangular voltage pulse as an input.

4.2.4 Synaptic Plasticity: Potentiation and Depression Mechanisms

A sufficient increment or decrement in device conductance is similar to the potentiation (P) or depression (D) mechanisms, respectively, of the synapses in a neuromorphic system [7]. The potentiation and depression processes can be achieved by applying rectangular voltage pulses. For the potentiation and depression processes, a chain of 50 positive pulses with an amplitude of +4 V and pulse width of 100 ms and a chain of 40 negative pulses with an amplitude of -4 V and pulse width of 100 ms are used for the excitation of the synapse. It should be noted that the overall electrical flux passing through the memristive device is zero after completion of the potentiation and depression processes, and the synaptic weight of the memristive device returns to its initial state. Figure 4.4 shows the response of a train of 50 positive voltage pulses, followed by 40 negative pulses. By applying a train of positive voltage pulses, the synaptic weight of the memristive device is continuously strengthened, known as potentiation, while in the case of negative voltage pulses the synaptic weight of the device is gradually weakened, which leads to depression process.

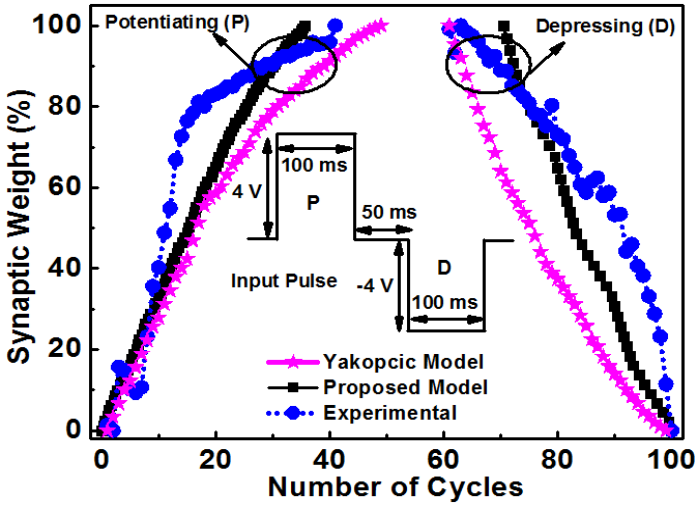

Figure 4.4: Variation in synaptic weight under the influence of consecutive potentiation (positive) and depression (negative) pulses. Inset shows the applied positive and negative voltage pulses.

In order to evaluate the maximum error deviation (MED) of the modeled fitting data with corresponding experimental results, a similar mathematical formulation approach is used which has been reported by Bakar *et al* [11]

and Hemmati *et al* [12]. By implementing the mathematical approach, the Yakopcic model results show the ~36.8% MED at a specific point while the developed analytical model results represent the ~20.1% MED with respect to the corresponding experimental data [7-8].

4.3 Generic Analytical Memristive Model for Neuromorphic Computation

The development of a generic model for the memristive systems which simulates the biologically inspired nervous system of living beings, is one of the most attracting aspects. More specifically, the develop generic model has capability to resolve the problems in the field of artificial neural network with better efficacy. Here, a generic, non-linear analytical memristive model, which is based on interfacial switching mechanism, has been discussed. The proposed model has the capability to simulate the high-density neural network of biological synapses that regulates the communication efficacy among neurons and can implement the learning capability of the neurons. Further, the developed non-linear analytical model is the parallel connection of the rectifier and memristive device which shows better non-linear profile along with non-ideal effects and rectifying nature in its pinched hysteresis loop in the resistive switching characteristics. Moreover, developed analytical model shows the significant low value of MED ~4.44% for Y_2O_3-based and ~4.5% for WO_3-based memristive systems, respectively, in its neuromorphic characteristics with respect to the corresponding experimental results [1, 7-8]. Therefore, the proposed analytical memristive model can be utilized to develop the memristive system for real-world applications based on neuromorphic behaviors of any transition metal oxide-based memristive systems.

4.3.1 Resistive Switching Characteristic

To investigate the various experimentally-obtained characteristics of Y_2O_3-based memristive system, similar electrical conditions are used which have been reported elsewhere [7]. For analyzing the resistive switching characteristics, a triangular voltage waveform is applied on the device with peak-to-peak voltage amplitude of ±5 V with a compliance current of 10

mA. Figure 4.5 depicts the pinched hysteresis loop in the resistive switching characteristics of developed memristive devices along with their modeled data. In order to calculate the MED of the modeled data with the corresponding experimental results, similar mathematical pathway is used which has been reported by Bakar *et al* [11], Hemmati *et al* [12], and Kumar *et al* [13]. By utilizing as reported [11-13] mathematical formulation, the modeled data shows ~18.5% MED at +4 V in resistive switching response as shown in Figure 4.5 with respect to the experimental data of the fabricated device. The presence of a pinched hysteresis loop in resistive switching characteristics of the device is a fingerprint of memristive system [9]. Moreover, Chua [10] has claimed that the pinched hysteresis loop can be collapsed into a single-valued function.

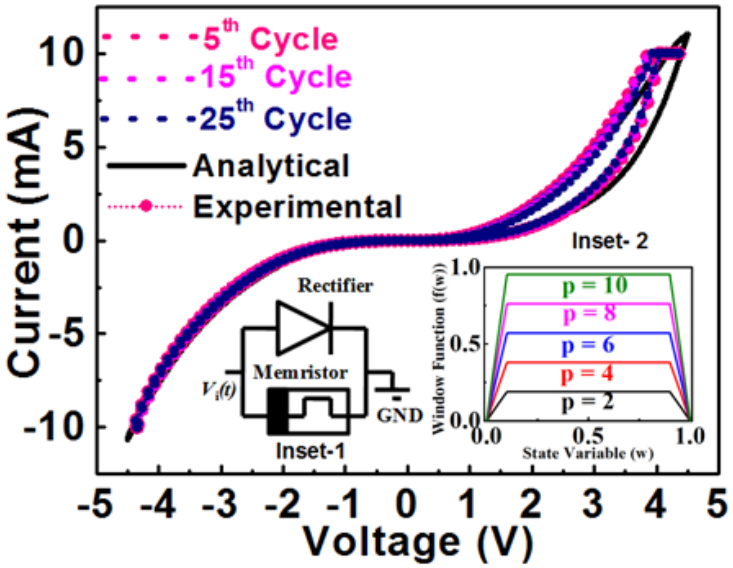

Figure 4.5: Resistive switching characteristic of a memristive device (sweep rate: 1.042 V s^{-1}). Inset-1 and inset-2 show parallel connection of rectifier and memristive device and piecewise window function, respectively.

4.3.2 Variations in Device Conductance and Power Consumption

Figure 4.6(a) shows the actual power utilization by the device under operation/test. The power utilized by the device under test is dependent on both applied voltage and current flow through the device. The significant variations in the current and voltage can lead to a change in the utilized

power by the device. The negative direction of power represents the current direction from ground terminal to excitation terminal. The device utilizes maximum power when the state variable is close to unity, i.e., the device is in the 'ON' state. The modeled data shows ~2% MED at +4 V as shown in Figure 4.6(a) with respect to the associated experimental result.

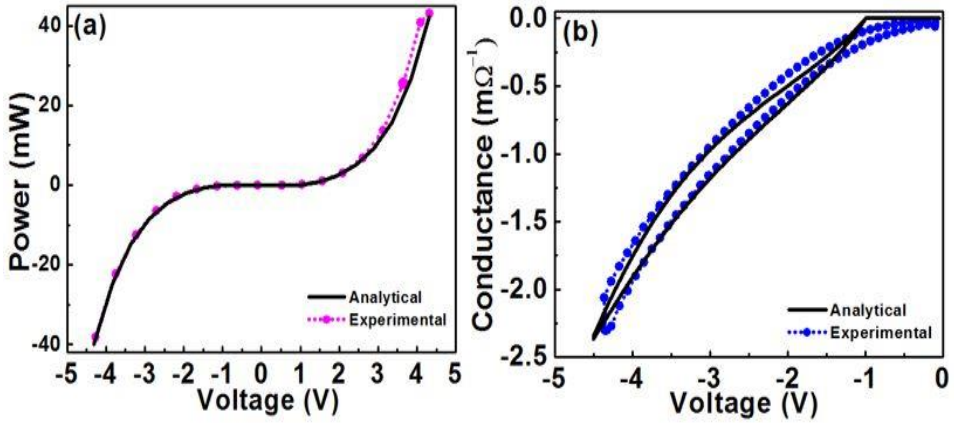

Figure 4.6: (a) Actual power utilization by the device under test, (b) Change in device conductance under negative voltage polarity (sweep rate: 1.042 V s^{-1}). Inset shows the variation in device conductance under positive voltage polarity.

Figure 4.6(b) depicts the variations in the device conductance under the application of applied negative voltage bias from 0 to -5 V. However, conductance is a positive quantity, and in this case, the negative direction of conductance under negative voltage polarity shows the flow of current in the opposite direction and the obtained modeled data shows ~14.4% MED at -2 V as shown in Figure 4.6(b) with the respective experimental data.

4.3.3 Conductance Variations and Synaptic Learning Mechanism

Figure 4.7(a) shows the change in conductance of the fabricated memristive systems along with their modeled data. Here, it is noted that whenever a chain of 100 successive positive rectangular voltage pulses with different amplitudes such as +2 and +2.5 V and pulse widths of 50 and 100 ms are imposed on the memristive system, significant variations in the device conductance is observed due to a larger change in the device current [7-8].

Wang *et al* [14] have also reported similar characteristics in amorphous InGaZnO-based memristive devices. Therefore, if the variation in the device conductance is observed which is also similar to the synaptic weight update, then the above discussed mechanism shows closed analogy with the non-linear transmission characteristics of a real biological synapse [9]. The modeled data of device conductance variation under different voltage amplitude shows <1% MED with respect to the experimental data.

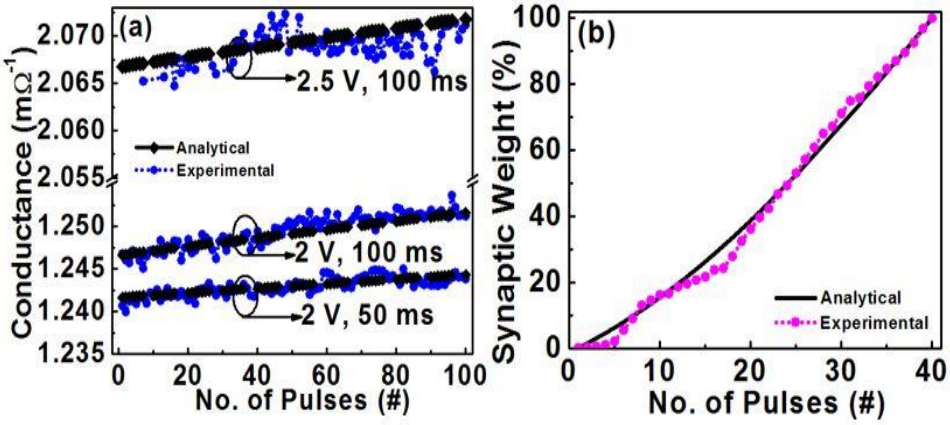

Figure 4.7: (a) Variation in conductance under different voltage amplitude with the pulse number, and (b) Synaptic learning characteristics of memristive system.

Further, to analyze the 'synaptic learning' behavior of the memristive systems, a train of 40 successive positive rectangular voltage pulses with an amplitude of +4 V and pulse width of 100 ms is applied on the memristive device. Under the excitation of such positive successive pulses, the synaptic weight is continuously strengthened along with the number of pulses as the device is continuously in ON state. In this case, the modeled learning behavior shows ~11.2% MED with corresponding experimental data at pulse number 18, as shown in Figure 4.7(b).

4.3.4 Neuromorphic Functionality: Potentiation and Depression Processes

Figure 4.8(a) shows the synaptic behavior of the memristive system in terms of potentiation and depression processes. Under the application of a train of 50 successive positive rectangular voltage pulses with an amplitude of +4 V and a pulse width of 100 ms, the synaptic weight of memristive

system is continuously strengthened and this mechanism is termed as the potentiation. While, in the case of depression mechanism, a train of 40 successive negative rectangular voltage pulses with an amplitude of -4 V and a pulse width of 100 ms is imposed on the memristive system where the synaptic weight of the memristive system is gradually debilitated.

After the potentiation and depression mechanisms, the overall electric flux passing through the memristive systems is zero and synaptic weight of the memristive system returns back to its initial level [1]. This process is analogous to the learning behavior of the human brain whereas the synaptic weight of the neuromorphic system changes according to the number of electrical stimuli received during the learning process. The proposed non-linear analytical model shows ~4.44% MED at pulse number 85 with respect to the corresponding experimental outcome.

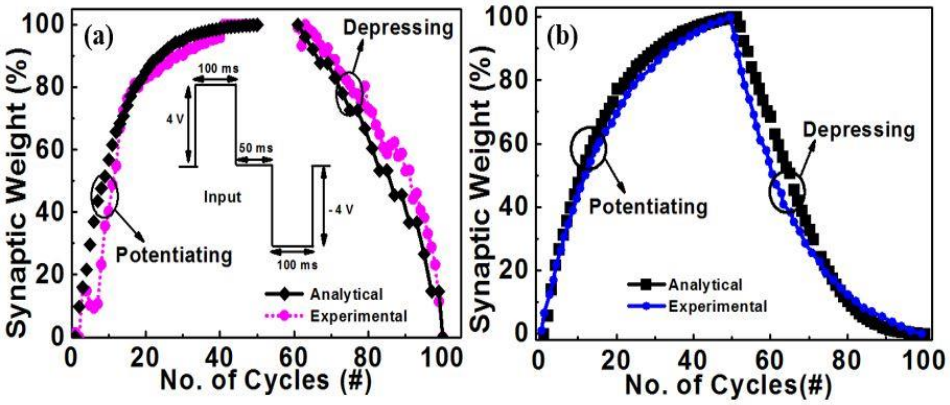

Figure 4.8: (a) Change in synaptic weight under the excitation of successive positive (potentiation) and negative (depression) cycles in Y_2O_3-based memristive device. Inset shows the applied rectangular voltage as an input pulse, and (b) Synaptic plasticity behavior of the WO_3-based memristive device under potentiating and depression mechanisms.

Figure 4.8(b) represents the potentiation (P) and depression (D) process of the device while studying the synaptic plasticity behavior. During the potentiation process, a train of 50 successive positive rectangular voltage pulses with an amplitude of +1.2 V followed by 50 rectangular negative pulses with an amplitude of -1.2 V and pulse width of 5 μs is applied on the device. Under positive pulses, the synaptic weight is strengthened with the

number of stimulating positive pulses and debilitated under the negative voltage pulses.

4.4 3D Physical Electro-Thermal Modeling of Nanoscale Memristor for Synaptic Application

In this section, we have discussed the physical electro-thermal modeling of nanoscale Y_2O_3-based memristor. The presented simulation study is carried out by the combined software package of COMSOL Multiphysics and MATLAB. The presented physical modeling is based on the minimization of free energy of the utilized materials at an applied voltage. The simulated results exhibit a stable pinched hysteresis loop in the resistive switching (RS) response in multiple switching cycles. The RS responses show low values of coefficient of variability (C_V) i.e., 17.36% and 17.09% in SET and RESET voltages, respectively, during C2C variation. The impact of voltage ramp rate (V_{RR}) on the device characteristics such as switching response and synaptic plasticity behavior of the device, is successfully investigated. The simulated outcomes significantly depict the impact of oxide layer thickness on the switching voltages in the nanoscale device.

4.4.1 Resistive switching response

Figure 4.9(a) shows the simulated RS response of the Y_2O_3-based memristive device under an applied voltage of ±1.5 V with a pulse width of ~10 ms imposed to the top electrode via a load resistance. The RS response is divided into four parts: positive forming voltage ($+V_F$), positive SET voltage (V_{SET}), negative rupture voltage ($-V_R$), and negative RESET voltage (V_{RESET}).

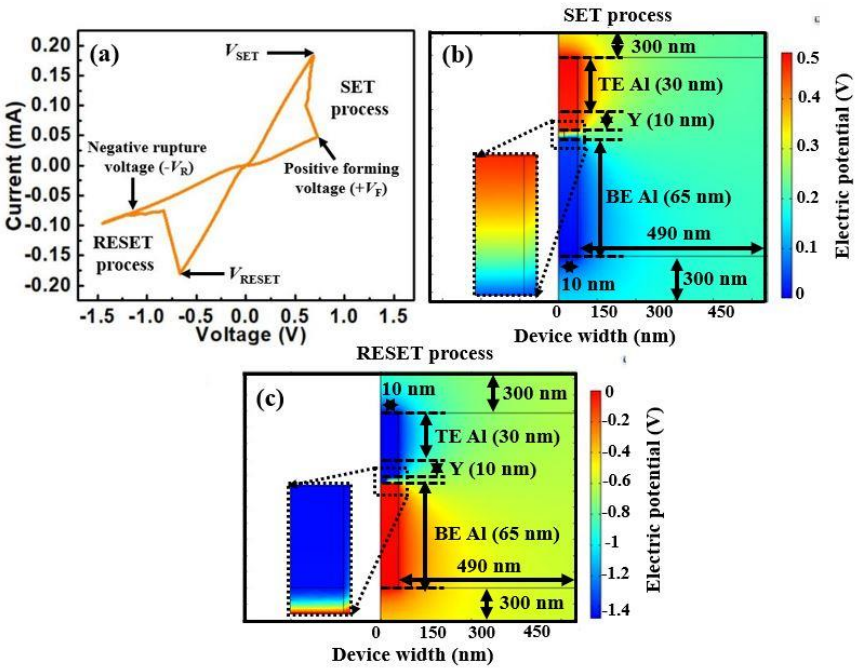

Figure 4.9: (a) Resistive switching response of Y_2O_3-based memristive device, electric potential distribution under (b) SET and (c) RESET processes. The "red" spot at the top electrode side in (b) shows the formation of CFs, while the "blue" spot at the top electrode side in (c) shows the rupturing of CFs.

During the forming process, all the CFs are formed inside the RS Y_2O_3 layer and memristive device is switched into the SET position for voltage amplitude $\leq V_F$, as shown in Figure 4.9(b). For the Y_2O_3-based memristive device, the simulated V_F and V_{SET} are +0.7261 and +0.6585 V, respectively. On the other hand, during the rupturing process, all the formed CFs are ruptured and memristive device is switched into RESET position for voltage amplitude $\leq -V_R$, as shown in Figure 4.9(c). The simulated values of $-V_R$ and V_{RESET} are -1.1119 and -0.6659 V, respectively.

4.4.2 Impact of cycle-to-cycle variation in resistive switching

C2C variations are associated with the stochastic nature of the resistive switching material of the memristor [15-16]. Specifically, C2C variations are induced due to the formation of some undefined current path during every switching cycle [15]. Therefore, every switching cycle is repeated under nominally identical conditions with slightly different microscopic structures.

Figure 4.10(a) depicts the RS response in 40 cycles under the continuous device operation in which the absolute valued *I-V* response for multiple cycles is represented in the inset. Figure 4.10(b) shows the C2C variations in V_{SET} and V_{RESET}. To consider these variations, the coefficient of variability (C_V) is calculated and defined as the ratio of standard deviation (σ) to mean value (μ) [16] of the corresponding switching voltage parameters. For V_{SET} and V_{RESET}, the values of C_V are 17.36% and 17.09%, respectively. These moderate variations in the C2C C_V of the switching parameters confirm that the thermal stability of the Y_2O_3-based memristor is significantly beneficial as compared the other oxide materials [15, 17]. However, the fluctuations in the C2C operation of the memristive device is random in nature and more dominated due to the stochastic nature of ionic movement and uncontrolled formation of the conductive filament during the resistive switching process [16]. Also, it is dependent on the several other parameters such as induce electric field, internal Joule heating, and active area of the memory device.

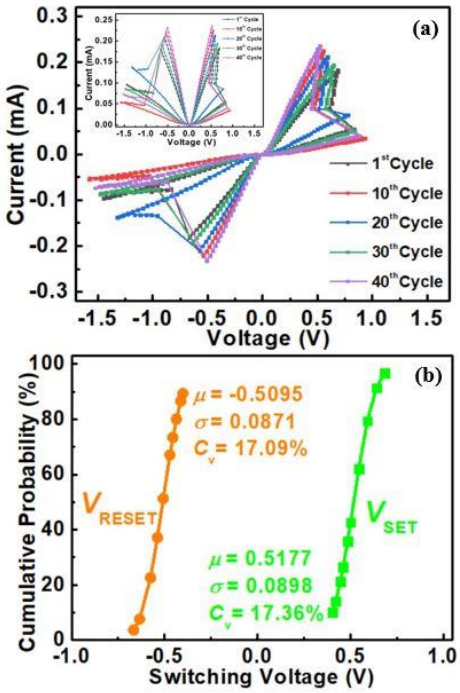

Figure 4.10: (a) Resistive switching response of Y_2O_3-based memristive device in continuous operation where the inset shows the I-V response in multiple cycles for absolute values of current along y-axis., (b) C2C variations in V_{SET} and V_{RESET}.

4.4.3 Impact of voltage ramp rate variation in resistive switching

Figure 4.11(a) shows the impact of the variation of voltage ramp rate (V_{RR}) on device switching characteristics and the inset in Figure 4.11(a) shows the *I-V* response for absolute values of current at y-axis. As seen from Figure 4.11(a-b), when one shifts from slower (100 V/s) to faster V_{RR} (1 MV/s), the values of V_{SET} and V_{RESET} are increased. It is observed that under fast V_{RR} the device switching speed is increased and no sufficient time windows are available for the mobile vacancies to settle down [18]. Similar behavior is also reported by Fantini *et al* [18] in HfO_2-based memristive device under fast electrical measurement. Hence, from the point of view of physical modeling, one can conclude that the RS characteristics are directly dependent on V_{RR} in cyclic operation.

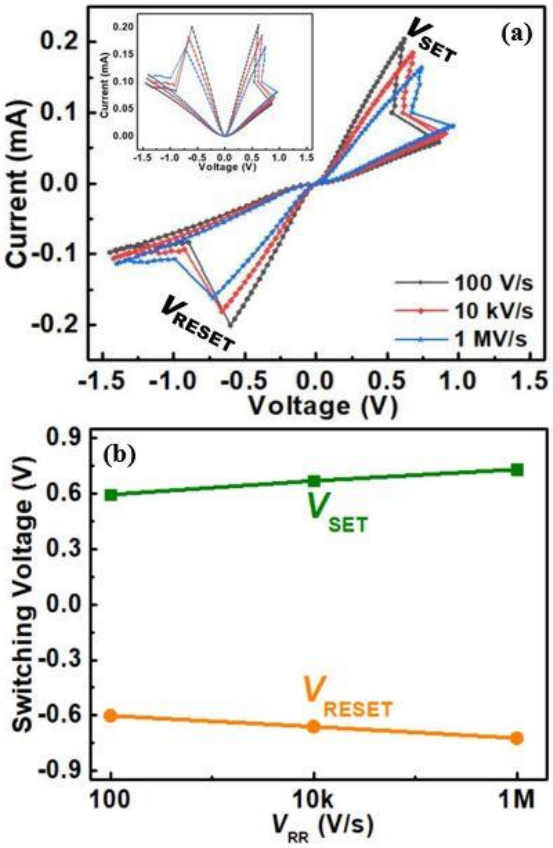

Figure 4.11: (a) Impact of V_{RR} variation on RS characteristics where the inset shows the I-V response for absolute values of current along y-axis, (b) Incremental trend in V_{SET} and V_{RESET} under different V_{RR}.

4.4.4 Impact of voltage ramp rate variation in synaptic plasticity

To emulate the synaptic plasticity behavior of the memristive device in terms of potentiation and depression, a train of positive and negative voltage pulses with amplitude of ±1.5 V and V_{RR} of 100 V/s are applied on the memristive device. As seen from Figure 4.12(a), under the application of positive voltage pulses, the synaptic weight or the normalized conductance of the memristive device is continuously strengthened. On the other hand, in case of negative electrical stimulus, the synaptic weight is gradually weakened, as shown in Figure 4.12(b). The continuous strengthening and weakening of the device conductance are analogous to the synaptic plasticity functionality of the human brain [1, 7, 19, 20-22]. Here, a train of 100 (50 positive and 50 negative) identical pulses with an amplitude of ±1.5 V and pulse width of 15 ms to compute the synaptic characteristics. As reported in the literature, when the identical pulses have been imposed, the metal/insulator interfaces are observed to exhibit gradual potentiation and abrupt depression process [23-26], as depicted in Figure 4.12(c). The abrupt change in the depression process is associated with the difference in metal and oxide free energy [27]. Moreover, the effect of V_{RR} over the synaptic weight is also investigated, as depicted in Figure 4.12(c), which clearly shows that under faster pulse operation (i.e., higher V_{RR}), the device conductance is significantly lower. The decrement in the device conductance at higher switching speed can be associated with the partial switching induced inside the device and follows almost linear behavior when the value of V_{RR} is changed from 100 V/s to 1 MV/s, as depicted in Figure 4.12(d). Similar linear decay in the synaptic weight is also reported by Costa *et al* [28] in porous silicon based memristor.

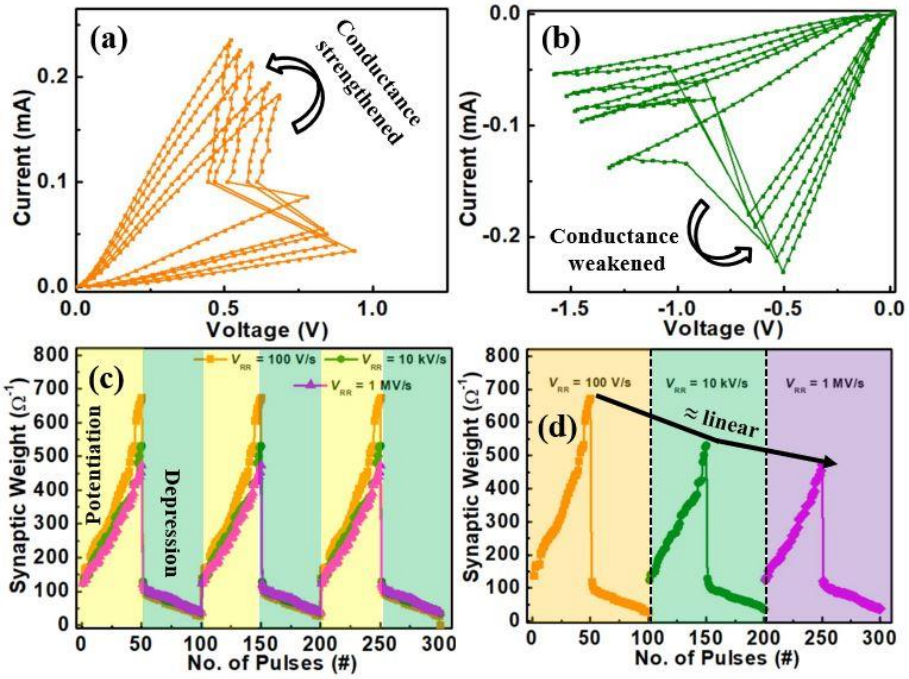

Figure 4.12: I-V characteristics of memristive device under consecutive (a) Potentiating voltage pulses of +1.5 V and (b) Depressing voltage pulses of -1.5 V at V_{RR} of 100 V/s, (c) Effect of V_{RR} variation on device synaptic weight, (d) Approximate linear decrement trend in synaptic weight under varied V_{RR}.

4.4.5 Impact of oxide thickness on switching voltages

In this section, the impact of thickness of the Y_2O_3 switching oxide layer on the switching voltages (i.e., V_{SET} and V_{RESET}) of the memristive device is studied. As shown in Figure 4.13, when switching oxide layer thickness is increased from 2 to 20 nm, the corresponding switching voltages are also increased due to the higher amount of applied voltage is required to switch the memristive device to the SET and RESET states. Similar behavior has also experimentally reported by Zhang *et al* [29] in $ZnMnO_2O_4$-based memristive devices. It should be noted that a higher amount of applied voltage is required to create the large electric field which further helps to accelerate the mobile ions/vacancies to form CFs inside the thick switching oxide layer.

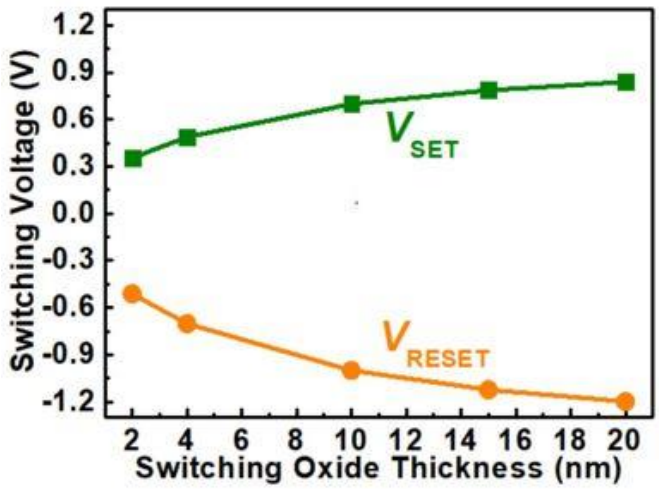

Figure 4.13: Impact of variations in switching oxide layer thickness on device switching voltage parameters.

Therefore, the adopted physical modeling approach offers benefits to the researchers to develop the Y_2O_3-based memristor which can be operated at low switching voltage with very thin oxide layer and make it suitable for low-power memory applications. The outcomes also reveal that the nanoscale Y_2O_3 memristor perfectly emulates the synaptic plasticity which leads to the possibility to build artificial synapses similar to the human brain system.

4.5 MCA: Optical, Material and Electrical Characterizations

Several characterizations have been performed such as the semiconductor parameter analyzer (SCS-4200A) system is utilized to study the resistive switching performance of the fabricated crossbar arrays size of (15×12) and (30×25); optical microscopy is used to see the realistic view of the fabricated crossbar arrays; field emission-scanning electron microscopy (FE-SEM, Carl Zeiss) is performed to investigate the surface morphological analysis of the resistive switching material; high-resolution transmission electron microscopy (HR-TEM, Hitachi HD2300A) is carried out for various interfacial study; and a conductive-atomic force microscopy (C-AFM, Shimadzu SPM-9500J3) is done to analyze the current distribution during the operational condition of the fabricated devices.

4.5.1 Optical Microscopy Characterization

Figure 4.14(a-c) shows the digital camera photograph and optical microscopy images of the fabricated memristive crossbar array architecture. As seen from Figure 4.14(b-c), the fabricated devices in the crossbar array have perfect aligned crosspoint structure which is highly desirable in case of the crossbar array fabrication to avoid any electrical shorting issues in the memristive devices.

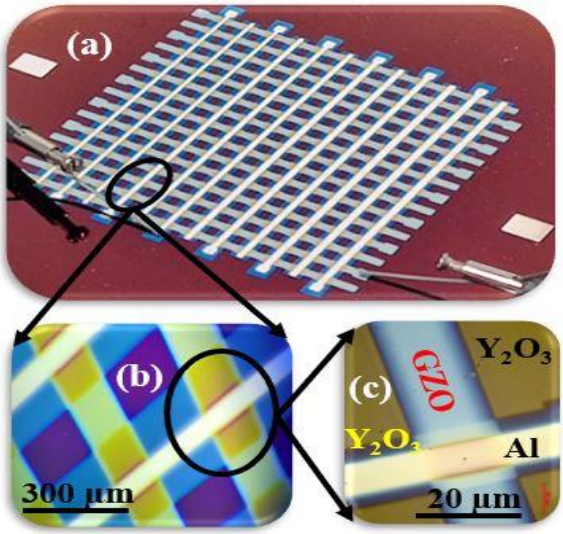

Figure 4.14: (a-c) Optical microscopy images of fabricated memristive crossbar array structure at different scale.

4.5.2 Material Characterizations

To investigate the surface morphology, grain size and grain distribution of the resistive switching layer of amorphous Y_2O_3, FE-SEM is utilized. Figure 4.15(a and b) shows the SEM outcomes at varied scales and exhibits a continuous Y_2O_3 SL layer with compact grains, which is also described elsewhere [30]. Moreover, we have performed cross-sectional HR-TEM to investigate the various interfaces of the fabricated devices in the crossbar array as shown in Figure 4.15(c). The cross-sectional HR-TEM analysis reveals that in the fabricated memristive structure all interfaces such as insulating Y_2O_3/Si, BE GZO/insulating Y_2O_3, Y_2O_3 SL/GZO are distinct and shows smooth and uniform film deposition. The HR-TEM analysis also reveals that there is no formation of interfacial oxide between Si and Y_2O_3

insulating layer which is beneficial for uniform SL deposition [31]. Figure 4.15(d-h) depicts the current distribution carried out by C-AFM study without any bias (0 V), at ±3 V and at ±5 V on the surface of Y_2O_3 SL. The current distribution in the "bright" images (Figure 4.15(e and g) at +3 and +5 V, respectively) is higher which denotes the high conduction state or "low resistance state (LRS)" of the memristive device. On the other hand, the current distribution in the "dark" images (Figure 4.15(d, f and h) at 0, -3, and -5 V) is lower which is corresponding to the low conduction state or "high resistance state (HRS)" of the memristive device. Here, it should be noted that the insignificant amount of surface current even at a large bias (±5 V) and area (1×1 μm^2) confirms that the conductive-filamentary-based switching might not be a dominant case for these devices. In fact, interface-type of resistive switching (see Figure 4.16) seems to be dominant at the interface between the metal electrode and the switching oxide as experimentally observed by Das *et al* [8] for Y_2O_3-based single memristive devices.

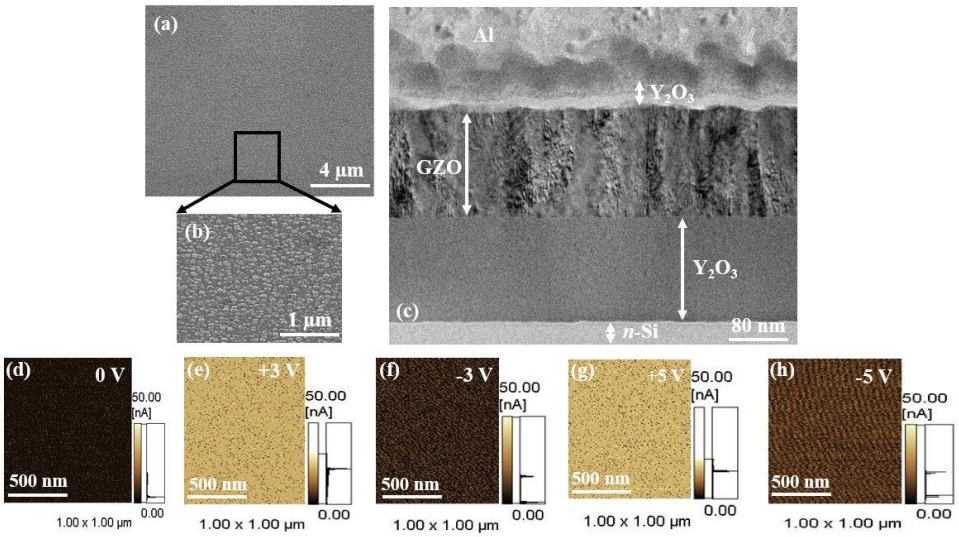

Figure 4.15: (a-b) FE-SEM images of top surface of Y_2O_3 thin film, (c) Cross-sectional HR-TEM image of fabricated memristive structure (n-Si/Y_2O_3/GZO/Y_2O_3/Al), (d-h) Conductive-AFM images of current distribution map in memristive structure at (g) No bias (0 V), (h and i) +3 V (bright: "LRS state") and -3 V (Dark: "HRS state"), respectively, and (j and k) +5 V (bright: "LRS state") and -5 V (Dark: "HRS state"), respectively.

4.5.3 Electrical Characterizations

4.5.3.1 Resistive Switching Response

To analyze the switching response of the crossbar array, top electrode (TE) is connected with the positive/negative voltage polarity of the SCS-4200A while bottom electrode (BE) is fixed to ground as depicted in Figure 4.16(a). For evaluating the switching response, a triangular voltage waveform is imposed on the device with an amplitude of ±3 V and pulse width of 100 ms, as shown in Figure 4.16(e), and captures the resistive switching performance of the single device in the crossbar array, as shown in Figure 4.16(d). During the memristive device testing in the crossbar array, tipping with source measurement unit (SMU) is deployed for target memristive device only and all other remaining devices are in floating condition. The value of compliance current (I_{CC}) is fixed at 20 µA during the measurement to prevent permanent damage to the device. Figure 4.16(b-c) shows the process of switching mechanism under different voltage polarities. When a positive voltage polarity (0 to +3 V) is imposed on the TE, the device resistance state is switched from high resistance state (HRS) to low resistance state (LRS). This process is known as "SET" process, as shown in Figure 4.16(b) and the SET voltage (V_{SET}) of the device is +1.8 V. The detailed switching mechanism of the Y_2O_3-based memristive device is reported by Das *et al* [8].

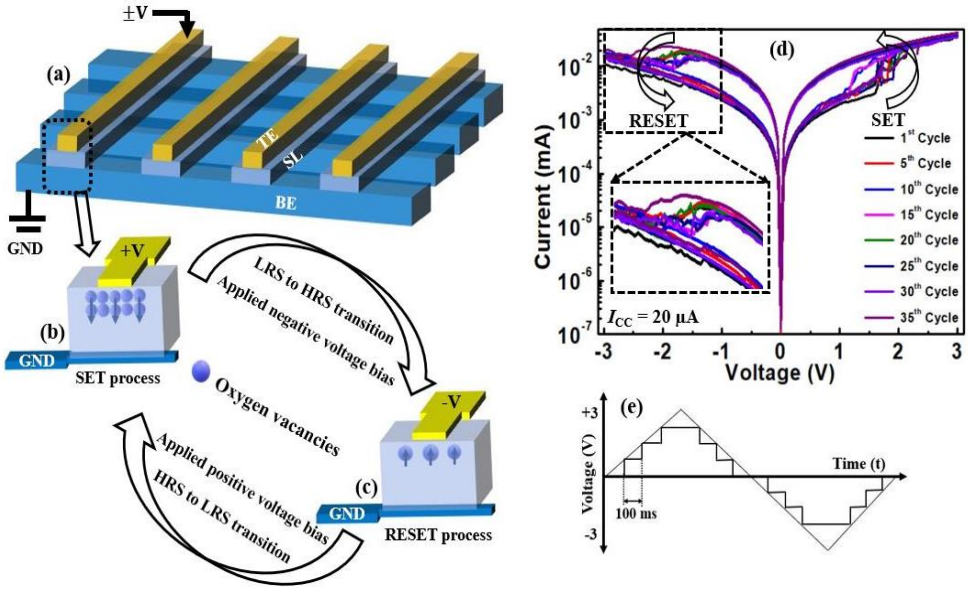

Figure 4.16: (a) Memristive crossbar array architecture. Interfacial switching mechanism in the memristive device: (b) Device during "SET" process under the positive voltage bias, (c) Device during "RESET" process under negative voltage bias, (d) Resistive switching characteristics of fabricated memristive crossbar array and inset shows the enlarge view of the resistive switching responses, (e) Schematic of applied input voltage waveform.

On the other hand, when the negative voltage bias (from 0 to -3 V) is imposed on the TE, the device resistance state is switched from LRS to HRS as described by Das *et al* [8]. This process is termed as "RESET" process as depicted in Figure 4.16(c) and the RESET voltage (V_{RESET}) of the device is -1.93 V. Furthermore, when the applied negative bias on TE is replaced by the positive bias, the device switches back from HRS to LRS as shown in Figure 4.16(b).

As seen from Figure 4.16(d), the resistive switching of devices in the crossbar array consistently follows the memristive behavior in multiple switching cycles and toggle between HRS to LRS and back without any noticeable change in the switching voltages i.e., V_{SET} and V_{RESET}. The negligible variation in the V_{SET} and V_{RESET} shows that the DIBS system is extremely promising to realize a reliable memristive crossbar array.

4.5.3.2 Endurance, Retention and Device Scaling Properties of MCA

To investigate the stability and reliability of the Al/Y_2O_3/GZO crossbar array, the endurance and retention measurements are performed. The devices in the array are observed to be stable up to ~7.5×10^5 switching cycles but beyond ~7×10^5, the value of I_{Ratio} is reduced down to ~30, as depicted in Figure 4.17(a). A high value of current ratio (I_{Ratio} > 200) is observed on an average for the memristive devices in the crossbar array. The high values of endurance and I_{Ratio} confirm that the memristive devices in crossbar array architecture show highly stable, reliable and reproducible resistive switching responses. Figure 4.17(b) depicts the device retention characteristic which can be emphasized that the HRS and LRS are distinctly separated from each other up to 2.25×10^5 s with I_{Ratio} > 200 and beyond 1.5×10^5 s, the value of I_{Ratio} is reduced down to ~30. Similar reduction in the value of R_{Ratio} from 640 to 80 is also reported by the Petzold *et al* [33] in Y_2O_3-based single memristive devices when the retention period goes beyond 5×10^5 s. Baeumer *et al* [34] have also reported that the current level in LRS state is reduced by 90% of its initial value (1 µA) at 10^3 s in the Nb:$SrTiO_3$-based single memristive device.

Maikap *et al* [35] have also reported that the value of R_{Ratio} is decreased from 15 to 10 when the retention period goes beyond 10^4 s in (4×4) TaO_x-based memristive crossbar array. This instability in the current/resistance ratio with time can be attributed to insufficient heat dissipation [36] while the device is under operation and, therefore, can be correlated with a writing error.

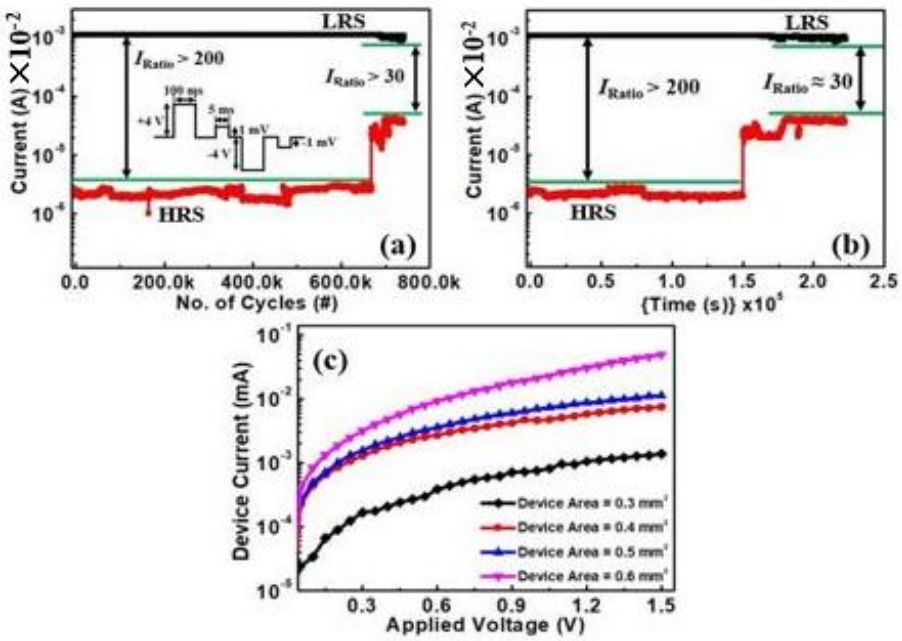

Figure 4.17: (a) Endurance measurement up to 7.5×10^5 cycles and degradation is found nearly 7×10^5 cycles in current ratio, and inset shows the applied input programming voltage pulse, (b) Retention measurement of the fabricated device up to 2.25×10^5 s and degradation is found nearly 1.5×10^5 s in current ratio, (c) Effect of area scaling via shadow mask on device current.

Moreover, in the oxide films, the spontaneous distribution of the oxygen vacancies upon reduction of the electric field is related to the thermal diffusion assisted by the repelling coulombic forces of the ionized vacancies [37]. Figure 4.17(c) shows the increase in current with the corresponding rise in the active area of the device [8]. At the third stage of the device fabrication via shadow masking technique, as depicted in Figure 3.4(h) in the chapter 3, the device area is scaled down from 0.6 to 0.3 mm^2 and subsequently the device current is measured.

4.5.3.3 Memristive Device Production Yield in Crossbar Array

The device yield is one of the crucial parameters in a memristive crossbar array, describes the percentage of working devices on a wafer-scale in comparison to total fabricated devices during a single fabrication process. The level of yield determines the cost-effectiveness and commercialization viability of the system. In total, 180 GZO/Y_2O_3/Al devices are measured

from the crossbar arrays, and 143 of them display bipolar resistive switching, as shown in Figure 4.16(d), implying a yield of 79.44% which are depicted in Figure 4.18.

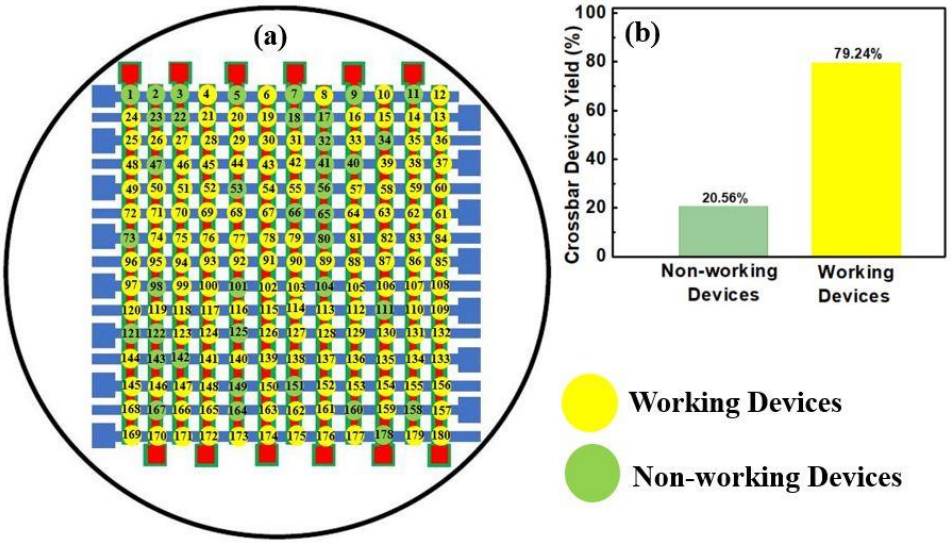

Figure 4.18: (a) Working and non-working devices mapping in (15×12) crossbar array structure, (b) Percentage scale for corresponding device yield.

It is important to note that the production device yield in the memristive crossbar array signifies an ambitious scientific importance to further decline the device manufacturing cost significantly. However, the memristive devices in the crossbar array structure still face poor fabrication yield and reliability which further hinder them from direct practical applications [38]. Here, to investigate the production yield of the fabricated memristive crossbar array, we have measured switching responses of all 750 devices in the array size of (30×25) and ~92.67% devices display a bipolar, stable, repeatable, and reliable switching response.

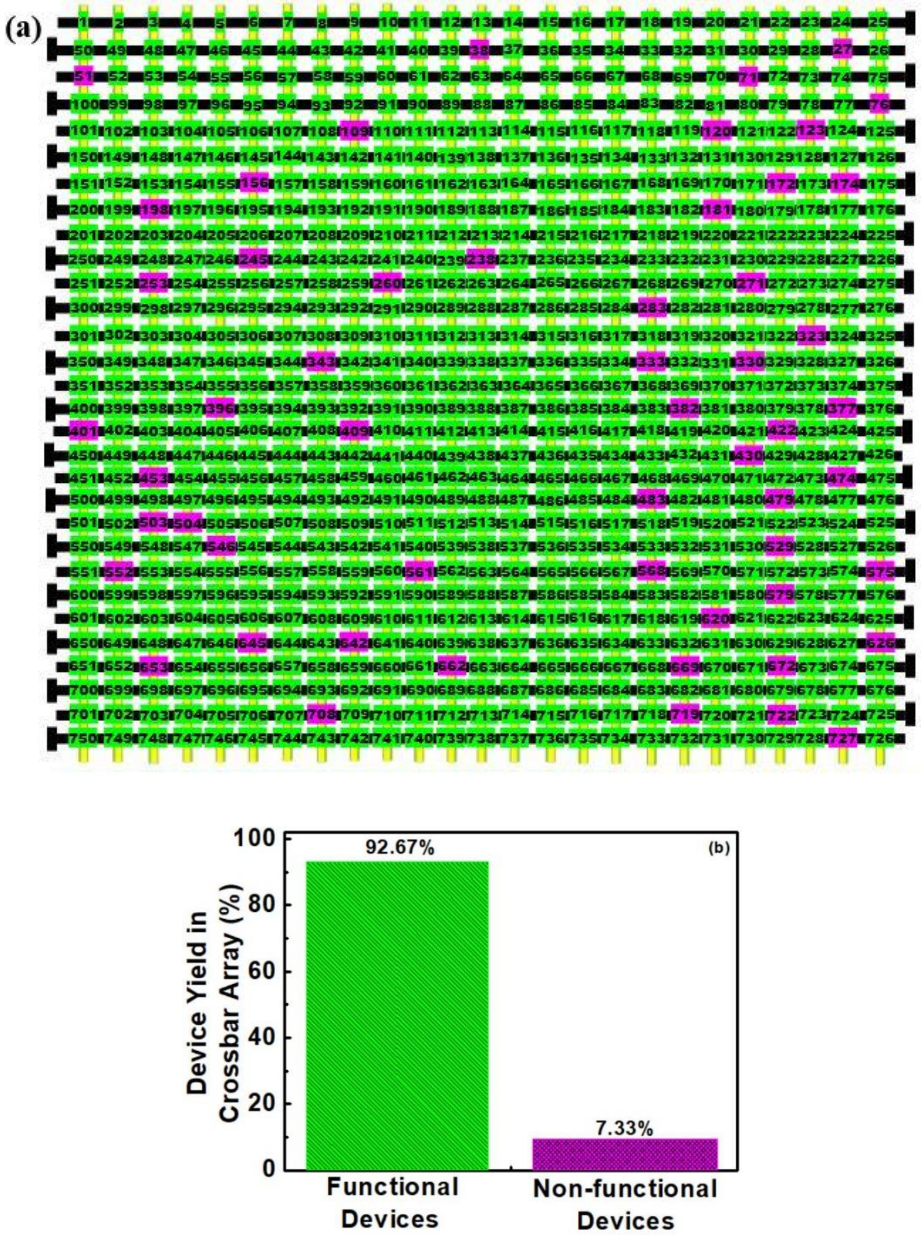

Figure 4.19: (a) Wafer-level location mapping for functional and non-functional devices in the (30×25) crossbar array, (b) Device yield in a percentage scale.

The wafer level location mapping and percentage yield of the functional and non-functional devices is depicted in Figure 4.19. The device yield can be further improved by involving nanofabrication processes as reported in previous reports [39-40] while realizing the crossbar array with reduced individual device area and larger device density and precise control over contaminants during the fabrication process as carried out in a cleanroom environment.

4.5.3.4 D2D and Device Area Impact on Switching Voltages

Figure 4.20(a-b) shows the variation in V_{SET} and V_{RESET} in various devices in the fabricated crossbar array structure. The devices in the crossbar array show lesser variation in V_{SET} and V_{RESET} in the D2D which further confirms that the fabricated crossbar array is highly stable and reliable with minimized D2D variations [31]. Figure 4.20(c) shows the location map for the devices (D1-D5) used in Figure 4.20(a-b).

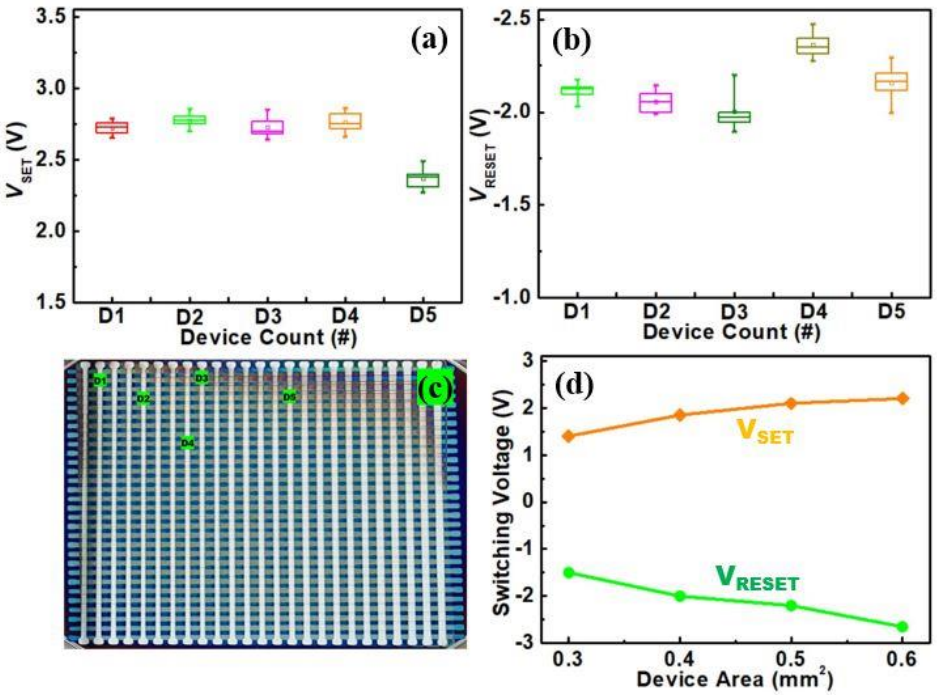

Figure 4.20: (a) Resistive switching response of device D4 in the fabricated MCA, (b-c) Variation in V_{SET} and V_{RESET} in D2D (5 devices are used). The error boxes show the slight variation in the V_{SET} and V_{RESET} during C2C operation of the device. (d) Impact of device area scaling on switching voltages.

The impact of device area scaling over the switching voltages is shown in Figure 4.20(d). It is observed that when the device area increases, the corresponding values of V_{SET} and V_{RESET} of the device are marginally increased. The slight variation in V_{SET} and V_{RESET} is associated with the observable increment in the device current due to the increment in the device active area which is favorable in terms of the availability of more

electronic sites for current conduction as reported by Das *et al* [8] and Nirantar *et al* [41].

4.5.3.5 Multilevel Current Programming Functionality and Potentiation and Depression Processes

To evaluate the multilevel current programming scheme on the fabricated MCA, we have selected the MCA size of (8×8) and varied the amplitude of applied input voltage (V_A) from +1.3 V (Figure 4.21(a)), +2.1 V (Figure 4.21(b)), +3 V (Figure 4.21(c)) to +4 V (Figure 4.21(d)) with constant 20 input pulses and 10 ms pulse width (PW). Here, word lines correspond to the top electrodes (TEs) and bit lines correspond to the bottom electrodes (BEs) of the fabricated MCA structure. As shown in Figure 4.21(e), the fabricated MCA exhibits multiple and distinct current levels when all the devices are in the 'ON' states, which further extends the capability of the fabricated MCA for a multilevel current programming scheme. Further, it should be noted that the device current is varied from 10 to 108 µA under different values of V_A with constant number of pulses, as depicted in a color bar of the current distribution map.

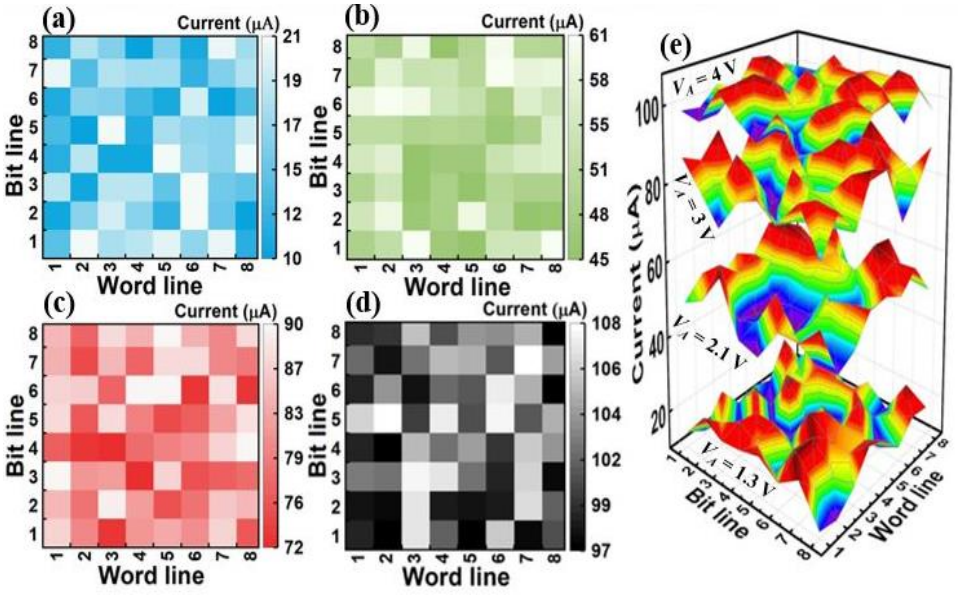

Figure 4.21: Multilevel current mapping of fabricated MCA devices with an array size of (8×8): (a) V_A = +1.3 V, (b) V_A = +2.1 V, (c) V_A = +3 V, (d) V_A = +4 V with 20 pulses and 10 ms pulse width, (e) Distinct current levels.

To extend the functionality of the fabricated MCA, synaptic weight modulation characteristics have been investigated. The potentiation and depression features of the artificial synapse have been mimicked by applying the input voltage pulses. Figure 4.22(a) shows the potentiation (P) process, wherein the device conductance is continuously strengthened under the application of 50 positive successive pulses with V_A = +1.3 V and PW = 10 ms. In the depression (D) process, 50 negative pulses are applied with of V_A = -1.0 V and PW = 10 ms, as depicted in Figure 4.22(b). Here, the amplitude of the read voltage pulse (V_R) is 0.1 V. Figure 4.22(c) and (d) show the combined plot and normalized current distribution of P and D. The nonlinearity (NL) factor values between P and D are found to be 0.67 at pulse number (n) = 25. The value of NL is defined the symmetrical behavior of the P and D with respect to linear fitting line. The obtained memristive device characteristics are in good agreement with the P and D functionalities of the real biological synapse [42].

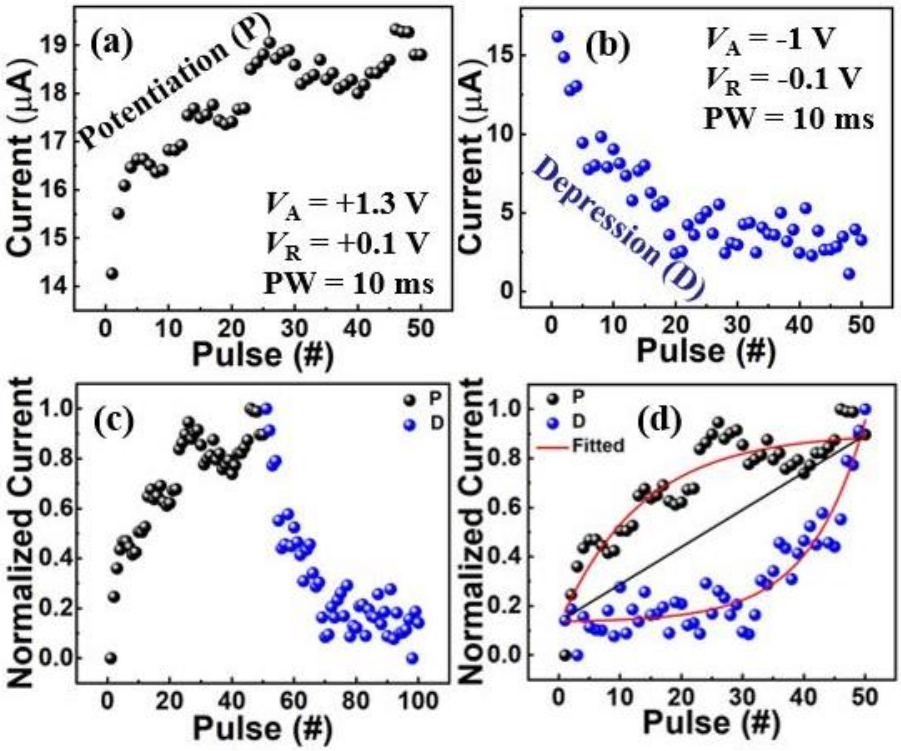

Figure 4.22: (a) Potentiation, (b) Depression, and (c-d) Normalized current distribution synaptic behaviors of the MCA. The pulse parameters are shown in the inset of each figure.

4.5.3.6 Demonstration of Spike Time Dependent Plasticity (STDP) on Fabricated MCA

The activity-dependent plasticity of fabricated MCA has been investigated by utilizing the Hebbian learning-based spike-time-dependent plasticity (STDP) rules. According to the Hebbian theory, the synaptic efficiency is strengthened/weakened by controlling the pre-and post-synaptic pulse activity [43-44]. The STDP responses are varied due to different spikes of stimulus reaching the synaptic cleft at different time intervals [45]. Sometimes, the polarity of the synaptic weight changes due to the temporal order of the pre- and post-synaptic spikes, as shown in Figure 4.23(a) and (b). While in other cases, the polarity of the synaptic weight is modulated due to the relative timing of the pre-and post-synaptic spikes, as shown in Figure 4.23(c) and (d). The exponential and Gaussian functions have been utilized to calculate the scaling factor (A), and time constant (τ) of STDP events. These variables are useful in computational neuroscience and neuromorphic hardware design [46].

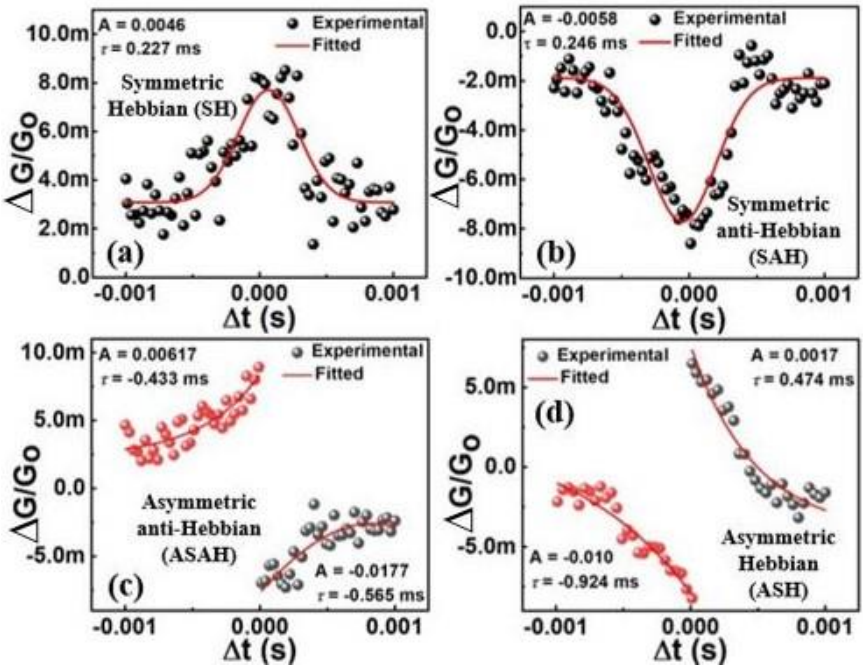

Figure 4.23: Demonstration of biological STDP forms mimicked using Y_2O_3 MCA. The values of A and τ are shown in the inset of each figure. (a) Symmetric Hebbian learning and (b) symmetric anti-Hebbian learning. Applied training spikes for (c) asymmetric anti-Hebbian learning and (d) asymmetric Hebbian learning.

As seen in Figure 4.23, four different types of STDP learning rules such as symmetric Hebbian (Figure 4.23(a)), symmetric anti-Hebbian (Figure 4.23(b)), asymmetric anti-Hebbian (Figure 4.23(c)), and asymmetric Hebbian learning rules (Figure 4.23(d)) are mimicked by utilizing the Y_2O_3 MCA and can be controlled with amplitude, polarity and duration of pre- and post-spikes [46-47]. Here, it should be noted that the effect of synaptic weight modulation can be more pronounced when trains of pre/post spikes are imposed on the electronic synapse as compared to the single pre/post pair which is similar to the biological synapse [46-48]. Moreover, by designing and optimizing the pulse schemes, the time constant can be further modulated in a wide temporal range, from the biological millisecond scale down to ultrafast nanoseconds [46]. This enables the flexibility of the neural circuit to design the neuromorphic system effectively.

4.6 Conclusion

In summary, an analytical model for a Y_2O_3-based memristive system with synaptic behavior and stable resistive-switching phenomena has been discussed. The learning and forgetting characteristics of the proposed analytical model display ~20.1% maximum deviation error with the experimental data, which is less than that reported elsewhere. The proposed model can be further considered for modeling of memristive devices for neuromorphic application. Further, a generic non-linear analytical model has been discussed for any material-based memristive system displaying resistive switching, synaptic learning and synaptic plasticity characteristics which are essential parameters for neuromorphic computing. The proposed model and its piecewise window function have shown better non-linear behavior in device current at device boundaries by considering the rectifying nature and non-ideal effects which are not incorporated by the other reported models available in the literature. The synaptic plasticity characteristic of modeled data shows ~4.44% MED in case of Y_2O_3 and ~4.5% MED in case of WO_3 with respect to corresponding experimental

results and these values are the least as compared to values reported in the literature till date.

Here, we have also discussed a physical electro-thermal modeling of nanoscale Y_2O_3-based memristor device. The simulated outcomes show the stable RS behavior in the pinched hysteresis RS response with multiple switching cycles. The simulated switching characteristics show lower values of C_V , i.e., 17.36% and 17.09% in V_{SET} and V_{RESET}, respectively, in C2C variation. The physical modeling also reveals the impact of V_{RR} on the device switching characteristics and shows that when V_{RR} is increased, switching voltages are slightly increased because under fast V_{RR} the device switching speed is increased and no sufficient time is available for the mobile vacancies to settle down. Moreover, the simulated memristor device has also effectively emulated the synaptic plasticity behavior which is analogous to the functionality of human brain. The simulation study reveals the impact of V_{RR} on device switching response which further significantly affects the synaptic plasticity functionality of the memristor device.

The fabricated (15×12) and (30×25) Y_2O_3-based memristive crossbar array architectures exhibit stable resistive switching characteristics based on interfacial mechanism, consistent switching repeatability in multiple cycles, and low variability in V_{SET} and V_{RESET} characteristics. Moreover, the fabricated crossbar array shows high current ratio (> 200), high device yield (79.56% in (15×12) and 92.67% in (30×25) crossbar arrays), excellent endurance characteristics up to ~7.5×10^5 (0.7 million) cycles and high retention of ~2.25×10^5 s. Furthermore, a large-area fabricated crossbar array of (30×25) on 3-inch Si substrate also depicts the excellent resistive switching properties with remarkable stability, repeatability and reproducibility in the resistive switching phenomena. The fabricated devices in crossbar array show a marginal variation in V_{SET} and V_{RESET} in case of D2D which further confirms the smooth and uniform thin film deposition by utilizing DIBS. The fabricated MCA structure are also fully capable to perform the multilevel current programing functionality under the application of varied input voltage amplitude which further utilize these

devices for multi-bit storage application. The realized MCA successfully demonstrated the synaptic learning capability by performing potentiation and depression processes at low input voltage and also effectively demonstrated the STDP analysis which are similar with the different type of Hebbian learning rules and analogous to the real biological system characteristics. This is encouraging for the practical application of the large-area memristive crossbar array. The feasible fabrication process via DIBS system also leads to the fabrication of high-density crossbar array with low-cost, and scalable manufacturing possibilities for the next-generation resistive memory devices.

4.7 References

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Chapter 5

Analysis of Coefficient of Variability in D2D and C2C

5.1 Introduction

As it is widely accepted that the memristive devices are one of the most promoting emerging memory technologies due to its outstanding features such as down-scaling, low power consumption, high speed, and possibility of multibit operation [1-6]. These aforementioned features are most useful in logic-in-memory applications, and neuromorphic computing architectures [1-6]. In the memristive devices, under the application of external electrical stimulus, the resistance of the switching oxide layer is changed between two distinct resistance states namely as; low resistance state (LRS) and high resistance state (HRS). In the simplest observation, the device can be SET under the LRS and RESET into the HRS, which further can be logical categorized as "1" and "0", respectively. However, there are several major hurdles to implement the large-scale memristive crossbar array into state-of-the art memory, in-memory computation and logic applications, are large device-to-device (D2D) and cycle-to-cycle (C2C) variabilities in both LRS and HRS or in the device switching voltages i.e., V_{SET} and V_{RESET} [7-8]. These variabilities typically follow a log-normal distribution [8] which can describe the stochastic nature of the switching process within one cell. Due to these variabilities, multiple resistances states are obtained for each switching cycle and for different cells on the same chip [9].

The resistive switching process in the transition metal oxides is happened to be driven by the nanoscale level movement of the donor-type defects such as oxygen vacancies [1, 10-11]. The nanoscale level movement further may help to change the resistance of the switching oxide layer or the resistance of the electrode/oxide interface [1, 10-11]. In the case of electroforming resistive switching mechanism, continuous conductive filaments (CFs) are formed between top and bottom electrodes [12]. The stochastic nature of the CFs has been suspected phenomenologically and

affected the thermodynamic stability of the generation/recombination of the oxygen vacancies into CFs [13-14] which further affects the shape and oxygen vacancy distribution of the CFs [12, 15-16]. Importantly, during the formation and rupture processes of CFs, the changes in microscopic structure of switching oxide layer which might cause the C2C variability in redox-based memristive devices.

The primary source of the variability is associated to the stochastic nature of the resistive switching process [8] inside the resistive switching layer which results in the different resistances states for each switching cycle and different values of resistance obtained for different memory cells on the same crossbar chip [17]. More specifically, the D2D variability is associated to the inhomogeneity in the switching system originated from the fabrication process [18-19]. Further, D2D can be a major obstacle to develop a large-scale passive crossbar array for accurate analog computation [20]. On the other hand, the C2C variability is connected with the stochastic nature of the resistive switching in a memristive device. Furthermore, the large field-accelerated random migration of ions also leads the variability in the memristive systems [9]. The induced local Joule heating and random ionic/electronic conductions are also affected the consistency in the resistive switching characteristics [9].

The electroforming-based memristive devices are more suffered from the large D2D and C2C variabilities because of the growth and disruption processes of the CFs are not well controlled [17]. On the other hand, to reduce the variability, an electroforming-free interface dominated, highly stable and uniform resistive switching characteristics of the memristive devices with high retention and endurance parameters are highly desired for neuromorphic computing and image processing. Moreover, in case of an electroforming-free memristive devices, the device switches from the pristine state to a particular resistance state depending on the applied input signal which excludes the unnecessary application of a strong electric field during the electroforming process that leads to large D2D variation or even damages the memristive system.

5.2 D2D Variability in Memristive Crossbar Array

Device-to-device (D2D) or spatial variations are the major obstacles to design and implementation of large-scale memristive crossbar array-based artificial neural networks (ANNs). Under D2D variations, various devices in the crossbar array show different non-linearity in the resistive switching characteristics. These variations are mostly appeared in the electroforming type memristive devices such as valance change memory (VCM) or electro-chemical memory (ECM) due to stochastic nature of formation and rupture of the CFs [17, 21]. The D2D variation is connected with the randomness occurred in the electroforming process which further leads to the different shapes and structures of the CFs inside the devices [21]. Therefore, it is essential to avoid the electroforming process during design and implementation of the large crossbar arrays.

On the other hand, forming-free resistive switching mechanism-based memristive devices with selector are played a very important role as it usually operates more frequently as compared to memristive device. However, if selector and memristive device face large switching variations, it will further increase the difficulties leads to the failure in the operation of crossbar arrays. Many fabrication strategies have been developed to design and implement the forming-free devices-based memristive crossbar array. Several studies [22-23] have been demonstrated to change the thickness of the resistive switching materials and some of the reported studies [24] utilized a conductive oxide materials layer as a bottom interface to increase the bottom interface resistance and eliminate the electroforming process as well as the effect of breakdown. Therefore, by controlling the concentration of defects such as oxygen vacancies or ions can also help to develop electroforming free resistive switching behavior-based memristive crossbar array [25-26]. Instead of the formation of CFs under the application of applied external electric field, the preformed CFs can also be avoided by precise control over the manufacturing process [27-21].

Generally, metal oxide-based memristive systems often show large variation, due to the stochastic nature of the switching process [17]. A

statistical analysis of 120 *I-V* switching cycles has been investigated on 30 GZO/Y_2O_3/Al memristive devices for quantitative estimation of the D2D variabilities in V_{SET} and V_{RESET} parameters by evaluating the coefficient of variation (C_V) by calculating the ratio of standard deviation (σ) to the mean value (μ) [28].

The statistical distribution of D2D variability data is plotted in Figure 5.1. The distribution is measured at I_{CC} of 20 µA and it is observed that the statistical distribution parameters are almost independent of the value of I_{CC} as depicted in Figure 5.2. The insignificant dependency of the variability on I_{CC} may be attributed to large bottom interface resistance (> 200 kΩ) at GZO/Y_2O_3. The statistical distribution in V_{SET} and V_{RESET} for D2D is matched with Gaussian fitting curves. The values of goodness of fitting (Chi-Sqr (χ)) and the error coefficient (R^2) are estimated as 0.01576 and 0.94635, respectively, for V_{SET} and 0.045 and 0.91386, respectively, for V_{RESET} in case of D2D variability, as described in Figure 5.1(a) and 5.1(b).

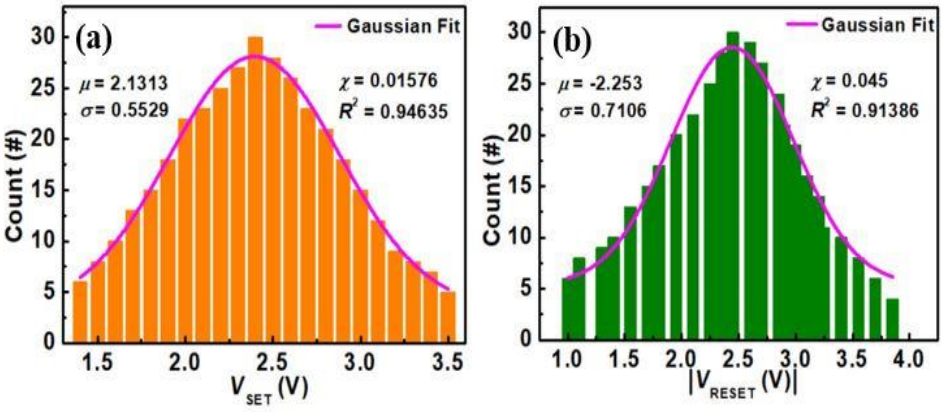


Figure 5.1: D2D statistical distribution of (a) V_{SET} and (b) V_{RESET} for 30 memristive devices fitted with Gaussian curves.

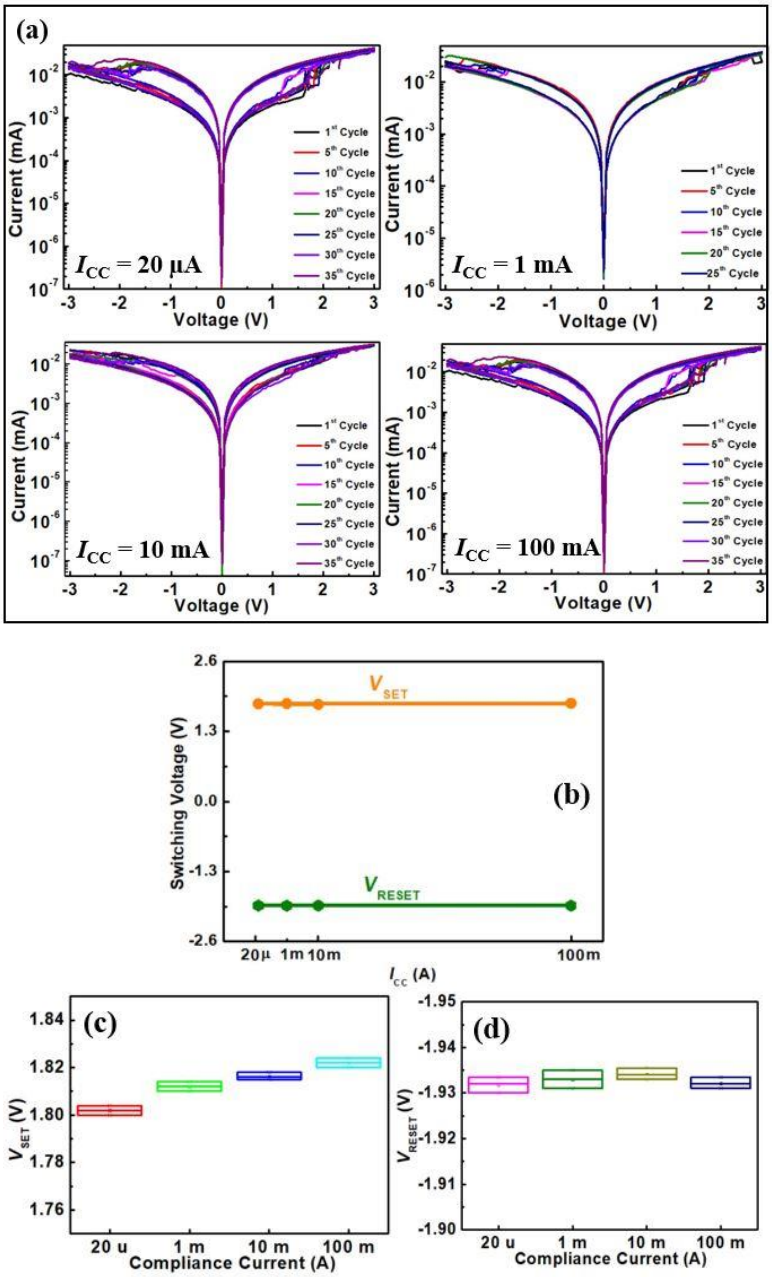


Figure 5.2: (a) Resistive switching response of memristive device at different values (20 µA, 1 mA, 10 mA, 100 mA) of compliance current (I_{CC}), (b) Negligible variation in V_{SET} and V_{RESET} over the different values of I_{CC}, (c-d) Error bar plots show the negligible variations in V_{SET} and V_{RESET} over different values of I_{CC}.

The cumulative probability distribution of D2D variability data is plotted in Figure 5.3 which shows the cumulative probability distribution in V_{SET} and V_{RESET} for 30 memristive devices using I_{CC} of 20 µA. The values of C_V for D2D variability in V_{SET} and V_{RESET}, as described in Figure 5.3 are 0.25

and 0.3154, respectively. Moreover, the experimentally obtained values of D2D, as described in Table 5.1, are comparatively less than those reported for TiN/HfO_x/AlO_y/Pt and Au/Cu-SiO_2/Cu resistive system-based crossbars, as reported in the published literature [29-31].

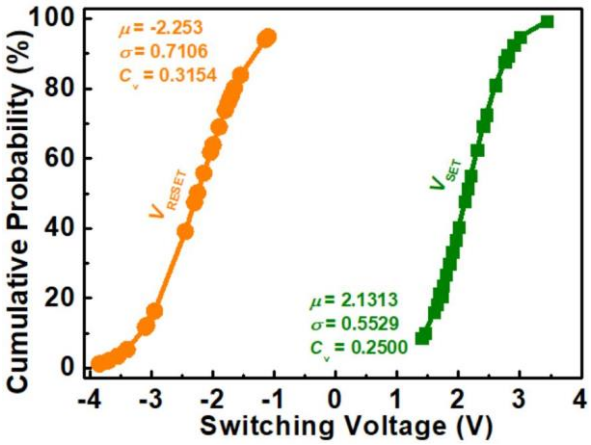


Figure 5.3: D2D cumulative probability distribution in V_{SET} and V_{RESET} for 30 memristive devices.

5.3 C2C Variability in Memristive Crossbar Array

The cycle-to-cycle (C2C) variation is associated with the instability in the CFs or random/stochastic formation of new CFs. However, by adopting perfect fabrication strategies it can be possible to control the CF formation/dissolution to reduce the C2C variation significantly. Previously, several reports [31-33] have been published in which bilayer resistive switching is adopted to confine the formation and rupture of CFs. More specifically, in this bilayer memristive structure, two different thermal conductivities and oxygen ion migration layers have been utilized which helps to increase the interface barrier. Thus, the CFs is completely ruptured in one oxide layer and remain unchanged in another oxide layer. The partially ruptured CFs in the bilayer structure can play a significant role in confining the formation of CFs which further beneficial for the uniform resistive switching.

On the other hand, if the interfaces between the resistive switching materials and the electrodes are not uniform, there should be many local sites available for CFs nucleation which further increases the randomness

of the film, especially its switching parameters. When a memristive device incorporates a uniform material with a smooth surface, a conducting paths and interfaces of the film surface are uniformed as compared to the random or zigzag which provides the reasonable similarity and uniformity in conductive sites and interfaces [34].

A statistical analysis of 120 *I-V* switching cycles is performed for quantitative estimation of the C2C variability in V_{SET} and V_{RESET} parameters by evaluating the coefficient of variation (C_V) by calculating the ratio of standard deviation (σ) to the mean value (μ) [28]. The statistical distribution of C2C variability data is plotted in Figure 5.4. The distribution is measured at I_{CC} of 20 µA and it is observed that the statistical distribution of V_{SET} and V_{RESET} for C2C are matched with Gaussian fitting curves. For C2C variation, the values of χ and R^2 are estimated as 0.000639 and 0.9611, respectively, for V_{SET} and 0.002071 and 0.9482, respectively, for V_{RESET}, as described in Figure 5.4(a) and 5.4(d).

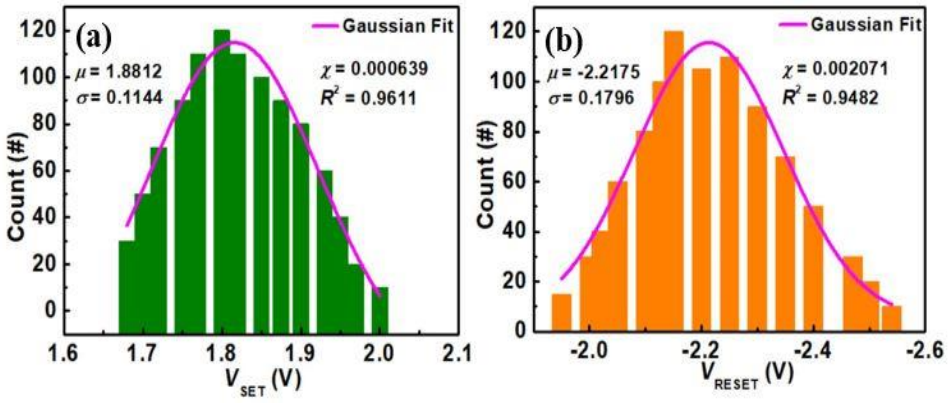


Figure 5.4: C2C statistical distribution for 120 cycles of (a) V_{SET} and (c) V_{RESET} in a single memristive device with Gaussian fitting.

The cumulative probability distribution of C2C variability data is plotted in Figure 5.5. The values of C_V for C2C variability in V_{SET} and V_{RESET}, as presented in Figure 5.5, are 0.0608 and 0.0809, respectively. These values, as described in Table 5.1, are comparatively less than those reported for TiN/HfO_x/AlO_y/Pt and Au/Cu-SiO_2/Cu resistive system-based crossbars, as reported in the published literature [29-31].

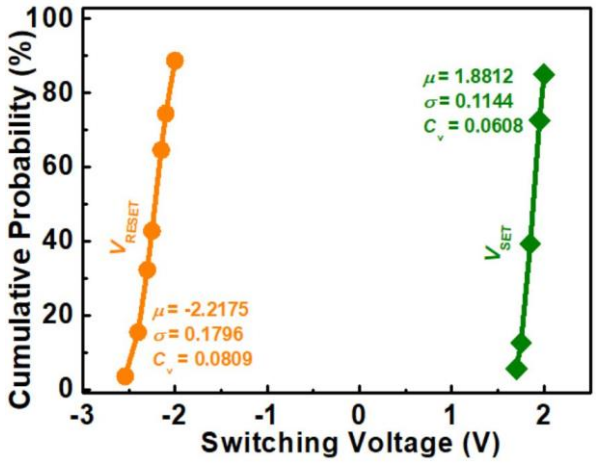


Figure 5.5: C2C cumulative probability distribution in V_{SET} and V_{RESET} for 120 cycles in a single memristive device.

Moreover, the C2C variability is associated with the stochastic nature of resistive switching in the memristive device and it is related to the large field-accelerated random migration of ions which leads the variability in memristive devices [35]. Besides that, the induced local Joule heating and random ionic/electronic conduction also account for the undesirable variations in the RESET and SET characteristics [35]. Hayakawa *et al* [36] and Niu *et al* [37] have demonstrated that the careful control of ionic movement to reduce the C2C variability in memristive devices which can also minimize the D2D variability as both are interlinked to each other in memristive crossbar array.

Table 5.1: Comparative analysis between our work and previously reported data.

References	**Our work**	Ref. [29]	Ref. [30]	Ref. [31]
Memristive structure in the crossbar	**GZO/Y_2O_3/Al**	TiN/HfO_x/AlO_y/Pt	Au/Cu-SiO_2/Cu	TiN/SiCN/Ta/Cu
Crossbar array size	**(15 ×12)**	(24×24)	(4×4)	(2×2)
V_{SET}/V_{RESET} (V)	**+1.8/-1.93**	+0.9/-2	+3/-3	+4/-2.6
Retention time (s)	**~2.25×10^5**	10^4	10^6	-
Endurance (cycles)	**~7.5×10^5**	10^4	10^4	150
I_{Ratio}	**> 200**	10-15	> 100	50
C_v for C2C variability	**0.0608 in SET 0.0809 in RESET**	0.1014 in SET 0.1554 in RESET	-	> 0.1504 in SET > 0.1244 in RESET
C_v for D2D variability	**0.25 in SET 0.3154 in RESET**	-	> 0.3517 in SET > 0.3253 in RESET	> 0.3519 in SET > 0.3210 in RESET
Deposition technique	**DIBS**	Atomic Layer Deposition	Aerosol jet printing	Radio Frequency-Plasma Enhanced Chemical Vapor Deposition

5.4 Impact of V_A, I_{CC}, and PW on C_V of D2D and C2C

It is well-known that the resistive switching phenomena is influenced by the levels of applied input voltage (V_A) and pulse width (PW) [38] as these two factors have significant impact on the Joule heating of individual device [17]. In memristive devices, the variation in the random distribution of oxygen vacancies at the interfaces and in the bulk switching material [28, 38-39] are also significantly affected by the values of V_A and PW.

Cumulative probability distribution in V_{SET} and V_{RESET} of D2D with varied compliance current (I_{CC}) is depicted in Figure 5.6. As observed from Figure 5.6, C_V values of 6.03%, 5.98% and 2.64% in V_{SET} and 11.51%, 10.13% and 11.36% in V_{RESET} are obtained at I_{CC} of 100, 200 and 300 µA, respectively. The low values of D2D C_V confirm the stability and reliability of the MCA developed on a 3-inch Si substrate. The D2D variability is associated with the inhomogeneity in the memristive cells which induces from the fabrication process [8, 18-19, 35] and poses a stringent challenge in the fabrication of large-scale MCA on a chip level [35].

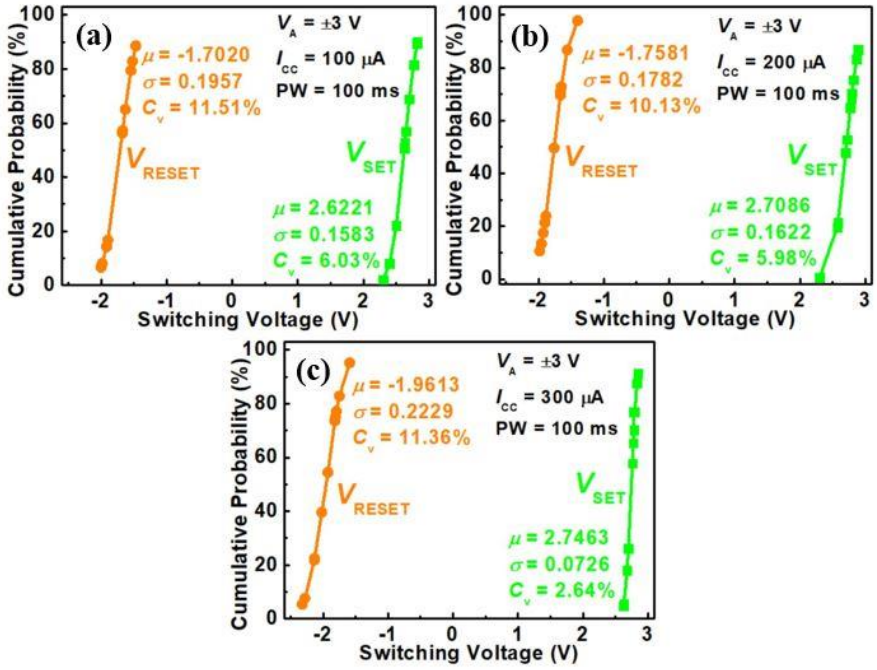


Figure 5.6: (a-c) D2D cumulative probability distribution in V_{SET} and V_{RESET} voltages at I_{CC} of 100, 200, 300 µA, respectively.

Cumulative probability distribution in V_{SET} and V_{RESET} of C2C with varied I_{CC} is presented in Figure 5.7. As observed from Figure 5.7, ultralow values of C_V of 1.58%, 0.2% and 0.4% in V_{SET} and 2.69%, 1.14% and 1.07% in V_{RESET} are obtained at I_{CC} of 100, 200 and 300 µA, respectively. These significantly ultralow values of C2C C_V establishes that the fabricated MCA has excellent cyclic stability, repeatability and reproducibility.

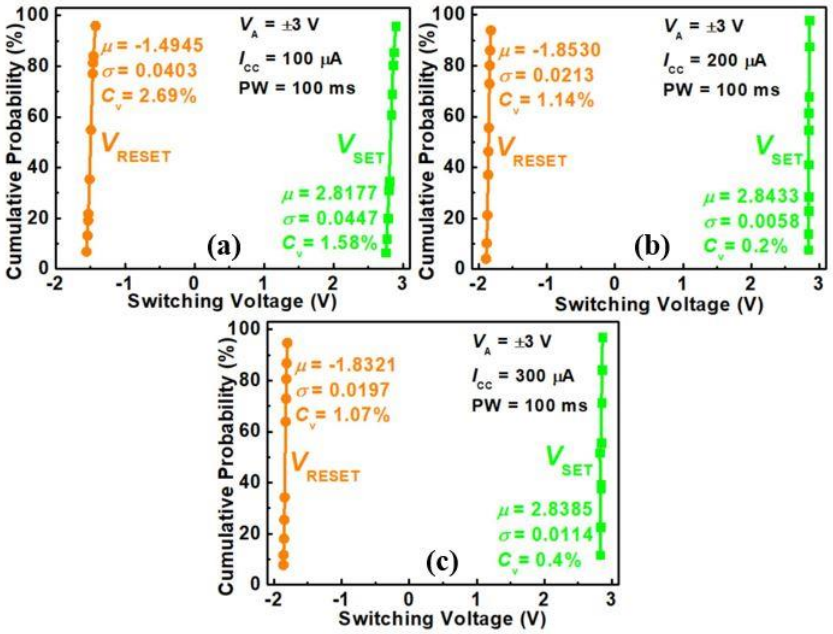
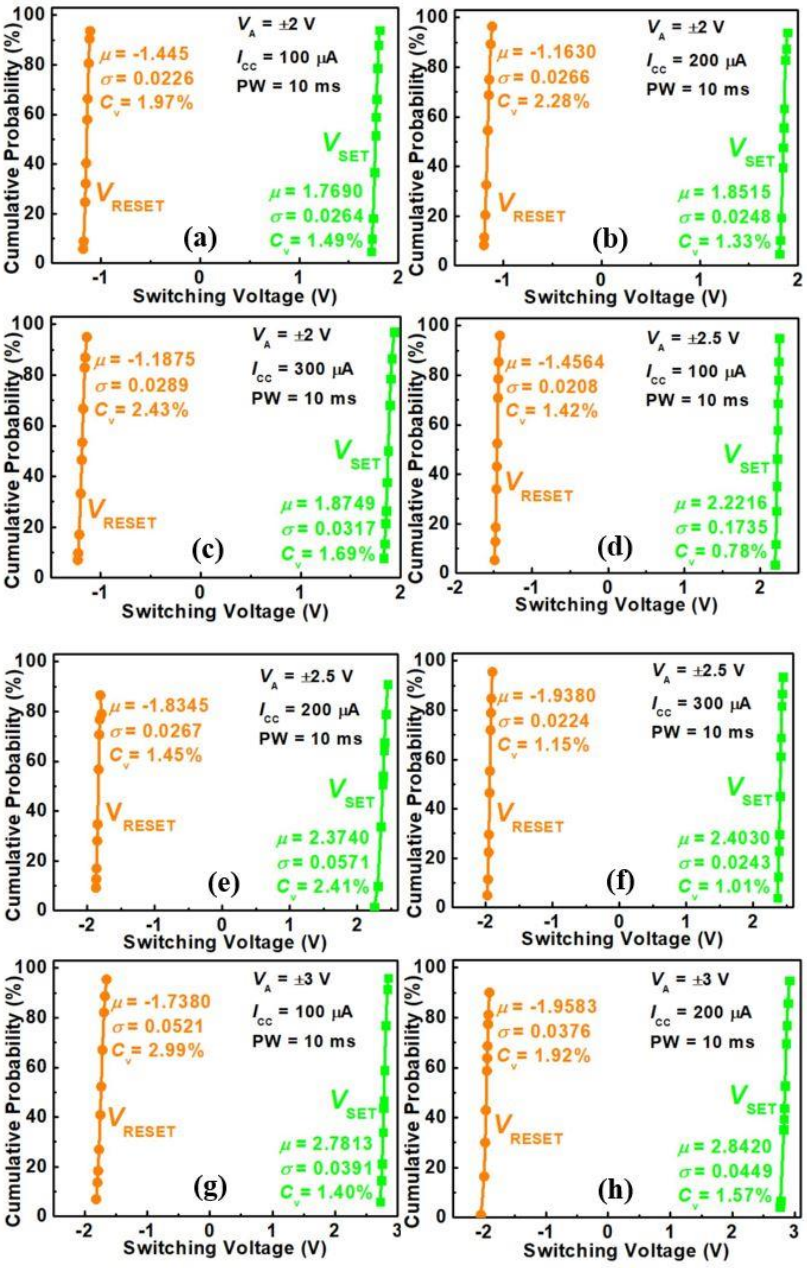


Figure 5.7: (a-c) C2C cumulative probability distribution in V_{SET} and V_{RESET} voltages at I_{CC} of 100, 200, 300 µA, respectively.

Further, the impact of V_A together with the variation in I_{CC} and PW on C2C C_V is depicted in Figure 5.8. From Figure 5.8, it can be observed that at the higher I_{CC} (300 µA), the values of C_V are smaller in both V_{SET} and V_{RESET} as compared to the lower I_{CC} (100 µA). At V_A of ±3 V, the calculated value of C_V in V_{SET} and V_{RESET} are minimized as compared to those for other applied voltage levels i.e., ±2 and ±2.5 V. Similarly, at higher PW (100 ms), the values of C2C C_V in both V_{SET} and V_{RESET} are comparatively lower as compared to those at lower PW (10 ms), as depicted in Figure 5.8. The efficient resistive switching of devices is observed under 10 and 100 ms PW, however, the values of C_V are comparatively lower in the case of 100 ms which may be attributed to the larger memory cell in the MCA. Moreover, we have experimentally achieved significantly low values of

D2D and C2C C_V are compared to those reported by other researchers [28, 31, 40] in Table 5.2.



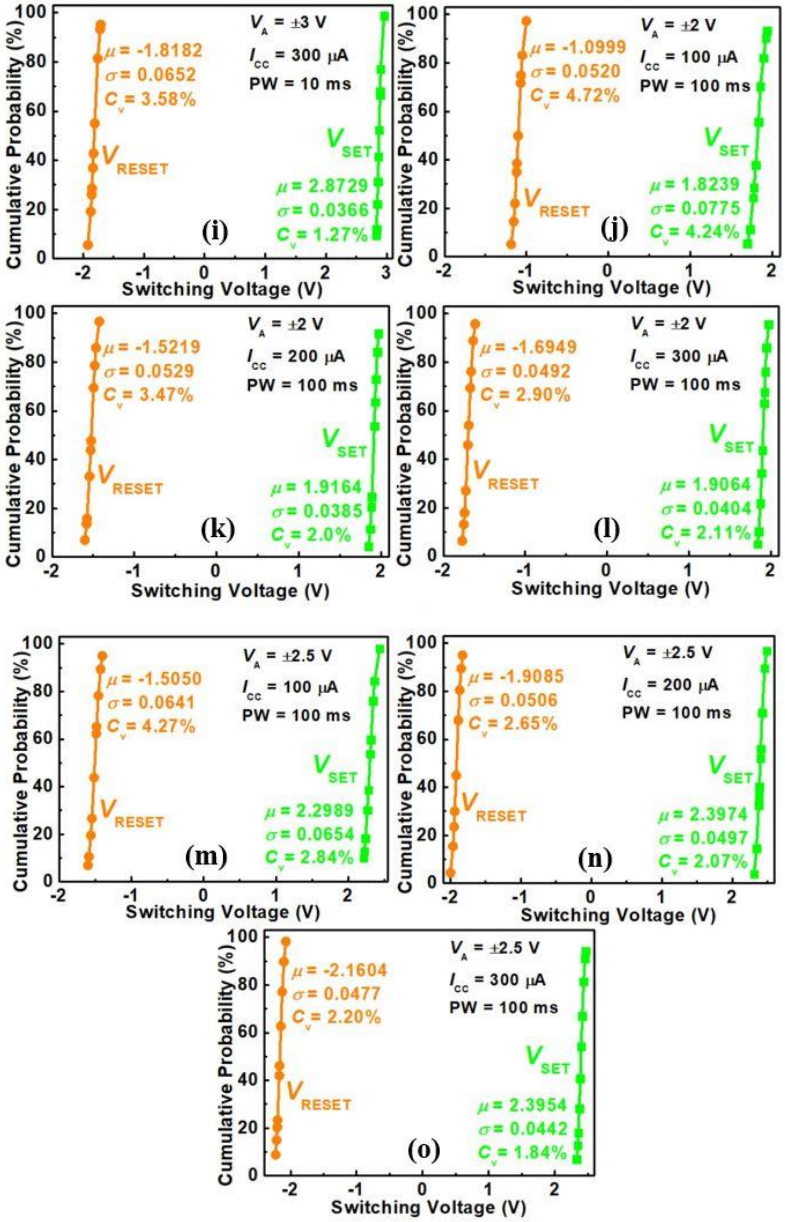


Figure 5.8: C2C cumulative probability distribution in V_{SET} and V_{RESET} voltages at (a-c) V_A = ±2 V, I_{CC} varied from 100 to 300 µA, and PW is constant at 10 ms, (d-f) V_A = ±2.5 V, I_{CC} varied from 100 to 300 µA, and PW is constant at 10 ms, (g-i) V_A = ±3 V, I_{CC} varied from 100 to 300 µA, and PW is constant at 10 ms, (j-l) V_A = ±2 V, I_{CC} varied from 100 to 300 µA, and PW is constant at 100 ms, (m-o) V_A = ±2.5 V, I_{CC} varied from 100 to 300 µA, and PW is constant at 100 ms.

Table 5.2: Comparative analysis between our work and previously reported data.

References	**Our work**	Ref. [28]	Ref. [31]	Ref. [40]
Memristive structure in the crossbar	**Al/Y_2O_3/GZO**	Ag/h-BN/Ag	TiN/Al_2O_3/SiCN/Ta/Cu	Ti/$HfSe_2$/Ti/Au
Crossbar array size	**(30 ×25)**	(10×10)	(2×2)	(5×5)
V_{SET}/V_{RESET} (V)	**+2.72/-2.24**	+2.60/-2.25	+2/-2	+0.7/-1.4
C_v for C2C variability	**SET: 0.2% and RESET: 1.07%**	SET: 1.53% and RESET: 6.21%	SET: 3.45% and RESET: 3.7%	SET: 2.42% and RESET: Not Available
C_v for D2D variability	**SET: 2.64% and RESET: 10.13%**	SET: 5.74% and RESET: 12.37%	Not Available	SET: 18.05% and RESET: 31.21%
Deposition technique	**DIBS**	Chemical Vapor Deposition	Radio Frequency-Plasma Enhanced Chemical Vapor Deposition	Molecular Beam Epitaxy

5.5 Conclusion

In conclusion, the fabricated memristive crossbar array on large-area of 3-inch exhibits excellent resistive switching properties with remarkable stability, repeatability and reproducibility in the resistive switching phenomena. Moreover, the fabricated devices show a marginal variation in V_{SET} and V_{RESET} in case of D2D. The fabricated devices also show low D2D variability in V_{SET} (2.64%) and V_{RESET} (10.13%) and ultralow C2C variability in V_{SET} (0.2%) and V_{RESET} (1.07%). Further, the fabricated memristive devices in the MCA also show a minimum level (2%) of overall variations in the values of C_V both for V_{SET} and V_{RESET} for varied levels of

I_{CC}, V_A and PW. This is encouraging for the practical application of the large-area MCA. Furthermore, the feasible fabrication process via DIBS system also leads to the fabrication of high-density crossbar array with low-cost, and scalable manufacturing possibilities for the next-generation resistive memory devices.

5.6 References

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Chapter 6

Read/Write Operation in Fabricated MCA Structure

6.1 Introduction

RRAM or memristive devices are the most promising future candidates for the next generation non-volatile memories not only due to its low power consumption, high switching speed, easy fabrication and excellent reliability but also its offer the ultimate nanometer level (< 10 nm) scaling which is more desirable for high-density crossbar array architectures [1]. However, due to high-density and compact crossbar array size the undesirable sneak current can arise from nearby unselected devices which is further affected the read/write margins and restricting the development of the large size of the crossbar array [2]. In the case of unipolar memristive devices, the sneak current problem can be minimized or neglected by connecting a diode in series with memristive device which acts as a selector device and this configuration is known as one diode-one resistor (1D1R) [3-4]. However, one directional operation of the diodes is not applicable for the bipolar memristive devices as it is inherently more stable. Further, complementary resistive switching (CRS) has also been proposed in which two bipolar resistive switching elements are connected in an anti-series configuration to suppress the sneak current [4-7], but CRS features have a destructive read problem.

Recently, a one selector-one resistor (1S1R) memory configuration has been proposed in which memory cell structure has one non-linear bipolar selector and one bipolar resistive switching element [8-10]. Several pull-up read/write schemes such as one bit line pull up (OBPU), all bit line pull up (ABPU) and partial bit line pull up (PBPU) have been utilized in the 1S1R memory configuration [11-13]. In the case of OBPU, the maximum size of a single crossbar array is estimated to be 10 Mb with at least a 10% read margin [14]. However, the aforementioned estimation may be too optimistic without considering line resistance, which cannot be neglected in the case of large crossbar arrays. Further, the read margin can be

improved by utilizing an ABPU scheme in a crossbar array with linear [13] and non-linear [15] cell resistances. The ABPU scheme also suggests that the optimization of the read scheme may play an important role in the read margins of the 1S1R configuration of the crossbar array with highly non-linear cell resistance. Furthermore, a PBPU scheme is useful to optimize the total power consumption during random read access. If the multiple or all bit lines are pulled up in memristive crossbar array, these are considered under PBPU and ABPU schemes.

Moreover, ABPU scheme substantially increased the maximum array size as compared to OBPU scheme while PBPU shows a moderate improvement in the read margin as compared to OBPU. Hence, an appropriate number of additional pull-up bit lines can be determined for the desired size of crossbar array depending on the application. The ABPU scheme can also be applicable for a large size crossbar array of 16 Mb in comparison to the OBPU scheme even when the line resistance is not negligible because the effective resistance at the sneak current path is substantially less sensitive to the array size.

6.2 One Bit line Pull Up (OBPU) Scheme

Figure 6.1 shows the crossbar array structure and equivalent circuit of 1S1R configuration by utilizing OBPU. The resistance of the non-linear resistive switching elements as a function of voltage is denoted by R_{sneak} and defined by the equation (1) as given below [11, 16-17]:

$$R_{\text{sneak}} = \frac{R_{\text{LRS}}^{\text{sneak}}(V_1)}{N-1} + \frac{R_{\text{LRS}}^{\text{sneak}}(V_2)}{(N-1)^2} + \frac{R_{\text{LRS}}^{\text{sneak}}(V_3)}{N-1} \quad (1)$$

The effective resistance values for HRS and LRS are defined by equations (2) and (3), respectively.

$$R_{\text{HRS}} = \frac{R_{\text{HRS}}^{\text{select}} \times R_{\text{sneak}}}{R_{\text{HRS}}^{\text{select}} + R_{\text{sneak}}} \quad (2)$$

$$R_{\text{LRS}} = \frac{R_{\text{LRS}}^{\text{select}} \times R_{\text{sneak}}}{R_{\text{LRS}}^{\text{select}} + R_{\text{sneak}}} \quad (3)$$

The resulting measurable normalized read voltage margin (ΔV) is given by equation (4):

$$\frac{\Delta V}{V_{\mathrm{pu}}} = \frac{V_{\mathrm{out,\ HRS}}}{V_{\mathrm{pu}}} - \frac{V_{\mathrm{out,\ LRS}}}{V_{\mathrm{pu}}} = \frac{R_{\mathrm{pu}}}{R_{\mathrm{HRS}}+R_{\mathrm{pu}}} - \frac{R_{\mathrm{pu}}}{R_{\mathrm{LRS}}+R_{\mathrm{pu}}} \quad (4)$$

where, the R_{select}, R_{sneak} and R_{pu} represent the resistance of selected cell, sneak path and connective resistance in measured system, respectively. The read margin decreased as increment in the crossbar line number (N) for both 1R and 1S1R devices. Therefore, the upper values of N with at least 10% read margin for general memristive and self-selective memristive devices.

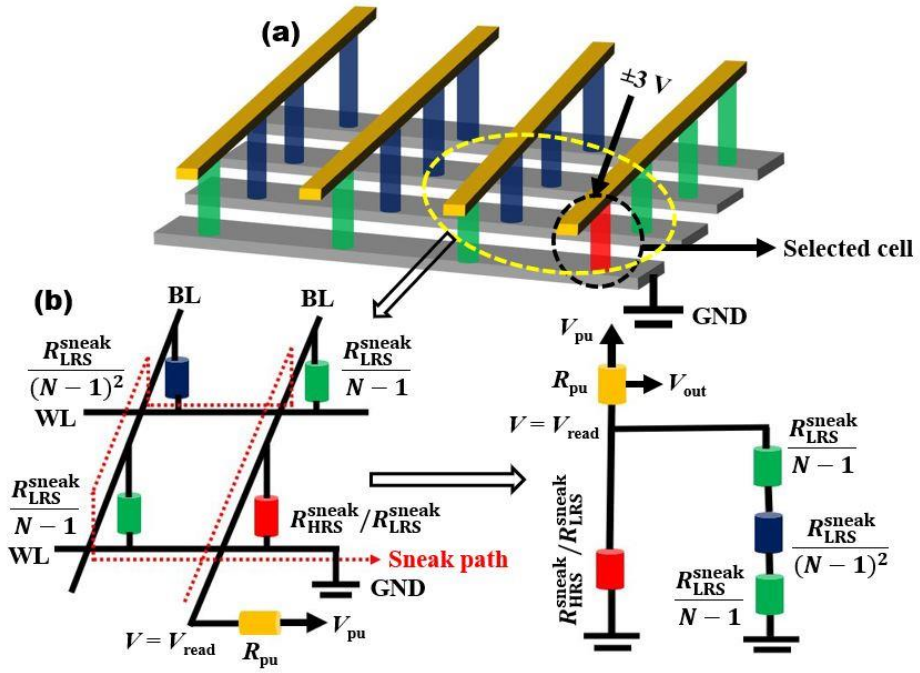

Figure 6.1: (a) A schematic of N × N crossbar arrays and (b) Corresponding equivalent circuit of crossbar arrays using one bit-line and pull-up read scheme, with which the red dotted line denotes the sneak path. The misreading current path (sneak path) in N × N crossbar arrays occurs where all bits are at LRS except the red cell is selected. The green regions are parallel resistor networks, namely bits on selected bit lines (BLs) and bits on selected word lines (WLs). The blue regions are bits on unselected WLs and BLs.

6.3 All Bit line Pull Up (ABPU) Scheme

For the enhancement in the read margin, ABPU scheme is utilized. Figure 6.2 shows the equivalent circuit diagram of a 1S1R non-linear memristive crossbar array under the ABPU scheme. In the case of ABPU scheme, at

the additional pull-up bit lines, V_3 is significantly higher as compared to V_1 and V_2 as described in equation (1) in the section 6.2. Whenever, a non-linearity factor (α) is greater than 1 i.e., α >1, the sneak path resistance is significantly higher than the resistance (either LRS or HRS) of the selected device [18]. Therefore, the read margin is effectively improved in ABPU by utilizing 1S1R cells. The mathematical formulations to calculate various resistance such as R_{sneak}, R_{LRS}, R_{HRS} and R_{pu} are mentioned in the section 6.2.

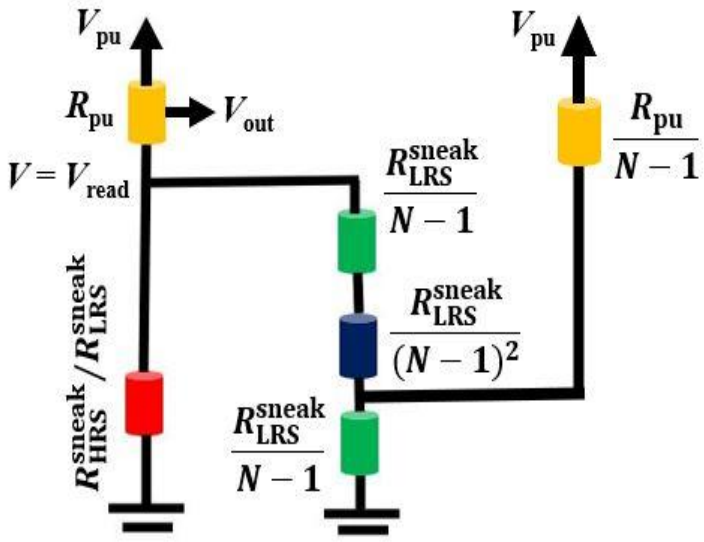

Figure 6.2: Equivalent circuit of the nonlinear 1S1R crossbar array under ABPU scheme.

6.4 Partial Bit line Pull Up (PBPU) Scheme

In this section, the additional practical considerations of the read margin are discussed which include the selection of V_{pu} and R_{pu}, and an alternative PBPU scheme. The selected value of V_{pu} can affect the non-linearity factor (α) which further affects the read margin. Theoretically, the optimized values of V_{pu} can be calculated numerically according to the non-linear characteristic of the 1S1R memristive cell [18]. However, the upper limit of V_{pu} is dependent on device switching voltage to prevent any bit from reading disturb during a potential full V_{pu} drop. Moreover, the optimized value of R_{pu} is preferable as compared to fix value as it can maximize the read margin. Considering the aforementioned discussion, PBPU is

examined with nearly 100% of the pull-up bit lines. Therefore, a suitable number of additional pull-up bit lines can be calculated for the desired array size as per the required application. Among all these schemes, ABPU scheme is extremely efficient to the simultaneous readout of the all-stored bits on the same word line as it may consume low power during operation.

6.5 Implementation of OBPU Read/Write Scheme on Fabricated MCA

6.5.1 Implementation of Read/Write Scheme on (4×4) MCA Structure

Section 6.2 describes the OBPU read scheme on memristive crossbar array. As observed in the integrated selector-based functioning of the crossbar array as in Figure 6.3(a), the individual memory cell has a different conductance state either "ON" or "OFF" depends on the programming applied bias condition which is similar to a one bit-line pull up (OBPU) scheme [19]. In this OBPU scheme, the applied voltage bias on the selected bit line is ±3 V, and the selected device in the array is either in LRS or HRS depend on the applied bias polarity. As shown by the device current-based color mapping in Figure 6.3(b), the accessibility of measurement data of a (4×4) 1S1R crossbar array is displayed in the worst-case scenario. One can easily extend the results to a multiple ($N\times N$) crossbar by integrating the additional peripheral circuits with the memory array [19-20]. Figure 6.3(c) depicts the results of a readout measurement to addressing tests based on the current of the LRS ("1") and the HRS ("0") with a (4×4) image representing the word "HNRG". The minor fluctuations observed in HRS and LRS can be further minimized by refining the fabrication processes [21-22]. The results evidently confirm that the GZO/Y_2O_3/Al crossbar array perform efficiently using 1S1R logic without electrical interference by integrating selector line with each memory cell [23].

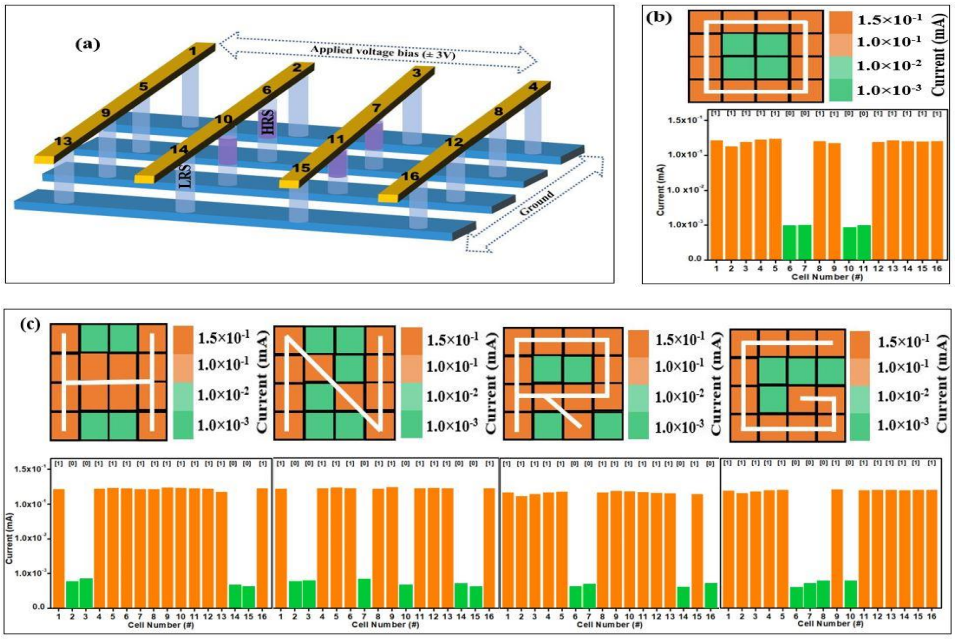

Figure 6.3: (a) Schematic of the crossbar memory array in a reading process, (b) Current histogram of a (4×4) 1S-1R crossbar-structured memory and the corresponding color map under the worst-case scenario, (c) Readout measurement of the addressing test result of the (4×4) GZO/Y_2O_3/Al crossbar array following 1S1R logic expressing the current histograms representing the word "HNRG".

6.5.2 Implementation of Read/Write Scheme on (8×8) MCA Structure

To investigate the writing capability of the fabricated MCA, a random (8×8) out of (30×25) of the MCA is selected. At the outset, all devices in the MCA are turned 'ON' by applying a constant input voltage of +1.3 V with a current in the range of 15-24 µA, as shown in Figure 6.4. Once the devices are in the 'ON' states, the input voltage amplitude is further increased to +2.1 V for those devices only which are required for alphabet writing. Such devices at a higher voltage excitation exhibit larger range of current of 35-45 µA, as demonstrated in Figure 6.4. Following this technique, one can easily write any desired alphabets such as "HNRG", "IITI", "SUK", and "GNU", as shown in Figure 6.4. It should be noted here that the Y_2O_3 MCA is successfully used to write multiple alphabet patterns that exhibits the robustness of the fabricated MCA.

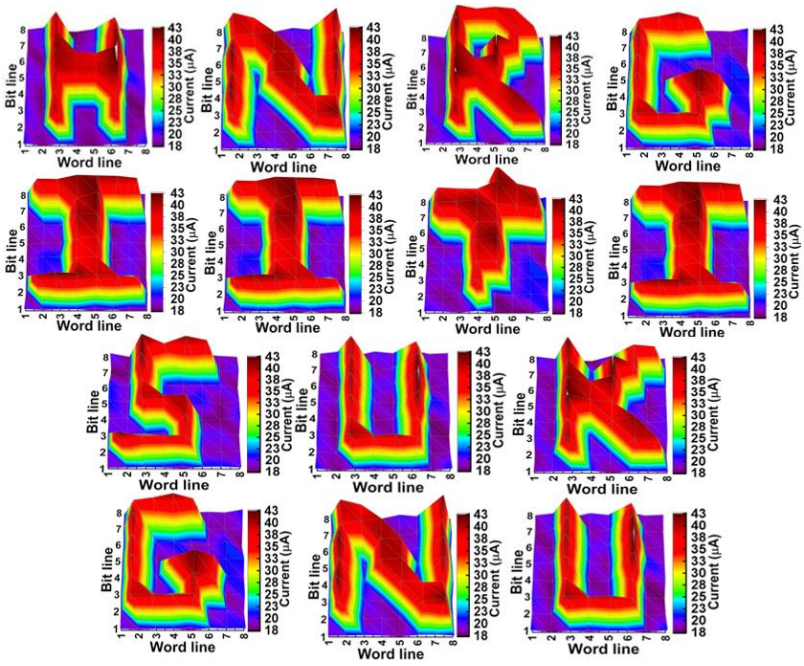

Figure 6.4: (8×8) MCA electric pulse writing for random alphabet.

6.6 Conclusion

In summary, this chapter describes the read/write schemes which have been utilized for the memristive crossbar array. The ABPU scheme is efficiently increased the array size as compared to OBPU scheme while PBPU is more useful to improve the read margin as compared to OBPU. Therefore, an appropriate number of additional pull-up bit lines can be determined for the desired size of crossbar array depending on the application. We have also implemented the OBPU read scheme on the DIBS grown (4×4) crossbar array and by utilizing current mapping method, word "HNRG" has been demonstrated. Furthermore, the writing of random alphabets has also been performed by considering multilevel current programming functionality of the selected (8×8) MCA structure and realized the multiple word such as "HNRG", "IITI", "SUK", and "GNU".

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Chapter 7

Conclusion and Future Perspective

Nowadays, semiconductor memories are an essential part of in-memory computation. As per the desirable requirement, various computing systems are required as per their abilities in the semiconductor memory functionality. Hence, we need to find an optimized solution as per our desirable task. From the last decade, a new non-volatile memory (NVM) prototype is discovered which can be utilized as a synapse and show the similar functionalities as analogues to the human brain. Several two terminals' devices efficiently show the resistive switching behavior in which their resistance is changed between two stable states i.e., LRS and HRS and the devices can remember the new resistance. These devices are known as RRAM which further can be considered in the broad category of memristive systems. The memristive devices behave like a tiny analog memory which forms a crosspoint junctions of the electrodes separated by the resistive switching materials. Further, memristive devices are more promising to be a high-density, energy efficient, simple structure, low cost, easy fabrication process and fast-switching memories. However, it is hard to say that the memristive device will be capable to replace the current memory technology completely.

In this work, we have proposed two analytical models and explored the crossbar array architecture of yttria-based memristive devices which are developed by the DIBS system and DC-magnetron sputtering. The proposed analytical models are efficiently emulated the various neuromorphic characteristics such as synaptic learning, synaptic plasticity functionality i.e., potentiation and depression, short-term memory (STM) and long-term memory (LTM). The 3D physical electro-thermal modeling further revealed the resistive switching performance of the nanoscale Y_2O_3-based memristor by considering the internal Joule heating and non-uniform distribution of electric field. The physical modeling also effectively shown the effect of device switching speed over the device switching parameters

(V_{SET} and V_{RESET}), and synaptic leaning behavior in terms of potentiation and depression processes. Further, the DIBS system offers numerous advantages such as it produces high-quality thin films with reasonably better compositional stoichiometry, small surface roughness, good adhesion to the substrate even at room temperature deposition and large-area scale electronic device fabrication. After the successful fabrication of crossbar array structure of the memristive devices, we have carried out several desirable experiments on the fabricated devices such as resistive switching response which is also termed as current-voltage measurement, optical microscopy measurement, FE-SEM, HR-TEM, and C-AFM. The performed experiments help us to understand the geometry of fabricated device structure in crossbar array, surface morphology of the deposited thin film, interfacial study, and mechanism and behavior of the memristive device. In the resistive switching responses, we have achieved consistent switching response in the multiple cycles with better repeatability, reproducibility, and have also achieved low D2D (2.64% in V_{SET}) and ultralow C2C (0.4% in V_{SET}) coefficient of variabilities (C_V) in the device switching voltages i.e., V_{SET} and V_{RESET}. Moreover, the devices in the crossbar array show better endurance i.e., 7.5×10^5 (0.7 million) cycles and good retention time i.e., 2.5×10^5 s with better current 'ON' and 'OFF' ratio. Furthermore, the device production yield in the crossbar array structure is > 92.50% with stable resistive switching response. However, the device production yield in the crossbar array can be further improved to precise control over contaminations during fabrication process and by utilization of the cleanroom environment.

To the best of the author's knowledge, the analytical modeling, fabrication of yttria-based memristive crossbar array by utilizing DIBS system and its detailed electrical and structural analysis have not been reported to date. Therefore, the presented study on yttria-based memristive crossbar array and corresponding relation with electrical, optical, elemental, and structural properties are impressive which can further lead to the development of compact high-density memristive chips.

7.1 Conclusions

The primary outcomes of this thesis are outlined as follows:

1. The first proposed analytical model of the memristive devices which is based on the Yakopcic model shows the good value of MED i.e., ~20.10% with respect to the experimental reported data in term of neuromorphic characteristics while the Yakopcic model shows ~36.80% MED. Hence, our proposed model shows ~16.66% better MED value as compared to the Yakopcic model with better non-linearity in the resistive switching response at the device boundaries. Moreover, the proposed analytical model successfully depicted the various memristive device characteristics such as learning behavior, and synaptic plasticity which are analogous to the human brain functionalities.

2. The second proposed analytical model is the parallel connection of the memristive device and rectifies (bunch of diodes). The proposed analytical model shows the remarkable accuracy with least values of MED i.e., ~4.44% in the case of Y_2O_3 and ~4.5% in the case of WO_3-based memristive devices in terms of neuromorphic characteristics. Further, the proposed model is also emulated the realistic memristive device behavior as it has ideal diode equation in its current-voltage relationship. Moreover, the proposed analytical model has better controllability over its resistive switching response due to the involvement of the newly piecewise window function.

3. The 3D physical electro-thermal modeling of nanoscale Y_2O_3-based memristor devices has been performed by utilizing combined software package of COMSOL Multiphysics and MATLAB. The discussed physical modeling is based on the minimization of free energy of the utilized materials at certain applied voltage. The simulated memristor device structure exhibits a stable pinched hysteresis loop in the resistive switching (RS) response in multiple switching cycles by considering internal Joule heating and non-uniform distribution of electric field. The RS responses show low values of coefficient of variability (C_V) i.e., 17.36% and 17.09%

in SET and RESET voltages, respectively, during C2C variations. The impact of V_{RR} on the device characteristics such as switching response and synaptic plasticity behavior of the device is also successfully investigated. Moreover, the performed simulation study significantly depicted the impact of oxide layer thickness on the switching voltages in the nanoscale device which further open the new way to develop nanoscale device to enable low power computation.

4. We have fabricated GZO/Y_2O_3/Al-based memristive crossbar array of (15×12) and (30×25) by utilizing DIBS and DC-magnetron sputtering through metal shadow mask technique. During the crossbar array fabrication, polycrystalline Y_2O_3 is used as an insulating layer instead of SiO_2 as it is provided better surface smoothness and roughness because of lower lattice mismatched (α_{Y2O3} = 10.60 Å; $2\alpha_{Si}$ = 10.86 Å) with Si substrate and it is grown at 100 °C substrate temperature and pure Ar environment in the assist ion source of the DIBS system.

5. The low resistive GZO is deposited on the insulating layer which acts as a bottom electrode and also provides the higher interfacial resistance which further helps us to fabricate the highly stable resistive switching memories with better cyclability as compared to Al metal. For the resistive switching medium, amorphous Y_2O_3 is used and it is deposited at 300 °C substrate temperature and Ar to O_2 ratio is 2:3 in the assist ion source of the DIBS system which shows better resistive switching response with Al as a top electrode.

6. Al forms the Schottky junction with yttria which plays an important role in the shape and size of the resistive switching response of the fabricated device. The bottom i.e., GZO/Y_2O_3 and top i.e., Y_2O_3/Al interfaces play a significant role in the bipolar resistive switching response of the fabricated devices in the crossbar array.

7. Our optical microscopy results reveal that the fabricated crossbar array structure is perfectly aligned to form crosspoint structure which is more desirable in the case of the crossbar memory array. FE-SEM and HR-TEM

analysis are confirmed that the deposited switching oxide layer has compact grain size with uniform structure and all device interfaces such as Si/Y_2O_3 (IL), Y_2O_3 (IL)/GZO, (BE) GZO/Y_2O_3 (SL) and Y_2O_3 (SL)/Al are clearly depicted separately which further confirm the better and smooth thin film deposition via DIBS system. Moreover, the C-AFM analysis reveals that the switching mechanism is interfacial dominated as no conductive filaments are formed inside the resistive switching medium which is also confirmed by the current level in the C-AFM mapping.

8. Our fabricated memristive devices in the crossbar array show excellent resistive switching characteristics with better repeatability and reproducibility, high ON/OFF current ratio, long endurance cycles (0.7 million) and good retention characteristics up to 2.5×10^5 s. We have also achieved high device production yield i.e., ~92.67% in the crossbar array size of (30×25).

9. The devices in the memristive crossbar array show the low D2D (2.64% in V_{SET} and 11.36% in V_{RESET}) and ultralow C2C (0.4% in V_{SET} and 1.07% in V_{RESET}) coefficient of variabilities (C_V) in the device switching voltages i.e., V_{SET} and V_{RESET}.

10. We have also experimentally investigated the impact of various electrical parameters such as compliance current (I_{CC}), applied input voltage and pulse width on C_V of V_{SET} and V_{RESET} of the devices in the fabricated memristive crossbar array. The obtained results show that the devices can be efficiently switched under the 10 ms and 100 ms pulse width but the values of C_V in V_{SET} and V_{RESET} are comparatively lower in the case of 100 ms which may be attributed due to the large device size. The overall variations in the C_V of V_{SET} and V_{RESET} due to the I_{CC}, applied voltages and pulse width are not much higher and can be easily covered within the range of 2% which is further more favorable for the high stability of the fabricated crossbar array.

11. The fabricated memristive crossbar array is also capable to perform integrated selector-based functioning in which individual memory cell has

a different conductance state under ‘ON’ and ‘OFF’ depending upon the programming applied voltages similar to a one bit-line pull up (OBPU) scheme. Based on the device current-based color mapping, the accessibility of measurement data of a (4×4) 1S-1R crossbar array is displayed the word “HNRG” in the worst-case scenario where current of the LRS (“1”) and the HRS (“0”) in the (4×4) crossbar array. Furthermore, the multilevel current programming functionality is enabled the writing capability of random alphabets by selecting (8×8) MCA structure and realized the multiple word such as “HNRG”, “IITI”, “SUK”, and “GNU”.

7.2 Future Scope

We have fabricated an electroforming free, Y_2O_3-based memristive crossbar arrays size of (15×12) and (30×25) with high endurance, stable, repeatable and reproducible switching response, good retention, high device production yield, low D2D and ultralow C2C variabilities. The resistive switching response of the fabricated crossbar array devices is interfacial dominated which can be further affected by the switching oxide layer thickness and electrode combinations. Further, it is observed that the device area scaling is significantly affected the device current level as well as device switching speed which can be further played a viable role to fabricate nanoscopic level devices to build high-density memristive crossbar array with nanosecond switching speed. Future scope of our research is outlined below:

1. Improvement in the memory endurance and retention by doping in Y_2O_3 or using two-dimensional (2D) material layer as a heat sink to introduce bilayers concept in the switching layer.

2. The device density in the crossbar array can be further improved by utilizing lithography process to scale down the size of the memristive devices.

3. The energy efficient memristive crossbar array can be fabricated by utilizing device scaling at nanometer level.