CURRENT AND CAPACITANCE MODEL OF UNDERLAP DOUBLE GATE MOSFET FOR ULTRA LOW POWER APPLICATIONS

M.Tech. Thesis

By

VIVEK KUMAR TIWARI

DISCIPLINE OF ELECTRICAL ENGINEERING

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **CURRENT AND CAPACITANCE MODEL OF UNDERLAP DOUBLE GATE MOSFET FOR ULTRA LOW POWER APPLICATIONS** in the partial fulfillment of the requirements for the award of the degree of **MASTER OF TECHNOLOGY** and submitted in the **DISCIPLINE OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from Aug 2021 to June 2023 under the supervision of Prof. Abhinav Kranti, Professor, IIT Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Vivek Tiwari
06/06/23

Signature of the student with date
(VIVEK KUMAR TIWARI)

This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

06/06/2023

Signature of the Supervisor of
M.Tech. (with date)
(Prof. Abhinav Kranti)

VIVEK KUMAR TIWARI has successfully given his/her M.Tech. Oral Examination held on **12 May, 2023** .

Signature(s) of Supervisor(s) of M.Tech. thesis
Date: 06/06/2023

Convener, DPGC
Date:

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Date:

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Thank you.

Vivek Kumar Tiwari

Dedicated to my family and my friends

Abstract

Current and Capacitance Model of Underlap Double Gate MOSFET for Ultra Low Power Applications

Ultra low power (ULP) CMOS circuits are gaining wide attention in recent times due to the growing demand for energy-harvesting devices. In ULP applications, supply voltage is limited to the threshold voltage of the transistor i.e. the transistor essentially operates in the subthreshold region. Thus, in ULP applications, the performance and speed of the circuit strongly depend on the subthreshold characteristics, extent of short channel effects (SCEs) and parasitic capacitance of the device. To overcome the SCEs, multi-gate transistors like double gate (DG) can be used, which can effectively suppress SCEs. However, a larger number of gates in DG MOSFET leads to a higher contribution of parasitic capacitance in the overall gate capacitance. This affects the circuit delay and operating speed of the ULP circuit. To overcome these challenges, DG MOSFET with underlap regions can be used. A larger separation between the heavily doped source/drain and the gate edge due to the underlap region significantly reduces parasitic capacitance. In addition, incorporating underlap in DG MOSFETs enhances short channel immunity by increasing the effective gate length.

This thesis presents the development of a subthreshold analytical model for channel potential and drain current. The proposed model, consisting of five regions, offers enhanced accuracy by considering the bias-dependent boundaries. Additionally, a comprehensive investigation of the channel and parasitic capacitance in DG underlap MOSFETs has been conducted, indicating the efficacy of larger underlap in reducing parasitic capacitance. Furthermore, this study highlights several potential advantages of larger underlap, including improved subthreshold swing, off current, and threshold voltage. These findings are supported by the analytical model and TCAD simulations, providing valuable insights into the benefits of incorporating larger underlap in MOSFET designs.

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NOMENCLATURE

S_{swing}	*Subthreshold swing*	*mV/dec*
V_{th}	*Threshold voltage*	*V*
I_{ON}/ I_{OFF}	*On-current to off-current ratio*	*Unitless*
I_{ON}	*On-current*	*A*
I_{OFF}	*Off-current*	*A*
L_g	*Transistor gate length*	*nm*
L_{un}	*Underlap length*	*nm*
L_{eff}	*Effective channel length*	*nm*
V_{gs}	*Gate voltage*	*V*
V_{ds}	*Drain voltage*	*V*
I_{ds}	*Drain current*	*A*
C_{gg}	*Gate capacitance*	F/nm^2
n_e	*Concentration of electrons*	nm^{-3}
t_{si}	*Silicon film thickness*	*nm*
t_{ox}	*Gate oxide thickness*	*nm*
N_A	*Acceptor dopant concentration*	nm^{-3}
R_I	*Region I*	*Unitless*
R_{II}	*Region II*	*Unitless*
R_{III}	*Region III*	*Unitless*
R_{IV}	*Region IV*	*Unitless*
R_V	*Region V*	*Unitless*
D_S	*Extension of depletion width towards source*	*nm*
D_D	*Extension of depletion width towards drain*	*nm*
Ψ_I	*Potential of region I*	*V*
q	*Electronic charge*	*C*
ε_{si}	*Permittivity of silicon*	*F/nm*

n_i	*Intrinsic carrier concentration*	nm^{-3}
V_f	*Quasi fermi potential*	V
k	*Boltzmann constant*	JK^{-1}
T	*Absolute Temperature*	K
V_{bi}	*Built-in potential*	V
K_1	*Intermediate constant*	m^{-2}
V_T	*Thermal voltage*	V
ε_{si}	*Permittivity of silicon*	F/nm
ε_{ox}	*Permittivity of gate oxide*	F/nm
M	*Unknown coefficient*	V
N	*Unknown coefficient*	V
Ψ_{II}	*Potential of region II*	V
E_S	*Electrical field at* $x = D_S$	V/nm
V_S	*Potential field at* $x = D_S$	V
Ψ_{III}	*Potential of region III*	V
$\Psi 1_{III}$	*Notation use for representation of 1D potential*	V
$\Psi 2_{III}$	*Notation use for representation of 2D potential*	V
C_{ox}	*Capacitance of oxide*	F/nm^2
r	*Silicon film capacitance to oxide capacitance ratio*	*Unitless*
A	*Unknown coefficient*	V
B	*Unknown coefficient*	V
λ	*Natural length of scaling*	nm^{-1}
P	*Unknown coefficient*	V
Q	*Unknown coefficient*	V
E_D	*Electrical field at* $x = L_g + D_D$	V/nm
Ψ_{IV}	*Potential of region IV*	V
K_2	*Intermediate constant*	m^{-1}
V_D	*Potential at* $x = L_g + D_D$	V
μ_n	*Mobility of electrons*	$m^2V^{-1}s^{-1}$

H_1	*Notation use to represent arbitrary function dependent on x, y and potential of region II*	m^{-3}
H_2	*Notation use to represent arbitrary function dependent on x, y and potential of region III*	m^{-3}
H_3	*Notation use to represent arbitrary function dependent on x, y and potential of region IV*	m^{-3}
ϕ_C	*Potential at the centre of silicon film*	V
N_D	*Donor doping concentration*	nm^{-3}
C_{if}	*Inner fringing capacitance*	F/nm^2
C_{gc}	*Gate to channel capacitance*	F/nm^2
C_{Para}	*Parasitic capacitance*	F/nm^2
C_{Side}	*Sidewall capacitance*	F/nm^2
C_{of}	*Outer fringing capacitance*	F/nm^2
C_{ov}	*Overlap capacitance*	F/nm^2
Q_{Mobile}	*Mobile charge density*	nm^{-3}
ϕ_S	*Potential at surface of film*	V

ACRONYMS

CMOS	*Complementary Metal Oxide Semiconductor*
MOSFET	*Metal Oxide Semiconductor field transistor*
SCE	*Short channel effects*
BTBT	*Band-to-band tunneling*
SOI	*Silicon-on-Insulator*
BOX	*Buried oxide*
3D	*Three dimensional*
ULP	*Ultra low power*
I_{OFF}	*Off current*
PDSOI	*Partially depleted Silicon-on-Insulator*
FDSOI	*Fully depleted Silicon-on-Insulator*
UTB	*Ultra thin body*
UTBB	*Ultra thin body BOX*
GP	*Ground plane*
DIBL	*Drain induced barrier lowering*
n^+	*Heavily doped donor type*
p^-	*Lightly doped acceptor type*
RDF	*Random Dopant Fluctuation*
DG	*Double gate*
TCAD	*Technology Computer-Aided Design*
FinFET	*Fin field effect transistor*
2D	*Two dimensional*
MOS	*Metal oxide semiconductor*

Chapter 1

Introduction

1.1 Motivation

The semiconductor industry has seen tremendous growth over the last few decades due to innovations at material, device, and circuit level since the development of the transistor in 1947 [1],[2]. This remarkable growth is driven by various factors, including technological advancements, and increasing demand in industries

Back in 1965, Gordon Moore made a prediction that famously known as Moore's Law. He foresaw that the number of transistors on a microchip would double approximately every two years [4],[5]. This exponential growth in transistor density has been made possible primarily through the advancements in Complementary Metal Oxide Semiconductor (CMOS) scaling. The semiconductor industry has relied on CMOS scaling as a crucial factor in keeping up with and fulfilling Moore's Law projections. There are various types of scaling theories proposed in the literature, along with their advantages and disadvantages [6]-[9]. To increase speed and circuit density, downsizing of CMOS transistors is essential. However, scaling of bulk Metal Oxide Semiconductor field effect transistor (MOSFET) beyond the 45 nm node faces various challenges due to several fundamental limits [10]-[12]. These limits include short channel effects (SCEs), quantum mechanical tunneling current, and random dopant fluctuations [13]-[15]. These effects cause subthreshold swing (S_{swing}) degradation, Threshold voltage (V_{th}) degradation with length scaling, strong impact of source/drain field on the channel, and band-to-band tunneling (BTBT) which can degrade the off-current [16]-[19]. Consequently, the on-to-off current ratio (I_{ON}/I_{OFF}) of a transistor also decreases leading to degradation in the electrical characteristics of transistors, where I_{ON} and I_{OFF} are the on current and off current, respectively. These factors make it challenging to maintain the required device performance while

lowering power consumption through the downscaling of bulk MOSFET [20].

1.2 Advancement of CMOS Technology

1.2.1 Bulk MOSFET

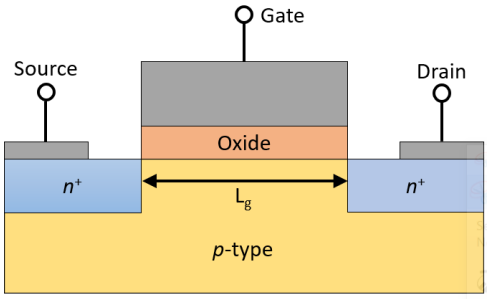

Fig. 1.1 Schematic of bulk MOSFET.

Initially, silicon wafers measuring approximately 800 micrometers in thickness were used for the production of bulk MOSFETs (Fig. 1.1). Nevertheless, only the uppermost micrometer of the wafer was employed in the manufacturing process of transistors [21]. As MOSFET continues to be miniaturized in bulk CMOS technology, the transistor is also approaching its physical limits due to multiple factors [22] such as

- As device dimensions shrink, controlling subthreshold current becomes more challenging, which can be overcome by increasing the channel doping.
- High doping concentrations lead to higher junction capacitance, which limits circuit speed.
- High doping concentrations can also degrade surface mobility due to increased scattering.
- Increasing the doping also enhances the electric field which can lead to reliability concerns.
- Enhancing the doping can also lead to random dopant fluctuations and quantum confinement effects.

Therefore, to support further scaling, alternative device structures are essential [22].

1.2.2 Silicon-on-Insulator (SOI)

To balance the trade-off between SCEs and high parasitic capacitance while enabling scaling, it is necessary to reduce doping while still maintaining decent subthreshold behavior. This issue can be overcome by adopting Silicon-on-Insulator (SOI) technology [22]. In SOI technology, an additional oxide layer called buried oxide (BOX) at the bottom of the active region (Silicon) provides the isolation between the channel and substrate as shown in Fig. 1.2.

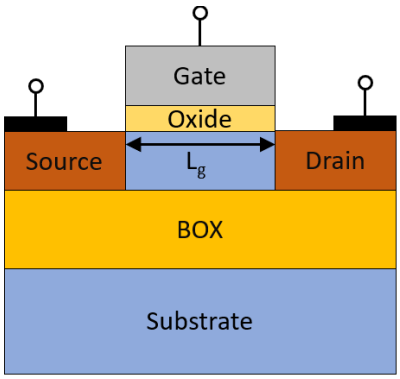

Fig. 1.2 Schematic of a Silicon-on-Insulator (SOI) MOSFET.

SOI MOSFET has several advantages as listed below [22]-[23].

- **Dielectric isolation:** SOI circuits are comprised of isolated device islands that are separated both horizontally from one another and vertically from the underlying substrate [24]. This prevents latch-up issues, reduces leakage current, reduces power consumption, and enhances circuit reliability.
- **Improved integrity:** SOI MOSFET structure demonstrates the capability to stack multiple layers of devices [25], consequently enhancing the potential for 3D integration.
- **Reduced fabrication steps:** Fabricating CMOS circuits on SOI technology offers advantages over bulk silicon. The streamlined procedure, which does not involve wells and inter-device trenches,

minimizes the necessary processing steps and enables greater design adaptability [27].

- **Mitigation of SCEs:** SCEs occur when source/drain electric field hinders the electrostatic controllability of the gate. In SOI devices, BOX layer limits the depletion width (in the vertical direction) [18], thereby enhancing gate controllability in undoped thin-film devices. Additionally, the field lines can penetrate the BOX before impacting the gated region leading to a decrease in gate controllability [28], [29]. However, this issue can be mitigated by utilizing an ultra-thin BOX [30], which terminates the field lines from source/drain to the substrate.
- **Low Voltage/Power operation:** SOI transistors enable low voltage/power operation [27], which is beneficial for ultra low power (ULP) applications. They exhibit significantly lower I_{OFF} than bulk MOSFET.
- **Enhanced reliability:** SOI devices have excellent tolerance to transient radiation effects [24],[28]. The reduction in device volume exposed to radiation-induced carrier generation leads to a substantial decrease in logic upsets.

These advantages make SOI technology appealing for various applications that require improved performance, reduced power consumption, and enhanced reliability.

Apart from the above-mentioned advantages, SOI technology comes with various limitations such as the floating body effect or kink effect, and self-heating [23], [30].

SOI MOSFET can further be classified into two categories.

- **Partially Depleted Silicon-on-Insulator (PDSOI) [30]:** In PDSOI MOSFET, the active silicon layer is not fully depleted of charge carriers (Fig. 1.3(a)). Instead, there are certain number of carriers present in the active layer. This can be achieved by controlling the thickness and doping of the active layer to achieve the desired electrical characteristics [30]. PD SOI technology offers several

advantages over traditional bulk Silicon designs, such as reduced power consumption, improved performance, and increased immunity to certain types of noise [30]. PDSOI is commonly used in applications where ULP consumption and high-speed performance are critical, such as mobile devices and high-performance computing.

- **Fully Depleted Silicon-on-Insulator (FDSOI) [32]:** In FDSOI MOSFET, the entire thickness of the silicon film, extending from the topmost surface to the BOX layer is depleted of majority carriers (electrons or holes) at zero bias (Fig. 1.3(b)).

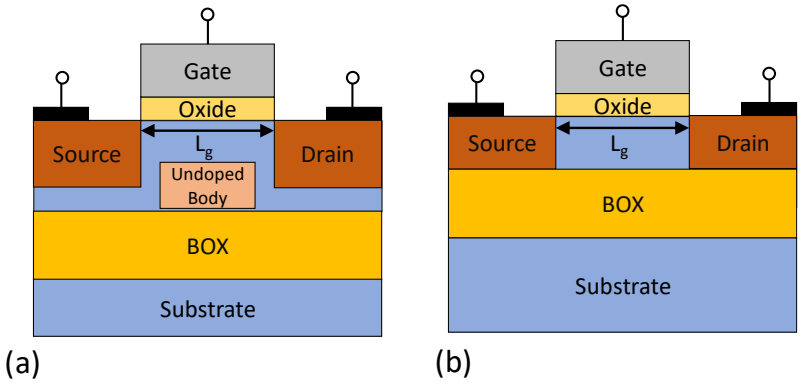

Fig. 1.3 Schematic representation of (a) PDSOI MOSFET and (b) FDSOI MOSFET.

In PDSOI MOSFET, impact ionization generated carriers (holes) are confined near the Si-BOX interface as there is no access to the substrate for allowing their escape. Consequently, these carriers cause an elevation in the body potential of the transistor, resulting in a decrease in the value of threshold voltage, which causes a sharp rise in drain current i.e. kink effect [23],[28],[30].

In the context of a thin film, FDSOI MOSFET shows a lower electric field near the drain compared to a PDSOI device. Consequently, the FDSOI device experiences reduced electron-hole pair generation. Additionally, unlike a PDSOI transistor, the source-to-body diode in an FDSOI MOSFET is inherently forward-biased due to the complete depletion of the film. This forward bias facilitates an easy

recombination of holes in the source region without requiring an increase in the body potential. These characteristics account for the absence of the kink effect observed in the FDSOI device [30].

FDSOI technology offers distinctive benefits, such as reduced junction capacitance, floating body effects, and enhanced subthreshold characteristics [33]. To further reduce SCEs in FDSOI technology, ultra thin body (UTB) or ultra thin body BOX (UTBB) SOI are the two alternative architectures [31].

Fig. 1.4(a) shows a UTB SOI device which is capable of being scaled down to gate length as short as 18 nm with a body thickness of 5 nm [33]. The implementation of an UTB structure in the design effectively mitigates the presence of leakage paths between source and drain regions. The electrostatic integrity of the transistor is enhanced in UTB devices, as the potential lines exhibit a predominantly flat profile [28]. Moreover, in FDSOI devices, the occurrence of SCEs can be mitigated by employing a thin BOX.

The introduction of ultra thin BOX (Fig 1.4(b)) enhances the horizontal coupling between source and drain through the substrate. This necessitates the inclusion of a heavily doped layer called the Ground Plane (GP) beneath the BOX to prevent lateral coupling to the substrate [22]. Another advantage of implementing the GP is that it redirects a significant portion of the field lines toward the GP, thereby mitigating horizontal coupling. However, it is important to note that the incorporation of GP leads to an increase in the body effect and capacitance, which can degrade the performance of the device [35]. The presence of GP helps in suppressing the depletion region beneath the BOX, leading to improved electrostatic control and a reduction in S_{swing}, drain induced barrier lowering (DIBL), and variability in V_{th}. Also, incorporating a GP offers the potential for V_{th} modulation through the addition of a contact for back gate biasing [36]-[38].

As the BOX thickness is further reduced, additional effects come into the picture [39] as follows:

1. Increased gate-to-gate coupling [39].
2. Parasitic capacitance is significantly increased. This can affect the speed, power consumption, and high-frequency performance.
3. The depletion region (in the substrate) can result in substrate current leakage, where current flows through the substrate instead of following the desired channel path. This leakage current can degrade device performance, increase power consumption, and affect circuit operation.

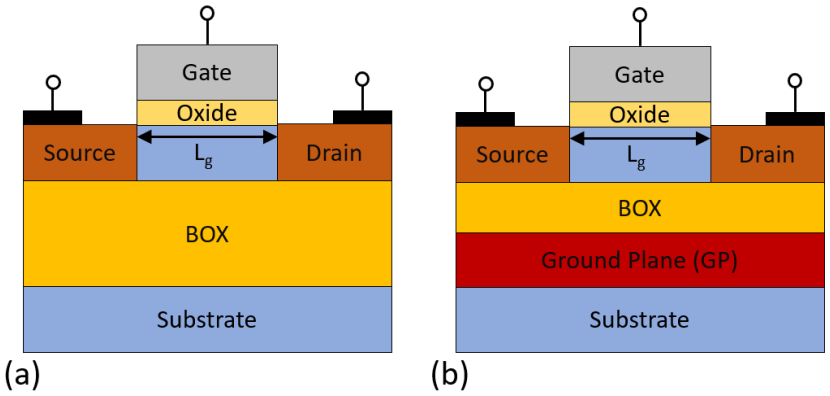

Fig. 1.4 Schematic representation of (a) Ultra thin body (UTB) and (b) Ultra thin body BOX (UTBB) FDSOI MOSFET.

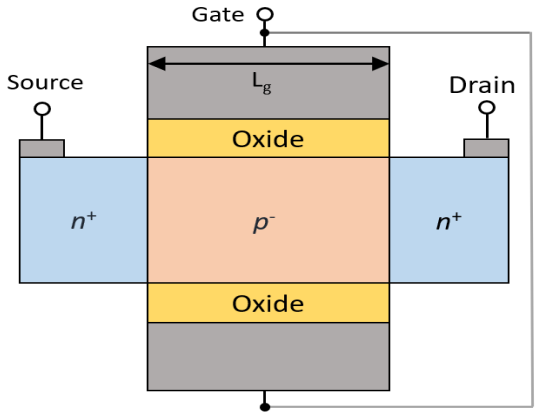

Fig. 1.5 Schematic diagram of a double gate (DG) MOSFET.

1.2.3 Multi-gate architecture

In comparison to SOI MOSFET, multi-gate MOSFETs exhibit improved scalability. This facilitates continued transistor miniaturization, enabling the development of smaller and more energy

efficient devices. Double gate (DG) MOSFET (Fig. 1.5) is a widely used multi-gate transistor configuration design, due to its advantages over traditional single-gate MOSFET [40]-[41]. Multi-gate MOSFETs address several issues encountered in single gate SOI transistors, particularly the adverse effects of SCEs. As transistors shrink in size, SCEs like DIBL and S_{swing} degradation become more prominent. The multi-gate structure mitigates these effects by improving electrostatic control, reducing leakage currents, and facilitating better scalability and continued miniaturization. Nevertheless, multi-gate MOSFETs present certain challenges, particularly in the fabrication process [42]-[44]. The precise alignment and patterning of multiple gates necessitate advanced lithography techniques and tighter manufacturing tolerances [43]. These complexities increase production costs and yield challenges, adding difficulty to the manufacturing process. Variability in device performance is another challenge associated with the multi-gate structure. Variations in gate length, thickness, and other parameters can impact the uniformity and performance of multi-gate MOSFETs. Such variations influence crucial transistor characteristics, including threshold voltage, leakage current, and switching speed [45]-[46]. Techniques like gate work-function engineering and strain engineering are employed to address these challenges and enhance device performance consistency. Additionally, multiple studies [47], [46] have shown that multiple-gate transistors suffer from Random Dopant Fluctuation (RDF) [47]-[48]. The challenges posed by RDF become more prominent as devices are scaled down to the nanoscale limit, where the discrete nature of doping leads to a limited number of atoms involved [49]-[51].

1.2.4 Double Gate (DG) MOSFET

DG SOI MOSFET shows a significant advancement in semiconductor technology compared to SOI MOSFET. While SOI MOSFET have played a crucial role in enhancing device performance and reducing power consumption, DG MOSFET offers even greater potential for further improving integrated circuits. DG MOSFET was

first proposed by Sekigawa in 1984 [36]. The presence of dual gate control in DG MOSFET (Fig. 1.5) significantly enhances the electrostatic integrity of the device [37].

In comparison to single-gate, UTB and UTBB MOSFET, DG MOSFET demonstrates greater electrostatic robustness as the control of the channel is facilitated by gates from both two sides, which enables an additional aspect of gate scalability [38]. In DG SOI transistors, the electric field generated by source/drain potentially impact the gated region. The relaxed body film thickness is particularly advantageous from the manufacturing perspective since the fabrication of ultra thin films poses significant technological challenges [32]. The enhanced scalability of DG devices with thin film makes them highly suitable for nanoscale regimes [52].

Overall, the advantages of DG MOSFET includes high immunity to SCEs scalability, reduced leakage currents, and compatibility with nanoscale existing technology. These advantages make DG MOSFET a promising choice for next-generation semiconductor devices. However, at the nanoscale dimension, the performance of DG MOSFET is hindered due to rise of SCEs, which can be overcome by adopting the underlap structures [53]-[54].

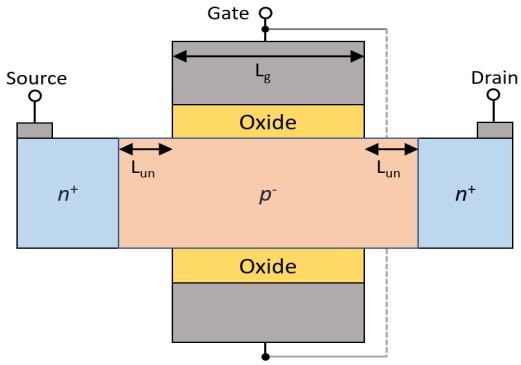

Fig. 1.6 Schematic representation of DG underlap MOSFET.

1.2.5 DG Underlap MOSFET

In underlap structure, an extension of channel doping beyond the gate edges (Fig. 1.6) results in extension of depletion region beyond gate

edges i.e. longer effective channel length, which is particularly beneficial for subthreshold or ultra low power operation. Additionally, peak electric field at the gate edge, and parasitic capacitance is also minimized.

1.4 Organization of the Thesis

Chapter 1 explores the significance of MOSFET device evolution. It examines the quest for improved performance, power efficiency, and integration capabilities necessitating the exploration of MOS technology.

Chapter 2 focuses on the growing dominance of SCEs in the nanoscale regime and their impact on device performance. It explores various SCEs and their consequences on MOSFET operation. The chapter also investigates the potential of DG underlap MOSFETs in improving device performance, particularly in ULP logic applications. Furthermore, it discusses the role of Technology Computer-Aided Design (TCAD) in modeling and simulating these advanced MOSFET structures.

Chapter 3 explores different modelling approaches for DG MOSFETs and focuses on the derivation of a semi-analytical model for electrostatic potential and subthreshold drain current**.** The chapter also highlights the validation of these models using TCAD simulations, serving as an essential tool, are employed for validating and enhancing the precision of the derived models.

Chapter 4 explores the various components of capacitance in DG underlap MOSFETs, focusing on the effects of underlap length on the device. Additionally, it introduces the idea of a piecewise model approach to effectively model the capacitance behavior of DG underlap MOSFETs**.**

Chapter 5 presents the conclusion of the conducted work and proposes the future scope of the research.

Chapter 2

Short Channel Effects in Nanoscale Transistors

2.1 Short Channel Effects

Short-channel effect (SCE) is an undesirable phenomenon that results from the sharing of electrical charges between the gate and the source/drain in the MOSFET [55]. This effect occurs when the depletion region, which is formed by the source/drain, extends towards the channel region of the transistor, causing a reduction in the effective channel length. Consequently, this diminishes the control that the gate has over the channel. As the dimensions of the device continue to shrink into the nanoscale range, the influence of the lateral field from the source/drain on the channel region becomes more pronounced. A reduction in gate controllability over the channel often results in degraded transistor performance which is termed as SCEs [56]. The performance of MOSFET is largely affected by SCEs that arise due to the above-mentioned reason. These effects include:

- **Drain induced barrier lowering (DIBL):** The conduction barrier primarily needs to be controlled by the vertical field i.e. gate bias (V_{gs}). As the drain voltage (V_{ds}) increases, a reduction in the source channel barrier is observed due to the enhancement in the lateral field. This results in an increase in leakage current due to the reduction in V_{th} of the transistor. As the transistor's lateral length shrinks down to nanoscale region, the impact of V_{gs} on the source channel barrier further increases which results in a comparatively higher reduction in V_{th} as compared to the longer channel devices. This causes the transistor to turn-on at lower V_{gs}. This is termed as DIBL effect in transistor [26],[57].
- **Velocity saturation:** In short channel devices electrical charge in the channel reaches its maximum velocity [58] due to enhanced lateral field. This velocity known as saturation velocity which impacts the current drive of a short-channel transistor [59].

- **Threshold voltage roll-off:** As the device dimension shrinks to the nanoscale region, a reduction in V_{th} is observed due to the enhancement in lateral field distribution in the channel region of the short channel transistor. The decrease in V_{th} is called as the threshold voltage roll-off [24],[48],[57],[60].

- **Punch-through effect:** The punch-through occurs when a reverse bias is applied to the drain of a MOSFET, leading to the extension of the depletion region. As a result, the two depletion regions from the drain and source regions merge, forming a single depletion region. This merging allows for the flow of leakage current, which eventually leads to the breakdown of the MOSFET [60].

- **Hot carrier injection:** When V_{gs} and V_{ds} reach sufficiently high levels, the electric field in the vicinity of the drain region triggers the generation of electron-hole pairs through impact ionization [62]. The injection of hot carriers into the gate dielectric can result in damage to its properties, affecting the overall performance and reliability of transistor [62].

- **Mobility degradation:** Short-channel transistor experiences reduced carrier mobility due to enhanced lateral electric field including impurities, surface roughness, and other imperfections. This reduction in mobility affects device performance, including lower drain current and slower switching speeds [63].

- **Subthreshold swing:** The performance of transistors in subthreshold region is heavily influenced by the control of V_{gs} over any changes in drain current. When the gate loses its control over the channel a wider gate bias interval is required to change the current by one decade. A subthreshold swing greater than 60 mV/decade at room temperature is indicative of higher I_{OFF} in the device [64].

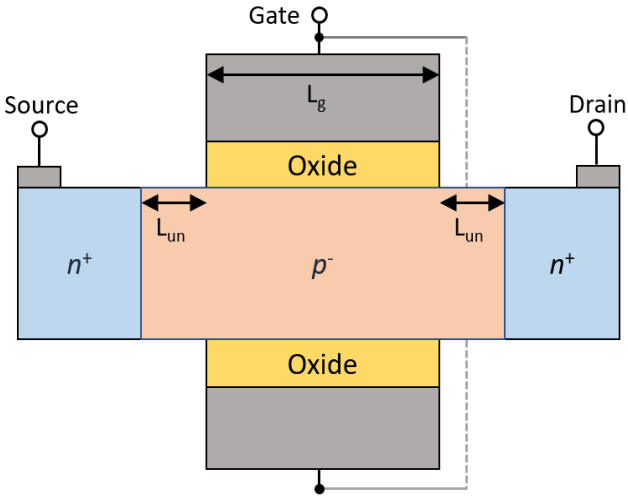

Fig. 2.1 Schematic diagram of DG underlap MOSFET.

2.2 Double Gate Underlap MOSFET

A multiple gate transistor such as planar double gate MOSFET (DG MOSFET) allows for better gate control due to front and top gates. The two gates strengthen the vertical (gate) electric field in comparison to the lateral (source/drain) field. However, at ultra-short channel lengths, the lateral field dominates over the vertical field, and SCEs degrade the performance of DG MOSFET. The technological options to limit SCEs are either to (i) move towards 3-dimensional architectures such as tri-gate, FinFET, nanowire, nanosheet, etc., [65]-[67] or (ii) adopt gate-source/drain underlap methodology [68]. Multi-gate MOSFET, even though exhibit immunity from SCEs, have limitations in terms of fabrication complexity and higher capacitance [43]. Underlap design in planar transistor topology allows for a longer channel length as the source/drain doping is maintained away from the gate edge [70]. The advantages of underlap design are as follows [68]-[77]:

- **Enhanced effective channel length (L_{eff})***:* Underlap MOSFET effectively increases the effective channel length (L_{eff}) as compared to traditional multi-gate MOSFET [69], [76], [77]**.** By intentionally positioning source/drain away from the gate (dual spacer process), the channel region exceeds the gate length of

the multi-gate transistor. This extension improves the control of current flow and reduces the impact of SCEs in the transistor. The extension of depletion in the subthreshold region can be shown in Fig. 2.2 through the electron concentration contour plot i.e. a lower electron concentration in the underlap region.

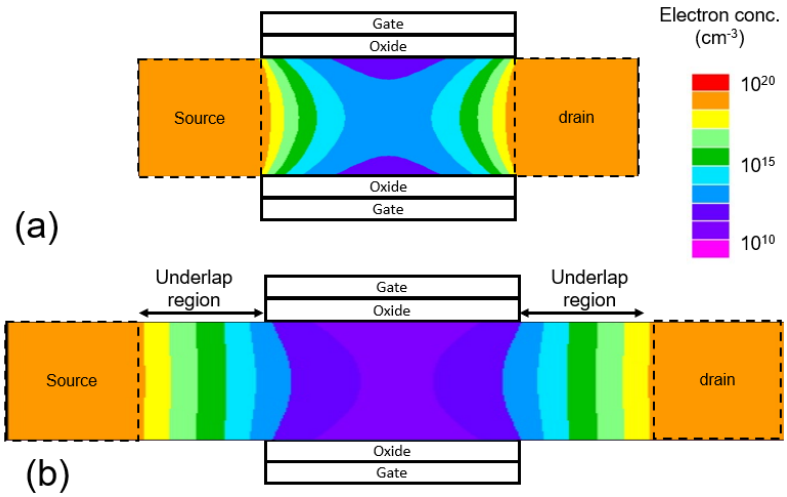

Fig. 2.2 Contour plot showing the variation of electron concentration in (a) DG MOSFET and (b) DG underlap MOSFET with underlap length of 12 nm. Parameters: gate voltage (V_{gs}) = drain voltage (V_{ds}) = 0 V, gate length (L_g) = 20 nm.

- **Better gate control:** The underlap configuration permits better control over the channel region by reducing the influence of drain region. This results in improved control over the V_{th} [77] and S_{swing}, which are critical parameters for transistor operation for low power applications. With enhanced gate control, underlap MOSFET achieve better transfer characteristics as compared to non-underlap device of the same gate length.

- **Improved subthreshold characteristics:** The deliberate underlap design reduces leakage currents and improves the I_{ON}/I_{OFF} [70], [71], [72], [78] provided on-current is considered around the threshold. This is particularly beneficial for achieving ultra low power (ULP) operation in applications where power consumption is a primary concern. Underlap MOSFET enables more efficient and power

conscious circuit design by reducing leakage current and enhancing energy efficiency.

- **Improved capacitance and delay**: Underlap MOSFET can reduce the inner fringing capacitance as the source/drain region are positioned away from the gate edge [70], [76]**.** For ULP applications, the inner fringing capacitance is a major component of the total capacitance. SCEs tend to enhance the parasitic capacitance in a MOSFET. Underlap methodology reduces the parasitic capacitance component and enhances the difference in capacitance values in the off- and on-states. A lower capacitance (off-state) can contribute to a lower delay [79].
- **Reduced tunneling current:** Gate underlap has an additional benefit of reducing direct tunneling as well as BTBT as the electric field is reduced [53].

Overall, underlap topology in planar DG MOSFET provides a viable solution to overcome SCEs, improve subthreshold characteristics, enable better gate control, enhance gate capacitance and lower delay. These advantages make underlap DG MOSFET a promising option for ULP applications.

2.3 Device Simulation with TCAD

The use of Technology Computer-Aided Design (TCAD) tools has revolutionized the semiconductor industry. TCAD provides a platform for accurately analysing device behaviour and optimizing designs, offering valuable insights to engineers and researchers prior to fabrication. Also, anomalous experimental observations can be evaluated and understood in-depth through TCAD.

One widely recognized TCAD tool is ATLAS from Silvaco [81]. ATLAS is a comprehensive simulation software that enables detailed simulation and analysis of various semiconductor devices, including MOSFETs, diodes, and bipolar transistors. It utilizes advanced algorithms and physical models to simulate the electrical behaviour of the above-mentioned devices under different operating

conditions. TCAD tool serves as a versatile framework for analyzing and optimizing device performance. It allows users to investigate the effects of process parameters, device geometries, material properties, and environmental conditions. This enables the identification of design limitations, optimization of device performance, and exploration of innovative device structures and materials. Through TCAD software, researchers can explore device characteristics such as current-voltage (*I*-*V*) and capacitance-voltage (*C*-*V*) characteristics, as well as transient responses. The software accounts for important physical phenomena like carrier transport, tunnelling, impact ionization, generation-recombination mechanism, field and concentration-dependent mobility, and quantum confinement effects, which ensure an accurate representation of device behaviour [81].

2.4 Analysis of DG Underlap MOSFET

In this section, an analysis of underlap DG MOSFET using TCAD tool is discussed. The focus of this study is to investigate the impact of underlap length (L_{un}) on the performance of DG devices with a fixed gate length (L_g) of 20 nm [81]. Additionally, a comparison is carried out between devices with different underlap lengths and those without any underlap.

The simulation results (Fig. 2.3(a)) reveal a significant impact of underlap length on the off-current of DG MOSFET. It is observed that I_{OFF} decreases by an order i.e. from 3.6 nA to 0.3 nA as the underlap length is varied from 0 to 12 nm. The L_{un} = 0 nm corresponds to an ideal MOSFET in which source/drain doping are positioned at the gate edge. The reduction in I_{OFF} is attributed to enhanced gate control achieved through underlap structure which reduces the lateral electric field and enhances the vertical electric field. In Fig. 2.3(b), it can be observed that DG MOSFET with underlap demonstrates a lower parasitic capacitance compared to the device without underlap (conventional transistor). This reduction in parasitic capacitance is due to the reduction in fringing capacitance.

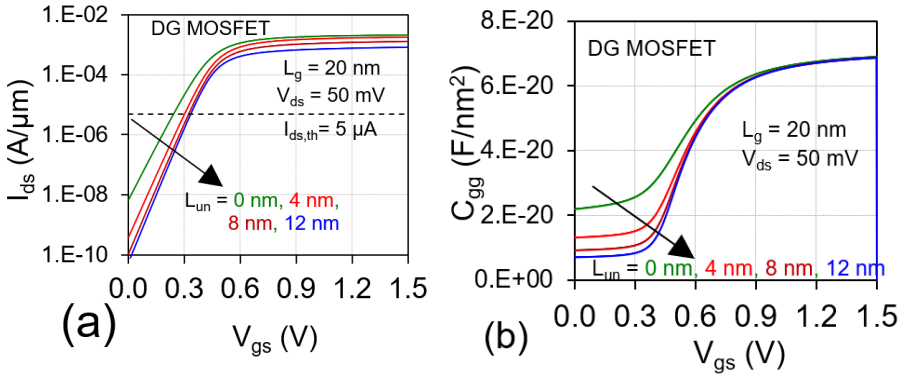

Fig. 2.3 Variation of (a) drain current (I_{ds}) and (b) gate capacitance (C_{gg}) with V_{gs} for DG underlap MOSFET with different L_{un} for L_g = 20 nm. L_{un} = 0 nm indicates a conventional DG MOSFET (without underlap).

From Fig. 2.4a, it is evident that V_{th} degradation improves from 0.243 V to 0.336 V with an increase in L_{un} i.e. V_{th} approaches long channel values. This improvement in the value of V_{th} indicates the reduction of SCEs. It is observed (Fig. 2.4b) that S_{swing} improves from 82.3 mV/dec to 66 mV/dec as the L_{un} is increased from 0 to 12 nm.

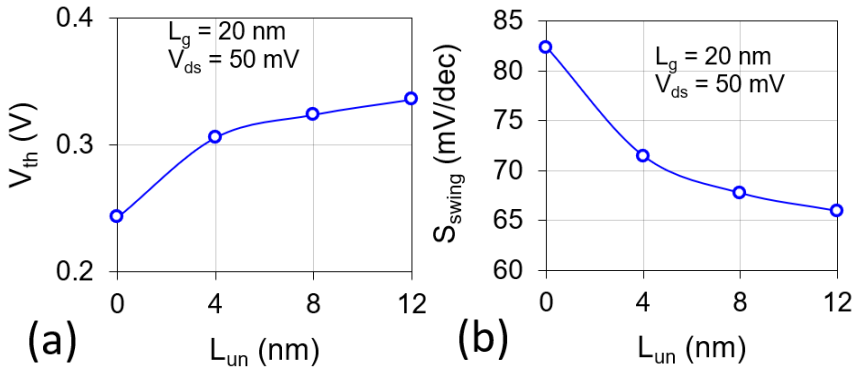

Fig. 2.4 Variation of (a) threshold voltage (V_{th}) and (b) subthreshold swing (S_{swing}) with L_{un} for L_g = 20 nm.

Indeed, the overall performance of the DG MOSFET is improved with the incorporation of underlap topology. The observed improvements in key performance metrics such as reduction in off-current, reduced roll-off in threshold voltage, nearly ideal values of subthreshold swing, and reduction in parasitic capacitance highlight the benefits of underlap for ULP applications.

2.5 Conclusion

This chapter has explored the impact of short channel effects on the performance of MOSFET. These effects, caused by shrinking device dimensions, pose challenges that can degrade device performance and affect reliability. However, the implementation of underlap architecture has emerged as a promising solution to mitigate these effects. Underlap devices exhibit enhanced robustness, reducing undesirable phenomena such as DIBL, threshold voltage roll-off, and parasitic. Furthermore, a comparative (without underlap) analysis of underlap-based DG MOSFET has been carried out using TCAD tool which shows that underlap structure helps in achieving improved transistor performances by reducing SCEs.

Chapter 3

Subthreshold Channel Potential and Drain Current for Double Gate Underlap MOSFET

3.1 Device Modelling

Device modeling plays a crucial role in capturing the intricate physical and electrical behavior exhibited by semiconductor devices [82]-[86]. These models can be broadly classified into two categories: physical device models and compact models [84], [85], each offering distinct advantages and serving specific purposes in understanding and characterizing device performance.

(1) Physical device models [84], [85] provide an understanding of underlying device physics, and invaluable insights into device operation. They allow for the determination of non-measurable quantities and enable the characterization of various physical parameters associated with the devices. These models comprehensively define the electrical behavior at the device terminals across different operational regions, encompassing characteristics such as current-voltage relationships and capacitance-voltage relations. Physical device models consider material properties, device geometry, dimensions, doping distribution, and carrier transport phenomena. Due to their precision and ability to capture the intricacies of device operation and underlying physics, these models are widely adopted in commercial numerical device simulators.

In contrast, compact models [84], [85] focus on reproducing the electrical behavior at the device terminals using interconnected electrical elements. They are designed as equivalent circuit models, with the overall model characteristics dependent on the specific device properties. Compact models offer computational efficiency and compact representation, making them highly suitable for circuit simulators, where faster and more extensive simulations are desired.

Although physical device models provide high accuracy, they are computationally intensive and may not be suitable for rapid simulations involving numerous devices and circuits. To address this challenge, several approaches have been developed to simplify physical device models into compact models [84]-[86].

- **Analytical models** [84]-[86] leverage device physics and provide closed-form solutions for physical quantities. However, these solutions are typically valid only within specific operating regimes, and it may be challenging to obtain a compact and continuous closed-form analytical model that covers all operating regimes, particularly for innovative MOSFET architectures.

- **Empirical models** [84]-[86], are based on curve fitting techniques, often employing polynomial or exponential functions. These models involve adjustable parameters that are tuned to fit the device characteristics. However, empirical models may lack physical significance and are often used in conjunction with analytical models to capture complex physical phenomena effectively.

- **Lookup table models** [84]-[86] employ pre-calculated tables containing values of physical or electrical quantities for various combinations of relevant parameters. These values can be obtained through numerical simulations or experimental measurements. During simulation, the model retrieves appropriate values from the table, eliminating the need for extensive calculations and saving computational time. However, the implementation of lookup table models requires a large dataset and interpolation functions to ensure high precision.

In summary, the later part of this chapter introduces a semi-analytical physical model. While most of the expressions in this model have closed-form solutions, numerical computation and analysis are necessary for certain equations to determine the values of unknown quantities. This semi-analytical approach strikes a balance between

accuracy and computational efficiency, making it a valuable tool for device modeling and simulation.

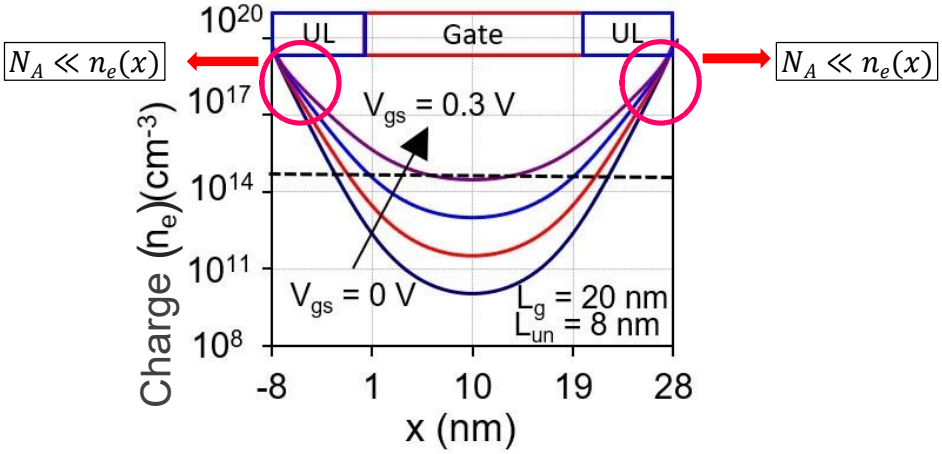

Fig. 3.1 Variation of electron concentration (n_e) along the channel length (x) in DG underlap MOSFET at different gate voltages (V_{gs}). Parameters: L_g = 20 nm, L_{un} = 8 nm, Silicon film thickness (t_{Si}) = 10 nm, oxide thickness (t_{ox}) = 1 nm, Doping concentration of silicon film (N_A) is 10^{20} cm^{-3} and V_{ds} = 0 V.

3.2 Subthreshold Model for DG Underlap MOSFET

In this section, a subthreshold analytical model for DG underlap MOSFET will be developed for ULP applications. By accurately understanding the device physics and selecting an appropriate approximation an effective model for DG underlap MOSFETs can be developed. In DG underlap MOSFET, the depletion region extends beyond gate edges. Also, the extension of the depletion region beyond gate edges varies with the gate voltages as shown in Fig. 3.1. Thus, in order to accurately model DG underlap MOSFET bias dependent depletion in the underlap region needs to be considered. Also, the electron concentration (n_e) at the gate edge is a function of (V_{gs}) and varies in the underlap region. Figure 3.1 illustrates the variation of n_e along the channel length (x) [81]. It is evident that the concentration is higher than the doping of the film (N_A = 10^{15} cm^{-3}) at source and drain edges, and the same cannot be neglected in analytical modeling. The underlap region of the film is not completely depleted, and the extent of

the depletion depends on the V_{gs}. However, in the existing model, the complete ungated region is considered to be depleted [72],[87]. Thus, to predict the device behavior correctly, the existing 3-region model (Region I: Source side underlap region, Region II: Drain side underlap region, and Region II: Gated region) needs to be converted into the 5-region model. Hence, a 5-region model is required to incorporate these considerations, which can offer greater accuracy compared to the 3-region models.

3.2.1 5-Region potential model

As illustrated in Fig. 3.1 and Fig. 3.2, region II (R_{II}) and region IV (R_{IV}) denote the extended depletion regions in the subthreshold region while region I (R_I) and region V (R_V) have sufficient (higher) electron concentration. Thus, R_I and R_V cannot be modeled with subthreshold approximation as the electron concentration is sufficiently high in these regions as compared to the doping in the channel (Fig. 3.1). Therefore, the bias dependent depletion of region III (R_{III}), R_{II}, and R_{IV} need to be considered in the model.

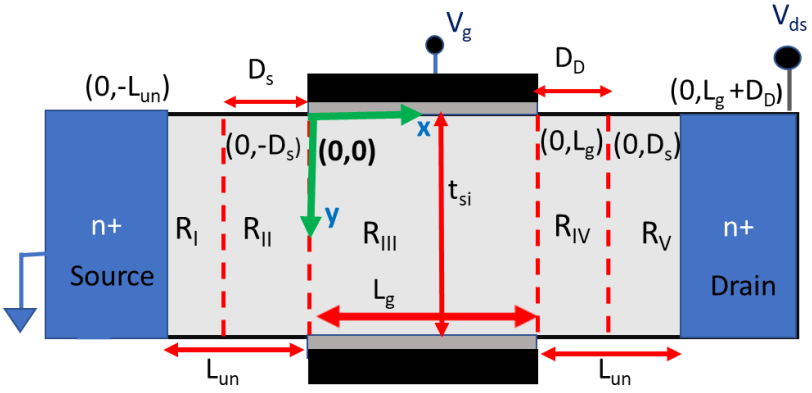

Fig. 3.2 An illustrative diagram showing the various regions (R_I to R_V) in a DG Underlap MOSFET.

3.2.1.1 Potential variation in Region I (R_I)

The region between the limits $-L_{un} \leq x \leq -D_s$ is defined as R_I. In this region, which is nearest to the heavily doped source, there is a

noticeable change in the electron concentration from $x = -L_{un}+L_g$ (source end) to $x = -L_{un}$ (boundary of R_I and R_{II}). This transition takes place from the highly doped (n^+) source to the underlap boundary (N_A). The transition in electrostatic potential over the Debye length is responsible for this change, and it is governed by the one-dimensional Poisson's equation. The equation for the potential distribution in R_I is given by:

$$\frac{d^2\Psi_I(x)}{dx^2} = \frac{-q}{\varepsilon_{si}}\left(-n_i exp\left(\frac{q\left(\Psi_I(x)-V_f(x)\right)}{kT}\right)\right) \quad (3.1)$$

where n_i represents the intrinsic carrier concentration of silicon, k denotes Boltzmann's constant, $V_f(x)$ represents the quasi-Fermi potential, q represents the charge of an electron, T represents the absolute temperature, and ε_{si} denotes the permittivity of silicon.

Multiplying and dividing by $\exp(qV_{bi}/kT)$ on the right-hand side of equation 3.1, following expression can be obtained

$$\frac{d^2\Psi_I(x)}{dx^2} = \frac{q}{\varepsilon_{si}} exp\left(\frac{qV_{bi}}{kT}\right)\left(n_i exp\left(\frac{q\left(\Psi_I(x)-V_f(x)-V_{bi}\right)}{kT}\right)\right) \quad (3.2)$$

where $V_{bi}=(kT/q)\ln\left(\frac{N_A}{n_i}\right)$ is the built in voltage, N_A is the doping of the film. The quasi-fermi potential at the source can be approximated as zero (V_f @ x = $-L_g - L_{un}$) ≈ 0), as it is independent of position (x) near the source. Further, using the Taylor's expansion, the exponential term in the right-hand side can be expanded and following equation can be obtained

$$\frac{d^2\Psi_I(x)}{dx^2} = K_1(V_T + \Psi_I(x) - V_{bi}) \quad (3.3)$$

where Ψ_I is the channel potential in R_I, V_T is thermal voltage at temperature T, and $K_1 = \frac{qn_i}{\varepsilon_{si}V_T} exp\left(\frac{qV_{bi}}{kT}\right)$.

The solution of equation (3.3) can be obtained as

$$\Psi_I(x) = Mexp\left(x\sqrt{K_1}\right) + Nexp\left(-x\sqrt{K_1}\right) + V_{bi} - V_T \quad (3.4)$$

where the coefficients *M* and *N* can be calculated by applying suitable boundary conditions.

3.2.1.2 Potential variation in region II (R_{II})

The region between the limits $-D_s \leq x \leq 0$ is defined as R_{II}. This region is positioned as the second closest to the heavily doped source. In this region, the width of depletion region towards the source is represented as D_S. Thus, 1-D Poisson's equations in R_{II} can be obtained as

$$\frac{d^2\Psi_{II}(x)}{dx^2} = \frac{qN_A}{\varepsilon_{si}} \tag{3.5}$$

where Ψ_{II} is the channel potential in R_{II}. By performing the double integral of equation (3.5) solution for Ψ_{II} can be obtained as

$$\Psi_{II}(x) = V_S - E_S(x + D_S) + \frac{qN_A}{2\varepsilon_{si}}(x + D_S)^2 \tag{3.6}$$

where V_s and E_s denote the potential and electric field at $x = D_S$, and these values can be determined by applying appropriate boundary conditions at the region interface.

3.2.1.3 Potential variation in region III (R_{III})

In the region beneath the gate, which spans from 0 to L_g (where L_g represents the gate length), the behavior is described by a 2-D Poisson's equation [88]. To enhance the validity of the model near threshold region, mobile charge needs to be consider along with doping density in the Poisson's equation [88]. Therefore, the Poisson's equation consisting of both mobile charge density and doping density in the R_{III} can be expressed as

$$\frac{d^2\Psi_{III}(x,y)}{dx^2} + \frac{d^2\Psi_{III}(x,y)}{dy^2} = \frac{qn_i}{\varepsilon_{si}} exp\left(\frac{q\left(\Psi_{III}(x) - V_f(x)\right)}{kT}\right) \tag{3.7}$$

The potential distribution in R_{III} (Ψ_{III}) can be represented using the principle of superposition, as illustrated below [88] - [90],

$$\Psi_{III}(x,y) = \Psi 1_{III}(y) + \Psi 2_{III}(x,y) \tag{3.8}$$

where $\Psi 1_{III}(y)$ represents the solution in the channel potential along the channel thickness (y) by solving 1D Poisson equation [88]. 1D Poisson equation for $\Psi 1_{III}(y)$ can be expressed as

$$\frac{d^2\Psi 1_{III}(x)}{dy^2} = \frac{q}{\varepsilon_{si}}\left(n_i exp\left(\frac{q\left(\Psi 1_{III}(x)\right)}{kT}\right)\right) \tag{3.9}$$

The boundary conditions for $\Psi 1_{III}(y)$ at the center and surface can be expressed as

$$\left.\frac{d\Psi 1_{III}(y)}{dy}\right|_{y=0} = 0 \tag{3.10}$$

$$-C_{OX}\left(V_{gs} - \Delta\Phi - V_f\right) = \varepsilon_{si}\left.\frac{d\Psi 1_{III}(y)}{dy}\right|_{y=\frac{t_{si}}{2}} \tag{3.11}$$

where C_{ox} is the oxide capacitance, $\Delta\phi$ is the flatband voltage.

Solution of $\Psi 1_{III}$ can be obtained by adopting the methodology used in [88], [91] as

$$\Psi 1_{III}(y) = \frac{-2kT}{q} ln\left(\frac{t_{si}}{2\beta_s}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}\, cos\left(\frac{2\beta_s y}{t_{si}}\right)\right) \tag{3.12}$$

where β_s is function of V_{gs} and can be calculated numerically by substituting $\Psi 1_{III}$ in equation (3.11) for $V_f = 0$ as

$$\frac{q\left(V_{gs} - \Delta\Phi - V_f\right)}{2kT} - ln\left(\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right)$$

$$= ln(\beta_s) - ln\left(cos(\beta_s)\right) + 2r\beta_s tan(\beta_s) \tag{3.13}$$

where $r = \frac{\varepsilon_{si}t_{ox}}{t_{si}\varepsilon_{ox}}$, t_{ox} is the oxide thickness, ε_{ox} is the oxide permittivity.

$\Psi 2_{III}(y)$ mentioned in equation (3.8) can be obtained by solving 2D Poisson's equation [89]-[92] shown below

$$\frac{d^2\Psi 2_{III}(x,y)}{dx^2} + \frac{d^2\Psi 2_{III}(x,y)}{dy^2} = 0 \tag{3.14}$$

Solution of equation (3.14) can be obtained as

$$\Psi 2_{III}(x,y) = \left(Aexp\left(\frac{x}{\lambda}\right) + Bexp\left(\frac{-x}{\lambda}\right)\right) cos\left(\frac{2\lambda}{t_{si}}\right) \tag{3.15}$$

where λ is the natural length [93] and A and B are unknown coefficient that can be calculated by applying boundary conditions.

Thus, Ψ_{III} in R_{III} can be obtained as

$$\Psi_{III} = \left(Aexp\left(\frac{x}{\lambda}\right) + Bexp\left(\frac{-x}{\lambda}\right)\right) cos\left(\frac{2\lambda}{t_{si}}\right) + \frac{-2kT}{q} ln\left(\frac{t_{si}}{2\beta_s}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}\, cos\left(\frac{2\beta_s y}{t_{si}}\right)\right) \tag{3.16}$$

where the values of unknown coefficient A and B can be determined by applying boundary conditions at gate edges.

3.2.1.4 Potential variation in region IV (R_{IV})

The region between the limits $L_g \leq x \leq L_g + D_D$ is defined as R_{IV}, which is located second closest to the heavily doped drain. In this region, depletion occurs, resulting in the right-hand side of 1-D Poisson's equations resembling the equation shown below (similar to R_{II}),

$$\frac{d^2\Psi_{IV}(x)}{dx^2} = \frac{qN_A}{\varepsilon_{si}} \tag{3.17}$$

where Ψ_{IV} is the channel potential in R_{IV}. Performing the double integral on equation (3.5), Ψ_{IV} can be obtained as

$$\Psi_{IV}(x) = V_D - E_D\left(x - L_g - D_D\right) + \frac{qN_A}{2\varepsilon_{si}}\left(x - L_g - D_D\right)^2 \tag{3.18}$$

where V_D and E_D represent the potential at $x = L_g + D_D$. These values can be determined by applying boundary conditions.

3.2.1.5 Potential variation in Region V

The region between the range $L_g + D_D \leq x \leq L_{un} + L_g$ is known as R_V. This region is located nearest to the heavily doped drain. The approach for finding the potential distribution in R_V is similar to that of R_I. The potential distribution in R_V can be describe using 1D Poisson's equation as

$$\frac{d^2\Psi_V(x)}{dx^2} = \frac{q}{\varepsilon_{si}}\left(n_i exp\left(\frac{q\left(\Psi_V(x)-V_f(x)\right)}{kT}\right)\right) \tag{3.19}$$

Multiplying and dividing the right-hand side of equation (3.19) by exp (qV_{bi}/kT), equation (3.19) can be written as

$$\frac{d^2\Psi_I(x)}{dx^2} = \frac{q}{\varepsilon_{si}} exp\left(\frac{qV_{bi}}{kT}\right)\left(n_i exp\left(\frac{q\left(\Psi_I(x)-V_f(x)-V_{bi}\right)}{kT}\right)\right) \tag{3.20}$$

where, $V_{bi}=(kT/q)\ln\left(\frac{N_A}{n_i}\right)$, N_A is the channel doping concentration of the film. $V_f(x)$ at the drain can be approximated to the drain voltage (V_{DS}), as it is independent of x near the source. By applying Taylor's expansion, the exponential term inside the bracket is expanded up to linear terms. Equation (3.2) then becomes,

$$\frac{d^2\Psi_V(x)}{dx^2} = K_1(V_T + \Psi_V(x) - V_{bi} - V_{DS}) \tag{3.21}$$

where V_T is thermal voltage equivalent at temperature T and $K_1 = \frac{qn_i}{\varepsilon_{si}V_T} exp\left(\frac{qV_{bi}}{kT}\right)$.

The solution to equation (3.21) can be obtained as

$$\Psi_V(x) = Pexp\left(x\sqrt{K_1}\right) + Qexp\left(-x\sqrt{K_1}\right) + V_{bi} + V_{DS} - V_T \tag{3.22}$$

The coefficients P and Q can be obtained by applying boundary conditions.

3.2.1.6 Boundary conditions

All the above-mentioned unknown coefficients (*A*, *B*, V_S, V_D, E_S, E_D, *M*, *N*, *P*, *Q*, D_S, and D_D) can be estimated using the potential and field continuation at the boundary of each region. The boundary conditions can be obtained by equating the potential and electric field of various regions at the boundaries as

$$\Psi_I(-L_{un}) = V_{bi} \tag{3.23a}$$

$$\Psi_I(-D_S) = \Psi_{II}(-D_S) \tag{3.23b}$$

$$\Psi_{II}(0) = \Psi_{III}(0) \tag{3.23c}$$

$$\Psi_{III}(L_g) = \Psi_{IV}(L_g) \tag{3.23d}$$

$$\Psi_{IV}(L_g + D_D) = \Psi_V(L_g + D_D) \tag{3.23e}$$

$$\Psi_V(L_g + L_{un}) = V_{bi} + V_{ds} \tag{3.23f}$$

$$\left.\frac{d\Psi_I(x)}{dx}\right|_{x = -D_S} = \left.\frac{d\Psi_{II}(x)}{dx}\right|_{x = -D_S} \tag{3.23g}$$

$$\left.\frac{d\Psi_{IV}(x)}{dx}\right|_{x = L_g + D_D} = \left.\frac{d\Psi_V(x)}{dx}\right|_{x = L_g + D_D} \tag{3.23h}$$

$$\left.\frac{d\Psi_{II}(x)}{dx}\right|_{x = 0} = \left.\frac{d\Psi_{III}(x)}{dx}\right|_{x = 0} \tag{3.23i}$$

$$\left.\frac{d\Psi_{III}(x)}{dx}\right|_{x = L_g} = \left.\frac{d\Psi_{IV}(x)}{dx}\right|_{x = L_g} \tag{3.23j}$$

$$\Psi_I(\infty) = V_{bi} \tag{3.23k}$$

$$\Psi_V(-\infty) = V_{bi} + V_{DS} \tag{3.23l}$$

Applying the boundary conditions shown in equations (3.23a)-(3.23l) for equations (3.4), (3.6), (3.16), (3.18), and (3.22), respectively, unknown coefficient can be obtained as

$$M = 0 \tag{3.24a}$$

$$Q = 0 \tag{3.24b}$$

$$N = V_T exp(-K_2 L_{un}) \tag{3.24c}$$

$$V_S = V_T exp\big(-K_2(L_{un} - D_S)\big) + V_{bi} - V_T \tag{3.24d}$$

$$P = V_T exp\left(-K_2\big(L_{un} + L_g\big)\right) \tag{3.24e}$$

$$V_D = V_T exp\big(-K_2(L_{un} - D_D)\big) + V_{DS} + V_{bi} - V_T \tag{3.24f}$$

$$E_S = V_T K_2 exp\big(-K_2(L_{un} - D_S)\big) \tag{3.24g}$$

$$V_D = -V_T K_2 exp\big(-K_2(L_{un} - D_D)\big) \tag{3.24h}$$

$$A = V_D + E_D V_D - \frac{qN_A}{2\varepsilon_{si}}\left(\frac{{D_D}^2 - {D_D}^2 exp\left(\frac{-L_g}{\lambda}\right) - V_S exp\left(\frac{-L_g}{\lambda}\right) + E_S D_S exp\left(\frac{-L_g}{\lambda}\right) - \Psi 1_{III}\left(1 - exp\left(\frac{-L_g}{\lambda}\right)\right)}{2sinh\left(\frac{L_g}{\lambda}\right)}\right) \tag{3.24i}$$

$$B = V_S - E_S D_S + \frac{qN_A}{2\varepsilon_{si}}{D_S}^2 - A + \frac{2KT}{q} ln\left(\frac{t_{si}}{2\beta_S}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}}\, cos\left(\frac{2\beta_S y}{t_{si}}\right)\right) \tag{3.25j}$$

Here, $K_2 = \sqrt{K_1}$

To obtained D_S, D_D, A and B equations (3.23i) and (3.23j) can be used as

$$\frac{qN_A D_S}{\varepsilon_{si}} - E_S = \frac{(A-B)}{\lambda} \tag{3.25}$$

$$\left(\frac{qN_AD_D}{\varepsilon_{si}} + E_D\right) = -\frac{\left(Aexp\left(\frac{L_g}{\lambda}\right) - Bexp\left(\frac{-L_g}{\lambda}\right)\right)}{\lambda} \quad (3.26)$$

Equations (3.24i), (3.24j), (3.25), and (3.26) can be solved numerically to obtain the values of D_D and D_S, and then all unknown coefficients are determined.

3.3 Subthreshold Current Model

The expression for the subthreshold drain-to-source current (I_{ds}) is given by equation [94], [95] as

$$I_{DS} = \frac{kTW\mu_n n_i\left(1 - exp\left(\frac{-V_{DS}}{V_T}\right)\right)}{H_1 + H_2 + H_3} \quad (3.27)$$

where H_1, H_2 and H_3 can be defined as

$$H_1 = \int_{-DS}^{0} \frac{dx}{\int_0^{T_{si}} exp\left(\frac{\Psi_{II}(x)}{V_T}\right)dy} \quad (3.28a)$$

$$H_2 = \int_0^{L_g} \frac{dx}{\int_0^{T_{si}} exp\left(\frac{\Psi_{III}(x,y)}{V_T}\right)dy} \quad (3.28b)$$

$$H_3 = \int_{L_g}^{L_g + D_D} \frac{dx}{\int_0^{T_{si}} exp\left(\frac{\Psi_{IV}(x,y)}{V_T}\right)dy} \quad (3.28c)$$

where W is the width of the device, and μ_n is the mobility of electrons. An analytical approximation for equation (3.27) is derived by considering piecewise assumptions instead of relying on numerical computation [94]-[95]. The value of H_1, H_2 and H_3 can be evaluated by trapezoidal rule [94].

3.4 Results and Discussion

By keeping certain device parameters fixed, such as the thickness of the silicon film (t_{si} = 10 nm), doping of the source/drain (N_D = 10^{20} cm^{-3}), doping of the silicon film (N_A = 10^{15} cm^{-3}), width of the gate (W = 1000 nm), and thickness of the oxide film (t_{ox} = 1 nm), gate

length (L_g = 20 nm), and L_{un} and biases (V_{gs} and V_{ds}) are varied to observe their impact on the potential and drain current (in the subthreshold region). To validate the proposed DG underlap subthreshold model, simulated Technology Computer-Aided Design) (TCAD) data has been used for which ATLAS device simulator has been used with appropriate models for generation-recombination, field and concentration dependent mobility. For all results, symbols are used for simulated data and the lines correspond to the derived model. By comparing the two, we can evaluate the accuracy of the derived model in subthreshold region. This allows for a comprehensive analysis of the predictive capabilities of the developed model.

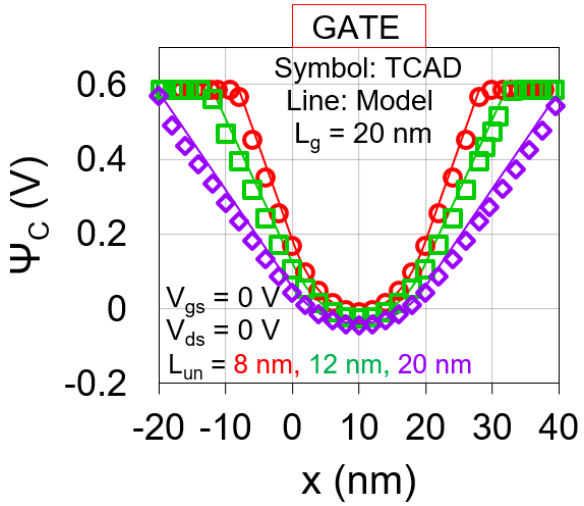

Fig. 3.3 Variation of center potential (Ψ_C) along the channel (x) with various underlap length (L_{un}) for V_{gs} = V_{ds} = 0 V. Other parameters are same as listed in Fig. 3.1.

Figure 3.3 depicts the variation of center potential (Ψ_C) in along the channel (x) for zero gate and drain bias for an underlap length varying from 8 nm to 20 nm. The derived model demonstrates clear agreement with TCAD results. The effect of underlap is distinctly visible on the channel potential. A larger L_{un} helps to reduce the minimum channel potential i.e. channel potential at x = 10 nm (mid-gate position), reduces as the underlap length increases from 8 nm to 20 nm.

Also, a larger underlap length helps to increase the effective channel length (through extended depletion region), which significantly suppresses the effect of drain (lateral) field on the channel potential i.e. immunity from SCEs.

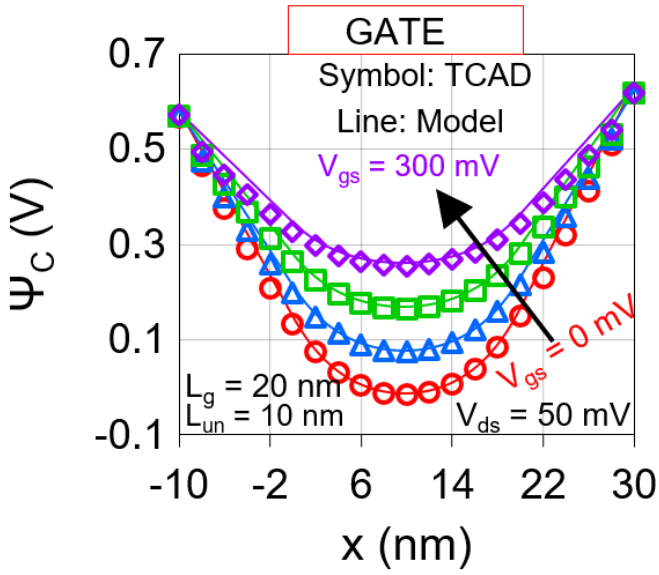

Fig. 3.4 Variation of center potential (Ψ_C) along the channel length (x) for various gate bias (V_{gs}) for a fixed L_g (20 nm) and L_{un} (10 nm). V_{ds} = 50 mV. Other parameters are same as listed in Fig. 3.1.

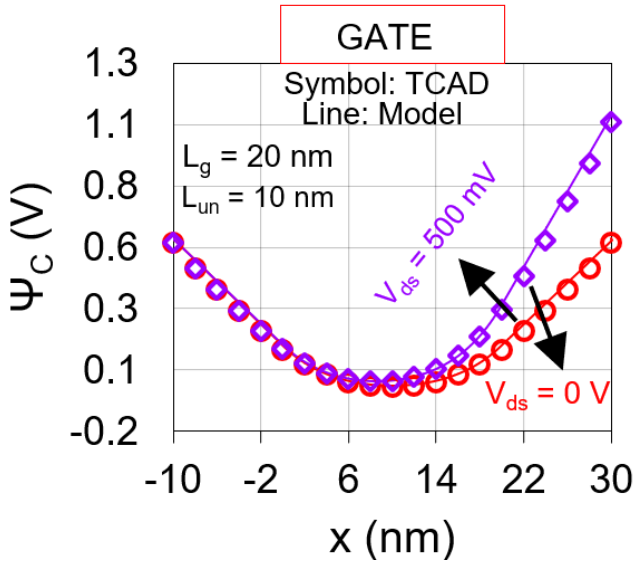

Fig. 3.5 Variation of center potential (Ψ_C) along the channel length (x) for a drain bias of 0 V and 500 mV. Other parameters are same as listed in Fig. 3.1.

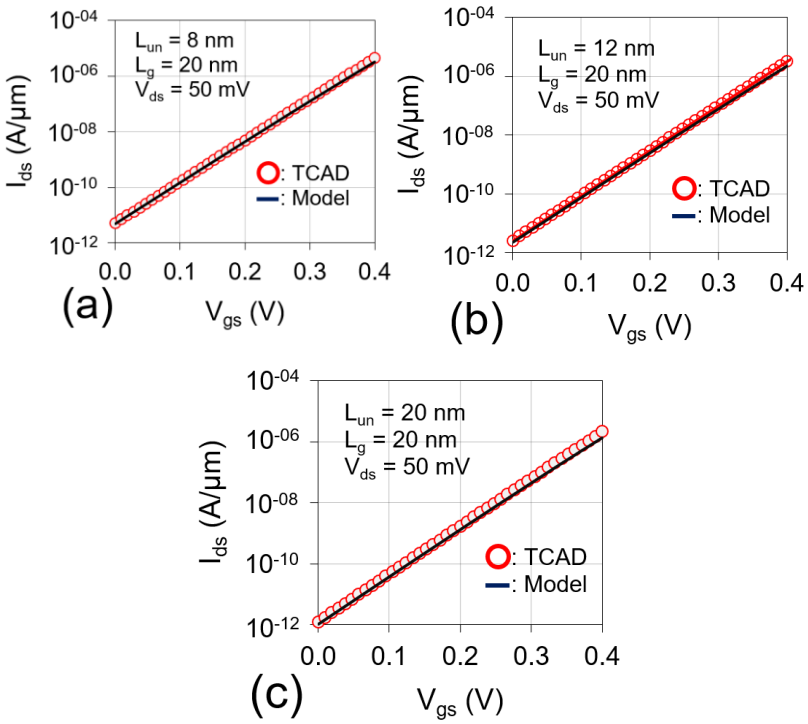

Fig. 3.6 Variation of subthreshold drain current with gate voltage (V_{gs}) for (a) L_{un} = 8 nm, (b) L_{un} = 12 nm, and (c) L_{un} = 20 nm. Other parameters are same as listed in Fig. 3.1.

Figure 3.4 shows the variation of center potential along the *x*-direction for a fixed L_g (20 nm) and fixed L_{un} (10 nm), for various V_{gs} (0 V to 300 mV). An increase in V_{gs} results in a rise in potential of underlap region i.e. rise in electron concentration in ungated region. This indicates that the extension of depletion in the ungated region has reduced as V_{gs} increases i.e. effective channel length decreases with an increase in V_{gs}. The derived model demonstrates a satisfactory agreement with the simulation results, indicating its capability to accurately predict the potential distribution at different V_{gs}. This substantiates the effectiveness of the model in capturing the device behavior, and its response to varying V_{gs} in the subthreshold region. Similarly, Fig. 3.5, shows the impact of V_{ds} on the center potential for fixed L_{un} and L_g. This figure indicates that by increasing V_{ds}, the minimum channel potential also increases because of enhanced drain electric field i.e. DIBL effect. Thus, the derived model successfully captures the magnitude of SCEs in the device.

Figures 3.6(a)-(c) shows the variation of I_{ds} with V_{gs} for L_{un} of 8 nm, 12 nm, and 20 nm, respectively. V_{ds} is fixed at 50 mV in Fig. 3.6. As L_{un} varies from 8 nm (Figure 3.6(a)) to 20 nm (Figure 3.6(c)), subthreshold swing varies from 68 mV/dec to 62 mV/dec, and I_{OFF} varies from 6 pA to 1 pA. DG MOSFET (without underlap) shows a subthreshold seeing of 82 mV/dec, and an I_{OFF} ~50 pA. Therefore, the results clearly indicate the benefits of an underlap region in the nanoscale DG MOSFET for ULP (subthreshold) applications.

3.5 Conclusion

In this chapter, a 5-Region model for DG underlap MOSFET is developed considering the bias dependent depletion in underlap region. The proposed potential and drain current model for underlap DG MOSFET shows good agreement in the subthreshold region for various underlap lengths and applied biases. As a result, this model can be effectively employed for circuit modeling for ULP applications. The ability to accurately represent the device characteristics and behavior in the subthreshold region makes the model a valuable tool for designing and optimizing circuits that operate at relatively low voltage levels.

Chapter 4

Investigation of Capacitance in Double Gate Underlap MOSFET

4.1 Importance of MOSFET Capacitance

MOSFET capacitance has significant importance in various aspects of digital and analog circuit design. Some of the key figures of merits of the device and circuit, which are affected by the MOSFET capacitance, are mentioned below:

Switching speed [96],[97]: The gate capacitance plays a key role in determining the switching speed of a MOSFET. It governs the time required to create the channel which affects the turn-on and turn-off times of the transistor. By accurately modeling and managing the gate capacitance, designers can optimize the switching speed of MOSFET-based circuits, leading to improved overall performance.

Power consumption [98],[99]: The gate capacitance directly influences the power consumption of a MOSFET. During switching operations, the transition between the on and off states of the transistor depends on its gate capacitance. Thus, degraded switching can cause high power dissipation. By minimizing the gate capacitance or optimizing its value, designers can reduce power consumption in MOSFET-based circuits, enhancing energy efficiency.

Circuit performance and signal integrity [100]-[102]: The gate capacitance affects various circuit performance parameters, including gain, frequency response, and signal integrity. It influences the input impedance of the MOSFET and the gain of amplifier circuits. Additionally, the gate capacitance interacts with other capacitances and resistances in the circuit, affecting signal propagation delays, rise and fall times, and overall circuit behavior.

Noise immunity [101],[102]: The gate capacitance helps in reducing the susceptibility of MOSFETs to external noise sources. The gate

capacitance can be utilized as a low-pass filter, attenuating high-frequency noise components, and improving the noise immunity of the device. By carefully considering the gate capacitance in circuit design, designers can enhance the robustness and reliability of MOSFET-based systems.

Device modeling and simulation [82]-[86]: Accurate modeling of MOS capacitance is crucial for device simulation and circuit analysis. It enables designers to predict the behavior of MOSFETs in different operating conditions, validate circuit performance, and optimize design parameters. MOS capacitance models, such as the well-known MOS capacitor models, provide a foundation for device simulation tools used in the semiconductor industry.

Thus, a proper understanding and optimization of MOS capacitance, particularly the gate capacitance in MOSFETs, are vital for achieving desired performance, power efficiency, signal integrity, and noise immunity in modern electronic circuits and systems.

4.2 Gate Capacitance of DG MOSFET

The gate capacitance (C_{gg}) of DG MOSFET depends on the capacitive coupling between the gate and the channel region of the device [103]. As the gate voltage (V_{gs}) increases, the source to channel barrier for electrons reduces, which results in an electron density increase underneath the gated region i.e. the formation of the inversion layer [103],[104]. Therefore, the charge underneath the gated region varies with V_{gs}, which constitutes the crux of gate capacitance.

Apart from the gate-to-channel coupling through the gate oxide, C_{gg} may have some unwanted components, which do not depend on the charge variation in the channel. Those components are known as parasitic components [105]. Thus, C_{gg} depends on the two capacitive components i) gate-to-channel capacitance (C_{gc}), which is due to the gate-to-channel coupling, and ii) parasitic capacitance (C_{Para}), which is due to the closely spaced metal electrodes and highly doped region

[105],[106]. Thus, an understanding of gate-to-channel capacitance and the parasitic capacitances in MOSFETs is crucial for accurate device modeling, circuit design, and performance optimization.

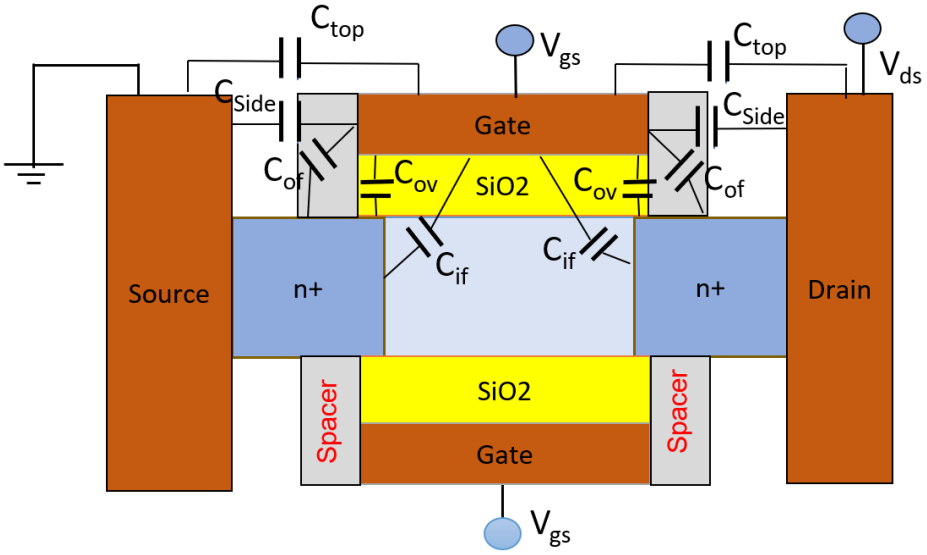

Fig. 4.1 Schematic diagram of DG MOSFET showing the parasitic components between source/drain and front gate. Similar components will be present between the back gate and drain/source terminals.

4.2.1 Gate to channel capacitance

The gate-to-channel capacitance (C_{gc}) refers to the capacitance between the gate electrode and the channel region of a MOSFET. It is an inherent capacitance that exists due to the capacitive coupling between gate and channel through gate oxide layer. C_{gc} is formed by the charges stored in the channel region that is influenced by V_{gs}. As V_{gs} increases, mobile charge density (Q_{Mobile}) under the gate increases, due to the reduced source to channel barrier for electrons, Q_{Mobile} in the channel can be obtained as [103],[104]

$$Q_{Mobile} = 2 \times C_{ox}\left(V_{gs} - \Delta\Phi - \Psi_S\right) \tag{4.1}$$

where C_{ox} is the gate oxide capacitance (= ε_{ox}/t_{ox}), $\Delta\Phi$ is the flatband voltage and Ψ_S is the minimum channel potential at the surface of the device. Factor '2' in equation (4.1) is due to the symmetric DG structure.

Using the equation (4.1), C_{gc} can be derived by differentiating the Q_{Mobile} with respect to the V_{gs} as

$$C_{gc} = 2 \times C_{ox}\left(1 - \frac{d\Psi_S}{dV_{gs}}\right) \tag{4.2}$$

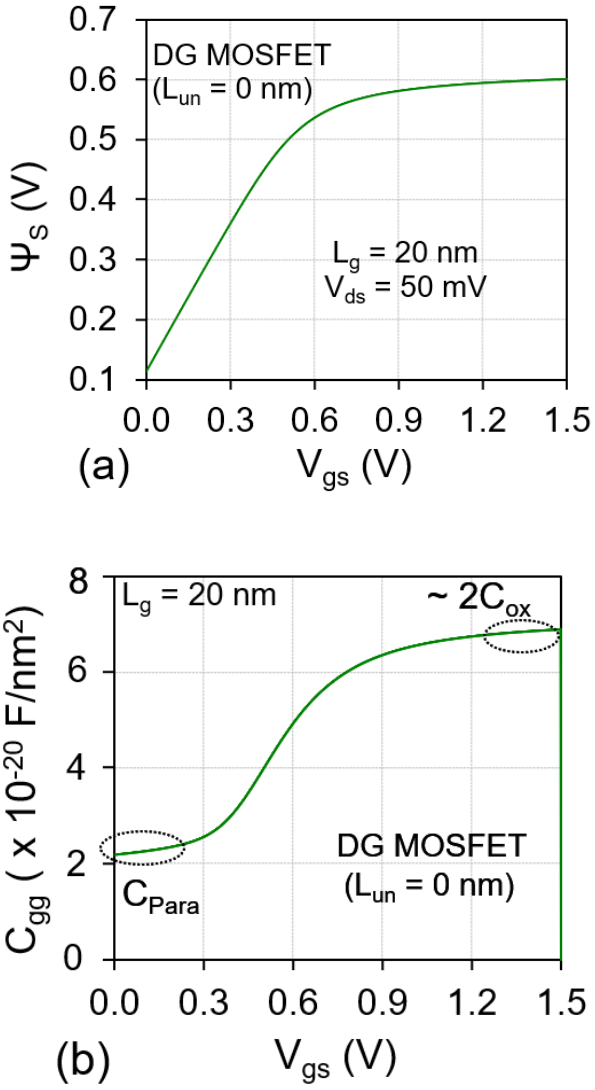

Fig. 4.2 Variation of (a) minimum surface potential (Ψ_S) and (b) gate capacitance (C_{gg}) of DG MOSFET with gate voltage (V_{gs}). Parameters: gate length (L_g) = 20 nm, drain voltage (V_{ds}) = 50 mV.

The gate-to-channel capacitance plays a key role to determine the device characteristics and performance. It affects the threshold voltage, and

influences the transconductance (g_m), which relates to the change in I_{ds} with respect to the V_{gs} [101],[102].

Figure 4.2(a) shows the variation of Ψ_S with V_{gs}. In the subthreshold region, Ψ_S varies linearly with V_{gs}, which results in C_{gg} not varying significantly with V_{gs} (Fig. 4.2(b)). As V_{gs} increases above the threshold voltage, Ψ_S shows a nonlinear relation (with V_{gs}) due to the formation of the inversion layer. Therefore, above the threshold voltage, C_{gg} increases with V_{gs}. However, for a very high value of V_{gs}, Ψ_S does not vary significantly i.e. the inversion layer shields the channel from the gate electric field. Thus, for very high V_{gs}, C_{gg} saturates at a value equal to the oxide capacitance (~ $2C_{ox}$ in DG MOSFET).

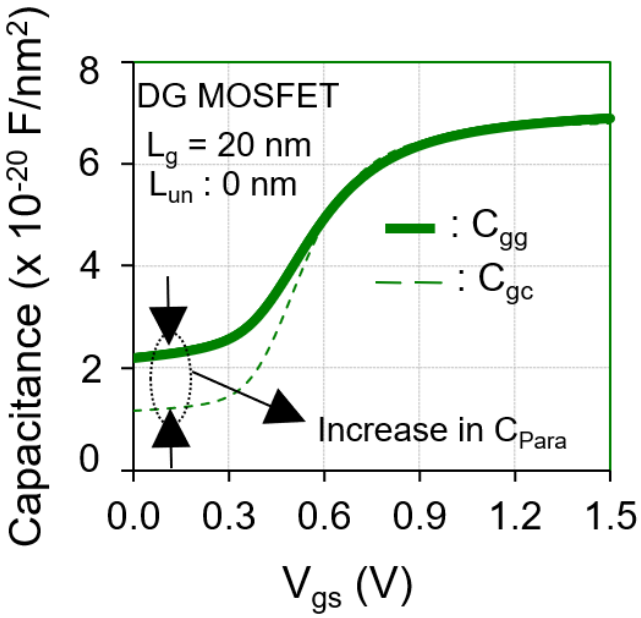

Fig. 4.3 Variation of C_{gg} and C_{gc} with V_{gs} in DG MOSFET. Parameters are the same as listed in Fig. 4.2.

Figure 4.3 shows the variation of C_{gg} and C_{gc} of DG MOSFET with V_{gs}. A long channel device, operating in the subthreshold region, attains a very low C_{gc} as the channel charge does not vary in the subthreshold region i.e. body factor of the device ($dV_{gs}/d\psi_s$) remains unity. However, in a short channel device, the body factor attains a value greater than unity ($dV_{gs}/d\psi_s > 1$) in the subthreshold region due to poor

gate controllability, which results in C_{gc} attains a finite value (~7×10^{-21} F/nm^2) in the subthreshold region for a L_g = 20 nm.

4.2.2 Parasitic capacitance

Parasitic capacitance is the undesirable capacitance that always exists between the closely spaced metal electrodes and the highly doped region. There are various types of parasitic capacitances observed in a DG MOSFET as shown in Fig 4.1.

- **Overlap capacitance (C_{ov}):** The capacitance formed due to overlapping between the highly doped source and drain regions under the gate is known as overlap capacitance. By reducing the overlap length, this component can be reduced.

- **Outer fringing capacitance (C_{of}):** The capacitance between the heavily doped source or drain and gate sidewall through the dielectric spacer is called outer fringe capacitance. This component depends on the proximity of source drain region with the gate.

- **Top fringing component (C_{top}):** The capacitance between top surface of the gate and source, drain electrodes is called as top fringing capacitance.

- **Sidewall capacitance (C_{Side}):** The capacitance between the gate and source/drain electrodes through the spacer is called sidewall capacitance [107]. This capacitance depends on spacer length and material [107].

- **Inner fringing capacitance (C_{if}):** The capacitance between the heavily doped source or drain junction and gate through the silicon is called inner fringe capacitance.

Thus, total gate capacitance can be obtained as

$$C_{gg} = C_{gc} + C_{Para} \tag{4.3}$$

where C_{Para} is the equivalent parasitic capacitance of all components and can be obtained using the approach reported in [108]-[110]. The difference in C_{gg} and C_{gc} in the subthreshold region can be considered as parasitic capacitance as shown in Fig. 4.3. C_{Para} decreases with V_{gs} because of reduction in C_{if}. An inversion region formed underneath gate shields the field lines between gate and source/drain region through silicon film which results in a reduction in C_{if} with gate biases and vanishes in the inversion region [108]-[110]. Therefore, the parasitic capacitance dominates only in the subthreshold region [108]-[110].

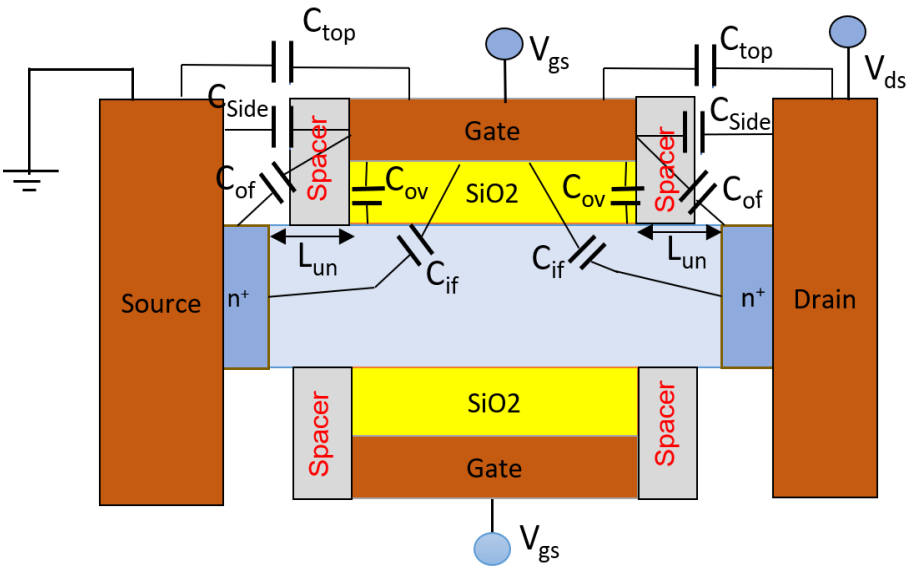

Fig. 4.4 Schematic diagram of DG underlap MOSFET showing various parasitic capacitance components.

Parasitic capacitances can lead to several effects, such as signal coupling, frequency response limitations, and increased power consumption. They can cause a reduction in gain, increase in propagation delay, and degradation in the overall performance of the circuit. These parasitic capacitances arise due to the physical structures and layout of the transistor, and they are typically unwanted capacitances that can impact device performance. Thus, by choosing an appropriate structure parasitic capacitance can be minimized.

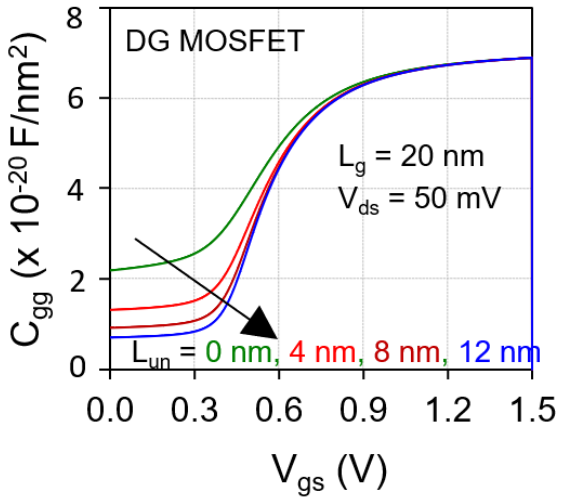

Fig. 4.5 Variation of gate capacitance (C_{gg}) with gate voltage (V_{gs}). For various underlap lengths (L_{un}). Other parameters are the same as listed in Fig. 4.2.

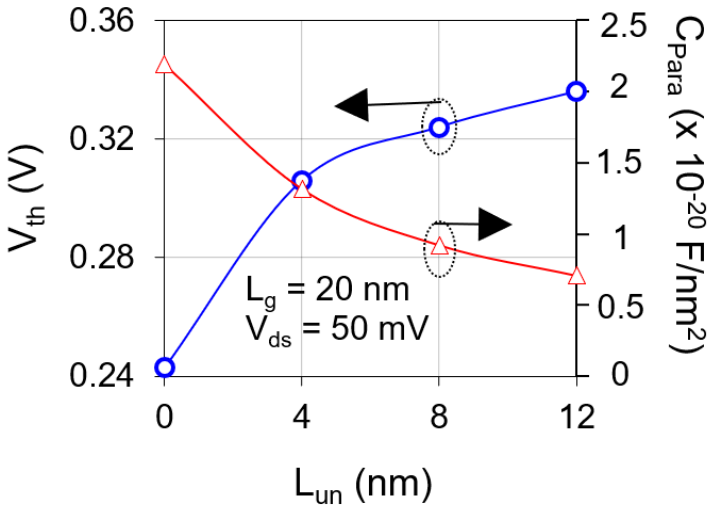

Fig. 4.6 Variation of parasitic capacitance (C_{Para}) extracted at V_{gs} = 0 V and threshold voltage (V_{th}) extracted using constant current method [111] for various underlap lengths (L_{un}). Other parameters are the same as listed in Fig. 4.2.

4.3 Gate Capacitance of DG Underlap MOSFET

Apart from improving the subthreshold swing, and off-current, underlap design in the DG structure can be used to suppress the parasitic capacitance [108]-[110].

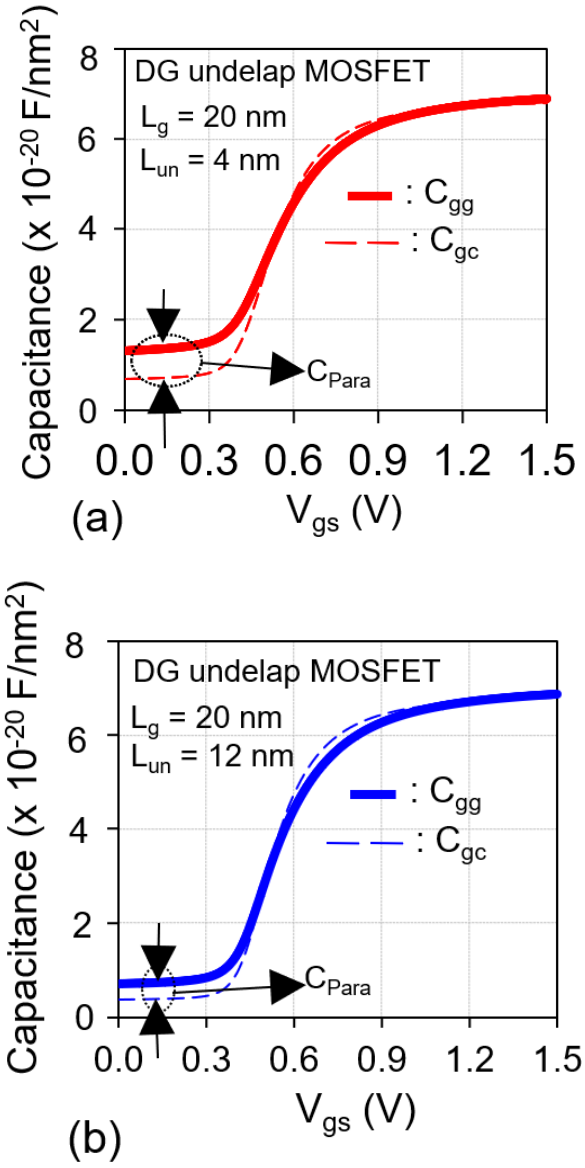

Fig. 4.7 Variation of C_{gg} and C_{gc} with V_{gs} in DG underlap MOSFET for (a) L_{un} = 4 nm, and (b) L_{un} = 12 nm. The parameters are the same as listed in Fig. 4.2.

An extension of a lightly doped channel beyond the gate edges helps to reduce the outer fringing capacitance component and inner fringing components as shown in Fig. 4.4. In DG underlap MOSFET, heavily doped source and drain region can be kept away from the gate through the underlap region. This results in a lower coupling between i) gate sidewall and source/drain region through the sidewall spacer (C_{of}), and ii) the gate bottom and source/drain region through silicon film (C_{if}) [108]-[110]. Therefore, DG underlap MOSFET device shows smaller

parasitic capacitance as compared to the conventional DG MOSFET (without underlap) as shown in Fig. 4.6. A drastic reduction in MOSFET's parasitic capacitance is observed in the C_{Para} as L_{un} increases from 0 nm (conventional DG MOSFET) to 12 nm i.e. C_{Para} decreases by 67%. Fig. 4.6 shows that choosing larger underlap causes both C_{Para} and threshold voltage (V_{th}) to improve i.e. V_{th} increases from 243 mV to 336 mV as L_{un} increases from 0 nm (conventional DG MOSFET) to 12 nm. Figure 4.7(a)-(b) shows the variation of C_{gg} and C_{gc} for underlap lengths of 4 nm and 12 nm, respectively. For L_{un} = 12 nm, a smaller difference in C_{gg} and C_{gc} is observed, which indicates a lower C_{Para} in the device with a larger L_{un}. Apart from a lower C_{Para}, a larger L_{un} also helps to reduce C_{gc} in the subthreshold region due to improved short-channel immunity. Therefore, an underlap structure can be a potential alternative for high-speed ULP applications because of its ability to attain lower parasitic capacitance and subthreshold swing.

4.4 Conclusion

In this chapter, gate to channel capacitance and parasitic capacitance are discussed in detail. In the subthreshold region, gate capacitance primarily depends on the parasitic capacitance. Thus, it is essential to minimize the parasitic capacitance in order to enhance the delay and cut-off frequency of the device. An underlap structure helps to keep heavily doped source drain away from the channel, which results in a reduced outer fringing and inner fringing capacitance. Also, increasing the underlap region length, the parasitic capacitance can further reduce.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

Transistor size has been steadily shrinking over the past 40 years to enhance device performance. Moore's Law forecasted that the quantity of transistors in integrated circuits would double every two years, driving the advancement in the number of transistors found in contemporary devices. In order to follow Moore's law predictions, the semiconductor industry has upgraded to multi-gate transistors such as double gate (DG) transistors to support further downscaling. However, due to a greater number of gates in DG MOSFET, a larger contribution of parasitic capacitance in total gate capacitance is observed. A larger parasitic capacitance in double gate MOSFET affects the circuit delay and cut-off frequency. Also, at very shorter gate lengths, short channel effects (SCEs) become dominant. In order to mitigate the challenges associated with SCEs and higher parasitic capacitance in DG MOSFET, underlap structure can be adopted. A DG MOSFET with underlap provides excellent short channel immunity because of enhanced effective length. Also, a larger separation between the heavily doped source/drain and metal gate (through underlap region) significantly reduces the outer and inner fringing capacitance which reflects in a lower parasitic capacitance.

In this thesis, a subthreshold model is derived for channel potential and drain current. The developed five region model can provide more accurate assessment as it considers the bias-dependent region boundaries. The developed models show good accuracy with the TCAD data for various biases and underlap length. In addition, a detailed study of channel and parasitic capacitance is also carried out for DG underlap MOSFET, which shows the suitability of larger underlap for reducing the parasitic capacitance. Other potential benefits of larger underlap such as improved subthreshold swing, off current,

and threshold voltage are also highlighted in this work through the analytical model and TCAD simulations.

5.2 Future Work

In this work, a subthreshold model is derived for potential and drain current, which is not valid for the above threshold region. However, a complete analytical model is also essential for circuit simulation utilizing the DG underlap MOSFET. Thus, the development of a complete model from the subthreshold region to the inversion region will be future work.

Also, in this work, current and potential is developed while the analysis done on capacitance is completely based on the TCAD simulation. Thus, extensive modeling of parasitic capacitance and channel capacitance may be another future work.

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