PHYSICAL MODELING AND LOGIC CIRCUIT IMPLEMENTATION OF Y_2O_3 BASED MEMRISTOR

M.Tech. Thesis

By

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DISCIPLINE OF ELECTRICAL ENGINEERING

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A THESIS

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MEGHA NAWARIA

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **PHYSICAL MODELING AND LOGIC CIRCUIT IMPLEMENTATION OF Y_2O_3 BASED MEMRISTOR** in the partial fulfillment of the requirements for the award of the degree of **MASTER OF TECHNOLOGY** and submitted in the **DEPARTMENT OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore** is an authentic record of my own work carried out during the time period from JUNE 2022 to MAY 2023 under the supervision of Prof. Shaibal Mukherjee, Professor Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Megha 30-05-2023

Signature of the student with date

(MEGHA NAWARIA)

This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

S. Mukherjee 30/May/2023

Signature of the Supervisor of

M.Tech. thesis (with date)

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MEGHA NAWARIA has successfully given her M.Tech. Oral Examination held on **16 MAY 2023**.

S. Mukherjee 30/May/2023

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DEDICATION

Dedicated to my family for their endless love, support and encouragement throughout my academic persuit. I hope this achievement would be a step closer to fullfill their dream they envisioned for me.

ABSTRACT

This work is a combination of comprehensive study of memristor physical modeling using COMSOL Multiphysics software and the application view of memristor in the Cadence Virtuoso. Memristors are a novel class of passive circuit elements that exhibit a unique property of memory, making them an exciting area of research for next-generation computing and memory devices. The goal of this work is to create a memristor physical model that is reliable and effective at predicting electrical behaviour and also able to implement digital circuits that is reliable and can replace CMOS based circuits .

The work begins with a detailed literature review of the memristor and it's existing memristor physical models and switching mechanisms. After a thorough understanding of the underlying physics and proposed memristor model that takes into account various factors such as the filament formation, ion migration, and electrical conduction mechanisms in memristive devices. The model is implemented in COMSOL Multiphysics, a powerful finite-element analysis software that can accurately simulate the complex behavior of memristors.The accuracy of the proposed model is verified by comparing the simulation results with the experimental data available in the literature. The simulation results are found to be in good agreement with the experimental data, indicating the accuracy of the proposed model.

Also, after a thorough understanding of the underlying principles, a new memristor-based logic circuit architecture is proposed. The proposed architecture is implemented using Verilog –A and simulated using Cadence Virtuoso software.The simulation results demonstrate the feasibility of implementing logic circuits using memristors. The proposed architecture shows promising results in terms of power consumption, area utilization, and delay compared to traditional CMOS-based logic circuits.

Furthermore, the proposed architecture is tested for various logic functions such as NOT, AND, OR, XOR, XNOR, NAND and NOR and the simulation results show accurate logic function output. Using the functions implemented above other logic circuits like 2×1 MUX, full adder and full subtractor have implemented.

The outcome of this work is a robust physical model that accurately predicts the behavior of memristive devices .It offers many potential advantages over traditional CMOS-based logic circuits and can be used for the design and optimization of low-power and high-speed logic circuits. This work contributes to the advancement of memristor technology and provides a platform for further research in this exciting field.

LIST OF PUBLICATIONS

[1] **Megha Nawaria**, Sanjay Kumar, Mohit Kumar Gautam, Narendra Singh Dhakad, Rohit Singh, Sonal Singhal, Pawan Kumar, Santosh Kumar Vishvakarma and Shaibal Mukherjee, "Memristor-inspired Digital Logic Circuits and Comparison with 90-/180-nm CMOS Technologies", IEEE Transactions on Electron Devices, Accepted, 2023, doi:10.1109/TED.2023.3278625.

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LIST OF ABBREVIATIONS

RRAM	Resistive Random Access Memory
STM	Short Term Memory
LTM	Long Term Memory
LRS	Low Resistive State
HRS	High Resistive State
CF	Conductive Filament

Chapter 1

Introduction

1.1 Motivation

The "Big Data" era's emergence is what is causing the downscaling of CMOS technology [1]. Non-volatile flash memory now on the market has already faced a number of technical obstacles in order to maintain Moore's law [2] inside the current Von-Neumann computer architecture [3]. The first effect of device structure minimization is a reduction in the distance between the floating gates of two neighbouring cells in CMOS technology. A read mistake would result from the floating of charges in one gate to the neighbouring cell as well as an unintended shift in threshold voltage [4]. Second, the charge transfer is made worse by the drop in oxide thickness because of leakage current in the off-state situation. Such threshold voltage variation would inject unreliable stochastic operation into the flash device's programme, erase, and retention capabilities [5].An alternate developing memory device is required to overcome such flash memory scaling difficulties. Furthermore, in order to support high computing throughput while maintaining the demand for low power applications, today's memory devices either need to have lower latency or more capacity. In the past ten years, research in this field has advanced significantly in terms of device size, power consumption, data retention, and endurance [6].It is challenging for the traditional Von-Neumann computer architecture to meet the memory demand with device scaling in practise. A non-Von Neumann architecture [7] with an alternative memory device to the existing CMOS technology is anticipated to provide a workable solution in this area.Resistive random-access memory (RRAM) has been studied for more than 40 years and has become a top contender for non-volatile memory in the future [8], [9].

1.2 Memristor

One class of these RRAM group devices is the memristor.The concept of the memristor was first introduced by the renowned electrical engineer Leon Chua in 1971, as the fourth fundamental passive circuit element alongside the resistor, capacitor, and inductor[10]. Chua theorized that a memristor would be a two-terminal device that could maintain a memory of the current and voltage history that it had been subjected to, and that this memory would be stored in the form of a change in its resistance [11, 12]. However, despite the theoretical prediction, it wasn't until nearly four decades later that the first practical memristor was demonstrated.

In 2008, a team of researchers at HP Labs led by R. Stanley Williams reported the discovery of a titanium dioxide-based memristor, which they had been working on since the late 1990s [10]. The HP memristor was able to store information by changing its resistance in response to the amount of electrical charge passed through it, and it was also able to switch between different resistance states very quickly, making it a promising candidate for future memory and computing applications [10]. Since then, memristors have been the subject of intensive research, with many variations of the device being developed, such as those based on other materials like tantalum oxide, niobium oxide, and silver chalcogenides [13]. Overall, the history of the memristor spans several decades of theoretical and experimental work, culminating in the discovery of practical devices with great potential for various applications in computing, memory, logic circuits and neural network [14, 15] . They are also being explored for their potential use in neuromorphic computing, which aims to mimic the behavior of biological neural networks to create more efficient and adaptive computing systems [14].

Overall, the discovery of memristor represents a major breakthrough in the field of electronics and has the potential to revolutionize various industries, from computing to medicine.

The relationship between each pair of quantities created is depicted in Figure 1.1. As shown in Figure 1.1, the relationship between flux (φ) and charge (Q) was determined to be the missing component.This suggests that the missing component maintains track of not only the quantity and direction of the charge flowing through it, but also its whole history. Despite the discovery,

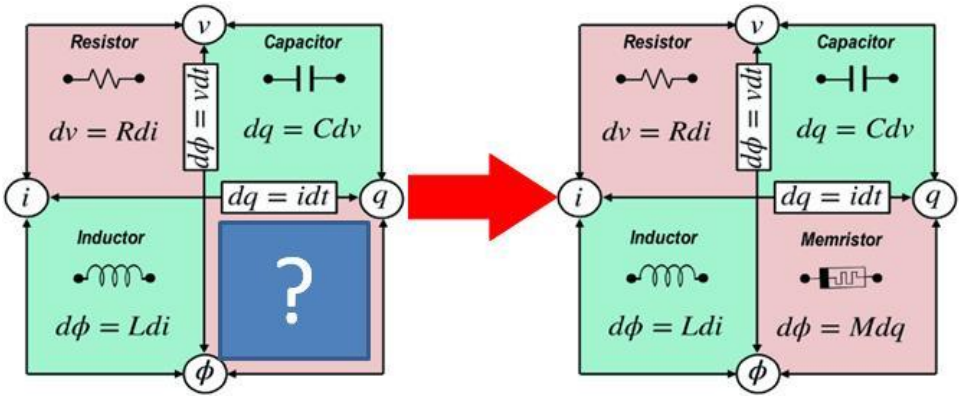

Figure 1.1 Linkage between four fundamental circuital elements.[16]

The ability to switch between stable resistance states and maintain the state even without a voltage supply is one of the shared characteristics of the memristive device family (non-volatility). Phase change memories (PCM), spin-torque transfer magnetic RAM (STT-MRAM), conductive bridge RAM (CB-RAM), and redox oxide-based RAM are a few of the well-known memristor-based memories (ReRAM). The proper model is required for applications using memristors in order to examine and simulate the system. We have discovered through reading the literature that the HP memristor model depends on oxygen vacancy drift. Figure 1.2 shows the $Pt/TiO_2/Pt$ structure of the HP Lab memristor model. The TiO2 oxide layer, which is sandwiched between the two noble metallic layers, specifically platinum, in the HP labs model, has a positively charged

oxygen vacancy on one side . A portion of the oxide layer that is undoped displays high resistance behaviour, whereas a portion that is doped displays low resistance behaviour.

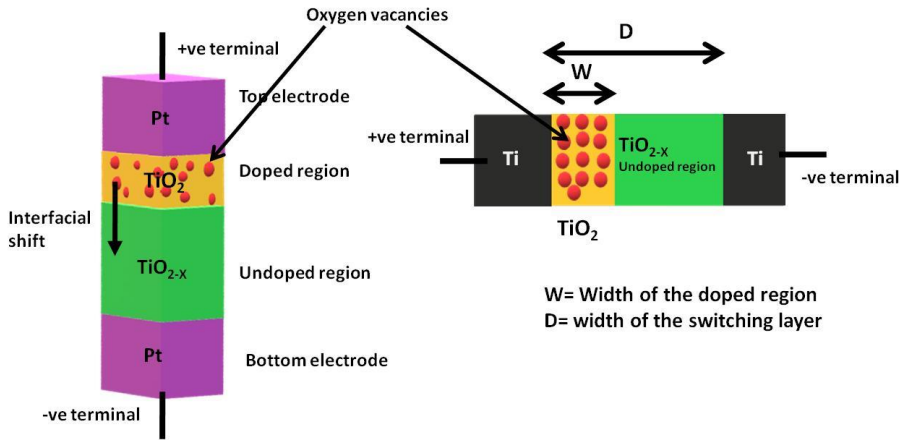

Figure 1.2 TiO_2 based memristor model presentation by HP Labs [16].

Then the proper supply is applied, ionic drift between the doped and consequently the undoped sections results in a change in the breadth of the doped zone. Here, the breadth of the doped region serves as a state variable.Additionally, the memristor enters a high resistance state as the width of the doped region gets closer to zero (HRS). The memristor enters a low resistance state as the doped region's width approaches a boundary (LRS). Because the memristor's dimensions are so small (nm), a change in the doped region can result from a low excitation in the supply. As a result, the memristor's resistance varies between HRS and LRS [17]. O_2^- ions are drawn to the lower electrode by negative bias electroforming, where they discharge to form O_2. The Magneli phase Ti_4O_7, which serves as a source/sink of oxygen vacancies in TiO_2, is the conducting channel thusly created. TiO_4 is a conductor, while TiO_2 is an insulator.Initial cell resistance is high (e.g., bit =0). Voltage causes TiO_4 to migrate, producing lower cell resistance. This state is stable when voltage removed. (e.g., bit =1). Reverse voltage cause TiO_4 to migrate back, causing higher cell resistance. This state is stable when voltage is removed. (e.g., bit =0).

The relationship between voltage, current, charge, and flux for the memristor is given by:

$$v(t) = M\big(q(t)\big)i(t) \qquad (1)$$

$$M(q) = \frac{d\varphi(q)}{dq} \qquad (2)$$

$$i(t) = W\big(\varphi(t)\big)v(t) \qquad (3)$$

$$W(\varphi) = \frac{dq(\varphi)}{d\varphi} \qquad (4)$$

where $W(\varphi)$ has the unit of conductance and $M(q)$ has the unit of resistance. When Equation (1) and (2) are analyzed, Equation (5) and (6) can be written as follows:

$$v(t) = M\left(\int_{-\infty}^{t} i(t)dt\right)i(t) \qquad (5)$$

$$i(t) = M\left(\int_{-\infty}^{t} v(t)dt\right)v(t) \qquad (6)$$

The memristor's current tells us something about its memristance value that is when the current flow through the memristor is off, the value of the memristance is retained, and when the current flow through the memristoris passed again, the value of the memristance changes from the lastretained value , i.e., before the cutoff.

This demonstrates the memristor's non-volatile property and also demonstrates that it is not an energy storage component [17, 18]. A resistor with memory is comparable to a memristor [19]. A memristor responds to a periodic bipolar signal by exhibiting a pinched hysteresis I-V characteristic that always crosses the origin.

As the frequency of the applied signal increases the pinched hysteresis loop shows the singled valued function and behaves as a linear resistor.

The pinched hysteresis loop behaves like a single-valued function when the frequency reaches infinity, similar to a resistor obeying Ohm's law[20, 21]. The scale limits of conventional electron storage-based memories have drawn a lot of attention to resistive random-access memory (RRAM)

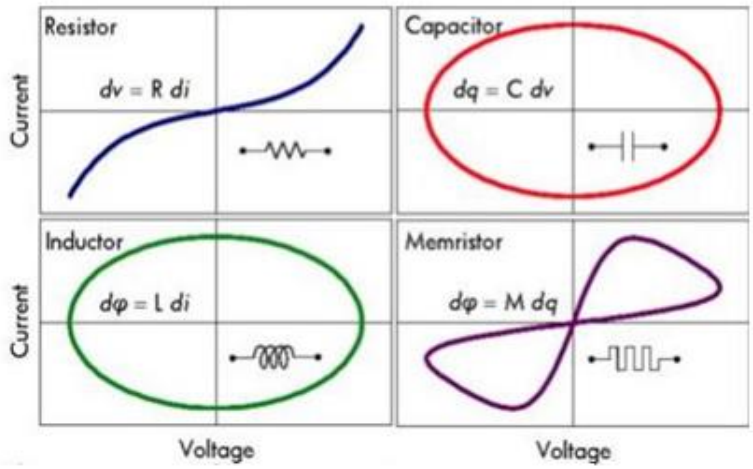

Figure 1.3 I-V Characteristics of four fundamental circuital elements [19].

or memristors [22–25]. Memristors can be divided into two categories based on their resistive switching mechanisms: filamentary-type and interfacial-type [24,26]. The filamentary-type memristor device exhibits a high switching speed as well as higher device scalability in comparison to interfacial-type memristor because it can be operated locally [26].However, the interfacial-type memristor is comparatively more suitable than the filamentary-type memristor to meet the desired requirements for the synaptic device [27]. Because the resistance change in the interfacial-type memristor results from electrochemical reactions between the reactive metal layer and resistive switching layer, it is extremely stable and analogue. The non-volatile memories must be evaluated differently from the resistive synaptic devices (NVMs). To implement the hardware for the neuro-inspired computing system, millions of resistive synaptic devices are necessarily required to integrate with other complementary metal oxide semiconductor (CMOS) device

components. Therefore, the device scalability is one of the most critical factors for hardware implementation. From the scalability point of view, the Y_2O_3-based synaptic device offers numerous advantages such as it is simple metal-insulator-metal (MIM) structure which can be highly stable and efficiently integrated into the crossbar array architecture.

Due to its unique and versatile qualities, memristors have a wide range of applications.

1. **Memory technology**: Memristors have great potential for used in memory devices, particularly as a form of non-volatile memory that can store data even when power is turned off . Unlike traditional memory devices, such as DRAM and flash memory, memristors do not require power to maintain their stored data.They are capable of being manufactured at smaller sizes, which can lead to higher storage densities . They alsohave faster read and write times than flash memory and can operate at lower power levels . Additionally, RRAMs have been shown to have a longer lifespan than traditional memory devices, meaning they can retain their data for longer periods of time.
2. **Neuromorphic computing**: The neuromorphic working of memristors is based on the idea of emulating the behavior of biological synapses, which are the connections between neurons in the brain . Synapses are capable of changing their strength over time, which is known as synaptic plasticity. This ability to change and adapt is a key feature of biological neural networks, and it is believed to be a key factor in the brain's ability to learn and process information . Memristors can be used to create artificial synapses that emulate this behavior by changing their resistance in response to the amount and direction of current that flows through them. This change in resistance can be used to modify the strength of the connection between two neurons in a neuromorphic circuit . In a

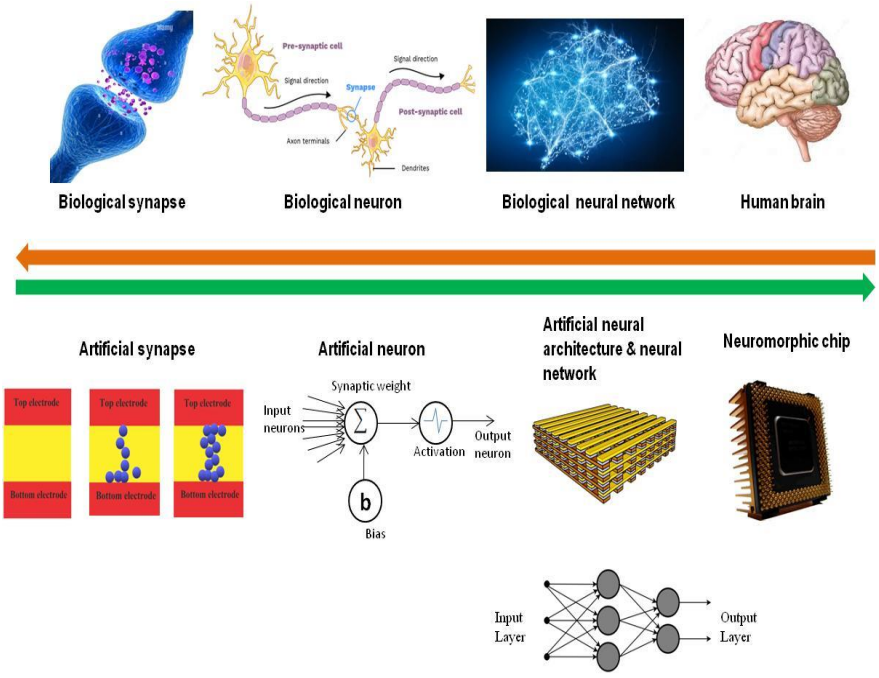

Figure 1.4 Schematic illustration of biological vs memristive crossbar based memristive system [20].

neuromorphic circuit, multiple memristors can be connected together to form a network of artificial synapses that can process information in a way that is similar to biological neural networks .

The strength of the connections between the memristors can be adjusted using various learning rules, which can be used to train the circuit to perform specific tasks. One advantage of using memristors in neuromorphic circuits is that they are capable of performing analog computations, which can be more efficient than the digital computations performed by traditional digital circuits. This is because analog circuits can perform computations in parallel, whereas digital circuits typically perform computations sequentially. Overall, the neuromorphic working of memristors holds great promise for creating artificial intelligence systems that are more efficient and adaptable than traditional digital systems. However, there is still much research that needs to be done to fully understand and optimize the performance of these systems.

3. **Internet of Things (IoT)**: Memristors can be used in IoT devices to enable the development of low-power, high performance computing systems that can operate in a variety of environments.
4. **Digital electronics**: Memristors can also be used in logic circuits , where they can be used to create new type of computational circuits that can perform calculations in a more efficient way than traditional digital circuits. One potential advantage of using memristors in digital electronics is that they can be made very small and can be integrated into existing semiconductor manufacturing processes, which makes them relatively easy to manufacture in large quantities However, there are still many challengesthat need to be overcome before memristors can be widely adopted in digital electronics, including issues related to reliability, power consumption, and compatibility with existing circuits. Overall, the potential applications of memristors are vast and exciting, making them a highly motivating area of research for scientists and engineers.

1.3 Organization

The first chapter of the introduction gives an outline of the technical difficulties that the current CMOS technology is currently facing due to the growing demand for high-capacity and inexpensive data storage. Memristors, non-transistor devices, have received substantial study as an alternative memory strategy.

In Chapter 2, we have discussed the analytical modeling, physical modeling and electrical characteristics for the Y_2O_3-based memristive crossbar array, in detail. Also, the detailed study of the memristive device having perturbations has also been done and the generated results are experimentally verified.

In Chapter 3, we have discussed the application point of view of the memristor in the digital circuit design by designing memristive based logic

gates, full adder, full subtractor and 2×1 Mux. Also, comparison of these circuits with respect to area, power and delay with the CMOS based designs has also been done in CADENCE Virtuoso at 90/180nm gpdk and reported.

In Chapter 4, Conclusion and Future Work.

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Chapter 2

Physical modeling of Y_2O_3 based memristor

2.1 Introduction

This chapter contains a detailed discussion of the physics and experimental demonstration of Y_2O_3-based memristors. A non-linear analytical memristive model that is already in existence and is based on the interfacial switching mechanism is fully explained in the first part [1,2]. By adding a Yttrium metal layer between the top electrode and the insulator layer for the same memristor model, we further researched and depicted the influence of the reservoir layer in memristors. Additionally, we looked into the internal electrical properties of yttrium-based and yttrium-less memristor models in the SET and RESET modules, including resistance, temperature, current, and filament radius. Furthermore, as the impact of a perturbation is essential in the manufacturing of a device, perturbations of different heights were evaluated independently and the relationship between current and voltage, ON to OFF current ratio ,internal electrical characteristics with all perturbation heights were studied and reported.

2.2 Analytical Model for Memristive Systems for Neuromorphic Computation

In the past one decade, several mathematical models [3,4, 5, 6] for memristor have been reported, as discussed in Table I. These reported models show their compatibility on various simulation platforms to perform the resistive switching response. Table I shows the comparative study between our proposed non-linear analytical memristor model [1] with other reported models [3, 4, 5, 6]. Here, equation (1) defines the

current-voltage (I-V) relationship of the proposed analytical model wherein several constants are used. Table II shows the numerical values and physical significance of the various parameters utilized in equation (1)

Table 1:Comparison between our model with other reported models

S.No	Model	State variable	Control Mechanism	Device Type	Simulation Compatible
1.	Linear drift [3]	0≤w≤D Dopedregion physical width	Current	Bipolar	SPICE
2.	Non-Linear ion drift [4]	0≤w≤1 Doped region normalised width	Voltage	Bipolar	No
3.	TEAM [5]	$x_{off}\leq x\leq x_{on}$	Current	Bipolar	Cadence Virtuoso
4.	Yakopcic [6]	0≤w≤1 Not explained physically	Voltage	Bipolar	SPICE/Verilog/MAPP
5.	Our Model [1]	0≤w≤1 Not explained physically	Voltage	Unipolar/Bipolar	Cadence Virtuoso

$$I(t) = \begin{cases} b_1 w^{a_1}\left(e^{\alpha_1 V_i(t)} - 1\right) + \chi\left(e^{\gamma V_i(t)} - 1\right), & V_i(t) \geqslant 0 \\ b_2 w^{a_2}\left(e^{\alpha_2 V_i(t)} - 1\right) + \chi\left(e^{\gamma V_i(t)} - 1\right), & V_i(t) < 0 \end{cases} \quad (1)$$

Here, first component on the right-hand side of equation (1)represents flux-controlled memristive behaviourwith interfacial switching

mechanism. While, the second term denotes the ideal diode behaviour in I-V characteristics and $V_i(t)$ is the applied input voltage.

Equation (2) describes a piecewise window function, *f(w),* that assures the state variable (w) is between 0 and 1. The range of parameter p sets the limit of the *f(w)*between 0 to 1, and if p>10, the upper value of the *f(w)* is more than 1 which clearly violates the essential conditions for window function, as reported by Prodromakis *et al*[7].

$$f(w) = \log\begin{Bmatrix}(1+w)^p,\ 0 \le w \le 0.1\\ (1.1)^p,\ 0.1 < w \le 0.9\\ (2-w)^p,\ 0.9 < w \le 1\end{Bmatrix} \quad (2)$$

Table 2: Physical interpretation and numerical values of parameters used in modeling.

Parameters	**Numerical Values**	**Physical Interpretation**
b_1	1.59×10^{-3}	Experimental fitting parameters
b_2	-6.2×10^{-4}	
a_1	1.2	Degree of influence of state variable under positive bias
a_2	0.3	Degree of influence of state variable under negative bias
α_1	0.60	Hysteresis loop area controlling parameters underpositive bias
α_2	-0.68	Hysteresis loop area controlling parameters undernegative bias
χ	1×10^{-11}	Magnitude of ideal diode behavior

A	5×10^{-4}	Control the effect of the window function
m	5	Control the effect of input on the state variable
p	2 $(0 < p \leq 10)$	Bounding parameter for window function between 0 and 1
γ	1	Diode parameters like thermal voltage and ideality factor

The time derivative of the state variable *w(t)* is represented by the equation (3) which is also dependent on the nature of input voltage and window function.

$$\frac{d\square}{dt} = A \times v_i^m(t) \times f(w) \quad (3)$$

From equation (3) it is cleared that constants A and m are the two independent variables which affect the time derivative of the state variable. To ensure that the opposite polarity of the applied voltage results in the opposite change in the rate of change of the state variable whereinparameter m must always be an odd number. Most importantly,the previously described models [7, 8] are dominated for bipolar memristive system while our proposed memristor model is well suitable to both unipolar and bipolar memristive systems.

2.3 Boundary Conditions

The boundary conditions that we used in our model is listed below.

1. **Electric Insulation (n.J = 0)**

   The SiO2 domain has three electrically insulated boundaries. The unit vector normal to the surface boundary in this case is n.

2. **Ground (V = 0)**

   The interface common to the bottom electrode and SiO_2 substrate is grounded.

3. **Terminal ($V = V_D$ or $I = I_S$)**

A load resistor is linked in series with the interface common to the power source and the top electrode.

4. **Temperature (T = 298 K)**

   It is assumed that the free surfaces of both SiO_2 layers are in touch with a bigger body that serves as a heat sink and maintains a constant temperature of ambient temperature. Additionally, the air domain's three limits are all at room temperature.

5. **Diffuse Surface (n.q = σB($T_{amb}^4 - T^4$))**

   According to Stefan-Boltzmann law, heat is lost through radiation from the entire device interface. Here q is the power radiated per surface area, σB is the Stefan-Boltzmann constant, and Tamb is the ambient temperature (298 K).

2.4 Analysis of the Physical Electro-Thermal Modeling (Yttriumless model)

The memristor's 2-D axisymmetric model is depicted in figure (2), whereas figure 2.1(a) and figure 2.1(b) respectively show the device's physical model in the RESET and SET regions. The 2D geometry of the memristive device in COMSOL allows for the conversion of the volume integrals to the area integrals..

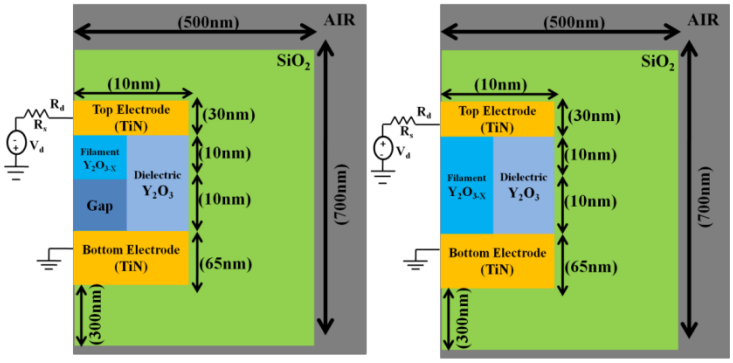


Figure 2.1: (a) 2D structure of memristive device under RESET/OFF operation (b) 2D structure of memristive device under SET/ON operation.For yttriumless device.

The computed device structure has a cross-sectional area of 314 nm^2. As seen in Figure 2.1, a thick layer of SiO2 is employed as the insulating layer, with a width of 500 nm and top and bottom thicknesses of 300 nm. When a memristor device is turned on, the thick layer of SiO_2 works as a heat shield layer, preventing uncontrolled heat transmission from the device to the ambient environment (i.e., air) [9]. The passivation layer's support in helping to keep the area around the device at a constant temperature enables the device's reliable resistive switching response [10]. The top electrode (TE) is 30 nm thick, the switching layer (Y_2O_3) is 15 nm thick, and the bottom electrode (BE) is 65 nm thick. The total effective thickness of the memristor device is 110 nm.

The switching phenomena in SET operation typically involves two processes:

Formation of filament between the electrodes.

- Nucleation and
- Longitudinal growth of CFs due to their probabilistic nature [11]
- Radial development of Conducting Filament.

Similarly, The switching phenomena in RESET operation typically involves two processes:

- Denucleation of the CF and
- Growth of the gap (or rupturing of the CFs). Nature of the growth of the gap is also of stochastic nature [11].

2.4.1 Multiphysics module

2.4.1.1 COMSOL images of yttriumless model in SET module

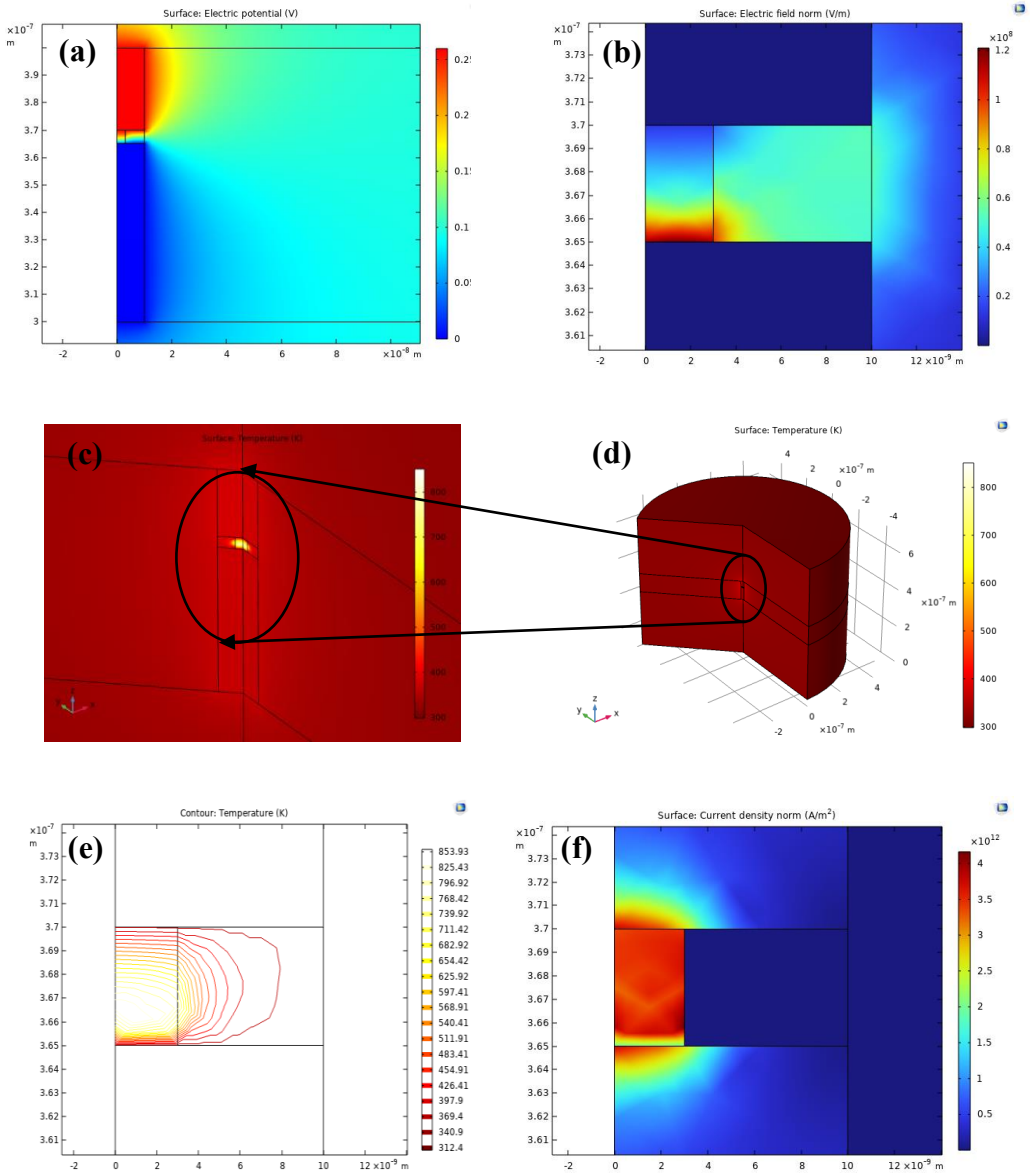


Figure 2.2: (a) 2-D electric potential plot (b)2-D electric field plot (c)Magnified image of 3-D temperature plot (d) 3-D temperature plot (e) 2-D surface current density plot (f) Temperature contopur plot . For the SET process of yttriumless model

2.4.1.2 COMSOL images of yttriumless model in RESET module

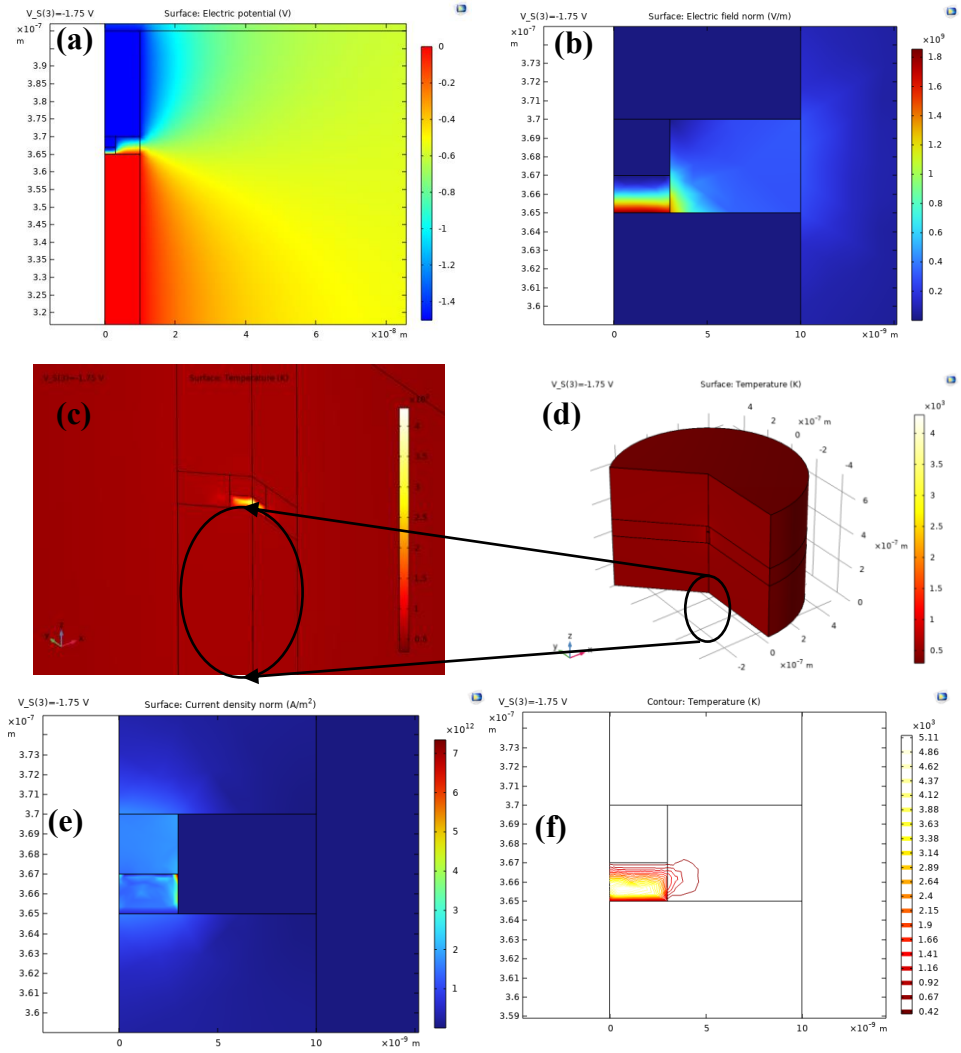


Figure 2.3: (a) 2-D electric potential plot (b)2-D electric field plot(c)Magnified image of 3-D temperature plot (d) 3-D temperature plot (e) 2-D surface current density plot (f) Temperature contopur plot . For the RESET process of yttriumless model.

2.5 Analysis of the Physical Electro-Thermal Modeling (Yttrium based model)

Figure 2.4 below shows the use of a layer of SiO_2 as thermal insulation around the memristor device to shield it from the outside environment and the incorporation of a 10 nm yttrium metal between the top electrode and the insulator (Y_2O_3) to enhance the memristor's performance by forming a stable conductive filament during the SET process.

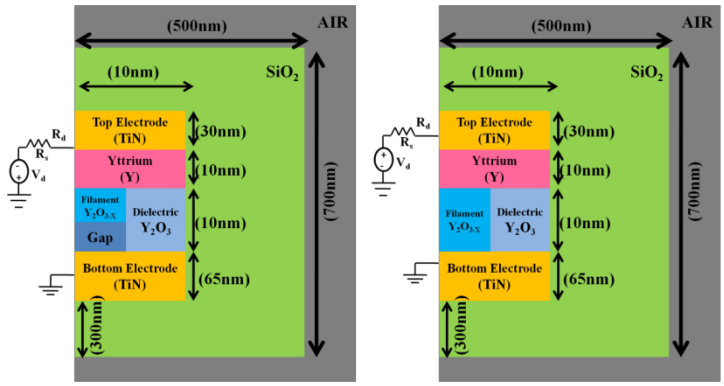
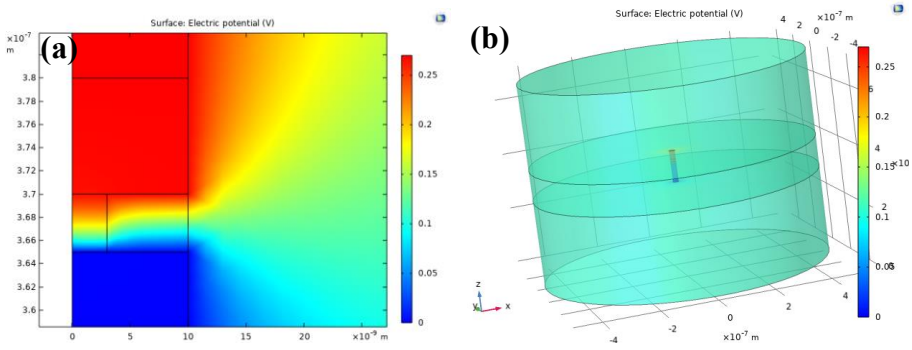


Figure 2.4: (a) 2D structure of memristive device under RESET/OFF operation (b) 2D structure of memristive device under SET/ON operation. For yttrium based model.

2.5.1 Multiphysics Module

2.5.1.1 COMSOL images of yttrium based model in SET module



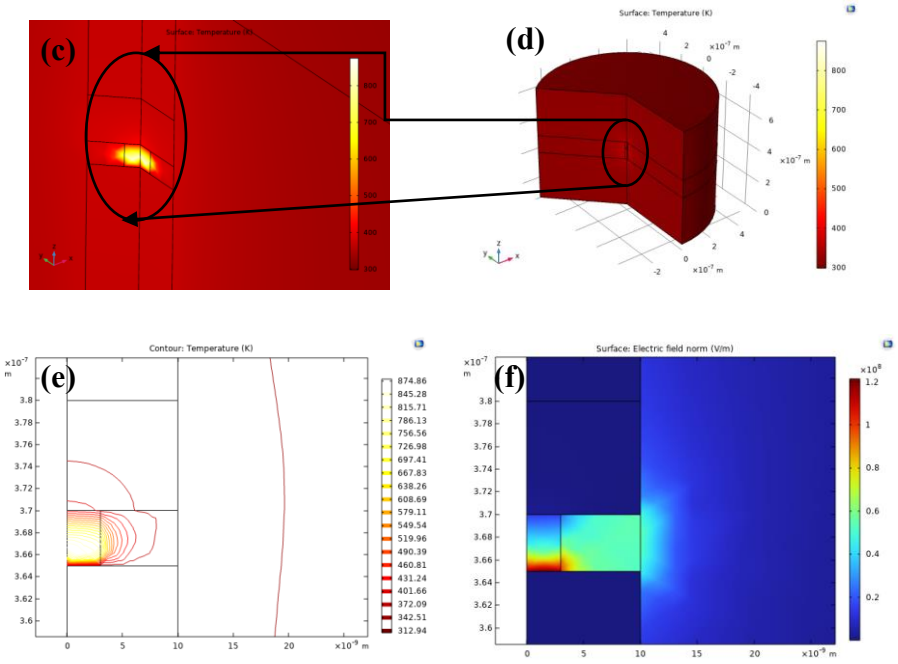
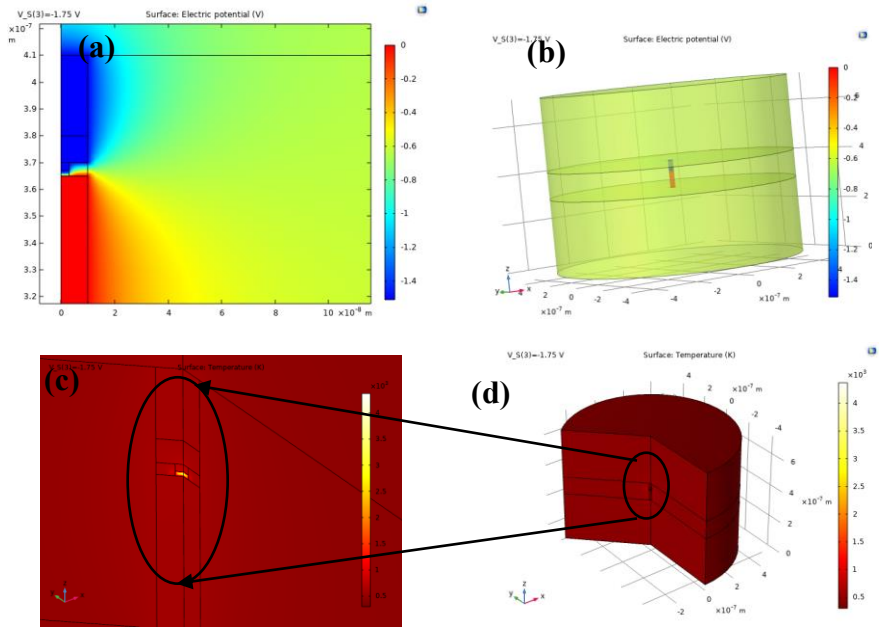


Figure 2.5: (a) 2-D electric potential plot (b)3-D electric field plot (c)Magnified image of 3-D temperature plot (d) 3-D temperature plot (e) Temperature contopur plot (f) 2-D Electric field plot . For the SET process of yttrium based model.

2.5.1.2 COMSOL images of yttrium based model in RESETmodule



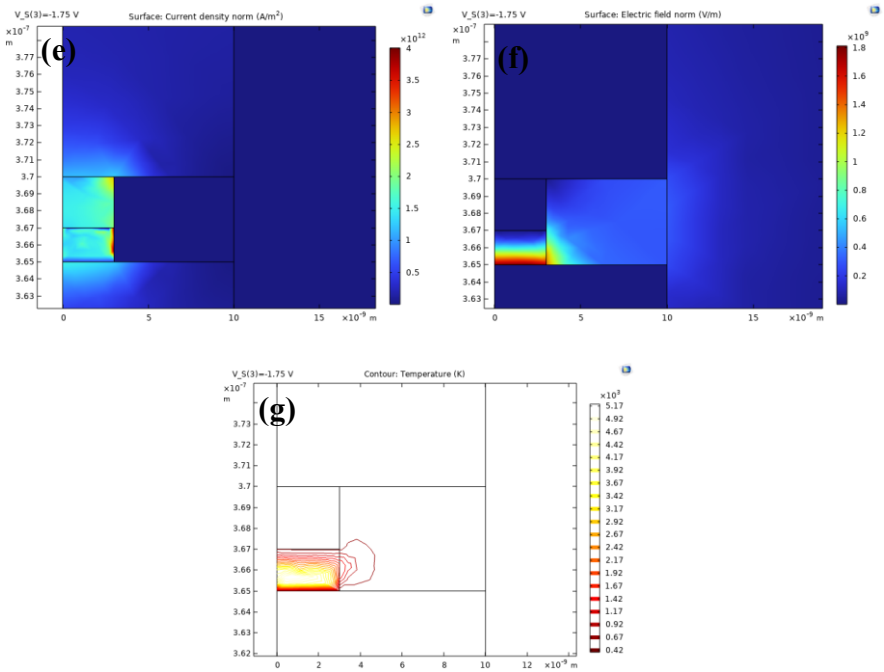


Figure 2.6: (a) 2-D electric potential plot (b)2-D electric field plot (c)Magnified image of 3-D temperature plot (d) 3-D temperature plot (e) 2-D surface current density plot (f) Temperature contopur plot . For the RESET process of yttriumless model.

2.6 Effect of perturbations on Memristor model

Perturbation or surface irregularities in a memristor refers to the introduction of small variations or disturbances in the current or voltage applied to the device. These perturbations can cause changes in the state of the memristor, such as altering its resistance or causing it to switch between different states. Surface irregularities in a memristor can arise from defects in the manufacturing process or due to changes in the device during use. These irregularities can affect the performance and reliability of the device, such as causing variations in the resistance values or leading to premature failure. It can occur due to multiple reasons like:

1. ***Lattice Mismatch:*** When different materials are formed on top of one another, there is a boundary zone where the two crystal

structures come into contact. The mismatched atomic positions at the crystal boundaries can create strain, which can lead to cracks or dislocations spreading throughout the structure if the lattice constants are sufficiently divergent. It can be disastrous for the active region if the meticulously constructed superlattice, which defines the quantum structure, is broken.

2. ***Growth rate:***It refers to the rate at which a particular layer of material is deposited onto a substrate to form the desired structure. The growth rate can be controlled by various process parameters such as temperature, pressure, and gas flow rate. The growth rate in fabrication is an important parameter to control because it can affect the properties and quality of the final product. For instance, if the growth rate is too slow or too fast, it can lead to defects or non-uniformities in the material, which can negatively impact the performance of the device. Therefore, optimizing the growth rate is an important aspect of the fabrication process to ensure that the final product meets the desired specifications.
3. ***Incomplete penetration:***It refers to a welding defect that occurs when the weld metal does not penetrate through the joint or base metal completely. In other words, the weld metal does not reach the root of the joint, leaving a gap or void that can weaken the strength of the weld. This defect can occur due to a variety of reasons such as improper welding technique, insufficient heat input, incorrect welding parameters, or poor fit-up of the joint. Incomplete penetration can also occur when the joint is too thick for a single pass welding or when the joint preparation is inadequate. Incomplete penetration is considered a serious welding defect because it can compromise the structural integrity of the welded component, leading to failure under stress or load. Therefore, it is important to ensure proper welding technique and parameters, as

well as appropriate joint preparation and fit-up, to avoid incomplete penetration in the fabrication process.

4. ***Unavailability of clean environment:*** The unavailability of a clean environment in fabrication can have a significant impact on the quality and reliability of the final product. In a fabrication process, a clean environment is necessary to prevent contamination of the materials and components being fabricated. Contamination can occur in various forms such as dust, particles, chemicals, or microorganisms, and can lead to defects or failures in the final product.

2.6.1 Ways to reduce perturbations during fabrication

To mitigate surface irregularities, researchers are exploring new materials and fabrication techniques to improve the quality and uniformity of the memristor surface. Additionally, advanced testing methods can help identify and characterize surface irregularities, enabling manufacturers to produce more consistent and reliable devices. Overall, addressing surface irregularities in memristors is an important research area for improving the performance and reliability of these devices in various applications.

There are many ways to reduce the surface roughness of any material during device fabrication but the major step supported by our research team was to fabricate Y_2O_3 based memristive device for neuromorphic application using the **Dual Ion Beam Sputtering (DIBS) system** thatoffers plenty of advantages compared to other conventional sputtering techniques, such as high-quality thin films with better compositional stoichiometry, small surface roughness, and good adhesion to the substrate. Other methods to improve the surface quality includes

- Subtractive method

- Additive post – treatment

In the subtractive approach, surface roughness is minimised by physically removing the material from the device, but in the additive post-treatment, the object is coated to reduce surface roughness. In comparison to subtractive post-treatments, additive post-treatments provide a number of benefits.First off, since no material from the original product is removed during additive post-treatments, mechanical qualities remain unaffected. Second, coatings can be applied without making direct contact between the coating device and the object, whereas applying a subtractive post-treatment to complex geometries might be extremely time-consuming or even impossible.However, the additive manufactured (AM) item receives a large increase in size due to the high amount of material that is appliedduring additive post-treatments employing modern coating technologies. Additionally, it's crucial to take into account the coating's adhesion to the AM surface when applying additive post-treatment techniques.

2.7 2-D structure of memristor model with perturbations

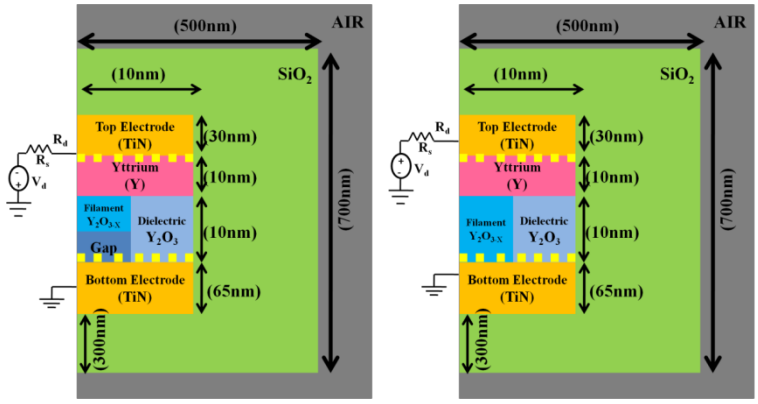


Figure 2.7: (a) 2D structure of memristive device under RESET/OFF operation (b) 2D structure of memristive device under SET/ON operation.

In this work, memristor characteristics are explored with different perturbation heights 0.1nm, 0.2nm, 0.5nm, 1.0nm, 1.5nm that are introduced both in the top and the bottom electrode. Here, the perturbation

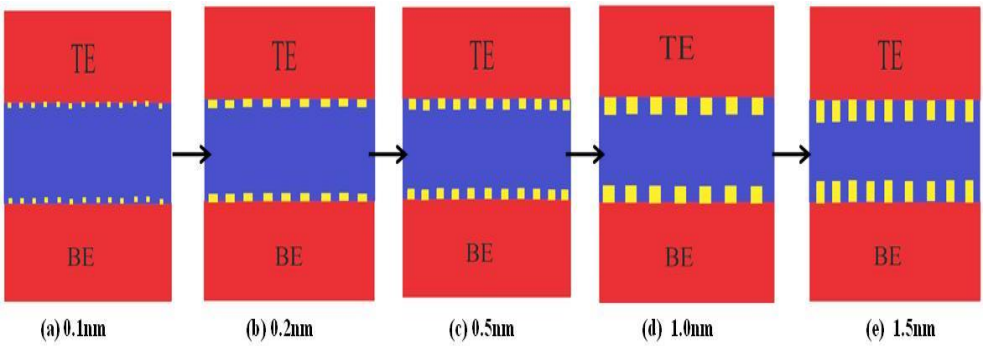


Figure 2.8: Memristive device under (a) 0.1nm perturbation (b) 0.2nm perturbation (c) 0.5nm perturbation (d) 1.0nm perturbation (e) 1.5nm perturbation

height is kept constant throughout a particular case. As long as this perturbation height is small it does not create a major effect but as as soon as this height starts increasing it starts giving a negative impact on the memristive device. It will lead to electrode degradation of the memristor or can lead to formation of non uniform electric field that can increase the variability in the switching characteristics of the memristor.

2.8 Result and Discussion

2.8.1 Analysis for the yttriumless model in SET module

Figure 2.3(a) displays the fluctuation in filament radius as a function of device current during the SET region. As the supply voltage is raised, more oxygen carriers begin to flow from the bottom electrode to the top electrode, increasing the device current as seen in figure 2.3(c). The filament's radius thereafter starts to increase as a result. Figure 2.3(a) illustrates how resistance in the entire device starts to drop as filament

radius rises. Similarly, resistance is inversely correlated to device current, so as current rises, resistance falls. Finally, as the supply voltage rises, more carriers are now travelling; as a result, the filament's carrier concentration rises and the temperature of the filament rises, as illustrated in figure 2.3(d).

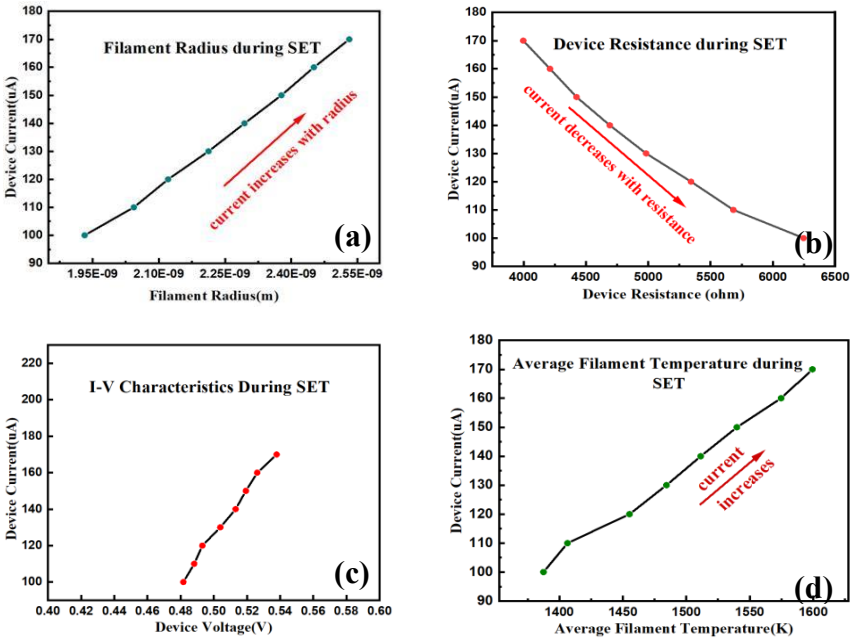


Figure 2.9:(a) Filament radius during SET region (b) Device resistance during SET region (c) I-V characteristics during SET region (d) Average filament Temperature during SET region .

2.8.2 Analysis for the yttriumless model in RESET module

Figure 2.5(a) shows the relationship between device current and device voltage. Oxygen vacancies start to drop to the bottom electrode when the device's negative bias supply voltage is increased, but current still flows just in the opposite direction and at a much loweramplitude than the original supplied voltage supply, as seen in figure 2.5(a) despite this.

Further, as vacancies begin to reappear, the filament channel begins to break and the gap width increases. As a result, more voltage is needed to

flow the current, which raises both the temperature and the disturbance across carriers, as shown in figures 2.5(c) and 2.5(b), respectively. Figure 2.5(d) illustrates the resistance variation that increases with supply voltage, indicating a decrease in overall current.

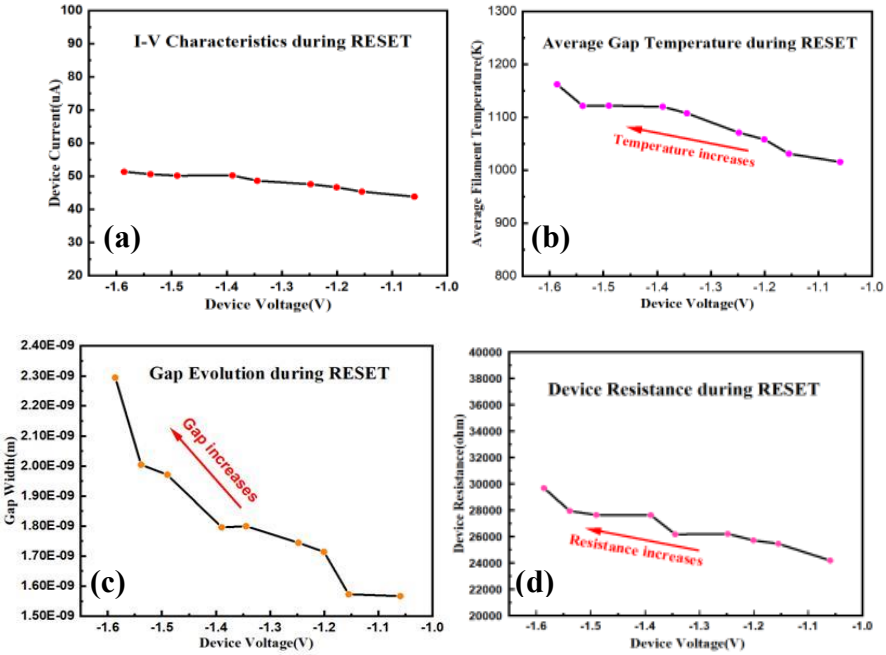


Figure 2.10: (a) I-V characteristics during RESET region (c) Average gap temperature during RESET region (d) Gap evolution during RESET region (e) Device resistance during RESET region

2.8.3 Analysis for the yttrium based model in SET module

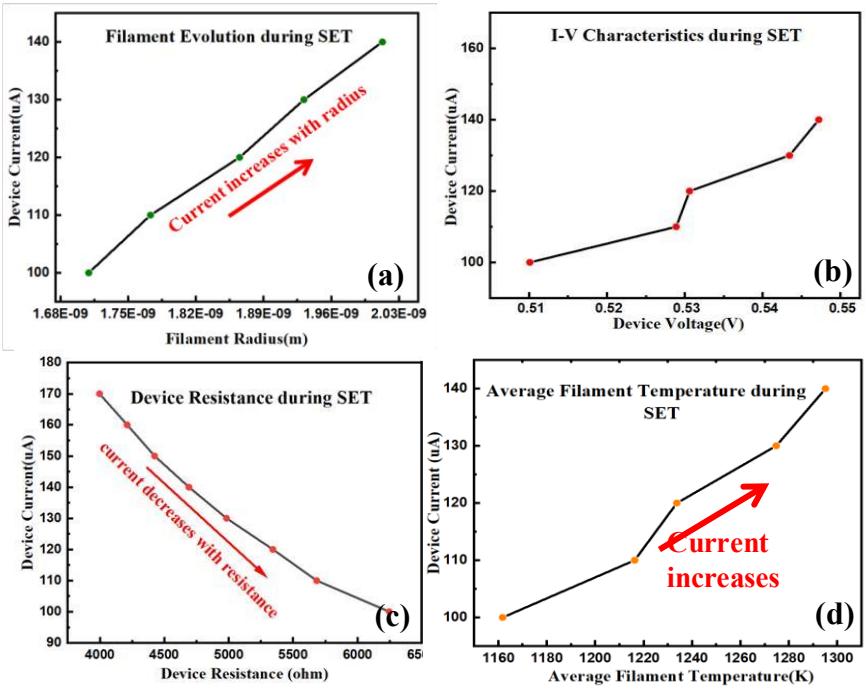


Figure 2.11: (a) Filament radius during SET region (b) Device resistance during SET region (c) I-V characteristics during SET region (d) Average filament Temperature during SET region

2.8.4 Analysis for the yttrium based model in RESET module

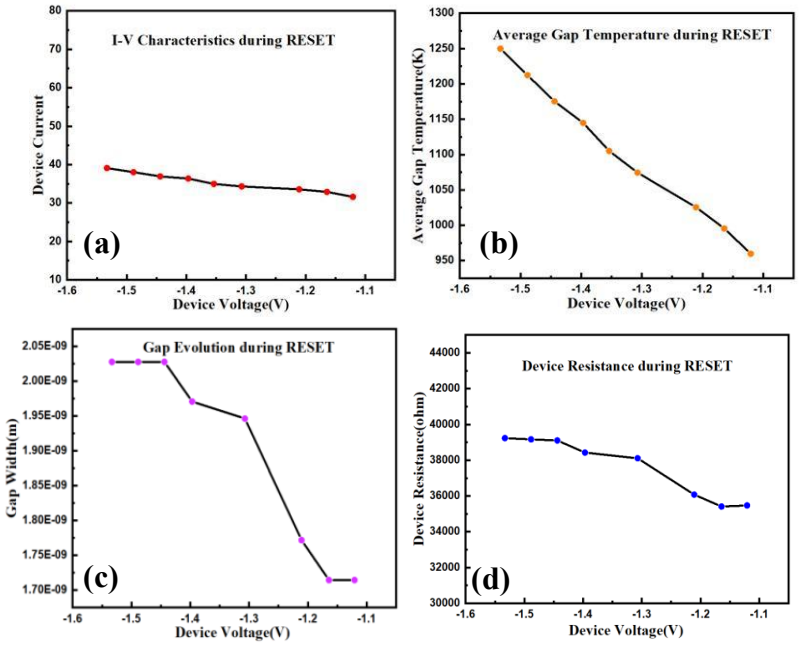


Figure 2.12: (a) I-V characteristics during RESET region (b) Average gap temperature during RESET region (c) Gap evolution during RESET region (d) Device resistance during RESET region

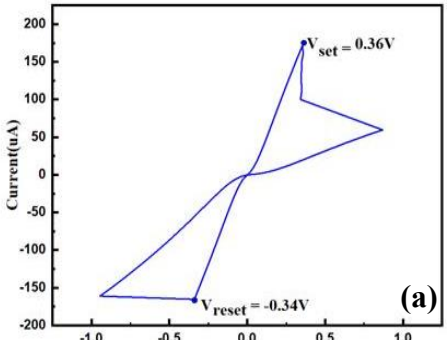
2.9 Electrical comparison between yttrium and yttriumless model

Table 3:Electrical Comarison between yttrium and yttriumless memristor models in SET and RESET region

Region	Parameter	Yttriumless	With Yttrium
SET	Switching voltage	HIGH	LOW
	Device temperature	HIGH	LOW
	Device resistance	HIGH	LOW

	Filament radius	LOW	HIGH
RESET	Gap temperature	LOW	HIGH
	Device resistance	LOW	HIGH
	Gap width	LOW	HIGH

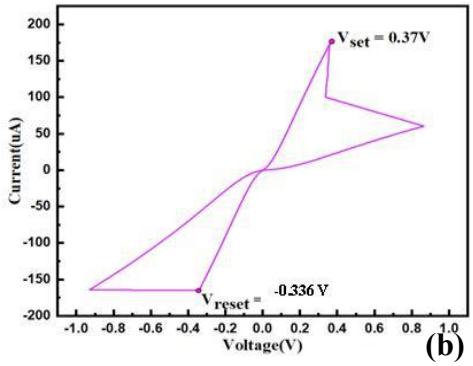
2.9.1 Result and Discussion



I_{on}/I_{off} ratio:

$$\frac{I_{on}}{I_{off}} \qquad \frac{Current\ at\ V_{on}}{Current\ at\ V_{off}}$$

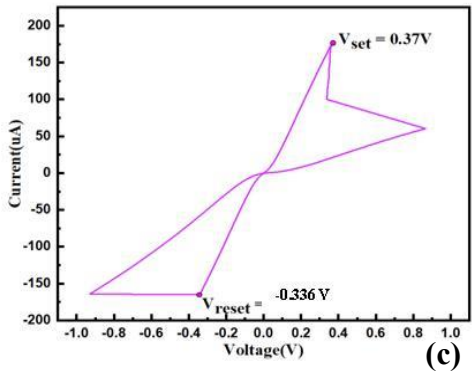
Here, $\left|\frac{I_{on}}{I_{off}}\right| = 8.865$



I_{on}/I_{off} ratio:

Here,

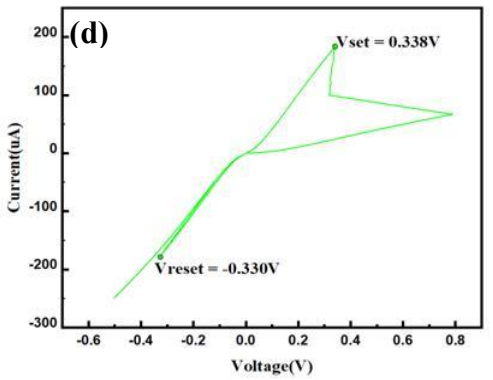
$$\left|\frac{I_{on}}{I_{off}}\right| = 8.422$$



I_{on}/I_{off} ratio:

Here,

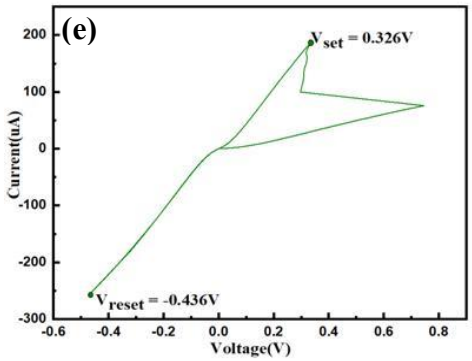
$$\left|\frac{I_{on}}{I_{off}}\right| = 8.422$$



I_{on}/I_{off} ratio:

Here,

$$\left|\frac{I_{on}}{I_{off}}\right| = 7.55$$



I_{on}/I_{off} ratio:

Here,

$$\left|\frac{I_{on}}{I_{off}}\right| = 6.55$$

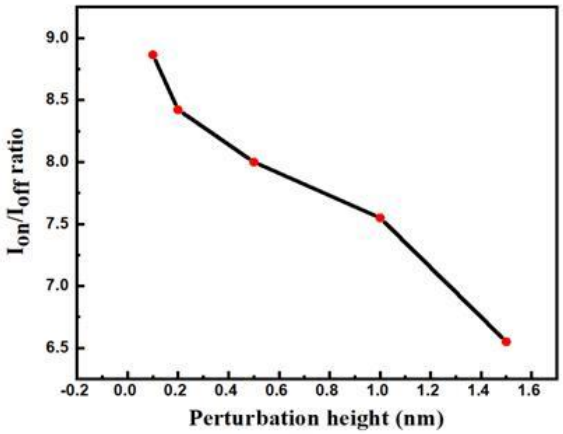


Figure 2.13: I-V Characteristics for (a) 0.1nm, (b) 0.2nm, (c) 0.5nm, (d) 1.0nm and (e) 1.5nm perturbations (f)Resultant Ion/Ioff ratio for all the perturbations.

The on-to-off current ratio of a memristor refers to the ratio of the maximum current that can be conducted through the memristor when it is in the on-state to the minimum current that flows through the memristor when it is in the off-state. This ratio is an important parameter that can have a significant impact on the performance of memristive devices and influences the type of application they can be useful.

A higher on-to-off current ratio is generally desirable as it allows for a more reliable and efficient operation of the device. Specifically, a higher on-to-off current ratio can lead to better device stability, improved signal-to-noise ratio, and reduced power consumption.A higher on to off current ratio is desirable for digital type of compution whereas lower ratio is suitable for analog computing.

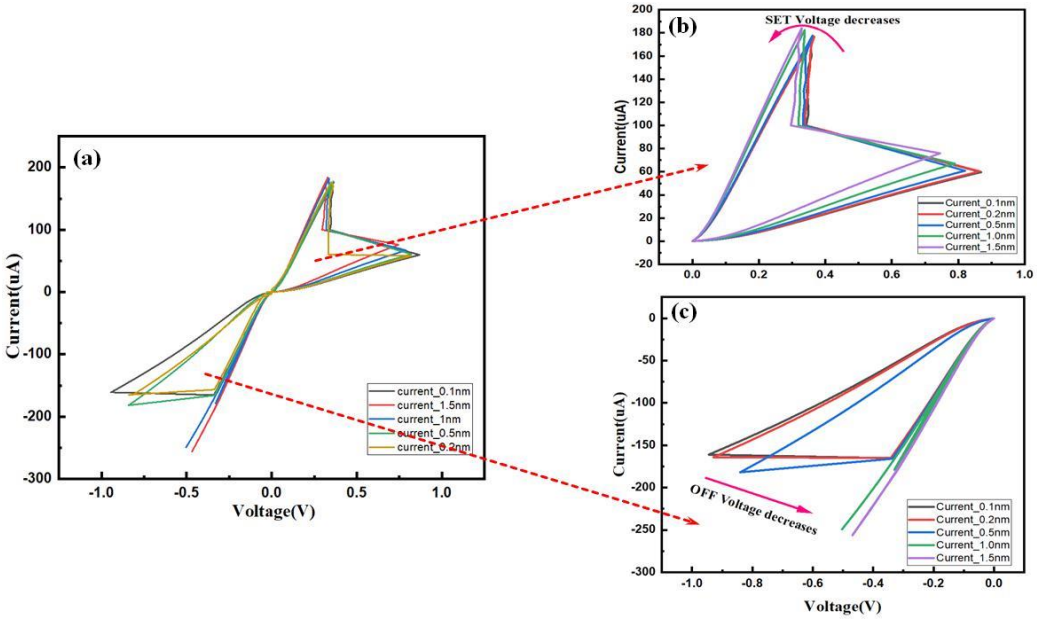


Figure 2.14: (a) Combined perturbations I-V Characteristics (b) I-V Characteristics for positive bias (c) I-V Characteristics for negative bias

With increase in perturbation height the distance between the top and the bottom electrode decreases and hence it takes less time for the carriers to do the migration.Therefore , the switching voltages decreases with increase in perturbation height i.e. set voltage and reset voltage requirement decreases.

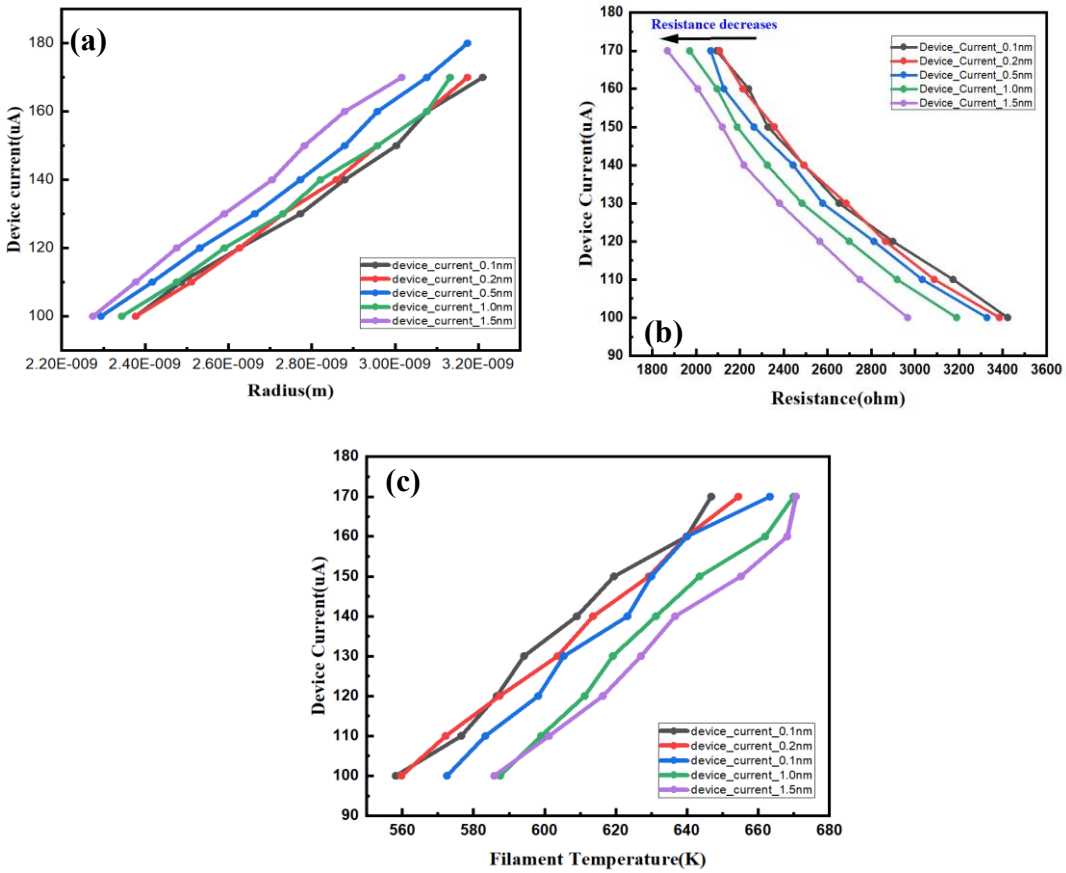


Figure 2.15 (a) Filament radius variation with device current (b) Resistance variation with device current (c)Average filament Temperature variation with device current

We have already seen the variation of radius , resitance and Temperature variation in the above section 2.4.1. With the introduction of perturbations we see that filament radius decreases as switching voltage decreases and we get the maximum current at lower voltages. Similarly, resistance and temperature of the device with maximum perturbation height is the minimum and maximum respectively.

2.10 References:

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Chapter 3

Logic circuit Implementation via Memristor

3.1 Introduction

Compact low-power devices with ultra-fast processing speed are the fundamental building blocks for the development of state-of-the-art system and memristor prominently fulfill these demands and plays a major role in digital circuit design. In this work, design, implementation, and performance evaluation of memristor-based logic gates such as NOT, AND, NAND, OR, NOR, X-OR and X-NOR, and combinational logic circuits such as adder, subtractor, and 2×1 mux are presented via SPECTRE in Cadence Virtuoso. Herein, we propose an optimized design of memristor-based logic gates and combinational logic circuits and draw a comparative study with the conventional 180-nm CMOS technology. The utilized memristor model is thoroughly validated with experimental results of a high-density Y_2O_3-based memristive crossbar array (MCA) which shows a significantly low values of coefficient of variabilities in device-to-device (D2D) and cycle-to-cycle (C2C) operation. The adopted memristor-based methodology significantly improves the performance of various logic designs which makes it area and power efficient and enables the major breakthrough in the designing of various low-power, low-cost, ultrafast and compact circuits.

3.2 Background

In the past several decades, complementary metal oxide semiconductor (CMOS) technology has led to digital electronics design and implement various digital circuits to perform logic operations [1]. However, over the period of time the CMOS technology has suffered from diverse challenges in terms of usage of large chip area, high power consumption, and low

data processing speed leading to the saturation of scaling and device performance [2]. Also, CMOS-based logic circuits suffer from high leakage power consumption which further reduces the device reliability [2]. The nanoscale memristors have the remarkable potential to overcome these limitations with their high scalability [3], high operating speed [4], high density in crossbar array architecture [4], and non-volatile nature [5]. Therefore, the capability of memristive devices can pave a new path for future computer technology wherein it may instantaneously flip ON and OFF without loss of data and also reduces the boot time of the system. On the other hand, the physical limitations of the current CMOS transistor push back the chip size and density due to scaling effects while memristive technology is already on the edge to hit those barriers effectively [6]. The memristor technology offers computing via vector-matrix multiplication in resource-intensive applications with low power consumption [7], high storage capability due to remarkable scaling ability [4, 8], fast processing speed [4], and ability to compute new logic patterns for computers. In this work, several logic gates such as NOT, AND, NAND, OR, NOR, X-OR, and X-NOR and combinational logic circuits such as 2×1 mux, full adder, and full subtractor have been designed and implemented using industrystandard Verilog-A coding in the Cadence Virtuoso platform. Herein, a non-linear analytical memristor model [9] is used to implement logic circuits as mentioned above. The utilized memristor model is thoroughly validated by the experimental results of Y_2O_3-based single memristor and memristive crossbar arrays (MCAs) that display stable switching response with ultralow values of device-to-device (D2D) and cycle-to-cycle (C2C) variability parameters [10].

3.3 Method of Implementation

The memristor model discussed in the chapter 2 is used to create the memristor symbol whose verilog–A code was first written in the Cadence

Virtuoso and then using that symbol logic circuits were implemented in 180nm and 90nm gpdk. For creating the circuit following steps were taken:

1. Create a new library and then new cell fron the file menu .
2. Add symbol of the memristor (whose verilog-A code was first written in cadence) and NMOS by choosing from their respective library after pressing 'I' (instance) anywhere on the screen .
3. Similarly add input pulse voltage, V_{DD} and ground from the 'analog' library.
4. Connect all the symbols using a wire.
5. Save the circuit by pressing 'shift +X'.
6. For output analysis, choose 'ADEL' from the 'analysis' option.
7. In the ADEL window now choose 'Transient analysis' and drop the value of time for which you have to observe the output.
8. In the output section add the axes about which you want to make the graph.
9. Press the play button .

Fig. 1 shows the implemented logic gates such as NOT (Figure 3.1(a)), AND (Figure 3.1(b)), NAND (Figure3.1(c)), NOR (Figure3.1 (d)), OR (Figure 3.1(e)), X-OR (Figure 3.1(f)) and X-NOR (Figure3.1(g)). As seen from Figure 3.1, one terminal of the memristor is connected to a DC voltage source i.e., V_{dd}, and V_{IN} and V_{OUT} are referred to as the input and output voltage signals, respectively. Here, it should be noted that when V_{IN} = 1 (high input voltage), the transistor turns "ON", and the memristor is in "SET" condition with $R_M = R_{ON}$. At the same time, NMOS is in saturation mode wherein the "ON" resistance R_T is near equal to 0.

On the other hand, when V_{IN} = 0 (low input voltage), the transistor is in "cut-off" region, but the memristor holds the previous resistance value and hence, the V_{OUT} is near equal to '1' followed by some voltage drop across the memristor [7]. For the NAND logic operation, the output is '0'

whenever both serially connected transistors are in “ON” condition and while in the case of NOR gate operation, the output becomes ‘1’ whenever both transistors are in “OFF” state. The similar logic operations are also followed in the case of AND, OR, X-OR and X-NOR logic gates. In this proposed work, the memristor acts as a variable resistor that has the ability to program, store and retain the previous input pattern and provide an output that is the function of current and past stored values. Here, an n-type metal oxide semiconductor (NMOS) transistor acts as a switch. The NMOS transistors can control the memristor’s resistance which further extends the use of memristor in programmable logic circuits to implement the power-efficient circuitries for signal processing [11], pattern recognition [12], and neural network applications [6]. By considering the aforementioned logic circuits, various combinational logic circuits such as full adder, full subtractor, and a multiplexer can also be implemented which consume less space, power, and time to perform the desired Here, Figure 3.2 shows the combinational logic circuits such as full adder (Figure 3.2(a)), full subtractor (Figure 3.2(b)), and 2×1 multiplexer (mux) (Figure 3.2(c)).

3.4 Result and Discussion

To design, implement and evaluate the memristor-based and traditional CMOS-based logic circuits, the industry-standard Cadence Virtuoso platform (gpdk 180 nm) is utilized with an identical set of input voltages wherein two different pulses with the same time period but different duty cycles. The identical set of input voltages ensures the correct functionality of all logic circuits with the same level of supply voltage i.e., 1 V. Here, Figure 3.3 shows the transient output responses of the memristor-based various logic circuits such as AND, OR, NAND, NOR, X-OR, and XNOR gates (Figure 3.3(a)), NOT gate (Figure 3.3(b)), and full adder and full subtractor (Figure 3.3(c)). Additionally, proposed memristor model is also

fully capable to perform the 2×1 mux logic operation, and output transient response is depicted in Figure 3.4.

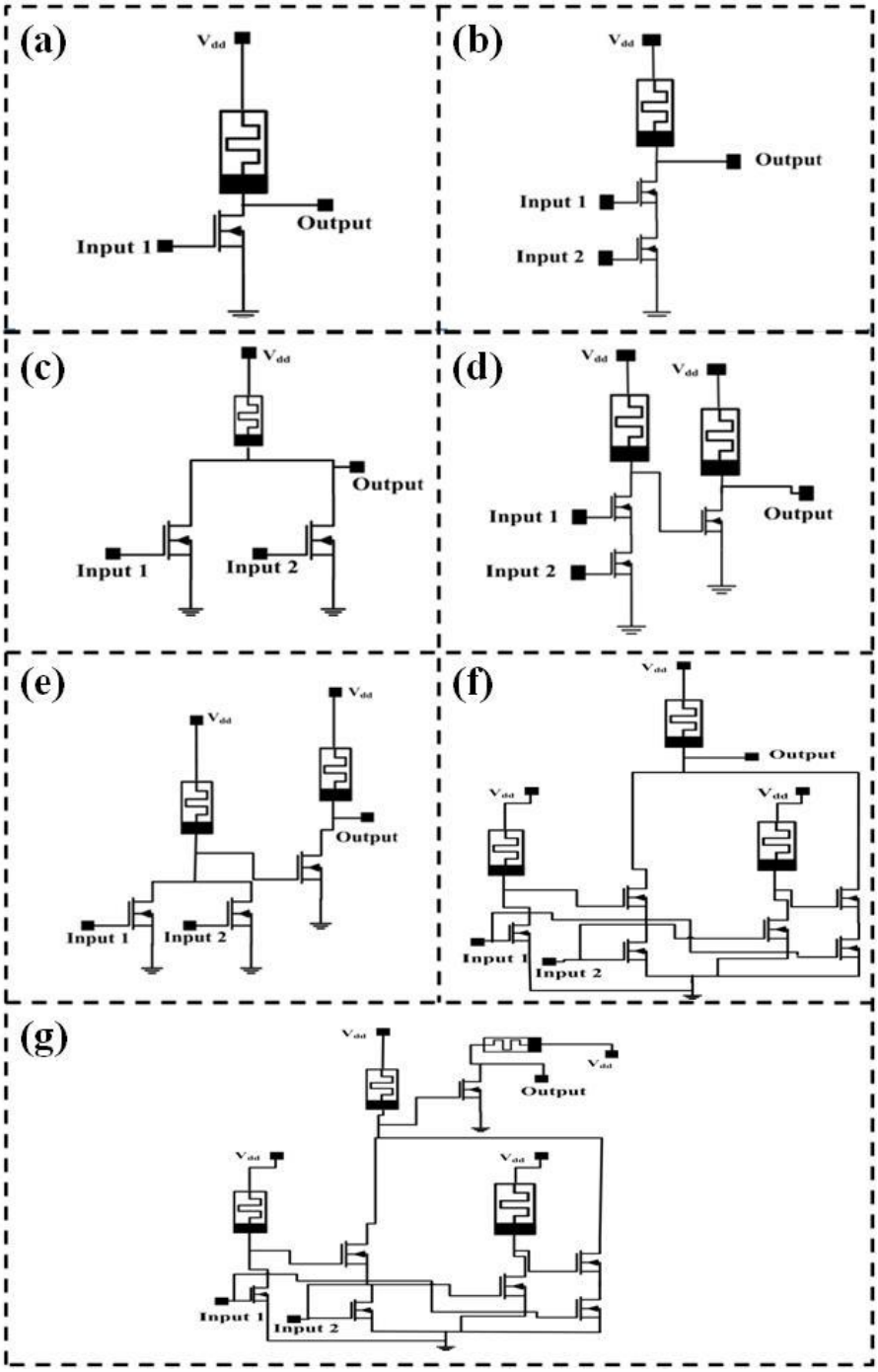

Figure 3.1 : Schematic diagram for (a) NOT gate, (b) NAND gate, (c)NOR gate, (d) AND gate ,(e) OR gate, (f) X-NOR gate and (g) X-OR gate

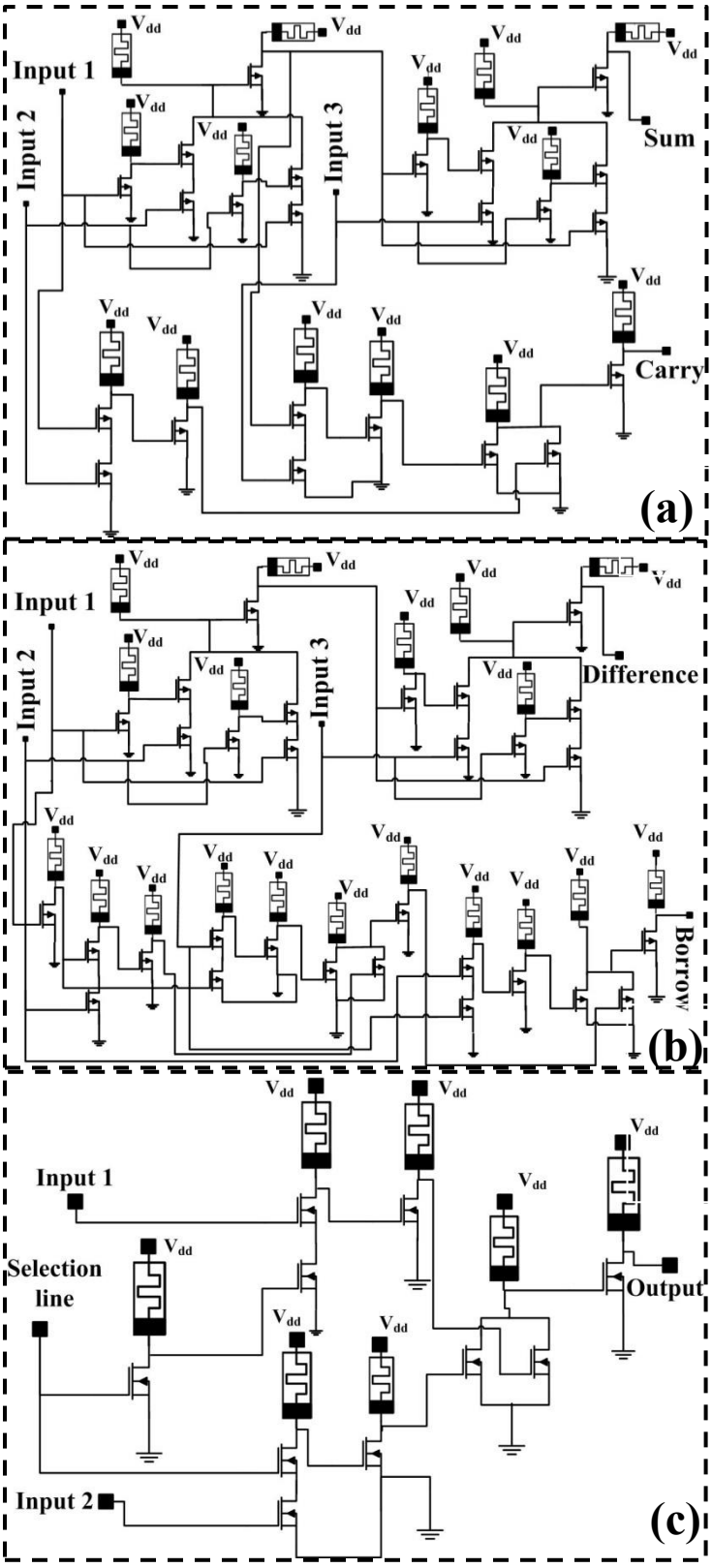

Figure 3.2 : Schematic diagram for (a) FULL adder, (b) FULL subtractor and, (c)2×1 MUX

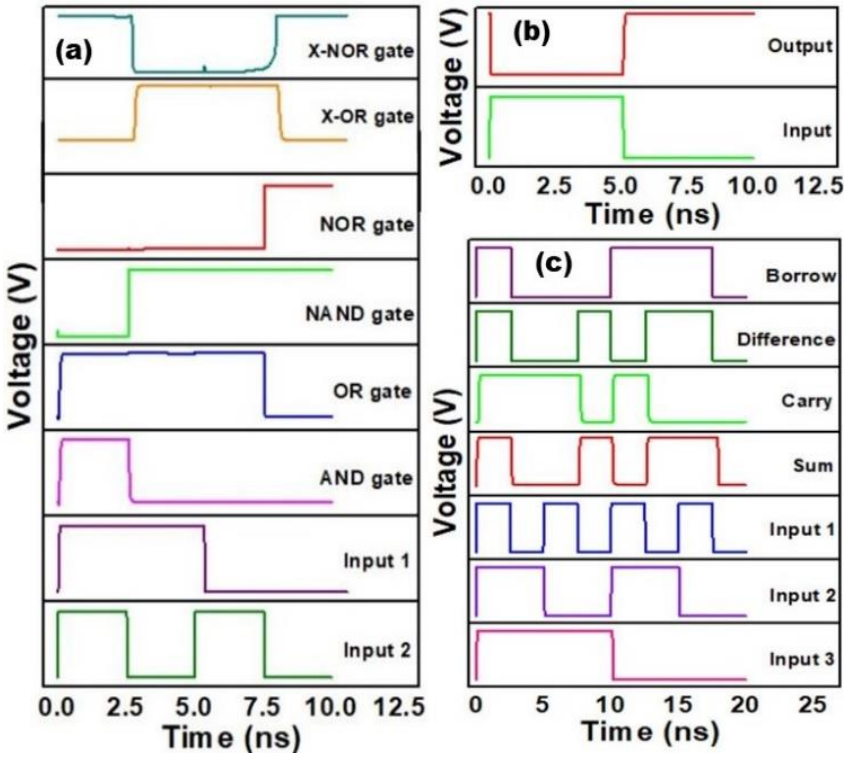

Figure 3.3: Transient responses for (a) AND, OR, NAND, NOR, X-OR and X-NOR gates, (b) NOT gate, and (c)full adder and full subtractor.

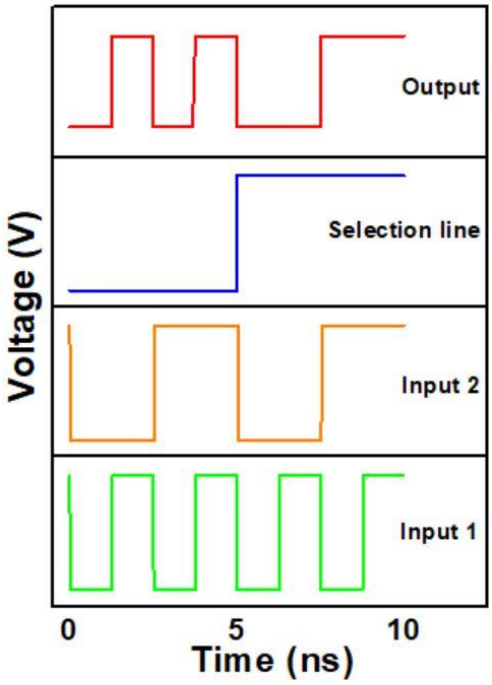

Figure 3.4: Transient response of a2×1 multiplexer.

3.4.1 Area Comparison

The design area of any logic circuit is the important physical parameter and its optimization is the critical task to designing the area efficient layout. It should be noted that if the number of devices in the circuit is increased, then the circuit consumes more area and power as compared to the circuit which has a relatively less number of devices. Here, Table 3 shows a comparative analysis between a number of devices used in the memristor-based and CMOS-based logic circuits [14].

As observed from Table 3, the total number of devices in the memristor-based logic is less than that in the CMOSbased logic circuits because a thousand memristors can be fabricated on the same chip-level area as consumed by a single CMOS.

Table 4: Area calculation for CMOS- and memristor-based logic circuits.

S.No	**Logic gates**	**CMOS model**	**Memristor model**		**% reduction in transistors**
		No.of transistors	**No. of transistors**	**No.of memristors**	
1.	NOT	2	1	1	50
2.	NAND	4	1	2	75
3.	NOR	4	1	2	75
4.	AND	6	2	3	66.66
5.	OR	6	2	3	66.66
6.	X-OR	22	4	7	81.81
7.	X-NOR	22	3	6	86.36
8.	2×1	20	10	7	50

	MUX				
9.	Full adder	62	14	23	77.41
10.	Full subtractor	76	19	30	75

Here, the area utilized by a memristor is 9 nm^2 while, the CMOS transistor consumes an area of 784 nm^2 [15]. Therefore, a memristor captures 98.85% less space than a CMOS transistor for chip-level implementation

3.4.2 Power Comparison

The primary goal of the represented work is to design and implement various logic circuits which perform the logic operations with better power efficiency as compared to conventional CMOS technology. Here, the calculated power is dependent on the output voltage and thus varies according to the type of logic gate. The output waveform for different circuits will be distinct for the same sets of input and hence, the power dissipation for all logic gates and different models can be differentiated [14]. Here, equation (5) is utilized to calculate the power of the implemented logic circuits.

$$Power = \frac{1}{T}\int_0^T \left[\left(V_{output} \times \left(I_{input\ 1} + I_{input\ 2}\right)\right) dt\right] \quad (5)$$

For the two-input logic gate, four permutations are possible such as {00}, {01}, {10}, and {11} and the power of each permutation has been calculated and considered for the evaluation. After the calculation, the logic permutation is considered which utilizes the highest power among them and this is assumed to represent the worst-case scenario of utilized power in a particular logic gate.

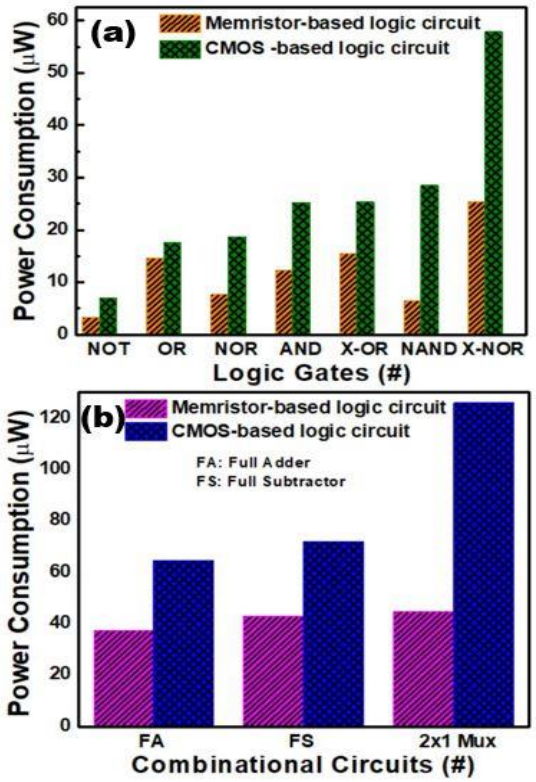

Figure 3.5: Comparison of power consumption between memristor-based and CMOS-based (a) logic gate circuits and (b) combinational logic circuits.

To evaluate the power consumption during logic operation, an input pulse is applied in such a way that all four combinations are changed in a single time period, and the value of 'T' (T is the time required for each logic operation varies according to the logic combination under operation. Next, the power is calculated utilizing the aforementioned method by integrating the total of all input currents and multiplying it by the output voltage at a certain time instant. Figure 3.5 shows the power consumption comparative analysis between memristor-based and CMOS-based logic circuits.As observed in Figure 3.5, the massive advantage of memristorbased logic circuits is that these consume significantly less power as compared to that by the existing CMOS technology which further extends the capabilities of the memristors to implement power-efficient logic circuits for a wide range of applications. As seen from Figure 3.5(a), the CMOS-based X-NOR gate consumes the highest power among all the logic gates while, after the introduction of the memristor-based X-NOR logic gate, the

power consumption is reduced by 56.04%. Similarly, the memristor-based NAND, NOT, NOR, AND, OR, and X-OR logic gates reduce power consumption by 77.29%, 53.55%, 58.95%, 51.30%, 16.38%, and 38.83%, respectively, as compared to the corresponding CMOS technology. In case of combinational logic circuits, a 2×1 mux, full adder, and full subtractor result in a reduction of power consumption by 64.51%, 42.08%, and 40.49%respectively, in comparison to the corresponding existing CMOS technology. However, power consumption is also dependent on the CMOS technology node and it can be further reduced if a lower technology node is adopted, as shown in Figure 3.6. As seen from Figure 3.6(a), the CMOS technology with 90-nm node consume comparatively less power than its 180-nm technology counterparts. While, the power consumption by the memristor-based logic circuits is much lower than the pre-existing CMOS technology nodes, as shown in Figure 3.6(b).

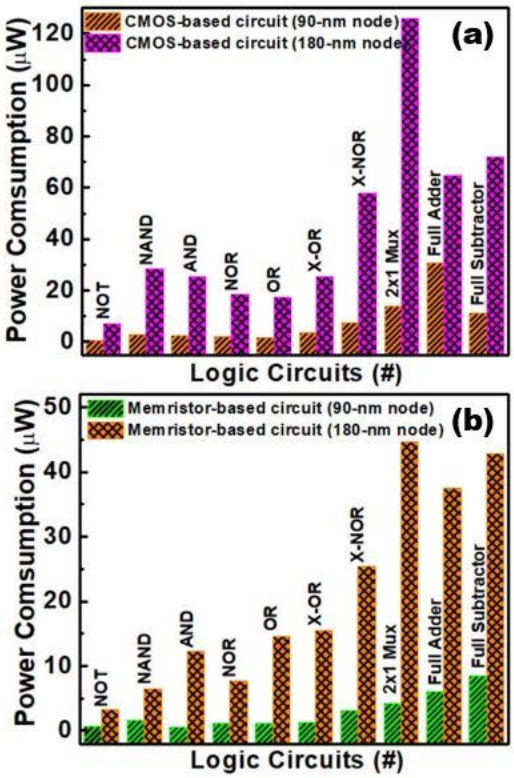

Figure 3.6: The impact of CMOS technology node on power consumption for (a) CMOS-based and (b) memristor-based logic circuits.

3.4.3 Delay Measurement

The delay is referred to the time required to obtain the output after applying the inputs. Here, the average delay is considered which is dependent on the rise time and fall time delay. Equation (6) is utilized to evaluate the average delay [14].

$$Averagedelay = \frac{Risetime + Falltime}{2} \qquad (6)$$

Figure 3.7 depicts the comparative analysis of delay between memristor-based and CMOS-based logic circuits.

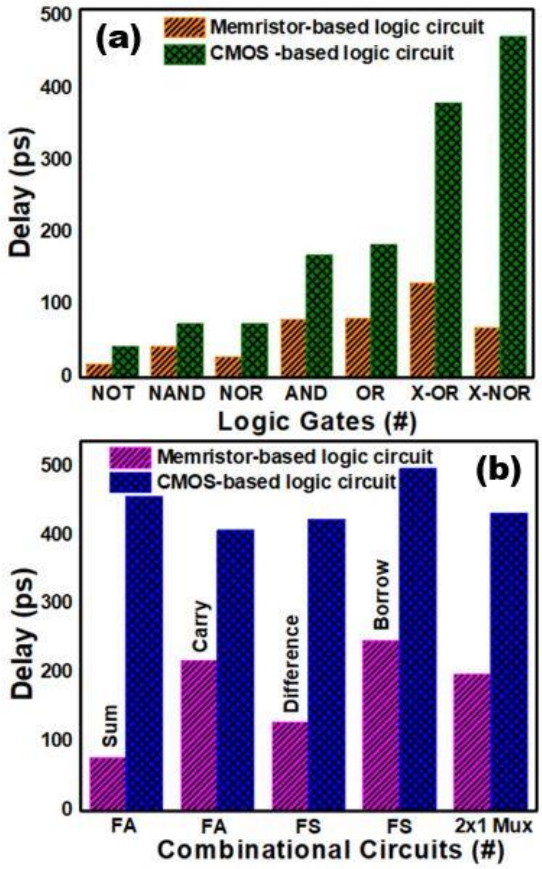

Figure 3.7: Comparison of delay between memristor-based and CMOS-based (a) logic gates and (b) combinational logic circuits.

For the delay calculation, the time difference between the input and output waveform is considered wherein both input and output reach 50% of the value and then subtract their times. As observed from Figure 3.7(a), the X-NOR and X-OR gates have most complex circuitry which provides the enormous decrement in the delay as compared to the existing CMOS technology. In the case of memristor-based logic gates such as NOT, AND, NAND, OR, NOR, X-OR, and X-NOR show 58.34%, 52.82%, 42.93%, 55.69%, 61.83%, 65.78%, and 85.42% delay improvement, respectively, as compared to CMOS technology (Figure 3.7(a)). While, the combinational logic circuits such as 2×1 mux, full adder, and full subtractor display 54.31%, 83.35% (Sum), 46.48% (Carry), 69.54% (Difference), and 54.31% (Borrow) delay improvement, respectively, in comparison to the existing CMOS technology (Figure 3.7(b)).

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Chapter 4

Conclusion and Future Outlook

4.1 Conclusion

We have reported the physical modeling of the memristor by taking reference of the Y_2O_3 based memristor for neuromorphic computation previously reported. In this study, we have investigated the electrical properties of the memristor in the presence and absence of the oxygen reservoir layer (Yttrium layer), which is present between the top electrode and the insulator layer and has a width of 10 nm. Resistance, temperature, gap width, current, and filament radius fluctuation with respect to applied voltage are examples of electrical properties. It is evident from the Table 3. that yttrium based model makes our device more stable and efficient as it has less switching voltages, less device temperature, less resistance as compared to without yttrium based memristor model also it has high filament radius, gap temperature and gap width that makes this device unique. Also, the effect of perturbations on the device switching voltages and electrical characteristics has also been done and the following observations are made.

1. Introducing perturbations leads to decrease in switching voltages of the device.

2. As the perturbation height increases SET voltage and OFF voltage requirements goes down.

3. Filament radius decreases leads to increases in resistance therefore current decreases i.e. loop area decreases.

4. ON/OFF current ratio decreases with increase in perturbation height making it suitable for analog/neuromorphic computation.

Also using the same non-linear analytical memristor model by *Sanjay et.al* implementation of various logic gates and combinational logic circuits via industry-standard Cadence Virtuoso has been done. The model is experimentally validated and demonstrated utilizing low-variance in-house fabricated MCAs. Moreover, the memristor-based logic circuits show significantly better performance in terms of the usage of number of components, total circuit chip area, and utilized power as compared to those for the existing CMOS-based combinational logic circuits wherein 180-nm CMOS technology has been utilized. Furthermore, the presented study reveals that the variation in the CMOS technology nodes (from 180-nm to 90-nm) significantly affects the power consumption in the logic circuitry.

4.2 Future Work

1. Investigating the physical modelling of the memristive device using stacked layers of MOS_2 and simulating different synaptic properties, such as short-term memory (STM) and long-term memory (LTM).
2. To analyse the switching behaviour of a memristive device with stacked-layer MoS_2 at nanosecond or picosecond pulse width.
3. Investigate DAC behaviour of MoS_2-based memristive device.
4. Design and implement power and delay efficient circuits for the amplifier, oscillator and neural networks.