Insightful Evaluation of Advantages and Challenges of Reconfigurable Transistor for Analog/RF Applications

MS (Research) Thesis

By

AAKASH ASHUTOSH DESHPANDE

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

JUNE 2023

Insightful Evaluation of Advantages and Challenges of Reconfigurable Transistor for Analog/RF Applications

A THESIS

Submitted in fulfillment of the
requirements for the award of the degree
of

Master of Science (Research)

by

AAKASH ASHUTOSH DESHPANDE

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE

JUNE 2023

INDIAN INSTITUTE OF TECHNOLOGY INDORE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **Insightful Evaluation of Advantages and Challenges of Reconfigurable Transistor for Analog/RF Applications** in the fulfillment of the requirements for the award of the degree of **MASTER OF SCIENCE (RESEARCH)** and submitted in the **DEPARTMENT OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from July 2021 to June 2023 under the supervision of Dr. Abhinav Kranti, Professor, Discipline of Electrical Engineering, Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

03/06/2023

Signature of the student with date
(AAKASH ASHUTOSH DESHPANDE)

This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

June 03, 2023

Signature of the Supervisor of MS (Research) thesis (with date)
(Prof. ABHINAV KRANTI)

AAKASH ASHUTOSH DESHPANDE has successfully given his~~/her~~ MS (Research) Oral Examination held on 22/09/2023.

22-Sept-2023
Signature of Chairperson (OEB) with date

22/09/2023
Signature(s) of Thesis Supervisor(s) with date

22/09/2023
Signature of Convener, DPGC with date

22 September 2023
Signature of Head of Discipline with date

ACKNOWLEDGEMENT

First and foremost, I extend my heartfelt gratitude to Prof. Abhinav Kranti, my M.S. (Research) supervisor, for his invaluable guidance, unwavering support, and constant motivation throughout my master's program. I would like to express my appreciation to my PSPC members, Prof. Saptarshi Ghosh, and Prof. Bhargav Vaidya, for their constructive suggestions during the evaluation presentations. I am extremely thankful to Prof. Jean-Pierre Raskin, Université catholique de Louvain, Belgium, for his valuable comments, which greatly contributed to the enhancement of my research work.

I would like to express my appreciation to IIT Indore for providing the necessary facilities for conducting my thesis work. I am grateful to all the faculty and staff members of the Electrical Engineering Department for their cooperation and encouragement throughout the process. Additionally, I extend my thanks to IIT Indore and the Ministry of Education, Government of India, for granting me the stipend during my M.S.(R) program. The project was made possible with the support of TCAD tools, which were provided through project funds (CRG/2019/002937) from the Department of Science and Technology, Government of India.

I convey my heartfelt gratitude to my lab members, Sandeep, and Rohit, for their continuous assistance and support during the project. Their help has been invaluable. I would also like to thank Vivek and Keerthi for their kind cooperation.

I extend my sincerest appreciation to my parents, Mrs. Sonali Deshpande (my mother) and Mr. Ashutosh Deshpande (my father), for their unwavering motivation and support during challenging times. Their encouragement has been instrumental in my journey. I express my gratitude to my friends Nisarg, Rushikesh, and all my M.S.(R) colleagues for the unforgettable moments we have shared throughout these two years. Their companionship has made this experience truly memorable.

Lastly, I would like to thank all those individuals who have knowingly or unknowingly aided me in various ways. Your contributions have been valuable, and I am grateful for your assistance.

Aakash Ashutosh Deshpande

Dedicated to my parents

Abstract

Insightful Evaluation of Advantages and Challenges of Reconfigurable Transistor for Analog/RF Applications

Over the last few years, the practice of reducing the size of transistors has reached a saturation point. This is primarily due to the severe influence of short channel effects (SCEs) such as drain induced barrier lowering (DIBL), threshold voltage (V_{th}) roll-off, etc., which significantly degrade the device performance when scaling down in the sub-100 nm regime. An alternative method for increasing the number of functions on a chip per unit area is to incorporate additional functionality within the same device, instead of reducing the device size. This is where Reconfigurable Field Effect Transistor (RFET) comes into play. The emergence of RFET, which can demonstrate both unipolar *n*-type and *p*-type functionality in a single device, has positioned itself as a robust rival to modern transistor architectures due to its exceptional performance at both device and circuit levels. RFET devices have shown promising results in a wide range of applications spanning from digital logic to trending topics like neuromorphic engineering. However, the effectiveness of RFET in analog/RF applications has not gained enough attention. To date, there exists a literature gap as only a limited number of studies have showcased the usefulness of RFET in the context of analog and RF applications. Research on analog/RF performance of RFET specifically at low current drives (ultra low power operation), has yet to be conducted. To become a prominent contender for modern mixed-signal applications (e.g. smartphones), RFET must not only enhance its digital characteristics, but also allocate comparable attention towards its analog functionality as well.

Although the ungated region and lower current drive of RFETs may compromise their digital and analog/RF performance at higher current levels (> 10 µA/µm), the device exhibits significant potential for analog/RF applications at lower current levels (< 10 µA/µm), where its inherent architecture becomes the primary determinant of performance. As such, an evaluation of the analog/RF

characteristics of RFET under low current conditions is of utmost importance. The research work focuses on assessing the analog/RF performance of two different RFET topologies namely three-gated (3G) and twin-gate (2G) RFET by benchmarking important analog/RF metrics like transconductance (g_m), transconductance-to-current ratio (g_m/I_{ds}), Early voltage (V_{EA}), intrinsic voltage gain (A_V), gate capacitance (C_{gg}) and cut-off frequency (f_T) against a conventional double-gate (DG) MOSFET for same total source-to-drain length (L_T = 100 nm) at low current levels (10^{-2} µA/µm to 10^{1} µA/µm).

Results reveal that despite RFET (3G and 2G) having a higher number of gates in comparison to the MOSFET, its gate parasitic capacitance ($C_{parasitic}$) is significantly reduced. In order to comprehend this unexpected result more effectively, an equivalent capacitance model was employed to examine the contribution of each parasitic component to the overall parasitic capacitance in the DG MOSFET, 3G RFET, and 2G RFET. The lower $C_{parasitic}$ (or lower C_{gg}) in the RFET can be attributed to the smaller values of parasitic components in the ungated (UG) region which greatly enhances the f_T (specifically for 3G RFET). In comparison to MOSFET, a three-gated RFET exhibits inferior A_V due to lower values of g_m/I_{ds} and V_{EA} caused by two factors: (i) inadequate current drive and (ii) significant drain induced barrier lowering (DIBL) effect. Conversely, the twin-gate RFET demonstrates strong resilience to the DIBL effect at low I_{ds}, resulting in a notably high V_{EA}. However, its A_V is compromised due to a sharp decline in V_{EA} at high I_{ds} in addition to poor g_m/I_{ds}. Hence, at high I_{ds} (> 1 µA/µm), there exists a gain (A_V) bottleneck for RFET topologies.

Analysis has been conducted on architecture optimization aimed to overcome A_V bottleneck and improve various analog/RF metrics of RFET. By increasing the control gate length (L_{CG}), RFET can surpass MOSFET by a significant margin in terms of A_V. Additionally, increasing the ungated region (L_{UG}) resulted in noteworthy enhancements in circuit delay (τ) and cut-off frequency (f_T), particularly for 3G RFET at lower current levels. Consequently, while 3G RFET is more suitable for high-speed (f_T) applications, 2G RFET is

more favorable for high-gain (A_V) applications. Thus, a tradeoff between choosing RFET architecture - 3G or 2G exists. These findings offer new insights into capacitance components and architecture optimization of RFET topologies, enabling the enhancement of analog/RF metrics at lower current drive.

LIST OF PUBLICATIONS

A. <u>In referred journals</u>:

1. **Aakash Ashutosh Deshpande**, Sandeep Semwal, Jean-Pierre Raskin, and Abhinav Kranti, "Insights into Parasitic Capacitance and Reconfigurable FET Architecture for Enhancing Analog/RF Metrics," ***IEEE Transactions on Electron Devices***, in press, 2023, doi: 10.1109/TED.2023.3310943, Impact factor: 3.1 (Accepted).

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

NOMENCLATURE

L_{min}	*Minimum feature size*	*nm*
L_G	*Transistor gate length*	*nm*
W	*Transistor width*	*nm*
W_{dm}	*Maximum depletion width*	*nm*
T_{ox}	*Gate oxide thickness*	*nm*
P	*Power consumption*	*W*
τ	*Circuit delay*	*ns*
k	*Permittivity*	*F/cm*
z	*Scaling Factor*	*Unitless*
A_V	*Voltage gain*	*dB*
g_m/I_{ds}	*Transconductance-to-current ratio*	V^{-1}
V_{EA}	*Early voltage*	*V*
g_m	*Transconductance*	*A/V*
I_{ds}	*Drain-to-source current*	*A*
f_T	*Cut-off frequency*	*GHz*
f_{MAX}	*Maximum oscillation frequency*	*GHz*
$\|H_{21}\|$	*Short Circuit Current Gain*	*dB*
V_{out}	*Output Voltage*	*V*
V_{in}	*Input Voltage*	*V*
V_{gs}	*Gate-to-source voltage*	*V*
dV_{th}	*Threshold voltage roll-off*	*V*
V_{bi}	*Built-in voltage*	*V*
V_{app}	*Applied voltage*	*V*
V_{th}	*Threshold voltage*	*V*
V_{ox}	*Voltage drop across gate oxide*	*V*
V_{ds}	*Supply voltage*	*V*

υ_T	*Thermal voltage*	*mV*
υ_{sat}	*Saturation velocity*	*m/s*
C_{ox}	*Oxide capacitance per unit area*	*fF/cm^2*
C_{gg}	*Gate capacitance per unit length*	*fF/μm*
C_{dm}	*Maximum depletion capacitance*	*fF/cm^2*
S_{swing}	*Subthreshold swing*	*mV/dec*
μ_o	*Low field mobility*	*cm^2/V-s*
m	*Subthreshold swing coefficient*	*Unitless*
ε_{si}	*Permittivity of silicon*	*F/cm*
ε_{ox}	*Permittivity of gate oxide*	*F/cm*
N_A	*Doping concentration of p-type substrate*	*cm^{-3}*
ϕ_{ox}	*Gate oxide barrier height*	*eV*
T_{BOX}	*Buried oxide (BOX) thickness*	*nm*
T_{Si}	*Silicon film thickness*	*nm*
R_C	*Contact Resistance*	*Ω*
I_{ON}	*On-current*	*mA*
I_{OFF}	*Off-current*	*nA*
I_{ON}/I_{OFF}	*On-current to off-current ratio*	*Unitless*
q	*Electronic charge*	*C*
E_{vac}	*Energy of free space (vacuum)*	*eV*
E_C	*Energy of conduction band*	*eV*
E_V	*Energy of valence band*	*eV*
E_F	*Energy of Fermi level*	*eV*
E_{FM}	*Fermi energy level of metal*	*eV*
E_{FS}	*Fermi energy level of semiconductor*	*eV*
E_g	*Bandgap of the semiconductor*	*eV*
χ	*Electron affinity of the material*	*eV*
χ_s	*Electron affinity of semiconductor*	*eV*
$\chi_{s,n}$	*Electron affinity of n-type semiconductor*	*eV*

$\chi_{s,p}$	*Electron affinity of p-type semiconductor*	*eV*
ϕ	*Work-function of the material*	*eV*
ϕ_M	*Work-function of metal*	*eV*
ϕ_S	*Work-function of semiconductor*	*eV*
ϕ_n	*Work-function of n-type semiconductor*	*eV*
ϕ_p	*Work-function of p-type semiconductor*	*eV*
$\phi_{b,n}$	*Schottky barrier height in n-type semiconductor*	*eV*
$\phi_{b,p}$	*Schottky barrier height in p-type semiconductor*	*eV*
T	*Temperature*	*K*
J_{TE}	*Current density of thermionic emission*	$\mu A/m^2$
m^*	*Effective mass of the carrier*	*kg*
m_n^*	*Effective mass of electron*	*kg*
m_p^*	*Effective mass of holes*	*kg*
m_o	*Rest mass of electron*	*kg*
A^*	*Richardson's constant*	A/m^2K^2
h	*Planck's constant*	m^2kg/s
$\hbar$	*Reduced Planck's constant*	m^2kg/s
k	*Boltzmann's constant*	*J/K*
L_{CG}	*Control gate length*	*nm*
L_{PG}	*Polarity gate length*	*nm*
L_{UG}	*Ungated region length*	*nm*
L_{SP}	*Spacer length*	*nm*
L_T	*Total length*	*nm*
L_{eff}	*Effective channel length*	*nm*
V_{cg}	*Control gate voltage*	*V*
V_{pg}	*Polarity gate voltage*	*V*
$T_{n,p}$	*Tunneling probability*	*Unitless*
E	*Applied electric field*	*V/m*
$C_{parasitic}$	*Parasitic gate capacitance*	$fF/\mu m$

$C_{of\_e1\_e2}$	*Outer fringing parasitic capacitance between e1 and e2*	*fF/μm*
$C_{top\_e1\_e2}$	*Top fringing parasitic capacitance between e1 and e2*	*fF/μm*
$C_{side\_e1\_e2}$	*Sidewall parasitic capacitance between e1 and e2*	*fF/μm*
$C_{if\_e1\_e2}$	*Inner fringing parasitic capacitance between e1 and e2*	*fF/μm*
C_{gs_para}	*Gate-to-source parasitic capacitance*	*fF/μm*
C_{gd_para}	*Gate-to-drain parasitic capacitance*	*fF/μm*
$(C_{gs\_para})_{MOS}$	*Gate-to-source parasitic capacitance of MOSFET*	*fF/μm*
$(C_{gd\_para})_{MOS}$	*Gate-to-drain parasitic capacitance of MOSFET*	*fF/μm*
$C_{top\_g\_s}$	*Top fringing parasitic capacitance between gate and source*	*fF/μm*
$C_{of\_g\_s}$	*Outer fringing parasitic capacitance between gate and source*	*fF/μm*
$C_{if\_g\_s}$	*Inner fringing parasitic capacitance between gate and source*	*fF/μm*
C_{pg_s}	*Parasitic capacitance between PG and source*	*fF/μm*
C_{pg_d}	*Parasitic capacitance between PG and drain*	*fF/μm*
$C_{top\_pg\_s}$	*Top fringing parasitic capacitance between PG and source*	*fF/μm*
$C_{of\_pg\_s}$	*Outer fringing parasitic capacitance between PG and source*	*fF/μm*
$C_{if\_pg\_s}$	*Inner fringing parasitic capacitance between PG and source*	*fF/μm*
C_{cg_pg}	*Parasitic capacitance between CG and PG*	*fF/μm*
$C_{top\_cg\_pg}$	*Top fringing parasitic capacitance between CG and PG*	*fF/μm*
$C_{side\_cg\_pg}$	*Sidewall parasitic capacitance between CG and PG*	*fF/μm*
$C_{if\_cg\_pg}$	*Inner fringing parasitic capacitance between CG*	*fF/μm*

	and PG	
C_{cg_s}	*Series combination of C_{pg_s} and C_{cg_pg}*	*fF/μm*
$C_{if\_cg\_s}$	*Inner fringing parasitic capacitance between CG and source*	*fF/μm*
$C_{if\_cg\_d}$	*Inner fringing parasitic capacitance between CG and drain*	*fF/μm*
$(C_{gs\_para})_{RFET\text{-}A}$	*CG-to-source parasitic capacitance of RFET-A*	*fF/μm*
$(C_{gs\_para})_{RFET\text{-}B}$	*CG-to-source parasitic capacitance of RFET-B*	*fF/μm*
$(C_{gd\_para})_{RFET\text{-}B}$	*CG-to-drain parasitic capacitance of RFET-B*	*fF/μm*
$C_{top\_cg\_s}$	*Top fringing parasitic capacitance between CG and source*	*fF/μm*
$C_{of\_cg\_s}$	*Outer fringing parasitic capacitance between CG and source*	*fF/μm*
$C_{if\_cg\_s}$	*Inner fringing parasitic capacitance between CG and source*	*fF/μm*
$C_{top\_pg\_d}$	*Top fringing parasitic capacitance between PG and drain*	*fF/μm*
$C_{of\_pg\_d}$	*Outer fringing parasitic capacitance between PG and drain*	*fF/μm*
$C_{if\_pg\_d}$	*Inner fringing parasitic capacitance between PG and drain*	*fF/μm*

ACRONYMS

DSP	*Digital Signal Processor*
FEM	*Front End Module*
RF	*Radio Frequency*
IRDS	*International Roadmap for Devices and Systems*
Wi-Fi	*Wireless Fidelity*
IoT	*Internet of Things*
5G	*5^{th} Generation*
6G	*6^{th} Generation*
WSN	*Wireless Sensor Network*
IC	*Integrated Circuit*
MOS	*Metal Oxide Semiconductor*
FET	*Field Effect Transistor*
CMOS	*Complementary MOS*
BiCMOS	*Bipolar-Complementary MOS*
nMOS	*n-type MOS structure*
pMOS	*p-type MOS structure*
n	*Donor type*
p	*Acceptor type*
n^+	*Heavily doped donor type*
p^+	*Heavily doped acceptor type*
S/D	*Source or Drain*
BJT	*Bipolar Junction Transistor*
Si	*Silicon*
SiO_2	*Silicon Dioxide*
SiGe	*Silicon-Germanium*
GaN	*Gallium Nitride*
GaAs	*Gallium Arsenide*
I/O	*Input-Output*

SoC	*System on Chip*
CFS	*Constant Field Scaling*
CVS	*Constant Voltage Scaling*
GS	*Generalized Scaling*
SCE	*Short Channel Effects*
BTBT	*Band-to-band tunneling*
DIBL	*Drain induced barrier lowering*
FN	*Fowler-Nordheim*
GIDL	*Gate induced drain lowering*
SOI	*Silicon-on-Insulator*
PD SOI	*Partially Depleted SOI*
FD SOI	*Fully Depleted SOI*
BOX	*Buried Oxide*
UTB	*Ultra Thin Body*
UTBB	*Ultra Thin Body BOX*
DELTA	*Depleted Lean-channel Transistor*
GP	*Ground Plane*
DG	*Double Gate*
CGP	*Contact Gate Pitch*
GAA FET	*Gate-All-Around FET*
RFET	*Reconfigurable FET*
3G RFET	*Three-gate RFET*
2G RFET	*Twin-gate RFET*
CG	*Control Gate*
UG	*Ungated region*
PG	*Polarity Gate*
SB	*Schottky Barrier*
SBH	*Schottky Barrier Height*
M-S	*Metal-Semiconductor*
RFET-A	*RFET type-A (3G RFET)*
RFET-B	*RFET type-B (2G RFET)*

TCAD	*Technology Computer Aided Design*
UST	*Universal Schottky Tunneling*
ALU	*Arithmetic Logic Unit*
DRAM	*Dynamic Random Access Memory*
CB	*Conduction Band*
VB	*Valence Band*
GBP	*Gain-Bandwidth Product*

Chapter 1

Introduction

1.1 Motivation – Analog/RF Systems

In 2022, the transistor completed 75 years [1] in the semiconductor industry and has truly come a long way beating all the odds by encroaching into several application areas like wireless communication, automobile, and consumer electronics. In 1965, Gordon Moore predicted that the transistor count on a chip would double every 18 months [2]. Increased transistor count on an integrated chip leads to greater functionality, less computation time, and reduced manufacturing cost. Despite obstacles, innovations by industry and researchers have made it possible by reducing the feature size to continue Moore's Law for almost 60 years. In modern day mobile communication systems, while processing of the information is done using digital circuits, the front-end modules (FEM) of wireless systems consist of analog circuits and will continue to do so for the foreseeable future due to better efficiency of analog coding techniques [3]. Scaling down the transistor results in performance enhancement of the RF circuit enhances due to high speed, reduced power consumption, and high circuit density. Analog/RF device/circuit progress is hindered by limited area and power efficiency [4, 5]. Lower voltage headroom with every generation of transistor scaling yields analog circuits with degraded performance [6, 7]. The degraded performance of the transistor can be attributed to the fact that the improvements made to transistors through scaling are outweighed by the negative impacts of second order effects and reduced supply voltage [8]. The International Roadmap for Devices and Systems (IRDS) [9] features distinct guidelines for the scaling of analog and digital circuits.

The wireless communication market has rapidly grown with the rise of telecommunication technologies such as mobile phones, Wi-Fi (Wireless Fidelity), etc. The emergence of the Internet of Things (IoT) has further increased the demand for advanced and application-specific wireless technologies.

Equivalent to Moore's law on semiconductors, Edholm's law [10] states that the telecommunication data rates double every 18 months. Higher data rates, higher capacity, and many more connected devices will be demanded by the next generation of wireless technology like 5G communication standard and IoT [11]. Applications such as IoT and Wireless Sensor Networks (WSN) require low energy consumption due to their limited power supply and intermittent operation. Circuit power management is critical to conserve energy and extend battery life, and directly affects the power efficiency of transistor technology. Unwanted harmonics generated in the communication systems are suppressed using linearization techniques. Linearity requirements ensure protection from intermodulation products and higher-order harmonics [12]. Hence, the use of transistors with low distortion is envisaged. The scaling of transistor parameters makes it increasingly difficult to cope with the desired performance, and hence mandates innovation at device/circuit level.

The RF integrated circuits (IC) performance is closely related to the analog and high frequency characteristics of transistors. As a result, upgrading current semiconductor technologies is necessary to meet the demands of upcoming wireless circuits and systems that have high specifications. Heterogeneous integration of compound semiconductors (III-V materials) with the existing Complementary Metal Oxide Semiconductor (CMOS) technology which is also referred to as hybrid integration is slowly emerging as a strong contender for next-generation mobile communication protocols like 6G communication standard [11], [13-21]. Multigate transistor architectures are also gaining considerable attention to replace the conventional planar transistors in RF-FEMs [22]-[29].

1.2 Evolution of CMOS Technology for Analog/RF Applications

In the early days, CMOS was not an obvious technology for RF millimeter-wave applications in terms of performance, especially compared to SiGe and III-

V technologies [30, 31]. However, in recent times, CMOS has now established itself as a market leader due to its superior performance, excellent integration capability, and low cost due to its firm domination in digital electronics. MOSFETs were considered as “slow” devices due to the lower intrinsic mobility of Silicon compared to other compound semiconductors like GaN and GaAs [32]. Due to the proximity of the inversion channel in a MOSFET to the Si/SiO_2 interface, various factors such as interface roughness, crystal imperfections, and interface traps have led to a further deterioration in the mobility of carriers within the transistor [32]. Modern technologies have an approximate peak nMOS f_T of 10 THz-nm/L_{min}, indicating that the “practical” operating frequency can be roughly estimated at 1 THz-nm/L_{min} [33], where L_{min} represents the minimum feature size.

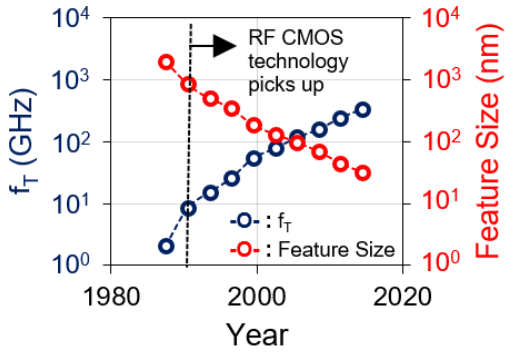

Fig. 1.1 Variation of cut-off frequency (f_T) and feature size of the transistor over the years [34].

Wireless applications in the 1990s were operating in the 1 GHz frequency range. During that period, CMOS technology was mature enough to be used for a transistor for its implementation in the RF domain (Fig. 1.1). Practical implementations were seen a few years later. Modern ICs comprise a blend of digital and analog components, encompassing a substantial digital core (including Digital Signal Processor and memory) encircled by numerous analog interface components (such as input-output, converters, and RF FEMs) [12]. This complex architecture is also called a System-on-chip (SoC). The transceiver of a wireless cellphone is an example that consists of an SoC where the analog and RF functions are integrated with digital logic in deep submicron CMOS. From an

integration perspective, all these functions should be on a single die. This makes it economically more viable. The fusion of advanced RF transistors and the capacity to incorporate compact digital back-end features on a solitary silicon chip amplifies the possibilities for creating intricate integrated circuits suitable for a wide-range of mixed-signal applications [35]. CMOS technologies are predominantly utilized for analog circuit design due to the widespread popularity of SoC, whereas bipolar, BiCMOS (Bipolar CMOS), and compound technologies find applications in highly specialized scenarios [5].

CMOS has been crucial in digital and analog/RF electronics, with reduced costs and ongoing advancements. Despite potential limitations, it is difficult for alternative technologies to match CMOS's superiority. To overcome challenges, innovative transistors like strained silicon and high permittivity (high-k)/metal gates enhance performance [36]. The drive for continued downscaling, cost-effectiveness, suitability in SoC applications, and ongoing research on CMOS technologies serve as motivating factors for its continued utilization in RF.

Table 1.1

Summary of scaling methods.

Before scaling	**After scaling**		
	Constant field scaling method	Constant voltage scaling method	Generalized scaling method
Area	Area/z^2	Area	Area/z^2
Power *(P)*	P/z^2	zP	$\alpha^3 P/z^2$
Delay (τ)	τ/z	τ/z^2	$\tau/\alpha z$

1.3 Transistor Scaling

To meet the demand for high-performance applications, semiconductor industries are compelled to innovate and produce smaller, energy-efficient devices, driven by the trend of miniaturization that's crucial in applications such

as mobile devices, wearables, and IoT devices where space is limited. Some of the transistor scaling methods are mentioned in this section along with the changes in key device parameters like area, power consumption (P), and delay (τ) before and after scaling are illustrated in Table 1.1.

- **Transistor Scaling Methods:**

1. **Constant field scaling (CFS) method [38]:** In this method, **t**he electric field inside the transistor is maintained the same while the voltages and the dimensions are scaled by a scaling factor z. A significant improvement is observed for area, P, and τ showcasing the benefits of constant field scaling (Table 1.1). However, there are some constraints associated with using this method. It is observed that with each technology node, as compared to length scaling, a hinderance is seen for voltage scaling. Scaling voltage levels below 1 V poses a big challenge for device engineers [6,7].

2. **Constant voltage scaling (CVS) method [38]:** In this method, the terminal voltages and operating power supply voltage are maintained same while the device dimensions are downscaled by a scaling factor z. A major disadvantage of the constant voltage method is that P increases z-times (Table 1.1). The area occupied by the device also remains unchanged, defeating the very purpose of scaling. Only τ shows an improvement (reduces by z^2 times) when using this method.

3. **Generalized scaling (GS) method [38]:** When transitioning from one technology node to another, two scaling factors, α and z, are used ($1 < \alpha < z$), instead of just one. Linear dimensions, doping concentrations, and terminal voltages are scaled by a factor of $1/z$, z, and α/z respectively. By properly optimizing the values of α and z, a balance between P and τ can be made by using the results from Table 1.1.

1.4 Impact of Transistor Downscaling on Analog/RF Performance

Transistor scaling in analog and RF circuit design involves a complex set of trade-offs that must be carefully optimized to achieve optimal performance across a range of performance parameters. Cut-off frequency (f_T), intrinsic voltage gain (A_V), transconductance-to-current ratio (g_m/I_{ds}), linearity, noise, and device matching are key performance matrices for RF and analog circuits. Enhancing one of these aspects often results in a decline in the others, making it challenging to optimize the device across all metrics [39]. Two of the main metrics for analog/RF performance are:

- **Intrinsic voltage gain (A_V):** Ratio of the output voltage (V_{out}) to the input voltage (V_{in}) of a transistor. It is usually measured in decibels (dB) i.e. $(A_V)_{dB} = 20\log_{10}(|V_{out}/V_{in}|)$ [38].
- **Cut-off frequency (f_T):** The frequency at which the short circuit current gain ($|H_{21}|$) of the transistor is equal to unity [40]. It is usually measured in GHz.

Some of the most important scaling trade-offs between analog performance matrices are mentioned below:

1. Trade-off between voltage gain (A_V) and cut-off frequency (f_T):

The voltage gain of a conventional MOSFET is given by $A_V = g_m/g_{ds}$, where g_m and g_{ds} are the input and output transconductance respectively. By downscaling the transistor, g_m does not change much for a given current density. For a transistor biased in a saturation region, drain current (I_{ds}) can be obtained as

$$I_{ds} = WC_{ox}(V_{gs} - V_{th})v_{sat} \quad (1.1)$$

where W is the transistor width, C_{ox} is the gate oxide capacitance, V_{gs} is the gate-to-source voltage (input bias), V_{th} is the threshold voltage of the device and v_{sat} is the saturation velocity.

Therefore, g_m ($= \partial I_{ds}/\partial V_{gs} = WC_{ox}v_{sat}$) depends on W and C_{ox}. The scaling of W is directly proportional to L_G, while the scaling of C_{ox} is inversely

proportional to L_G [41], where L_G is the transistor length. Hence, g_m does not depend on L_G. Nevertheless, due to different physical drain leakage mechanisms, the amplified g_{ds} in short channel MOS devices cause a reduction in A_V as shown in Fig. 1.2(a). Unlike A_V, f_T (= $g_m/2\pi C_{gg}$) usually increases with transistor downscaling. Despite g_m remaining nearly unchanged, the gate capacitance (C_{gg}) scales directly proportional to L_G which leads to the enhancement in f_T (Fig. 1.2(b)). Hence, when optimizing the design of a device at a specific technology node, device engineers face a trade-off between A_V and f_T.

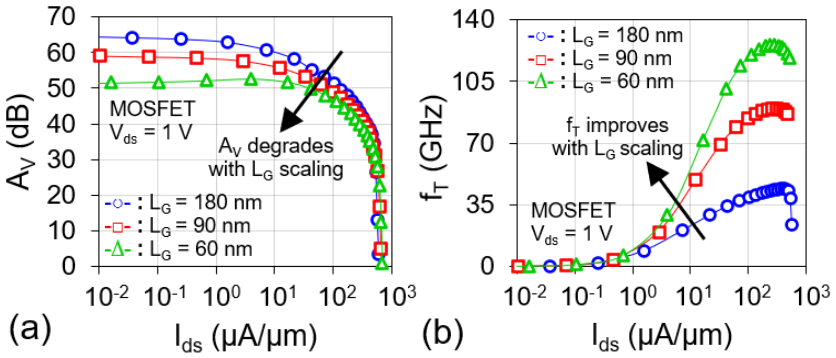

Fig. 1.2 Variation of (a) voltage gain (A_V) and (b) cut-off frequency (f_T) with drain current (I_{ds}) in a MOSFET for different transistor lengths (L_G) at V_{ds} = 1 V.

2. Trade-off between the speed (f_T) and the power efficiency (g_m/I_{ds}):

The g_m/I_{ds} ratio is known as "power efficiency" or "transconductance efficiency" [42]. Altering the size of the transistor does not have a substantial impact on peak g_m/I_{ds} ratio (see Fig. 1.3(a)) if SCEs are controlled. MOSFET attains high g_m/I_{ds} value in the weak-inversion region i.e. at low V_{gs}. Working with high g_m/I_{ds} significantly contributes to power reduction, but it entails a trade-off in terms of linearity. Transistors that operate at high g_m/I_{ds} demonstrate characteristics resembling those of a bipolar junction transistor (BJT), resulting in higher distortion compared to a MOSFET operating in strong inversion [42].

The cut-off frequency (f_T) of a transistor attains a maximum value in strong inversion region (see Fig. 1.3(a)) and generally increases with ($V_{gs} - V_{th}$) in contrast to g_m/I_{ds}. This results in a fundamental trade-off between a transistor's power efficiency, reflected in the g_m/I_{ds} ratio, and its self-loaded bandwidth,

represented by f_T [42]. Consequently, achieving an optimal balance between these two crucial parameters poses a fundamental challenge in analog design. Hence, to gain the benefits of both g_m/I_{ds} and f_T in a scenario where some compromises can be tolerated, the product of g_m/I_{ds} and f_T becomes a compelling metric to consider (Fig. 1.3(b)). $g_m/I_{ds} \times f_T$ shows a peak around a gate overdrive ($V_{gs} - V_{th}$) of 100 mV (also referred to as "sweet spot") across technology nodes [42].

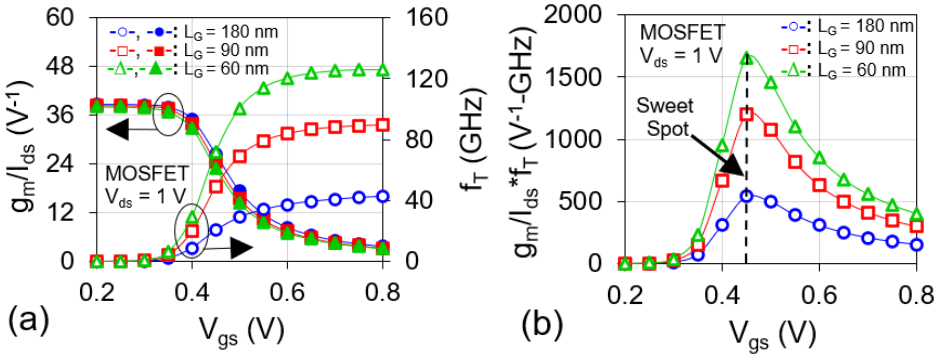

Fig. 1.3 Variation of (a) transconductance-to-current ratio (g_m/I_{ds}) and cut-off frequency (f_T) and (c) $g_m/I_{ds} \times f_T$ with input bias (V_{gs}) in a MOSFET for different transistor lengths (L_G) at V_{ds} = 1 V.

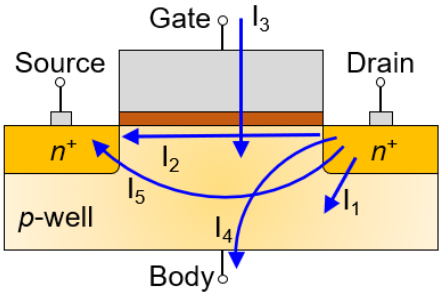

Fig. 1.4 Illustration of different leakage current mechanisms (I_1 to I_5) in a conventional bulk MOSFET [43].

1.5 Challenges in Transistor Scaling

Transistor downscaling benefits include higher packaging density and enhanced switching speed. However, it also has drawbacks such as degraded subthreshold swing (S_{swing}) and V_{th} roll-off (dV_{th}). These issues arise from increased off-leakage currents and SCEs that impact performance when MOSFET is scaled down in sub-100 nm gate length. The variation in the off-state current

(I_{OFF}) directly affects V_{th} and S_{swing}, making it the primary limiting factor for downsizing (Fig. 1.4) [37].

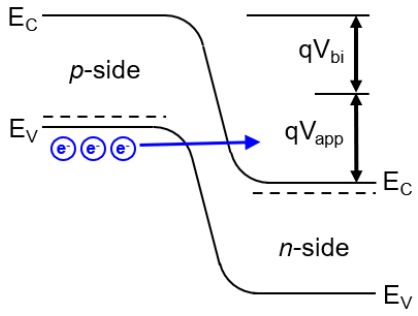

Fig. 1.5 BTBT in a reversed biased *pn*-junction of a MOSFET with heavily doped substrate at high V_{ds}. V_{bi} and V_{app} are built-in and applied voltage respectively.

1. Leakage current in reverse-biased *pn* junction (I_1):

The MOS transistor is characterized by two *pn* junctions: drain and source connected to the channel/body. Typically, these junctions are biased in the reverse direction, leading to leakage current consisting of two primary components i) Minority carrier diffusion near the depletion region edge and ii) electron-hole pair generation occurs within the reverse-biased depletion region [44]. Reverse bias leakage current of *pn* junction (I_{REV}) depends on junction area and doping concentration [44]. In cases where both *n* and *p* regions are heavily doped, band-to-band tunneling (BTBT) becomes the dominant factor in *pn* junction leakage [38] (Fig. 1.5). The *pn* junction in scaled devices experiences a notable tunneling current due to the combined effect of high doping and abrupt doping configurations [44].

2. Subthreshold current (I_2):

Irrespective of the length of the gate, the subthreshold off-state component is inevitable in MOSFET. Subthreshold current occurs between the source and the drain of the MOSFET when it operates below threshold voltage ($V_{gs} \leq V_{th}$). Unlike drift component which dominates the current between drain and source in the strong inversion region, diffusion dominates the current component in the

subthreshold region. For an *n*-type classical MOSFET device, the subthreshold current (I_{ds}) can be expressed as [38]:

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L_G}(m-1)(\upsilon_T)^2 \times e^{(V_{gs}-V_{th})/m\upsilon_T} \times \left(1 - e^{-V_{ds}/\upsilon_T}\right) \quad (1.2)$$

where m is the body factor, which can be obtained as

$$m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\varepsilon_{si}/W_{dm}}{\varepsilon_{ox}/T_{ox}} \approx 1 + \frac{3T_{ox}}{W_{dm}} \quad (1.3)$$

where μ_0 is the low field mobility, $\upsilon_T = kT/q$ is the thermal voltage, V_{th} is the threshold voltage, C_{dm} is the depletion layer capacitance, W_{dm} is the maximum depletion layer width, T_{ox} is the oxide thickness, k is the Boltzmann's constant, q is the electron charge and T is the temperature.

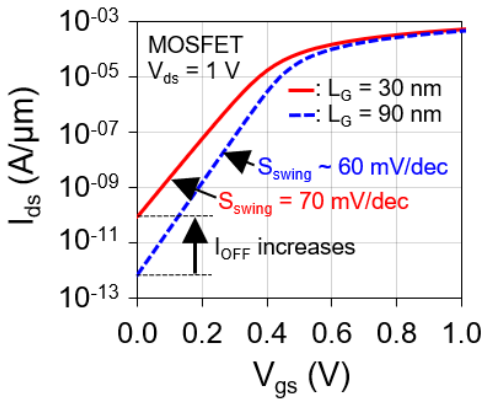

Fig. 1.6 Transfer characteristics (I_{ds}-V_{gs}) of a MOSFET for gate lengths (L_G) of 30 nm and 90 nm at V_{ds} = 1 V.

Subthreshold swing (S_{swing}) refers to a measure of how efficiently a transistor can control the flow of current in its subthreshold region. It is a metric that quantifies the steepness of the transistor. S_{swing} is determined by the inverse of the subthreshold slope (SS) i.e. $S_{swing} = 1/SS$. In simpler terms, S_{swing} represents the gate voltage required to change subthreshold current by one decade [38]. The expression for S_{swing} is given by:

$$S_{swing} = \left(\frac{d(log_{10}I_{ds})}{dV_{gs}}\right)^{-1} = 2.3m\frac{kT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right) \quad (1.4)$$

$$S_{swing} \approx 60\left(1 + \frac{C_{dm}}{C_{ox}}\right) mV/decade \text{ @ } 300\ K \quad (1.5)$$

For long-channel devices, W_{dm} attain a high value due to low substrate doping ($N_A \sim 10^{15}$ cm^{-3}). Hence, C_{dm} is very low compared to C_{ox} and S_{swing} approaches 60 mV/decade at T = 300 K as per Eq. (1.5). As per Dennard scaling theory [45], the substrate doping must be upscaled for short channel devices. This increases C_{dm}, and therefore, for short channel devices, S_{swing} is usually found in the range of 70 to 120 mV/dec [46]. As technology generations advance, both supply voltage and V_{th} need to be proportionally reduced in order to ensure a high drive current capability. The degradation of S_{swing} and the increase in I_{OFF} of a scaled MOSFET can be observed in Fig. 1.6 when the device dimensions are scaled down. Short channel devices exhibit inadequate electrostatic control of the gate on the conducting channel due to SCEs such as V_{th} roll-off (dV_{th}) and drain induced barrier lowering (DIBL) [38].

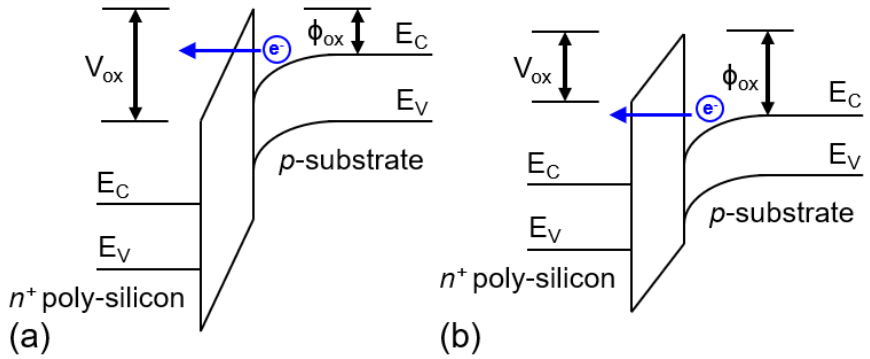

Fig. 1.7 (a) Fowler-Nordheim **(**FN) tunneling and (b) direct tunneling of electrons in a MOSFET illustrated using energy-band diagrams.

3. Gate oxide tunneling current (I_3):

Along with scaling other device dimensions, the gate oxide layer thickness also needs to be scaled down to maintain the electrostatic integrity over the channel. Consequently, the enhanced electric field strength in the vertical direction leads to electron tunneling across the oxide interface. As a result, a current is generated due to tunneling of electrons through the gate oxide [37]. The tunneling mechanism between the substrate and polysilicon gate can be primarily divided into two parts, as explained further:

1) **Fowler-Nordheim (FN) tunneling:** As shown in Fig. 1.7(a), the conduction band electrons from the substrate region tunnel through the triangular potential barrier, reaching the n^+ poly-silicon gate [42]. FN tunneling is valid only for $V_{ox} > \phi_{ox}$, where V_{ox} is the voltage drop across the oxide and ϕ_{ox} is the barrier height for electrons in the conduction band. Since most of the short channel devices operate at $V_{ox} < \phi_{ox}$, FN tunneling is negligible.

2) **Direct tunneling:** For devices with oxide thickness (T_{ox}) less than 1 nm, electrons from the inverted silicon surface directly tunnel through a trapezoidal potential barrier [46] as shown in Fig. 1.7(b). Hence, direct tunneling occurs only at $V_{ox} < \phi_{ox}$. In modern transistors, the direct tunneling current is a significant problem that can be mitigated by opting for high-k gate dielectrics like HfO_2, ZrO_2, etc. instead of thin oxides, which are the preferred choice.

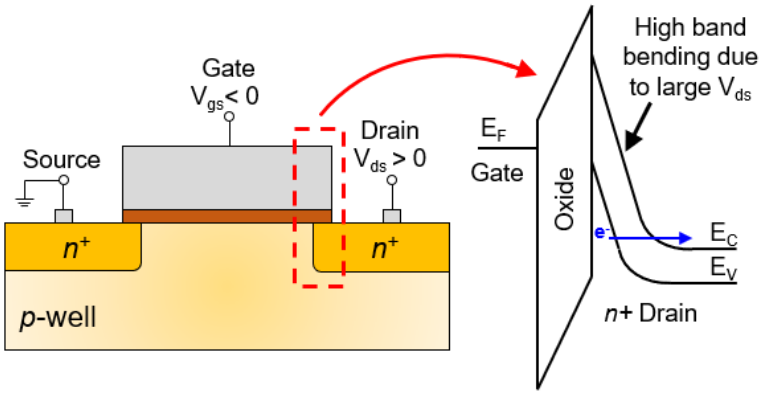

Fig. 1.8 Illustration of GIDL in a bulk MOSFET via band-to-band tunneling (BTBT) using energy band diagrams. The direction of the arrow in the energy band diagram indicates the flow of electrons.

4. Gate induced barrier lowering current (I_4):

Fig. 1.8 illustrates the energy band diagram of an *n*-type MOSFET with gate overlap region for a negative gate voltage ($V_{gs} < 0$) and a high drain voltage ($V_{ds} > 0$). A sufficiently negative V_{gs}, resulting in a significant band bending at the oxide interface that exceeds or equals the E_g/q of the drain and causes BTBT [43]. The electrons located in the valence band of the *n*-type drain will tunnel through

the narrowed band gap and transition into the conduction band resulting into a current flow. Scaling of T_{OX} enhances the vertical field which increases gate induced drain lowering (GIDL) current thereby negatively impacting the device performance.

5. Channel punchthrough current (I_5):

Fig. 1.9 demonstrates the occurrence of punchthrough, which happens when the depletion regions due to source and drain merge due to the reduced channel length and increased reverse bias voltage. In short channel devices, the depletion regions have the potential to expand along the lateral direction. Decreasing gate length while maintaining the same doping level reduces the distance between the boundaries of the depletion regions [38]. Furthermore, an increase in the reverse bias across the junctions, along with a rise in the supply voltage, brings the junctions closer together which eventually results in punchthrough.

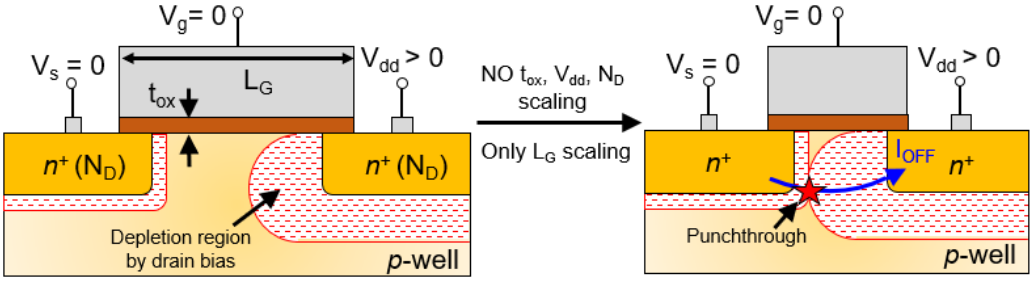

Fig. 1.9 Schematic illustration of punchthrough phenomena in MOSFET.

1.6 Evolution of Transistor Technology

1.6.1 Bulk Technology

In the early and mid-1950s, a significant advancement was achieved in growing pure, single-crystal silicon (Si), which led to the exclusive fabrication of MOS transistors on bulk Silicon substrates [48]. Bulk MOSFETs (Fig. 1.10) were originally produced on silicon wafers with a thickness of around 800 micrometers,

however, only the topmost micrometer of the wafer was utilized for manufacturing transistors [49]. The integrated circuit led to the development of CMOS technology, which combined *p*MOS and *n*MOS to reduce power consumption. Long channel bulk MOSFETs were effective but downsizing caused undesired SCEs [49, 50]. Some of them are described below:

1. **Degraded mobility and transconductance:** Downscaling transistor size as per Dennard's rules [45] requires increasing channel doping. This negatively impacts various device parameters such as increased V_{th}, mobility (due to increased scattering of carriers), and variability [49].

2. **Latch-up phenomena:** The origin of this issue can be attributed to the presence of parasitic *npn* and *pnp* transistors within the diffused regions of MOSFET. As a result, the device behaves like a thyristor, leading to a significant increase in current, thereby causing damage to the circuit [50].

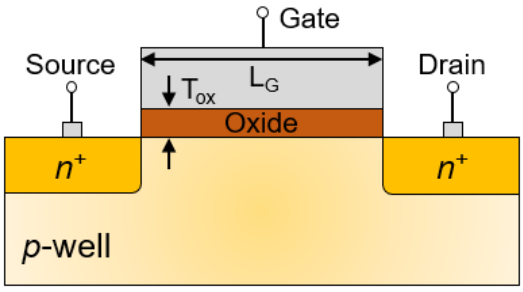

Fig. 1.10 Schematic of an *n*-type bulk MOSFET with a gate length of L_G and gate oxide thickness of T_{OX}.

1.6.2 Silicon-on-Insulator (SOI) Technology

To address these challenges and enable downscaling, Silicon-on-Insulator (SOI) technology was developed [51]. This technique involves isolating the channel region from the substrate through smart-cut technology [52], which helps overcome the limitations associated with these issues.

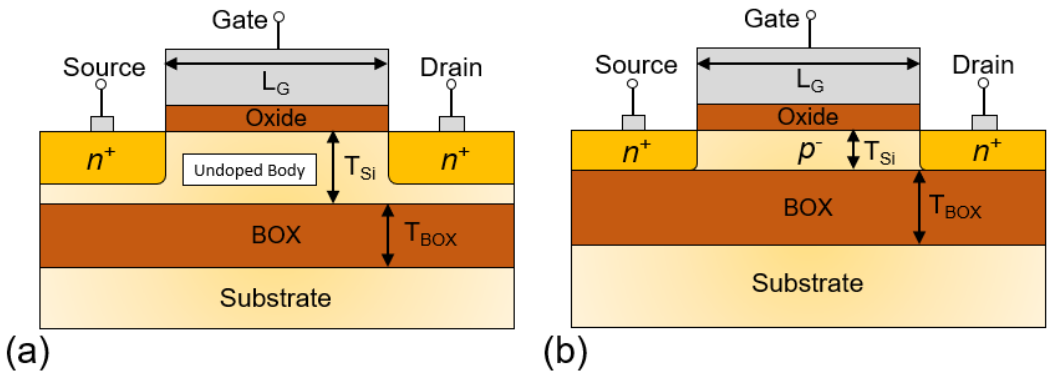

Fig. 1.11 Schematic of (a) partially depleted (PD) and (b) fully depleted (FD) Silicon-on-Insulator (SOI) MOSFET with a gate length of L_G, film thickness of T_{Si}, and buried oxide thickness of T_{BOX}.

Compared to bulk Silicon technology, SOI technology presents certain inherent benefits as follows:

1. **Dielectric Isolation:** SOI circuits employ isolated device regions with a dielectric material, enabling shorter inter device distances and eliminating latch-up concerns compared to traditional circuits [53].

2. **Reduced short channel effects (SCEs):** SCEs occurs when the electric field from the source/drain affects the channel potential. SOI devices solve this by limiting the depletion width, but the buried oxide (BOX) can still allow the field to penetrate and interfere with the channel.

3. **Circuit designing and processing:** SOI is easier to use for CMOS circuits than bulk Silicon because of fewer fabrication process steps [54] without wells and inter-device trenches. SOI also provides advantages such as improved performance, reduced processing requirements, and increased yield.

SOI MOSFETs can be broadly categorized in two types depending on the thickness of the silicon film (T_{Si}) as follows:

1. **Partially Depleted Silicon-on-Insulator (PDSOI):** A partially depleted SOI device has a depleted upper silicon film at zero gate bias, while the bottom part of the silicon film remains undepleted (Fig. 1.11(a)).

2. **Fully Depleted Silicon-on-Insulator (FDSOI):** A thin silicon film in a fully depleted SOI MOSFET allows a complete depletion of charge carrier at zero bias (Fig. 1.11(b)).

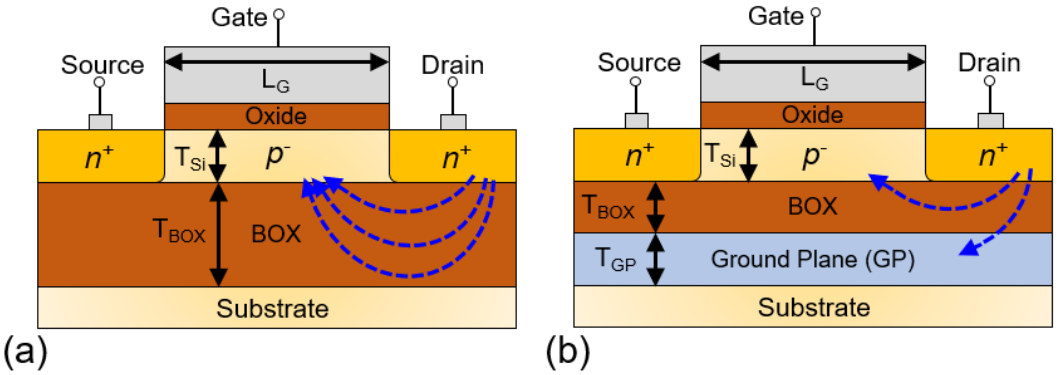

Fig. 1.12 Schematic diagram of (a) Ultra Thin Body (UTB) and (b) Ultra Thin Body BOX (UTBB) fully depleted (FD) SOI MOSFET with gate length of L_G and film thickness of T_{Si}.

In PDSOI devices, since the bottom of the Silicon film remains undepleted, it suffers from some undesired electrical effects [56, 56]. In PDSOI configurations, although the depletion region remains unaffected by the film thickness, variations in the number of accumulated holes in the body can give rise to changes in the body potential. This, in turn, has the potential to influence the electrical characteristics and modify the threshold voltage [57]. On the other hand, FDSOI technology maintains a constant depletion region irrespective of the bias condition due to a fully depleted channel [57]. By providing enhanced control over the Silicon film through the gate, FDSOI devices offer higher transconductance and exhibit reduced susceptibility to secondary effects such as DIBL, dV_{th}. Moreover, FDSOI can nearly ideal S_{swing}, making it well-suited for low-power applications [58].

FDSOI MOSFET can be classified into the following category:

- **Ultra Thin Body (UTB) SOI MOSFET:** Shrinking devices to the nanoscale limit poses a significant challenge in improving SOI MOSFETs, primarily due to DIBL. To overcome the issues faced by sub-50 nm SOI devices, one approach is to reduce the film thickness (T_{Si}) to 10 nm or even less [59, 60], resulting in ultra thin body (UTB) SOI MOSFETs. In FDSOI configurations, the thickness of the silicon film plays a crucial role in controlling the electric field. UTB devices exhibit nearly flat potential lines, which enhances the electrostatic stability of the transistor [52]. Moreover, FDSOI devices utilize a thin BOX, which helps mitigate SCEs by limiting the lateral field that can penetrate through the buried oxide from the source/drain depletion regions [61] (Fig. 1.12 (a)).

- **Ultra Thin Body and BOX (UTBB) SOI MOSFET:** The incorporation of an ultra thin BOX improves the electrostatic integrity of the transistor, thus allowing for further downscaling in comparison to UTB MOSFET as shown in Fig. 1.12(b). The primary advantage of utilizing a Ground Plane (GP) [53] is that a significant portion of the electric field lines conclude below the BOX, thereby minimizing the penetration of the lateral field. However, this approach results in an elevation of body effect and capacitance, leading to a decline in the performance of the device. Despite the integration of a GP structure, increased capacitance and body effect adversely affect the functionality of UTBB MOSFET [60]. Hence, it is essential to explore alternative devices that can effectively address SCEs.

1.6.3 Multi-gate transistor architectures

The requirement for MOS transistor scaling for improved performance has resulted in a significant advancement in transistor architecture. As a result, multiple-gate (also referred to as multi-gate) transistors have been developed to enhance device performance and minimize SCEs.

1. **Double Gate (DG) MOSFET**: In 1984, Sekigawa introduced a modified MOS architecture inspired by the UTBB structure. This design involved incorporating a second gate at the bottom and keeping the thickness of BOX same as the front gate oxide [62]. In Double Gate (DG) operation, the front and back gates of the device can either be electrically connected to each other, forming a symmetric MOS configuration, or they can be operated independently with separate biases, resulting in an asymmetric MOS configuration. This device offers several significant advantages [63, 64] as follows: 1) Enhanced immunity from SCEs, 2) High g_m, 3) Optimal S_{swing}, 4) Improved I_{ON}/I_{OFF}, etc.

2. **FinFET:** Due to the complexity in the fabrication process for perfect positioning of front and back gates [65] in a DG MOSFET, a fully DEpleted Lean-channel TrAnsistor (DELTA) was developed [66]. This structure consisted of vertically positioned silicon film with gates on both sides of the silicon film and was named DG FinFET [67]. In contrast to the horizontal channel of planar MOSFETs, FinFET features a vertical channel referred to as a fin. By adding more fins to the structure, the current drive can be improved. FinFETs have a vertical design that provides enhanced immunity to SCEs and allows for high packing density [68].

3. **Gate-All-Around (GAA) Transistor:** The use of Gate-All-Around (GAA) configuration can enhance the gate controllability of the transistor. This configuration surrounds the channel region with the gate electrode, resulting in improved gate controllability compared to other structures [69]. As a result, it significantly reduces SCEs. Examples of GAA configurations can be: 1) Nanowire FET [70] and 2) Nanosheet [71]. GAA transistor is a widely used structure in logic applications [72, 73] due to its excellent short channel characteristics. GAA FETs are considered as promising structures for replacing FinFETs in advanced technology nodes due to their excellent gate controllability.

1.7 Conclusion

The extensive dedication to research and innovation in the analog/RF field has resulted in the extensive adoption of CMOS devices in wireless and communication domains. The reduction in transistor size significantly contributes to improved speed, area, and other factors. However, this downsizing also presents challenges due to the emergence of SCEs such as DIBL and dV_{th}. Short channel devices experience higher I_{OFF} and face trade-offs when considering various analog/RF performance metrics. To suppress these SCEs, one can utilize SOI and multi-gate transistor architectures such as DG SOI MOSFET and GAA Nanowire FETs for advanced technology nodes. Still, CMOS technology requires separate fabrication process for *n*MOS and *p*MOS transistors.

1.8 Organization of Thesis

The thesis organization is described as follows:

Chapter 1 gives an overview of the motivation for analog/RF systems and the evolution of CMOS technology in analog/RF applications. Need for transistor scaling and trade-offs in analog/RF performance metrics are discussed. The drawbacks of bulk technology followed by the evolution of SOI technologies and transistor architectures described.

Chapter 2 introduces the concepts of three-gated (3G) and twin-gate (2G) reconfigurable field effect transistor and its operation. Advantages and transfer characteristics of reconfigurable transistors are also discussed in this chapter.

Chapter 3 provides a detailed assessment of analog/RF performance of RFET (both 3G and 2G) at low current drives by benchmarking them with a conventional MOSFET. Parasitic capacitance of both RFET and MOSFET is explained using an equivalent capacitance model.

Chapter 4 discusses the architecture optimization techniques in RFET devices for suppressing the voltage gain bottleneck and for enhancing other analog/RF metrics.

Chapter 5 provides a summary of the conclusions derived from the research conducted in the thesis, while highlighting potential areas for future work.

Chapter 2

Reconfigurable Field Effect Transistor (RFET)

2.1 Challenges in Scaling of Nanoscale Devices

In nanoscale device, SCEs are predominant due to poor gate controllability. This can be suppressed through the multigate transistors as discussed in the previous chapter. Multigate transistors support further scaling through the advancements in advance processes, including the deposition of thin oxide, enhanced junction profiles, and novel contact materials [74]. The introduction of FinFET architecture, which greatly enhances channel electrostatics, has made it possible to scale down gate length to 15 nm at the 7 nm technology node [75]. Pushing the limits of fin-width scaling below 5 nm thickness is anticipated to lead to performance deterioration due to variability in fin-width across the channel and shifts in threshold voltage (V_{th}) [76]. Even the advanced process integration methods can't ensure uniformity of the fin along the channel. Thus, various variabilities and quantum confinement effects are expected to impose a fundamental limitation on the scaling of fin-width [77].

As the scaling continues to follow the projections of Moore's Law [2], many effects such as SCEs and random dopant fluctuations become dominant in the nanoscale regime [78]. As a result, the reliability of MOSFET operation is being challenged, and the fabrication process is becoming more complex [76]. The conductivity of contacts critically determines the overall chip performance as they connect transistors in close proximity to each other and to metal interconnect layers, serving as the sole path for current flow between individual transistors and the global circuitry [80]. The source/drain (S/D) contact area has seen a tremendous reduction (~75%) in 7 nm technology node as compared to 22 nm technology node [75]. The significant reduction in surface area may result in dominance of contact resistance (R_C) in the upcoming technology nodes compared to channel resistance [81]-[83]. For a current contact resistivity of 2×10^{-9} Ω-m [77], the performance of FinFET will experience a substantial degradation when

the contact gate pitch (CGP) falls below ~ 40 nm [77]. This prompts a need to explore an alternative approach that addresses the issue of R_C. Reconfigurable field-effect transistor (RFET) presents an inherent solution by employing metal-semiconductor (M-S) junctions at source and drain, mitigating concerns related to the complexity of the fabrication process and the associated cost (low thermal budget) [84].

Also, conventional CMOS technology provides either *n*-type or *p*-type operation based on the fabrication process, which restricts circuit density. However, by altering the polarity of biases, RFETs can function as both *n*-type and *p*-type devices, eliminating the necessity of manufacturing a separate *p*-type device as in a CMOS counterpart. This capability enables additional functionality within a single device [88]. This also ensure that the circuit density can be enhanced without drastic scaling of the device dimensions.

2.2 Reconfigurable FET

RFET is an undoped device, which does not require physical doping to enable switching between *n*-type and *p*-type operation modes [84]-[99]. Instead of physical doping, RFET uses electrostatic doping to generate mobile carriers through an external voltage. RFETs provide transistor level reconfigurability, allowing for both static and dynamic runtime programming [97]. By incorporating CMOS compatible reconfigurable transistors as supplementary components, the versatility of electronic systems can be enhanced without the requirement for scaling, resulting in improved logic expressiveness and decreased costs per fundamental logic function [101].

The programmable feature of RFET has significant potential for realizing high-density digital logic circuits like logic gates, AND-OR-Invert or OR-AND-Invert logic [91], one-bit Arithmetic Logic Unit (ALU) [100], and power-gated differential cascade voltage switch logic [102]. High retention capacitorless dynamic random-access memory (DRAM) for standalone [103] and embedded [104] applications have been demonstrated using RFET. Hardware security

features like watermarking [105], logic locking and split manufacturing [106], and delay-invariant logic gates [107] have been proposed using RFET. RFETs typically have two gate electrodes: one for selecting the type of charge carrier (electrons or holes) called polarity gate (PG) and the other gate called control gate (CG) for modulating the channel conductance and current.

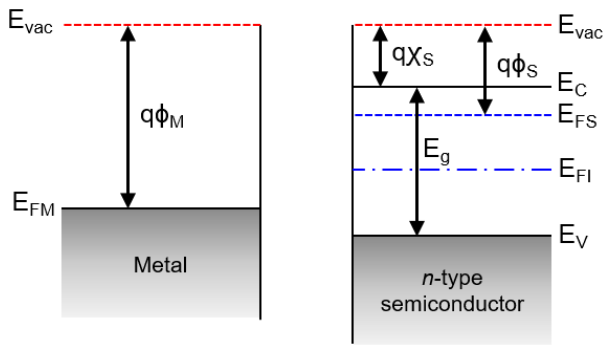

Fig. 2.1 Energy band diagram of metal and *n*-type semiconductor [38].

2.3 Metal Semiconductor Contact

The architecture of RFET incorporates a metal (M) - semiconductor (Si) junction. The nature of this junction, which combines a metal and a semiconductor (M-S), can result in either a rectifying Schottky contact or a non-rectifying (Ohmic) contact, depending on the work function and electron affinity of the metal and semiconductor [37]. Fig. 2.1 illustrates the energy band diagram of the metal and (*n*-type) semiconductor prior to junction formation, where various energy levels are represented, including the work function of the metal (ϕ_M), the electron affinity of the semiconductor (χ_s), the work function of the semiconductor (ϕ_S), the vacuum energy level (E_{vac}), the conduction band energy level (E_C), the valence band energy level (E_V), and the Fermi energy level (E_F) [37]. The work function (ϕ) is defined as the energy required to move an electron from E_F to E_{vac}, while the electron affinity (χ) represents the energy difference between E_{vac} and E_C. In metals, where the energy band between E_C and E_V is zero, the work function and electron affinity are equivalent. To gain insights into the current conduction behavior in the RFET, it is necessary to examine the characteristics of Schottky contacts.

2.3.1 Schottky Contacts

Prior to the formation of the metal-semiconductor (M-S) junction, the Fermi levels of the metal (E_{FM}) and the semiconductor (E_{FS}) are misaligned (Fig. 2.1). To establish alignment between E_{FM} and E_{FS}, resulting in an equilibrium state, charge transfer occurs from the semiconductor to the metal. This process leads to the formation of a Schottky contact [38]. The formation of Schottky contacts is possible in two scenarios, depending on the type of semiconductor described as follows:

1) *n*-type semiconductor ($\phi_M > \phi_n$):

In the case of *n*-type semiconductors, electrons from higher energy levels of semiconductor moves towards the lower energy levels of metal resulting in a depletion or space charge region at the junction as shown in Fig. 2.2(a).

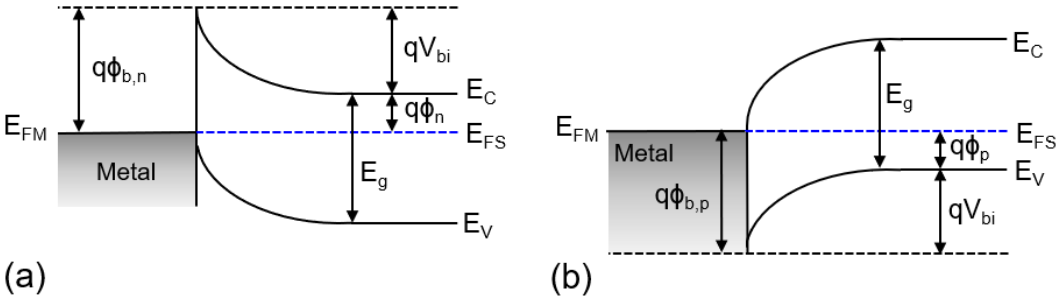

Fig. 2.2 Illustration of energy band diagram of metal with (a) *n*-type semiconductor and (b) *p*-type semiconductor junction [38].

The potential barrier height for electrons, as seen from the metal side to move to E_C represented by $q\phi_{b,n}$, is known as Schottky Barrier Height (SBH) for electrons and is given by [38]:

$$q\phi_{b,n} = q(\phi_M - \chi_{s,n}) \tag{2.1}$$

On the other hand, the potential energy barrier as seen from the semiconductor side for electron, to move to the metal side is known as built-in potential (V_{bi}) and is given by [38]:

$$qV_{bi} = q(\phi_{b,n} - \phi_n) \tag{2.2}$$

2) *p*-type semiconductor ($\phi_M < \phi_p$):

Similar to the *n*-type semiconductors, the depletion region is also created when the holes from the *p*-type semiconductor move towards the metal energy level at equilibrium (Fig. 2.2(b)). SBH for holes is given by [38]:

$$q\phi_{b,p} = E_g - q(\phi_M - \chi_{s,p}) \tag{2.3}$$

2.4 Conduction Mechanisms through Schottky Barrier

Only the conduction mechanisms in the *n*-type semiconductor are explained here i.e. the condition where, $\phi_M > \phi_n$. The conduction across the Schottky barrier is influenced by the applied bias and can be categorized into three distinct types as shown in Fig. 2.3 [38]:

1. **Thermionic Emission:** During thermionic emission, electrons acquire sufficient energy (~ SBH) and crosses the energy barrier. The current density of thermionic emission is dependent on factors such as temperature (*T*), the height of the energy barrier ($\phi_{b,n}$), and the effective mass of the carrier (*m**). At room temperature, the equation of thermion conduction is shown below [108]:

$$J_{TE} = A^* T^2 exp\left(-\frac{q\phi_{b,n}}{kT}\right) \tag{2.4}$$

where *A** = Richardson's constant given by,

$$A^* = \frac{4\pi q m^* k^2}{h^3} \tag{2.5}$$

2. **Field Emission:** The applied field provides enough energy for certain electrons to tunnel through the barrier near the conduction band, a process known as field emission as shown in Fig. 2.3.
3. **Thermionic Field Emission:** Electrons that are thermally excited and possess higher energy than the conduction band, but not enough to surpass the barrier, can also tunnel through the barrier when an electric field is present. This type

of tunneling is known as thermionic field emission. Both field emission and thermionic field emission are significantly impacted by the tunneling width at M-S junction. In heavily doped semiconductors, the tunneling width at M-S junction become very low, which allows for current to flow via these two phenomena [108]. On the other hand, in lightly doped semiconductors, the effects of field emission and thermionic field emission are relatively negligible when compared to thermionic emission, due to the larger tunneling width.

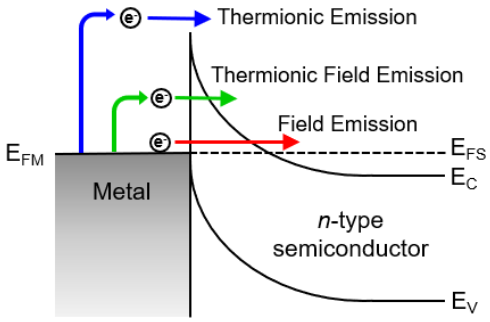

Fig. 2.3 Different mechanism responsible for conduction at M-S junction.

2.5 Reconfigurable Field Effect Transistor

The concept of RFET [84]-[99] originates from the Schottky Barrier Field Effect Transistor (SBFET), which employs two M-S junctions at the source and drain and uses a single gate for current flow. However, SBFETs suffer from ambipolar behavior, which can be suppressed by adding another gate at the source side. Later, these two gates are separated and controlled independently to achieve reconfigurability.

A RFET involves two gates: control gate (CG) and the polarity gate (PG). To allow carrier injection from the source and drain to semiconductor via tunneling, two M-S Schottky junctions are required. An RFET consists of metal (typically NiSi [85]) for S/D along with an intrinsic Si-body.

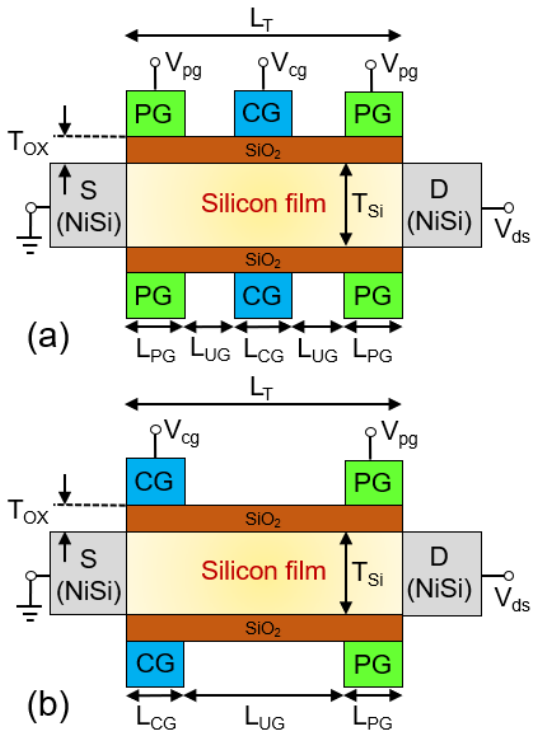

Fig. 2.4 Schematic representation of (a) RFET type-A (RFET-A) and (b) RFET type-B (RFET-B) in DG configuration.

RFETs can be broadly classified into two types based on the position of CG and PG as tri-gated (RFET-A) [85, 86, 88, 89, 91, 92, 93, 95, 98, 99] and twin-gate (RFET-B) [87, 90, 94, 96, 97]. RFET-A consists of one control gate (CG) and two polarity gates (PG)) while RFET-B consists of one CG and one PG. The corresponding schematic diagrams are shown in Fig. 2.4(a) and Fig. 2.4(b) for RFET-A and RFET-B, respectively. The length of CG, ungated region (UG) and PG is represented by L_{CG}, L_{UG} and L_{PG}, respectively. RFET-A includes two PG at the source (S) and drain (D) side, as well as a CG in the middle. In contrast, RFET-B employs one CG at the source and PG at the drain. In both cases, the injection of carriers is performed by PG by modulating the tunneling width through V_{pg}, and the flow of carriers is regulated by CG voltage (V_{cg}). In RFET-A, this flow of carriers is regulated at the middle of the device (by V_{cg}), while in RFET-B, it is done at the source end (by V_{cg}). By applying a positive bias at the PG ($V_{pg} > 0$), electrons can be injected into the semiconductor to facilitate it as *n*-type, while a negative bias enables the injection of holes and facilitate the device

to be *p*-type, thereby achieving reconfigurability. The two PGs in RFET-A can be shorted and controlled with a single bias.

Since RFET-A employs a greater number of gates than RFET-B, it offers greater controllability, resulting in better subthreshold swing. However, using a higher number of gates also increases fabrication complexity and cost.

2.6 Operation of RFET

Silvaco ATLAS TCAD tool [109] is used to analyze RFET-A, RFET-B and MOSFET with appropriate models. The universal Schottky tunneling (UST) model utilizes effective electron and hole masses of $0.3m_o$ and $0.2m_o$, respectively, to capture current conduction at M-S junction via thermionic emission and tunneling. m_o denotes the rest mass of the electron [84]. Other models to capture the essential physics of concentration and field-dependence of mobility, and Auger and Shockley Read Hall recombination have been included in the TCAD simulation [109]. The calibration of transfer characteristics of GAA RFET (RFET-A and RFET-B) with experimental work [90, 93] is shown in Fig. 2.5. For further analysis, the same physical models have been carried out to investigate the DG RFET because of the same conduction mechanism.

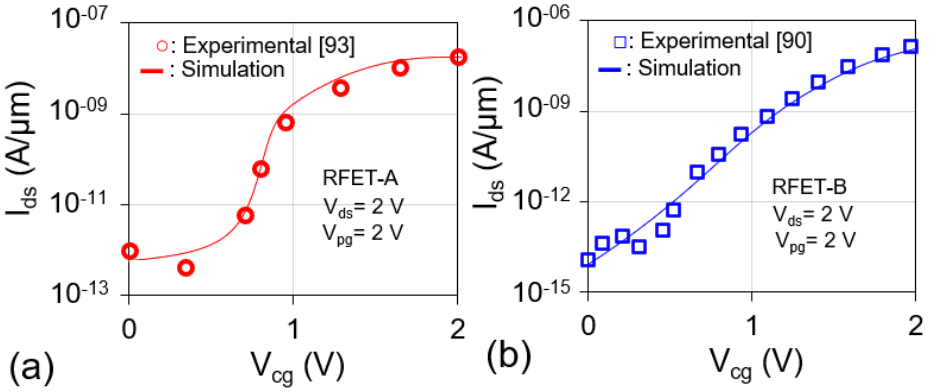

Fig. 2.5 Calibration of simulated results with experimental data for (a) RFET-A [93] and (b) RFET-B [90].

To explain the working of RFET-A and RFET-B, the total length (L_T) of 100 nm is considered for both the devices with following device dimensions:

- RFET-A: $L_{PG} = L_{UG} = L_{CG} = 20$ nm
- RFET-B: $L_{CG} = L_{PG} = 20$ nm, $L_{UG} = 60$ nm

For both RFET topologies, silicon film thickness (T_{Si}) of 10 nm and SiO_2 layer thickness (T_{OX}) of 1.5 nm is considered. In both RFETs, a fixed workfunction of 4.6 eV is considered for NiSi S/D, which corresponds to a SBH of 0.43 eV. The workfunction of CG and PG in RFET-A and RFET-B is kept at 4.73 eV and 4.85 eV, respectively, to achieve reconfigurable behavior.

Flatband Condition: When no terminal voltages (V_{cg}, V_{pg}, V_{ds}) are applied on the RFET, the energy-bands are essentially flat as shown in Fig. 2.6(a)-(b). Neither the electrons nor the holes will be able to cross the Schottky barrier (SB), and hence, no current will flow in the device.

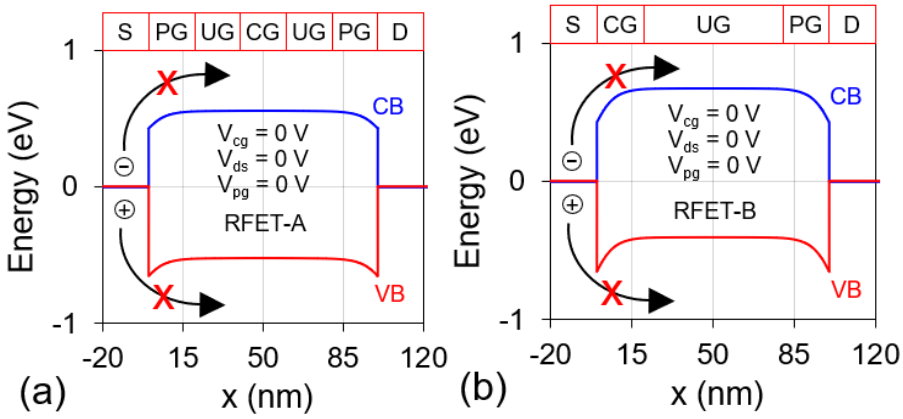

Fig. 2.6 (a) RFET-A and (b) RFET-B at flat band condition (zero bias).

***n*-type operation (OFF condition):** To configure RFET as an *n*-type device, a positive voltage at PG ($V_{pg} > 0$) is applied. This causes electrons to accumulate underneath the PG i.e. a field-induced 'doping' process that results in the region underneath the PG becoming *n*-type. Hence, energy bands bend downwards as shown in Fig. 2.7(a)-(b).

For RFET-A, I_{OFF} (I_{ds} at $V_{cg} = 0$) consists of thermionic emission as well as the thermionic assisted field emission of electrons at the M-S junction. Thermionic-assisted field emission is possible due to the high voltage at PG (V_{pg}

= 1.5 V) and the positive bias applied at drain (V_{ds} > 0) which enables the tunneling of electrons from source side to semiconductor. However, since the energy barrier between PG and CG is high, only a small number of carriers can cross the barrier and negligible current flows through the device. A similar case exists for RFET-B except that CG also regulates tunneling width of one of the SB. At V_{cg} = 0, the SB tunneling width for electrons (at the source side) is very large and I_{OFF} majorly consists of thermionic emission of electrons. Hence, RFET-B attains a lower I_{OFF} as compared to RFET-A as shown in Fig. 2.8.

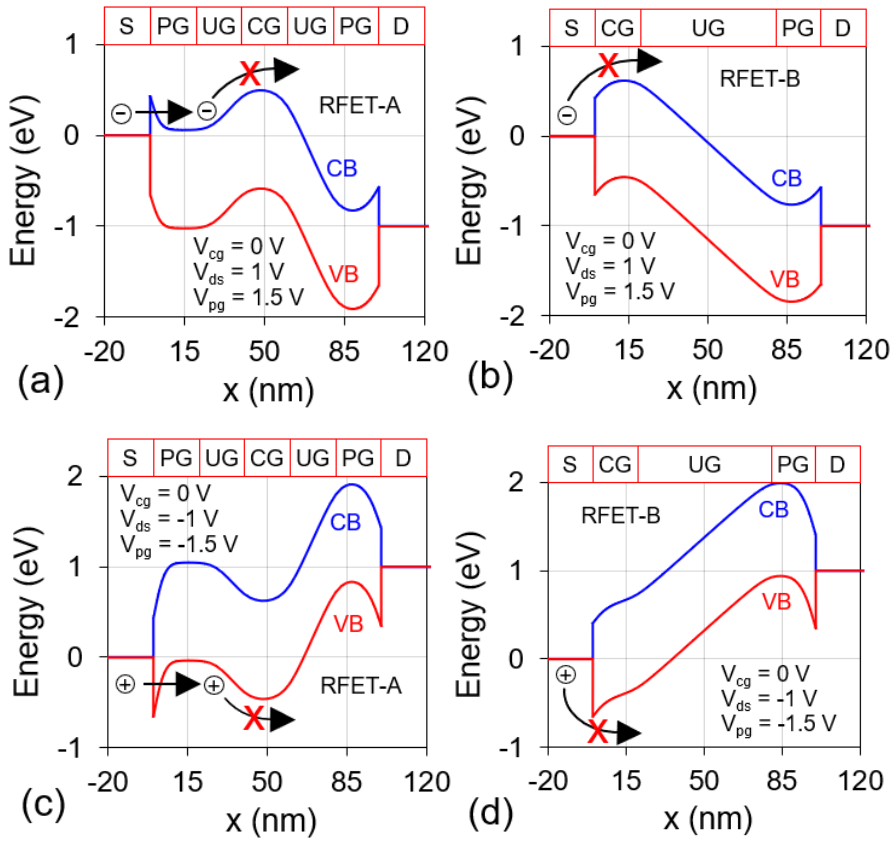

Fig. 2.7 Energy band diagram for *n*-type operation of (a) RFET-A and (b) RFET-B in OFF condition, and *p*-type operation of (c) RFET-A and (d) RFET-B in OFF condition.

***p*-type operation (OFF condition):** RFET can be operated as a *p*-type device by applying a negative bias to the polarity gate (V_{pg} < 0). Consequently, holes will accumulate beneath PG, resulting in an upward bending of the bands as shown in

Fig. 2.7(c)-(d). However, due to reasons similar to the case of *n*-type operation, extremely low current will be present at zero bias (V_{cg} = 0 V).

The subthreshold swing (S_{swing}) of RFET-A is influenced by thermionic emission between PG and CG, whereas for RFET-B, S_{swing} is determined by both thermionic emission (at low V_{cg}) and tunneling (at moderate V_{cg}) at M-S junction, which leads to two distinct slopes in the subthreshold regions [110]. Fig. 2.8 shows a degraded S_{swing} for RFET-B which is due to the V_{cg} dependent tunneling width at the source side SB. Consequently, higher V_{cg} is required to effectively modulate tunneling width, and in turn, the current [94]. In contrast, RFET-A does not rely on V_{cg} to control tunneling at M-S junction, which leads to a lower S_{swing} in comparison to RFET-B.

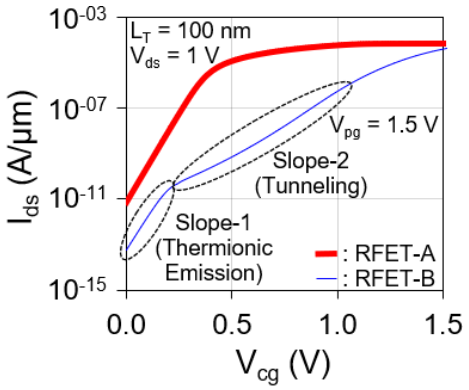

Fig. 2.8 Comparison of transfer characteristics (I_{ds}-V_{cg}) of RFET-A and RFET-B for n-type operation.

***n*-type operation (ON condition):** To turn-on RFET (A and B) in *n*-type mode, a positive bias is applied on CG which lowers the energy barrier underneath CG as shown in Fig. 2.9(a)-(b). For RFET-A, a decrease in the energy barrier between the ungated regions permits the electrons to flow unhindered towards drain terminal due to the electric field generated by V_{ds}. In the case of RFET-B, by applying $V_{cg} > 0$, the tunneling width at the source side M-S junction reduces, which enable the tunneling of electrons into the semiconductor and reach drain terminal because of the lateral electric field.

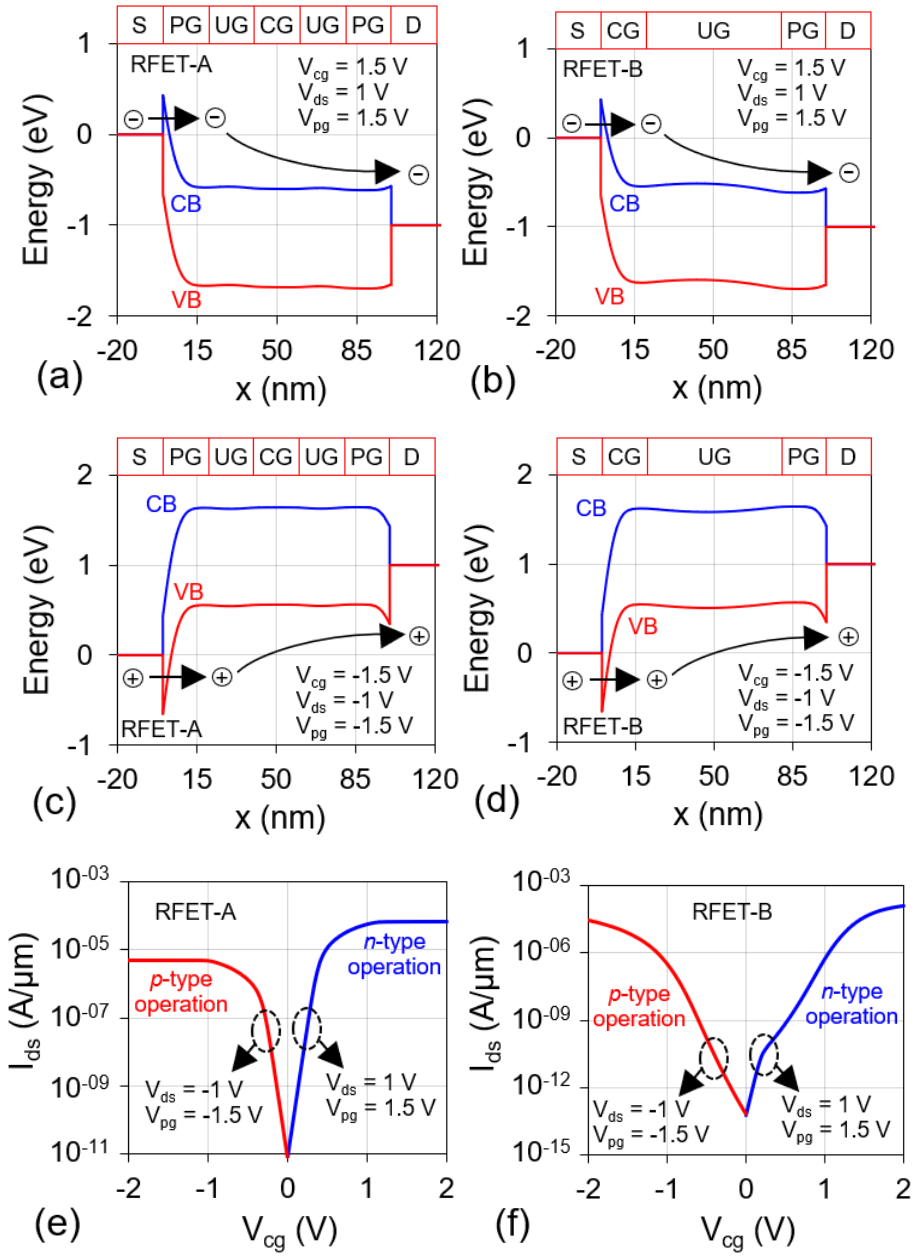

Fig. 2.9 Energy band diagrams illustrating *n*-type operation in (a) RFET-A and (b) RFET-B, *p*-type operation in (c) RFET-A and (d) RFET-B. Transfer characteristics showing of *n*-type and *p*-type operation in (e) RFET-A and (f) RFET-B.

***p*-type operation (ON condition):** Similarly, to turn-on the RFET in *p*-type mode ($V_{pg} < 0$), a negative bias is applied on CG which causes the energy bands to bend

upwards as shown in Fig. 2.9(c)-(d). Similar to the case of *n*-type operation, when a drain supply is applied ($V_{ds} < 0$), holes can flow smoothly through the channel and reach drain end.

Hence, RFET can achieve reconfigurability (both *n*-type and *p*-type operation) by applying appropriate biases as illustrated for RFET-A and RFET-B in Fig. 2.9(e) and Fig. 2.9(f), respectively.

2.7 Drain Current Characteristics of RFET

Characteristics of RFET can be categorized into two distinct parts - transfer characteristics and drain or output characteristics.

Since there are two distinct gates, two separate transfer curves exist: I_{ds} vs V_{cg} curve and I_{ds} vs V_{pg} curve. For explaining the characteristics, the following device dimensions are considered:

- RFET-A: $L_{PG} = L_{UG} = L_{CG} = 20$ nm ($L_T = 100$ nm)
- RFET-B: $L_{CG} = L_{PG} = 20$ nm, $L_{UG} = 60$ nm ($L_T = 100$ nm)

For RFET-A, the tunneling width of SB depends only on the applied bias on polarity gates. But for RFET-B, both the control gate and polarity gate are responsible for modulating SB width. The tunneling probability ($T_{n,p}$) through a barrier can be expressed using Wentzel–Kramers–Brillouin (WKB) approximation for a triangular barrier as [111],

$$T_{n,p} \propto exp\left(-\frac{4\sqrt{2m^*_{n,p}}\left(\phi_{B,n,p}\right)^{3/2}}{3q\hbar E}\right) \tag{2.6}$$

where, m^* is the effective mass of electron (n) or hole (p), ϕ_B is the SBH for electrons (n) or holes (p), $\hbar$ is the reduced Planck's constant, and E is the applied electric field across the barrier.

- **I_{ds}-V_{cg} characteristics:**

Fig. 2.10(a)-(b) shows I_{ds}-V_{cg} characteristics of RFET (A and B) at fixed V_{ds} (= 1 V) for different values of V_{pg} in *n*-type mode.

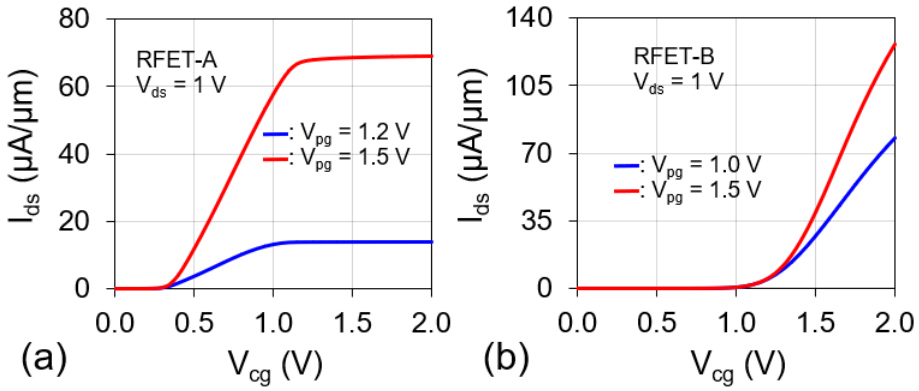

Fig. 2.10 I_{ds} vs V_{cg} characteristics for different V_{pg} of (a) RFET-A and (b) RFET-B at a fixed V_{ds} = 1 V.

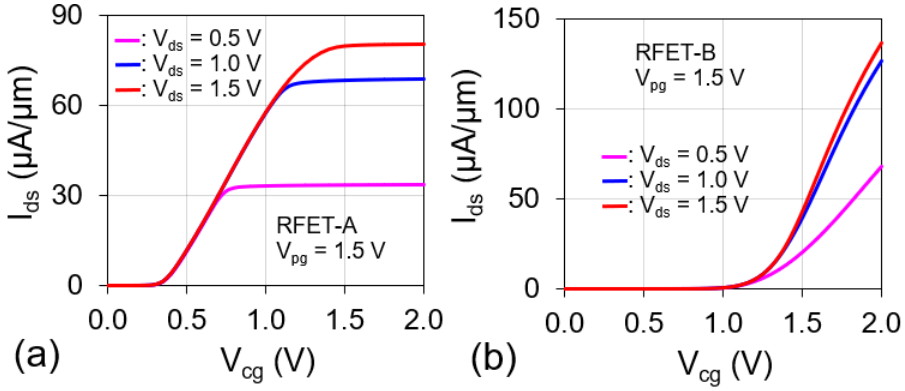

Fig. 2.11 I_{ds} vs V_{cg} characteristics for different V_{ds} of (a) RFET-A and (b) RFET-B at a fixed V_{ds} = 1 V.

An increase in the value of V_{pg} in RFET-A reduces the SB tunneling width which enhances the possibility of both the thermionic field emission and field emission of electrons i.e. drain current increases with V_{pg}. In RFET-B, SB tunneling width at the source side is governed by the control gate. For electrons to tunnel through the barrier (thermionic field emission), a high value of V_{cg} is required. At low V_{cg}, only thermionic emission of electrons is possible which contributes to a very low drain current. Hence, an appreciable amount of current is seen in the device only at high V_{cg} (> 1 V) in RFET-B. When V_{pg} is low, SB

tunneling width is high in drain region. Consequently, thermionic emission becomes more significant than the tunneling mechanism, and only a small number of electrons can pass through the barrier and reach drain terminal. However, with a high V_{pg}, the tunneling mechanism dominates over thermionic emission, resulting in a higher current.

Fig. 2.11(a)-(b) shows the I_{ds}-V_{cg} characteristics for various drain biases (V_{ds}) for a fixed V_{pg} of 1.5 V. A comparable pattern to that seen with V_{pg} (Fig. 2.10(a)-(b)) can be observed. This pattern arises because the barrier height at drain terminal decreases as V_{ds} increases. Consequently, a greater number of electrons can pass through the barrier due to both thermionic emission and tunneling.

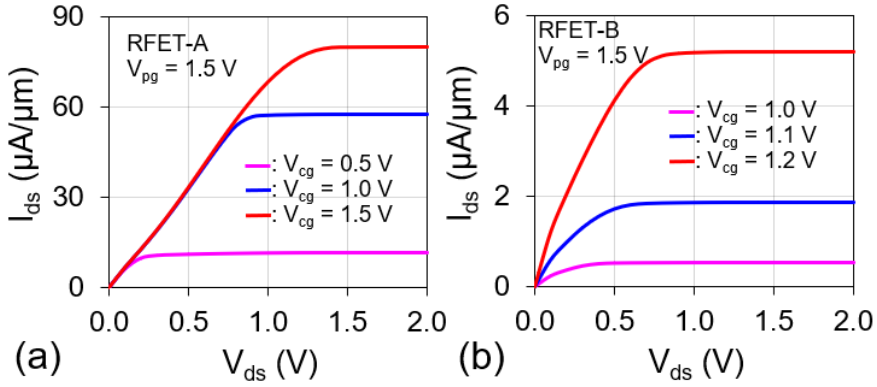

Fig. 2.12 Output characteristics (I_{ds} vs V_{ds}) for different V_{cg} of (a) RFET-A and (b) RFET-B at a fixed V_{pg} = 1 V.

- ***I*$_{ds}$-*V*$_{ds}$ characteristics:**

The output characteristics (I_{ds}-V_{ds}) of RFET for different values of V_{cg} at fixed V_{pg} (= 1.5 V) is shown in Fig. 2.12(a)-(b). As V_{ds} increases, the energy barrier for electrons, in both drain and ungated region move downwards. This results in a decrease in the barrier height at these locations, enabling more electrons to flow from the source. Ultimately, due to tunneling and thermionic emission at drain, the current increases linearly. However, after a certain voltage, the SBH at the drain becomes negligible because the higher voltage at the drain

causes metal Fermi level to significantly decrease. At this stage, only thermionic emission exists, and the current increases at a much slower rate due to the applied field for a given V_{cg}. If V_{pg} is decreased, the tunneling width increases, and fewer carriers are injected through the tunneling process, resulting in a lower current.

2.8 Conclusions

Reconfigurable Field Effect Transistor is an extension of Schottky-Barrier MOSFET having two separate gates which modifies its ambipolarity and provides unipolar *n*-type and *p*-type configuration. In this chapter reconfigurability in the two RFET architectures (RFET-A and RFET-B) are analyzed in detail through energy band diagrams and current characteristics. A good I_{ON}/I_{OFF} ratio of ~10^5 in RFET makes it suitable for logic applications. Among RFET architectures, RFET-B shows a lower I_{OFF} than RFET-A due to the dependence of tunneling width on the bias applied on control gate. Nevertheless, RFET-A exhibits enhanced S_{swing} as a result of superior gate control over the channel. The transfer characteristics of RFET resemble those of a conventional MOSFET.

Chapter 3

RFET for Analog/RF Applications

3.1 Introduction

At present, analog/RF applications in the market are dominated by the planar SOI technology [112]-[127]. Usually, multi-gated transistors (e.g. FinFETs) are not preferred over planar transistors because of their higher parasitic capacitance [128]-[136] which negatively affects the cut-off frequency (f_T) of the device despite providing better transfer characteristics. Among the SOI technologies, UTBB FD SOI technology stands out due to significantly better performance compared to bulk counterpart. Thus, UTBB FDSOI technology is well-suited for applications in communication systems, RF FEMs, mixed-signal SoCs, etc. [137]-[141]. Also, the existing CMOS technology requires distinct manufacturing processes for *n*MOS and *p*MOS transistors, resulting in limited logic circuit density. RFET, which can exhibit both *n*-type and *p*-type operation by applying an appropriate bias, have the potential to implement logic with fewer transistors as compared to complementary metal oxide semiconductor (CMOS) technology [101].

Apart from advantages of RFET in logic and memory [100]-[107], RFETs have shown potential for improving the power efficiency of analog circuits and implementing sensitive THz detectors [141]. High-gain differential pairs with lower area have been proposed with steep switching RFETs [143]. However, there is a gap in the literature regarding the effectiveness of RFET in analog and RF applications, as only a limited number of studies have been conducted in this area [143, 144]. Further research is required to evaluate the performance of RFET in analog/RF applications, particularly in low current drives for ULP operation. In modern handheld cellphones, the RF front-end module comprises digital cores that are surrounded by analog interface blocks. To be a competitive option for

mixed-signal applications, analog and RF functionality of RFET need to be investigated in detail.

3.2 Analysis of RFET and MOSFET for Low Current Levels

The main drawback of RFET is the lower current drive due to the presence of an ungated region which degrades analog/RF and digital performance. Thus, the potential of RFET for analog/RF applications need to be investigated at lower current levels (< 10 μA/μm) where performance is primarily dependent on the inherent architecture of the device. Hence, to analyze the analog/RF behavior of RFET, important figures of merit like transconductance (g_m), transconductance-to-current ratio (g_m/I_{ds}), Early voltage (V_{EA}), gain (A_V), gate capacitance (C_{gg}) and cut-off frequency (f_T) are benchmarked with a conventional double-gate (DG) MOSFET for same total source-to-drain length (L_T = 100 nm).

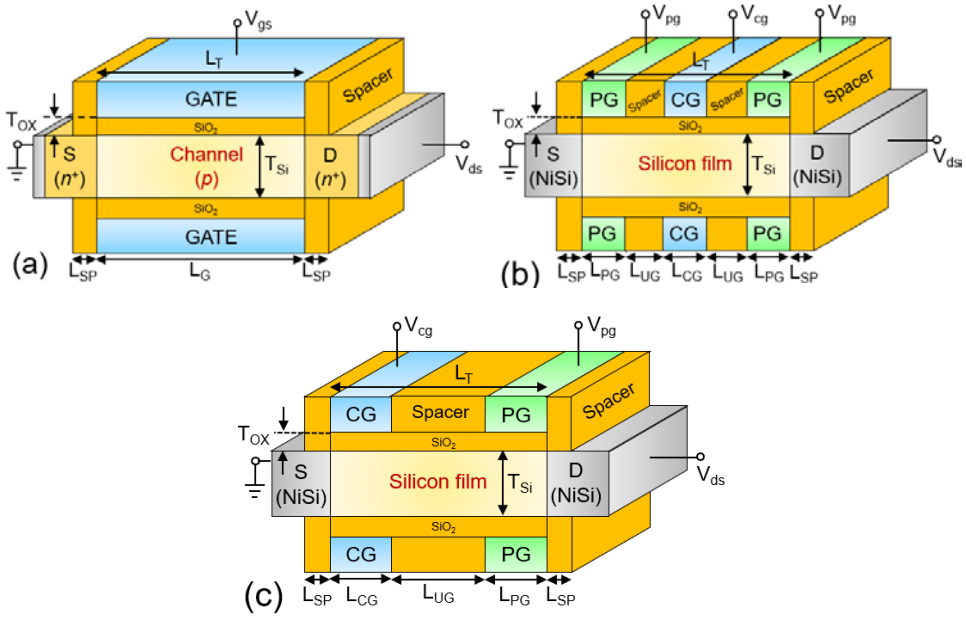

Fig. 3.1 Schematic representation of a DG (a) MOSFET, (b) RFET type-A (RFET-A), and (c) RFET type-B (RFET-B).

The schematic diagram of MOSFET, RFET-A and RFET-B in DG configurations are shown in Fig. 3.1(a)-(c). In both RFET topologies, the work function of S/D Nickel Silicide (NiSi) is kept at 4.6 eV, corresponding to a SBH

of 0.43 eV. The universal Schottky tunneling (UST) module is utilized to account for tunneling through the SB, employing effective masses of electrons ($0.3m_o$) and holes ($0.2m_o$), where m_o represents the rest mass of an electron. Other models have already been described in Chapter 2. For further analysis a silicon film (T_{Si}) of 10 nm, SiO_2 layer (T_{ox}) of 1.5 nm, and the length of SiO_2 sidewall spacer (L_{SP}) is fixed to 10 nm. In the ungated region (between the CG and PG) of both the RFETs, a SiO_2 spacer is used to isolate the PG and CG. Five different architectures for L_T = 100 nm are considered for RFET-A (Fig. 3.2(a)) and RFET-B (Fig. 3.2(b)) depending on the contribution of control gate length (L_{CG}), polarity gate length (L_{PG}), and ungated region length (L_{UG}).

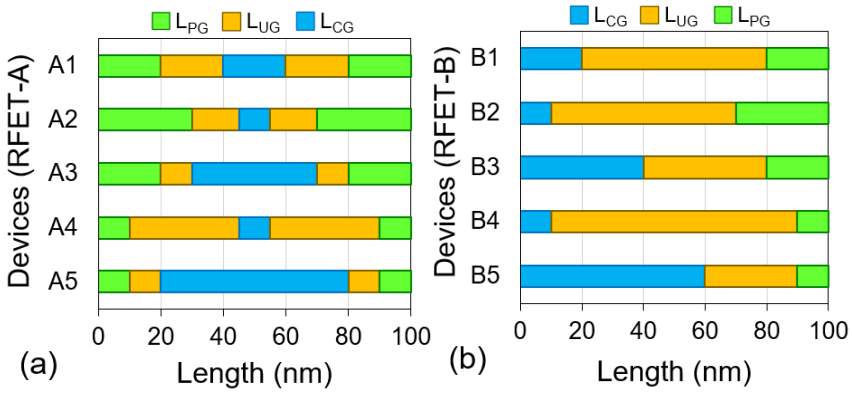

Fig. 3.2 Various combinations of lengths (L_{PG}, L_{UG}, L_{CG}) for (a) RFET-A and (b) RFET-B with for a fixed L_T of 100 nm.

Figure 3.3 shows the variation of f_T with I_{ds} in MOSFET and RFET devices. MOSFET shows a peak of f_T at ~300 μA/μm which is consistent with the results reported in the literature [145]. In contrast, RFET devices A1 and B1 show a peak of f_T at ~32 μA/μm and ~11 μA/μm, respectively, because of low current drive that results from (i) a larger SBH, and (ii) a higher device resistance because of the ungated region between PG and CG (Fig. 3.1(b)-(c)). The occurrence of the peak of f_T at a lower current level makes RFET a suitable device for ULP analog/RF applications. Therefore, in this work, only a low current level range (10^{-2} to 10^{1} μA/μm) is considered.

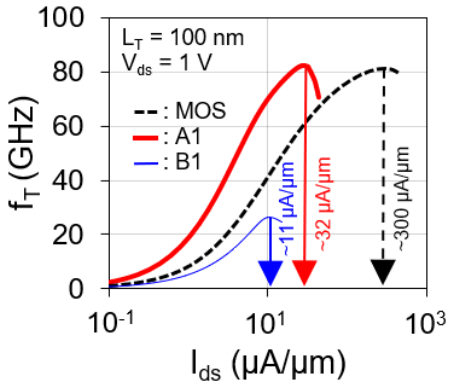

Fig. 3.3 Variation of cut-off frequency (f_T) with I_{ds} for DG MOSFET, RFET-A (A1), and RFET-B (B1) at V_{ds} = 1 V. V_{pg} = 1.5 V for RFET.

Fig. 3.4 shows the comparison of I_{OFF} (I_{ds} @ V_{gs} = 0 V) and average subthreshold swing (S_{swing}). S_{swing} can be obtained as [146]:

$$S_{swing} = V_{th}/\log_{10}\{I_{ds}(@\ V_{gs} = V_{th})/I_{ds}(@\ V_{gs} = 0)\} \quad (3.1)$$

where V_{th} is the threshold voltage of the device.

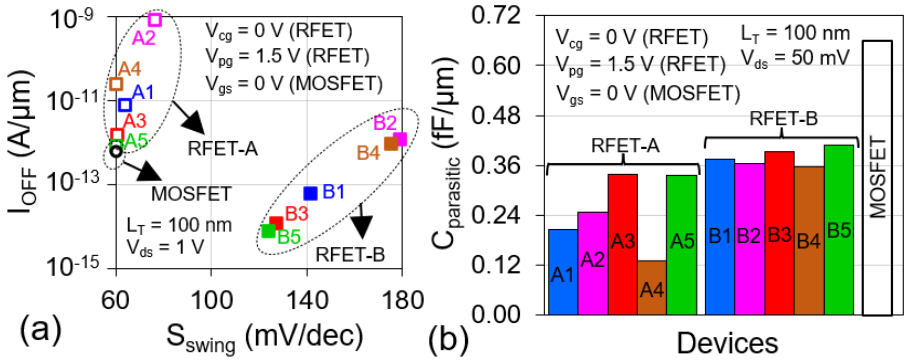

Fig. 3.4 (a) Comparison of off-current (I_{OFF}) and average subthreshold swing (S_{swing}) of DG MOSFET, RFET-A, and RFET-B at V_{ds} = 1 V. (b) Comparison of gate parasitic capacitance ($C_{parasitic}$) of RFET-A, RFET-B and DG MOSFET at V_{ds} = 50 mV. V_{pg} = 1.5 V for RFET.

RFET-B devices show a lower I_{OFF} than RFET-A devices, except B2, while RFET-A devices exhibit better S_{swing} than RFET-B devices (Fig. 3.4(a)). A clear understanding of the role of energy bands and the electron is crucial to differentiate the digital and analog/RF performance of RFET-A and RFET-B.

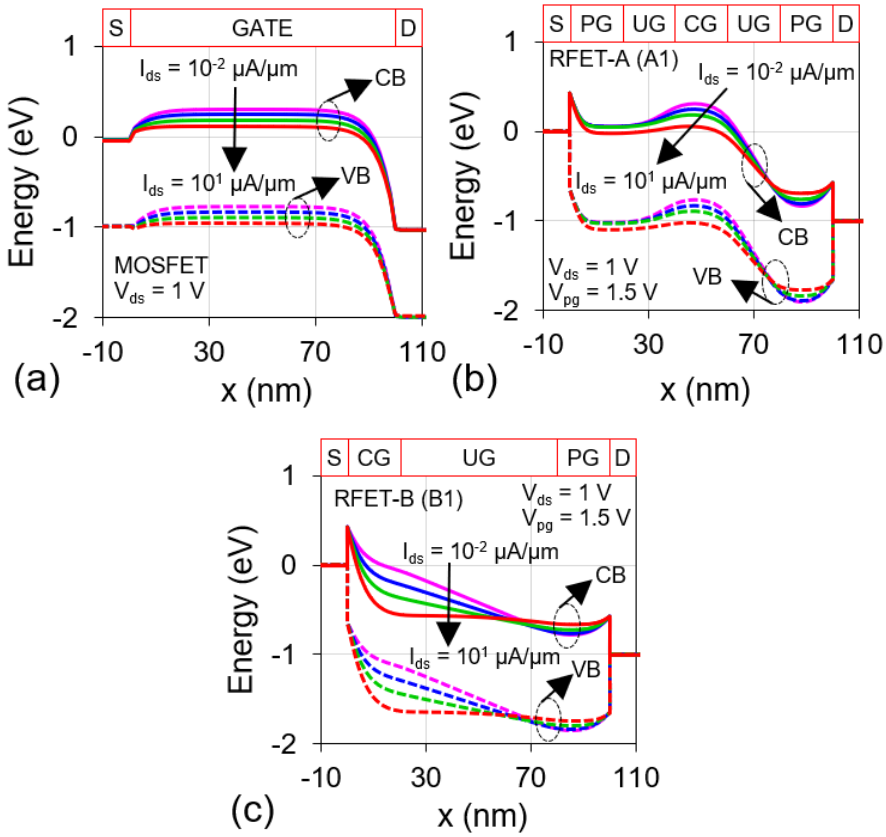

Fig. 3.5 Variation in conduction band (CB) and valence band (VB) energies along lateral direction (x) for different current levels (10^{-2} µA/µm to 10 µA/µm) in (a) DG MOSFET, (b) RFET-A (@ device A1) and (c) RFET-B (@ device B1). V_{pg} = 1.5 V (for RFET).

In MOSFET, the gate voltage (V_{gs}) facilitates conduction by lowering the energy barrier between the source and channel (Fig. 3.5(a)). However, in RFET-A, two PGs modulate the tunneling width at M-S junction through appropriate V_{pg} and enable the tunneling of electrons ($V_{pg} > 0$) and holes ($V_{pg} < 0$) from metal to semiconductor, while the control gate voltage (V_{cg}) modulates the thermionic barrier between PG and CG (Fig. 3.5(b)) and controls the flow of electrons (Fig. 3.6(a)). With an increase in I_{ds} (and subsequently V_{cg}), the concentration of electrons below CG rises. This results in a greater number of electrons being able to tunnel through the SB and enter the semiconductor. Similarly, in RFET-B, CG regulates tunneling width at source side SB (Fig. 3.5(b)) and enables tunneling of electrons ($V_{cg} > 0$) and holes ($V_{cg} < 0$) (Fig. 3.6(b)). At V_{cg} = 0 in RFET-B,

thermionic assisted field emission of electrons at the M-S junction is almost negligible due to larger SB width, and I_{OFF} majorly consists of thermionic emission, which is low due to SB height (= 0.43 eV). On the other hand, in RFET-A, I_{OFF} consists of both thermionic emission and thermionic-assisted field emission of electrons at the M-S junction. The fixed voltage at PG (V_{pg} = 1.5 V) enables the tunneling of electrons, resulting in thermionic-assisted field emission. Therefore, RFET-B shows lower I_{OFF} than RFET-A (Fig. 3.4(a)), but RFET-B suffers from degraded S_{swing} due to a high electric field near the M-S junction which reduces the control of the gate (CG) over the channel. as seen in chapter 2 as well.

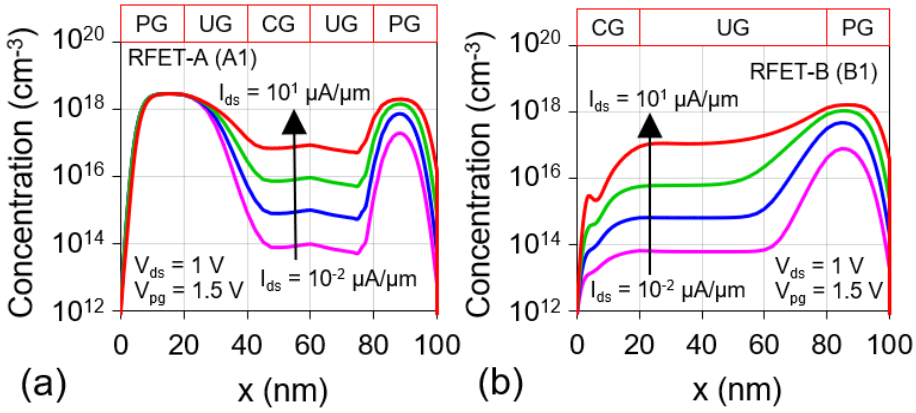

Fig. 3.6 Variation of electron concentration at the center of the film along the lateral direction (x) for different current levels in (a) RFET-A1 and (b) RFET-B1.

RFET-A exhibits a comparatively higher I_{OFF} and S_{swing} than DG MOSFET, which is attributed to its lower effective length (L_{CG} = 20 nm as compared to L_G = 100 nm of MOSFET). The energy band diagram shown in Fig. 3.5(a)-(c) clearly indicates that the gate controllability of both RFET topologies and DG MOSFET depends on L_{CG} and L_T, respectively. Even with a greater number of gates and higher I_{OFF} (only for RFET-A), both RFET topologies offer a smaller parasitic capacitance ($C_{parasitic}$) as compared to DG MOSFET as shown in Fig. 3.4(b). The reasoning for this unconventional result is given in the subsequent sections.

3.3 Extraction and Investigation of Various Parasitic Capacitance Components of RFET

Fig. 3.7(a)-(f) show the parasitic capacitive components associated with device structure and their equivalent capacitance model for RFET-A, RFET-B and MOSFET. The parasitic capacitive components associated with MOSFET and RFET are the outer ($C_{of\_e1\_e2}$), top ($C_{top\_e1\_e2}$), sidewall ($C_{side\_e1\_e2}$), and inner ($C_{if\_e1\_e2}$) fringing components between any two electrodes (e1 and e2 where they can be source, drain, CG, and PG [147]).

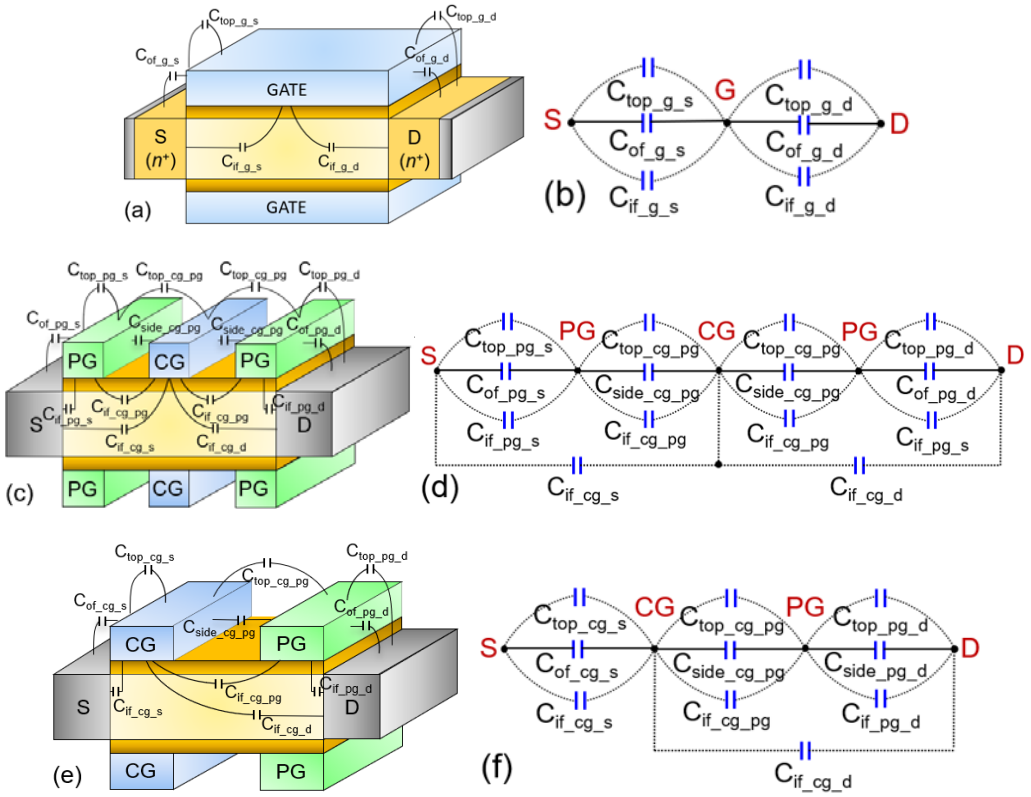

Fig. 3.7 (a) Schematic diagram showing parasitic components and (b) equivalent capacitance network for DG MOSFET. (c) Parasitic components for RFET-A and (d) equivalent network. (e) Parasitic components of RFET-B and (f) equivalent network.

The total parasitic gate capacitance ($C_{parasitic}$) is given by the sum of gate-to-source parasitic capacitance (C_{gs_para}) and gate-to-drain parasitic capacitance

(C_{gd_para}) i.e. $C_{parasitic} = C_{gs\_para} + C_{gd\_para}$. Due to symmetry in the architecture of MOSFET and RFET-A (with reference to CG), only the total parasitic capacitance between the gate (CG for RFET) and the source is taken into consideration since, $C_{gs\_para} \approx C_{gd\_para}$. However, for RFET-B, the analysis of the equivalent parasitic capacitance for both drain and source parts is carried out due to its asymmetrical architecture.

For MOSFET, the total parasitic capacitance between gate and source i.e. $(C_{gs\_para})_{MOS}$ is the parallel combination of $C_{top\_g\_s}$, $C_{side\_g\_s}$, and $C_{if\_g\_s}$ (Fig. 3.7(b)), and hence, is given as

$$(C_{gs\_para})_{MOS} = C_{top\_g\_s} + C_{side\_g\_s} + C_{if\_g\_s} \tag{3.2}$$

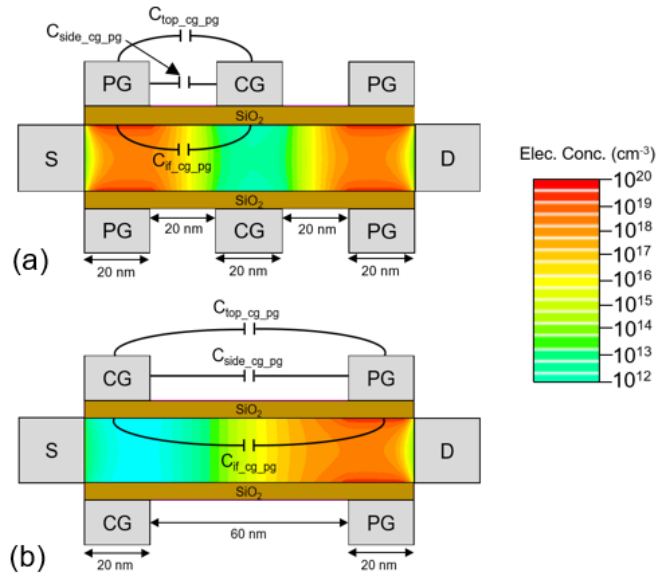

Fig. 3.8 Contour plots for electron concentration (cm^{-3}) in (a) RFET-A1 and (b) RFET-B1 along with various parasitic capacitive components in between CG and PG at V_{ds} = 50 mV and V_{pg} = 1.5 V.

For RFET-A shown in Fig. 3.7(d), additional terms are introduced to simplify the complex parasitic capacitance circuit. C_{pg_s} is the parallel combination of $C_{top\_pg\_s}$, $C_{of\_pg\_s}$, and $C_{if\_pg\_s}$ i.e. the total parasitic capacitance between PG and source given as follows

$$C_{pg\_s} = C_{top\_pg\_s} + C_{of\_pg\_s} + C_{if\_pg\_s} \quad (3.3)$$

Similarly, the total parasitic capacitance between CG and PG which is defined as C_{cg_pg} is the parallel combination of $C_{top\_cg\_pg}$, $C_{side\_cg\_pg,}$ and $C_{if\_cg\_pg}$ and can be expressed as

$$C_{cg\_pg} = C_{top\_cg\_pg} + C_{side\_cg\_pg} + C_{if\_cg\_pg} \quad (3.4)$$

C_{cg_s} is defined as the series combination of C_{pg_s} and C_{cg_pg}. Hence, C_{cg_s} can be approximated to the minimum of the two capacitances (C_{pg_s}, C_{cg_pg}) as

$$C_{cg\_s} = \text{series}\{C_{pg\_s}, C_{cg\_pg}\} = (C_{pg\_s} \times C_{cg\_pg})/(C_{pg\_s} + C_{cg\_pg}) \quad (3.5)$$

$$C_{cg\_s} \approx \text{minimum}\{C_{pg\_s}, C_{cg\_pg}\} \quad (3.6)$$

$C_{if\_cg\_s}$ is the inner fringing component between CG and the source. Finally, the total parasitic capacitance between the CG and source for RFET-A i.e. $(C_{gs\_para})_{RFET\text{-}A}$ is given by the parallel combination of C_{cg_s} and $C_{if\_cg\_s}$ as

$$(C_{gs\_para})_{RFET\text{-}A} = C_{cg\_s} + C_{if\_cg\_s} \quad (3.7)$$

In the case of RFET-B (Fig. 3.7(f)), the equivalent parasitic capacitance for the source and drain part will be different. Similar to the equation of MOSFET (Eq. (3.2)), $(C_{gs\_para})_{RFET\text{-}B}$ is given by the parallel combination of $C_{top\_cg\_s}$, $C_{of\_cg\_s,}$ and $C_{if\_cg\_s}$, as

$$(C_{gs\_para})_{RFET\text{-}B} = C_{top\_cg\_s} + C_{of\_cg\_s} + C_{if\_cg\_s} \quad (3.8)$$

Similar to Eq. (3.3)-(3.8) for RFET-A, for RFET-B, C_{pg_d} is defined as the parallel combination of $C_{top\_pg\_d}$, $C_{of\_pg\_d,}$ and $C_{if\_pg\_d}$, while C_{cg_pg} is defined as the parallel combination of $C_{top\_cg\_pg}$, $C_{side\_cg\_pg,}$ and $C_{if\_cg\_pg}$. C_{cg_d} is given by the series combination of C_{cg_pg} and C_{pg_d}. $C_{if\_cg\_d}$ is the inner fringing component between CG and drain. Hence, $(C_{gd\_para})_{RFET\text{-}B}$ is given by the parallel combination of C_{cg_d} and $C_{if\_cg\_d}$ as

$$(C_{gd\_para})_{RFET\text{-}B} = C_{cg\_d} + C_{if\_cg\_d} \quad (3.9)$$

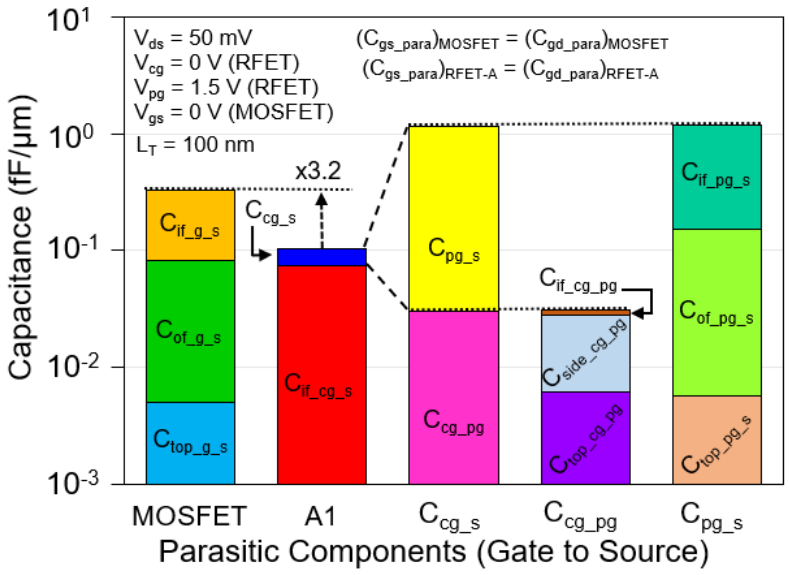

Fig. 3.9 Different components of gate-to-source parasitic capacitance extracted at V_{gs} = 0 V (for MOSFET), and V_{cg} = 0 V (for RFET-A (A1)) for V_{ds} = 50 mV and V_{pg} = 1.5 V (for RFET). The total parasitic capacitance will be twice of the value shown in the figure.

RFET-A (A1) is considered for the analysis. Due to the larger separation between CG and PG in RFET-A (A1), top ($C_{top\_cg\_pg}$ ~ 6.22×10^{-3} fF/µm) and sidewall ($C_{side\_cg\_pg}$ ~ 2.25×10^{-2} fF/µm) parasitic components will attain low values, and $C_{top\_cg\_pg}$ (~ 6.22×10^{-3} fF/µm) will be lower due to lesser coupling between gates at the top surface. Since V_{pg} = 1.5 V, an inversion layer is formed underneath PG as can be seen in Fig. 3.8(a). Due to this, the inner fringing component between CG and PG ($C_{if\_cg\_pg}$ ~ 2.21×10^{-3} fF/µm) gets screened and becomes negligible (Fig. 3.9). Consequently, C_{cg_pg} (~ 3.1×10^{-2} fF/µm) turns out to be significantly lower than C_{pg_s} (~ 1.12 fF/µm) as shown in equation (3.3), and therefore, an even smaller C_{cg_s} (~ 3.01×10^{-2} fF/µm) is obtained because of the series combination of Eq. (3.5) and (3.6). Comparing the inner fringing component between the gate and source in both devices (RFET-A and MOSFET), $C_{if\_cg\_s}$ (~ 7.39×10^{-2} fF/µm) will be smaller than $C_{if\_g\_s}$ (~ 2.5×10^{-1} fF/µm) because of the larger separation in RFET-A. Thanks to the series combination effect, $(C_{gs\_para})_{RFET-A}$ turns out (~ 1.03×10^{-1} fF/µm) to be significantly lower (~3.2 times) than $(C_{gs\_para})_{MOS}$ (~ 3.3×10^{-1} fF/µm).

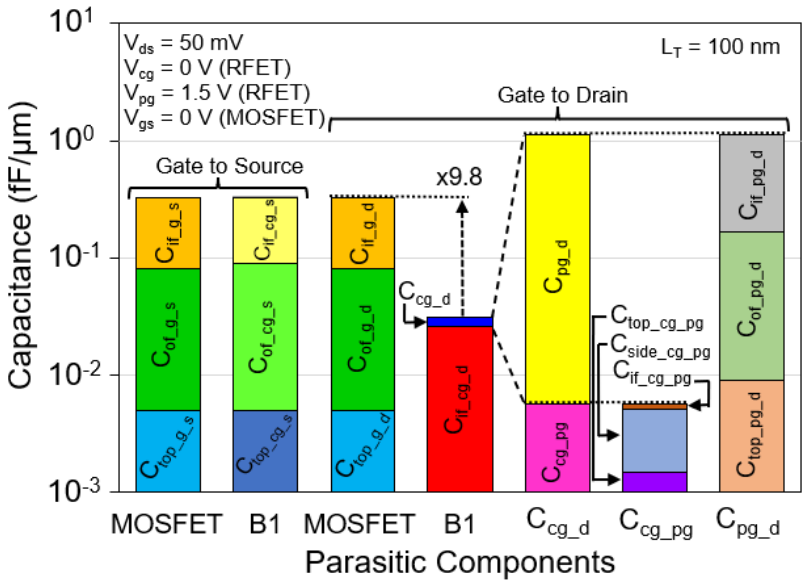

Fig. 3.10 Different components of gate-to-source and gate/CG-to-drain parasitic capacitance extracted at V_{gs} = 0 V (for MOSFET), and V_{cg} = 0 V (for RFET-B (B1)) for V_{ds} = 50 mV and V_{pg} = 1.5 V (for RFET).

The value of the parasitic capacitive components between gate and source will be almost equal for RFET-B and MOSFET because of the same parasitic components (Fig. 3.7(b), 3.7(f)) i.e. $(C_{gs\_para})_{MOS} \approx (C_{gs\_para})_{RFET\text{-}B}$ (Fig. 3.10). For MOSFET, due to its symmetry, $(C_{gs\_para})_{MOS} \approx (C_{gd\_para})_{MOS} \sim 3.3\times10^{-1}$ fF/µm. However, in RFET-B, the contribution of $(C_{gs\_para})_{RFET\text{-}B}$ and $(C_{gd\_para})_{RFET\text{-}B}$ in $(C_{parasitic})_{RFET\text{-}B}$ will be different because of asymmetry (with reference to CG). Due to V_{pg} (= 1.5 V), $C_{if\_cg\_pg}$ (~ 4.71×10^{-4} fF/µm) attains a very low value (Fig. 3.10) due to the inversion layer formed below PG (Fig. 3.8(b)), which directly translates to a significantly lower C_{cg_d} (~ 5.62×10^{-3} fF/µm) due to series combination, as seen in the case of RFET-A. This significantly reduces $(C_{gd\_para})_{RFET\text{-}B}$ (~9.7 times lower than MOSFET). Hence, the total parasitic gate capacitance ($C_{parasitic}$) in RFET-B is lower than MOSFET but higher than RFET-A due to the series combination of the source and drain part. Thus, due to the ungated region and applied V_{pg}, RFET shows a lower value of parasitic capacitance (Fig. 3.4(b)).

3.4 Analog/RF Figure of Merits of RFET for Low Current Levels

In the sub-100 nm regime, parasitic capacitance can influence the gate capacitance (C_{gg}). Due to a lower $C_{parasitic}$ (Fig. 3.9, 3.10), a significantly suppressed C_{gg} in RFET is observed (Fig. 3.11(a)).

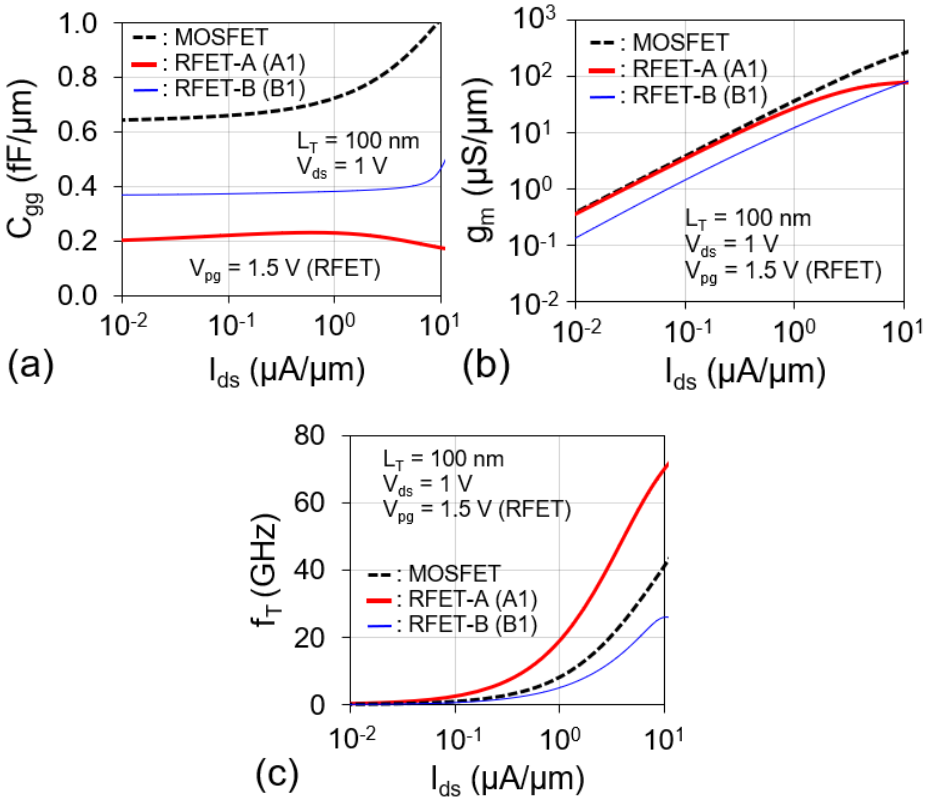

Fig. 3.11 Comparison of (a) total gate capacitance (C_{gg}), (b) transconductance (g_m), and (c) cut-off frequency (f_T) in DG MOSFET, RFET-A1, and RFET-B1 for various values of drain current (I_{ds}) at V_{ds} = 1V. V_{pg} = 1.5 V (for RFET).

As V_{cg} increases (I_{ds} increases), for RFET-A, the energy barrier between CG and PG decreases which results in the transfer of electrons from source to drain. This causes a reduction in $C_{if\_cg\_pg}$ and $C_{if\_cg\_d}$. Hence, at I_{ds} > 0.6 µA/µm, C_{gg} shows a dip. This effect is not seen in RFET-B because of the lower contribution of CG-to-drain parasitic capacitance towards C_{gg} as compared to the parasitic capacitance between CG-to-source (Fig. 3.10).

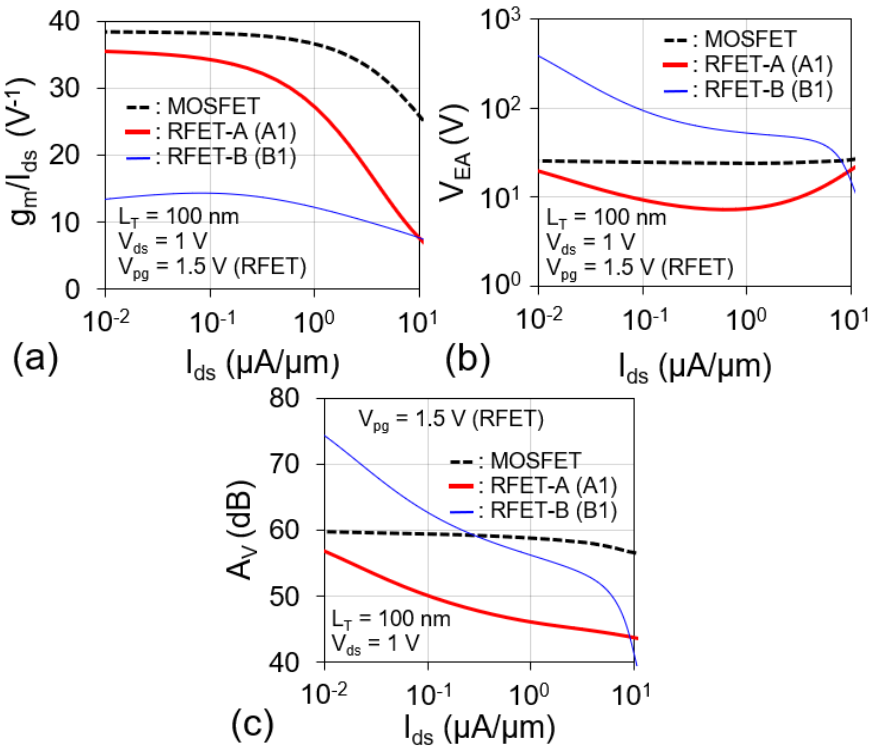

Fig. 3.12 Comparison of (a) transconductance to current ratio (g_m/I_{ds}), (b) Early voltage (V_{EA}) and (c) voltage gain (A_V) in DG MOSFET, RFET-A1, and RFET-B1 for various values of drain current (I_{ds}) at V_{ds} = 1V. V_{pg} = 1.5 V (for RFET).

The cut-off frequency (f_T) of transistor depends on transconductance (g_m) and gate capacitance (C_{gg}) i.e. f_T directly proportional to g_m/C_{gg}. At low I_{ds} (< 1 μA), RFET-A shows slightly lower g_m (Fig. 3.11(b)) as compared to DG MOSFET because of the lower effective channel length ($L_{CG} < L_{eff} < L_{CG} + 2L_{UG}$) with respect to DG MOSFET ($L_{eff} \approx L_G$) as shown in Fig. 3.5(a)-(c). However, at higher I_{ds} (> 1 μA), g_m of RFET-A decreases because of poor current driving capability resulting from higher series resistance due to the ungated region. However, a significantly lower value of C_{gg} in RFET-A (A1) (Fig. 3.11(a)) compensates for its poor g_m, and hence, a higher f_T is observed vis-à-vis DG MOSFET (Fig. 3.11(c)). However, for RFET-B, a very low g_m (Fig. 3.11(b)) and relatively higher C_{gg} (Fig. 3.11(a)) results in a much lower f_T (Fig. 3.11(c)). Fig. 3.12(a) shows lower g_m/I_{ds} values for both RFET topologies over the entire I_{ds} range due to lower effective channel length (greater influence of drain) and poor

g_m. At lower current drive (subthreshold regime), the impact of drain bias on channel conduction depends on the degree of DIBL in the device. Hence, RFET-A always shows lower Early voltage (V_{EA}) than DG MOSFET because of its lower effective channel length (or higher degree of DIBL) as shown in Fig. 3.12(b). An increase in V_{cg} causes a reduction in L_{eff} (an extension of the depletion region beyond the CG edges decreases [148]) and V_{EA} degrades till I_{ds} ~1 μA/μm. For I_{ds} > 1 μA, L_{eff} does not change significantly and attains a minimum value (~ L_{CG}) [149]. In the weak inversion, the resistance offered by CG becomes comparable to the sum of the resistance governed by polarity gate (PG), ungated region (UG), and S/D regions. This reduces the effective drain to source bias ($V_{ds,eff}$) across L_{CG} [149], thereby reducing g_{ds} (= $\partial I_{ds}/\partial V_{ds}$). Hence, a rise in V_{EA} of RFET-A is observed. Due to the lower g_m/I_{ds} and V_{EA} values, RFET-A attains a smaller gain ($A_V = g_m/I_{ds} \times V_{EA}$) as shown in Fig. 3.12(c). However, in RFET-B, a wider ungated region (60 nm in B1 as compared to 20 nm in A1) between CG and drain reduces the impact of drain bias on the channel. Hence, a higher value of V_{EA} is observed in RFET-B at low I_{ds} (< 0.1 μA/μm) as shown in Fig. 3.12(b). However, as V_{cg} increases (or I_{ds} increases), the electron concentration in the ungated region also increases as shown in Fig. 3.6(b) (tunneling of electrons from M to S at source), which causes a higher impact of drain bias on the channel i.e. V_{EA} degrades sharply. Hence, RFET-B shows a higher intrinsic gain (A_V) than DG MOSFET and RFET-A (Fig. 3.12(c)) at low I_{ds}. However, at I_{ds} ~ 10 μA/μm, the gain of RFET-B significantly degrades and becomes lower than that of DG MOSFET and RFET-A because of a sharp reduction of V_{EA}.

3.5 Conclusions

The analog/RF performance of RFET (at low I_{ds}) were assessed focusing on ULP applications. The underlap architecture of RFET results in a significantly lower value of $C_{parasitic}$ which tremendously benefits RFET-A in achieving a higher f_T. However, a lower value of A_V remains a bottleneck for RFET topologies at I_{ds} > 1 μA/μm. This requires careful optimization of the architecture. The same is discussed in the next chapter of the thesis.

Chapter 4

Architecture Optimization to Enhance Analog/RF Metrics in RFET

4.1 Motivation

In applications where enhancement of gain and the bandwidth of amplifiers is required, the gain-bandwidth product (GBP) becomes a key parameter. GBP represents the product of the open-loop voltage gain (A_V) and the bandwidth or cut-off frequency (f_T) of the amplifier [150]. In a transistor amplifier, A_V decreases as the frequency increases due to the internal capacitances and other parasitic effects [150]. GBP indicates the maximum frequency at which the amplifier can provide a specified voltage gain. It influences the trade-off between gain and bandwidth, determines the frequency response, affects stability, and helps in selecting transistors for specific applications.

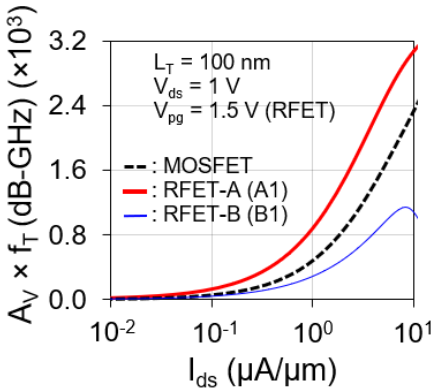

Fig. 4.1 Variation of gain-bandwidth product ($A_V \times f_T$) with drain current (I_{ds}) for MOSFET, RFET-A (A1) and RFET-B (B1) at V_{ds} = 1 V. V_{pg} = 1.5 V for RFET.

Fig. 4.1 compares the GBP of MOSFET, RFET-A (A1), and RFET-B (B1). RFET-A (A1) achieves the highest GBP despite having a lower A_V (Fig. 3.12(c)) than MOSFET, due to its superior f_T (Fig. 3.11(c)). While RFET-B (B1) attains the lowest GBP due to its poor A_V and f_T. Even though the GBP of RFET-

A (A1) is high, its A_V remains a major bottleneck. In order to fully utilize the potential of RFETs, their performance needs to be improved in terms of both - A_V and f_T.

RFETs offer the flexibility to vary the L_{CG}, L_{UG} and L_{PG} for a fixed L_T. This means that the device architecture can be optimized to remove the voltage gain bottleneck and enhance cut-off frequency simultaneously. To achieve this goal, RFET device architectures A1 to A5 (Fig. 3.2(a)) and B1 to B5 (Fig. 3.2(b)) will be considered, and their performance will be compared with DG MOSFET (Fig. 3.1(a)) with length (L_T = 100 nm) at I_{ds} = 1 µA/µm. By analyzing the FoMs of different device dimensions, optimal device architecture for achieving both high A_V and f_T i.e. high GBP in RFETs can be identified.

4.2 Optimization of L_{CG}/L_T to enhance gain of RFET

An increase in L_{CG} of RFET increases its gate controllability, thereby increasing its transconductance (g_m). Hence, it can be observed in Fig. 4.2(a) that g_m/I_{ds} of RFET increases with L_{CG} (or L_{CG}/L_T). A higher value of g_m/I_{ds} is observed in A4 compared to A2 for the same L_{CG}/L_T (= 0.1) because of larger L_{UG} (lesser SCEs). g_m/I_{ds} of RFET-A increases by ~36.8% by increasing L_{CG}/L_T from 0.1 (A2) to 0.6 (A5). Still, g_m/I_{ds} of A5 (= 31.4 V^{-1}) with L_{CG} = 60 nm (highest L_{CG} amongst all RFET-A devices) is lower than MOSFET (= 37.6 V^{-1}) at I_{ds} = 1 µA/µm primarily due to lower L_{CG} (compared to L_G = 100 nm of MOSFET). However, in RFET-B, only the 1st slope improves with L_{CG}/L_T as it is governed by thermionic emission while the 2nd slope remains independent of L_{CG}/L_T as it depends on tunneling [110]. Therefore, by increasing L_{CG}/L_T, g_m/I_{ds} does not change significantly as shown in Fig. 4.2(a).

Similarly, V_{EA} also increases with L_{CG}/L_T because of the reduced DIBL effect (Fig. 4.2(b)). RFET devices A2, A4, B2, and B4 show lower values of V_{EA} due to smaller L_{CG}/L_T (= 0.1). As L_{CG}/L_T ratio increases from 0.2 (A1, B1) to 0.6 (A5, B5), the improvement in V_{EA} for RFET-B devices is significantly higher than for RFET-A devices. This is because of greater immunity of RFET-B to DIBL

effect (Fig. 3.12(b)). Hence, the impact of increasing L_{CG} (L_{CG}/L_T) in RFET-B is much more prominent than in RFET-A. This enhancement achieved in V_{EA} is a big advantage for RFET (especially RFET-B) to overcome its gain constraint. Therefore, by enhancing g_m/I_{ds} and V_{EA} through L_{CG}/L_T of RFET-A, the bottleneck associated with poor A_V (= $g_m/I_{ds} \times V_{EA}$) of RFET-A and RFET-B can be overcome.

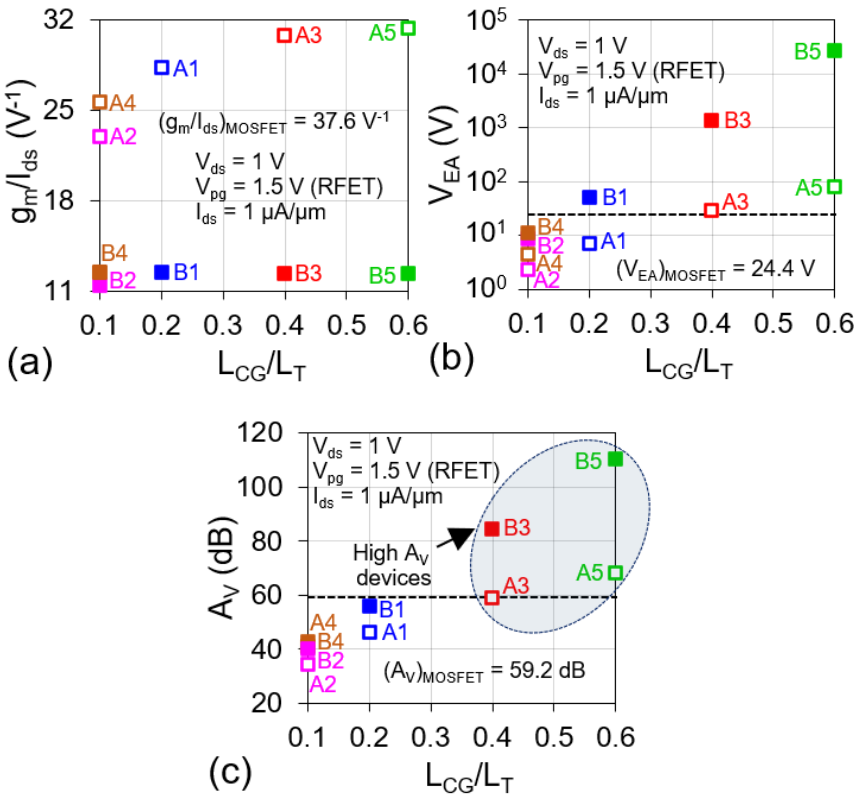

Fig. 4.2 Variation of (a) transconductance to current ratio (g_m/I_{ds}), (b) Early voltage (V_{EA}) and (c) voltage gain (A_V) for RFET devices with the ratio of control gate length to the total channel length (L_{CG}/L_T) at V_{ds} = 1 V and I_{ds} = 1 µA/µm. V_{pg} = 1.5 V for RFET.

Fig. 4.2(c) shows that A_V is directly proportional to the L_{CG}/L_T (Fig. 4.2(c)). Devices A1, A2, B2, A4, and B4 show low values of A_V because of low g_m/I_{ds} and low V_{EA}. Even though B1 shows a higher V_{EA} than MOSFET (= 24.4 V), its A_V is ~5.3% lower due to its poor g_m/I_{ds}. While A3 shows comparable A_V, A5 shows ~14.9% higher A_V than MOSFET (= 59.2 dB) despite lower g_m/I_{ds} due

to their high values of V_{EA}. Owing to the massive values of V_{EA} achieved by B3 and B5, they show ~1.43 times and ~1.9 times higher A_V than MOSFET, respectively. Therefore, in the context of low-power operation (I_{ds} = 1 µA/µm), A3, B3, A5, and B5 can be used as high-gain (A_V) devices.

4.3 Optimization of L_{UG}/L_T to enhance intrinsic speed of RFET

The primary reason for the higher cut-off frequency (f_T) of RFET (specifically RFET-A) compared to MOSFET is its lower C_{gg} (Fig. 3.11(a)). The gate capacitance (C_{gg}) of RFET is lower than that of MOSFET primarily due to the lower parasitic capacitance ($C_{parasitic}$) (Fig. 3.4(b), 3.9, 3.10) of RFET. Hence, to improve the speed (f_T) of the device, it is important to understand the behavior of the parasitic capacitive components which govern the value of C_{gg}.

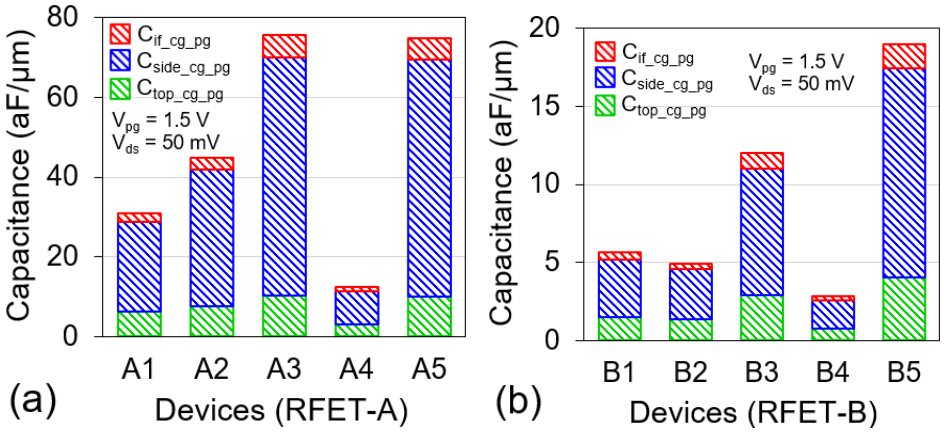

Fig. 4.3 Comparison of top ($C_{top\_cg\_pg}$), sidewall ($C_{side\_cg\_pg}$), and inner fringing ($C_{if\_cg\_pg}$) parasitic capacitive components in (a) RFET-A and (b) RFET-B at V_{ds} = 50 mV and V_{pg} = 1.5 V.

It was observed that the series combination effect and low values of the C_{cg_pg} components were majorly responsible for lower $C_{parasitic}$ in RFET (Fig. 3.9, 3.10). Hence, the components associated with C_{cg_pg} need to be examined. Fig. 4.3(a)-(b) shows the capacitance distribution of the top ($C_{top\_cg\_pg}$), sidewall ($C_{side\_cg\_pg}$), and inner fringing ($C_{if\_cg\_pg}$) parasitic components between CG and

PG of RFET-A and RFET-B devices, respectively. The distribution of the components is strongly governed by the length of the ungated region (L_{UG}) in the RFET devices. Devices with high L_{UG} (A4, B4) attain low values of the parasitic components i.e. low C_{cg_pg}, while devices that have low L_{UG} (A3, A5, B5) show higher values of the parasitic components. Therefore, to enhance the f_T, L_{UG}/L_T can be maximized for fixed L_T.

Since C_{gg} of RFET is significantly impacted by its parasitic part, it can be concluded that C_{gg} of RFET is most vulnerable to the changes made in L_{UG} in comparison to L_{CG} and L_{PG}. This strong dominance of L_{UG} is reflected in Fig. 4.4 where C_{gg} and L_{UG} show a reciprocal behavior with each other. The dependence of C_{gg} on L_{UG}/L_T is more prominent in RFET-A as compared to RFET-B since the series combination effect on $C_{parasitic}$ is due to both the source as well as drain part in RFET-A.

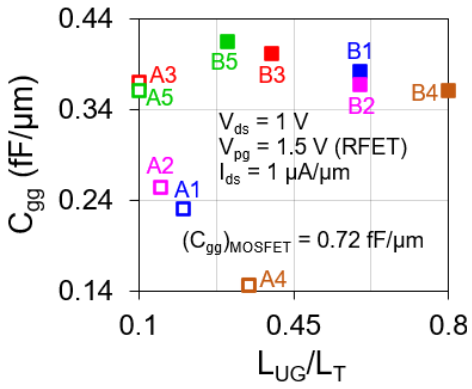

Fig. 4.4 Variation of gate capacitance (C_{gg}) for RFET devices with the ratio of ungated region length to the total channel length (L_{UG}/L_T) at V_{ds} = 1 V and I_{ds} = 1 μA/μm. V_{pg} is 1.5 V for RFET.

An important parameter for logic devices is the circuit delay (τ) given by the formula, $\tau = C_{gg} \times V_{dd}/I_{ds}$, where V_{dd} is the maximum applied voltage on the device [38]. Therefore, V_{dd} = 1 V for MOSFET and V_{dd} = 1.5 V for RFET. Since, τ directionally proportional to C_{gg} and C_{gg} directionally proportional to $1/L_{UG}$ (Fig. 4.4), which results in τ also increases with $1/L_{UG}$. Thus, τ also shows the same trends with L_{UG}/L_T similar to C_{gg} (Fig. 4.5(a)). Due to the lower C_{gg} for all

RFET architectures than that of MOSFET, the corresponding τ is also lower than that of MOSFET (= 0.72 ns) showcasing the suitability of RFET for ULP logic devices.

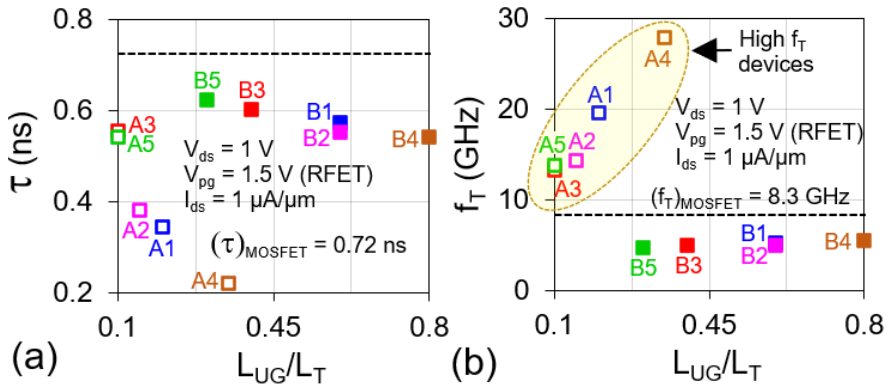

Fig. 4.5 Variation of (a) circuit delay (τ) and (b) cut-off frequency (f_T) for RFET devices with the ratio of ungated region length to the total channel length (L_{UG}/L_T) at V_{ds} = 1 V and I_{ds} = 1 µA/µm. V_{pg} is 1.5 V for RFET.

Since, f_T is directionally proportional to g_m/C_{gg}, which results in f_T also directionally proportional to L_{UG} as shown in Fig. 4.5(b). By increasing the L_{UG}/L_T of RFET-A devices from 0.1 (A3) to 0.35 (A4), f_T is enhanced remarkably (~1.95 times). An unappreciable change is seen in the f_T of RFET-B devices when increasing L_{UG}/L_T because of the insignificant change in its C_{gg} (Fig. 4.4) when varying L_{UG}/L_T. Also, because of poor g_m (Fig. 6(b)), f_T is bogged down, resulting in lower values for all the RFET-B devices in comparison to MOSFET. Therefore, by increasing the ungated region (L_{UG}) of RFET (especially RFET-A), its speed (f_T) can be enhanced. All RFET-A devices (A1 to A5) attain f_T higher than that of MOSFET (= 8.3 GHz) at I_{ds} = 1 µA/µm, out of which, A4 with the highest f_T can be used as a high-speed device at low current levels.

4.4 Performance comparison of RFET devices with MOSFET

Fig. 4.6(a) shows A_V versus f_T of all RFET (A and B) devices and MOSFET at I_{ds} = 1 µA/µm. Only devices A3 and A5 achieve both a higher A_V

and a higher f_T as compared to MOSFET. Fig. 4.6(b) compares the gain-bandwidth product (GBP) i.e. $A_V \times f_T$ of RFET devices and MOSFET. All RFET-A devices show a higher GBP than MOSFET due to their enhanced f_T (Fig. 4.5(b)). Because of degraded f_T in RFET-B (Fig. 4.5(b)), except B5, all RFET-B devices show a lower GBP than MOSFET. B5 achieves a higher GBP due to its superior A_V (Fig. 4.2(c)). Results indicate that an optimized RFET device has the potential to outperform MOSFET at lower current levels.

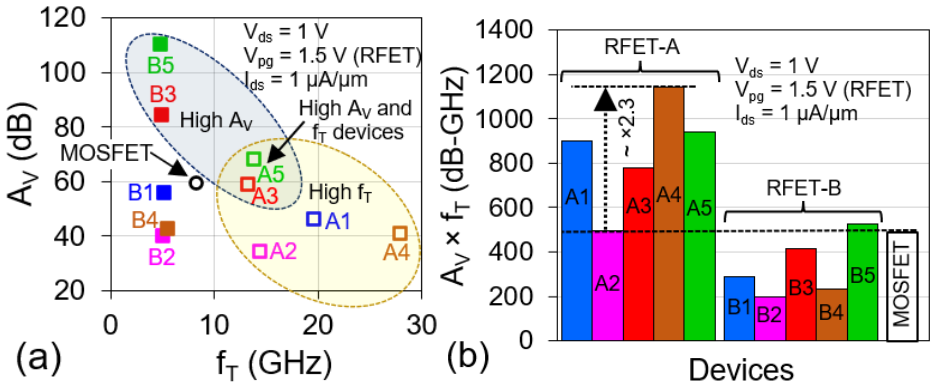

Fig. 4.6 (a) Variation of A_V with f_T and (b) Comparison of ($A_V \times f_T$) for DG MOSFET and RFET devices at V_{ds} = 1 V and I_{ds} = 1 µA/µm. V_{pg} = 1.5 V for RFET.

4.5 Conclusions

To overcome the lower voltage gain (A_V) of RFET and to enhance analog/RF metrics at low I_{ds} (= 1 µA/µm), architecture optimization techniques were discussed for RFET (A and B) topologies. By increasing the value of L_{CG}/L_T, RFET was able to overcome the A_V of MOSFET because of enhanced gate controllability. Also, by increasing the value of L_{UG}/L_T, a significant improvement in the circuit delay (τ) and cut-off frequency (f_T) is observed especially for RFET-A devices. Results indicate that for high-speed (f_T) applications, RFET-A will be more suitable, whereas, for high gain (A_V) applications, RFET-B will be more favorable. Comparing the performance of RFET and MOSFET based on analog/RF metrics, RFET-A outperforms

MOSFET in all the aspects i.e. A_V, τ, f_T, and $A_V \times f_T$ (GBP) making it a strong contender for low-power analog/RF applications.

Chapter 5

Conclusion and Scope for Future Work

5.1 Conclusion

The Reconfigurable Field Effect Transistor (RFET) [84]-[99] derives its concept from the SB MOSFET structure, incorporating two M-S junctions at the source and drain. The SB MOSFET uses a single gate to regulate the current in the device, but it is hindered by the ambipolar behavior of the current. To overcome this issue, additional gate(s) are included in the device architecture. Similar to a conventional MOSFET, RFET has a gate, called control gate (CG), which controls the flow of carriers in the channel. Additional gate(s), called polarity gate (PG), is used to configure the channel polarity. These two gates are separated and individually controlled to achieve reconfigurability. Since source and drain are made up of metal (NiSi) and the channel is intrinsic (undoped *p*-type), the issues related to fabrication process complexity are eliminated and the cost due to low thermal budget reduces. Furthermore, because of its reconfigurable nature, there is no need to fabricate a *p*-type device. At the logic implementation level, this leads to a reduced number of transistors compared to standard CMOS logic for implementing the desired functionality [101].

The research work focuses on assessing the analog/RF performance of a three-gate and a twin-gate RFET by benchmarking their figures of merits (FoMs) with a conventional double-gate (DG) MOSFET for the same total gate length (L_T = 100 nm) at low current levels (10^{-2} μA/μm to 10 μA/μm). First, the subthreshold swing (S_{swing}) and off-current (I_{OFF}) of both RFET topologies were compared. It was observed that while RFET-A (three-gated RFET) devices show S_{swing} comparable to a conventional MOSFET due to similar conduction mechanism (thermionic emission), RFET-A devices attain a much higher I_{OFF} due to tunneling of charged carriers resulting from a high V_{pg}. In contrast, RFET-B (twin-gate RFET) devices suffers with degraded S_{swing} since its S_{swing} depends on

tunneling as well as thermionic emission of charged carriers. However, all RFET-B devices (except B5) show lower I_{OFF} because of the high SB tunneling width experienced by the charged carriers at zero bias.

Also, a detailed explanation for the parasitic gate capacitance ($C_{parasitic}$) of DG MOSFET, RFET-A and RFET-B was provided through an equivalent capacitance model. The parasitic capacitive components between CG and PG i.e. ungated region (UG) of RFET and the series combination effect were majorly responsible for a lower $C_{parasitic}$ in RFET which also resulted in a lower C_{gg}. Because of a significantly smaller C_{gg} of RFET as compared to that of MOSFET, RFET (only RFET-A) was able to achieve a much higher f_T. Due to poor g_m of RFET-B, its f_T was degraded despite a lower C_{gg}.

The voltage gain (A_V) of RFET-A was degraded by poor g_m/I_{ds} and V_{EA} values arising from (i) poor current drive and (ii) high degree of drain induced barrier lowering (DIBL) effect. RFET-B shows high tolerance to DIBL effect at low I_{ds} (< 1 μA/μm) and hence a very high value of V_{EA}. However, because of a sharp decrease in V_{EA} at high I_{ds} (> 1 μA/μm) coupled with poor g_m/I_{ds}, its A_V is also degraded. To remove the A_V bottleneck and enhance other analog/RF metrics as well associated with RFET, architecture optimization techniques were discussed.

RFET-A architecture with $L_{CG}/L_T < 0.2$ and $0.1 \leq L_{UG}/L_T \leq 0.35$ can achieve highest cut-off frequency but with low intrinsic voltage gain. RFET-B designed with $L_{CG}/L_T \geq 0.4$ is favorably positioned towards high-intrinsic gain but with a degraded bandwidth. In terms of optimum gain-bandwidth trade-off, a three-gate RFET with $L_{CG}/L_T \geq 0.4$ and $L_{UG}/L_T = 0.1$ can provide enhancement of both gain and bandwidth vis-à-vis DG MOSFET. Results provide new insights into architecture optimization of RFETs topologies for enhancing analog/RF metrics at lower drive currents. Ultimately, this study contributes to the ongoing effort to develop RFETs as a viable alternative to MOSFETs in high-speed, low-power applications.

5.2 Scope for Future Work

This work provides a comprehensive examination of several crucial analog/RF performance measures, such as A_V and f_T, specifically at low I_{ds}. Nonetheless, additional analysis can be conducted to explore other significant performance metrics, including maximum-oscillation frequency (f_{MAX}), $g_m/I_{ds}\times f_T$ (speed and power efficiency trade-off parameter), g_m^2/I_{ds} [151], and linearity metrics like VIP_3 [152]. Furthermore, investigating the sensitivity of performance metrics (e.g.: A_V, f_T, $g_m/I_{ds}\times f_T$, g_m^2/I_{ds}) to device and technological parameters in RFET also presents an intriguing subject of interest. Low Noise Amplifiers (LNAs), Power Amplifiers (PAs), Voltage Controlled Oscillators (VCOs), and others, used in RF Front End Modules (FEMs) [153] commonly incorporate both *n*-type and *p*-type transistors in their circuit components. Consequently, it is essential to leverage the reconfigurability feature of RFETs, enabling both *n*-type and *p*-type operations within the same device, to thoroughly evaluate the performance of circuits like LNAs, PAs, VCOs, and so on. Furthermore, it is crucial to compare their performance against their counterparts using CMOS technology.

A comparison of contacted gate pitch (CGP) of conventional MOSFET and RFET topology is also essential for layout comparison. In MOSFET technology, CGP describes the spacing of the gates between two adjacent transistors when the S/D regions are contacted [154]. CGP or gate pitch can be measured as the distance between the centre to centre of the gates or the distance between corresponding edges of the gates. While Baldauf et. al. [110] has considered the spacing between the program gate (PG) and control gate (CG) in RFET as gate pitch, few other works [155, 156] on RFET technology have considered the distance between the same gates as gate pitch. Thus, further investigation is required for detailed analysis of gate pitch estimation.

REFERENCES

[1] Iwai, H., (2022) History of transistor invention: 75th anniversary, Proceedings of IEEE 16th International Conference on Solid-State & Integrated Circuit Technology (ICSICT), pp. 1-10.

[2] Moore G. E., (1965) Cramming more components onto integrated circuits, Electronics, 38, 114-117.

[3] Lee, T.H., (2003) The design of CMOS radio-frequency integrated circuits, Cambridge university press (ISBN 9780521613897).

[4] Kousai, S., (2014) Recent progress in CMOS RF circuit design, IEICE Electronics Express, 11, 20132011-20132011.

[5] Kinget, P.R., (2015) Scaling analog circuits into deep nanoscale CMOS: Obstacles and ways to overcome them, Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp. 1-8.

[6] Decoutere, S., Wambacq, P., Subramanian, V., Borremans, J. and Mercha, A., (2006) Technologies for (sub-) 45nm Analog/RF CMOS-Circuit Design Opportunities and Challenges, Proceedings of IEEE Custom Integrated Circuits Conference, pp. 679-686.

[7] Mak, P.I. and Martins, R.P., (2010) High-/mixed-voltage RF and analog CMOS circuits come of age, IEEE Circuits and Systems Magazine, 10, 27-39.

[8] Annema, A.J., (1999) Analog circuit performance and process scaling, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 46, 711-725.

[9] International Roadmap for Devices and Systems (IRDS), 2022 (Available: https://irds.ieee.org).

[10] Cherry, S., (2004) Edholm's law of bandwidth, IEEE spectrum, 41, 58-60.

[11] Vandooren, A., Parvais, B., Witters, L., Walke, A., Vais, A., Merckling, C., Lin, D., Waldron, N., Wambacq, P., Mocuta, D. and Collaert, N., (2017) 3D technologies for analog/RF applications, Proceedings of IEEE SOI-3D-

Subthreshold Microelectronics Technology Unified Conference (S3S), pp. 1-3.

[12] Annema, A.J., Nauta, B., Van Langevelde, R. and Tuinhout, H., (2005) Analog circuits in ultra-deep-submicron CMOS, IEEE journal of solid-state circuits, 40, 132-143.

[13] Passi, V. and Raskin, J.P., (2017) Review on analog/radio frequency performance of advanced silicon MOSFETs, Semiconductor Science and Technology, 32, 123004.

[14] Collaert, N., Alian, A., Chen, S.H., Deshpande, V., Ingels, M., Putcha, V., Sibaja-Hernandez, A., van Liempd, B., Vais, A., Vandooren, A. and Walke, A., (2018) Semiconductor technologies for next generation mobile communications, Proceedings of 14th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), pp. 1-4.

[15] Parvais, B., Peralagu, U., Vais, A., Alian, A., Witters, L., Mols, Y., Walke, A., Ingels, M., Yu, H., Putcha, V. and Khaled, A., (2020) Advanced transistors for high frequency applications, ECS Transactions, 97, 27.

[16] Collaert, N., Alian, A., Banerjee, A., Chauhan, V., ElKashlan, R.Y., Hsu, B., Ingels, M., Khaled, A., Kodandarama, K.V., Kunert, B. and Mols, Y., (2020) From 5G to 6G: will compound semiconductors make the difference? Proceedings of IEEE 15th International Conference on Solid-State & Integrated Circuit Technology (ICSICT), pp. 1-4.

[17] Parvais, B., Alian, A., Peralagu, U., Rodriguez, R., Yadav, S., Khaled, A., Elkashlan, R.Y., Putcha, V., Sibaja-Hernandez, A., Zhao, M. and Wambacq, P., (2020) GaN-on-Si mm-wave RF devices integrated in a 200mm CMOS Compatible 3-Level Cu BEOL, Proceedings of IEEE International Electron Devices Meeting (IEDM), pp. 8-1.

[18] Yu, Q., Then, H.W., Thomson, D., Chou, J., Garrett, J., Huang, I., Momson, I., Ravikumar, S., Hwangbo, S., Latorre-Rey, A. and Roy, A., (2022) 5G mmWave Power Amplifier and Low-Noise Amplifier in 300mm GaN-on-Si Technology, Proceedings of IEEE Symposium on VLSI Technology and Circuits, pp. 126-127.

[19] Jeong, J., Kim, S.K., Kim, J., Geum, D.M., Kim, D., Jo, E., Jeong, H., Park, J., Jang, J.H., Choi, S. and Kwon, I., (2022) Heterogeneous and monolithic 3D integration of III–V-based radio frequency devices on Si CMOS circuits, ACS nano, 16, 9031-9040.

[20] Collaert, N., Alian, A., Banerjee, A., Boccardi, G., Cardinael, P., Chauhan, V., Desset, C., ElKashlan, R., Khaled, A., Ingels, M. and Kunert, B., (2022) III-V/III-N technologies for next generation high-capacity wireless communication, Proceedings of IEEE International Electron Devices Meeting (IEDM), pp. 11-5.

[21] Strinati, E.C., Peeters, M., Neve, C.R., Gomony, M.D., Cathelin, A., Boldi, M.R., Ingels, M., Banerjee, A., Chevalier, P., Kozicki, B. and Belot, D., (2022) The Hardware Foundation of 6G: The NEW-6G Approach, Proceedings of IEEE Joint European Conference on Networks and Communications & 6G Summit (EuCNC/6G Summit), pp. 423-428.

[22] Parvais, B., Subramanian, V., Mercha, A., Dehan, M., Wambacq, P., Sanssen, W., Groeseneken, G. and Decoutere, S., (2007) FinFET technology for analog and RF circuits, Proceedings of 14th IEEE International Conference on Electronics, Circuits and Systems, pp. 182-185.

[23] Wambacq, P., Verbruggen, B., Scheir, K., Borremans, J., Dehan, M., Linten, D., De Heyn, V., Van der Plas, G., Mercha, A., Parvais, B. and Gustin, C., (2007) The potential of FinFETs for analog and RF circuit applications, IEEE Transactions on Circuits and Systems I: Regular Papers, 54, 2541-2551.

[24] Singh, J., Ciavatti, J., Sundaram, K., Wong, J.S., Bandyopadhyay, A., Zhang, X., Li, S., Bellaouar, A., Watts, J., Lee, J.G. and Samavedam, S.B., (2017) 14-nm FinFET technology for analog and RF applications, IEEE Transactions on electron devices, 65, 31-37.

[25] Callender, S., Shin, W., Lee, H.J., Pellerano, S. and Hull, C., (2018) FinFET for mm wave-technology and circuit design challenges, Proceedings of IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), pp. 168-173.

[26] Parvais, B., Hellings, G., Simicic, M., Weckx, P., Mitard, J., Jang, D., Deshpande, V., Van Liempc, B., Veloso, A., Vandooren, A. and Waldron, N., (2018) Scaling CMOS beyond Si FinFET: an analog/RF perspective, Proceedings of IEEE 48th European Solid-State Device Research Conference (ESSDERC), pp. 158-161.

[27] Bhoir, M.S., Chiarella, T., Ragnarsson, L.Å., Mitard, J., Terzeiva, V., Horiguchi, N. and Mohapatra, N.R., (2019) Analog performance and its variability in sub-10 nm fin-width FinFETs: A detailed analysis, IEEE Journal of the Electron Devices Society, 7, 1217-1224.

[28] Hiramoto, T., (2019) Five nanometre CMOS technology, Nature Electronics, 2, 557-558.

[29] Suh, Y., Bao, J., Lin, V., Kuo, W., Kim, L., Chen, Y., Wang, H., Gao, Y., Cheng, J., Wang, X.Y. and Park, H., (2022) High Performance 5G mobile SoC Design-Technology Co-Optimization for PPA and Manufacturability with 5nm EUV FinFET technology, Proceedings of IEEE International Electron Devices Meeting (IEDM), pp. 27-4.

[30] Razavi, B., (1999) CMOS technology characterization for analog and RF design, IEEE journal of solid-state circuits, 34, 268-276.

[31] Heydari, B., Bohsali, M., Adabi, E. and Niknejad, A.M., (2007) Millimeter-wave devices and circuit blocks up to 104 GHz in 90 nm CMOS, IEEE Journal of Solid-State Circuits, 42, 2893-2903.

[32] Liou, J.J. and Schwierz, F., (2003) RF MOSFET: recent advances, current status and future trends, Solid-State Electronics, 47, 1881-1895.

[33] Lee, T.H., (2007) From oxymoron to mainstream: the evolution and future of RF CMOS, Proceedings of IEEE International Workshop on Radio-Frequency Integration Technology, pp. 1-6.

[34] Bennett, H.S., Brederlow, R., Costa, J.C., Cottrell, P.E., Huang, W.M., Immorlica, A.A., Mueller, J.E., Racanelli, M., Shichijo, H., Weitzel, C.E. and Zhao, B., (2005) Device and technology evolution for Si-based RF integrated circuits, IEEE Transactions on Electron Devices, 52, 1235-1258.

[35] Schmid, R.L., Ulusoy, A.Ç., Zeinolabedinzadeh, S. and Cressler, J.D., (2015) A comparison of the degradation in RF performance due to device interconnects in advanced SiGe HBT and CMOS technologies, IEEE Transactions on Electron Devices, 62, 1803-1810.

[36] Jan, C.H., Agostinelli, M., Deshpande, H., El-Tanani, M.A., Hafez, W., Jalan, U., Janbay, L., Kang, M., Lakdawala, H., Lin, J. and Lu, Y.L., (2010) RF CMOS technology scaling in high-k/metal gate era for RF SoC (system-on-chip) applications, Proceedings of IEEE International Electron Devices Meeting, pp. 27-2.

[37] Iwai, H., (2015) Future of nano CMOS technology, Solid-State Electronics, 112, 56-67.

[38] Taur Y., and Ning T. H., (2009) MOSFET devices. In: Fundamentals of modern VLSI devices, 2nd edn., Cambridge University Press (ISBN 978-0-521-83294-6).

[39] Suryagandh, S.S., Garg, M., Gupta, M. and Woo, J.C., (2004) Analog performance of scaled bulk and SOI MOSFETs, Proceedings of IEEE 7th International Conference on Solid-State and Integrated Circuits Technology, pp. 153-158.

[40] Dambrine, G., Raynaud, C., Lederer, D., Dehan, M., Rozeaux, O., Vanmackelberg, M., Danneville, F., Lepilliet, S. and Raskin, J.P., (2003) What are the limiting parameters of deep-submicron MOSFETs for high frequency applications?, IEEE Electron Device Letters, 24, 189-191.

[41] Lewyn, L.L., Ytterdal, T., Wulff, C. and Martin, K., (2009) Analog circuit design in nanoscale CMOS technologies, Proceedings of the IEEE, 97, 1687-1714.

[42] Murmann, B., Nikaeen, P., Connelly, D.J. and Dutton, R.W., (2006) Impact of scaling on analog performance and associated modeling needs, IEEE Transactions on Electron Devices, 53, 2160-2167.

[43] Roy, K., Mukhopadhyay, S. and Mahmoodi-Meimand, H., (2003) Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits, Proceedings of the IEEE, 91, 305-327.

[44] Pierret, R.F., (1996) Semiconductor device fundamentals, 2nd edn., Pearson Education India (ISBN 9780201543933).

[45] Dennard R. H., Gaensslen F. H., Rideout V. L., Bassous E., and LeBlanc A. R. (1974), Design of Ion-Implanted Small MOSFET‘s Dimensions with Very Small Physical Dimensions, IEEE Journal of Solid-State Circuits, 9, 256–268.

[46] Godoy, A., López-Villanueva, J.A., Jiménez-Tejada, J.A., Palma, A. and Gámiz, F., (2001) A simple subthreshold swing model for short channel MOSFETs, Solid-State Electronics, 45, 391-397.

[47] Schuegraf, K.F. and Hu, C., (1993) Hole injection oxide breakdown model for very low voltage lifetime extrapolation, IEEE 31st Annual Proceedings Reliability Physics 1993, pp. 7-12.

[48] Streetman B. G. and Banerjee S. K., (2009) Solid State Electronic Devices, 6th edn., Pearson Education Inc., New Jersey 07458 (ISBN978-81 -203-3020-7).

[49] Colinge J.-P., (1997) Silicon-on-Insulator Technology: Materials to VLSI, 3rd edn., Springer Science Business Media, New York (ISBN 978-1-4613-4795-8).

[50] Ochoa A., and Dawes W., (1979) Latch-up control in CMOS integrated circuits, IEEE Transaction on Nuclear Science, 26, 5065-5068.

[51] Colinge J.-P., (1989) Thin-film SOI technology: the solution to many submicron CMOS problems, Proceedings of IEEE Electron Devices Meeting (IEDM), pp. 817– 820.

[52] Bruel, M., Aspar, B., Charlet, B., Maleville, C., Poumeyrol, T., Soubie, A., Auberton-Herve, A.J., Lamure, J.M., Barge, T., Metral, F. and Trucchi, S., (1995) “Smart cut”: a promising new SOI material technology, Proceedings of IEEE International SOI Conference, pp. 178-179.

[53] Musseau, O., (1996) Single-event effects in SOI technologies and devices, IEEE Transactions on Nuclear Science, 43, 603-613.

[54] Cristoloveanu S., and Lee S., (1995) Electrical characterization of silicon on insulator materials and devices, The Kluwer International Series in Engineering and Computer Science (ISBN 978-0-7923-9548-5).

[55] Choi J. Y., and Fossum J. G., (1991) Analysis and control of floating body bipolar effects in fully depleted submicrometer SOI MOSFET's, IEEE Transaction on Electron Devices, 38, 1384–1391.

[56] Kato K., Wada T., and Taniguchi K., (1985) Analysis of kink characteristics in silicon-on-insulator MOSFETs using two-carrier modelling, IEEE Transaction on Electron Devices, 32, 458-462.

[57] Adan A. O., Higashi K., and Fukushima Y., (1999) Analytical threshold voltage model for ultrathin SOI MOSFET's including short channel and floating-body effects, IEEE Transaction on Electron Devices, 46, 729–737.

[58] Sakurai T., Matsuzawa A., and Douseki T., (2006) Fully depleted SOI CMOS circuits and technology for ultra-low-power applications, Springer, Japan (ISBN 978-0-387-29218-2).

[59] Yan R. H., Ourmazd A., and Lee K. F., (1992) Scaling the Si MOSFET: From bulk to SOI to bulk, IEEE Transaction on Electron Devices, 39, 1704–1710.

[60] Beranger C. F., Denorme S., Perreau P., Buj C., Faynot O., Andrieu F., Tosti L., Barnola S., Salvetat T., Garros X., Cassé M., Allain F., Loubet N., Pham-Nguyen L., Deloffre E., Gros-Jean M., Beneyton R., Laviron C., Marin M., Leyris C., Haendler S., Leverd F., Gouraud P., Scheiblin P., Clement L., Pantel R., Deleonibus S., Skotnicki T., (2009) FDSOI devices with thin BOX and ground plane integration for 32 nm node and below, Solid-State Electronics, 53, 730–734.

[61] Yeh P. C., and Fossum J. G., (1995) Physical subthreshold MOSFET modeling applied to viable design of deep submicrometer fully depleted SOI low-voltage CMOS technology, IEEE Transaction on Electron Devices, 42, 1605–1613.

[62] Sekigawa T. and Hayashi Y., (1984) Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate, Solid. State. Electron., 27, 827–828.

[63] Balestra F., Cristoloveanu S., Benachir M., Brini J and Elewa T, (1987) Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance, IEEE Electron Device Letters, 8, 410-412.

[64] Suzuki K., Tanaka T., Tosaka Y., Horie H., and Arimoto Y., (1993) Scaling theory for double-gate SOI MOSFETs, IEEE Transaction on Electron Devices, 40, 2326-2329.

[65] Wong H.-S. P., Chan K. K., and Taur Y. (1997) Self-aligned (top and bottom) dual-gate MOSFET with a 25 nm thick silicon channel, IEEE Electron Devices Meeting, 427-430.

[66] Hisamoto D., Kaga T., Kawamoto Y., and Takeda E., (1989) A fully depleted lean channel transistor (DELTA)-a novel vertical ultra-thin SOI MOSFET, Proceedings of IEEE Electron Devices Meeting (IEDM), pp. 833-836.

[67] Colinge J.-P., (2004) Multiple gate SOI MOSFETs, Solid-State Electronics, 48, 897-905.

[68] Maszara, W. P., and Lin, M. R., (2013) FinFETs— Technology and circuit design challenges, Proceedings of the IEEE European Solid-State Device Research Conference (ESSDERC), pp. 3-8.

[69] Jurczak, M., Skotnicki, T., Paoli, M., Tormen, B., Martins, J., Regolini, J.L., Dutartre, D., Ribot, P., Lenoble, D., Pantel, R. and Monfray, S., (2000) Silicon-on-Nothing (SON)-an innovative process for advanced CMOS, IEEE Transactions on Electron Devices, 47, 2179-2187.

[70] Barraud, S., Lapras, V., Previtali, B., Samson, M.P., Lacord, J., Martinie, S., Jaud, M.A., Athanasiou, S., Triozon, F., Rozeau, O. and Hartmann, J.M., (2017) Performance and design considerations for gate-all-around stacked-NanoWires FETs, Proceedings of IEEE International Electron Devices Meeting (IEDM), pp. 29-2.

[71] Lee, Y.M., Na, M.H., Chu, A., Young, A., Hook, T., Liebmann, L., Nowak, E.J., Baek, S.H., Sengupta, R., Trombley, H. and Miao, X., (2017) Accurate performance evaluation for the horizontal nanosheet standard-cell design space beyond 7nm technology, Proceedings of IEEE International Electron Devices Meeting (IEDM), pp. 29-3.

[72] Tanaka, H., Kido, M., Yahashi, K., Oomura, M., Katsumata, R., Kito, M., Fukuzumi, Y., Sato, M., Nagata, Y., Matsuoka, Y. and Iwata, Y., (2007) Bit cost scalable technology with punch and plug process for ultra high-density flash memory, Proceedings of IEEE Symposium on VLSI Technology, pp. 14-15.

[73] Kim J, Hong A. J, Kim S. M, Song E. B, Park J. H, Han J, Choi S, Jang D, Moon J.-T, Wang K. L., (2009) Novel vertical-stacked-array-transistor (VSAT) for ultra-high-density and cost-effective NAND flash memory devices and SSD (solid state drive), Proceedings of Symposium on VLSI Technology, Honolulu, HI, pp. 186-187.

[74] Thiele, S., Kinberger, W., Granzner, R., Fiori, G. and Schwierz, F., (2017) The prospects of two-dimensional materials for ultimately scaled CMOS, Proceedings of IEEE Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), pp. 113-116.

[75] Auth, C., Allen, C., Blattner, A., Bergstrom, D., Brazier, M., Bost, M., Buehler, M., Chikarmane, V., Ghani, T., Glassman, T. and Grover, R., (2012) A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors, Proceedings of IEEE Symposium on VLSI technology (VLSIT), pp. 131-132.

[76] Chang, J.B., Guillorn, M., Solomon, P.M., Lin, C.H., Engelmann, S.U., Pyzyna, A., Ott, J.A. and Haensch, W.E., (2011) Scaling of SOI FinFETs down to fin width of 4 nm for the 10nm technology node, Proceedings of IEEE Symposium on VLSI Technology-Digest of Technical Papers, pp. 12-13.

[77] Razavieh, A., Zeitzoff, P. and Nowak, E.J., (2019) Challenges and limitations of CMOS scaling for FinFET and beyond architectures, IEEE Transactions on Nanotechnology, 18, 999-1004.

[78] Gnudi, A., Reggiani, S., Gnani, E. and Baccarani, G., (2012) Analysis of threshold voltage variability due to random dopant fluctuations in junctionless FETs, IEEE Electron Device Letters, 33, 336-338.

[79] Xiong, W. (W.) (2008). Multigate MOSFET Technology. In: Colinge, JP. (eds) FinFETs and Other Multi-Gate Transistors. Springer, Boston, pp. 49-111 (ISBN 9780387717524).

[80] 2017. [Online]. Available: http://blog.appliedmaterials.com.

[81] Maassen, J., Jeong, C., Baraskar, A., Rodwell, M. and Lundstrom, M., (2013) Full band calculations of the intrinsic lower limit of contact resistivity, Applied Physics Letters, 102, p.111605.

[82] Niimi, H., Liu, Z., Gluschenkov, O., Mochizuki, S., Fronheiser, J., Li, J., Demarest, J., Zhang, C., Liu, B., Yang, J. and Raymond, M., (2016) Sub-10^{-9} Ω-cm^2 n-Type Contact Resistivity for FinFET Technology, IEEE Electron Device Letters, 37, 1371-1374.

[83] Shine, G., Weber, C.E. and Saraswat, K.C., (2016) Statistical limits of contact resistivity due to atomistic variation in nanoscale contacts, Proceedings of IEEE Symposium on VLSI Technology, pp. 1-2.

[84] Navarro C., Barraud S., Martinie S., Lacord J., Jaud M., and Vinet M. (2017), Reconfigurable field effect transistor for advanced CMOS: Advantages and limitations, Solid-State Electronics, 128, 155-162.

[85] Marchi M. D., Zhang J., Frache S., Sacchetto D., Gaillardon P.-E., Leblebici Y., and Micheli G. D. (2014), Top–down fabrication of gate all-around vertically stacked silicon nanowire FETs with controllable polarity, IEEE Transactions Nanotechnology, 13, 1029–1038.

[86] Marchi M. D., Zhang J., Frache S., Sacchetto D., Gaillardon P.-E., Leblebici Y., and Micheli G. D. (2014), Configurable logic gates using polarity-controlled silicon nanowire gate-all-around FETs, IEEE Electron Device Letters, 35, 880–882.

[87] Sun B., Richstein B., Liebisch P., Frahm T., Scholz S., Trommer J., Mikolajick T., Knoch J. (2021), On the Operation Modes of Dual-Gate Reconfigurable Nanowire Transistors, IEEE Transactions on Electron Devices, 68, 3684-3689.

[88] Cadareanu P. and Gaillardon P. -E. (2021), A TCAD Simulation Study of Three-Independent-Gate Field-Effect Transistors at the 10-nm Node, IEEE Transactions on Electron Devices, 68, 4129-4135.

[89] Zhang J., Gaillardon P., and Micheli G. D., (2013) Dual-threshold voltage configurable circuits with three-independent-gate silicon nanowire FETs, Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2111-2114.

[90] Trommer J., André H., Tim B., Stefan S., Thomas M., and Weber W. M. (2015), Functionality-enhanced logic gate design enabled by symmetrical reconfigurable silicon nanowire transistors, IEEE Transactions on Nanotechnology, 14, 689-698.

[91] Zhang J., Marchi M D., Sacchetto D., Gaillardon P., Leblebici Y., and De Micheli G. (2014), Polarity-Controllable Silicon Nanowire Transistors with Dual Threshold Voltages, IEEE Transactions on Electron Devices, 61, 3654-3660.

[92] Böckle R., Sistani M., Lipovec B., Pohl D., Rellinghaus B., Lugstein A., Weber W. M. (2022), A Top-Down Platform Enabling Ge Based Reconfigurable Transistors, Advanced Materials Technologies, 7, 2100647, 2022.

[93] Simon M., Liang B., Fischer D., Knaut M., Tahn A., Mikolajick T., and Weber W. M. (2020), Top-Down Fabricated Reconfigurable FET With Two Symmetric and High-Current On-States, IEEE Electron Device Letters, 41, 1110-1113.

[94] Simon, M., Heinzig, A., Trommer, J., Baldauf, T., Mikolajick, T. and Weber, W.M., (2016) Bringing reconfigurable nanowire FETs to a logic circuits compatible process platform, Proceedings of IEEE Nanotechnology Materials and Devices Conference (NMDC), pp. 1-3.

[95] Sistani M., Böckle R., Falkensteiner D., Luong M. A., Hertog M. I. d., Lugstein A. and Weber W. M. (2021), Nanometer-Scale Ge-Based Adaptable Transistors Providing Programmable Negative Differential Resistance Enabling Multivalued Logic, ACS Nano, 15, 18135-18141.

[96] Heinzig A., Slesazeck S., Kreupl F., Mikolajick T., and Weber W. M. (2012), Reconfigurable Silicon Nanowire Transistors, Nano Letters, 12, 119-124.

[97] Heinzig A., Mikolajick T., Trommer J., Grimm D., and Weber W. M. (2013), Dually Active Silicon Nanowire Transistors and Circuits with Equal Electron and Hole Transport, Nano Letters, 13, 4176-4181.

[98] Zhang J., Trommer J., Weber W. M., Gaillardon P.-E., and Micheli G. D. (2015), On Temperature Dependency of Steep Subthreshold Slope in Dual-Independent-Gate FinFET, IEEE Journal of the Electron Devices Society, 3, 452-456.

[99] Zhang J., Marchi M. D., Gaillardon P. -E. and Micheli G. D., (2014) A Schottky-barrier silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 decades of current, Proceedings of IEEE International Electron Devices Meeting, pp. 13.4.1-13.4.4.

[100] Rai S., Trommer J., Raitza M., Mikolajick T., Weber W. M., and Kumar A. (2019), Designing Efficient Circuits Based on Runtime Reconfigurable Field-Effect Transistors, IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, 27, 560-572.

[101] Trommer, J., Heinzig, A., Baldauf, T., Mikolajick, T., Weber, W.M., Raitza, M. and Völp, M., (2016) Reconfigurable nanowire transistors with multiple independent gates for efficient and programmable combinational circuits, Proceedings of IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 169-174.

[102] Amarú, L., Gaillardon, P.E., Zhang, J. and De Micheli, G., (2013) Power-gated differential logic style based on double-gate controllable-polarity transistors, IEEE Transactions on Circuits and Systems II: Express Briefs, 60, 672-676.

[103] Nirala, R.K., Semwal, S. and Kranti, A., (2022) A critique of length and bias dependent constraints for 1T-DRAM operation through RFET, Semiconductor Science and Technology, 37, 105013.

[104] Roy, A.S., Semwal, S. and Kranti, A., (2022) An insightful assessment of 1T-DRAM with misaligned polarity gate in RFET, IEEE Transactions on Electron Devices, 69, 3163-3168.

[105] Rai, S., Rupani, A., Nath, P. and Kumar, A., (2019) Hardware watermarking using polymorphic inverter designs based on reconfigurable nanotechnologies, Proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 663-669.

[106] Rai, S., Patnaik, S., Rupani, A., Knechtel, J., Sinanoglu, O. and Kumar, A., (2020) Security promises and vulnerabilities in emerging reconfigurable nanotechnology-based circuits, IEEE Transactions on Emerging Topics in Computing, 10, 763-778.

[107] Galderisi, G., Mikolajick, T. and Trommer, J., (2022) Reconfigurable field effect transistors design solutions for delay-invariant logic gates, IEEE Embedded Systems Letters, 14, 107-110.

[108] Neamen D. A., (2012) Semiconductor Physics and Devices: Basic Principles, 4th edn. McGraw-Hill, New York (ISBN 9780073529585).

[109] ATLAS User Manual. Silvaco, Santa Clara, CA, USA, 2015.

[110] Baldauf, T., Heinzig, A., Mikolajick, T. and Weber, W.M., (2019) Scaling aspects of nanowire Schottky junction based reconfigurable field effect transistors, Proceedings of IEEE Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), pp. 1-4.

[111] Sze, S. M., Li, Y., & Ng, K. K. (2021). Physics of semiconductor devices. John Wiley & Sons. (ISBN 978-0-470-06832-8).

[112] Colinge, J.P., (1998) Fully-depleted SOI CMOS for analog applications, IEEE Transactions on Electron Devices, 45, 1010-1016.

[113] Shahidi, G.G., (2002) SOI technology for the GHz era, IBM journal of Research and Development, 46, 121-131.

[114] Lee, S., Jagannathan, B., Narasimha, S., Chou, A., Zamdmer, N., Johnson, J., Williams, R., Wagner, L., Kim, J., Plouchart, J.O. and Pekarik, J., (2007) Record RF performance of 45-nm SOI CMOS technology, IEEE International Electron Devices Meeting (IEDM), pp. 255-258.

[115] Kranti, A., Burignat, S., Raskin, J.P. and Armstrong, G.A., (2009) Underlap channel UTBB MOSFETs for low-power analog/RF applications, Proceedings of the 10th IEEE International Conference on Ultimate Integration of Silicon, pp. 173-176.

[116] Kranti, A., Burignat, S., Raskin, J.P. and Armstrong, G.A., (2010) Analog/RF performance of sub-100 nm SOI MOSFETs with non-classical gate-source/drain underlap channel design, Proceedings of the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), pp. 45-48.

[117] Kranti, A., Raskin, J.P. and Armstrong, G.A., (2011) Source/Drain engineered ultra-low power analog/RF UTBB MOSFETs, Proceedings of IEEE Ultimate Integration on Silicon (ULIS), pp. 1-4.

[118] Ali, K.B., Neve, C.R., Gharsallah, A. and Raskin, J.P., (2012) RF SOI CMOS technology on commercial trap-rich high resistivity SOI wafer, Proceedings of IEEE International SOI Conference, pp. 1-2.

[119] Kilchytska, V., Arshad, M.M., Makovejev, S., Olsen, S., Andrieu, F., Poiroux, T., Faynot, O., Raskin, J.P. and Flandre, D., (2012) Ultra-thin body and thin-BOX SOI CMOS technology analog figures of merit, Solid-State Electronics, 70, 50-58.

[120] Arshad, M.M., Makovejev, S., Olsen, S., Andrieu, F., Raskin, J.P., Flandre, D. and Kilchytska, V., (2013) UTBB SOI MOSFETs analog figures of merit: Effects of ground plane and asymmetric double-gate regime, Solid-state electronics, 90, 56-64.

[121] Joshi, A., Lee, T.Y., Chen, Y.Y. and Whitefield, D., (2014) Recent advances and future trends in SOI for RF applications, Proceedings of IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp. 1-3.

[122] Itocazu, V.T., Sonnenberg, V., Simoen, E., Claeys, C. and Martino, J.A., (2015) Ground plane influence on UTBB SOI nMOSFET analog parameters, Proceedings of IEEE 30th Symposium on Microelectronics Technology and Devices (SBMicro), pp. 1-4.

[123] Shaked, Z., Hurwitz, P., Heiman, A., Moen, K., Kanawati, R., Chaudhry, S. and Racanelli, M., (2015) SOI technology for front end applications, Proceedings of IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS), pp. 1-3.

[124] Itocazu, V.T., Sonnenberg, V., Simoen, E., Claeys, C. and Martino, J.A., (2016) Influence of different UTBB SOI technologies on analog parameters, Proceedings of IEEE 31st Symposium on Microelectronics Technology and Devices (SBMicro), pp. 1-4.

[125] Raskin, J.P., (2016) SOI technology pushes the limits of CMOS for RF applications, Proceedings of IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), pp. 17-20.

[126] Kilchytska, V., Esfeh, B.K., Gimeno, C., Parvais, B., Planes, N., Haond, M., Raskin, J.P. and Flandre, D., (2017) Comparative study of non-linearities in 28 nm node FDSOI and Bulk MOSFETs, Proceedings of IEEE Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), pp. 128-131.

[127] Raskin, J.P., (2022) Fully depleted SOI technology for millimeter-wave integrated circuits, IEEE Journal of the Electron Devices Society, 10, 424-434.

[128] Dixit, A., Kottantharayil, A., Collaert, N., Goodwin, M., Jurczak, M. and De Meyer, K., (2005) Analysis of the parasitic S/D resistance in multiple-gate FETs, IEEE Transactions on Electron Devices, 52, 1132-1140.

[129] Subramanian, V., Parvais, B., Borremans, J., Mercha, A., Linten, D., Wambacq, P., Loo, J., Dehan, M., Collaert, N., Kubicek, S. and Lander, R.J.P., (2005) Device and circuit-level analog performance trade-offs: a comparative study of planar bulk FETs versus FinFETs, Proceedings

of IEEE International Electron Devices Meeting (IEDM) Technical Digest, pp. 898-901.

[130] Lederer, D., Kilchytska, V., Rudenko, T., Collaert, N., Flandre, D., Dixit, A., De Meyer, K. and Raskin, J.P., (2005) FinFET analogue characterization from DC to 110 GHz, Solid-State Electronics, 49, 1488-1496.

[131] Lederer, D., Parvais, B., Mercha, A., Collaert, N., Jurczak, M., Raskin, J.P. and Decoutere, S., (2006) Dependence of FinFET RF performance on fin width, Digest of Papers. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, pp. 4.

[132] Lim, T.C., Kranti, A. and Armstrong, G.A., (2006) Performance assessment of nanoscale multiple gate MOSFETs (MuGFETs) for RF applications, Proceedings of IEEE European Microwave Integrated Circuits Conference, pp. 308-311.

[133] Kranti, A. and Armstrong, G.A., (2007) Comparative analysis of nanoscale MOS device architectures for RF applications, Semiconductor science and technology, 22, 481.

[134] Subramanian, V., Mercha, A., Parvais, B., Dehan, M., Groeseneken, G., Sansen, W. and Decoutere, S., (2010) Identifying the bottlenecks to the RF performance of FinFETs, Proceedings of IEEE 23rd International Conference on VLSI Design, pp. 111-116.

[135] Raskin, J.P., (2015) FinFET versus UTBB SOI - an RF perspective, Proceedings of IEEE 45th European Solid State Device Research Conference (ESSDERC), pp. 84-88.

[136] Raskin, J.P., (2016) FinFET and UTBB for RF SOI communication systems, Solid-State Electronics, 125, 73-81.

[137] Beigné, E., Christmann, J.F., Valentian, A., Billoint, O., Amat, E. and Morche, D., (2015) UTBB FDSOI technology flexibility for ultra-low power internet-of-things applications, Proceedings of IEEE 45th European Solid State Device Research Conference (ESSDERC), pp. 164-167.

[138] Carter, R., Mazurier, J., Pirro, L., Sachse, J.U., Baars, P., Faul, J., Grass, C., Grasshoff, G., Javorka, P., Kammler, T. and Preusse, A., (2016) 22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications, Proceedings of IEEE International Electron Devices Meeting (IEDM), pp. 2-2.

[139] Raskin, J.P., (2018) Fully Depleted SOI Technologies from Digital to RF and beyond, Proceedings of IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp. 1-3.

[140] Cathelin, A., (2017) Fully depleted silicon on insulator devices CMOS: The 28-nm node is the perfect technology for analog, RF, mmW, and mixed-signal system-on-chip integration, IEEE Solid-State Circuits Magazine, 9, 18-26.

[141] Chevalier, P., Gianesello, F., Pallotta, A., Goncalves, J.A., Bertrand, G., Borrel, J., Boissonnet, L., Brezza, E., Buczko, M., Canderle, E. and Celi, D., (2020) PD-SOI CMOS and SiGe BiCMOS Technologies for 5G and 6G communications, Proceedings of IEEE International Electron Devices Meeting (IEDM), pp. 34-4.

[142] Fettweis, G., Leo, K., Voit, B., Schneider, U. and Scheuvens, L., (2018) Venturing electronics into unknown grounds, Proceedings of IEEE International Electron Devices Meeting (IEDM), pp. 1-2.

[143] Couriol, M., Cadareanu, P., Giacomin, E. and Gaillardon, P.E., (2021) A novel high-gain amplifier circuit using super-steep-subthreshold-slope field-effect transistors, Proceedings of IFIP/IEEE 29th International Conference on Very Large-Scale Integration (VLSI-SoC), pp. 1-6.

[144] Bhattacharjee, A., Saikiran, M. and Dasgupta, S., (2017) A first insight to the thermal dependence of the DC, analog and RF performance of an S/D spacer engineered DG-ambipolar FET, IEEE Transactions on Electron Devices, 64, 4327-4334.

[145] Dickson, T.O., Yau, K.H., Chalvatzis, T., Mangan, A.M., Laskin, E., Beerkens, R., Westergaard, P., Tazlauanu, M., Yang, M.T. and Voinigescu, S.P., (2006) The invariance of characteristic current densities in nanoscale

MOSFETs and its impact on algorithmic design methodologies and design porting of Si (Ge)(Bi) CMOS high-speed building blocks, IEEE Journal of Solid-State Circuits, 41, 1830-1845.

[146] Seabaugh, A.C. and Zhang, Q., (2010) Low-voltage tunnel transistors for beyond CMOS logic, Proceedings of the IEEE, 98, pp.2095-2110.

[147] Cadareanu, P., Romero-Gonzalez, J. and Gaillardon, P.E., (2021) Parasitic capacitance analysis of three-independent-gate field-effect transistors, IEEE Journal of the Electron Devices Society, 9, 400-408.

[148] Lacord, J., Ghibaudo, G. and Boeuf, F., (2012) Comprehensive and accurate parasitic capacitance models for two-and three-dimensional CMOS device structures, IEEE Transactions on Electron Devices, 59, 1332-1344.

[149] Mane, S., Semwal, S. and Kranti, A., (2021) Improved mobility extraction methodology for reconfigurable transistors considering resistive components and effective drain bias, IEEE Transactions on Electron Devices, 68, 4797-4800.

[150] B. Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2001 (ISBN 978-9325983274).

[151] Song, I., Jeon, J., Jhon, H.S., Kim, J., Park, B.G., Lee, J.D. and Shin, H., (2008) A simple figure of merit of RF MOSFET for low-noise amplifier design, IEEE Electron Device Letters, 29, 1380-1382.

[152] Toole, B., Plett, C. and Cloutier, M., (2004) RF circuit implications of moderate inversion enhanced linear region in MOSFETs, IEEE Transactions on Circuits and Systems I: Regular Papers, 51, 319-328.

[153] Danilovic, D., Milovanovic, V., Cathelin, A., Vladimirescu, A. and Nikolic, B., (2016) Low-power inductorless RF receiver front-end with IIP2 calibration through body bias control in 28nm UTBB FDSOI, Proceedings of IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp. 87-90.

[154] Khakifirooz, A. and Antoniadis, D. A., (2008) MOSFET performance scaling—Part II: Future directions, IEEE Transactions on Electron Devices, 55, 1401-1408.

[155] Rai, S., Rupani, A., Walter, D., Raitza, M., Heinzig, A., Baldauf, T., Trommer, J., Mayr, C., Weber, W. M. and Kumar, A., (2018) A physical synthesis flow for early technology evaluation of silicon nanowire based reconfigurable FETs, Proceedings of IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 605–608.

[156] Quijada, J. N., Baldauf, T., Rai, S., Heinzig, A., Kumar, A., Weber, W. M., Mikolajick, T. and Trommer, J., (2022) Germanium Nanowire Reconfigurable Transistor Model for Predictive Technology Evaluation, IEEE Transactions on Nanotechnology, 21, 728-736.