Low Power CMOS Integrated Circuits for Phase-Locked Loop Frequency Synthesizers

Ph.D. Thesis

By

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A THESIS

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled "**LOW POWER CMOS INTEGRATED CIRCUITS FOR PHASE-LOCKED LOOP FREQUENCY SYNTHESIZERS**" in the partial fulfillment of the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY** and submitted in the **DEPARTMENT OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from March 2015 to September 2022 under the supervision of Dr. Santosh Kumar Vishvakarma, Professor at Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Ravi Kumar

29/09/2022

Signature of the student with date

(RAVI KUMAR)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Santosh

22/09/2022

Signature of Thesis Supervisor with date

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RAVI KUMAR has successfully given his Ph.D. Oral Examination held on 08/07/2024.

Santosh

08/07/2024

Signature of Thesis Supervisor with date

(DR. SANTOSH KUMAR VISHVAKARMA)

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Dedicated

to

my beloved family and well-wishers

ABSTRACT

With the progress in science and technology where most electronic devices are connected over the internet, the demand for data transmission and data storage has increased rapidly. With this increasing demand for higher data transmission, low-power and low-cost circuit design has become a great concern for Radio Frequency integrated circuit (RFIC) designers. Various new protocols and standards such as IEEE 802.3cd, IEEE 802.3bs, and optical inter-networking forum (OIF) CEI-56G/112G have been proposed which increases the data transmission rate through a single channel. Phase locked loop (PLL) based frequency synthesizers have become one of the most critical elements of such high-speed transceivers since their performance dictates the quality of communication.

The performance matrix of a PLL includes low Phase Noise/Jitter, low reference spur, wide tuning range, lower settling time, lower power consumption, and less silicon area. Voltage Controlled Oscillator (VCO) is the major noise contributor to the loop and can eat up a larger silicon area when implemented with an LC tank. Since VCO and divider are the two blocks running at the highest frequency, they become the major contributor to total power consumption. Therefore, achieving lower power consumption while meeting other application specific requirements in PLL is taken up as a scope of this thesis.

Addressing the power consumption issue, the major contribution of the thesis targets the design of low-power prescalers. With our specific interest in low power and low area circuits, we focus our discussion on low-power and high-frequency divider architectures, and best practices to achieve high-frequency operation with low power and minimum active silicon area.

To achieve low power operation in frequency dividers, a novel dual modulus prescaler architecture is proposed for loop divider using True Single-Phase Clocking (TSPC) logic. Another work on the frequency divider addresses the duty cycle issue which tries to achieve close to 50% duty cycle for an output clock signal.

Besides this, the fabrication process, operating voltage, and temperature (PVT) have a predominant effect on the performance of Oscillators and can change oscillator gain (K_{VCO}). It can directly affect the PLL performance by increasing locking time or pushing the PLL out of the lock. Therefore, a novel constant-transconductance bias technique is proposed to reduce the PVT sensitivity of an oscillator.

A novel Folded Cascode Opamp with enhanced gain and low input referred noise is also explored. The final contribution is made towards a low-power and low-jitter charge pump PLL for wire-line communication systems.

Contents

List of Figures

List of Tables

List of Abbreviations

IoT	:	Internet of Things
IC	:	Integrated Circuit
MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor
PMOS	:	P-type Metal Oxide Semiconductor
NMOS	:	N-type Metal Oxide Semiconductor
CMOS	:	Complimentary Metal Oxide Semiconductor
PLL	:	Phase Locked Loop
PFD	:	Phase Frequency Detector
V2I	:	Voltage to Current Converter
CCO	:	Current Controlled Oscillator
VCO	:	Voltage Controlled Oscillator
LPF	:	Low Pass Filter
CSVCO	:	Current Starved Voltage Controlled Oscillator
CP	:	Charge Pump
CPPLL	:	Charge Pump Phase Locked Loop
RF	:	Radio Frequency
Opamp	:	Operational Amplifier
RO	:	Ring Oscillator
PVT	:	Process Voltage Temperature
BGR	:	Band Gap Reference
FC	:	Folded Cascode
OTA	:	Operational Transconductance Amplifier
UGB	:	Unity Gain Bandwidth
PSD	:	Power Spectral Density
FVF	:	Flipped Voltage Follower
SNR	:	Signal to Noise Ratio

List of Symbols

V_{th}	:	Threshold voltage
g_m	:	Transconductance
g_{ds}	:	Drain to Source Transconductance
V_{DD}	:	Supply voltage
V_{ds}	:	Drain to source voltage
V_{gs}	:	Gate to source voltage
V_{SB}	:	Drain to Source to body voltage
γ	:	Body effect coefficient
R_{ds}	:	Drain to source resistance
T	:	Temperature
W/L	:	Transistor width to length ratio
σ	:	Standard Deviation

Chapter 1

Introduction

1.1 Background and Motivation

Modern Systems-on-Chip (SoCs) integrate various subsystems on a single chip operating at different clock speeds. Clocking support to these subsystems is provided by numerous Phase Locked Loops which take off-chip crystal output as a reference and generate high-speed on-chip clock signal providing multiple clocks to SoC. Figure 1.1 shows an example of such SoC which boasts ∼20 PLLs for clock generation and accounts for 7% of total SoC power [1]. The SoC is made up of elements such as the CPU, GPU, DDR, PCIe, and others that operate at frequencies between a few MHz and GHz. One of SoC's serial link communication systems, PCIe operates at a very high speed and has stringent noise performance specifications for its input and output clock signals.

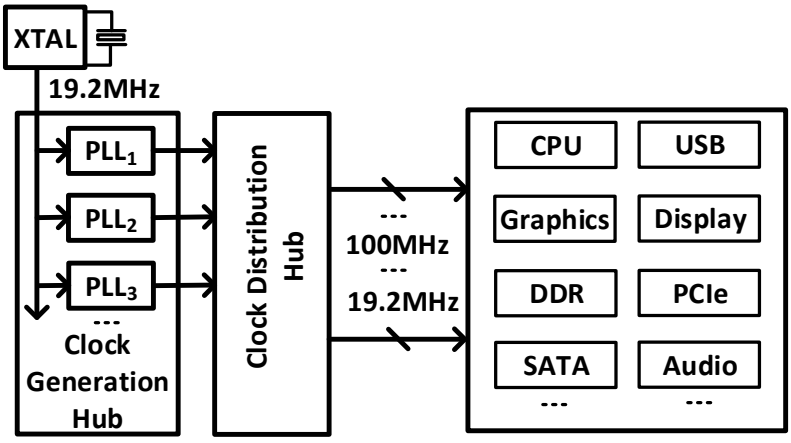


Figure 1.1: Clock generation and distribution in typical SoC with single crystal (XTAL)

Figure 1.2 depicts the block diagram of a typical serial link transceiver where the Transmitter takes serial input data D_{in} and transmits it through a physical channel by the output driver. At the receiving end, the signal is amplified first for detection, and then recovered using Clock and Data Recovery (CDR) circuit. PLL at the transmitter side (Tx-PLL) and receiver side (Rx-PLL) are used to provide a clock for transmitting the data and receiving the data, respectively. Since serial communication link works at high frequencies, for error-free transmission and detection, clock

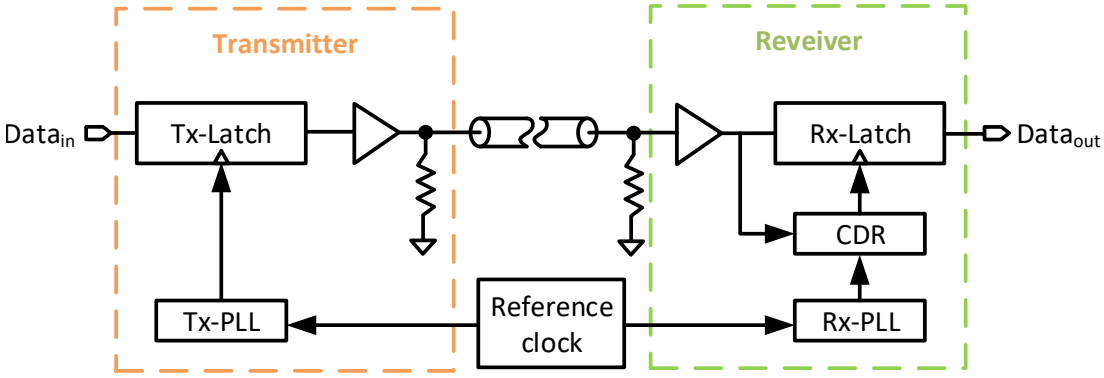


Figure 1.2: Typical serial link transceiver

generating circuitry also has very tight specifications in terms of phase noise and jitter.

Similar to wire-line communication, frequency synthesizer plays an important role in wireless communication. Figure 1.3 shows the system level design of RF transceiver. The left side shows the up-conversion where the synthesizer signal is modulated for transmission and right side shows the down-conversion where the received signal is modulated by the synthesizer signal. Therefore, the frequency synthesizer plays a crucial role in channel selection here.

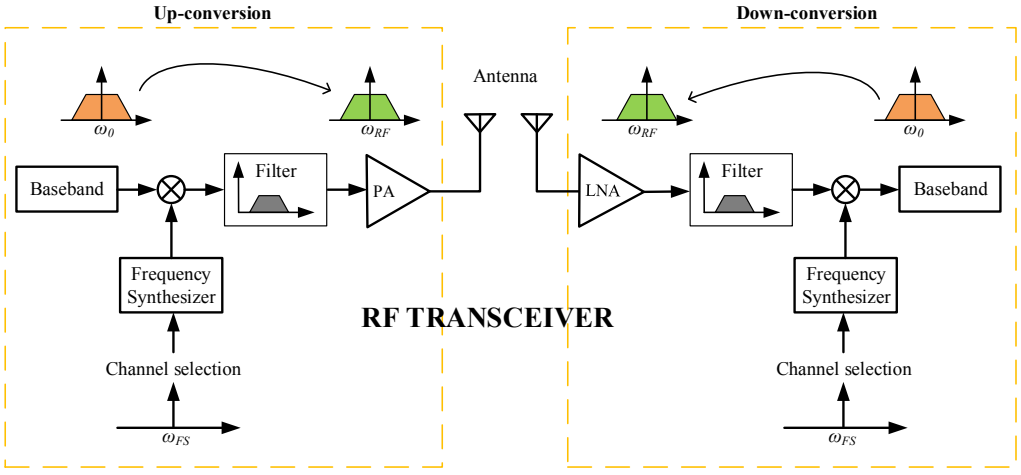


Figure 1.3: Frequency synthesis in RF transceiver

All the systems discussed above use frequency synthesizers for frequency synthesis or high-speed clock generation. Two types of architectures exist for a frequency synthesizer, direct frequency synthesizer and indirect frequency synthesizer [2, 3]. Direct frequency synthesizer does not have any feedback loop and can be implemented in analog or digital. Although this type of synthesizer has very fast switching speed, it is not suitable for high-speed applications. On the other hand, indirect frequency synthesizers are implemented using PLL and have slower switching speed. However, low power dissipation also becomes a necessity for current SoCs when several PLLs are used to supply clocks to numerous subsystems.

Even though the power dissipated by PLL can be a small fraction of total active power, during the sleep mode of the IC it can still be significant. For modern SoCs where multiple PLLs are

employed to provide clocks to numerous subsystems, lower power dissipation also becomes a must requirement. In the advent of the Internet of Things where tons of data are being processed at high-speed, lower power consumption is one of the popular demands for battery-operated devices [4–6]. Therefore, the objective of the thesis is to investigate the low power analog PLL components and their design, keeping intact the noise performance.

1.2 Thesis Contributions

This thesis reports the design and analysis of charge pump PLL's sub-blocks. The key contributions of this thesis are summarized below -

1. A Low Power Dual Modulus Prescaler

In this work, a dual modulus prescaler is designed using True Single-Phase Clocking (TSPC). Since it contains D flip-flops and logic gates, a novel dual modulus prescaler is proposed. It comprises a Pulse Extension logic to switch between N and N+1 division ratios. Additionally, redundant TSPC stages are eliminated to save power consumption and the active silicon area occupied by the circuit.

2. A Programmable Output Divider with 50% Duty Cycle

This work suggests a novel frequency divider for the output clock of a PLL. This study offers a solution to the modern System on Chips (SoC) multi-clock requirement, which calls for the use of several PLLs to supply various parts with numerous clock signals. Multiple dividers can be placed at the output of a PLL that can generate multiple frequencies instead of using multiple PLLs to generate lower harmonic frequencies. This divider has duty cycle correction circuitry that brings the output duty cycle close to 50%.

3. A Constant Transconductance Bias Technique for VCO

A novel bias technique for VCO using constant-g_m is proposed in this work. Since the oscillator's gain can vary 3 times across Process Voltage and Temperature, it can increase the locking time of the PLL. This technique tries to compensate for this PVT variation by negative feedback which tracks the transconductance of VCO stages and compensates the frequency.

4. A Gain Enhanced Folded Cascode Opamp

In this work, a novel folded cascode Opamp is proposed for low noise and high gain operations. It has large voltage swing, lesser area and power consumption as compared to traditional FC Opamps.

5. A 2-4 GHz Low Power and Low Jitter Charge Pump PLL

In this work, a 2-4 GHz charge pump PLL is discussed which employs the proposed 2/3 dual modulus prescaler as the first stage in feedback divider. The implemented design takes advantage of Ring Oscillator over the LC tank for further power reduction.

1.3 Thesis Organization

The remaining sections of this thesis is organized as follows:

- **Chapter 2** - The fundamentals of frequency synthesizer and it's building blocks such as Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), Voltage Controlled Oscillator (VCO), and Frequency Divider are discussed in this chapter. The chapter explains the PLL's performance matrix including Jitter, phase noise, stability, bandwidth, etc. This chapter also provides a concise overview of the key challenges involved in designing a PLL such as dead-zone, current mismatch in charge pump, locking failure, and bandwidth limitations.

- **Chapter 3** - The design and analysis of a novel dual modulus prescaler for a feedback loop divider are covered in this chapter. To extend the division from 2 to 3, a new 2/3 circuit is developed in which a two stage TSPC logic is employed rather than a four stage TSPC flip-flop. A novel 8/9 dual modulus prescaler for low power applications is designed using the proposed 2/3 prescaler.

- **Chapter 4** - In order to produce lower harmonics of a PLL output frequency outside of a PLL, this chapter demonstrates the design and analysis of a programmable output frequency divider. This proposed divider supports 50% duty cycle therefore can be used for any clock signals which has the same requirement.

- **Chapter 5** - This chapter demonstrates the proposed constant g_m bias techniques to compensate PVT variations in a VCO. Due to PVT, oscillation frequency changes by almost 3-times which is not desirable when working with limited bandwidth PLL. The proposed technique provides a solution to compensate this PVT variation on VCO by using a negative feedback system.

- **Chapter 6** - The proposed design of a novel Folded Cascode (FC) Opamp providing low noise and high gain is discussed in this chapter. It uses novel gain boosting technique to achieve higher gain while maintaining lower power consumption. Because of its large swing it can be used in a charge pump as well for better current mismatch.

- **Chapter 7** - This chapter discusses the implemented 2-4 GHz low jitter PLL. It uses the novel 2/3 dual modulus prescaler discussed in chapter 3 as the first stage of the frequency divider. The demonstrated PLL appears to be suitable for wire-line applications.

- **Chapter 8** - Finally, the thesis is concluded in this chapter. Additionally, limitation of the presented work and the direction of the future research work is also provided.

Chapter 2

Phase-Locked Loop Fundamentals

Phase-Locked Loop based frequency synthesizers are extensively used in high-speed microprocessors, serial link communication and wireless communication systems. Mostly three major types of PLL are common for transceivers - Analog/Charge-pump PLL (CPPLL), Hybrid PLL and All-digital PLL (ADPLL). A charge pump based PLL is chosen for this work which is suitable as clock generator for wire-line communication systems. The basics of CPPLL, its components, and their shortcomings are covered in this chapter. Additionally, design challenges of a CPPLL are also discussed.

2.1 Introduction

2.1.1 Operating principle

A PLL is a negative feedback system which tracks the frequency and phase of input reference signal in order to generate a periodic output. Figure 2.1 shows the generic block diagram of a PLL consisting Phase Detector (PD), low pass filter/loop filter (LPF), Voltage Controlled Oscillator (VCO) and frequency divider. Reference clock (Ref_{clk}) is derived from a crystal oscillator and offers excellent phase noise performance. Although crystal oscillators can be used for frequency synthesis but they have their own limitations. For example they can't generate clock signal of more than few MHz frequency and only one clock signal can be extracted from a single crystal which makes them unsuitable for frequency synthesis. The PLL loop tracks the frequency and phase of this clean clock and tries to minimize the phase difference between Ref_{clk} and feedback signal $Fdiv_{clk}$. PD generates output error signal which has an average value proportional to the phase difference of the inputs.

The loop filter generates controlled voltage to drive the VCO based on the error signal and modifies the frequency of the output VCO_{clk}. Frequency divider divides down the VCO's output phase and frequency by a specified division number "N" and makes the phase and frequency of VCO_{clk} comparable to Ref_{clk}. This cycle of lowering or raising the VCO's control voltage continues until the phase error caused by the PD achieves zero or a steady value. By employing the negative

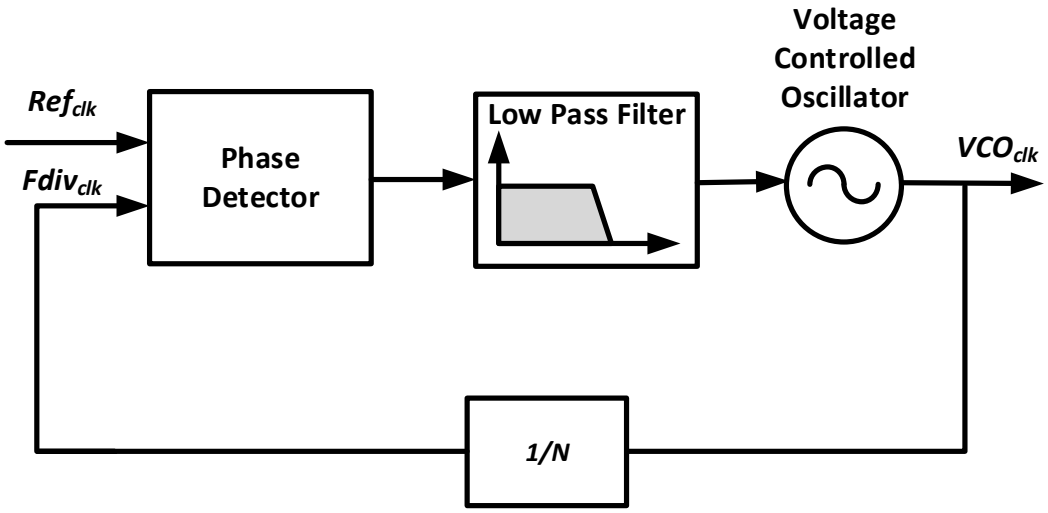


Figure 2.1: Block diagram of a basic Phase Locked Loop

feedback, PLL tracks the Ref_{clk} and attempts to deliver a high frequency and low noise clock. If the VCO_{clk} drifts in any way, PD generates the error signal, which once more restores the VCO to the proper frequency. Since RF transceivers undertake multiple channel selection, a PLL-based frequency synthesizer's division value N is made programmable in order to obtain the required channel frequency [7, 8].

Being a negative feedback system, it also suffers from stability issues. Phase errors that exceeds the PLL's acquisition range may prevent the PLL from ever reaching to a locked state. Similar to this, a few other factors affect the time and frequency response of the PLL loop, which will be covered in more detail in the next sections.

When it comes to implementation, PLLs may be constructed using analog as well as digital components. An ADPLL contains fully digital blocks whereas Analog PLL contains all analog components. Hybrid PLL on the other side uses both analog as well as digital in a single loop depending on the application [9–12].

2.1.2 Type-I PLL

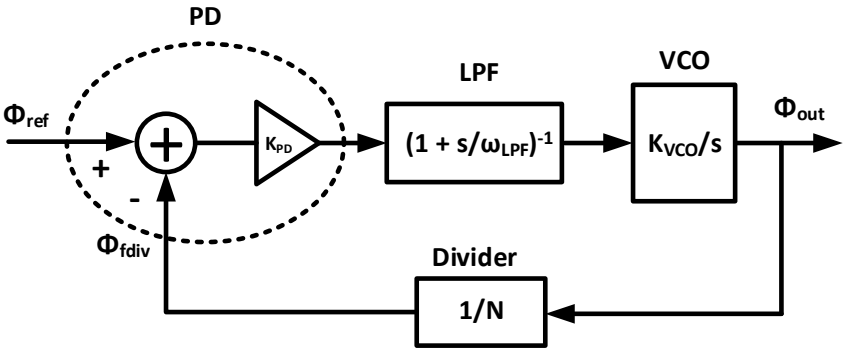


Figure 2.2: Block diagram of the type-I PLL's linear model

Figure 2.2 shows the linear gain model block diagram of the type-I PLL which employs PD

as comparator. This PD generates output proportional to phase difference of Ref_{clk} and $Fdiv_{clk}$. Gain of each block is mentioned in the linear model itself. The open loop transfer function in S-domain ($H_O(s)$) can be given as

$$H_O(s) = \phi_{out}/\phi_{ref} = \frac{K_{PD}K_{VCO}}{NS}F(s) \tag{2.1}$$

where K_{PD} and K_{VCO} represents the gain of PD and VCO, respectively. F(s) represents the loop filter's transfer function. If F(s) is first order low pass filter, it's transfer function is given as [13]

$$F(s) = \frac{1}{1 + s/\omega_{LPF}} \tag{2.2}$$

where ω_{LPF} represents 3-db frequency of the LPF. Replacing the F(s) transfer function in 2.1, the open loop transfer function can be reformulated as

$$H_O(s) = \phi_{out}/\phi_{ref} = \frac{K_{PD}K_{VCO}}{N}\frac{1}{s(1 + s/\omega_{LPF})} \tag{2.3}$$

Since the equation above has only one pole at zero, this sort of PLL is called type-I PLL. Owing to the pole at origin, ϕ_{out} goes to infinity if s goes to zero. It implies that the PLL in closed loop condition ensures to track the slow varying excess phase ϕ_{ref}.

Closed loop transfer function H(s) of the type-I PLL can be written as

$$H(s) = \frac{K_{PD}K_{VCO}}{s^2/\omega_{LPF} + s + K_{PD}K_{VCO}/N} \tag{2.4}$$

From (2.4), transfer function contains two poles. This equation is comparable to the second order equation of the control system theory [14] which is given as

$$H(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{2.5}$$

where ω_n is natural frequency and ξ is the damping factor which defines whether the closed loop system is under-damped, critically-damped or over-damped.

By equating (2.4) and (2.5), ω_n and ξ of the type-I PLL system can be written as

$$\omega_n = \sqrt{\frac{\omega_{LPF}K_{PD}K_{VCO}}{N}} \tag{2.6}$$

$$\xi = \frac{1}{2}\sqrt{\frac{\omega_{LPF}N}{K_{PD}K_{VCO}}} \tag{2.7}$$

and product of ξ and ω_n turns out to be $\omega_{LPF}/2$.

From control theory, two poles of the second order system in (2.5) are given by

$$S_{1,2} = -\xi\omega_n \pm \omega_n\sqrt{\xi^2 - 1} \tag{2.8}$$

Therefore, poles of the closed loop system of type-I PLL are located at

$$S_{1,2} = \frac{\omega_{LPF}}{2} \pm \frac{1}{2}\sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}} \tag{2.9}$$

From above equation, when $\omega_{LPF}^2 - 4K_{PD}K_{VCO}/N > 0$, closed loop system becomes over damped and therefore has real poles. In this case, transient response of the system contains two exponential with time constant equivalent to reciprocal of pole locations, $1/S_1$ and $1/S_2$. In the other scenario when $\omega_{LPF}^2 - 4K_{PD}K_{VCO}/N < 0$, system becomes under-damped and has complex poles. In this case ,transient response of the system to unity step input frequency is given by

$$\omega_{out}(t) = \left[1 - e^{-\frac{t}{2}\omega_{LPF}} \cos\left(\sqrt{4K_{PD}K_{VCO}/N - \omega_{LPF}^2}\right)t\right] N\Delta\omega u(t) + \left[\frac{\omega_{LPF}}{\sqrt{4K_{PD}K_{VCO}/N - \omega_{LPF}^2}} \sin\left(\sqrt{4K_{PD}K_{VCO}/N - \omega_{LPF}^2}\right)t\right] N\Delta\omega u(t) \tag{2.10}$$

where $\omega_{out}(t)$ represents the change in the output frequency and $\Delta\omega u(t)$ represents the unit step change in input frequency. Above equation contains a sinusoidal response with the frequency $(4K_{PD}K_{VCO}/N - \omega_{LPF}^2)^{1/2}$ which decays with the time constant $2/\omega_{LPF}$.

Step changes in input phase exhibit the same response as in (2.10) because the instantaneous frequency of any signal is the time derivative of its phase. In order to get the faster settling of the output, ω_{LPF} must be maximized because the exponential decay represents the settling time of the output waveform. However, lower value of ω_{LPF} is required to suppress high frequency noise components from the PD. This is a trade-off between settling time and ripple on the control voltage of VCO. Another crucial factor is $K_{PD}K_{VCO}$ which must be kept high to reduce phase error of the phase detector but it's higher value tends to reduces the damping factor ξ and thus stability of the overall system. These are the trade-offs of in type-I PLL between ripple, settling time and stability.

Another limitation of type-I PLL is it's acquisition range. Since input frequencies to PD are unequal, locking of the loop becomes nonlinear process and loop fails to lock itself if the difference between ω_{Ref} and ω_{Fdiv} is not in order of ω_{LPF} [7, 8]. All these issues of the type-I PLL are addressed by type-II PLL [8] which replaces PD by Phase Frequency Detector (PFD) and a Charge Pump (CP) circuit.

2.1.3 Type-II PLL

Figure 2.3 shows the architectural block diagram of a charge pump PLL. Instead of using only phase detection in the loop, Phase Frequency Detector is employed for both phase and frequency detection. PFD generated UP and DN pulses according to phase error. Charge pump switches are turned ON and OFF according to logic level of UP and DN signal, which can either source the current to the loop filter or sink the current from the loop filter to generate control voltage for VCO. Being the discrete system, S-domain analysis for PLL holds true if bandwidth of the system

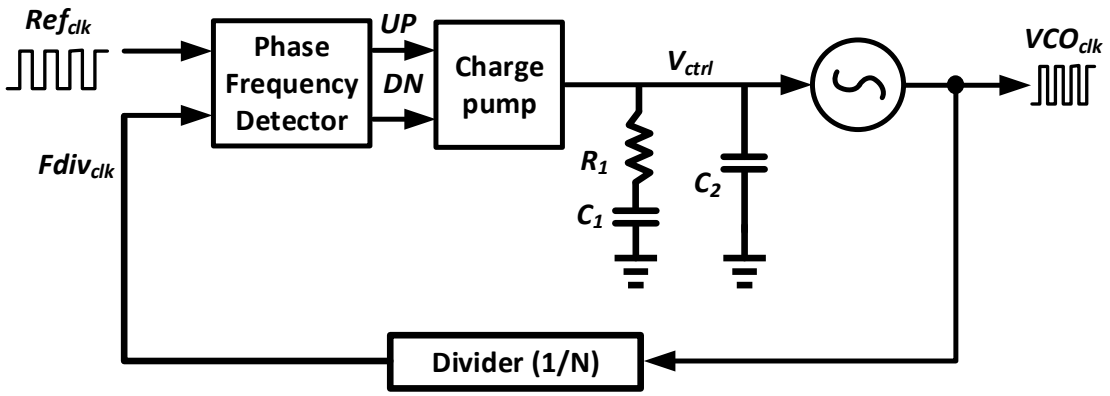


Figure 2.3: Block diagram of a type-II third order charge pump PLL

is kept around $1/10^{th}$ of the reference frequency [8].

Figure 2.4 shows the linear model of the charge pump PLL where each block is represented by it's transfer function. Considering $\phi_{err} = \phi_{ref} - \phi_{fdiv}$ as average phase error output of PFD and

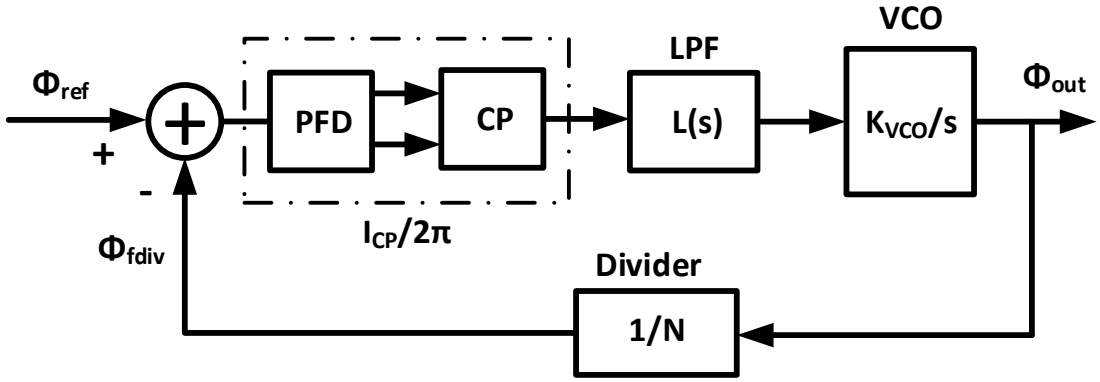


Figure 2.4: Linear Model of the Charge Pump PLL

I_d as average current output of the charge pump, overall gain of PFD with charge-pump can be written as

$$\frac{I_d(s)}{\phi_{err}(s)} = \frac{I_{CP}}{2\pi} \tag{2.11}$$

where I_{CP} represents the charging and discharging current of CP.

Transfer function of the passive 2^{nd} order loop filter shown in Figure 2.3 is given by

$$L(s) = \frac{s + \frac{1}{R_1 C_1}}{C_2 s \left(s + \frac{1}{R_1 \frac{C_1 C_2}{C_1 + C_2}} \right)} \tag{2.12}$$

Therefore, the open loop transfer function of the type-II third order PLL can be written as

$$H_O(s) = \frac{K_{VCO} I_{CP}}{2\pi N} \frac{s + \frac{1}{R_1 C_1}}{C_2 s^2 \left(s + \frac{1}{R_1 \frac{C_1 C_2}{C_1 + C_2}} \right)} \tag{2.13}$$

Since above transfer function contains two poles at origin and has denominator of 3^{rd} order system, this type of PLL is called type-II third order PLL. In the above equation, two poles at the origin represents two integrator in the loop, one from VCO and other one is generated by loop capacitance C_2. Zero and pole location frequencies of the (2.13) are given by

$$\omega_z = 1/R_1C_1 \tag{2.14}$$

$$\omega_{p1} = 0, \qquad \omega_{p2} = 0, \qquad \omega_{p3} = \frac{1}{R_1 \frac{C_1C_2}{C_1+C_2}} \tag{2.15}$$

Above equations indicates the system has two poles at the origin, one zero (ω_z) located at $1/R_1C_1$ and one pole (ω_{p3}) at $(C_1+C_2)/R_1C_1C_2$. In order to have a stable system, ω_z must be lesser than Unity Gain Bandwidth (ω_{ugb}) whereas ω_{p3} needs to have much larger value than the (ω_{ugb}).

Similarly, the closed-loop transfer function of the type-II third-order CPPLL system can be written as

$$H(s) = \frac{K_{vco}I_{CP}}{2\pi NC_2} \frac{s + \frac{1}{R_1C_1}}{s^3 + \frac{1}{R\left(\frac{C_1C_2}{C_1+C_2}\right)}s^2 + \frac{K_{VCO}I_{CP}}{2\pi NC_2}s + \frac{K_{VCO}I_{CP}}{2\pi NRC_1C_2}} \tag{2.16}$$

For the stability of the PLL loop, if previously mentioned limitation "$\omega_z < \omega_{ugb} < \omega_{p3}$" holds true, than (2.16) can be approximated as

$$H(s) = \frac{K_{VCO}I_{CP}}{2\pi NC_2} \frac{1 + sR_1C_1}{s^2 + \frac{K_{VCO}I_{CP}R}{2\pi N}s + \frac{K_{VCO}I_{CP}}{2\pi NC_2}} \tag{2.17}$$

After comparing (2.17) with (2.5), natural frequency and the damping factor for the type-II PLL system can be given as

$$\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi NC_2}}, \qquad \xi = \frac{R}{2}\sqrt{\frac{K_{VCO}I_{CP}C_2}{2\pi N}} \tag{2.18}$$

Phase margin (Φ_M) dictates the stability of any feedback system. Looking at the closed loop transfer function in (2.17), it's phase margin can be written as

$$\Phi_M = \arctan\left(\frac{\omega_{ugb}}{\omega_z}\right) - \arctan\left(\frac{\omega_{ugb}}{\omega_{p3}}\right) \tag{2.19}$$

where second term shows the degradation in phase margin due to extra pole created by R_1 and C_2. Pole locations of the closed loop system are given by

$$S_{1,2} = -\frac{I_{CP}K_{VCO}R_1}{4\pi N} \pm \frac{1}{2}\sqrt{\left(\frac{I_{CP}K_{VCO}}{2\pi N}\right)\left(\frac{I_{CP}K_{VCO}R^2}{2\pi N} - \frac{4}{C_2}\right)} \tag{2.20}$$

From the above equation, the closed loop system becomes under-damped when $\frac{I_{CP}K_{VCO}}{2\pi N} < \frac{4}{C_2R^2}$.

2.2 Divider Driven Architectures of PLL

The frequency synthesizer's programmability is introduced by the loop divider, which also produces output frequencies with a predetermined channel spacing. The following sections cover the two architectures of frequency synthesizer's-

2.2.1 Integer-N PLL

Integer-N frequency synthesizer consists of an integer divider in the feedback loop which can change it's value in integer steps. Output frequencies have the channel spacing of reference signal due to an integer divider [15–17]. This architecture limits the loop bandwidth to be much lower than the reference frequency [8]. This limitation on bandwidth results in higher settling time and higher in-band phase noise.

Figure 2.5 shows the Pulse Swallow Counter based divider which is commonly used in Integer-N PLLs. This prescaler is implemented using a programmable counter, a pulse swallow counter and a dual modulus divider. Both Programmable and swallow counters are used to select the desired channel frequency range. More detailed description of this prescaler is presented in chapter 4.

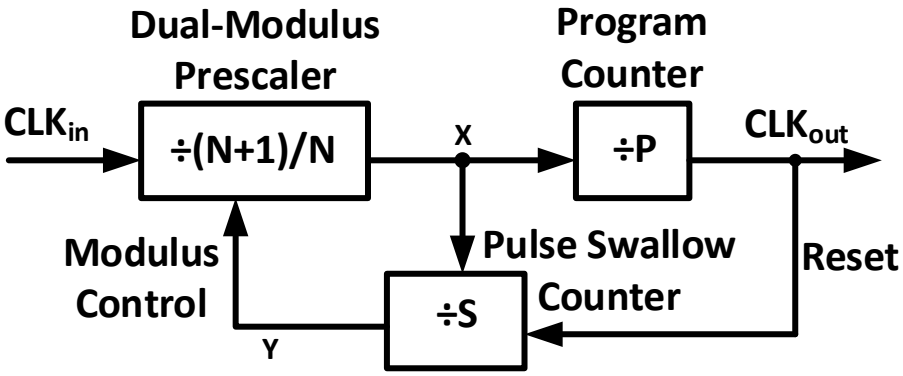


Figure 2.5: Prescaler used in Integer-N PLL

RF communication systems work with limited channel bandwidth. As previously stated, an integer-N PLL can alter the output frequency only in integer steps. To obtain narrow channel spacing, a lower reference frequency and a larger division ratio divider are needed. As the noise contribution of the divider in the loop is $20 \log N$, where N is the division number, it increases the divider's noise contribution to the loop which is undesirable.

Lowering the reference frequency leads to much lower loop bandwidth ($1/10^{th}$ of reference clock) which is not suitable for noisy VCO as loop filter will pass most of it's noise to PLL's output. Very low value of bandwidth can even increase the settling time of the PLL due to slow response of the loop. Therefore, Integer-N PLLs are mostly used in applications with very wide channel bandwidth[18–21].

2.2.2 Fractional-N PLL

Fractional-N frequency synthesizer consists of a fractional feedback divider in loop and therefore able to generate frequencies apart by a fraction of reference frequency[22–24]. Fractional divider is implemented by incorporating N/N+1 dual modulus prescaler and switching the division ration between N and N+1 for specific periods. Due to the divider's fractional division factor, there are no limits on the reference frequency in this situation, and it benefits from a higher loop bandwidth for faster settling and improved VCO noise suppression [25].

The following equation describes the relationship between Reference (f_{Ref}) and output frequency (f_{VCO}) of a fractional-N PLL -

$$f_{VCO} = f_{Ref}\left(N + \frac{K}{F}\right) \tag{2.21}$$

where N, K, F all are integer numbers with conditions $\frac{K}{F} < 1$ and $N < F$.

The fractional divider's implementation differs from the implementation of integer divider. In a multi-modulus frequency divider, prescaler's division mode is controlled by additional digital circuitry in the fractional divider to obtain the desired fractional division number. Fractional division is accomplished by averaging the N and N+1 division over a number of cycles and therefore fractional-N PLL experiences systematic spurious tones which are present at harmonics of reference frequency. In order to reduce the amplitude of these tones, a delta-sigma modulator is incorporated to introduce randomness at the cost of additional non-idealities into the system and an additional power dissipation. [18, 26–29].

2.3 Building Blocks and Impairments of CPPLL

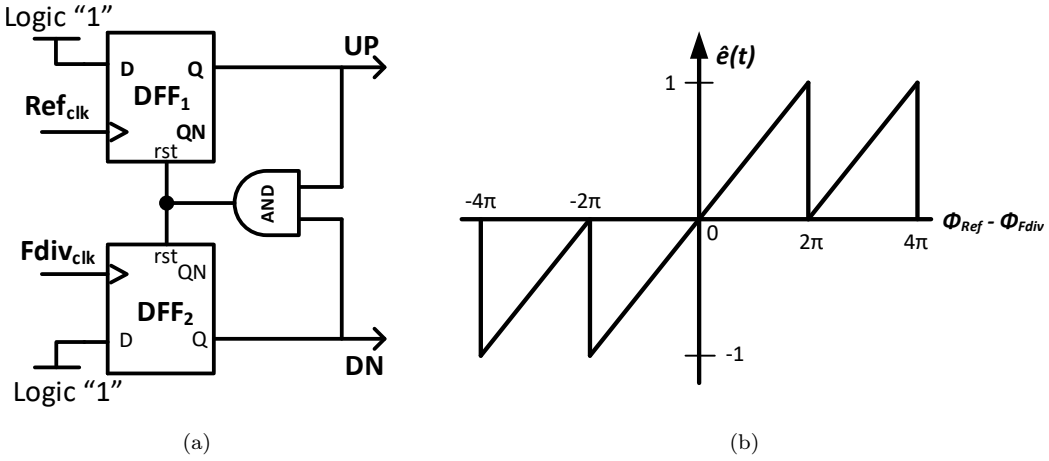
Each component of a Charge pump PLL is discussed in this section along with their non-idealities.

2.3.1 Phase Frequency Detector

A phase and frequency detector (PFD) is used to track the phase and frequency difference of its inputs. A standard tri-state PFD generates two signals, "UP" and "DN" based on the phase difference between reference clock and feedback clock as shown in Figure 2.3. A generic D flip flop (DFF) based tri-state phase frequency detector is shown in Figure 2.6 (a). One DFF takes reference input (Ref_{clk}) as clock signal and other takes frequency divider's output ($Fdiv_{clk}$) while keeping input terminals of both flops in active high state. Phase difference between UP and DN is proportional to phase difference between Ref_{clk} and $Fdiv_{clk}$. When UP signal becomes "1", charge pump works as a current source and charges the loop capacitor whereas when DN becomes "1", charge pump works as a current sink and discharges the loop capacitor. When both UP and DN signals are "1", it resets the D flip flops and switches UP and DN signals back to "0".

Figure 2.6 (b) shows the relationship between input and output phase difference of PFD. It can be seen that average error $e(\bar{t})$ of the output phase difference "$UP - DN$" is linear to input phase

difference "$\phi_{Ref} - \phi_{Fdiv}$" from -2π to $+2\pi$. Right half plane of Figure 2.6 (b) displays the case when Ref_{clk} leads $Fdiv_{clk}$ and therefore the difference "$\phi_{Ref} - \phi_{Fdiv}$" comes out to be positive. Similarly left half plane of Figure 2.6 (b) demonstrates the scenario when $Fdiv_{clk}$ leads Ref_{clk}k.



(a) (b)

Figure 2.6: (a) Tri-state PFD (b) Gain of PFD

A tri-state PFD has two significant drawbacks, "dead zone" and "blind zone" [30, 31]. Figure 2.7 depicts the dead-zone problem. When the phase difference between Ref_{clk} and $Fdiv_{clk}$ is almost zero, both UP and DN pulses remains "1" for very short duration. When this time duration is not sufficient to turn on the charge pump switches, it results in zero output current from charge pump to loop filter. During this time there is no relation between input and output. PFD becomes a non linear circuit which detects incorrect phase difference and introduces more jitter to PLL system [32].

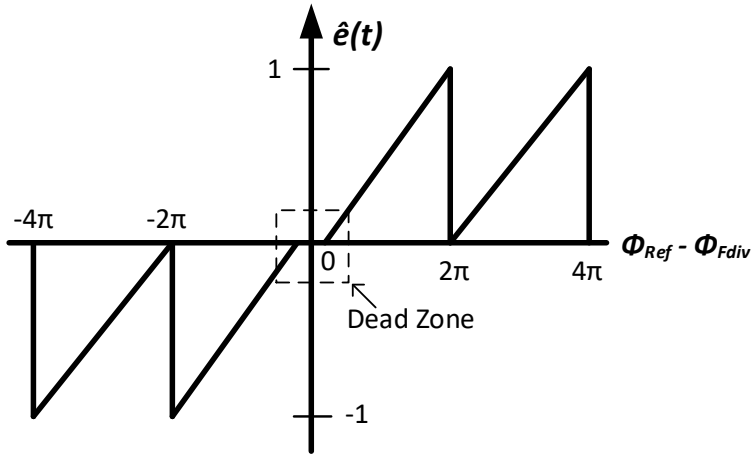
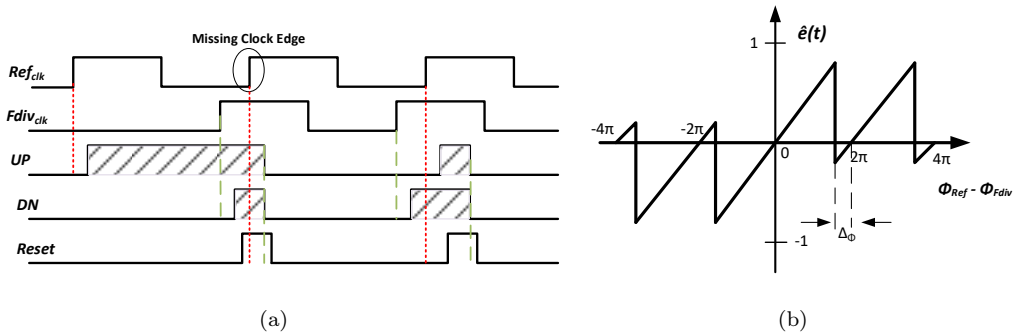


Figure 2.7: Dead-zone in tri-state PFD

In blind zone issue, leading phase is not detected when phase difference between reference clock and feedback clock is close to 2π. It can be seen in Figure 2.8 (a) that second rising edge of the leading signal Ref_{clk} is falling in reset region and therefore missed by the PFD which then does



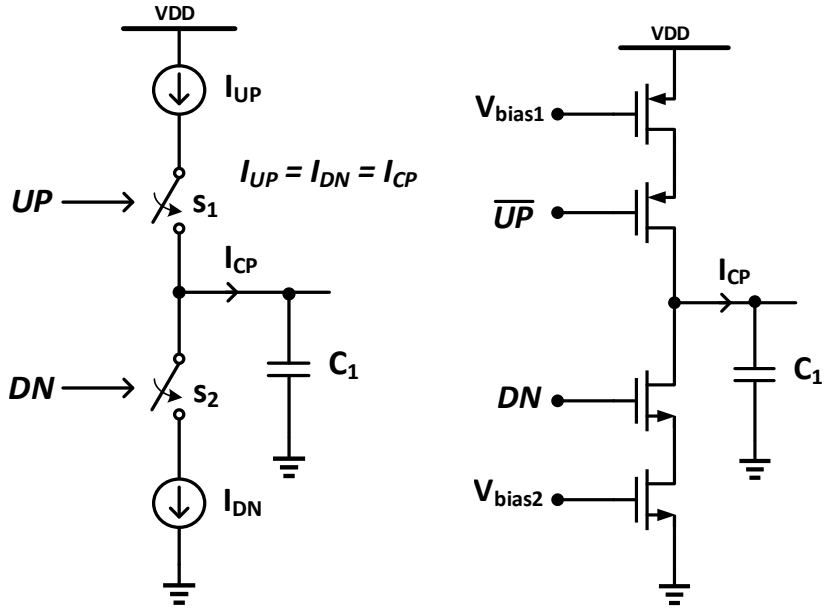
(a) (b)

Figure 2.8: (a) Rising edge of Ref_{clk} being missed by PFD (b) blindzone in a PFD

not report correct phase difference. It reduces the linear operating range of the PFD lesser than 4π as shown in Figure 2.8 (b).

There is a substantial amount of literature available on the main PFD architectures, including NAND based PFD, precharge-type PFD and latch based PFD [33–35]. The latch-based PFD is often used for its high operating speed with low power dissipation and wide input range. Additionally, the literature reports several designs of a dead zone-free PLL with low phase noise and fast locking capabilities [36–38].

2.3.2 Charge Pump



(a) (b)

Figure 2.9: (a) Basic concept of a charge pump (b) Transistor level implementation

Figure 2.9 (a) and (b) shows the basic concept of charge pump and its transistors level realization, respectively [39, 40]. Charge pump serves as both a current source and a sink for the loop filter. When UP is "1", it turns ON switch S_1 and charges the capacitor C_1 which builds the

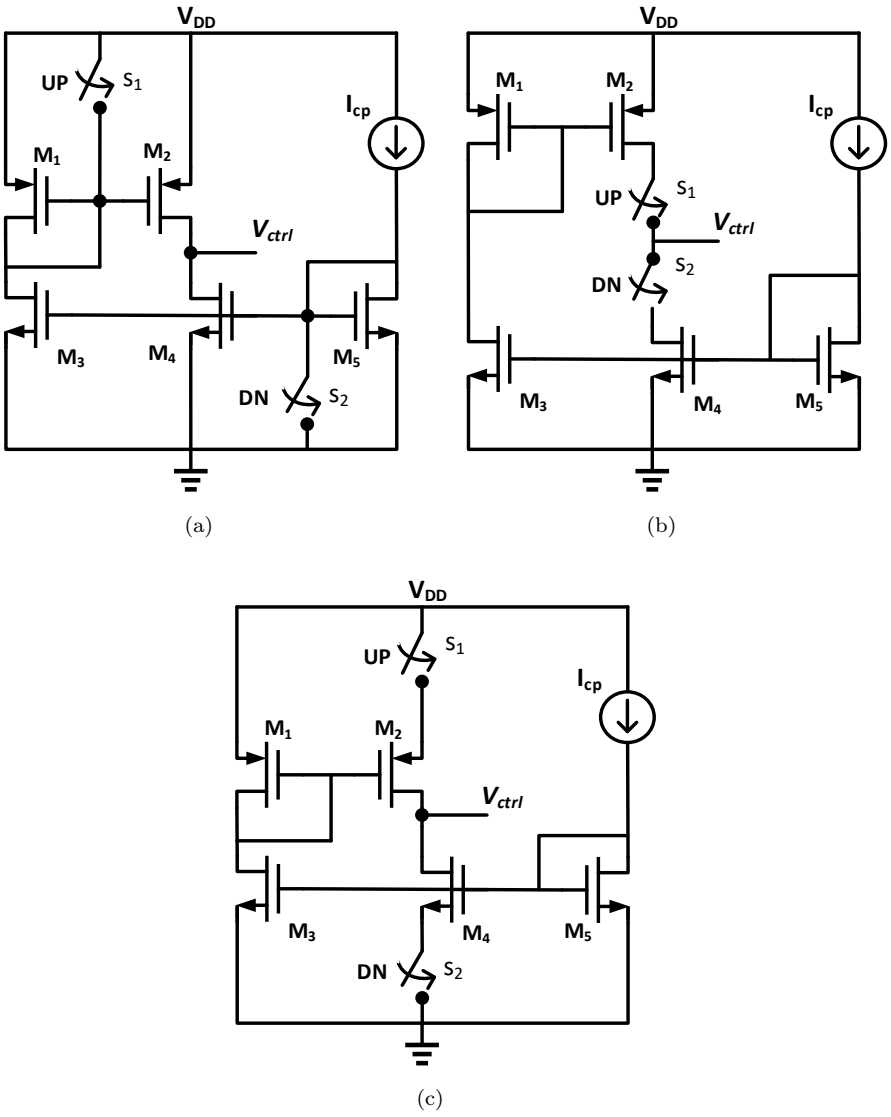


Figure 2.10: (a) Gate-switched charge pump (b) Drain-switched charge pump (c) Source-switched charge pump

voltage at node V_{ctrl}. Similarly, when DN becomes "1", it turns ON the switch S_2 and discharges C_1. Charging current I_1 and discharging current I_2 are equal. There are several charge pump circuit topologies depending on where switches are placed in the pull-up and pull-down networks, as shown in Figure 2.10.

Figure 2.10 (a) shows the gate switched architecture of the charge pump where switches are placed at gate of current source transistors M_2 and M_4. When UP goes to logic "1", transistor M_2 is turned OFF and when DN goes to "1", transistor M_4 is turned OFF. Major issue with gates switched CP is leakage current. Since both the switches are implemented using transistors, both have finite off-resistance which enables the flow of leakage current through these two switches due to their operation in sub-threshold region. Solution to this problem is to minimize the charge pump current I_{cp} but it increases the switching time as transconductance of biasing transistors M_1 and M_5 decreases with reduction in current value. Charge sharing is one more issue with

this architecture which takes place among drain capacitance of transistor M_2, M_4 and loop filter's capacitance.

Figure 2.10 (b) shows the drain switched architecture of charge pump where switches are placed at the drain of current source transistors M_2 and M_4. This architecture also suffers from charge sharing issue as drain terminal of switches is tied to loop capacitor and source is tied to bigger capacitance of current source transistors.

Figure 2.10 (c) shows the source switched charge pump architecture where switches are placed at source terminal of the current source transistors M_2 and M_4. Advantage of this architecture is that I_{cp} current can be minimized without affecting the switching time of the switches since both biasing transistors M_3 and M_5 are not connected to them.

However, due to utilization of different device types in the implementation of pull-up and pull-down network, all the above discussed architectures still suffer from current mismatch problem. This mismatch between pull-up and pull-down network causes periodic glitches, called reference spurs. These periodic glitches are reference frequency apart from each other and introduces static phase offset and dynamic jitter into the PLL loop. Amplitude of these reference spurs S_r can be expressed as follows [41]:

$$S_r = 20log\left(\frac{I_{cp}\phi_e R_1 K_{VCO}}{\sqrt{2}\pi f_{Ref}}\right) - 20log\frac{f_{Ref}}{f_{LPF}}(dBc) \tag{2.22}$$

where I_{cp} is the charge pump current, ϕ_e is the phase offset, R_1 is the resistor in the loop filter, f_{Ref} is the reference frequency and f_{LPF} is the pole frequency of loop filter.

2.3.3 Loop Filter

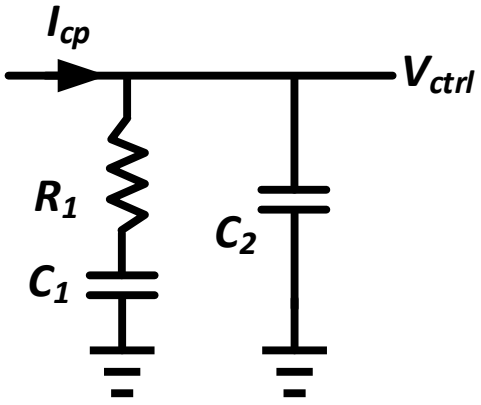


Figure 2.11: Second order passive loop filter

Loop filter in PLL determines the stability of the system. Loop filters are classified into two categories, passive and active filters. Because of noise and complexity, passive filters are preferred over active filter in PLLs.

Figure 2.11 depicts the typical second order loop filter with one resistance and two capacitance.

It derived before, the first branch with resistance R_1 and capacitance C_1 introduces one zero located at $1/R_1C_1$ before unity gain bandwidth for stability. Due to charging and discharging current, resistance introduces sudden jumps in the control voltage. Second branch incorporates capacitance C_2 that compensates these sudden jumps which helps to suppress spikes in control voltage. This C_2 also creates one pole which makes PLL a third order system and can cause instability as well. Therefore, recommended value of C_2 is around $1/10^{th}$ of C_1 to maintain stability of the feedback system while designing analog PLL [7]. Since phase margin governs the stability of feedback, it is advised to keep it beyond 45° [17]. Bandwidth plays major role when it comes to the phase noise or jitter requirements. While a lower bandwidth PLL takes longer to settle but has fewer reference spurs and better VCO noise suppression, a higher loop bandwidth PLL has better VCO noise suppression, lower settling time but higher reference spurs.

2.3.4 Voltage Controlled Oscillator

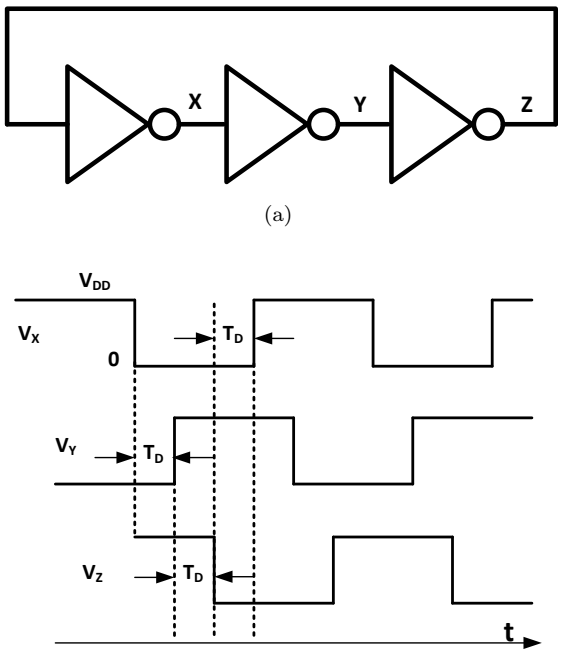


Figure 2.12: (a) Ring oscillator with three inverter stages (b) Working principle of three stage ring oscillator

Oscillators are the key element for clock generation circuits. According to "Barkhausen criteria" [40], any negative feedback system needs to satisfy the following two conditions to oscillate -

- Open loop gain should be greater than 1.
- Total phase shift around the loop should be equal to 360°.

To ensure the oscillation across PVT corners, open loop gain is chosen to be twice or thrice of the required value [40].

In a PLL, control voltage generated by loop filter determines the output frequency of the oscillator. Relation between input control voltage and output oscillation frequency of the VCO can be written as follows -

$$f_{VCO} = f_o + K_{VCO}V_{ctrl} \tag{2.23}$$

where f_{VCO} represents the output frequency, f_o represents the free running oscillation frequency, K_{VCO} represents the gain and V_{ctrl} represents the input control voltage of the VCO.

Mostly two main architectures are common for VCO, ring-type and LC-type. Ring oscillators are very compact, easy to integrate and consume lesser area on chip whereas LC tank based oscillators occupy large area, and not easy to integrate. In case of stringent requirement on phase noise, LC type oscillators are preferred over Ring oscillators due to their better phase noise performance than the ring oscillator [42–45]. Figure 2.12 (a) shows the ring oscillator architecture using three inverter stages. Oscillation builds up with time due to available noise at internal nodes. Figure 2.12 (b) shows that timing waveform of each inverter stage. When one internal node is assumed to have voltage level of V_{DD}, oscillation frequency of the VCO f_{VCO} comes to be $1/6T_D$ where T_D is the delay of one inverter. Therefore, oscillation frequency of a N-stage ring oscillator can be written as

$$f_{VCO} = 1/NT_D \tag{2.24}$$

One of the most commonly used architectures of ring oscillator for a PLL loop is Current Starved Voltage Controlled Oscillator (CSVCO) which is shown in Figure 2.13. Chain of inverters is placed between diode connected PMOS and NMOS transistors which steer the current flow through inverters. Input control voltage V_{ctrl} determines the mount of current mirrored into diode connected transistors which decides the oscillation frequency of the VCO.

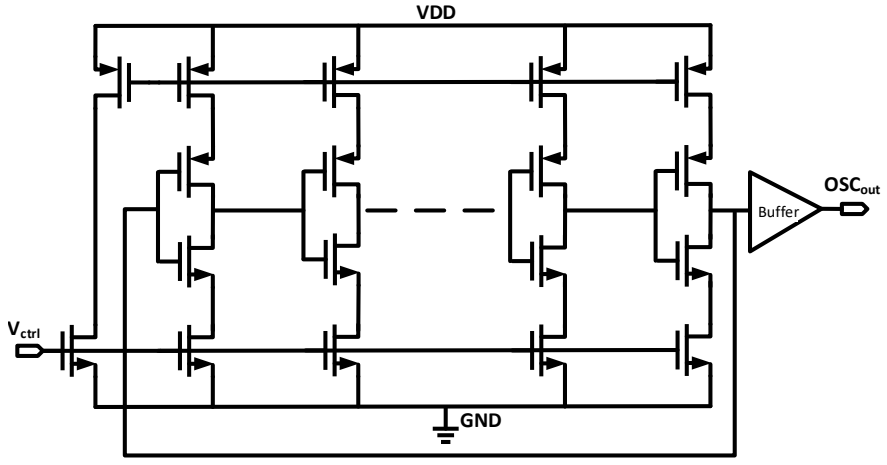


Figure 2.13: Basic architecture of Current Starved VCO

2.3.5 Frequency Divider

Another important element of the synthesizers is the frequency divider, which also operates at the VCO's output frequency. It takes input from VCO and makes it comparable with reference frequency so that PFD can generate error signal based on their phase difference. Key attributes of a frequency divider are higher operating frequency, power consumption, required range of division ratios and amplitude of the input signal or sensitivity.

Mostly two architectures are extensively used for frequency dividers, Pulse Swallow Counter based and Vaucher's 2/3 dual modulus cell based. Each of them is described as follows -

Pulse Swallow Divider

The integer divider in the integer-N PLL is constructed using the pulse swallow divider as shown in Figure 2.14. It is comprised of a program counter (P), a swallow counter (S) and a dual-modulus divider (N). P and S are down counters which are loaded with a number at a certain moment and starts counting down by one step with each input cycle.

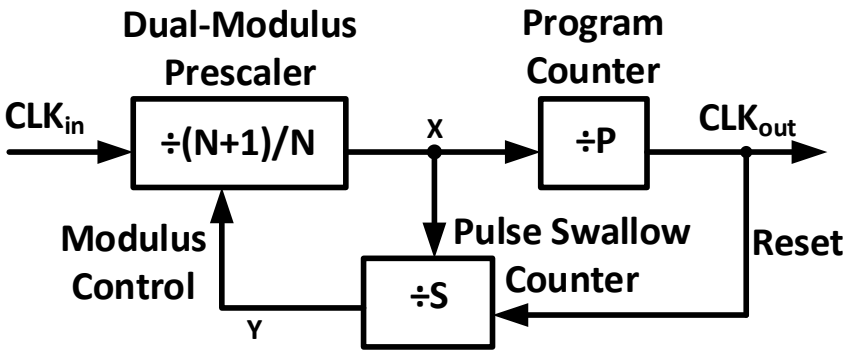


Figure 2.14: Block diagram of Pulse Swallow Divider

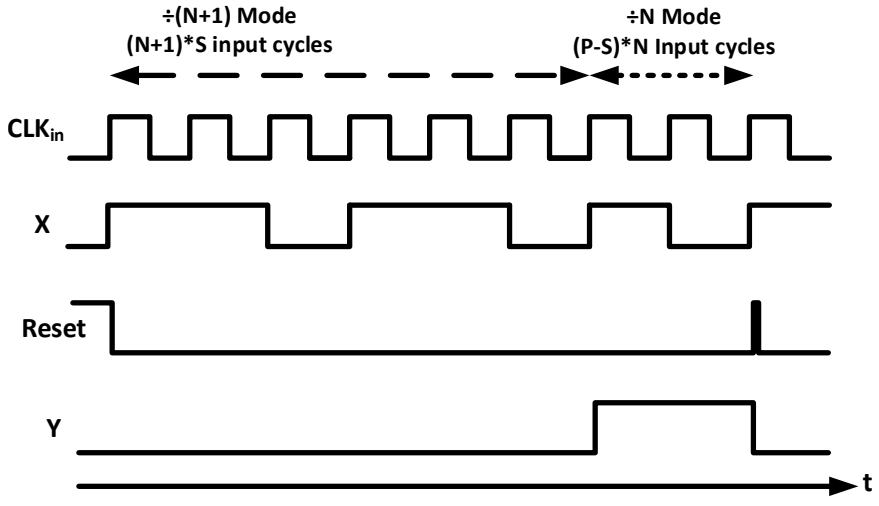


Figure 2.15: Timing waveform of Pulse Swallow Divider

Figure 2.15 shows the timing waveform of a pulse swallow divider. It can be seen from the waveform that dual modulus prescaler works in N+1 mode for S counts and changes to N for P-S counts. Thus, the total division value becomes $NP + S$. by keeping product NP constant, S can be changed to achieve required channel spacing at the output of the frequency synthesizer.

Vaucher's 2/3 Prescaler based Divider

An alternative of Pulse Swallow Counter based divider was invented by Vaucher [46]. This type of divider contains cascade connection of 2/3 prescaler to achieve programmable division ratios as shown in Figure 2.16.

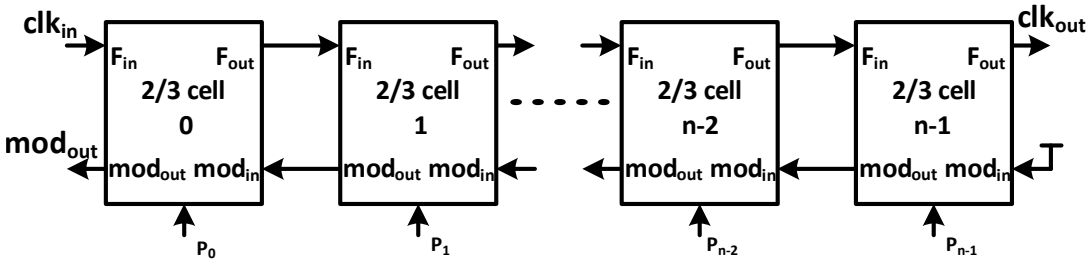


Figure 2.16: 2/3 prescaler based programmable divider

Architecture of the Vaucher's prescaler is shown in Figure 2.17 and detailed discussion of this architecture is given in chapter 4.

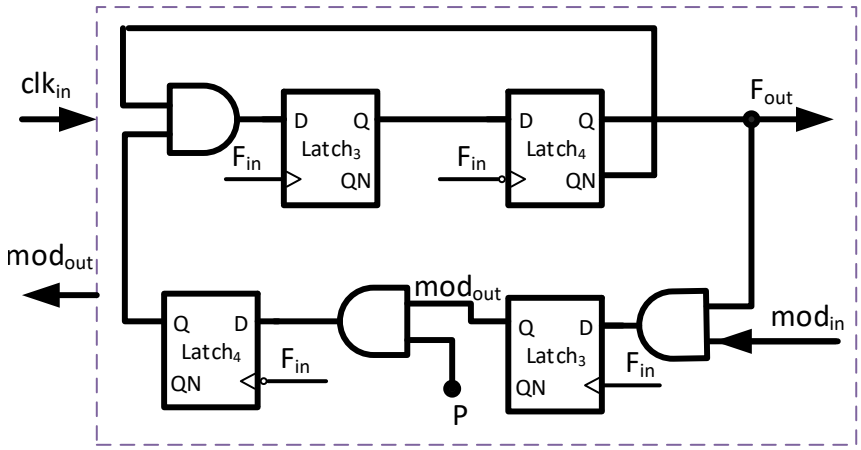


Figure 2.17: Architecture of Vaucher's 2/3 dual modulus prescaler

Implementation of high speed frequency dividers require high speed flops and logic gates. Dynamic logic cells are faster than static due to their precharge and hold mechanism. True single phase clocking (TSPC) and Extended True Single Phase Clocking (E-TSPC) are popular architectures for dynamic logic implementation.

A transistor level schematic of basic TSPC DFF is shown in Figure 2.18 (a). Operation of this DFF is as follows: when clk is "0", first branch passes complement of the input D to node A, node B is in precharge mode and therefore isolates input from node QN. When clk goes to logic "1",

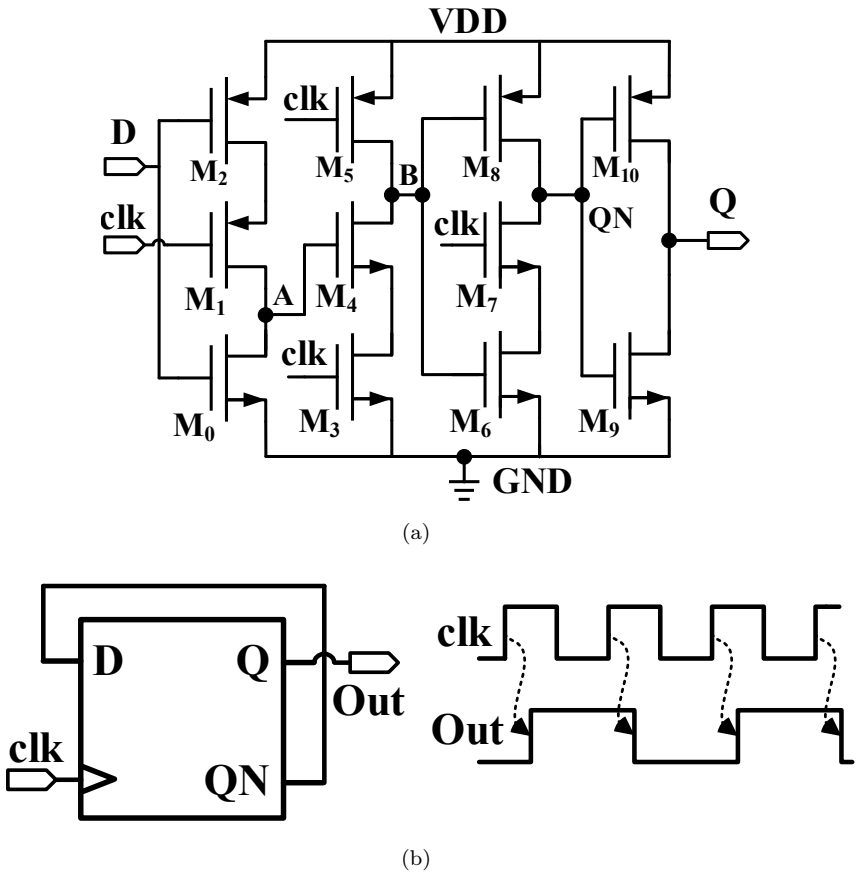


Figure 2.18: (a) TSPC flip flop (b) Divide-by-2 operation

node B falls to "0" if A is "1" otherwise holds the logic "1" and third branch becomes transparent by passing complement of D to QN. Thus TSPC DFF is in precharge state when clk is "0" and in evaluation state when clk is "1". The basic operating principle of DFF based frequency divider is shown in Figure 2.18 (b). With every rising clock edge, DFF toggles its output signal, performing divide-by-2 operation on input clock.

It becomes crucial to talk about the many performance parameters that drive the various PLLs for the various application-specific requirements after discussing each component of PLL. Therefore, a few essential PLL performance indicators are presented in the next section.

2.4 Performance Matrix of Frequency Synthesizers

Major performance indices of a frequency synthesizer are as follows-

2.4.1 Phase Noise and Jitter

The most critical factor for clock generation circuits remains spectral purity which is defined as phase noise in a synthesizer and VCO is the most significant phase noise contributor in the loop. Power Spectral Density (PSD) of an oscillator is shown in Figure 2.19 where signal noise follows the Gaussian distribution. Here, phase noise is described as the noise to signal amplitude ratio at

an offset frequency f_m in a bandwidth of 1 Hz.

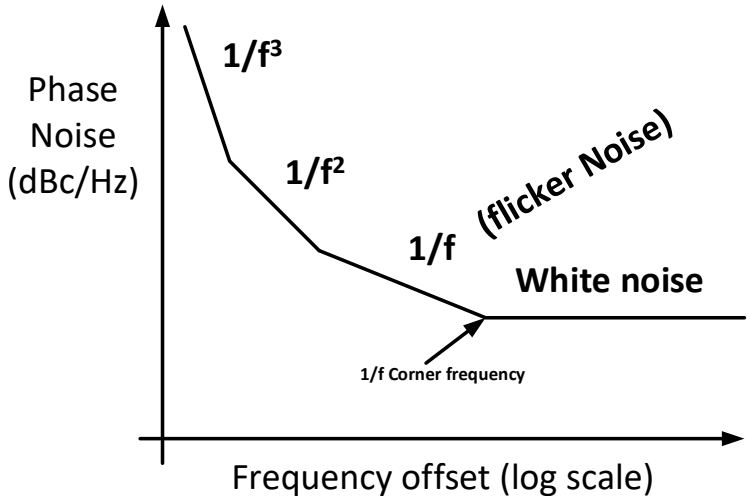


Figure 2.19: Oscillator's phase noise

Generally, oscillator's performance is defined by Single Side Band (SSB) phase noise in dBc/Hz and plotted as a function of frequency offset as shown in Figure 2.19. Curvature of the phase noise follows different regions which indicates different major noise contributors in that frequency range. Constant noise floor in the above figure shows the dominance of thermal noise whereas 1/f region shows the flicker noise dominance with 20 dB/decade slope.

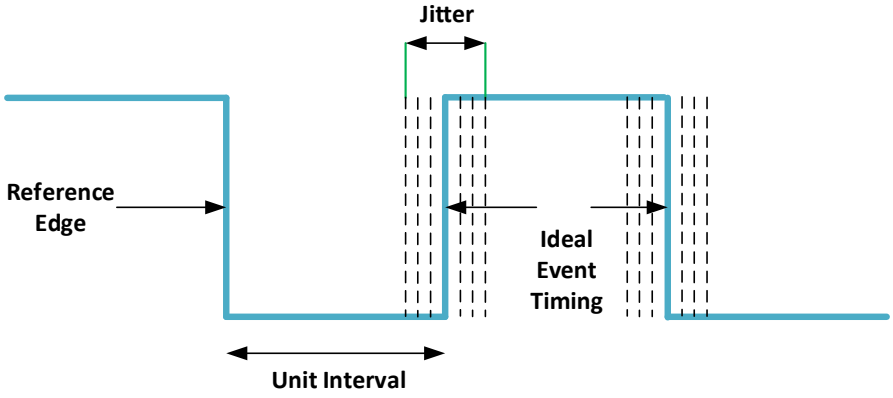


Figure 2.20: Deviation of a clock signal from its ideal position

Similar to phase noise in frequency domain, noise in time domain is called Jitter which is uncertainty in arrival of clock edge from it's ideal position as shown in Figure 2.20. Since jitter is deviation of an clock edge from it's ideal position, it's defined in terms of variance σ^2.

Jitter is broadly classified into two types, random jitter and deterministic jitter. Random jitter follows the Gaussian process which sometimes referred as intrinsic noise. Since random jitter is unbound and intrinsic, it is hard to diagnose. On the other hand, deterministic jitter is not random and has specific cause attached to it. For example, noise coming from power supply which is periodic in nature can be classified as deterministic jitter.

2.4.2 Reference Spurs

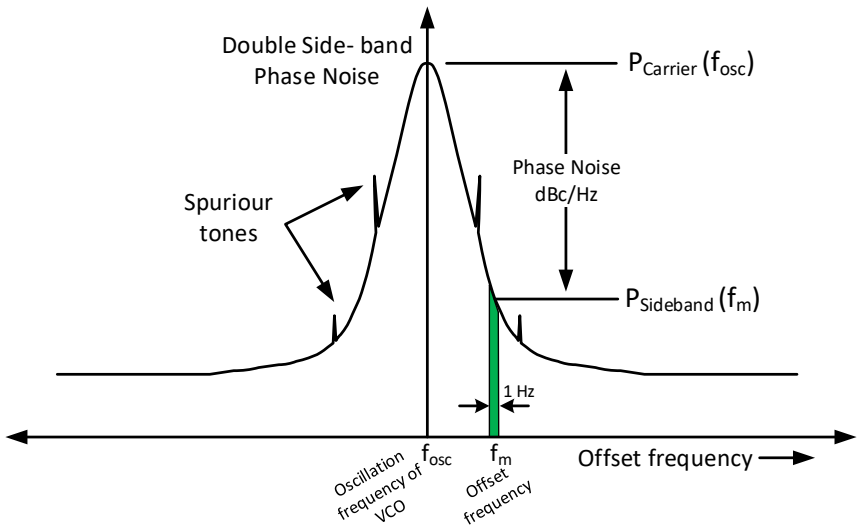


Figure 2.21: Presence of reference spurs in phase noise of PLL

In addition to the phase noise, PLL has to deal with reference spurs also. These spurs are mainly caused by non-idealities of PFD and charge pump such as PFD delay, charge pump switching delay, charge pump current mismatch, charge sharing etc [47]. Periodic ripples are generated on VCO control voltage due to these non-idealities. VCO modulates these ripple voltages and generates spurs at offset frequencies which are multiple of reference frequencies as shown in Figure 2.21. Periodicity of spur depends on PFD and charge pump behaviour whereas its magnitude is dependent on VCO and loop filter characteristics.

2.4.3 Bandwidth and Stability

Bandwidth is one of the crucial parameter while designing a PLL. Loop filter components decide the poles and zeros location of PLL loop and therefore controls the stability of the loop. A low pass filter is used in PLL which controls the noise passing through it and therefore have an affect on the settling time of the PLL. Lower loop bandwidth results in slow tracking of reference which results in higher settling time but is beneficial for lower reference spurs. Integer-N PLL suffers from very low bandwidth issue due to Gardner's stability criteria where bandwidth needs to be $1/10^{th}$ of reference frequency for loop's stability [8].

Being a negative feedback system, stability of PLL is measured from gain margin and phase margin through linear model. Location of zero and poles are affected by parasitics of the other PLL components as well which can reduce the phase margin drastically and drive the loop towards instability. Therefore, stability of a synthesizer needs to be checked for all conditions when designing a PLL based frequency synthesizer.

Chapter 3

Low Power Dual Modulus Prescaler

For frequency synthesizers for low power applications like the Internet of Things, power consumption is one of the most important factors. Frequency divider, which receives its input straight from the oscillator becomes the second-highest power-consuming block in any PLL after the Voltage Controlled Oscillator (VCO). This chapter introduces a dual modulus prescaler topology for low power frequency synthesis applications and briefly discusses the principles of frequency dividers.

3.1 Introduction

The frequency synthesizer with a dual modulus prescaler is one of the critical blocks in a communication system [48, 49]. Apart from the VCO, prescaler is the highest power consuming block of the frequency synthesizer. Thus the frequency prescaler needs careful design considerations for a robust frequency synthesizer [50–53]. The main design criteria for a frequency prescaler are speed, power consumption, and the required division ratios [52]. The following sections illustrates the existing frequency divider architectures.

3.2 State-of-the-art Prescalers

First stage of frequency divider takes input as VCO clock to divider down its frequency so that PFD can compare its phase and frequency with the reference signal as discussed in the previous chapter. It implies that first stage of the divider has to operate at highest operating frequency of synthesizer which leads to the design of prescalers. Any frequency divider in PLL loop consists of two stages, a synchronous prescaler and an asynchronous static counter. Most dual modulus prescalers are used as first stage of frequency dividers which are discussed in the next section.

3.2.1 Dual Modulus Prescaler

The two widely utilized basic dual-modulus TSPC prescalers are divide-by-2/3 and divide-by-4/5 prescaler. Mostly, due to its speed and power efficiency, divide-by-2/3 prescaler is preferred over

divide-by-4/5 to design lower division ratio prescalers such as divide-by-8/9. Figure 3.1 shows the conceptual design of a basic 2/3 dual modulus prescaler. It employs two DFFs for extending division from 2 to 3. When Mode Control (MC) is "1", node D/3 always remains "1". This behaviour makes the topology act as a toggle flip flop or a divide-by-2 circuit. When MC is "0", low phase of the $D2_{out}$ is extended for one clock cycle which in turn extends clk_{out} and therefore it function as divide-by-3 as shown in Figure 3.2.

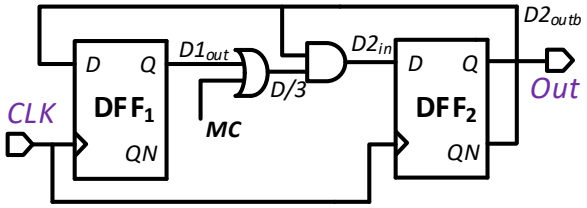


Figure 3.1: Block diagram of a conventional synchronous 2/3 prescaler

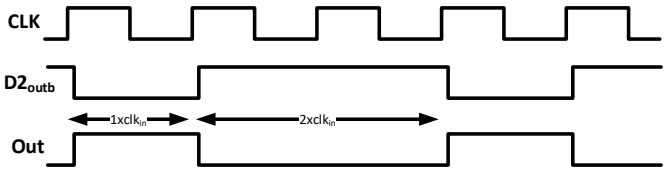


Figure 3.2: Divide-by-3 operation of 2/3 prescaler

Several architectures are available for 2/3 dual modulus prescaler including static logic dividers, Injection-Locked Frequency Dividers (ILFD) [54, 55], Current Mode Logic (CML) [56], and dynamic logic dividers which include True Single-Phase Clock (TSPC) logic [57], and Extended TSPC (E-TSPC) logic [53], [58]. Although ILFD can achieve high speed with lesser power consumption, narrow locking range limits it's utilization. CML can operate at higher frequencies for wide band applications, it suffers from high power consumption and dependence on advanced processes [59]. The state of the art CMOS N/N+1 prescalers based on TSPC and E-TSPC are preferred owing to their lower power consumption, single clock phase, small silicon area, and ease of implementation [53, 57–60].

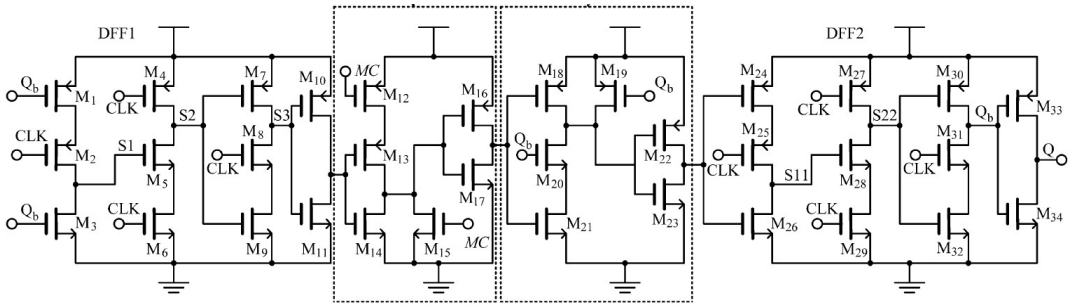


Figure 3.3: Gate level schematic of conventional 2/3 prescaler

Figure 3.3 shows the TSPC logic based gate level schematic of conventional 2/3 prescaler. External logic gates, OR and AND are placed between DFF1 and DFF2. When MC is "1",

transistor M15 is always ON and keeps output of OR gates always “1" and makes one input of AND gate “1", functioning as divide-by-2 circuit. When MC is “0", Transistor M12 is always ON therefore charges source of transistor M13 to “1". When $D2_{outb}$ becomes 1 but $D1_{out}$ is still “0" for one cycle, output also remains “0" for one extra CLK cycle, performing divide-by-3 operation as shown in Figure 3.2. There have been many recent developments on dual modulus prescaler trying to reduce the delay in critical timing path and increase operating frequency while keeping design low power.

One of such work is presented in [49] where a 2/3 prescaler is proposed using TSPC logic. This prescaler is realized using two DFFs and two NOR gates as shown in Figure 3.4. One NOR gate is embedded in last stage of DFF1 whereas second in first stage of DFF2.

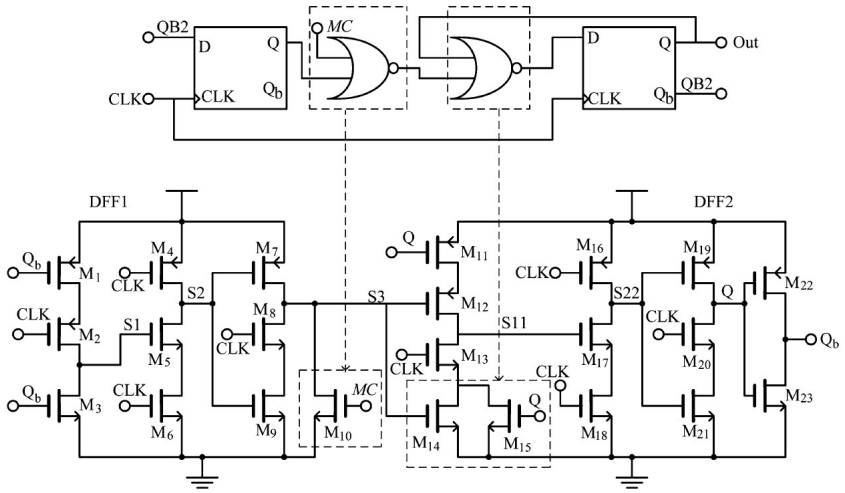


Figure 3.4: Gate level schematic of 2/3 prescaler proposed in [49]

Similar to TSPC, Figure 3.5 shows the schematic of 2/3 prescaler proposed in [61] using E-TSPC logic. Each stage has only two MOSFETs due to which switching speed of internal nodes increases. Absence of stacked devices and faster switching speed make this type of architecture more suitable for high speed applications. In addition, other advantage of this architecture is that AND and OR logic gates are embedded in the first stage of the flops by adding only one transistor in each flop.

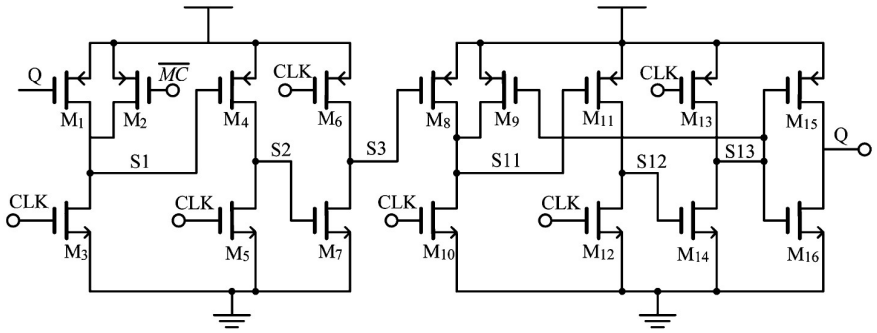


Figure 3.5: Gate level schematic of 2/3 prescaler proposed in [61]

As shown in above figures, E-TSPC prescalers are similar to TSPC circuit but have one less transistor in each branch. Although E-TSPC prescaler has the merit of higher operating frequency compared to TSPC prescalers, the higher power consumption reduces their applicability in low power Phase-Locked-Loop (PLL) frequency synthesizers [62]. Moreover, E-TSPC prescalers need larger amplitude for the clock signal unlike TSPC based prescalers. Consequently, the TSPC based dual/multi-modulus prescalers is preferred in power conscious PLL applications [53, 59, 60].

There are two major sources of power consumption, namely short-circuit power and switching power [60]. In 2/3 precalers, TSPC consumes higher switching power due to higher loading, but due to much higher short circuit power consumed by E-TSPC, TSPC shows lesser overall power consumption which makes them a suitable choice for low power prescalers [49, 60]. Previous work has already highlighted that in dual modulus prescalers the first stage which is operating at highest frequency is the main bottleneck in realizing a low power frequency synthesizer. Much efforts have been devoted to reduce the power consumption of the first stage of frequency dividers. In addition, previous studies [49–53] have underlined various architectural modifications to further improve the speed and power consumption. However, these modifications have led to increase in minimum operating frequency of the prescaler.

Hence, all the above discussion shows a need of low power dual modulus prescaler. This chapter discusses such topology of low power 8/9 dual modulus prescaler. It consists of a synchronous 2/3 divider followed by an asynchronous divide-by-4 unit. Through an in-depth analysis and design optimization we propose a novel ultra-low power divide-by-2/3 prescaler with improved power efficiency. By utilizing the proposed technique, the maximum speed of the prescaler is increased by 40% comparing with conventional 2/3 prescalers reported in [49, 63]. Results show that the proposed novel 2/3 prescaler adopted in the divide-by-8/9 prescaler can operate from 2 MHz to 5.5 GHz frequency range. Before proceeding for the proposed 8/9 prescaler, next section discussed the conventional architecture of the divide-by-8/9 prescaler first.

3.3 Conventional Divide-by-8/9 Prescaler

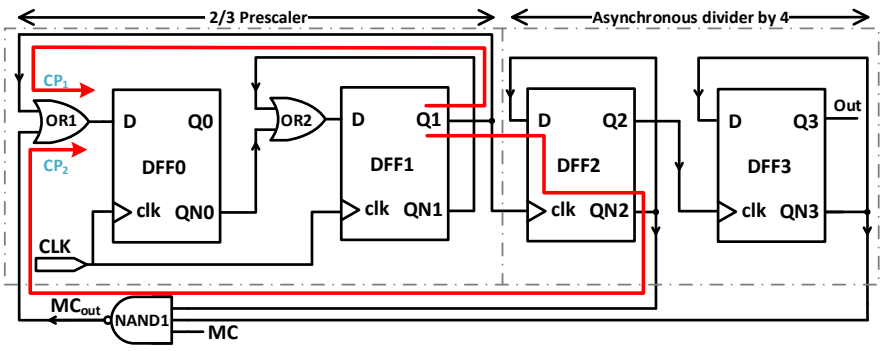


Figure 3.6: Block diagram of the conventional 8/9 prescaler

3.3.1 Architecture and Operating Principle

Figure 3.6 shows the conventional divide-by-8/9 prescaler which consists of four DFFs, one NAND gate and two OR gates. The division ratio of the prescaler is controlled by Modulus Control (MC) signal. When MC is "0", the prescaler operates in divide-by-8 mode whereas divider performs divide-by-9 operation when MC is "1" .

3.3.2 Propagation Delay

Typically, maximum operating frequency of any digital logic is restricted by its critical timing path. For example, CP_1 and CP_2 represents the two critical paths of the prescaler as shown in Figure 3.6. CP_1 contains the propagation delay of one CLK-to-Q of DFF1 and one OR gate (OR1) whereas CP_2 contains propagation delay of CLK-to-Q of DFF1, CLK-to-QN of DFF2, NAND1 and OR1. Therefore, delay of both critical paths can be written as follows

$$T_{d,CP_1} = t_{CLK-Q,DFF1} + t_{OR1} + t_{set,DFF0} \tag{3.1}$$

$$T_{d,CP_2} = t_{clk-Q,DFF1} + t_{clk-QN,DFF2} + t_{OR1} + t_{NAND1} + t_{set,DFF0} \tag{3.2}$$

where $t_{CLK-Q,DFF1}$ and $t_{CLK-QN,DFF2}$ represents propagation delay of DFF1 and DFF2. t_{NAND1}, t_{OR1} and $t_{set,DFF0}$ represents propagation delay of NAND1 ,OR1 and setup time of DFF0, respectively. If the propagation delay of each logic gate and flop is considered identical and optimized routing is done in layout, it can be assumed that CP_1 has shorter timing path as compared to CP_2. Therefore, the only remaining critical path in the design will be CP_2. By further layout optimization to reduce parasitics, the maximum operating frequency of the 8/9 prescaler can be increased.

3.3.3 Power Consumption

It is clear from (3.2) that in order to reduce the critical path, propagation delay of DFFs need to be optimized which can not be resolved beyond the limits of given CMOS technology. Power consumption also becomes a major concern for higher operating frequency as TSPC designs suffer mainly from switching power [61] and therefore it becomes a challenge for designers to optimize the design for higher frequencies while maintaining the power efficiency. From Figure 3.6, power consumption of 2/3 prescaler needs significant reduction as it operates at highest frequency. Theoretically, during divide-by-2 operation, almost 50% power can be saved by eliminating one flip-flop. As presented in [49], conventional prescaler contains total 12 switching nodes representing total switching power $P_{switch,conv-2/3}$ as

$$P_{switch,conv-2/3} = \sum_{i=1}^{12} f_{CLK} C_{Li} V_{DD}^2 \tag{3.3}$$

where f_{CLK} represents input clock frequency, C_{Li} represents load at each internal node and V_{DD} represents power supply of the circuit. From Figure 3.6, total power consumption of the 8/9 prescaler, $P_{switch,conv-8/9}$ can be given as

$$P_{switch,conv-8/9} = P_{\text{switch,DFF1}} + P_{\text{OR1}} + P_{\text{switch,DFF2}} + P_{\text{OR2}} + P_{\text{NAND1}} + P_{asy-div-4} \quad (3.4)$$

where $P_{\text{switch,DFF1}}$, $P_{\text{switch,DFF2}}$, $P_{asy-div-4}$ represents the switching power consumption of DFF1, DFF2 and asynchronous divide-by-4 unit, respectively. P_{OR1}, P_{OR2}, P_{NAND1} represents the power consumption of logic gates.

3.4 Proposed Divide-by-8/9 Prescaler

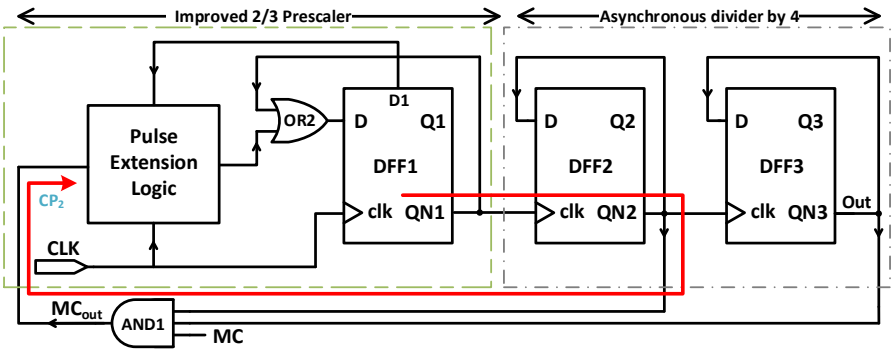


Figure 3.7: Block diagram of the proposed 8/9 prescaler

Figure 3.7 shows the block diagram of the proposed divide-by-8/9 prescaler. A new improved 2/3 dual modulus prescaler is combined with an asynchronous divide-by-4 unit to perform divide-by-8/9 operation. Compared with the conventional circuit (Figure 3.6), two main changes are adopted in the proposed 8/9 dual modulus prescaler. First, an improved 2/3 Prescaler is designed, using one D flip flop (DFF1) and Pulse Extension Logic (PEL) circuit. Second, instead of nodes Q1 and Q2, QN1 and QN2 of DFF1 and DFF2 are connected to input clock of DFF2 and DFF3, respectively [52]. Thus, the propagation delay of DFF2, and DFF3 decreases from CLK-to-Q to CLK-to-QN. As a result, critical path length is further reduced.

Figure 3.8 (a) shows a transistor-level architecture of the proposed PEL circuit. One of the input to the PEL is MC_{out} which is output of the logic gate AND1 and other input is D1 which is internal node of DFF0. The proposed circuit operates as follows. When Mode Control of PEL circuit MC_{PEL} is ”0”, transistor M1 turns ON and switches node X to ”1” as soon as CLK becomes ”0”. MC_{PEL} turns OFF the transistor M5, so node X remains at logic ”1” and turns ON transistor M8. As soon as CLK becomes "1", OUT is charged to logic ”1”. When MC_{PEL} is ”1”, transistor M5 turns ON, node X remains at logic ”1” if IN is ”0” otherwise discharges to logic ”0”. As CLK becomes ”1”, Out will pass the complement of X. Figure 3.8 (b) depicts the timing waveform of the PEL for better understanding of the circuit. When plotting the waveform, it is assumed that

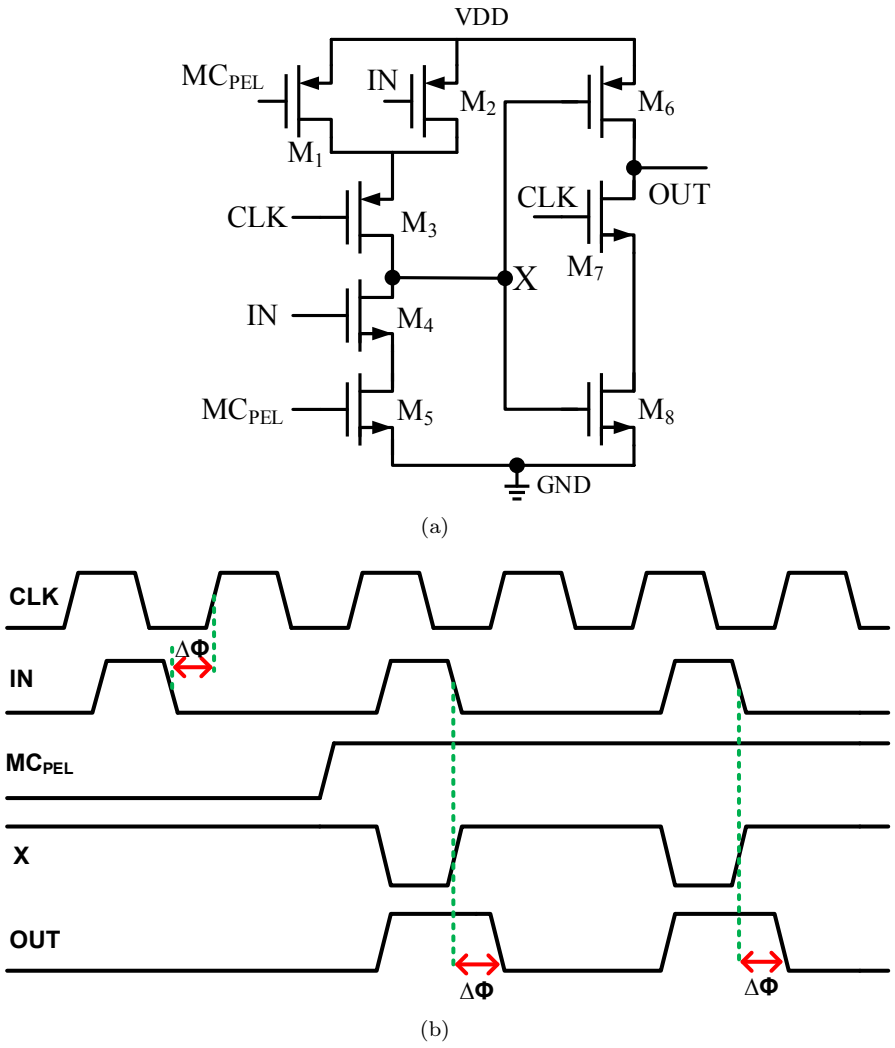


Figure 3.8: (a) Pulse Extension Logic circuit (b) Timing waveform of the Pulse Extension Logic

signal IN is driven by the frequency, $f_{CLK}/2$. It is clear from the waveform that signal IN and Out has the same period, but additional phase $\Delta\phi$ is added in the output, which is same as the phase difference between IN and CLK. This relation between IN and OUT signal has been utilized to extend the positive phase of the output signal QN1 of DFF1 for one clock cycle to perform the divide-by-3 operation.

Figure 3.9 shows the transistor-level architecture of the proposed divide-by-8/9 prescaler. In order to reduce the delay caused by external logic gates, AND1 is absorbed in the first stage of PEL circuit using NMOS transistors M6-M8 while OR1 gate is embedded in the second stage of DFF1 using a PMOS M15, whose source is connected to VDD supply and drain is connected to source of transistor M16. The branch driven by node QN is removed from each flop to further reduce power and delay.

In Figure 3.9, transistors M0-M11 forms PEL circuit and M12-M21 forms DFF1. Therefore

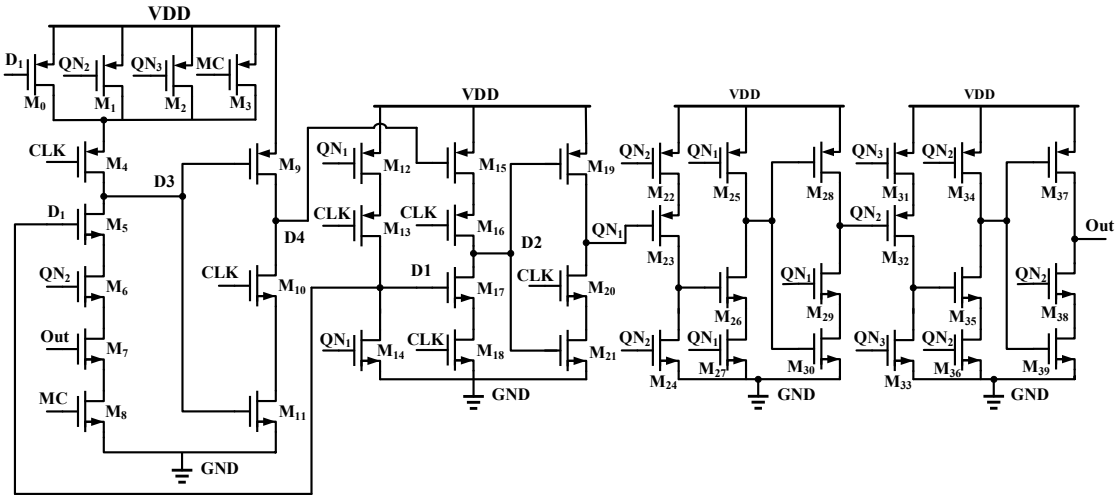


Figure 3.9: Transistor level architecture of the proposed 8/9 prescaler (L = 0.18μm)

total power consumption of the improved 2/3 prescaler consisting PEL and DFF1 is

$$P_{improved-2/3} = \sum_{i=1}^{5} f_{CLK} C_{Li} V_{DD}^2 \tag{3.5}$$

where f_{CLK} is the frequency of input clock signal, C_{Li} represents load capacitance of nodes D1, D2, QN1, D3 and D4.

Major advantage of replacing one DFF by PEL circuit in improved 2/3 prescaler is that, only DFF1 is active during divide-by-2 operation which reduces the total number of switching nodes to 3 (D1, D2, QN1). Theoretically, this can reduce total switching power by almost 74% as compared to conventional 2/3 prescaler. Even in divide-by-3 mode of operation, total number of switching nodes increases to 5 (D1, D2, D3, D4, QN1), which can still save almost 60% of total power as compared to conventional design of 2/3 prescaler.

Load capacitance at the output node of each flip-flop can be described using the method mentioned in [64]. Due to additional connection to gate terminal of transistor M5 the load capacitance at node D1 is increased by C_{gM5} as shown in Figure 3.9. The load capacitance at the output node, QN1 for the proposed 2/3 prescaler standalone unit is

$$C_{L\_improved-2/3} = C_{dbM19} + C_{dbM20} + 2C_{gdM19} + 2C_{gd20} + C_{gM12} + C_{gM14} \tag{3.6}$$

The above equation shows a very significant reduction in load capacitance of the proposed 2/3 prescaler as compared to the prescalers presented in [49]. Since the load of internal node D1 has increased, more effort is required in transistor sizing to achieve higher operating frequency. Moreover, area of the proposed 2/3 prescaler is also significantly reduced as it uses only 18 transistors (excluding M1, M2, M6, M7 which are part of AND1) as compared to the architectures shown previously [49, 60] which uses more than 20 transistors. Hence, the area and total power consumption is reduced significantly when the proposed 2/3 prescaler is used in a divide-by-8/9 prescaler.

3.4.1 Divide-by-8 Mode

In this section, divide-by-8 operation of the proposed 8/9 prescaler is discussed. When the control signal MC is "0", transistor M8 is turned-OFF and transistor M3 is turned-ON which charges node D3 to logic "1" when CLK goes to logic "0". Since transistor M8 is OFF, there is no direct path from node D3 to ground, so D3 remains at logic "1" and turns-ON transistor M11. When CLK goes to logic "1", output node D4 discharges to "0" through transistors M10-M11 and turns-ON transistor M15. Source of transistor M16 gets connected to power supply VDD through transistor M15. In this case when transistor M15 is ON, DFF1 (M12-M21) becomes identical to DFF2 (M22-M30) and DFF3 (M31-M39). So, when MC is "0", each DFF functions as divide-by-2 unit. As DFF1, DFF2 and DFF3 are connected in series, each flop operates at f_{CLK}, $f_{CLK}/2$ and $f_{CLK}/4$ respectively, as a result the output frequency f_{Out} becomes $f_{CLK}/8$.

Power Consumption

Total switching power of the proposed 8/9 prescaler during divide-by-8 mode is given by (3.7)

$$P_{Pro-div-8} = P_{\text{switch,DFF1}} + P_{\text{OR2}} + P_{\text{AND1}} + P_{asy-div-4} \tag{3.7}$$

where $P_{\text{switch,DFF1}}$ is switching power consumption of DFF1, P_{AND1}, P_{OR2} represents the power consumption of logic gates and $P_{asy-div-4}$ represents the power consumed by the asynchronous divide-by-4 unit. As there is no switching in PEL circuit when MC is "0", it's power consumption is excluded from total power.

Power consumption of DFF1 (Figure 3.9) is sum of power consumed by it's all three branches and can be written as

$$P_{switch,DFF1} = \sum_{i=1}^{3} f_{CLK} C_{Li} V_{DD}^2 \tag{3.8}$$

As the asynchronous divide-by-4 units receives QN1 as its input clock whose frequency is $f_{CLK}/2$, its power consumption can be written as

$$P_{asy-div-4} = \frac{f_{CLK} V_{DD}^2}{2} \left(\sum_{j=1}^{3} C_{Lj} + \frac{\sum_{i=k}^{3} C_{Lk}}{2} \right) \tag{3.9}$$

where $P_{asy-div-4}$ represents sum of the power consumption of DFF2 and DFF3, f_{CLK} is input frequency to the div-by-4 unit, C_{Lj} and C_{Lk} represents load at each internal node of DFF2 and DFF3, respectively.

Since each DFF is operating at different frequency, transistor sizing in the proposed 8/9 prescaler is also reduced progressively to further reduce the power consumption and therefore (3.9) uses different notations for load capacitance.

3.4.2 Divide-by-9 Mode

From (Figure 3.9), when control signal MC is "1", transistor M3 is turned-OFF and M8 is turned-ON. Until nodes D1, QN2 and Out becomes logic "1", node D3 and D4 remains at logic "1" and "0", respectively. When D1, QN2 and Out become "1", it creates direct path from D3 to ground, switches node D3 to "0" and D4 to "1". This logically high D4 turns-OFF transistor M15 for one CLK cycle, disconnecting source of transistor M16 from power supply and forces node D2 to hold its previous value. As can be seen from timing diagram in Figure 3.10 that whenever D3 goes to

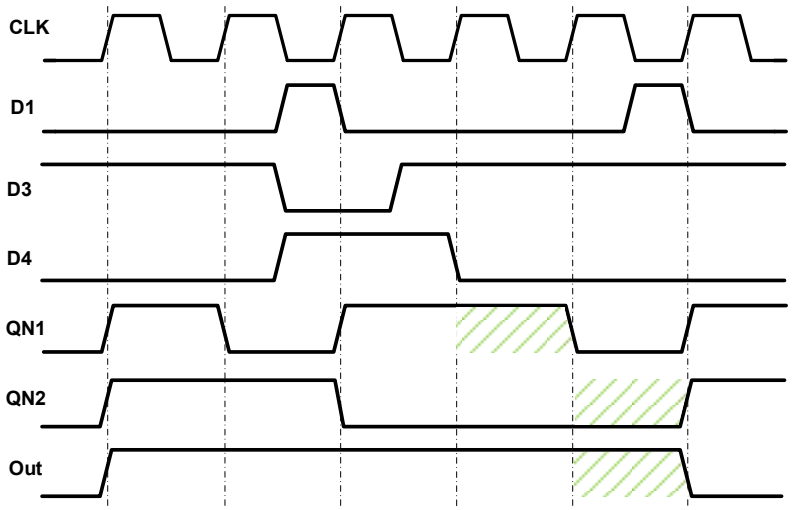


Figure 3.10: Divide-by-9 operation of the proposed 8/9 prescaler when MC is "1"

logic "0", it forces D4 to logic "1" accordingly. Transistor M16 gets disconnected from VDD and node D2 hold its previous value "0" for one extra CLK cycle which reflects in QN1 as highlighted in Figure 3.10. Thus DFF1 extends its one CLK cycle and perform divide-by-3 operation with the help of PEL circuit. There is no change in the functionality of asynchronous divide-by-4 circuit except its input frequency becomes $f_{CLK}/3$ and the whole 8/9 prescaler performs divide-by-9 operation.

Power Consumption

In addition, the key operation in divide-by-9 mode is the divide-by-3 operation of the improved 2/3 prescaler. In this mode, PEL circuit also has switching activity and therefore power consumption of the proposed 8/9 prescaler during this mode can be written as

$$P_{Pro-div-9} = P_{\text{switch,PEL}} + P_{\text{switch,DFF1}} + P'_{asy-div-4} \tag{3.10}$$

where $P_{switch,PEL}$ represents switching power consumption of PEL, and $P'_{asy-div-4}$ represents power consumption of asynchronous divide-by-4 unit during divide-by-9 operation.

Since asynchronous divide-by-4 unit has input frequency of $f_{CLK}/3$, its power consumption

Table 3.1: Transistor sizing of the proposed 8/9 prescaler

M0	5μ	M10	4μ	M20	4μ	M30	3.2μ
M1	5μ	M11	4μ	M21	4μ	M31	4.5μ
M2	5μ	M12	6μ	M22	6μ	M32	6μ
M3	5μ	M13	3μ	M23	3μ	M33	2.5μ
M4	7μ	M14	1.4μ	M24	2.5μ	M34	5μ
M5	3μ	M15	4.5μ	M25	6μ	M35	5.25μ
M6	2.8μ	M16	5.5μ	M26	5.25μ	M36	4.8μ
M7	2.6μ	M17	4.5μ	M27	4.8μ	M37	7μ
M8	2.6μ	M18	4.8μ	M28	7μ	M38	4μ
M9	3.8μ	M19	6μ	M29	4μ	M39	3.2μ

can be written as

$$P'_{asy-div-4} = \frac{f_{CLK}V_{DD}^2}{3}\left(\sum_{j=1}^{3} C_{Lj} + \frac{\sum_{i=k}^{3} C_{Lk}}{2}\right) \tag{3.11}$$

3.5 Simulation Results

The proposed 8/9 prescaler is implemented in 0.18μm CMOS technology using Cadence Design Environment. The transistor sizing used in the proposed design is shown in Table 3.2. Simulations were carried out using Cadence Spectre at typical corner and 27° C temperature with 1.8V supply.

To drive the prescaler, sine wave with 1.8V peak-to-peak swing is used as an input clock. Figure 3.11 shows layout of the proposed 8/9 prescaler, which occupies the area of 33 x 24 μm^2.

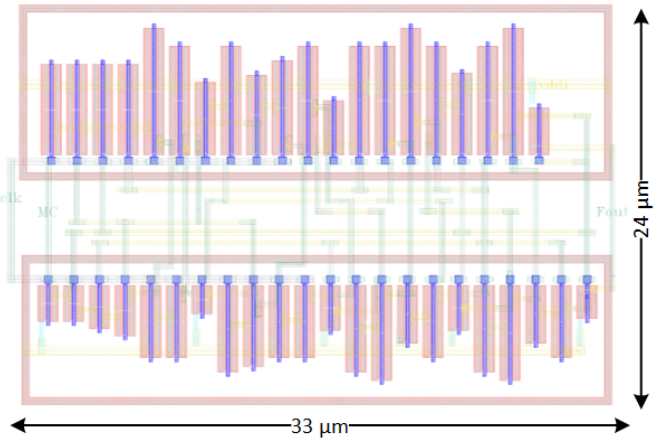


Figure 3.11: Layout of the proposed 8/9 prescaler

Figure 3.12 depicts the simulated waveform of main internal nodes during divide-by-8 mode and divide-by-9 mode for the 8/9 prescaler, respectively. Figure 3.12 (b) shows that internal nodes D3 and D4 only have switching activity for one clock cycle, indicating nearly the same power consumption for both modes of operation.

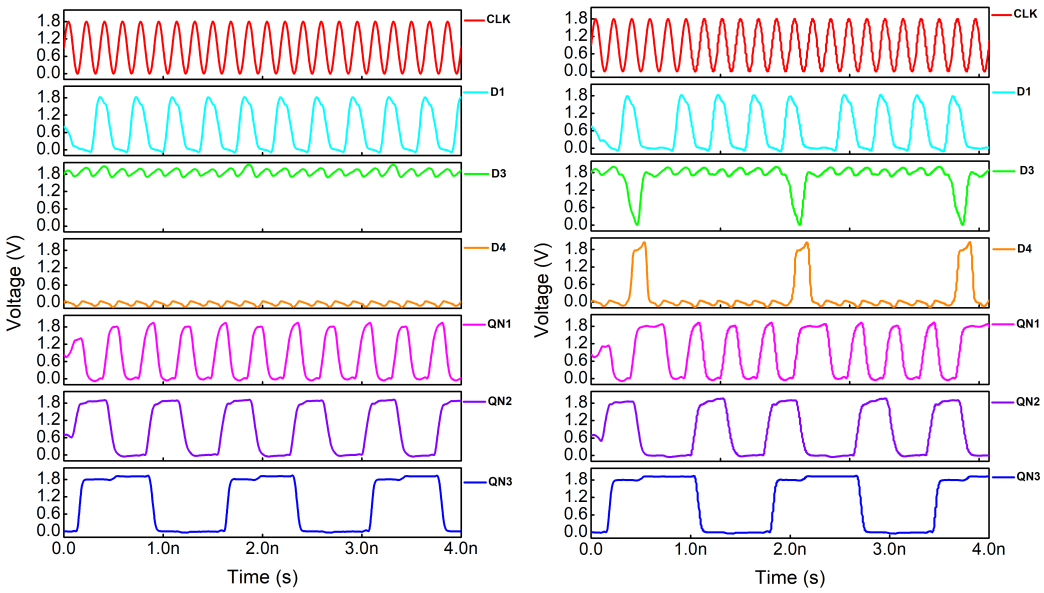


Figure 3.12: Waveform of internal nodes at 5.5 GHz during (a) divide-by-8 mode (b) divide-by-9 mode

Figure 3.13 (a) shows the post-layout simulated power consumption of the proposed prescaler versus working frequency for divide-by-8 and divide-by-9 mode. Results indicate that the prescaler can achieve a maximum operating frequency of 5.5 GHz during divide-by-9 mode. Figure 3.13 (b) shows the power consumption of the 2/3 prescaler across different frequencies. Working at maximum frequency, most of the power of 8/9 prescaler is consumed by 2/3 prescaler which can be concluded from the Figure 3.13 (b).

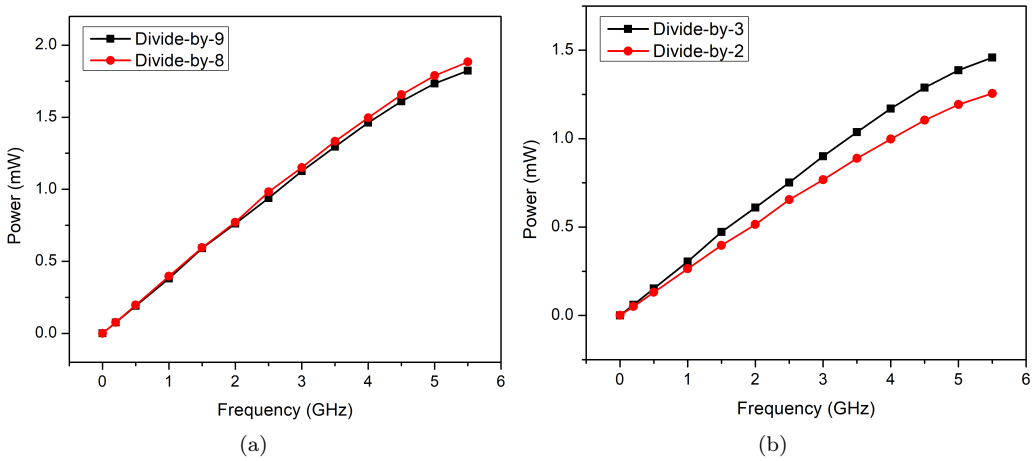


Figure 3.13: (a) Power vs frequency of the implemented 8/9 Prescaler (b) Power vs frequency of the proposed 2/3 Prescaler

By choosing the transistor sizing appropriately, the maximum operating frequency of the prescaler can be further increased [63, 65]. The maximum power consumption of the proposed prescaler at the maximum working frequency is 1.9 mW during the divide-by-8 mode. Both modes consume nearly the same amount of power at the same frequency, which was only achieved by adopting

a two-stage PEL circuit and eliminating one redundant branch from each DFF. The prescaler proposed in this work achieves a power efficiency of 350 μW/GHz, resulting in the lowest power consumption compared with the previously published literature [61, 62, 66–68]. Table 3.2 compares the proposed prescaler with previously reported works. The maximum operating frequency of the proposed circuit is comparable with the previous works. A significant improvement in power consumption is observed compared with previously published literature. Additionally, the proposed circuit achieves wide operating frequency range from 2 MHz-5.5 GHz.

Table 3.2: Comparison with the state-of-the-art

Design Parameters	**[66]**	**[67]**	**[61]**	**[62]**	**[68]**	**This Work**
Type	TSPC	TSPC	E-TSPC	TSPC	TSPC	TSPC
Division Ratio	2/3	7/8/9	8/9	32/33, 47/48	15/16	8/9
Frequency (GHz)	0.2-2.4	3.4-5	1-4	2.4-2.484, 5-5.8	0.5-3.125	0.002-5.5
Power (mW)	0.7	1.6	3.3	2.2	4.23	1.9
FoM (GHz/mW)	3.4	3.125	1.21	2.6	0.7	2.9
Supply (V)	1	1.2	1.8	1.8	1.8	1.8
Process (μm)	0.18	0.13	0.18	0.18	0.18	0.18

3.6 Summary

This chapter discusses the fundamentals of dual modulus prescalers and their implementation using TSPC and E-TSPC logic. A novel low power 2/3 and 8/9 dual modulus prescaler is also presented by using TSPC logic. The proposed 2/3 prescaler saves more than 74% power compared to the conventional 2/3 prescaler [49]. The proposed prescaler is designed using 0.18 μm CMOS technology which consumes a power of 1.9 mW under the 1.8 V supply voltage. First 2/3 stage consumes maximum 1.48 mW of power when working in divide-by-3 mode. The proposed circuit achieves an operating range of 2 MHz to 5.5 GHz. Prescalers reported in [61, 68] consume higher power while having the lower number for highest operating frequency. Prescalers in [62, 66, 67] consume lesser power but their minimum operating frequency is much higher than the proposed design. Therefore, the proposed design is suitable for wide-band applications as compared to the state-of-the-art presented in Table 3.2. Since frequency dividers are power hungry block inside a PLL, a novel output frequency divider for PLL is discussed in the next chapter.

Chapter 4

Programmable Frequency Divider

Frequency dividers are one of the most critical blocks of frequency synthesizers and PLLs. Some applications require a 50% duty cycle from the clock signal which becomes difficult when division ratio of the divider is also large. Therefore, this chapter discusses the available architectures of frequency divider which can be used with PLLs to provide 50% output duty cycle even at high division ratios.

4.1 Introduction

Frequency Synthesizer is the critical blocks of the RF Integrated Circuits (RFIC) in wireless communication systems [48, 49, 69–72]. Voltage-controlled oscillators and programmable frequency dividers are the highest power-consuming blocks of the frequency Synthesizer [73]. Major specifications desired from a programmable frequency divider are high operating frequency, low power consumption, large division ratio coverage, low noise contribution, division ratio controlled by binary bits, and output duty cycle close to 50% [52].

Therefore, programmable dividers need careful considerations when being designed for low power and low noise frequency synthesis applications [52, 53, 74, 75]. If the output clock is being used for clocking applications, 50% duty cycle becomes one of the major criteria for the clock signal. Several architectures are available for programmable frequency dividers but not all can achieve a 50% duty cycle [46, 76–79].

Programmable dividers consist of dual modulus Prescaler to cover required divisions. One of the commonly used prescalers is Vaucher prescaler [46] which can perform either divide-by-2 or divide-by-3 operation depending on its mode control signal. In [46], a 20-bit programmable divider is presented with a division ratio coverage of 8 to 524287. The major problem with this divider is that its output signal can't achieve 50% duty cycle for higher division ratios. For example, duty cycle for a division ratio of 8 is exactly 50% but becomes almost 0.00153% for a division ratio of 524287. This extremely low duty cycle can cause the failure of the loop divider inside a frequency synthesizer. Therefore, it becomes challenging to achieve 50% duty cycle along with a full division

range, especially, for higher divisions. The next section discusses the available architectures of frequency dividers.

4.2 Conventional Programmable Frequency Dividers

Two common types of frequency dividers used in clocking applications are divide by 2/3 prescaler based frequency dividers and programmable frequency dividers which are explained as follows -

4.2.1 Divide-by-2/3 based Programmable Frequency Divider

The dual modular divider, shown in Figure 4.1, was proposed to extend the division range of frequency dividers [67, 80], but it cannot provide 50% output duty-cycle as explained in the previous section.

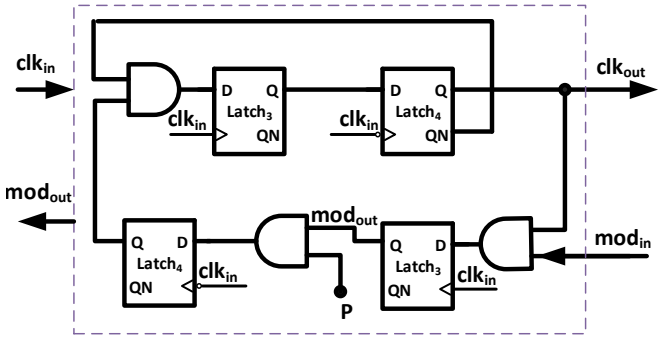


Figure 4.1: 2/3 Dual modulus prescaler proposed in [46]

Programmable frequency dividers are constructed by connecting these 2/3 dual modulus prescalers in a chain, and the division ratio is changed by the controlling bits P_i as shown in Figure 4.2. Each 2/3 prescaler stage can perform divide-by-3 if mod_{in} and P_i both are "1", otherwise it only performs divide-by-2 operation.

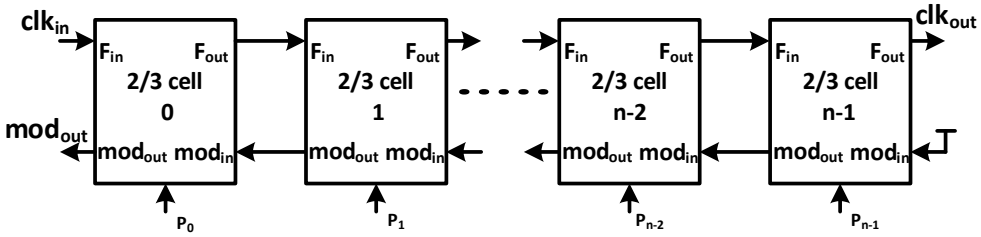


Figure 4.2: Conventional architecture of frequency divider based on 2/3 prescaler

Time period of the output signal of this type of divider is expressed as follows [46]

$$T_{out} = \left(2^n + 2^{n-1}P_{n-1} + 2^{n-2}P_{n-2} + \cdots + 2^1P_1 + P_0\right) \times T_{in} \tag{4.1}$$

where n represents the number of 2/3 prescaler stages, T_{in} is the period of the input clock signal and P_i is programming bits to control the division ratio of the divider chain.

To increases the division ratio, number of 2/3 prescaler stages can be increased to achieve required division. Minimum division of the divider can be decreased by using external logic which can disconnect some stages from the chain in order to achieve division less than 2^n [46].

4.2.2 Programmable Counter based Frequency Divider

Another type of frequency divider based on Pulse Swallow Counter (PSC) is shown in Figure 4.3. It consists of one Dual Modulus Divider (DMD), one Program Counter (PC) and one PSC.

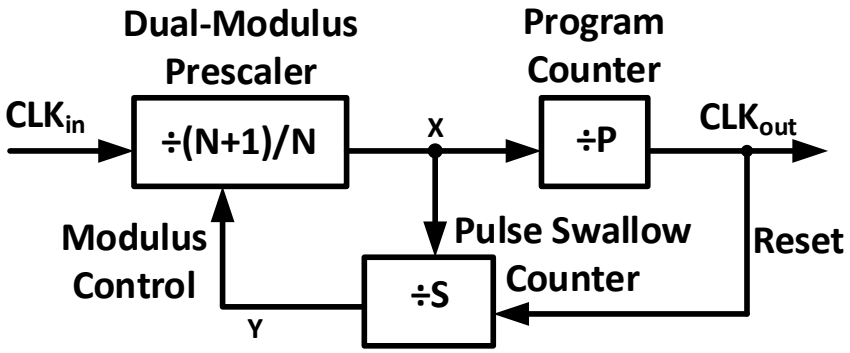


Figure 4.3: Pulse Swallow Counter based frequency divider

When Modulus Control (MC) is "1", DMD works in div-by-N+1 mode else in div-by-N mode. PSC counts S cycles of node X with N+1 division, then PC starts count down for P-S cycles of node X with N division.

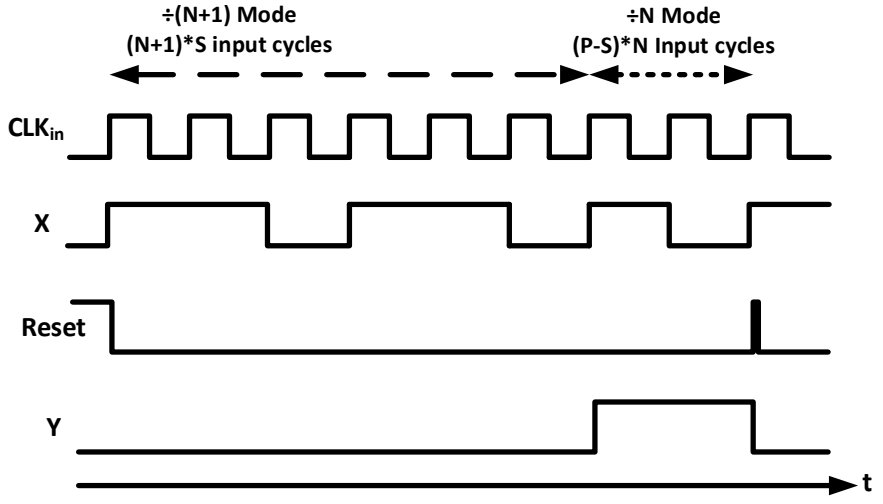


Figure 4.4: Waveform of internal node in Pulse Swallow Counter based frequency divider

As soon as PC reaches “0", it resets PSC and repeats the same pattern as shown in Figure 4.4. Therefore, the division ratio of divider can be written as

$$\frac{CLK_{in}}{CLK_{out}} = (N+1) * S + N * (P - S) = S + P * N \tag{4.2}$$

Typical RF synthesis applications cover frequency band of 2.4 GHz - 2.48 GHz for Bluetooth. It can be implemented using the PSC by keeping P*N = 2400 and varying S from 0-80 for 1 MHz reference signal.

4.3 Proposed Programmable Frequency Divider

4.3.1 Conceptual Design

Figure 4.5 shows the block level topology of the proposed divider which can provide 50% output duty cycle for each division ratio. The block diagram consists of a chain of conventional 2/3 prescalers and a proposed 2-to-7 modulus prescaler stage. This proposed 2-to-7 Prescaler stage has two controlling input bits, P_0 and P_1 ,and one extra input mod_shift which becomes ‘"1" when programmable division number (Pdiv) is > 3 else remains "0". In the last 2/3 cell, mod_{in} is connected directly to the supply to enable flow of mod_{out} from right most cell to left most cell. External 2x1 MUX are used to reduce the minimum division number of the circuit. When the select signal of the MUX is enabled, it passes the mod_{out} of one stage to the preceding stage. But when MUX select is "0", it breaks the chain of 2/3 cells and connects mod_{in} to the supply for reducing the division ratio. This concept of reducing the minimum division ratio is adopted from [46].

4.3.2 Implementation of the Proposed Circuit

Circuit diagram of the proposed 2-to-7 modulus Prescaler is shown in Figure 4.6. The basic concept behind the development of this novel architecture is to first divide the given division number by half, then feed it to additional divide-by-2 logic to preform remaining divisions and to correct the duty cycle. It contains one modified 2/3 prescaler, one Auxiliary Path for Extension (APEx) logic, an additional divide-by-2 (AD2) logic, and a Duty Cycle Correction Logic for Odd Integers (DCCOI). Working of these blocks are explained in the following sections.

Modified 2/3

This part of the proposed circuit is similar to the Vaucher’s 2/3 cell. To accommodate it into the suggested design, a few extra logic gates are added. One multiplexer (MUX1) is added which has two inputs, P_0 and P_1 and one select signal mod_shift. When mod_shift is "0", P_0 is passed on to $mux1_O$ else P_1 is passed. Select signal mod_shift becomes “1" only when the given division number is > 3.

In addition, one NAND gate is added too, which is embedded in the flop F2. One input to this gate

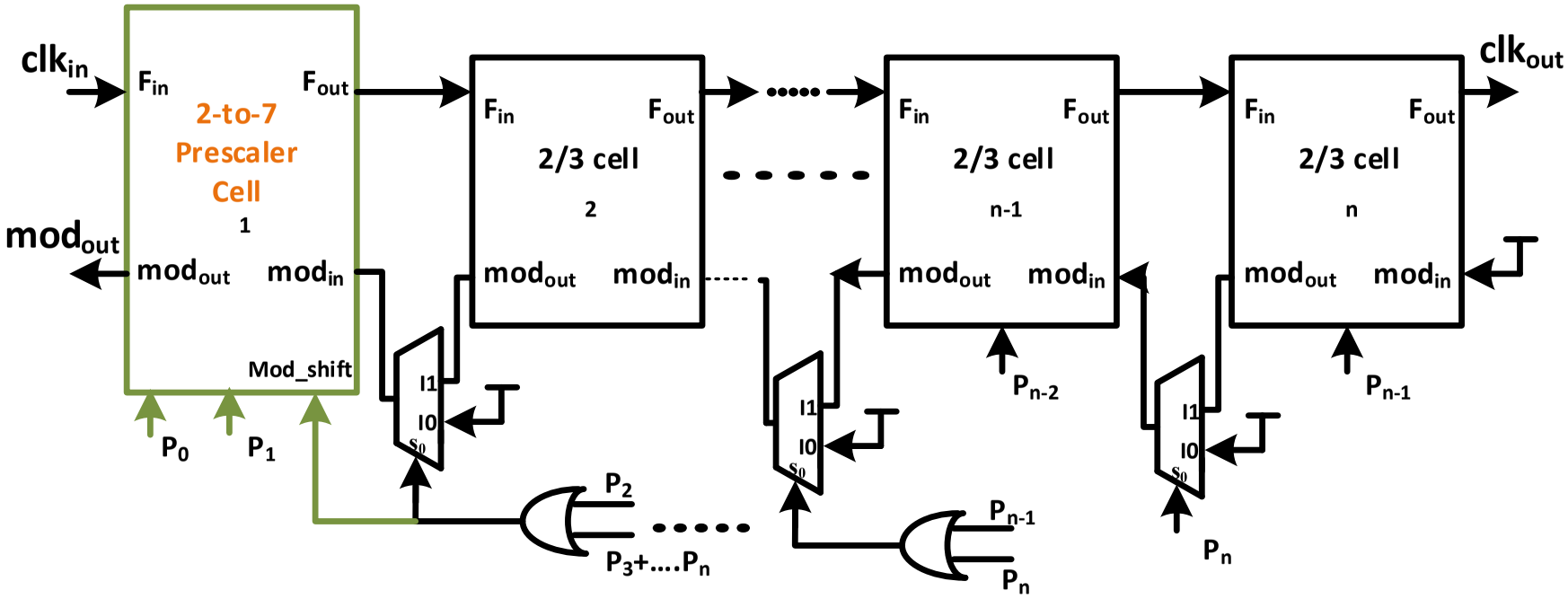


Figure 4.5: Proposed frequency divider's block diagram consisting a novel 2-to-7 modulus prescaler

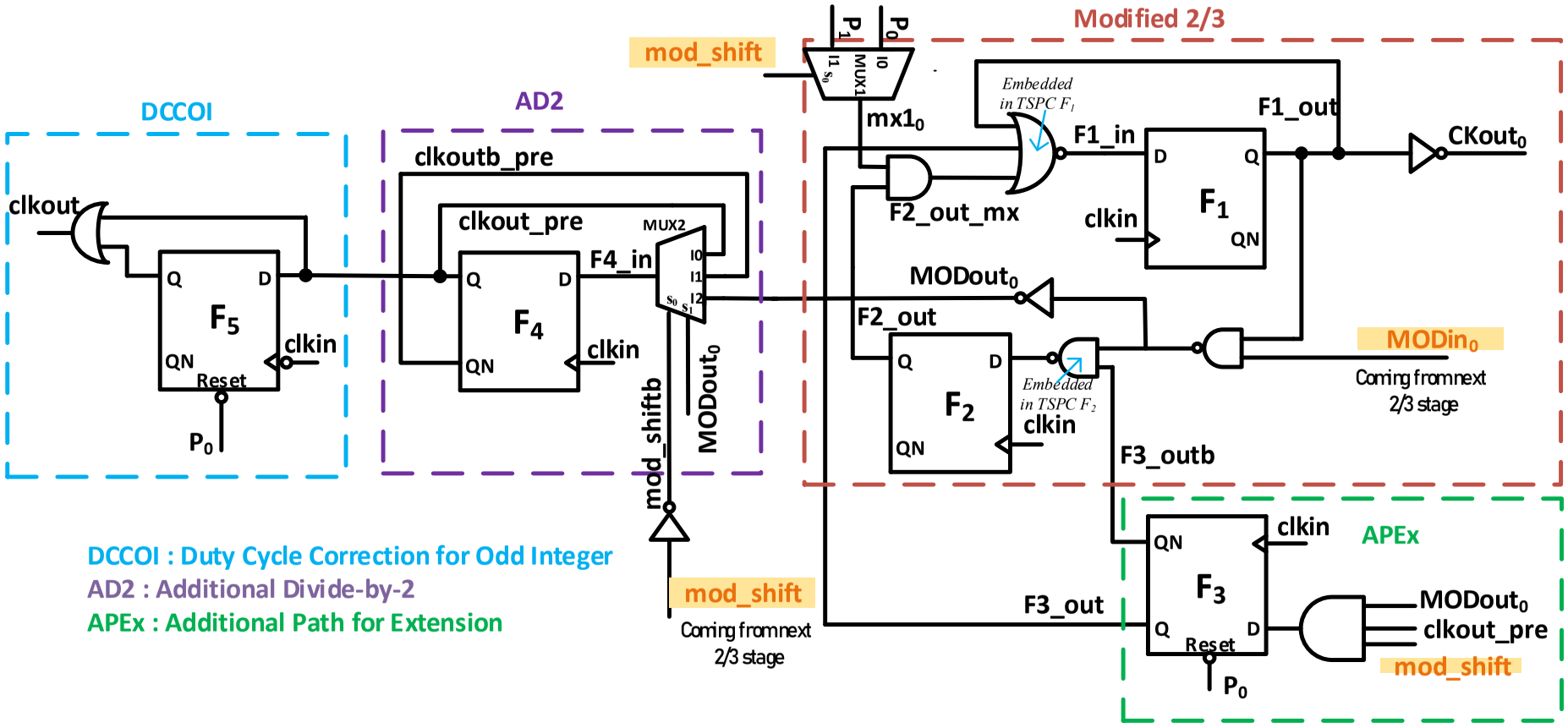


Figure 4.6: Proposed 2-7 prescaler circuit design

is coming from preceding NAND gate and is equivalent to inverted of $MODout_0$. Other input, $F3\_outb$, is coming from APEx logic. Objective of adding the NAND is when given division number is > 3, $F3\_outb$ helps the flop F2 to extend logic "0" for one extra clock cycle at node $F1\_in$ for performing the division above 3.

APEx

It consists of one flop F3 and one three-input AND gate. The flop gets reset when division number is either "0" or even. The output of the AND gate remains "0" if Pdiv is < 4. So, this part of the circuit works only when division number is > 3 for an odd integer number. Different operating division conditions will be used to provide a clear understanding of this concept.

AD2

This logic performs the remaining divide by 2 operation on the input signal $MODout_0$ coming from Modified 2/3. It comprises of one flop F4 and one 3x1 multiplexer (MUX2). This MUX2 has two select signal, mod_shiftb and $MODout_0$ which passes the $MODout_0$ at output clkout_pre when Pdiv is < 4 and simply works as bypass logic. When Pdiv becomes > 3, it works as divide-by-2 circuit by toggling between Q and QN of the flop as input signal. Interesting point of this AD2 is that instead of working at half of the clkin frequency, it works at frequency of clkin so that half cycle of clock can be added further by DCCOI logic to correct duty cycle for an odd integers.

DCCOI

This logic is included only to correct duty cycle when Pdiv is odd integer. It adds half clock cycle of clkin to the clkint_pre signal coming from AD2. In case of even integer, flop F5 remains in reset state, adding nothing to clkin_pre.

To achieve high speed operation, design is implemented using TSPC flops and logic gates are merged inside the TSPC stages of the flops itself in order to reduce the critical timing paths of the overall design. Additionally, it provides benefit to remove redundant static inverter stage when only output QN is required.

4.3.3 Operating principle for different division ratios

To understand the working of the proposed 2-to-7 prescaler, one 2-127 multi modulus divider is implemented. Simulated timing waveform of the major internal nodes are shown in Figure 4.7-Figure 4.13. To understand the working principle of the proposed circuit, 7 cases of different division ratio cases are described as follows.

- **Pdiv = 2**

  In this case, the whole circuit reduces to standard 2/3 Prescaler. Since Pdiv is an even integer and is < 4, APEx remains inactive and therefore the flop F5 also remains inactive in DCCOI

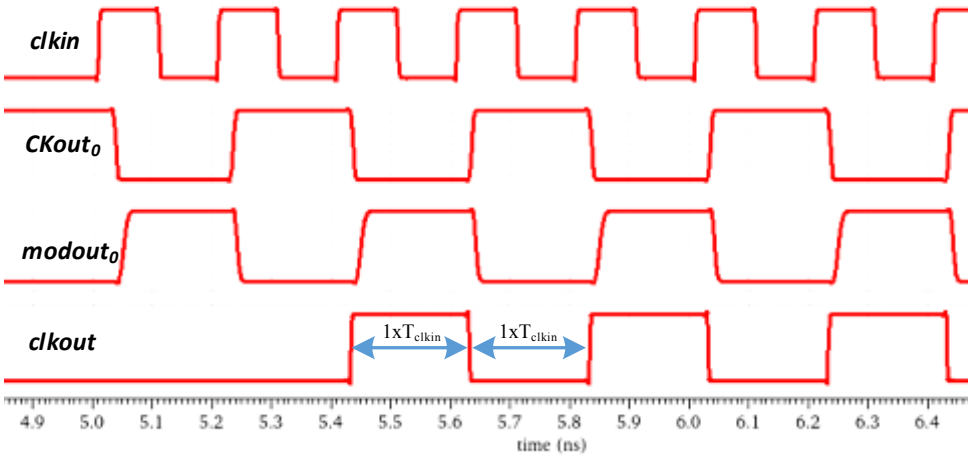


Figure 4.7: Timing waveform during divide-by-2 operation at 5 GHz input frequency

logic. The simulated timings waveform of the prescaler for divide-by-2 operation is given in Figure 4.7. When Pdiv = 2, the Output path F2_out becomes inactive as P_0 is "0". F1 forms the toggle flip flop structure and thus performs divide-by-2 operation. $MODout_0$ of Modified 2/3 passes through MUX2. Because mod_shift is "0" for Pdiv < 4, flop F4 passes the $MODout_0$ with one clock cycle delay and generates clkout_pre. Since P_0 is even, no duty cycle correction is performed on clkout_pre. Thus one input to OR gate becomes "0" and clkout is generated.

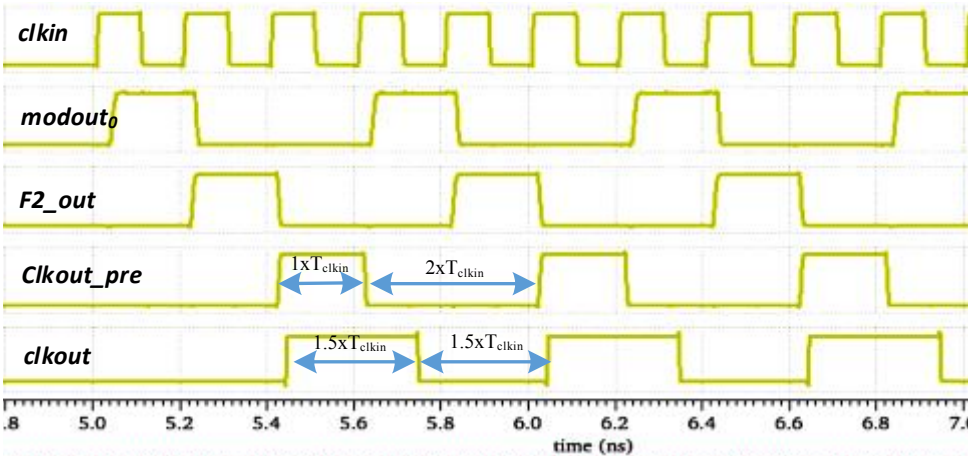


Figure 4.8: Timing waveform during divide-by-3 operation at 5 GHz input frequency

- **Pdiv = 3**

In this case, Modified 2/3 and DCCOI remains as an active portion of the circuit while AD2 simply bypasses the $MODout_0$ to clkout_pre. APEx remains inactive because mod_shift is < 4. From Figure 4.8, when PDiv=3, signal F2_out overwrites the F1_out and extends it for one extra clock cycle of clkin, as a result $MODout_0$ becomes "1" for one clkin cycle. Since P_0 is "1", half cycle is added by flop F5 in clkout_pre signal and thus the clkout is generated with 50% duty cycle.

- **Pdiv= 4**

When Pdiv=4, Modified 2/3 block works as divide-by-2 logic. $MODout_0$ is passed to the flop F4. Since Pdiv is 3, mod_shift becomes "1" and therefore loop formed by the flop F4 and MUX2 divides down the $MODout_0$ by 2. The output signal clkout_pre becomes divided by 4 of the input clock clkin. Timing waveform of the major signals for this case is shown in Figure 4.9. APEx and DCCOI remains inactive for this case.

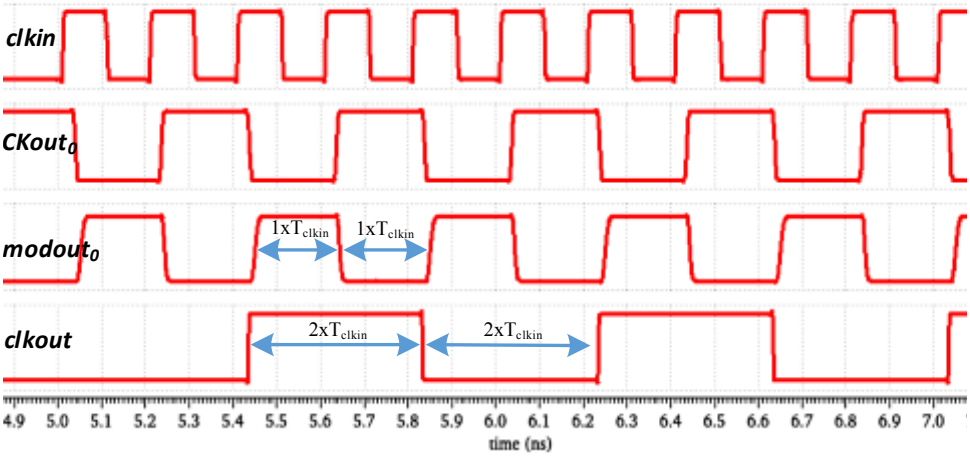


Figure 4.9: Timing waveform during divide-by-4 operation at 5 GHz input frequency

- **Pdiv = 5**

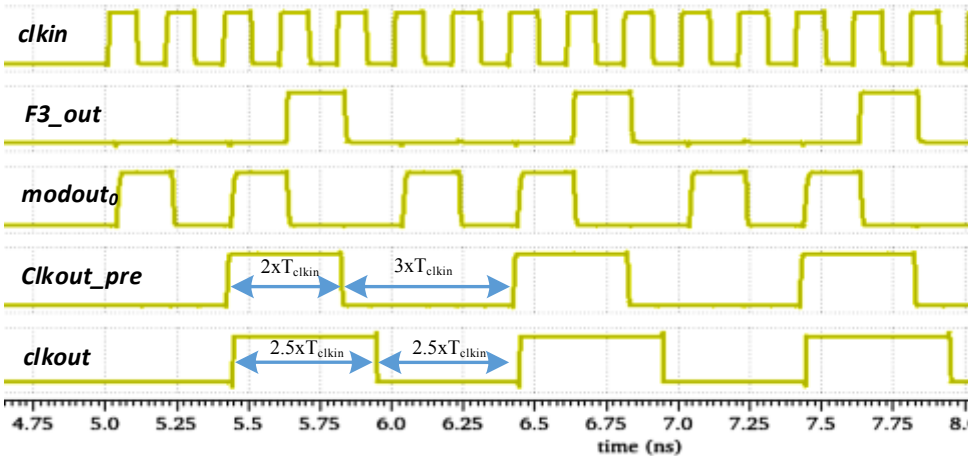


Figure 4.10: Timing waveform during divide-by-5 operation at 5 GHz input frequency

APEx and AD2 logic becomes active for this case. Timing waveform is shown in Figure 4.10. Since mod_shift is "1" and P_1 is "0", MUX1's output, $mux1_0$ becomes "0" which forces F2_out_mx to be "0". Interesting point in this case is that the signal F3_out goes to OR gate and overrides the "0" of F1_out for one clock cycle as shown in Figure 4.10. $MODout_0$ goes to AD2 logic where it is further divided-by-2 and generates clkout_pre. This clkout_pre goes to the 4 input AND gate of APEx logic. One of the APEx output F3_out becomes

"1" when $MODout_0$ also goes to "1" which forces $MODout_0$ to extent for one extra clkin cycle. This way $MODout_0$ toggles between divide-by-2 and divide-by-3 for 5 clock cycles which makes clkout_pre to be divide-by-5 of clkin frequency. This clkout_pre doesn't have 50% duty cycle. DCCOI adds half clock cycle of clkin to clkout_pre to generate clkout with 50% duty cycle.

- **Pdiv= 6**

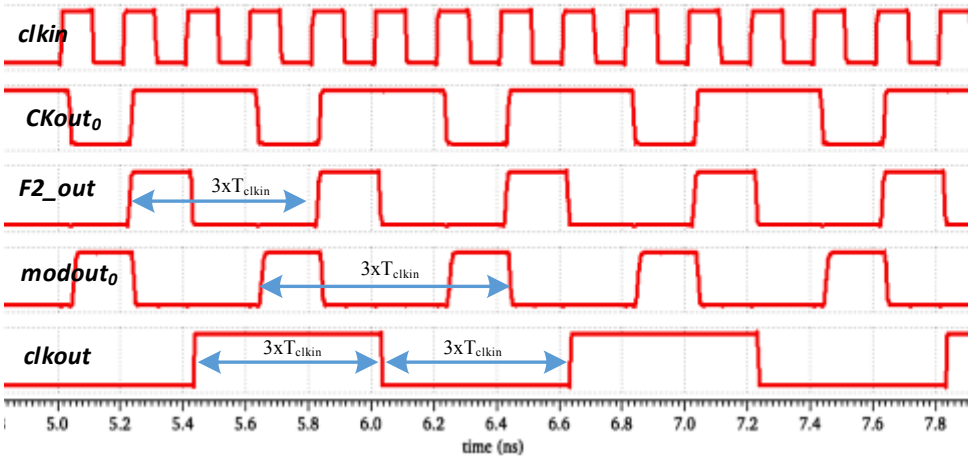


Figure 4.11: Timing waveform during divide-by-6 operation at 5 GHz input frequency

Timing waveform of this case is shown in Figure 4.11. Here, modified 2/3 works as a divide-by-3 circuit. Its output $MODout_0$ is fed to the AD2 logic. Since mod_shiftb is "0", AD2 performs additional divide-by-2 operation on it and therefore output clkout_pre becomes divide-by-6 of clkin. Since Pdiv is an even integer, DCCOI remains inactive and therefore clkout_pre with 50% duty cycle passes through OR gate and generates the clkout.

- **Pdiv= 7**

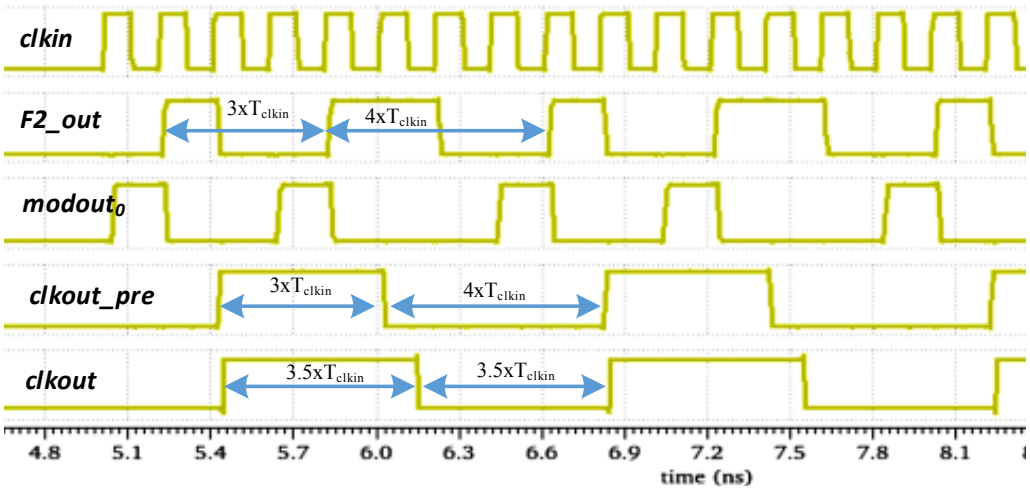


Figure 4.12: Timing waveform during divide-by-7 operation at 5 GHz input frequency

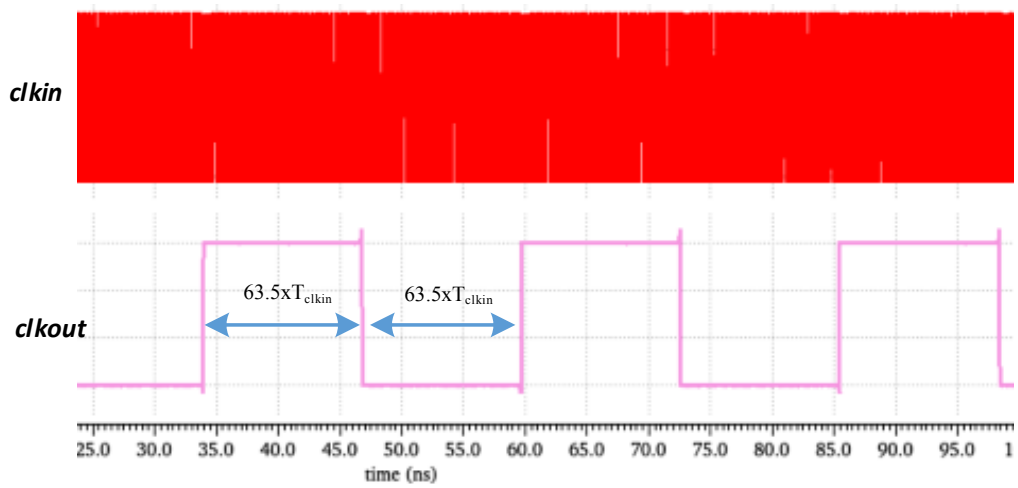


Figure 4.13: Timing waveform during divide-by-127 operation at 5 GHz input frequency

When Pdiv is set to 7, APEx logic makes the $MODout_0$ of modified 2/3 logic toggle between 2 and 3 which is then passed on to AD2 logic. Thus half cycle of clkout_pre contains 4 cycles of clkin and the other half contains 3 cycles of clkin, making clkout_pre to be divided by 7 as shown in Figure 4.12. This clkout_pre is sent to DCCOI logic where half cycle of clkin is added in the signal and clkout is generated with 50% duty cycle.

4.3.4 Implementation of 2-7 multi modulus prescaler

To understand the working principle of the proposed 2-7 prescaler for higher division number, a prescaler with modulus range of 2-127 is implemented using 4 standard 2/3 dual modulus prescaler stages as shown in Figure 4.14.

The implemented prescaler can perform minimum division of 2 and maximum division of 127. The case of Pdiv=127 is taken as an example and its simulated timing waveform is shown in Figure 4.13. All the 2/3 stages work in divide-by-3 mode and 2-7 prescaler in divide-by-7 mode for this case, generating clkout with 50% duty cycle.

4.4 Simulation Results

The proposed prescaler is implemented in 0.18μm CMOS technology using Cadence Design Environment. Simulations were carried out using Cadence Spectre at five different corners at 27° C and 125° C temperature with three different supplies of 1.62V, 1.8V and 1.92V supply. Simulated wave-forms of the prescaler for different division ratios are shown from Figure 4.8 - Figure 4.13 which depict that output duty cycle is always 50% for minimum to maximum divisions of the prescaler.

Figure 4.15 shows the simulated duty cycle of the prescaler across PVT for cases of Pdiv=2 and 3. Variation in PVT includes five process corners, namely, Fast-N Fast-P (FF), Fast-N Slow-P (FS), Slow-N Fast-P (SF), Slow-N Slow-P (SS), and Typical-N Typical-P (TT). Three voltage

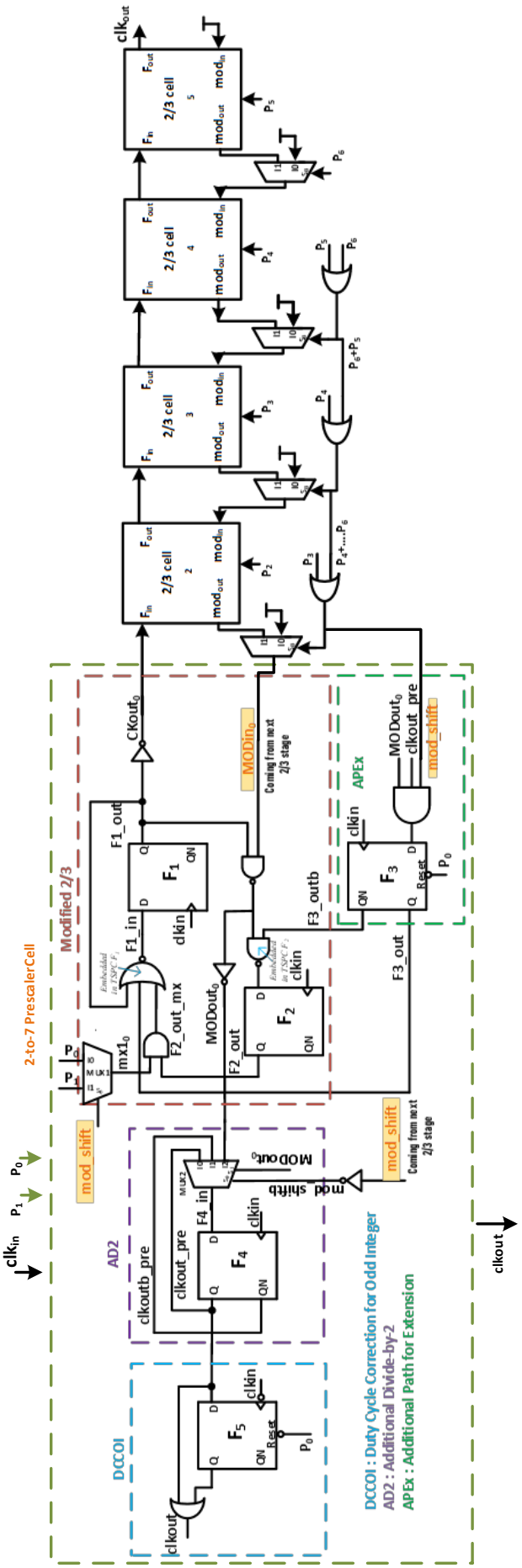


Figure 4.14: Implemented 2-127 multi modulus prescaler

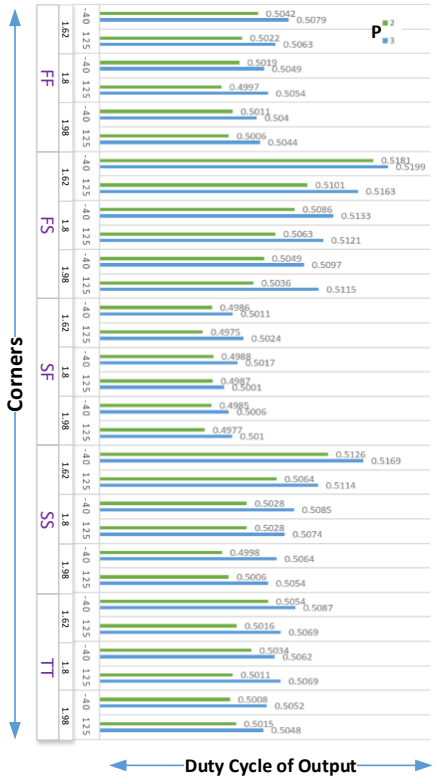


Figure 4.15: Output duty cycle of the proposed prescaler when Piv = 2 and 3

supplies 1.62V, 1.8V, and 1.98V are taken at two extreme temperatures, -40° C and 125° C. It can be concluded from Figure 4.15 that the circuit has duty cycle variation from 50-50.8% at the typical corner and 50-52% at the worst corner (FS). Figure 4.16 shows the simulated power consumption of the proposed prescaler across a frequency range from 2 MHz - 5 GHz. Results indicate that the proposed prescaler can achieve a maximum operating frequency of 5 GHz which can be further increased by optimizing the transistor sizing [63, 65]. The power consumption of the implemented 2-127 prescaler during divide-by-127 operation is 6.5 mW at the maximum working frequency of 5 GHz. The 2-to-127 prescaler achieves a power efficiency of 0.77 GHz/mW, resulting in better power efficiency as compared to the recent literature. Table 4.1 compares the proposed prescaler results with a few previously reported research work. From the table, significant improvement in power consumption can be observed compared with previously published work. Additionally, prescaler achieves a wide operating frequency from 2 MHz - 5 GHz.

4.5 Summary

This chapter discusses the fundamental requirement of a 50% duty cycle from a clock generating circuit for clocking applications. It discusses the conventional divider architectures and their inability to achieve 50% output duty cycle. Some of the recently published work on dividers have also been reviewed. Then, this chapter jumps to the proposed design of a 2-7 multi modulus prescaler with its operating principle. The proposed prescaler is implemented in 0.18μm CMOS

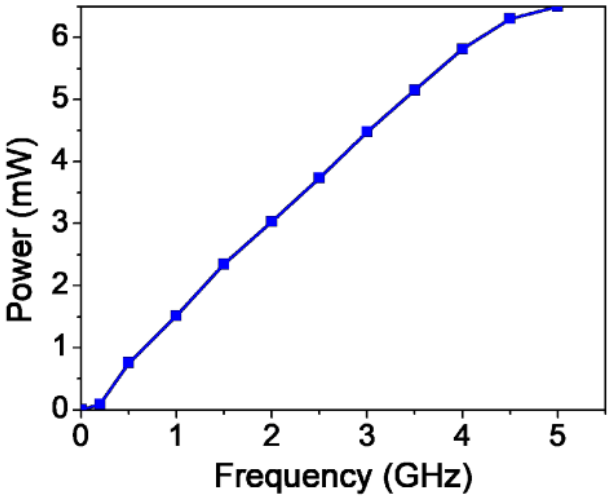


Figure 4.16: Power versus frequency of the proposed circuit

Table 4.1: Comparison with the state-of-the-art

Design Parameters	**[81]**	**[82]**	**[83]**	**This Work**
Duty Cycle Correction	Yes	Yes	Yes	Yes
Division Range	13-1278	8-510	1-256	2-127
Frequency (GHz)	3	2.5	2.3	5
Power (mW)	3.58	15	3.4	6.5
FoM (GHz/mW)	0.84	0.17	0.68	0.78
Supply (V)	1.5	1.8	1.8	1.8
Process (μm)	0.18	0.18	0.18	0.18

technology. It consumes 6.5 mW from 1.8V supply at typical corner. It achieves 0.77 GHz/mW efficiency at 5 GHz operating frequency. Implemented prescaler achieves an operating range of 2 MHz - 5 GHz which makes it suitable for the wide-band applications where 50% duty cycle is required.

Chapter 5

A Constant Transconductance Bias Technique for VCO

5.1 Introduction

There has been a significant increase in the interest of on-chip oscillators for providing less noisy clock for applications targeting frequency range in GHz. A typical serial link communication system needs a high-frequency clock to sample the incoming data. For example, Double Data Rate (DDR) memory controller needs a clock with an accurate 50% duty cycle [84].

A Voltage Controlled Oscillator (VCO) is placed inside a Phase Locked Loop (PLL) to generate accurate clock frequencies of ≈100ppm, which then generates the required frequency clock by tracking the phase and frequency of crystal oscillator [6, 85–89]. In addition to low jitter, a VCO should also have minuscule power consumption, small form factor, and a low variation across various PVT corners [90, 91]. Ring oscillators are popular for their low power consumption, wide tuning range, compactness and moderate jitter performance.

Although, LC oscillators are known for their ultra-low jitter performance, but due to the presence of inductors and capacitors they occupies larger area as compared to ring oscillators [92–97]. Therefore, recent literature has focused on improving the ring VCO performance to make it a viable replacement of the LC VCO while saving a considerable amount of silicon area [98–102].

5.2 Available Literature on PVT Insensitive VCO

In the modern CMOS technologies, Process Voltage Temperature (PVT) variations in the Integrated Circuits (ICs) are one of the biggest concerns. In a ring oscillator, its oscillation frequency and it's gain K_{VCO} are also very sensitive to PVT [103–106]. Many literature have reported that the K_{VCO} is very sensitive across PVT corners, which makes them difficult to be integrated even in wide tuning range PLLs [103, 104, 107, 108]. There have been several techniques proposed in the past to reduce the frequency sensitivity of ring oscillator across the PVT corners.

- PTAT Current Source based Compensation

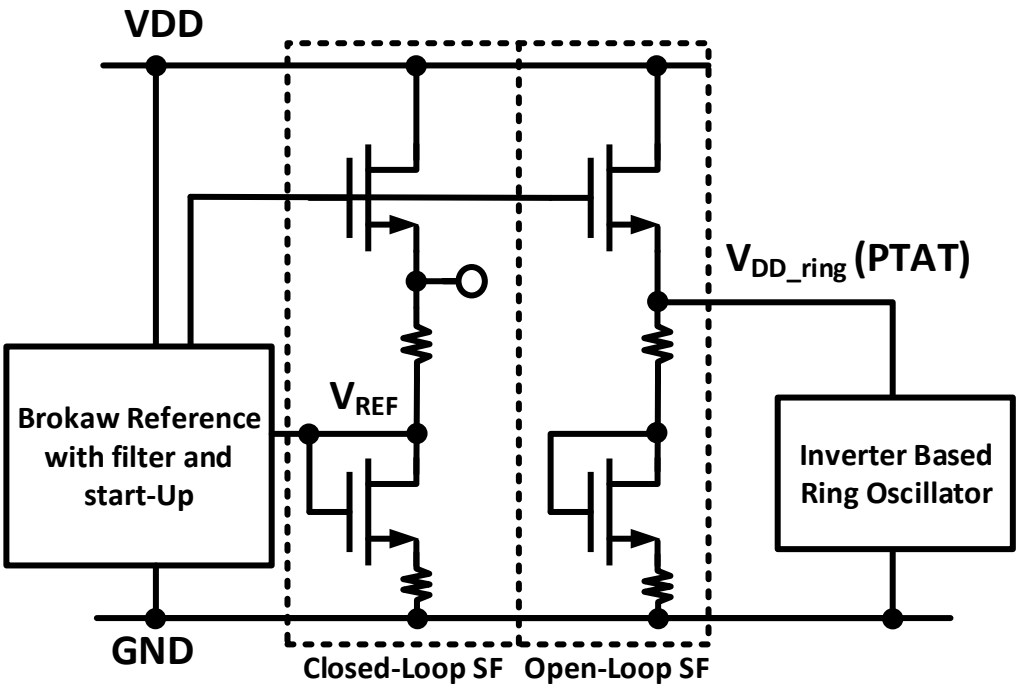


Figure 5.1: Constant gm bias proposed in [107]

Authors in [107] proposed a technique which uses Proportional to Absolute Temperature (PTAT) current to compensate the temperature sensitivity as shown in Figure 5.1. Since this type of PTAT generation circuitry requires Bipolar Junction Transistors (BJTs), it requires extra mask for fabrication process there this solution is not cost effective.

Figure 5.2 shows another technique proposed in [109]. It uses Inversely Proportional to Absolute Temperature (IPTAT) technique to compensate the temperature sensitivity. Even though it doesn't uses BJT in proposed circuitry, higher power consumption is one of the major disadvantage of this technique.

- Regulator based Compensation

Authors in [110] reported process and temperature compensation by adjusting the supply of the inverter with the help of a regulator as shown in Figure 5.3. It uses a Self Bias Generator (SBG) as regulator which controls the supply of two VCO, one sitting inside of PLL loop and one outside. Use of SBG along with two VCOs makes this topology more power hungry and therefore not suitable for low power applications.

Authors in [111] also proposed similar techniques but always trading some other parameters while improving the VCO characteristics

- Transconductance Tracking based Compensation

Authors in [112] proposed inverter transconductance (g_m) adjustment technique for energy efficient transmitter driver as shown in Figure 5.4. The currents I1 and I2 are forced to be

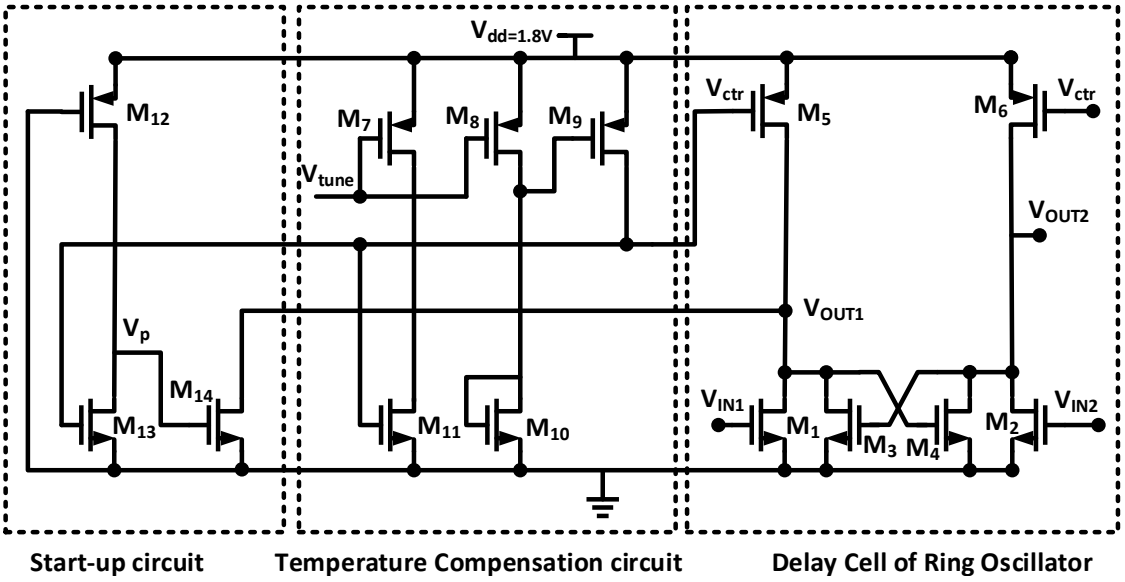


Figure 5.2: Constant gm bias proposed in [109]

equal using a feedback loop. Gm of the 1x inverter is made constant with voltage V2 which is equal to V1 also. Due to 2/1 ratio of the transistor sizing in inverters, Gm of inverter with 1x strength is written as

$$G_m = \frac{1}{R_{EXT}} \left(\alpha - \frac{\alpha}{2^{1/\alpha}}\right) \left[2 + \left(\frac{\beta_p}{\beta_n}\right)^{1/\alpha} + \left(\frac{\beta_n}{\beta_p}\right)^{1/\alpha}\right]. \tag{5.1}$$

Even though author emphasizes from the above equation that Gm only depends on external resistance R_{EXT} and not process or temperature dependent, this topology is very sensitive to transistor models as square law has been used to derive the g_m expression.

Other issue with this architecture is that it employs on compensated capacitance C_{comp} for stability of the loop, which anyhow increases the active area of the physical implementation of the design. Similarly, authors in [113] have assumed the square low to generate temperature compensated circuit for ring oscillator.

All the techniques discussed above are either not suitable for low power applications or can not be considered as effective in deep sub-micron technologies as transistor current equation does not follow square law [40, 114].

Therefore, the work proposed in this chapter is based on a novel bias circuit that makes the inverter transconductance less sensitive to PVT. This further makes the frequency of the VCO less dependent on temperature and process variations.

Next section talks about the fundamentals of ring oscillators and their associated issues.

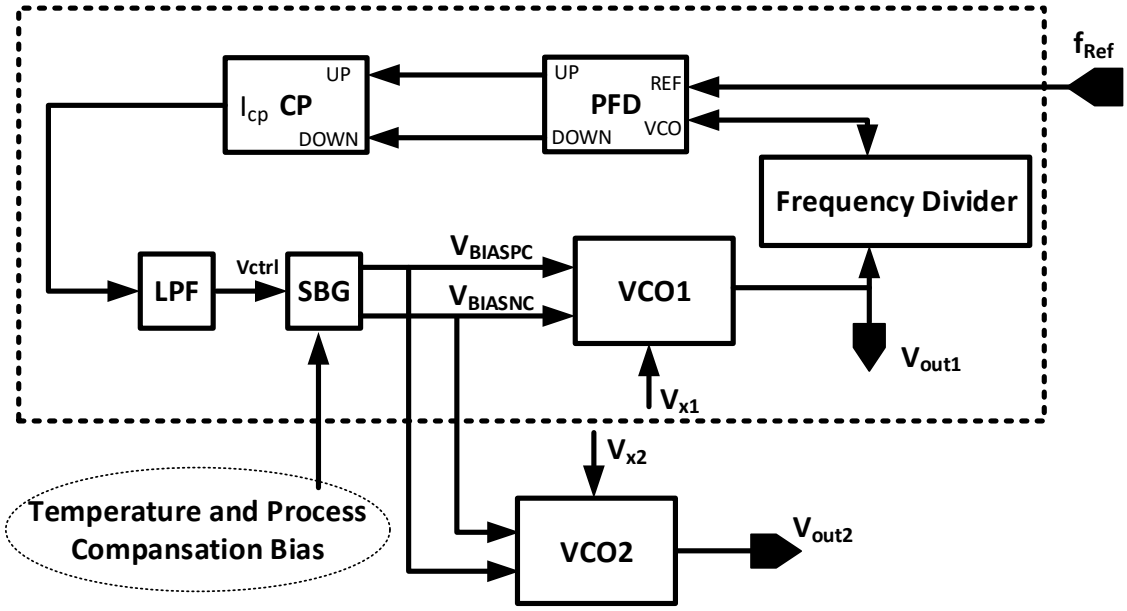


Figure 5.3: Constant gm bias proposed in [110]

5.3 Overview of Ring Oscillator

In a ring oscillator architecture, odd number of inverters are required in the loop in single ended architecture whereas even number of inverters can perform oscillation in differential signaling. Figure 5.5 shows the simplified schematic of the ring oscillator, which consists of single ended inverters connected in a loop.

In general, the differential output is necessary for the present modern day complex Application Specific Integrated Circuit (ASIC) implementations, hence even number of inverters are used in the proposed circuit with a feedback swapping which will be discussed in the coming sections. The small signal oscillation frequency F_{OSC} of a ring oscillator is approximately expressed as follows [107] [115]

$$F_{\mathrm{OSC}} = K\frac{g_m}{C_L} \tag{5.2}$$

where, g_m is the transconductance of the inverter, K is the arbitrary constant and C_L is the load capacitance at output node. As seen from the (5.2), F_{OSC} is directly proportional to g_m.

Generally, F_{OSC} is sensitive to PVT as g_m can vary ≈3 times due to the hot carrier effects and velocity saturation in scaled CMOS technologies as CMOS technologies are moving towards sub 1V power supply range [116]. This could even shrink below to meet a certain frequency range for PLL, where K_{VCO} is found to be increasing from generation to generation [117]. K_{VCO} which is defined as the ratio of change in the frequency to the change in control voltage, plays a major role in deciding the Loop Bandwidth of PLL (BW_{PLL}).

This BW_{PLL} can be defined as follows -

$$BW_{\mathrm{PLL}} = \frac{I_{CP}R_{LPF}K_{VCO}}{2\pi N} \tag{5.3}$$

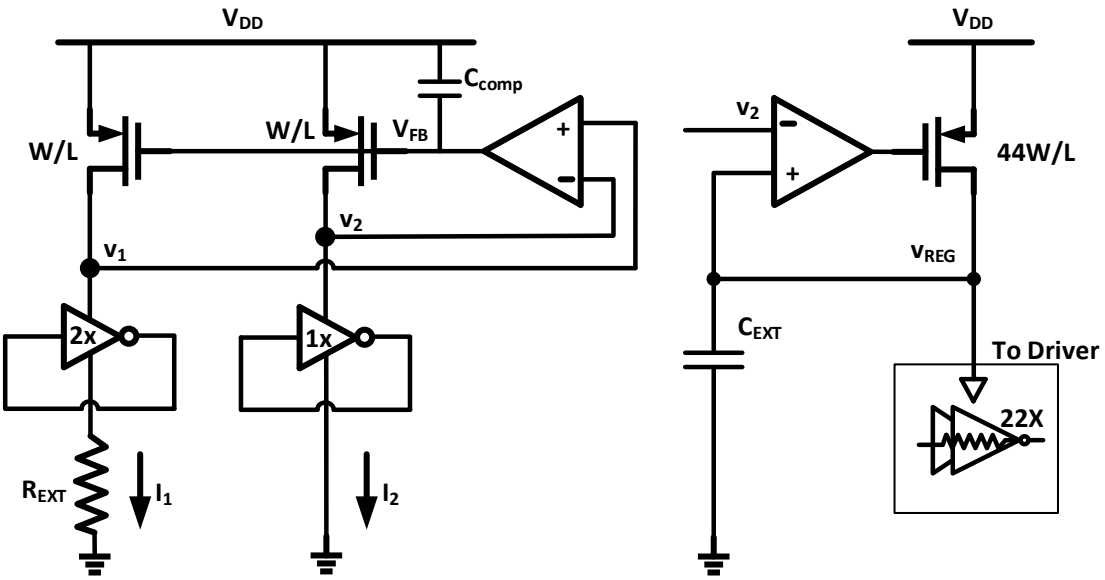


Figure 5.4: Constant gm bias proposed in [112]

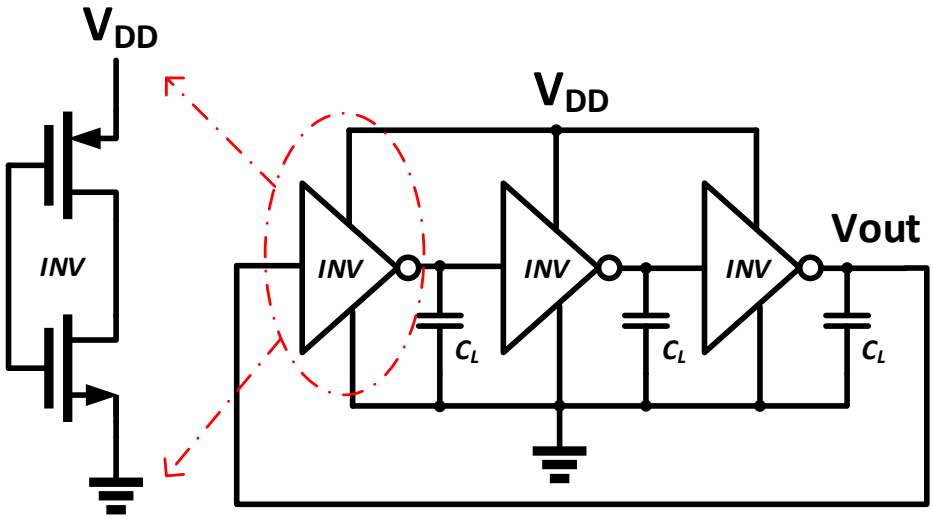


Figure 5.5: Simplified diagram of ring oscillator

Where I_{CP} represents charge pump current, R_{LPF} resistance of low pass filter, and N is the division ratio of divider. It can be concluded from the above equation that K_{VCO} variation directly affects the Bandwidth of a PLL.

Depending on the application and communication protocols the tolerance in bandwidth modulation varies. For example, in the case of Bluetooth protocols, bandwidth can't change by more than 3% across PVT, otherwise inter-modulation can take place due to neighboring channels leakage, which leads to Bit Error Rate (BER) in the data transmission [118].

5.4 Proposed Technique

In this, a low power solution is presented by adjusting the supply of the inverter through a negative feedback such that the effective g_m is constant across the PVT corners. In the proposed circuit, the

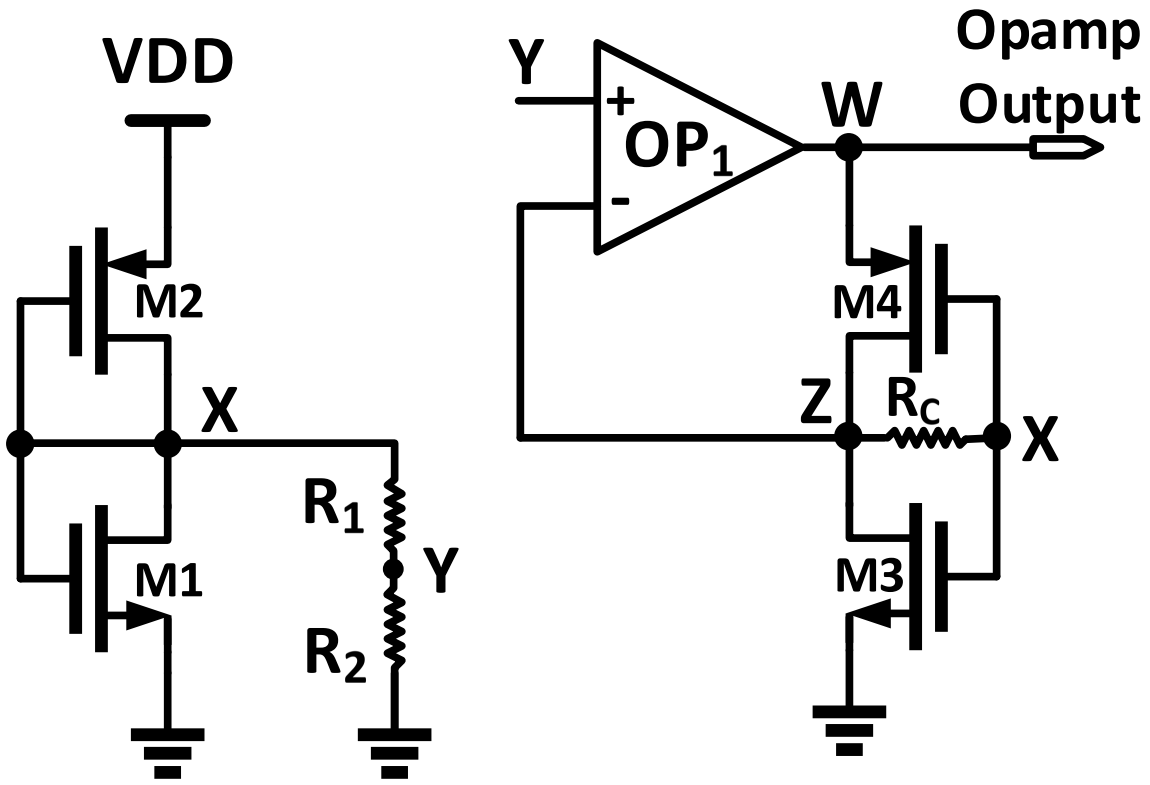


Figure 5.6: Schematic of the proposed constant-g_m bias technique.

main idea is to adjust the supply voltage of the inverter so that the small signal current through the inverter and the reference become same.

Figure 5.6 shows the schematic diagram of proposed constant g_m bias circuit. Left side of the figure shows the self-bias inverter consisting transistor M1 and M2, forming servo loop. This self-biased inverter is used as a reference generator for Operational Amplifier (OP_1) as shown in right side of the Figure 5.6.

The node voltage at X, generated through servo loop is the trip point of the inverter. As shown in fig. 5.6, drain terminals of transistors M1 and M2 are connected to resistance R_1,R_2 which forms the potential divider. The ratio of R_1 and R_2 is chosen such that potential at node Y (V_Y) is slightly less than the potential at node X (V_X). As shown in Figure 5.6, the resistance R_C is connected across the nodes X and Z such that the current flowing through the resistor can be expressed as the following equation -

$$I_{\mathrm{R_C}} = \frac{V_Z - V_X}{R_C} \tag{5.4}$$

Where V_Z and $V_X$represents the node voltages at node Z and node X respectively.

By considering the small signal model the current flowing out of the inverter I_{inv} which is formed by transistor M3 and M4 can be written as -

$$I_{inv} = g_{m3}V_X + g_{m4}(V_X - V_W) \tag{5.5}$$

Where g_{m1} and g_{m2} represents the transconductance of transistor M1, M2 respectively and V_W represents the output voltage of OP_1.

As shown in fig. 5.6, output voltage V_W is connected to the supply of the 4-stage ring oscillator as well as to the replica bias formed by transistor M3 and M4. The node voltage V_W can be expressed as -

$$V_W = \left(\frac{g_{m3}}{g_{m4}} + \frac{1}{g_{m4}R_C}\right)V_X - V_Z\left(\frac{1}{g_{m4}R_C}\right) \tag{5.6}$$

By using (5.5) and (5.6) effective transconductance of replica consisting transistor M3 and M4 can be written as follows -

$$g_{m3} + g_{m4} = \left(\frac{1}{R_C}\right) \tag{5.7}$$

Above equation concludes that the sum of the NMOS (M3) and PMOS (M4) transconductance of inverter only depends on the reference resistance R_C.

Supply of the ring oscillator across PVT varies such that it requires more current at fast process and high temperature [119] corners. The negative feedback formed by transistor M3, M4 and OP_1 takes care of the supply variation of ring oscillator such that the effective transconductance tracks the resistor R_C and tries to stabilize the oscillation frequency.

In this design an NMOS input stage folded cascode operational amplifier has been used, with

a constant current bias generator to keep the transistors in the saturation [120]. A 4-stage ring oscillator has been designed with oscillation frequency of 5 GHz in typical process corner. Figure 5.7 shows the 4-stage ring VCO, where each delay stage consists of the differential inverters with cross coupled latch to guarantee the differential operation. The frequency of the VCO is control by the current starving transistor [118, 119].

5.4.1 Design of Differential RO

As discussed before that an oscillator must meet few important specifications such as low power dissipation, low phase noise, and small active area on silicon. Therefore, a cross coupled differential ring oscillator is adopted to test the proposed technique.

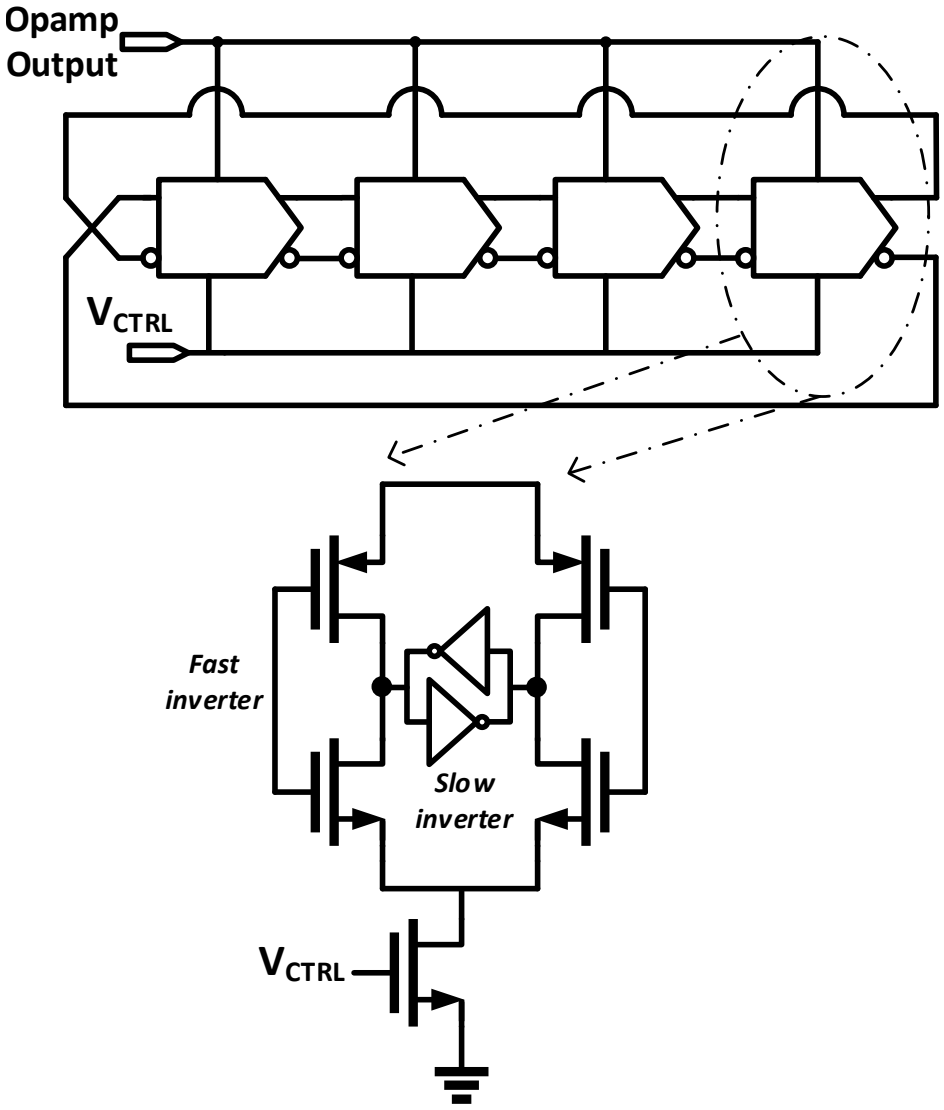


Figure 5.7: Schematic of the differential ring oscillator

There are various reasons to choose this topology. First, odd number of stages are required in a single ended structure whereas we can achieve required tuning range with even number of stages in differential architecture. Second, single ended structure has no common-mode rejection

of supply and substrate noise [121]. Another benefit of selecting differential architecture is that both in-phase and quadrature phase outputs can be extracted from delay cells, which fulfills the demand in modern days communication systems.

Figure 5.7 shows the circuit structure of the implemented differential ring oscillator for proposed technique. It consists of four cascaded differential delay cells. The use of four cells was chosen to decrease the oscillation frequency for a desired center frequency of around 5 GHz.

The delay cell is composed of a differential pair consisting two fast inverters along with two slow inverters connected as latch to ensure the differential operation of the circuit. Ratio of fast inverter transistor sizing to slow inverters sizing is kept around 4x1.

The operation of the cell can be described as follows: by changing the control voltage V_{CTRL}, current through differential inverter is changed which control the delay of unit cell. Therefore, its delay time and thus the frequency of the whole oscillator is varied by steering current through V_{CTRL}.

5.4.2 Design of folded cascode Opamp (OP_1)

The proposed technique employs a self biased Opamp shown in Figure 5.8 [120]. Reason for selecting this architecture is that its self biased and does not require additional bias current source.

Figure 5.8 shows the architecture of the used folded cascode Opamp.

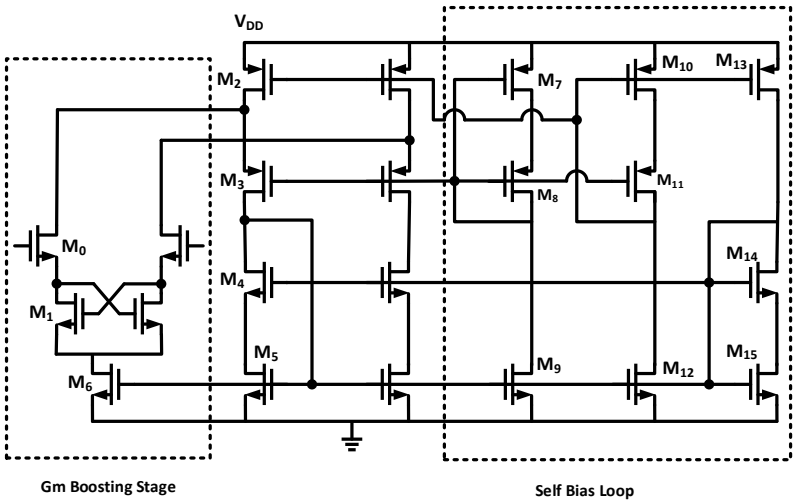


Figure 5.8: Schematic of the folded cascode Opamp used in proposed technique

Transistors M0 form the input differential pair whereas negative degenerative resistance is provided by cross coupled pair of M1 transistors to boost the gain of single stage. Second branch pair shows the loading of first stage formed by transistors M2-M5. Remaining 3 branches are to generate proper biasing to keep all the loading transistors in saturation formed by transistors M13-M15.

The implemented self-bias loop senses the cascode load current through M7-M8 transistors and adjusts gate voltage of tail current source transistor M6. Transistor sizing of differential pair M0 is kept very high to lower the intrinsic offset.

5.5 Simulations Results

The proposed technique has been implemented using Cadence Design Environment in 65nm CMOS technology with 1V power supply. Post-layout simulations has been carried out using Spectre. As explained in the previous section, the g_m of the inverter has been stabilized against PVT corners. Simulations show that the g_m of conventional CMOS inverter has 21% variation across PVT with a nominal value of 100 μS in the typical corner.

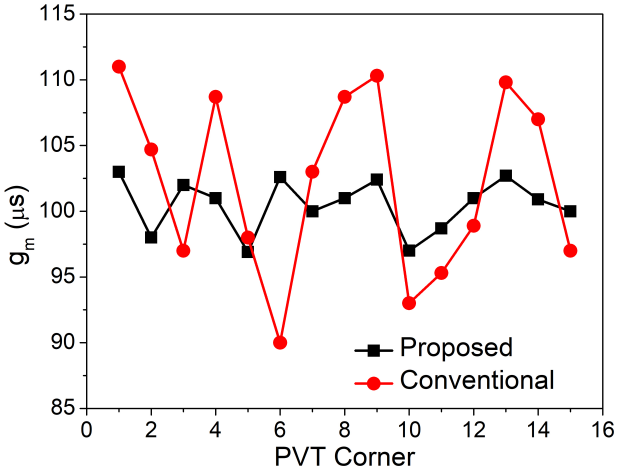


Figure 5.9: Inverter g_m of conventional and proposed technique

Figure 5.9 depicts the comparison of g_m of inverter for conventional and proposed technique across corners. It is clear that variation in g_m has decreased from 21% to 5% with the proposed technique.

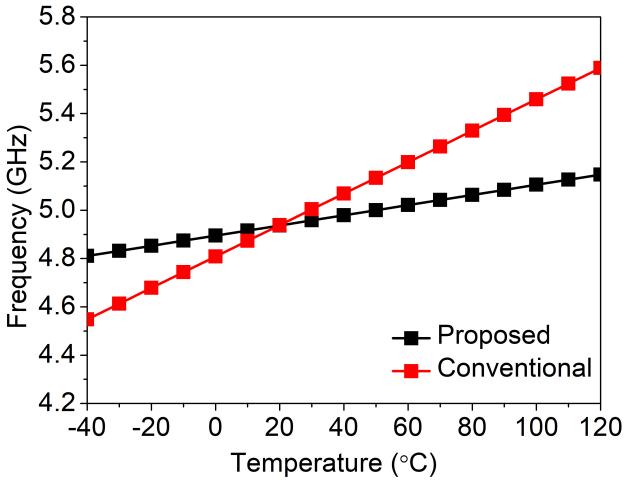


Figure 5.10: Variation of oscillation frequency with temperature

Figure 5.10 shows the temperature sensitivity of the VCO having center frequency of 5 GHz While varying the temperature from -40 to 120° The conventional VCO frequency has 19.3% variation around 5 GHz whereas, the temperature sensitivity has decreased to 7.5% with the proposed technique. The sensitivity can be improved further by taking care of the systematic offset of the used OP_1.

Figure 5.11 shows the variation of K_{VCO} with control voltage V_{ctrl} for the conventional and proposed technique at typical corner.

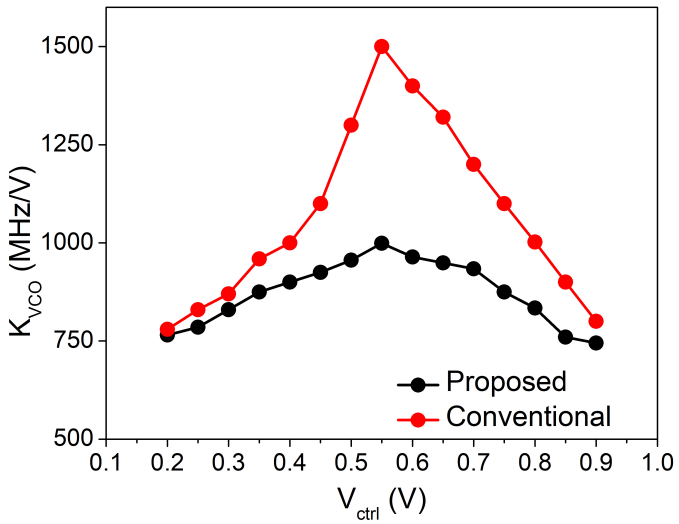


Figure 5.11: K_{VCO} variation with V_{ctrl}

The K_{VCO} of oscillator in conventional topology starts with 765 MHz/V and peaks to 1500 MHz/V at the intermediate control voltage. Whereas with the proposed technique K_{VCO} starts with 750 MHz/v and peaks to 987 MHz/V. Hence, from Figure 5.11 we can clearly say that the K_{VCO} variation has been decreased by 46% with the proposed technique.

Monte-Carlo simulations with 200-points sample have been performed and histogram of free running frequency of the VCO is shown in Figure 5.12.

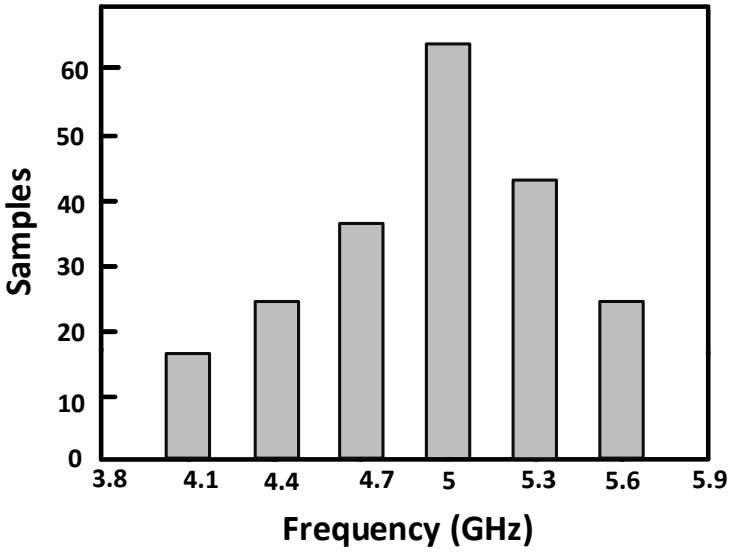


Figure 5.12: Output Frequency Histogram of the 4-stage VCO

It can be seen that the mean frequency is 5 GHz, with the standard deviation of 280 MHz, which translates to 5.6% random variation.

Figure 5.13 depicts the phase noise plot of the ring oscillator which achieves the spot spectral

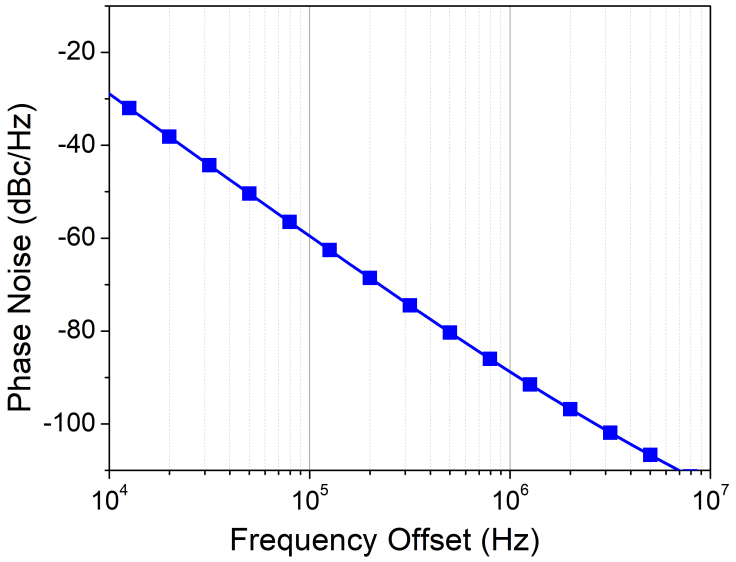


Figure 5.13: Phase Noise plot of the 4-stage VCO

density of -100 dBc/Hz at the 1 MHz offset frequency which can be improved further by optimizing the VCO.

5.6 Summary

Phase Locked Loop (PLL) is an on-chip clock generator for timing-centri electronic systems. Voltage Controlled Oscillator (VCO) is the key element for high performance PLLs. This chapter provides detailed qualitative explanation on voltage controlled oscillators and their operation. It has been proven that variation of small signal transconductance (g_m) is the main dominant source of frequency and gain (K_{VCO}) variation in a VCO. In this work, simulation result for the conventional ring oscillator are presented which demonstrates almost 3 times variation of K_{VCO} across Process Voltage Temperature (PVT) corners. Such huge sensitivity to PVT corners is undesirable for high bandwidth PLL design. To mitigate this sensitivity, a constant-gm bias circuit is proposed, with a detailed mathematical analysis. A prototype of 4-stage ring oscillator with center frequency of 5 GHz is developed in 65nm TSMC CMOS technology, and post-layout simulation results are carried out. Results show that maximum K_{VCO} variation is 28% and frequency variation at given control voltage is 17%. Temperature sensitivity has been decreased from 19.3% to 7%. Proposed solution consumes 2.4 mW power from 1V power supply. The produced simulation results prove the robustness of the proposed bias technique.

Chapter 6

Gain Enhanced Folded Cascode Opamp

6.1 Introduction

Internet of things (IOT) and smart sensors are getting a lot of traction in the present era. The main bottleneck of these circuit realizations is to have an accurate reference voltage/current generator, which is through a Bandgap Reference (BGR). The accuracy requirement of the BGR is becoming stringent. Hence Opamps are suffering from poor voltage head-rooms. Therefore, designing high gain Opamps became very challenging.

Recently Folded Cascade (FC) Opamp has gotten a lot of traction compared to the telescopic cascade because of its relatively larger signal swing and gain compared to the telescopic Opamp [120]. Also PMOS input pair Opamp is the major choice among various Opamps due to its better frequency response and lower flicker noise. Unfortunately, voltage gain of FC Opamps in 45nm and lower CMOS technology nodes is getting lower than 40dB due to the lower output impedance g_{ds}.

6.2 Recent literature on FC Opamps

There has been a lot of research done to develop high-performance FC Opamps. In [123], authors proposed a multi current mirror Operational Transconductance Amplifier (OTA) to enhance the gain and slew rate. In [122], a recycled architecture of FC Opamp is presented to enhance gain and Unity Gain Bandwidth (UGB) by splitting the current in the differential pair as shown in Figure 6.1. A modified version of [124] is presented in [122] to embed the class-AB output stage. Authors in [125] describes the double recycling technique to enhance gain further. However, all of the above-proposed techniques are not suitable for high-bandwidth applications as the frequency response of the OTA has several low-frequency pole-zero doublets.

Next sections discusses the fundamentals of FC Opamp using conventional architecture.

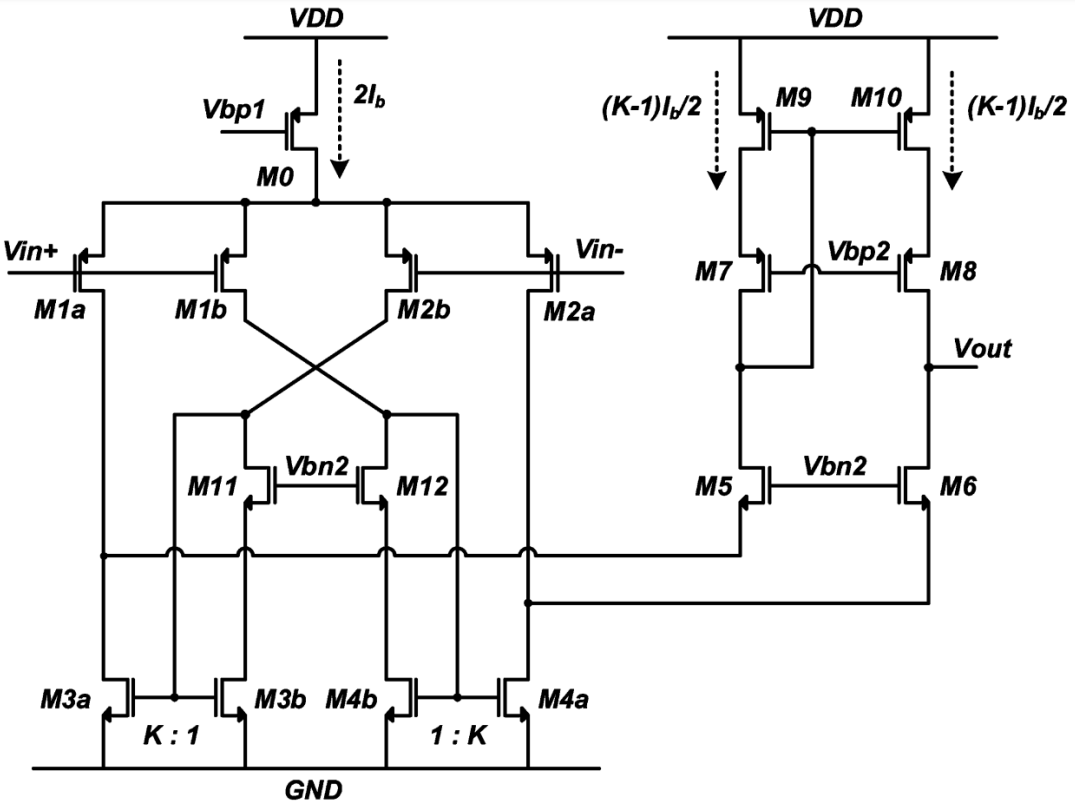


Figure 6.1: PMOS input folded Cascode Opamp proposed in [122]

6.3 Understanding Conventional Folded Cascode Opamp

Figure 6.2 depicts the conventional NMOS input FC Opamp. Transistors M1 form the differential pair, M4 form the cascade load and M6 form cascaded output current mirror. FC Opamp can be viewed as NMOS differential amplifier signal current injected into the PMOS current buffer (common-gate amplifier). As shown in Figure 6.2, the differential pair signal is be injected into source of transistor M4, hence both transistor M1 and M4 bias currents have to be balanced by transistor M3 so that it can carry a much higher current than other transistors. Bias voltages Vb_1, Vb_2, Vb_3 are generated from a typical high swing cascade network [123]. The output swing is not directly related to the input common-mode voltage because of the folding nature at the drain of transistors M3 and therefore the voltage swing output stage is high. The differential output swing can be expressed as 2x($V_{DD} - V_{OV}$) where V_{OV} represents the overdrive voltage, which is relatively high compared to the telescopic version. Also, designing unity gain voltage buffers is relatively easier because of the reason listed above. Though higher swing is the main advantage of the proposed Opamp, it has several disadvantages also as listed below [122]. First, It has poor low-frequency voltage gain because the output impedance is lower due to the g_{ds1} loading at drain of transistors M3. The dc voltage gain $A_V$can be expressed as follows

$$A_V = \frac{g_{m1}}{\frac{g_{ds5}g_{ds6}}{g_{m5}} + \frac{(g_{ds3}+g_{ds1})g_{ds4}}{g_{m4}}} \tag{6.1}$$

where g_m, g_{ds} represent the small-signal transconductance and output conductance respectively.

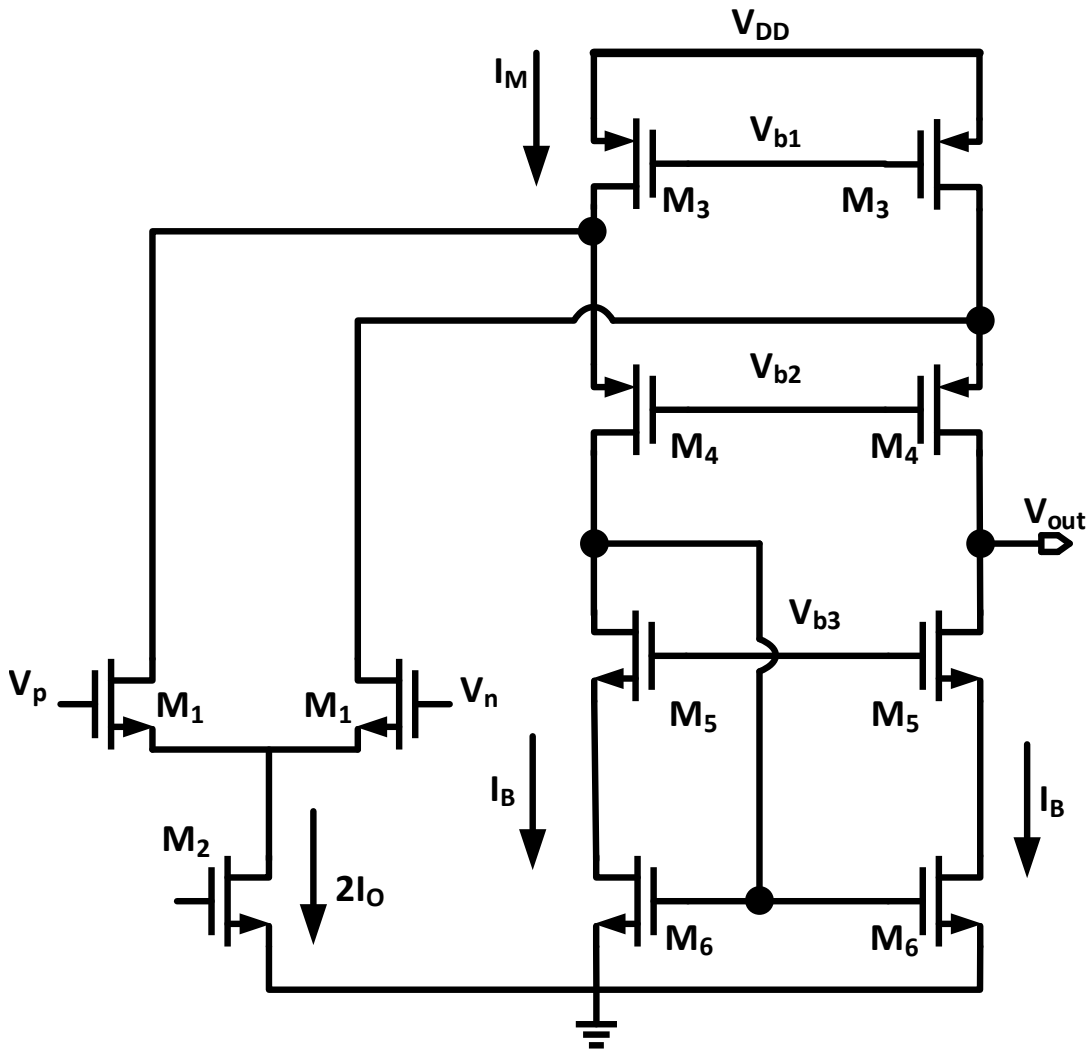


Figure 6.2: Conventional NMOS input folded Cascode Opamp

The second disadvantage is the higher power consumption. From the Figure 6.2, it is clear that M3 should carry sum of the M1 and M4 current which means $I_M = I_B + I_0$. The +ve and –ve slew rate of the FC Opamp can be expressed as ((6.2)), hence to achieve symmetric slew rate $I_B >= 2 * I_0$ needs to be satisfied, otherwise output signal will be distorted heavily which is highly undesirable in a switched capacitor amplifier.

$$SlewRate(SR) = \frac{2 * I_0}{C_L} \tag{6.2}$$

Overall, the power consumption is much higher than the telescopic Opamp which is mainly due to the folding nature of the Opamp. The input-referred power spectral density (PSD) can be expressed as shown in Equation(6.7) -

$$V_n^2 = \frac{4KT\gamma}{g_{m1}} \left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m6}}{g_{m1}}\right) \tag{6.3}$$

The majority of the thermal noise is contributed by the transistors M1, M3 and M6. Cascade

transistor noise in the proposed architecture is suppressed by the intrinsic gain of the transistors they are excluded in ((6.7)). In the conventional telescopic Opamp there is no contribution by transistor M6 in the noise. Since transistors M3 carry a much higher current than any other transistor, its transconductance g_{m3} is high and hence results in more noise. This is considered the major disadvantage of the FC Opamp compared to the telescopic, especially in high-resolution applications like continuous-time sigma-delta ADC/DAC applications [125].

In a summary Folded cascade Opamp is interesting architecture from the signal swing point of view but it has poor dc gain and higher input-referred noise while consuming more power [126] as well.

6.4 Proposed Gain Boosting Folded Cascode Opamp Technique

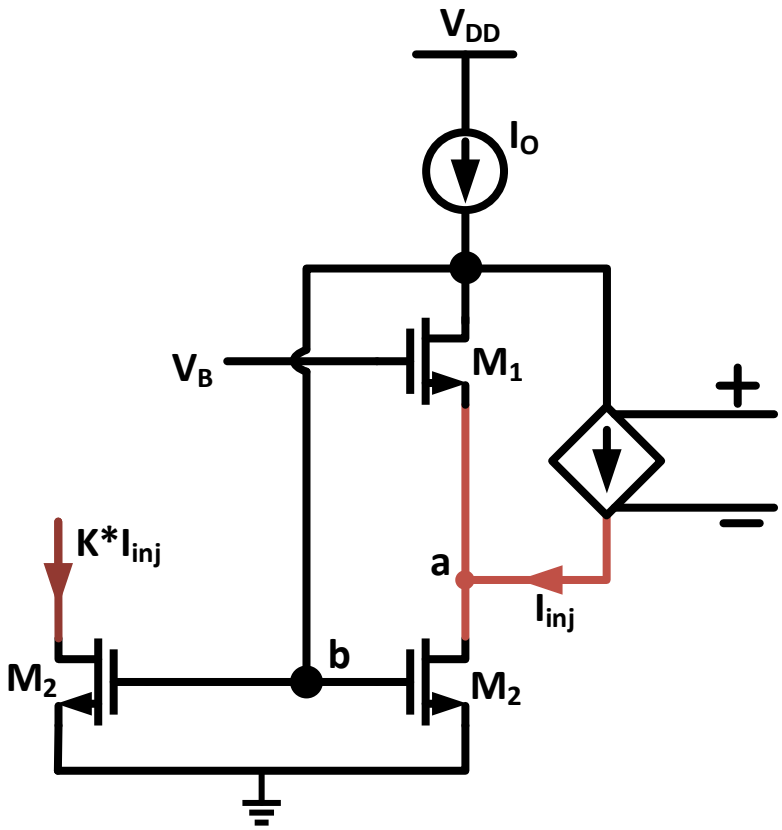


Figure 6.3: Flipped Voltage Follower (FVF) assisted differential pair

The folding transistor M3 shown in Figure 6.2) carries more current without contributing any signal current and therefore no contribution in voltage gain while contributing more noise. One way of utilizing g_{m3} is to somehow inject the input differential voltage signal onto the gates of the transistors M3, which requires two steps to be followed. The first step is to separate some of the input signal current from the differential pair and the second step is to inject that current on top

of the gate of transistor M3. Figure 6.3 depicts the idea of the first step, which is Flipped Voltage Follower (FVF) assisted differential pair [127][128]. It's a voltage buffer formed by transistors M2. The shunt-shunt feedback from the drain of transistor M1 to the M2 gate reduces the output impedance from $1/g_{m1}$ to $g_{ds2}/(g_{m1}g_{m2})$. If there is any signal injected into node "a" shown in Figure 6.5, it has to flow through transistor M2 only since M1 is biased with the fixed current source IB. Hence by using a current mirror formed by transistor M2, signal current can be amplified. In the Figure 6.3, voltage controlled current source (VCCS) represents the differential pair. The impedance at node "a" is very low such that it can act as a tail node in the differential pair [129][130]. Based on this concept, the proposed Opamp is synthesized.

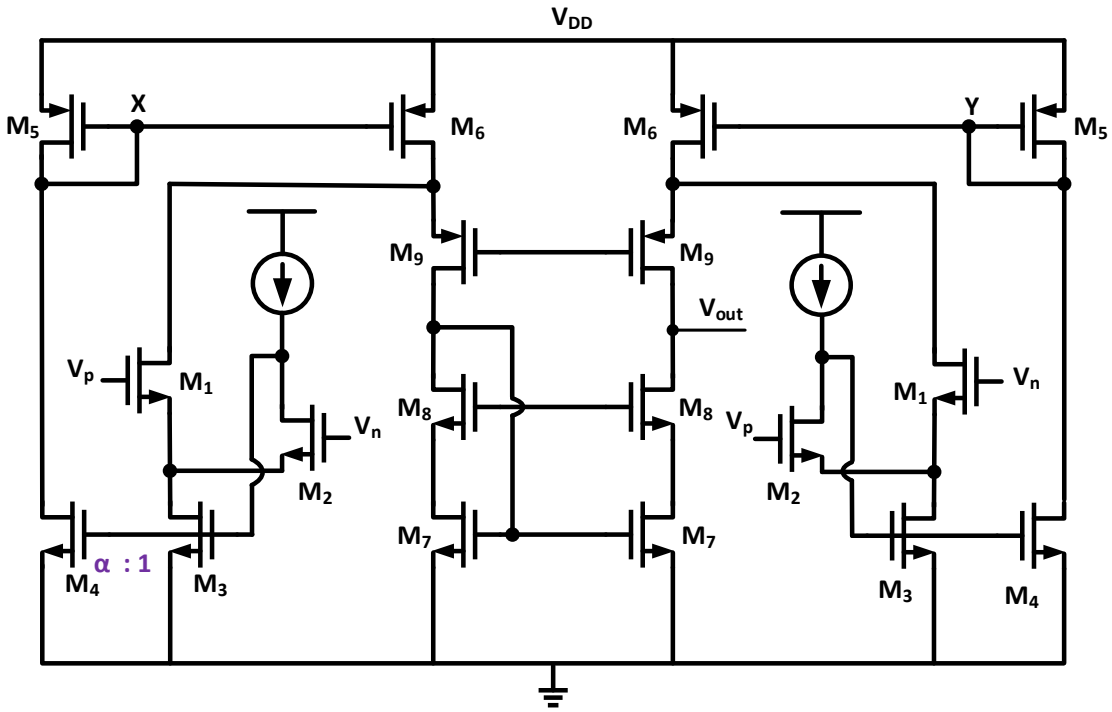


Figure 6.4: Proposed Gain enhanced Folded Cascode Opamp

Figure 6.4 shows the proposed gain enhanced FC Opamp. Here transistors M1,M2 and M3 form FVF assisted differential pair. Compared to the Figure 6.3, the only difference in the FVF circuit is that transistors M1 and M2, are exited by the differential signals V_P, V_N. Transistors M1 and M3 carry small signal currents proportional to $g_{m1}(V_P - V_N)$. The signal current of transistor M1 will be injected into the source terminal of M9 exactly like the traditional FC cascade Opamp. The main difference in the proposal is Folding transistor M6, it's gate is exited by the signal also such that it contributes signal current instead of only supporting the bias current. Transistors M4 and M5 form an amplifier which converts current through transistor M3 into the voltage at source of M3, the current mirror gain ratio is kept α. The voltage at source of transistor M3 and current through transistor M6 can be expressed as follows-

$$V_X = \alpha \frac{g_{m1}}{g_{m5}} (V_P - V_N) \tag{6.4}$$

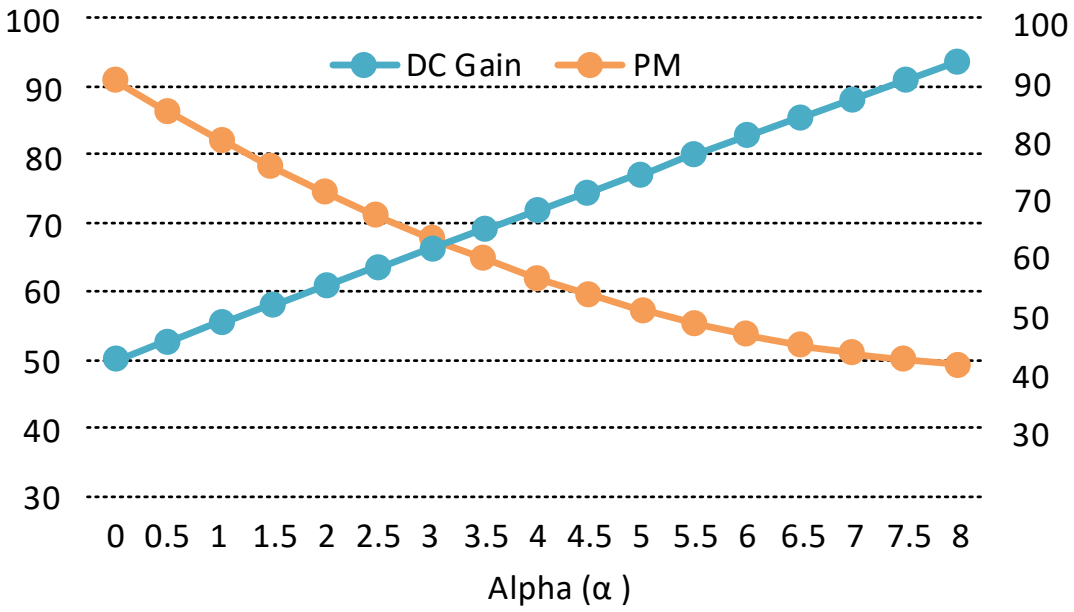


Figure 6.5: DC gain and PM versus α

$$I_{M6} = g_{m6}\alpha\frac{g_{m1}}{g_{m5}}(V_P - V_N) \tag{6.5}$$

The voltage gain of the proposed amplifier can be expressed as follows-

$$A_V = \frac{g_{m1}(1+\alpha\frac{g_{m6}}{g_{m5}})}{\frac{g_{ds5}g_{ds6}}{g_{m5}} + \frac{(g_{ds3}+g_{ds1})g_{ds4}}{g_{m4}}} \tag{6.6}$$

It reveals that the gain of the proposed amplifier is improved by $1 + \alpha g_{m6}/g_{m5}$ times compared to the traditional FC amplifier, which is a substantial improvement. Boosting of this gain can be adjusted by controlling the transistor sizing ratio α. Hence α can be considered as the main design parameter for the proposed Opamp.

Due to the increase in the effective transconductance, the input-referred noise is also decrease proportionally. Equation(6.7) shows the significant reduction in PSD of the input-referred noise in comparison to the conventional FC (6.3).

$$V_n^2 = \frac{4KT\gamma}{g_{m1}(1+\alpha\frac{g_{m6}}{g_{m5}})}\left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m6}}{g_{m1}}\right) \tag{6.7}$$

One issue with the proposed technique is the limit on ratio factor α. From the Equation(6.6), it is inferred that α has no upper limit to achieve enhanced DC gain which is not the case in reality. Increasing α affects the stability[131] of the proposed Opamp and therefore can not be increased beyond a limit. From looking at the Figure 6.4, the parasitic capacitance at source of transistor M3 creates an additional pole in the transfer function and compromises the stability. Hence increasing α improves the dc gain though but decreases the Phase margin (PM) as well. Equation(6.8) shows the closed-form solution for PM as a function of α where W_u represents the Unity Gain Bandwidth

(UGB) and C_X is the capacitance at source terminal of transistor M3.

$$PhaseMargin = 90° - tan^{-1}\left(\frac{W_U}{g_{m5}/C_X}\right) \tag{6.8}$$

Figure 6.5 shows the DC gain and PM versus α of the model Opamp. As explained before, gain increases with α, starting from 50-95dB while varying α from 0 to 8, whereas the PM decreases from 90-40. The optimal value of α lies around 3 in this particular implementation. Beyond this value, significant ringing is found in step response.

6.5 Simulations Results

The proposed technique has been implemented in 1 poly 10 metal 28nm CMOS technology. Conventional and the proposed FC Opamp have been designed for proper comparison. Designed with g_m/i_d ratio of 15 for the differential pair and 8 for the current mirrors [132]. The Opamp is designed with 1V power supply and draws 33μA in a Fast-N Fast-P (FF) process corner and 125°C temperature.

Figure 6.6 shows the frequency response of both conventional and proposed Opamps in unity gain configuration.

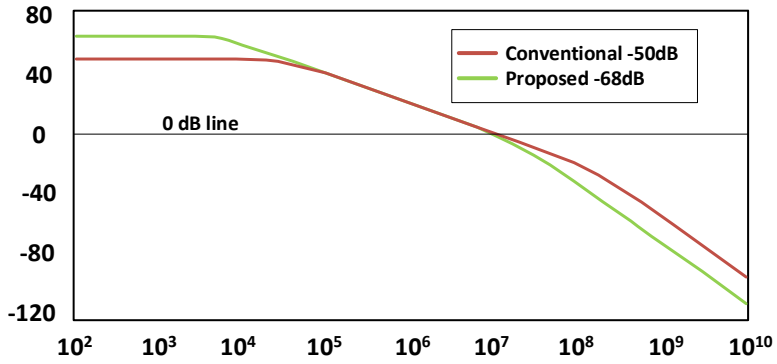


Figure 6.6: Frequency response of the Proposed and Conventional Opamp

Conventional Opamp has 50dB gain whereas the proposed has been displayed 68 dB, achieving 18 dB from gain boosting while keeping the UGB around 10MHz. It can be seen that the proposed Opamp has a non-dominate pole at 20 MHz and due to this the PM has become 63°C, whereas the conventional Opamp PM is close to 90°C.

Figure 6.7 shows the simulated input-referred noise of both Opamps. As explained in Equation(6.7), the proposed solution has a substantial reduction in the noise due to the contribution of the g_m of folding devices. At low frequency, the PSD of the proposed Opamp is improved by 4.5dB. The integrated RMS noise of the proposed Opamp is 51.9μV, whereas the conventional resulted in 62.3μV, providing an improvement of $\tilde{2}0\%$. Usually, noise improvement results in Signal to Noise Ratio (SNR) enhancement without increasing the power consumption of the Opamp. Figure 6.8 depicts the 200-point histogram of the DC gain which shows a 68dB mean (μ) and standard devi-

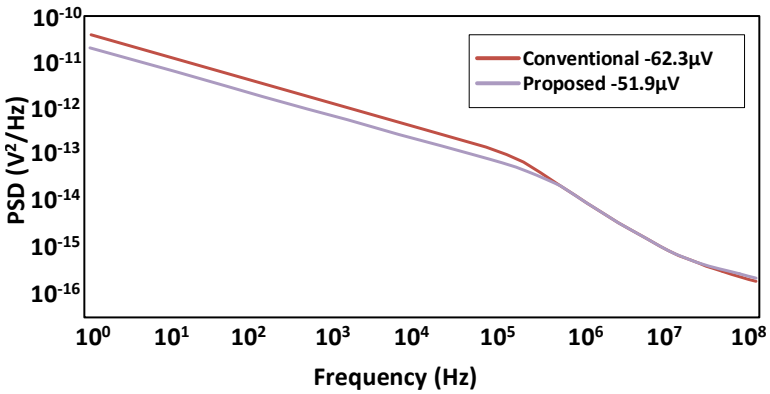


Figure 6.7: Simulated noise of the Proposed and Conventional Opamp

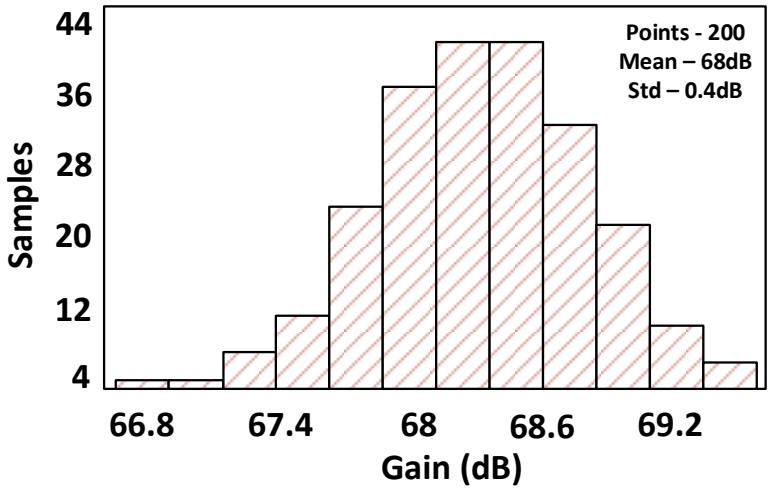


Figure 6.8: 200 point Histogram of the DC gain

ation (σ) of 0.4dB (0.5%). Figure 6.9 shows the layout of the proposed circuit which occupies a 78 x 46 μm^2 active silicon area. All the mismatch reduction techniques like common centroid and inter-digitization techniques for the differential pairs and current mirrors [133] have been adopted for physical implementation.

Table 6.1: Comparison with the state-of-the-art

Design Parameters	**[123]**	**[122]**	**[124]**	**This Work**
Technology (nm)	90	180	65	28
Load Capacitance (pF)	5	5.6	5	10
DC gain (dB)	59	53.6	62	68
FoM (MHz.pF/μW)	3.58	15	3.4	6.5

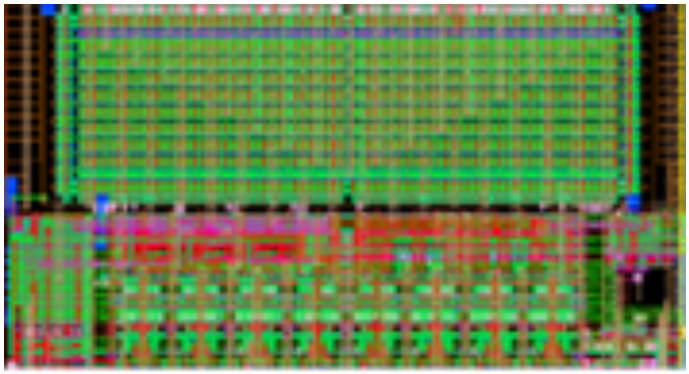


Figure 6.9: Layout of proposed design

6.6 Summary

As folded cascade Opamp is the preferred first stage choice in a typical two-stage Opamp due to relaxed headroom and better output swing, this chapter discusses the proposed work on gain boosting technique for folded cascode Opamp. FVF assisted differential pair based gain boosting technique is explained which extracts the signal and injects it onto the gate of the folding devices and hence contribute to gain. In addition to the gain contribution, noise contribution of folding transistors is also reduced with the proposed technique. The proposed FC Opamp is implemented in 28nm TSMC CMOS technology and post-layout simulation results are also performed. The proposed Opamp achieves 68 dB DC gain, which is 18 dB higher as compared to the implemented conventional FC Opamp. Circuit exhibits 20% improvement in the input-referred noise with the same power consumption of the conventional one. Further, the circuit consumes 33μW of power from a 1V power supply and occupies a 78x46 μm^2 silicon area. Table 6.1 shows the comparison of the proposed work with state of the art. It can be concluded from the table that proposed circuit is very much energy efficient even with the higher loading.

Chapter 7

A 2-4 GHz Low Jitter Frequency Synthesizer

7.1 Introduction

A circuit known as a clock generator creates the timing or clock signal needed by sequential circuits to operate. Depending on the situation, the circuit may generate a square wave or any other complex signal. Microprocessors can employ a PLL as a clock generator. When the PLL is programmed to lock with the required clock frequency, even if the reference signal changes due to distortions, it will automatically detect the changes and produce an output that is always equal to the required clock frequency. Therefore, this chapter discusses the implementation of a 2-4 GHz PLL as a clock generator for wire-line applications. In section 7.2, each component of PLL is discussed with its architecture, implementation, and performance. Finally, Section 7.3 explains the simulation results and Section 7.4 summarizes the chapter.

7.2 Implementation of PLL Components

This section discusses the design of each component along with their performance.

7.2.1 Top level architecture

Two major architectures are available for frequency synthesizers, an integer-N, and a fractional-N. Integer architecture is the simplest architecture that allows the output frequency to be changed in multiples of the reference frequency, maintaining channel spacing of reference. However, due to limitations on bandwidth for stability criteria, it suffers from spurious tones and a longer settling time. As the wire-line standard does not have very stringent requirements on spurs and settling time, an Integer-N type PLL architecture is adopted for the implementation.

As shown in Figure 7.1, the synthesizer consists of a phase frequency detector, charge pump, low pass filter, a Voltage controlled oscillator, and a multi-modulus divider. A 20 MHz reference

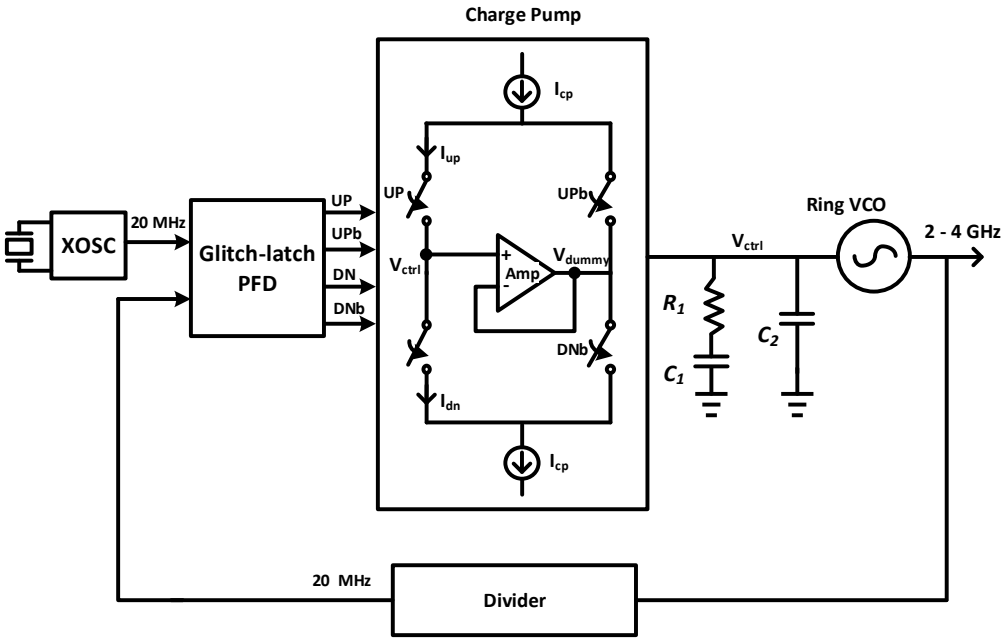


Figure 7.1: Top level block diagram of the implemented 2.4 GHz PLL

frequency is chosen for the synthesizer. Conventional glitch-latch PFD has been used, along with a single ended charge pump which has differential current steering. VCO consists of two parts, a voltage-to-current converter (V2I) and a current controlled oscillator (CCO). The 8-bit multi-modulus prescaler is implemented using programmable dual-modulus prescaler units. Due to the high speed operation of the divider, the first stage is adopted from the proposed 2/3 prescaler discussed in chapter 3 which used Pulse Extension logic (PEL). In the chain, 7 stages of 2/3 prescaler cells are connected like a ripple counter to cover the full range of division from 2 GHz to 4 GHz [134].

A conceptual block diagram of the implemented voltage controlled oscillator is shown in Figure 7.2 (a). It consists of voltage to current converter (V2I) and a current controlled oscillator (CCO) [135, 136]. V2I takes voltage V_{ctrl} as input and generates current I_{ring} for the CCO and controls its output frequency.

Circuit level implementation of the voltage to current converter is shown in Figure 7.2 (b). Transistors M_3-M_7 form a current mirror circuit that mirrors the drain current of transistor M_3 to I_{ring} based on the ratio of transistor M_3 and M_7. For better current matching, cascode current mirror is implemented so that the drain voltage of M_7 can follow the drain of M_5[40]. An additional branch with transistors M_1-M_2 generates bias voltage V_{casc_bias} for cascode transistors M_4 and M_6. Since whole circuit works as a gain stage for VCO, the sizing of transistors is kept such that all the transistors work in the saturation region only.

Figure 7.2 (c) shows the circuit of the current controlled oscillator. It consists of 5-inverter stages connected in feedback, a buffer stage to isolate the frequency generations transistors from the loading effect, and one rail-to-rail converter stage which makes the swing of CCO output phases rail-to-rail. The whole circuit receives input current I_{ring} from V2I which decides the switching

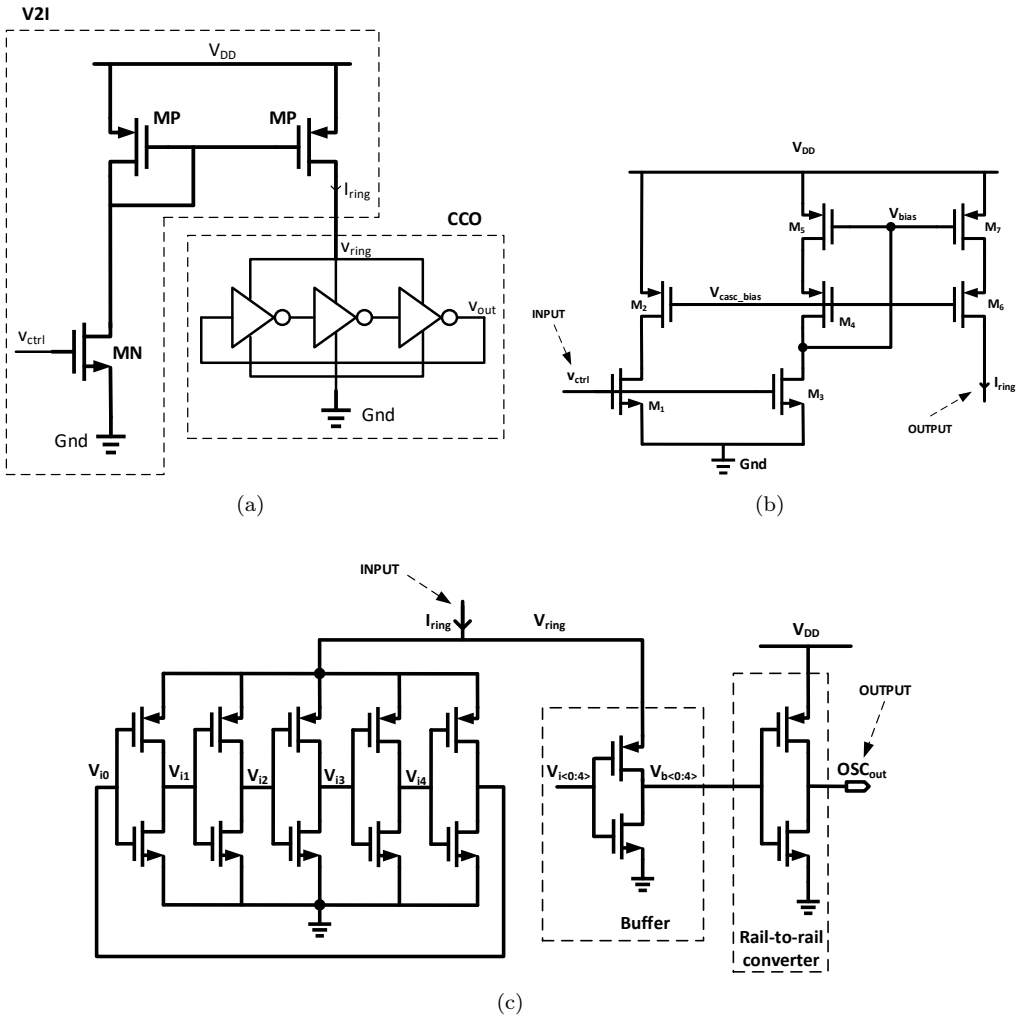


Figure 7.2: (a) Conceptual block diagram of VCO (b) Schematic of voltage to current converter (c) Schematic of current controlled oscillator

speed of each inverter and therefore controls the oscillation frequency. Output phases of 5-inverters V_{i0}-V_{i4} are sent to an inverter stage which serves as a buffer. It prevents the frequency generating stages from loading variation effect due to Process Voltage and Temperature (PVT). Since voltage node V_{ring} varies with V_{ctrl}, rail-to-rail output can't be achieved from the inverter chain. Therefore, the output of buffer stages V_{b0}-V_{b4} are send to inverter stages with a supply of V_{DD} as shown in Figure 7.2 (c).

Figure 7.3 shows the output frequency of the VCO as a function of its control voltage V_{ctrl}. It is also seen that the V_{ctrl} and output frequency vary linearly for a range of 1.8 GHz to 4.5 GHz while V_{ctrl} varies from 0.8V to 1.3V.

The phase noise plot of the VCO is shown in Figure 7.4 which shows the simulated phase noise across worst case corner. From the graph, the worst case phase noise at 1 MHz offset frequency is -90.58 dBc/Hz when VCO is operating at 2 GHz frequency.

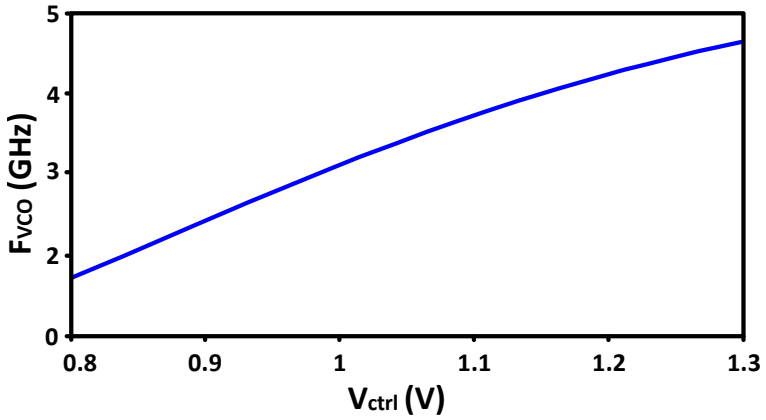


Figure 7.3: Output frequency of VCO as a function of control voltage

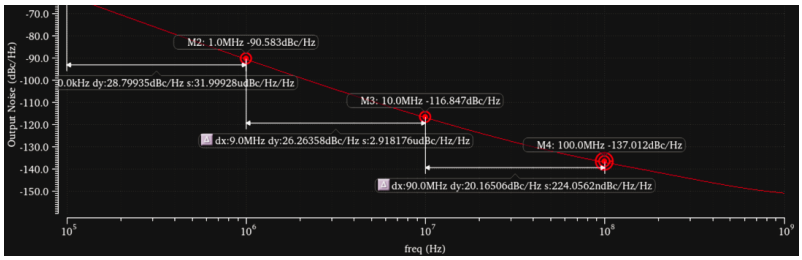


Figure 7.4: Simulated open loop phase noise of the VCO

7.2.2 Loop Filter(passive implementation)

Second order low pass filter is commonly used in PLLs. When PLL is in locked condition, linear model can be used to derive the transfer function of the PLL loop. Figure 7.5 shows the second order loop filter and its transfer function can be is given as

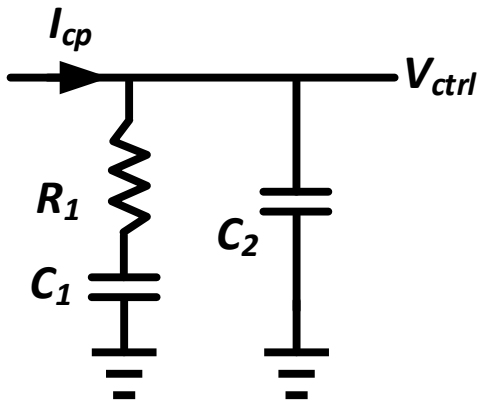


Figure 7.5: Second order passive loop filter

$$L(s) = \frac{s + \frac{1}{R_1 C_1}}{C_2 s \left(s + \frac{1}{R_1 \frac{C_1 C_2}{C_1 + C_2}} \right)} \tag{7.1}$$

Therefore, the open loop transfer function of the implemented type-II third order PLL shown

in Figure 7.1 can be written as

$$H_O(s) = \frac{K_{VCO} I_{CP}}{2\pi N} \frac{s + \frac{1}{R_1 C_1}}{C_2 s^2 \left(s + \frac{1}{R_1 \frac{C_1 C_2}{C_1 + C_2}} \right)} \tag{7.2}$$

Frequencies of the zero and pole locations of the (7.2) PLL are given by

$$\omega_z = 1/R_1 C_1 \tag{7.3}$$

$$\omega_{p1} = 0, \qquad \omega_{p2} = 0, \qquad \omega_{p3} = \frac{1}{R_1 \frac{C_1 C_2}{C_1 + C_2}} \tag{7.4}$$

Phase of the open loop transfer function in (7.2) can be written as -

$$\angle H_O(s) = -\pi + \arctan\left(\frac{\omega}{\omega_z}\right) - \arctan\left(\frac{\omega}{\omega_{p3}}\right) \tag{7.5}$$

From the above equation, phase margin which is angle contribution of both the zero and poles at unity gain frequency can be written as

$$\Phi_M = \arctan\left(\frac{\omega_{ugb}}{\omega_z}\right) - \arctan\left(\frac{\omega_{ugb}}{\omega_{p3}}\right) \tag{7.6}$$

From the bode plot shown in Figure 7.6, it is observed that the phase lag due to the third pole ω_{p3} nearly cancels the phase lead introduced by the zero ω_z around relatively flat portion in the phase plot. The maximum phase margin can be calculated by equating the first derivative of (7.6) to zero. It can be shown that the maximum phase margin occurs when

$$\omega_{ugb} = \omega_z \sqrt{\frac{C_1}{C_2} + 1} \tag{7.7}$$

Substituting the ω_{ugb} from above equation into the phase margin expression in (7.6), we get the following

$$\Phi_M = \arctan\left(\sqrt{\frac{C_1}{C_2} + 1}\right) - \arctan\left(\frac{1}{\sqrt{\frac{C_1}{C_2} + 1}}\right) \tag{7.8}$$

$$C_1 = 2C_2 \left(\tan^2 \Phi_M + \tan \Phi_M \sqrt{\tan^2 \Phi_M + 1} \right) \tag{7.9}$$

Equations (7.8) and (7.9) describes the relationship between the two capacitors and phase margin. Since a single PLL can't serve every applications therefore every application has different specification for their embedded frequency synthesizer. The loop bandwidth and phase margin are the two parameters governed by the application. For a given loop bandwidth and phase margin, all variables present in (7.8) or (7.9) can be calculated.

There is a trade-off between charge pump current I_{cp}, area of the loop filter, and noise contribution of loop resistance and charge pump. Lower I_{cp} leads to a larger resistance value, relaxing

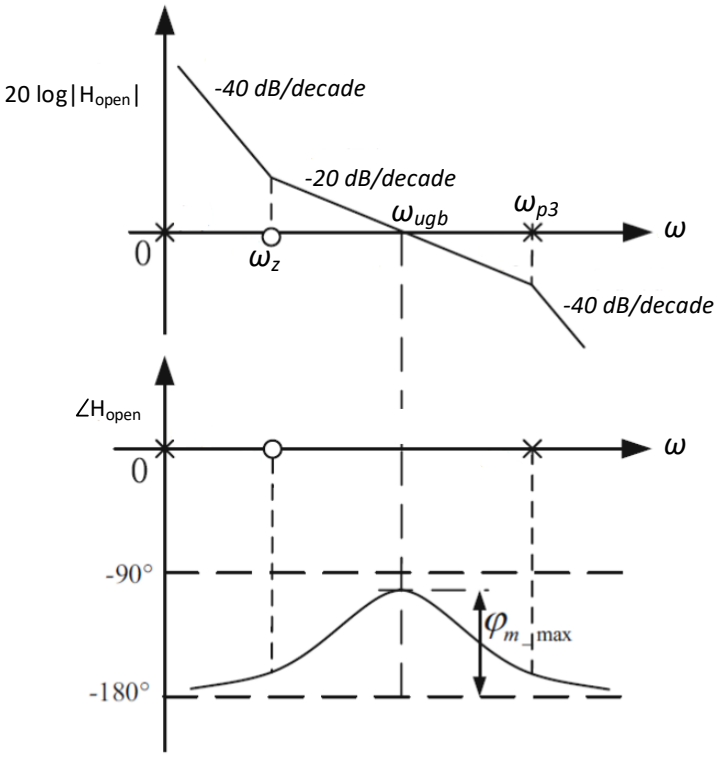


Figure 7.6: Schematic of low current mismatch charge pump

the capacitance sizes which results in a lower area of the loop filter. But lower charge pump current requires larger loop resistance which increases noise contribution by resistance and charge pump noise also gets increased. Since phase noise requirements for wire-lines applications are not stringent, for the implemented integer-N PLL, with a 100μA charge pump current, a tolerable value of resistance is found to be 9.1 kΩ which led to capacitors of 70pF and 4pF.

7.2.3 Charge Pump

Schematic of the charge pump is shown in Figure 7.7. A single ended charge pump is used with differential current steering to reduce the current mismatch. Transistor M_1-M_6 form the current mirror circuit to generate bias voltages CP_{nbias} and CP_{pbias}. Transistors M_4 and M_6 work as a current source to produce I_{up} and I_{dn} currents, respectively. Switches S_1-S_4 and amplifier (Amp) connected in unity gain feedback helps to perform the differential current steering mechanism. When UP is high, switch S_1 gets closed and charges the node V_{ctrl} whereas when DN is high, switch S_2 gets closed and discharges the V_{ctrl}. During the time when UP is low (UPb is high) switch S_1 goes OFF, switch S_3 turns ON which forces V_{ctrl} to follow V_{dummy} and resolves the charge sharing issue. Similar mechanism happens when DN is low (DNb is high), switch S_2 goes OFF, switch S_4 helps V_{ctrl} to maintain its voltage level till the time either S_1 or S_2 gets turned ON.

Since Opamp needs to support the same amount of current as I_{up} or I_{dn}, NMOS input differential pair is used as an amplifier for this charge pump in which transistor M_2 works as tail current

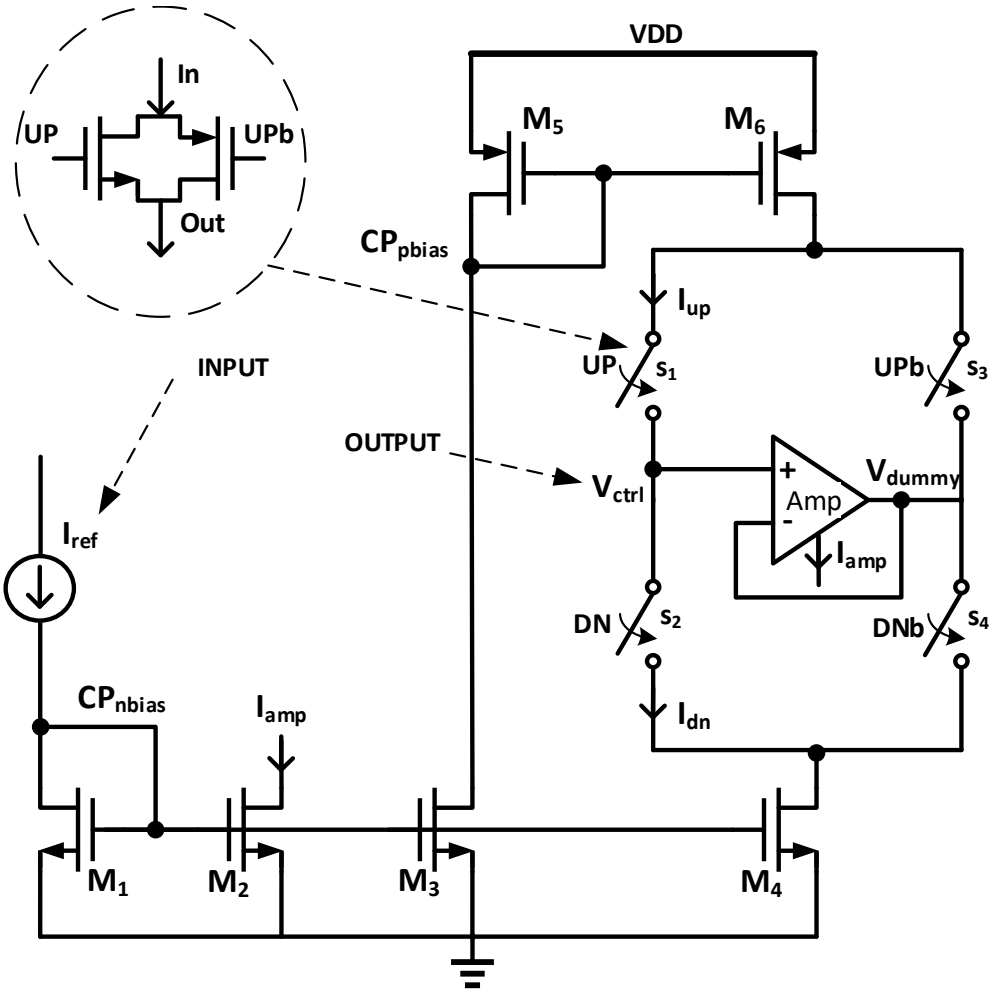


Figure 7.7: Schematic of the charge pump

source device. Figure 7.7 shows the transmission gate based switches which are adopted due to their almost constant resistance.

7.2.4 PFD

Schematic of the implemented glitch-latch based PFD is shown in Figure 7.8. Instead of using DFFs, this PFD consists of pulsed latches for faster acquisition rate [137, 138]. When the rising edge of Ref_{clk} comes, it generates a small pulse width Ref_{pulse}. Since node Resetb is high initially, transistor M_2 is turned ON which sets node V_x to low and output UP to high. As soon as the rising edge of the other input $Fdiv_{clk}$ comes, node $Fdiv_{pulse}$ turns ON transistor M_2. Because of direct path to ground, node V_y goes to low and output DN becomes high. Since both V_x and V_y are in low logic stage, it triggers reset of the whole circuit by switching node Resetb from high to low.

A major advantage of this architecture is that as long as Ref_{pulse} remains high, information of rising edge of Ref_{clk} passes to output even during reset time period. Same is true for input $Fdiv_{clk}$ and pulse signal $Fdiv_{pulse}$. It implies that glitch-latch based PFD does not miss the rising edge of inputs even during reset time period.

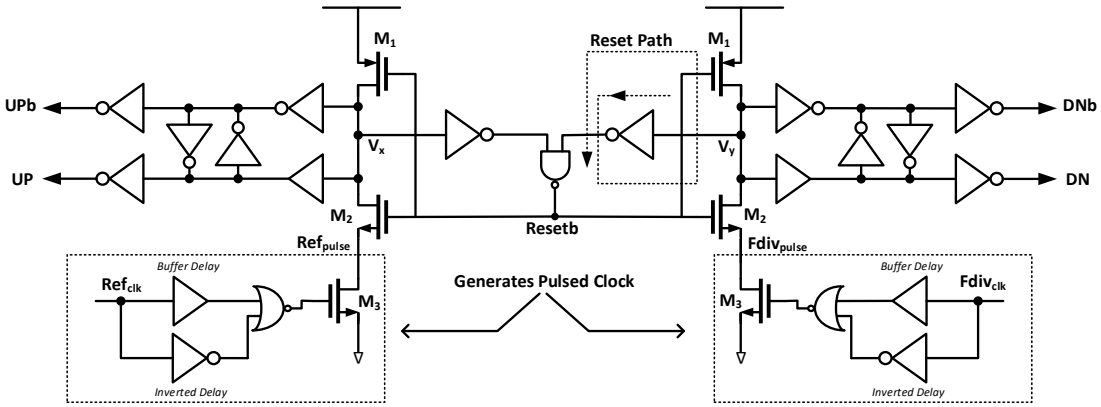


Figure 7.8: Schematic of glitch latch based PFD

7.2.5 Loop Divider

A 7-bit multi modulus programmable divider is implemented as shown in Figure 7.9. In any frequency divider, its first stage operates at the highest frequency of the PLL as it receives input directly from VCO. Therefore, instead of using standard 2/3 prescaler, first stage of the divider uses the proposed 2/3 dual modulus prescaler which has been discussed in Chapter 3. The rest of the cells in divider chain are standards Vaucher's 2/3 cells. Mod_{in} of the last cell is kept at logic high to enable dual modulus division of each 2/3 cell.

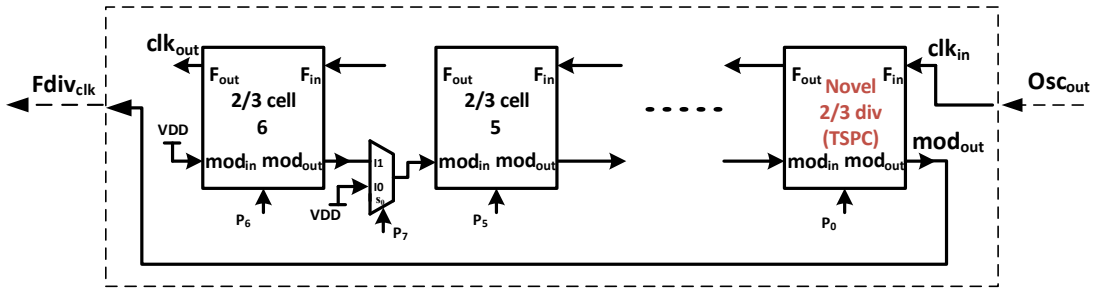


Figure 7.9: Schematic of 7-bit multimodulus divider

7.3 Performance of Implemented PLL

All the sub-blocks of PLL are implemented using $0.18\mu m$ technology. It is observed that charge pump phase noise dominates before the loop bandwidth whereas VCO phase noise dominates after the loop bandwidth frequency. The implemented PLL achieves decent phase noise of -90dBc/Hz and 1-σ phase jitter of 3.2ps at 1MHz offset frequency. Table 7.1 summarizes the specifications of implemented PLL.

7.4 Summary

This chapter presents the implemented 2-4 GHz Phase Locked Loop for wire-line applications. Design methodology is explained along with the working of each sub-block. Simulation results

Table 7.1: Summary of performance parameters of the implemented PLL

Parameter	**Value**
Process (μm)	0.18
Frequency (GHz)	2 - 4
Reference (MHz)	20
Phase Noise (dBc/Hz)	-90 @1MHz
Phase Jitter at 1MHz (ps)	3.2
Phase Jitter at 10MHz (ps)	0.8
Power Consumption (mW)	17.6

*Phase noise and jitter numbers are shown when PLL is locked at 2 GHz frequency

including frequency range, Phase noise and phase jitter of the PLL are summarized in Table 7.1. The synthesizer consumes 17.6mW power from a 1.8V supply. It achieves phase noise of -90dBc/Hz and Phase jitter of 3.2ps at 1 MHz offset frequency when PLL is locked at 2 GHz.

Chapter 8

Conclusion and Future Work

The objective of this thesis revolves around the development of low power sub-modules of an integer-N PLL based frequency synthesizer. Using the foundation of analog and digital circuit design, a fully integrated integer-N PLL is implemented using 180nm CMOS technology. The major contribution of the thesis has been on design of low power frequency dividers since they have significant power dissipation due to their highest frequency operation in a synthesizer. Apart from the divider, a few analog circuit topologies such as PVT insensitive VCO and gain boosted folded cascode Opamp are also described that have helped to achieve better performance of PLL.

Chapter 2 explains the fundamentals of Phase locked loop based frequency synthesizers. Different architectures of the PLL are discussed such as type-I and type-II PLL. Divider driven architectures like integer-N and fractional-N PLL are also discussed. The basic architecture, its operation, and non-linearity are also touched upon for each component of a PLL. Then, the major performance indices are explained which helps to target synthesizer design for specific applications.

Chapter 3 discusses the fundamentals of a frequency divider that is used in the feedback path of a PLL. Various available architectures to support high speed and low power operation are discussed along with their drawbacks. Then the proposed dual modulus 2/3 technique is explained which uses Pulse Extension Logic and one DFF for 2/3 prescaler to reduce the power consumption significantly. A novel 8/9 dual modulus prescaler design is discussed which used the Pulse Extension Logic to switch between divide-by-8 and divide-by-9 mode. The proposed prescaler is implemented in 180nm CMOS technology with 1.8V power supply. The implemented 8/9 prescaler's power dissipation is 1.9 mW when being operated at input frequency of 5.5 GHz.

In Chapter 4, different architecture for frequency dividers are discussed which can support 50% duty cycle for the output signal. It is observed that the dividers chain based on Vaucher's 2/3 prescaler is incapable of providing 50% duty cycle out signal. Other dividers targeting 50% duty cycle used external logic to achieve close to 50% duty cycle at the cost of extra power consumption. A novel multi modulus divider is discussed which does not require any external logic and can achieve close to 50% output duty cycle. The proposed 2-to-7 multi modulus divider is implemented in 180nm CMOS technology which can operate up to 5 GHz of input frequency and

draws 6.5 mW power from 1.8V power supply.

In Chapter 5, fundamentals of ring oscillators are reviewed and its sensitive to Process Voltage and Temperature is investigated. Numerous available architecture to mitigate the PVT variation on ring oscillators are also discussed along with their drawbacks. It is found that the most of the proposed techniques have used square low to get to the solution for making PVT insensitive VCO which is not very promising for advanced technologies as transistor current equation doesn't follow the square-low. This investigation has helped to propose a novel constant transconductance bias technique which used Opamp based negative feedback to counter the PVT variation in a ring oscillator. The proposed biasing technique is implemented in 65nm CMOS technology which draws 2.4 mW power consumption from a 1V supply.

In Chapter 6, design technique of conventional Folded Cascode (FC) Opamp is discussed. It is observed that an PMOS present in the second branch does not contribute to the Opamp's gain but degrades the noise performance of FC Opamp. Therefore, a novel technique of gain boosting is proposed to exploit the transconductance of the transistor which does not participate in gain enhancement and rather increases the overall noise. The proposed technique uses the Flipped Voltage Follower (FVF) concept to implement the novel gain boosted folded cascode Opamp architecture. The proposed FC Opamp is implemented in 28nm CMOS technology with 1V power supply. It exhibits around 20% improvement in the input referred noise and achieves 68dB gain while driving 10pF load capacitance.

In Chapter 7, a fully integrated 2-4 GHz integer-N PLL based frequency synthesizer as clock generator for wire-line applications is demonstrated. This PLL is implemented in 180nm CMOS technology with 1.8V power supply. It used a ring oscillator along with a voltage to current converter as a VCO which saves significant area and power as compared to LC tank structure. The designed VCO achieves 1.8 GHz to 4.5 GHz of oscillation frequency range with tuning voltage varying from 0.8V to 1.3V. A glitch latch PFD is adopted for phase and frequency comparison whereas single ended charge pump structure with Opamp is used. PLL employs the 7-bit multi modulus divider which comprises of 7 Vaucher's 2/3 prescaler and first stage as novel 2/3 prescaler with Pulse Extension Logic as discussed in Chapter 3. The whole synthesizer consumes total power of 17.6 mW.

8.1 Limitations and Future Work

We have presented a generic framework for the low-power high speed frequency dividers and PVT insensitive bias technique for oscillators. However, there are some limitations and future courses of action can be used to overcome these limitations and further improve the quality of the proposed work. In this concern, some of the salient points are as follows:

1. In this thesis, we have only considered the TSPC logic to implement low power high speed frequency dividers due to their less short circuit current. The proposed modulus divider architecture with Pulse Extension Logic is not suitable for higher division as the series con-

nection of NMOS in the first stage of 2/3 will face overdrive voltage issue. A modulus divider for a higher division can be proposed.

2. The proposed constant transconductance bias technique requires Opamp which is power extensive and resistance which has PVT variation associated with it. An improved technique can be proposed with a low power amplifier which does not include passive elements.

3. The proposed 2-to-7 modulus divider supports divide-by-2 as a minimum division factor. There is a scope of adding divide-by-1 or divide-by-0.5 to it without increasing the power dissipation of the present design.

4. Only biasing technique is proposed for PVT insensitive VCO. Since there isn't much literature available on PVT insensitive PLLs, architecture for PVT insensitive PLL can be explored.

5. The main focus of the thesis is the development of low-power high-frequency dividers for low-power synthesizers. Due to the lack of a frequency divider in the feedback loop, sub-sampling PLL architecture has recently become one of the most promising architectures for low power improved phase noise performance PLL. It is possible to suggest new designs for low-power frequency synthesizers without sacrificing the phase noise performance because there is a lot of room for research in this architecture.

Finally, we can conclude that the intended objectives of designing low-power CMOS integrated circuits for Phase Locked Loop frequency synthesizers have been successfully achieved.

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List of publications/patents

(A) Publications from PhD thesis work

A1. In refereed Journals:

1. **R. Kumar**, P. Bohara, K. Thakur, S. K. Vishvakarma, "A 5.5 GHz 1.9 mW Low Power 8/9 Dual Modulus Divider in 180nm CMOS Technology," *Journal of Circuits, Systems, and Computers*, 32(04) (2023) p. 2350068. DOI: 10.1142/S0218126623500688.

2. **R. Kumar**, R. Nagulapalli, S. K. Vishvakarma, "A Novel Bias Circuit Technique to Reduce the PVT variations in Ring Oscillator using 65nm CMOS Technology," *Journal of Circuits, Systems, and Computers*, 32(04) (2023) p. 2350059. DOI: 10.1142/S0218126623500597.

3. **R. Kumar**, R. Sharma, R. Nagulapalli, S. K. Vishvakarma, "A 5 GHz 6.5 mW 2-to-7 Modulus Programmable Prescaler with 50% Output Duty Cycle." (About to submit).

A2. In refereed conferences:

1. **R. Kumar**, R. Nagulapalli, S. K. Vishvakarma, "A Novel Gain Enhanced Folded Cascode OPAMP in 28nm CMOS technology," International Conference on Electrical, Computer and Energy Technologies (ICECET), Czech Republic, 2022, pp. 1-4. DOI: 10.1109/ICECET55527.2022.9872766.

2. **R. Kumar**, R. Nagulapalli, R. Hake, S. K. Vishvakarma, "A Low-Power 2-to-7 Modulus Programmable Prescaler with 50% Output Duty Cycle," International Conference on Electrical, Computer and Energy Technologies (ICECET), Czech Republic, 2022, pp. 1-5. DOI: 10.1109/ICECET55527.2022.9873078.

(B) Patents from PhD thesis work

1. **R. Kumar**, R. Nagulapalli, S. K. Vishvakarma, " Constant transconductance bias Device," *Indian Patent*, Application no. 202221042164. (Filed)

(C) Other publications during PhD

C1. In refereed Journals:

1. M. Kumawat, A. Dalal, M. S. Choudhary, **R. Kumar**, G. Singhand S. K. Vishvakarma,"Wave Combining Driver Based Serial Data Link Transceiver Design for Multi-Standard Applications," *Journal of Nanoelectronics and Optoelectronics*, Volume 14, Number 5, May 2019, pp. 675-679 (5).

2. M. Kumawat, A. K. Upadhyay, S. Sharma, **R. Kumar**, G. Singh and S. K. Vishvakarma," An Improved Current Mode Logic Latch for High Speed Applications," *International Journal of Communication Systems*, Volume 33, Issue 13, Sep 2020.

3. M. Kumawat, M. S. Choudhary, **R. Kumar**, G. Singh and S. K. Vishvakarma, "A Novel CML Latch Based Wave Pipelined Asynchronous SerDes Transceiver for Low Power Application," *Journal of Circuits, Systems and Computers*, Volume 29, Issue 7, June 2020.

(D) Other patents during PhD

1. **R. Kumar**, R. Geetla, D. Jain, G. Agrawal, " High-Speed Multi-phase Digital Frequency Synthesizer for Clocking Applications," *US Patent US20240088879A1.*

2. **R. Kumar**, D. Jain, K. Thakur, G. Agrawal, " Circuitry and Method for Fractional Division of High-Frequency Clock Signals," *US Patent US20230126891A1.*