B. TECH. PROJECT REPORT

On

Modeling RRAM for Image Processing Applications

BY

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Modeling RRAM for Image Processing Applications

A PROJECT REPORT

Submitted in partial fulfillment of the
requirements for the award of the degrees

of
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in
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Submitted by:
Sandeep Meena (150002030)

Guided by:
Dr. Shaibal Mukherjee

INDIAN INSTITUTE OF TECHNOLOGY INDORE
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CANDIDATE'S DECLARATION

We hereby declare that the project entitled **"Modeling RRAM for Image Processing Applications"** submitted in partial fulfillment for the award of the degree of Bachelor of Technology completed under the supervision of **Dr. Shaibal Mukherjee, Associate Professor,** Discipline of Electrical Engineering, IIT Indore is an authentic work.

Further, I declare that I have not submitted this work for the award of any other degree elsewhere.

Signature and name of the student with date

_____

CERTIFICATE by BTP Guide

It is certified that the above statement made by the students is correct to the best of my/~~our~~ knowledge.

Signature of BTP Guide with dates and designation

Preface

This report on **"Modeling RRAM for Image Processing Applications"** is prepared under the guidance of Dr. Shaibal Mukherjee, Associate Professor, Discipline of Electrical Engineering, IIT Indore.

Through this report we have tried to study the modeling of RRAM and effect of thickness, states and time on Current-Voltage characteristics in RRAM.

We have tried our best to explain this content to a reader in a lucid manner with comprehensive theory. We have added photographs and experimental results to make it more illustrative.

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I wish to thank Dr. Shaibal Mukherjee for his kind support and valuable guidance. Throughout the project he has been available for all my queries and doubts, he has also facilitated with an environment to think independently and encouraged to my ideas. I would also like to thank Mr. Mangal Das and Mr. Amitesh Kumar for their special guidance and kind support. It is their help and support, due to which I am able to complete the design and technical report.

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Abstract

Resistive Random Access Memory (RRAM) is a promising candidate for future memory due to its high-efficiency, high speed and energy-saving characteristics. In recent years, continuous improvement and in-depth investigation in both materials and electrical switching mechanisms have not only lead to a breakthrough in the performance of digital non-volatile memory (NVM), but also lead to other possible memory functionality. In this work, we provide a comprehensive discussion on the model proposed for the design and description of resistive random access memory (RRAM), and effect of time, thickness, on state resistance and state of device on the current–voltage hysteresis.

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CHAPTER 1

Introduction of RRAM

1.1 RRAM

The term Resistive Random Access Memory (RRAM) is the most promising candidate for next generation memory due to its advantages in both working memory and main memory. Like working memory, RRAM has very low operation voltage and power, extremely fast write/erase speeds, and great reliability. Like main memory, RRAM is non-volatile, and has great storage capacity. Moreover, due to the excellent compatibility with integrated circuit (IC) processes and scaling capability, RRAM has great potential for production and commercialization. In RRAM device research, using the via hole type structure in the manufacturing process to clarify the physical mechanism and electrical measurements is preferable. Moreover, such a structure can eliminate the problem of film uniformity and is more reliable for the analysis of reliability and mechanism. Furthermore, due to the scaling capability, 1R-RRAM is very practical for main memory.

For the manufacturing process of 1R-RRAM, the devices are simple two-terminal metal-insulator-metal (MIM) structure. the bottom electrode is deposited and patterned by a lithography process first. Then, the insulator layer is deposited, and a lithography process is used to pattern the cell size and active region via hole. After that, the switching layer is grown by using a chemical vapor deposition (CVD) or physical vapor deposition (PVD) process. Finally, the top electrode is deposited and patterned by a lithography process. An as-prepared RRAM is in a highly resistive state. During the ‘forming’ process, conducting paths form in the switching layer by applying a high voltage stress as a soft breakdown, and the RRAM is switched into a low resistance state (LRS) RRAM in a LRS is switched to a high resistance state (HRS) by applying a ‘reset voltage’ reset process RRAM is switched from a HRS to a LRS by applying a ‘set voltage’ (set process). Red-ox reaction and/or anodization near the interface between the electrode and switching layer is widely considered to be the mechanism behind the formation and rupture of the conducting paths.
RRAM can be classified into two types with respect to the operating electrical polarity.

(1) **Non-polar:** where the switching procedure is independent of the polarity of the operating voltage. The physical mechanism of the Non-polar type is usually interpreted as the Joule heating effect, and thus the operating electrical polarity does not depend on the polarity of the operating voltage.

(2) **Bipolar:** where the set process and reset process must occur with opposite voltage polarities. In contrast, the mechanism of the bipolar type is usually regarded as the red-ox reaction and electrochemical migration. Hence, the operating electrical polarity is dependent on the polarity of the operating voltage.

We will classify RRAM into four parts with respect to the resistive switching mechanism.

(1) **Anion-type RRAM:** the mechanism of this type of RRAM is dominated by oxygen ions (negative charge).

(2) **Cation-type RRAM:** the mechanism of this type of RRAM is dominated by the redox reaction and migration of metal ions (positive charge), this type of RRAM is well-known in conductive bridge RAM (CBRAM).

(3) **Carbon based RRAM:** we will illustrate the switching mechanism and properties of carbon-based materials as the RRAM switching layer.

(4) **Oxide-based electrode RRAM:** Electronic modules have been expected to be renovated in order to possess multiple functionalities, such as portability, transparency, flexibility, and wearability.

To achieve a very high nonlinearity to fulfill the combination of fast switching and immunity the development of a general understanding of the electrochemical and physical processes that determine the switching kinetics of PCM, VCM and ECM.PCM, VCM, and ECM devices can be switched repetitively, between a high resistance state (HRS) and a low resistance state (LRS).

(1) **Phase Change Memories:** Phase change memory devices can be found on the pseudo-binary line between GeTe and Sb2Te3.During RESET the conductive crystalline phase change material is locally heated (via Joule heating) above the melting temperature and subsequently cooled down. This way, the atomically disordered liquid material is melt-quenched, resulting in an amorphous solid state. The RESET process is mainly controlled by the thermal time constant of a phase change memory cell and especially its surrounding rather than by the phase change material.

(2) **Electrochemical Metallization Memories:** In electrochemical cells it depends on the voltage regime, which mechanism is the rate-determining one for switching. While electro-crystallization dominates at low voltages, electron transfer in the medium voltage range and a mixture of electron transfer and ion migration at high voltages. ECM cells consist of one active silver or copper electrode, an ion conducting insulating layer and an inert electrode. ECM cells consist of one active silver or copper electrode, an ion insulating layer and an inert electrode.

(3) **Valence Change Memories:** In valence change materials, ion migration is found to be accelerated by a combined effect of electric field and local temperature increase due to Joule heating. It is widely accepted that the switching mechanism of VCM cells is based on the movement of oxygen ions in terms of a vacancy transport mechanism accompanied by a local valence change.

Leon Chua argued that all two-terminal non-volatile memory devices including RRAM should be considered memristors In Next Chapter we will study about memristor.

CHAPTER 2

Introduction of Memristor

2.1 Memristor

A resistor is defined by the relationship between voltage V and current i(dV= Rdi),the capacitor is defined by the relationship between charge q and voltage V (dq = Cdv), the inductor is defined by the relationship between flux ϕ and current i (dϕ = Ldi).,In addition, the current i is defined as the time derivative of the charge q and according to Faraday's law, the voltage V is defined as the time derivative of the flux ϕ.

Leon Chua compared the above model to that of Aristotle's theory of matter, according to this theory all matter consists of earth, water, air, and fire. Each of these elements exhibits two of the four fundamental properties of moistness, dryness, coldness, and hotness. From this theory he saw a striking resemblance and predicted the existence of the fourth kind of element and called it memristor.

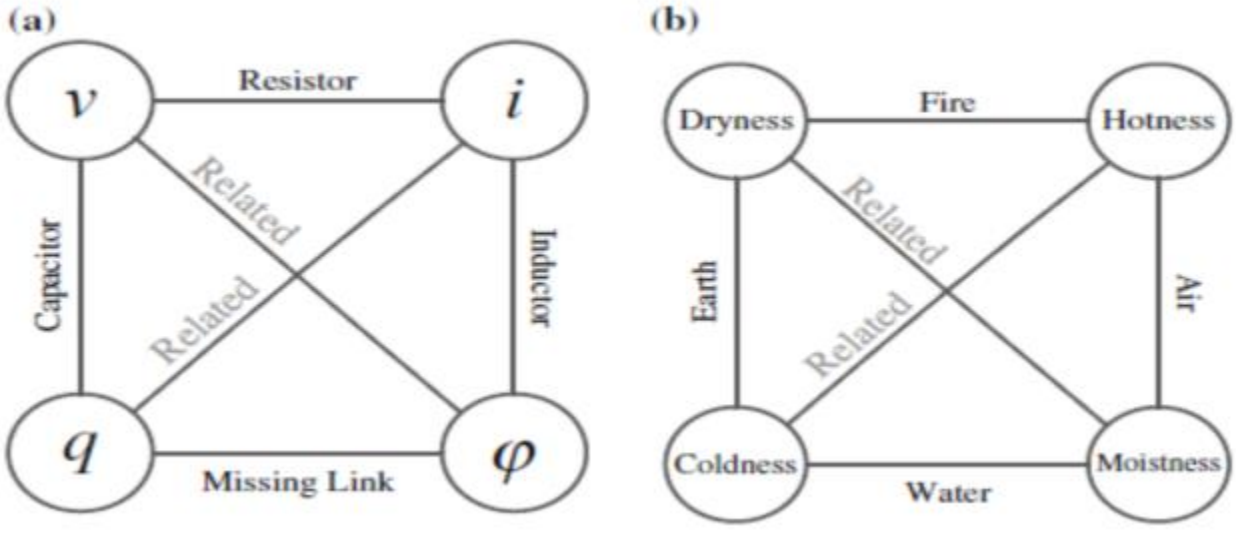

Figure.1 (a) The Relation Between Circuit Elements, (b) Aristotle's Theory of Matter.

2.2 Historical Background of the Mem-Element:

a. In 1960, Prof. Bernard Widrow of Stanford University developed a new circuit element called the memistor.

b. The memistor was a three-terminal device for which the conductance between two of the terminals was controlled by the time-integral of the current into the third terminal.

c. Memistors formed the basic components of the neural-network architecture called ADALINE (ADAptive LInear NEuron).

d. Later, it was proved that the memistor and memristor are different devices.

e. In 1971, Leon Chua mathematically predicted that there is a fourth fundamental circuit element characterized by a relationship between charge and flux linkage.

f. In 2008, the memristor in device form was developed by Stanley Williams and his group in the Information and Quantum Systems (IQS) Lab at HP.

It is well known that the four main fundamental circuit variables are current 'i' , voltage 'V', charge 'q', and flux 'ϕ', For linear elements, f (V, i) = 0, f (V, q) = 0, f (ϕ, i) = 0 .Prof. Leon Chua predicted mathematically that there is a device representing the missing relation characterized by g(ϕ, q) = 0 which he named the memristor,so we can say memristor is a 2-terminal circuit element characterized by a *constitutive relation* between two mathematical variables q and ϕ representing the time integral of the element's current *i(t),* and

voltage *v(t)*; namely,

$$q(t) \triangleq \int_{-\infty}^{t} i(\tau)\, d\tau \tag{1}$$

$$\varphi(t) \triangleq \int_{-\infty}^{t} v(\tau)\, d\tau \tag{2}$$

It is important to stress that "q" and "ϕ" are defined mathematically and need not have any physical interpretations. Nevertheless, we call q the charge and ϕ the flux of the memristor coincide with the formula relating charge to current, and flux to voltage, respectively. We say the memristor is charge-controlled, or flux-controlled if its constitutive relation can be expressed by

$$\varphi = \hat{\varphi}(q) \tag{3}$$

or

$$q = \hat{q}(\varphi) \tag{4}$$

Respectively, where $\phi\hat{}(q)$ and $q\hat{}(\phi)$ are continuous and piece wise-differentiate functions with bounded *slope*. Differentiating above equation with respect to time (t), we obtain

$$v = \frac{d\varphi}{dt} = \frac{d\hat{\varphi}(q)}{dq}\frac{dq}{dt} = R(q)I \tag{5}$$

where

$$R(q) = \frac{d\hat{\varphi}(q)}{dq} \tag{6}$$

R(q) is called the memristance at q, and has the unit of Ohms (Ω), and

$$i = \frac{dq}{dt} = \frac{d\hat{q}(\varphi)}{d\varphi}\frac{d\varphi}{dt} = G(\varphi)v \tag{7}$$

Where

$$G(\varphi) = \frac{d\hat{q}(\varphi)}{d\varphi} \tag{8}$$

G(q) is called the memductance at ϕ and has the unit of Siemens (S).

2.3 Pinched hysteresis loop:

all memristors exhibit a distinctive “fingerprint” characterized by a pinched hysteresis loop confined to the first and the third quadrants of the v–i plane.The pinched hysteresis loop shrinks and tends to a straight line as frequency increases.

Consider the ideal memristor with unambiguous constitutive relation between the flux ϕ and the charge q

$$f(\varphi, q) = 0 \tag{9}$$

where

$$\varphi(t) = \int_0^t v(\tau)d\tau, q(t) = q_0 + \int_0^t i(\tau)d\tau \tag{10}$$

Here, ϕ_0 and q_0 are the initial flux and charge at time t = 0. The memristor will be driven by sinusoidal current i(t) with zero-dc level and with the repeating period T

$$i(t) = I_{max} \sin(\omega t) \tag{11}$$

where I_{max} and $\omega = 2\pi/T$ are the magnitude and angular frequency, respectively. The pinched v−i hysteresis loop is formed by two loops Γ_1 and Γ_1 and odd symmetric with respect to the origin. Their areas S and S can be computed vi integrals

$$S = \oint_{\Gamma_t} vdi \tag{12}$$

$$S' = \oint_{\Gamma_1'} vdi = -S \tag{13}$$

The area closed into the positively oriented loop, i.e., a loop drawn by the operating point in a counterclockwise direction, has the minus sign, and vice versa. Considering the odd symmetry of the complete loop $\Gamma=\Gamma 1 \cup \Gamma 1$, one can write

$$\oint_{\Gamma} vdi = 0 \tag{14}$$

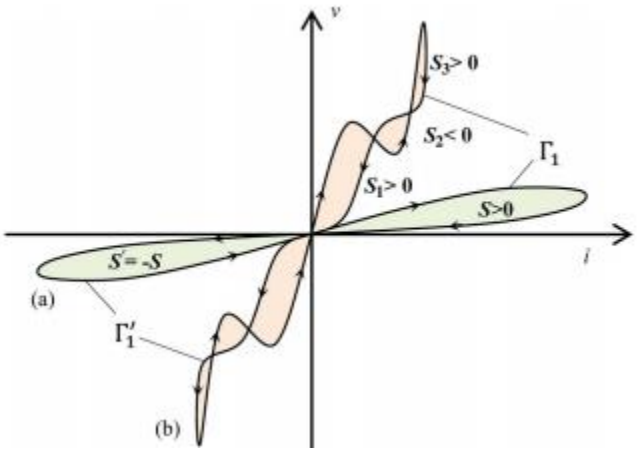

Fig.2 Examples of the PHLs of ideal memristors.

(a) Simple loop with coherent area S and (b) multiple-point loop with area S = S1 + S2 + S3.

2.4 Continuum of non-volatile memories:

If end is one opens or short circuits a memristor having a resistance R_0 at $t = t_0$ so that the memristor is in equilibrium.it's mean that the memristor does not lose the value of ϕ and q when both voltage v and current i become zero.So,if the power is switched off memristor holds unchanged value of q_0 and $\phi 0$.

Hence the passive memristor exhibits non-volatile memory.

An ideal memristor is therefore defined by State-dependent Ohm's law:

$$v = R(x)i \tag{15}$$

Memristor state equation:

$$i = dx/dt \tag{16}$$

The pinched loop itself is useless as a model since it cannot be used to predict the voltage response to arbitrarily applied current signals, and vice versa.

Hence Pinched hysteresis loops are not models

CHAPTER 3

Modeling of RRAM

A very important aspect of developing electronic devices based on new semiconductor technologies is the role of modeling. An accurate and comprehensive model is of paramount importance in understanding the device operation, designing it for optimum performance, and verifying that it matches the required specifications. A number of models have been proposed with varying degrees of accuracy, different features, and mixed results. So, any developer aiming to design a robust and flexible model for RRAM devices should have information about the methods tried before and the constraints faced.Models which introduced new features such as threshold effects taking filament gap as the state variable have been reviewed. Some of the models which account for unipolar devices and temperature effect are reviewed in detail. Also considered are physical models based on the device growth dynamics. Along with these, models considering only bipolar devices change of CF size and many other factors are taken into account.Schematic of conduction mechanism and relation between BLC and ELC.

3.1 Linear Ion Drift Model :

A simple two-terminal device was reported, where an oxide (Y_2O_3) of thickness D was sandwiched in between two Al electrodes. Hysteresis I-V switching curves have been compared with the simulated curve. Although the exact mechanism of these devices was not completely understood at that time, it was one of the first instances where resistive switching memories were classified into memristive systems.

A schematic device structure of Y_2O_3-based memristor is , where there are two variable resistances in series, called as R_{ON} which is the low resistance in the semiconductor region with higher dopant concentration. A lesser dopant concentration makes the other part higher in resistance, called as R_{OFF}. Relation between the applied voltage v(t) and current through the system i(t) owing to ohmic electronic conductance and linear ionic drift in a uniform field with average ion mobility is given by

$$V(t) = [R_{on}(w(t)/D) + R_{off}(1 - (w(t)/D))]i(t) \tag{17}$$

Although the equation above itself is non-linear, the resistance of the device linearly changes with the applied voltage v(t), thus the attribution of linearity to the model. Device acts as a perfect memristor for only a particular bounded range of the state variable w. The state variable is define u_v

$$dw/dt = u(R_{on}/D)\, i(t) \tag{18}$$

CHAPTER 4

Results and Conclusion

4.1 Experiments and Analysis:

Relation between the applied voltage v(t) and current through the system i(t) owing to ohmic electronic conductance and linear ionic drift in a uniform field with average ion mobility is given by the following equation

$$V(t) = [R_{on}(w(t)/D) + R_{off}(1 - (w(t)/D))]i(t)$$

Although the equation above itself is non-linear, the resistance of the device linearly changes with the applied voltage v(t), thus the attribution of linearity to the model. Device acts as a perfect memristor for only a particular bounded range of the state variable w. The state variable is defined

$$w(t) = (u_v * R_{on} * q)/D$$

All the parameters in above equation are define as

R_{off}	off state resistance	12000Ω
R_{on}	on state resistance	4000Ω
D	Thickness of memristive layer	60 nm
w(t)	State of device	0.5
u_v	Mobility of ion	1.6e-^{15} m^2 s^{-1} $volt^{-1}$

After plotting the Eq [17] with the help of Matlab we got a Hysteresis loop as current -voltage characteristics .

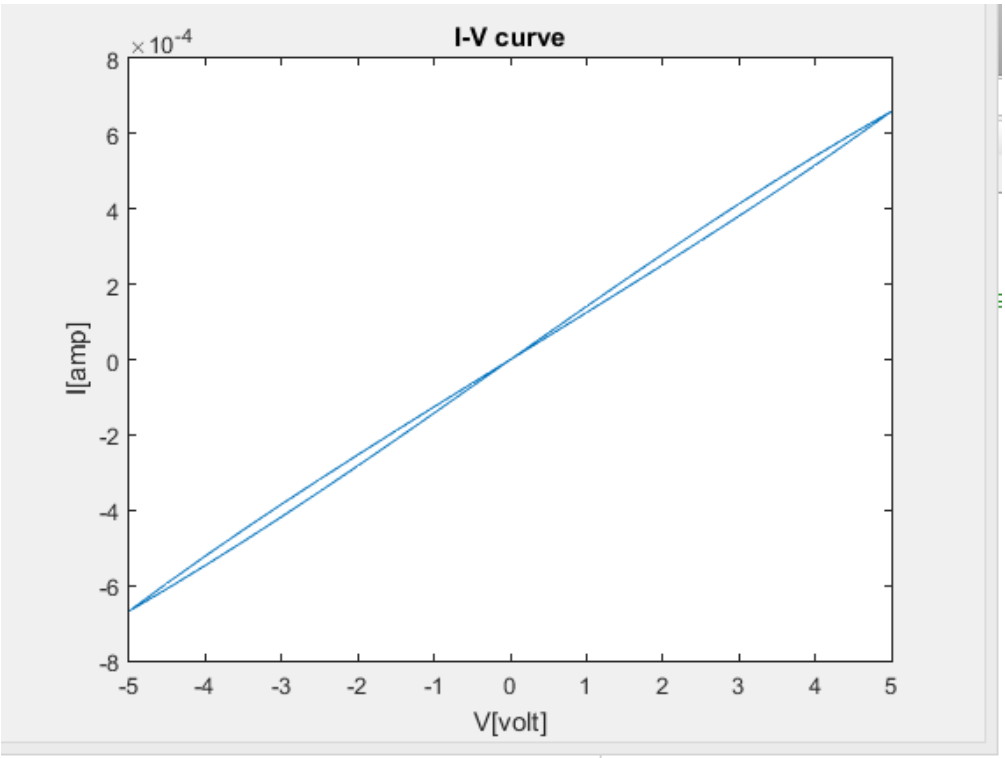

Fig.3 Current-Voltage characteristics

The Figure 3 has been taken as ideal Current-Voltage Characteristics for following excrement:

4.2 Results :

4.2.1 Effect of ramp-rate on resistive switching (RS) :

In Matlab, first we evaluate the data with time (t =10 ms) after that we evaluate the data with time (t = 30 ms) and we get some change in current-voltage characteristics,observations are following in Table.1

	A(X1)	It0.01(Y1)	voltae(X2)	It0.03(Y2)
Long N	Voltae	current	voltage	current
Units				
Comme	t = 0.01	t = 0.01	t = 0.03	t = 0.03
1	0	0	0	0
2	0.5	6.25E-5	0.5	6.25E-5
3	1	1.25143E-4	1	1.25429E-4
4	1.5	1.88143E-4	1.5	1.89446E-4
5	2	2.51724E-4	2	2.55266E-4
6	2.5	3.16115E-4	2.5	3.23695E-4
7	3	3.81561E-4	3	3.95686E-4
8	3.5	4.48326E-4	3.5	4.72417E-4
9	4	5.16698E-4	4	5.55393E-4
10	4.5	5.86997E-4	4.5	6.46624E-4
11	5	6.59581E-4	5	7.48903E-4
12	4.5	6.01249E-4	4.5	7.08783E-4
13	4	5.40777E-4	4	6.62368E-4
14	3.5	4.78277E-4	3.5	6.08774E-4
15	3	4.13895E-4	3	5.47143E-4
16	2.5	3.47808E-4	2.5	4.76759E-4
17	2	2.80223E-4	2	3.97201E-4
18	1.5	2.11377E-4	1.5	3.08545E-4
19	1	1.41533E-4	1	2.11569E-4
20	0.5	7.09736E-5	0.5	1.07897E-4
21	0	0	0	0
22	-0.5	-7.1078E-5	-0.5	-1.09007E-4
23	-1	-1.41947E-4	-1	-2.15771E-4
24	-1.5	-2.12297E-4	-1.5	-3.17198E-4
25	-2	-2.81828E-4	-2	-4.10877E-4
26	-2.5	-3.50257E-4	-2.5	-4.95312E-4
27	-3	-4.17323E-4	-3	-5.69915E-4
28	-3.5	-4.82791E-4	-3.5	-6.34842E-4
29	-4	-5.46456E-4	-4	-6.90748E-4
30	-4.5	-6.08145E-4	-4.5	-7.38564E-4
31	-5	-6.67717E-4	-5	-7.79313E-4
32	-4.5	-5.93234E-4	-4.5	-6.66003E-4
33	-4	-5.21375E-4	-4	-5.67538E-4
34	-3.5	-4.51728E-4	-3.5	-4.79702E-4
35	-3	-3.83932E-4	-3	-3.99681E-4
36	-2.5	-3.17668E-4	-2.5	-3.25488E-4
37	-2	-2.52648E-4	-2	-2.55652E-4
38	-1.5	-1.88608E-4	-1.5	-1.89038E-4
39	-1	-1.25306E-4	-1	-1.24726E-4
40	-0.5	-6.25098E-5	-0.5	-6.19414E-5
41	0	0	0	0

Table.1 Current-Voltage data with time (10 ms and 30 ms)

Now, we Plot the data from the Table.1

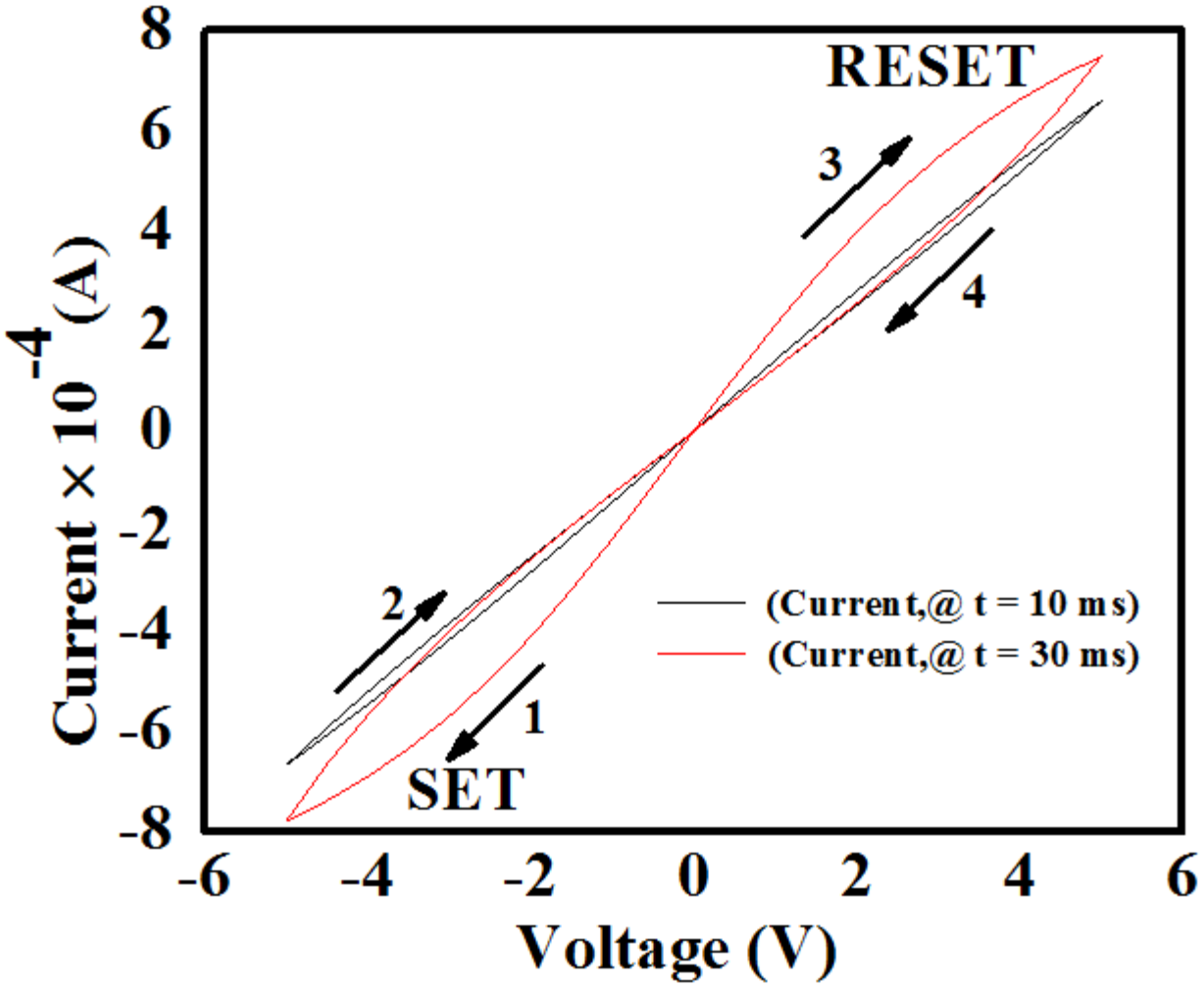

Fig.4 Effect of change in time on resistive switching (RS)

From this plot we observe that time plays an important role in the memristive effect in RS. In this model, when the parameter t increases from 10 ms to 30 ms, the switching voltage becomes lower, as shown in Fig. 4. On the contrary, the switching voltage would become higher when t decreases to 10 ms. By simulating, the feasibility of our device being applied in the memristive system is confirmed. For higher ramp-rate (dv/dt), the curve shrinks owing to memristive behavior.

4.2.2 Effect of thickness on resistive switching (RS):

In Matlab, first we evaluate the data with thickness (D = 60 nm) after that we evaluate the data with thickness (D = 40 nm) and we get some change in current-voltage characteristics,observations are following in Table.2

	A(X1)	ID40(Y1)	C(X2)	ID60(Y2)
Lo	voltae	current	voltage	current
Co	(D = 40)	(D = 40)	(D =60)	D = 60
1	0	0	0	0
2	0.5	6.25E-5	0.5	6.25E-5
3	1	1.25321E-4	1	1.25143E-4
4	1.5	1.88955E-4	1.5	1.88143E-4
5	2	2.53923E-4	2	2.51724E-4
6	2.5	3.20795E-4	2.5	3.16115E-4
7	3	3.90223E-4	3	3.81561E-4
8	3.5	4.62968E-4	3.5	4.48326E-4
9	4	5.39952E-4	4	5.16698E-4
10	4.5	6.22324E-4	4.5	5.86997E-4
11	5	7.11558E-4	5	6.59581E-4
12	4.5	6.62403E-4	4.5	6.01249E-4
13	4	6.08256E-4	4	5.40777E-4
14	3.5	5.48876E-4	3.5	4.78277E-4
15	3	4.84133E-4	3	4.13895E-4
16	2.5	4.14055E-4	2.5	3.47808E-4
17	2	3.38866E-4	2	2.80223E-4
18	1.5	2.59028E-4	1.5	2.11377E-4
19	1	1.75256E-4	1	1.41533E-4
20	0.5	8.852E-5	0.5	7.09736E-5
21	0	0	0	0
22	-0.5	-8.89774E-5	-0.5	-7.1078E-5
23	-1	-1.77035E-4	-1	-1.41947E-4
24	-1.5	-2.62851E-4	-1.5	-2.12297E-4
25	-2	-3.45252E-4	-2	-2.81828E-4
26	-2.5	-4.2329E-4	-2.5	-3.50257E-4
27	-3	-4.96282E-4	-3	-4.17323E-4
28	-3.5	-5.63813E-4	-3.5	-4.82791E-4
29	-4	-6.25717E-4	-4	-5.46456E-4
30	-4.5	-6.82035E-4	-4.5	-6.08145E-4
31	-5	-7.32965E-4	-5	-6.67717E-4
32	-4.5	-6.37211E-4	-4.5	-5.93234E-4
33	-4	-5.50129E-4	-4	-5.21375E-4
34	-3.5	-4.69706E-4	-3.5	-4.51728E-4
35	-3	-3.9445E-4	-3	-3.83932E-4
36	-2.5	-3.2321E-4	-2.5	-3.17668E-4
37	-2	-2.55072E-4	-2	-2.52648E-4
38	-1.5	-1.89284E-4	-1.5	-1.88608E-4
39	-1	-1.25209E-4	-1	-1.25306E-4
40	-0.5	-6.2284E-5	-0.5	-6.25098E-5
41	0	0	0	0

Table.2 Current-Voltage data with thickness (40 nm and 60 nm)

Now, we Plot the data from the Table.2

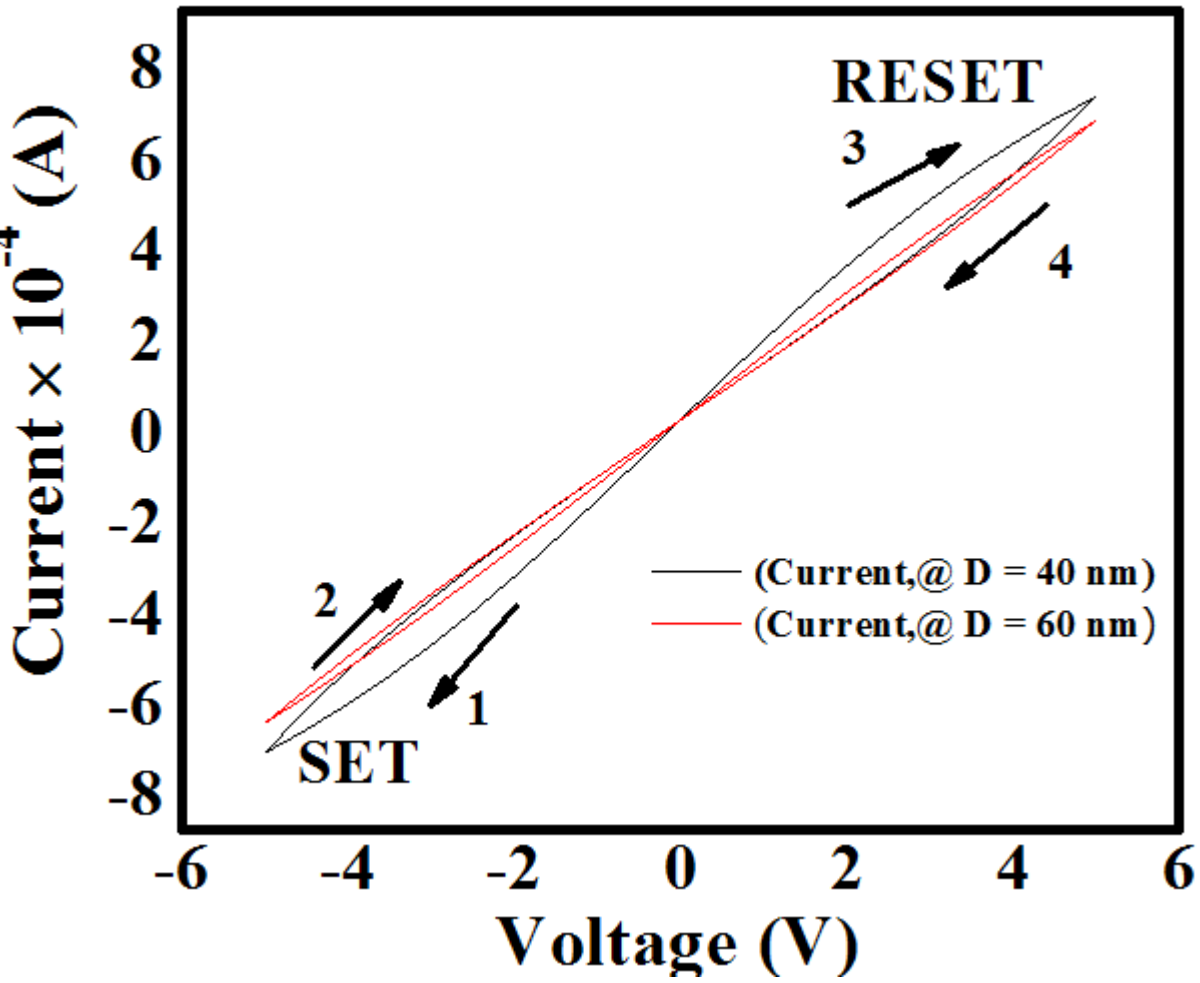

Fig.5 Effect of thickness on resistive switching (RS)

From this plot we observed that thickness plays an important role in the memristive effect in RS the device , the current–voltage hysteresis is dependent on the thickness. In particular, the set voltage gradually increased with increasing thickness in the high resistive state whereas the reset voltage remained almost constant in the low resistive state.

4.2.3 Effect of change in off state resistance on RS:

In Matlab, first we evaluate the data with off state resistance(R_{off} = 12KΩ) after that we evaluate the data with off state resistance(R_{off} = 8KΩ) and we get some change in current-voltage characteristics,observations are following in Table.3

Long Name	voltgae	current	voltgae	current
Units				
Comments	Roff =12KO	Roff =12kO	Roff = 3kO	Roff =3kO
1	0	0	0	0
2	0.5	6.25E-5	0.5	2.94118E-5
3	1	1.25143E-4	1	5.88718E-5
4	1.5	1.88143E-4	1.5	8.84529E-5
5	2	2.51724E-4	2	1.18229E-4
6	2.5	3.16115E-4	2.5	1.48278E-4
7	3	3.81561E-4	3	1.78678E-4
8	3.5	4.48326E-4	3.5	2.09514E-4
9	4	5.16698E-4	4	2.40876E-4
10	4.5	5.86997E-4	4.5	2.7286E-4
11	5	6.59581E-4	5	3.05573E-4
12	4.5	6.01249E-4	4.5	2.77471E-4
13	4	5.40777E-4	4	2.48656E-4
14	3.5	4.78277E-4	3.5	2.1918E-4
15	3	4.13895E-4	3	1.89098E-4
16	2.5	3.47808E-4	2.5	1.58476E-4
17	2	2.80223E-4	2	1.27387E-4
18	1.5	2.11377E-4	1.5	9.59093E-5
19	1	1.41533E-4	1	6.41258E-5
20	0.5	7.09736E-5	0.5	3.21255E-5
21	0	0	0	0
22	-0.5	-7.1078E-5	-0.5	-3.2157E-5
23	-1	-1.41947E-4	-1	-6.4251E-5
24	-1.5	-2.12297E-4	-1.5	-9.61883E-5
25	-2	-2.81828E-4	-2	-1.27877E-4
26	-2.5	-3.50257E-4	-2.5	-1.5923E-4
27	-3	-4.17323E-4	-3	-1.90162E-4
28	-3.5	-4.82791E-4	-3.5	-2.20596E-4
29	-4	-5.46456E-4	-4	-2.5046E-4
30	-4.5	-6.08145E-4	-4.5	-2.79689E-4
31	-5	-6.67717E-4	-5	-3.08227E-4
32	-4.5	-5.93234E-4	-4.5	-2.7493E-4
33	-4	-5.21375E-4	-4	-2.42452E-4
34	-3.5	-4.51728E-4	-3.5	-2.10679E-4
35	-3	-3.83932E-4	-3	-1.79504E-4
36	-2.5	-3.17668E-4	-2.5	-1.48829E-4
37	-2	-2.52648E-4	-2	-1.18565E-4
38	-1.5	-1.88608E-4	-1.5	-8.8629E-5
39	-1	-1.25306E-4	-1	-5.89397E-5
40	-0.5	-6.25098E-5	-0.5	-2.94214E-5
41	0	0	0	0

Table.3 Current-Voltage data with R_{off} (12KΩ and 8KΩ)

Now, we Plot the data from the Table.3

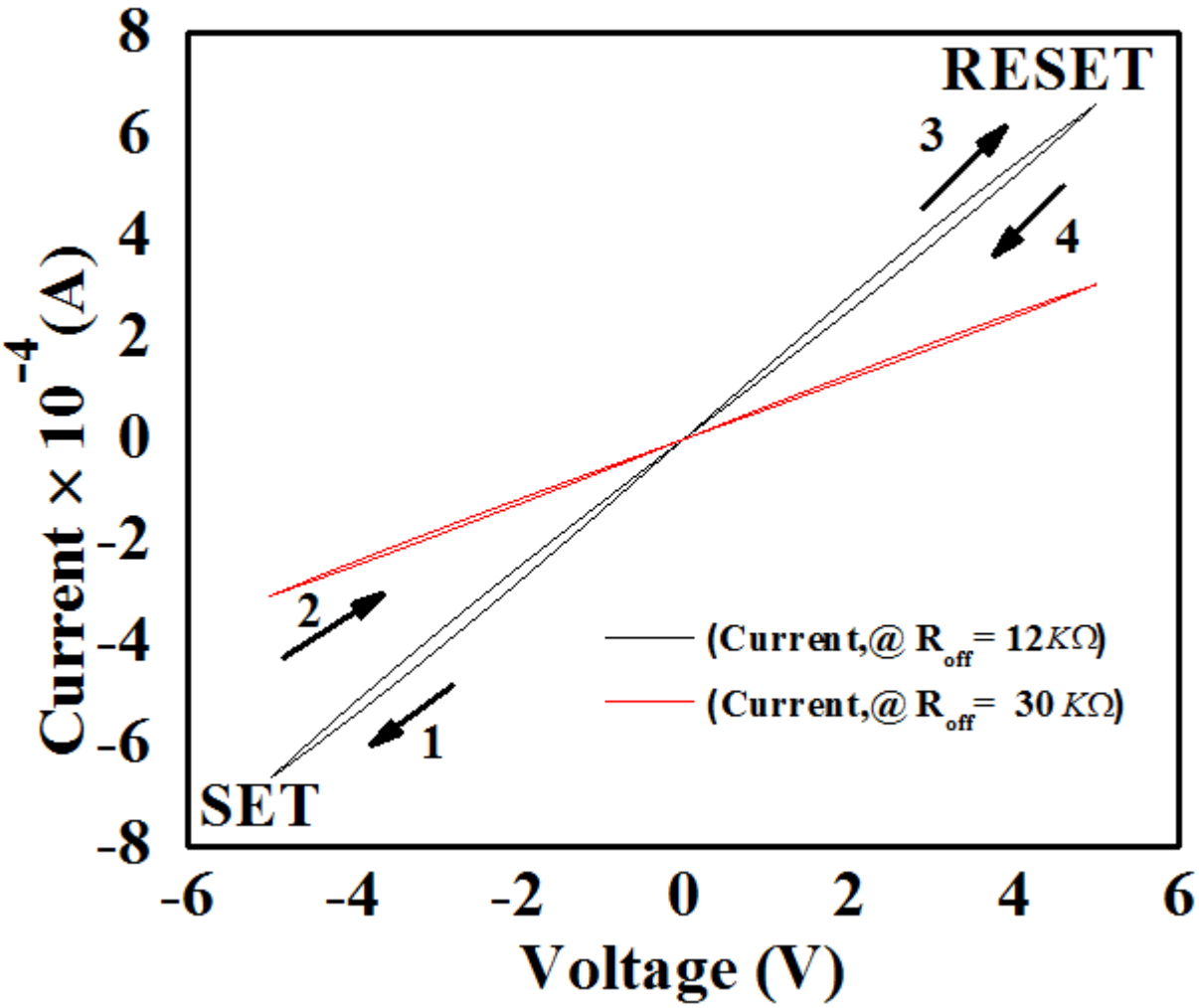

Fig.6 **Effect of R_{off} on resistive switching**

From Fig.6 we observed that observed that the current–voltage hysteresis is dependent on the R_{off} when we Increase Roff 12 KΩ to 30 KΩ the shifts current–voltage hysteresis shifts for lower values of current values.

4.2.4 Effect of state of device on resistive switching (RS):

In Matlab, first we evaluate the data with initial state of device (w(0) = 10) after that we evaluate the data with initial state of device (w(0) = 30) and we get some change in current-voltage characteristics,observations are following in Table.4

	A(X1)	B(Y1)	C(X2)	D(Y2)
Long	Voltage	current	voltage	current
Units	w(t) = 0.5	w(t) = 0.5	w(t) = 0.3	w(t) = 0.3
Com				
1	0	0	0	0
2	0.5	6.25E-5	0.5	5.20833E-5
3	1	1.25143E-4	1	1.04249E-4
4	1.5	1.88143E-4	1.5	1.56622E-4
5	2	2.51724E-4	2	2.09328E-4
6	2.5	3.16115E-4	2.5	2.62499E-4
7	3	3.81561E-4	3	3.16269E-4
8	3.5	4.48326E-4	3.5	3.70783E-4
9	4	5.16698E-4	4	4.26192E-4
10	4.5	5.86997E-4	4.5	4.82661E-4
11	5	6.59581E-4	5	5.40368E-4
12	4.5	6.01249E-4	4.5	4.90507E-4
13	4	5.40777E-4	4	4.39432E-4
14	3.5	4.78277E-4	3.5	3.87228E-4
15	3	4.13895E-4	3	3.33995E-4
16	2.5	3.47808E-4	2.5	2.79846E-4
17	2	2.80223E-4	2	2.24904E-4
18	1.5	2.11377E-4	1.5	1.69302E-4
19	1	1.41533E-4	1	1.13183E-4
20	0.5	7.09736E-5	0.5	5.66976E-5
21	0	0	0	0
22	-0.5	-7.1078E-5	-0.5	-5.67508E-5
23	-1	-1.41947E-4	-1	-1.13395E-4
24	-1.5	-2.12297E-4	-1.5	-1.69774E-4
25	-2	-2.81828E-4	-2	-2.25734E-4
26	-2.5	-3.50257E-4	-2.5	-2.81123E-4
27	-3	-4.17323E-4	-3	-3.358E-4
28	-3.5	-4.82791E-4	-3.5	-3.89632E-4
29	-4	-5.46456E-4	-4	-4.42496E-4
30	-4.5	-6.08145E-4	-4.5	-4.9428E-4
31	-5	-6.67717E-4	-5	-5.44888E-4
32	-4.5	-5.93234E-4	-4.5	-4.8619E-4
33	-4	-5.21375E-4	-4	-4.28885E-4
34	-3.5	-4.51728E-4	-3.5	-3.72775E-4
35	-3	-3.83932E-4	-3	-3.17683E-4
36	-2.5	-3.17668E-4	-2.5	-2.63444E-4
37	-2	-2.52648E-4	-2	-2.09906E-4
38	-1.5	-1.88608E-4	-1.5	-1.56925E-4
39	-1	-1.25306E-4	-1	-1.04367E-4
40	-0.5	-6.25098E-5	-0.5	-5.21008E-5
41	0	0	0	0

Table.4 Current-Voltage data with state of device (0.5 and 0.3)

Now, we Plot the data from the Table.4

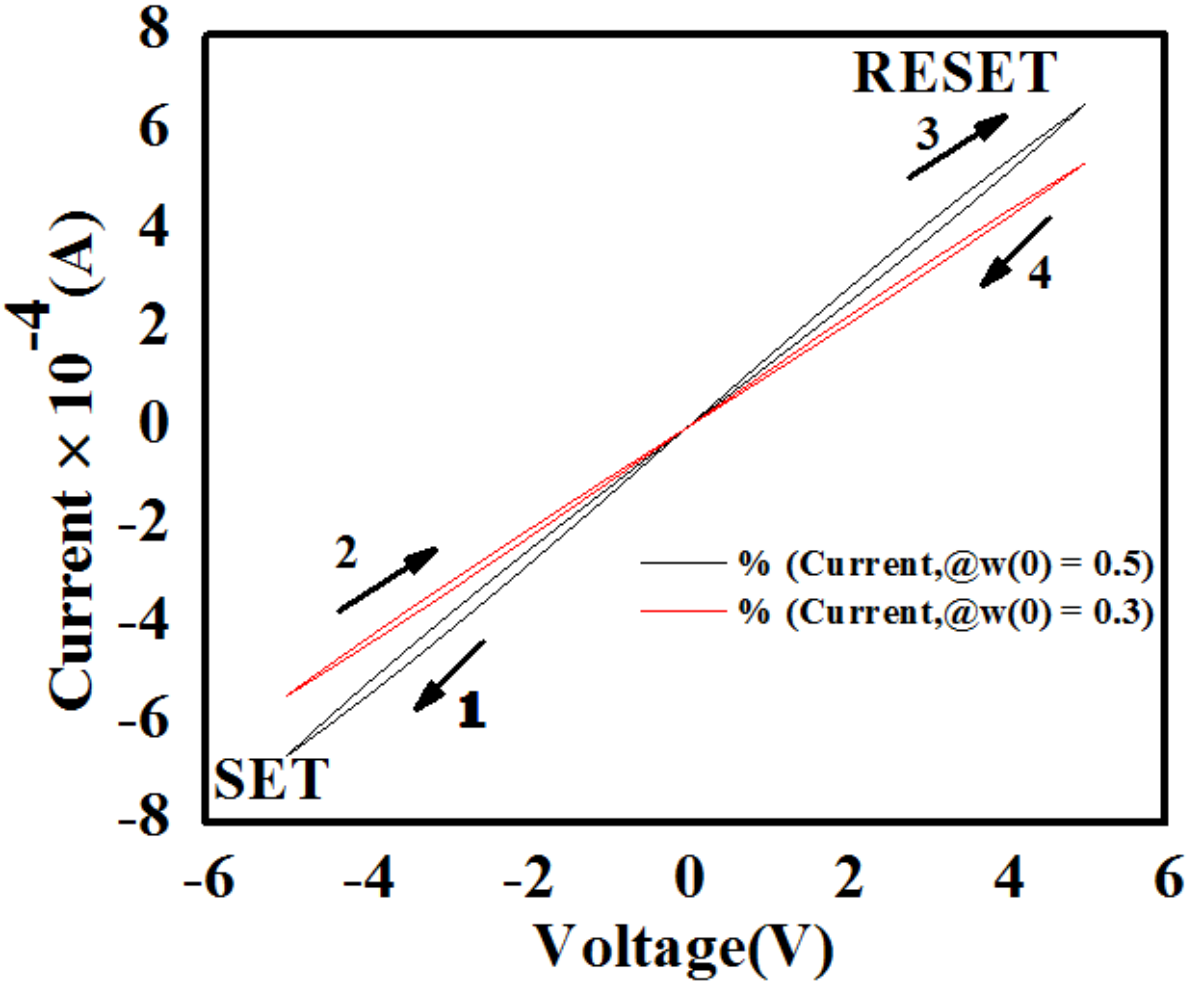

Fig.7 Effect of state of device on resistive switching

From Fig.7 we observed that the current–voltage hysteresis is dependent on the state of device when we decrease w(t) 0.5 to 0.3 , the switching current becomes lower .

4.3 Conclusion:

RRAM devices are one of the most popular non-volatile memory technologies with extensive study being undertaken to understand their mechanism and develop models to realize the device operation and design,accurate and simple device structure. The devices are simple two-terminal metal-insulator-metal (MIM) structure and switch between two resistance states low-resistance state (LRS) and high-resistance state (HRS) .RRAM shows a hysteric relation between the current and voltage characteristics and all the parameters like time,thickness,on state resistance and state of device affect the current–voltage hysteresis.

However, RRAM still suffers from some challenges for mass production, such as fluctuations of program/erase during operation, high operation current and reliability issues. Therefore, it is important to continue to search for a universal physical model and fabrication technology for RRAM, which meets the requirements of the non-volatile memory industry.

4.3 Future work:

We are currently working on important areas which are not yet completed and can be regarded as the future work in this field. Some of them are as follows:

- ➢ Investigation of thermal effects on memristor based RRAM.
- ➢ Development of efficient read and write circuits for memristor based RRAM
- ➢ investigation of stochastic and time series analysis of memristor based RRAM
- ➢ Study of ballistic transport and quantum mechanical effects on the nanoscale memristor device.
- ➢ Design and development of mixed mode programmable analog circuits using memristor. .
- ➢ Development of high performance memristor using physical synthesis technique.
- ➢ Modelling and Development of memristor based 1T1R memory architecture.
- ➢ Design a neuromorphic hardware platform using memristor.
- ➢ Study the nonlinear dynamics of the memristor for the cryptography applications.

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