B. TECH. PROJECT REPORT

On

Effect of Heavily Doped Semiconductor Film on Performance of Nanoscale Transistors

BY

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Effect of heavily doped semiconductor film on performance of nanoscale transistors

A PROJECT REPORT

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CANDIDATE'S DECLARATION

We hereby declare that the project entitled "**Effect of Heavily Doped Semiconductor on Performance of Nanoscale Transistors"** submitted in partial fulfillment for the award of the degree of Bachelor of Technology in 'ELECTRICAL ENGINEERING' completed under the supervision of **Dr. Abhinav Kranti,** Professor, Low Power Nanoelectronics Research Group, IIT Indore is an authentic work.

Further, I declare that I have not submitted this work for the award of any other degree elsewhere.

Pranjal Singh Tomar

CERTIFICATE by BTP Guide(s)

It is certified that the above statement made by the students is correct to the best of my/our knowledge.

Dr. Abhinav Kranti

Professor,

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Preface

This report on **"Effect of Heavily Doped Semiconductor Film on Performance of Silicon Nanoscale Transistors"** is prepared under the guidance of **Dr. Abhinav Kranti,** Professor, Discipline of Electrical Engineering, IIT Indore.

Through this report, I have presented an analysis of threshold voltage variability in Junctionless transistor due to random dopant fluctuations and how a change in channel material can lead to reduced variability.

The simulated results shown in the report are obtained by using TCAD simulation software (ATLAS from SILVACO).

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Abstract

This project work analyses the threshold voltage (V_{th}) variation due to random dopant fluctuations in Junctionless devices as the device is downscaled. The phenomenon of RDF has been reported as a critical cause of variability when downscaling of DG-MOSFETs. This work aims understand why threshold voltage variation occurs in the Junctionless devices when the channel region contains a random dopant. We have used the Shin's model to simulate the effect of random dopant and observe the change in potential distribution due to a single impurity dopant. This study aims to examine whether the threshold voltage (V_{th}) variation due to RDF is a critical issue. We have thus randomly placed dopants in the channel regions and performed many simulations to observe the variability spectrum of the threshold voltage (V_{th}). We then studied the potential distributions corresponding to maximum and minimum change to gain insights on the reason for variability. RDF is a statistical variation and no significant work has been done to mitigate the problem. Since variability can be influenced by the choice of materials we have attempted to reduce the variability by changing channel material.

Keywords: Junctionless Transistors, RDF, Threshold Voltage (V_{th}), MOSFETs, Variability.

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Chapter 1

Introduction

1.1 Motivation

MOSFETs are widely used in devices of everyday life, from mobile phones to computers. As consumers demand enhanced features, the transistor has to be miniaturized to achieve enhanced functionality and density at a reduced cost [1]. In such nanoscale regime, many new transistor architectures have emerged which need to be evaluated for their suitability and challenges. One such option is the heavily doped transistor which apart from having the same type of dopants in the semiconductor film, suffers from variability issues such as threshold voltage (V_{th}) variations [2]. The project aims to analyze the impact of the fluctuations in a heavily doped transistor, which has emerged as possible device options to enable downscaling at lower gate lengths. One possible device which mitigates the problem associated with the fabrication of ultra-sharp *pn* junction is Junctionless Transistor (JT) [3]. Due to the absence doping concentration gradient, the fabrication process of JT is relatively simpler as compared to standard CMOS [4–6]. Junctionless transistors are designed with uniform doping concentration throughout the film. The typical value of the channel doping ranges from 5×10^{18} and 10^{19} cm^{-3} [7].

As the device dimensions are scaled down to the nanoscale regime, the impurity dopants affect the device characteristics through the change in threshold voltage (V_{th}). To study the impact of dopant atoms JT is chosen as the device of study due to its relatively simple architecture. Similar to inversion mode transistor, scaling JT at lower gate length results in various undesirable effects due to random discrete dopant [8-15]. In the actual device fabrication, unintended impurity dopants can be located into the channel due to process fluctuations and uncertainties. The threshold voltage (V_{th}) variation occurs due to random dopants [6]. The project work explores the phenomenon of RDF (Random Dopant Fluctuations) and tries to evaluate the behavior of JT at lower gate length.

1.2 Metal Oxide Semiconductor Transistors

1.2.1 Overview

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is by far the most prevalent semiconductor device in Integrated Circuits (ICs). It is the basic building block of digital, analog, and memory circuits [16]. Figure 1.1 shows the basic schematic of a bulk *n*–channel MOSFET [17]. The n^+ source/drain regions are diffused or implanted into a relatively lightly doped *p*-type substrate and a thin oxide layer separates the conducting gate from the silicon surface [18]. No current flows from drain to source without a conduction channel between them. When a positive voltage is applied to the gate relative to the substrate (which is connected to the source in this case), positive charges are in effect deposited on the gate metal. In response, negative charges are induced in the underlying silicon, by the formation of a depletion region and a thin surface region containing mobile electrons (inversion layer below oxide) [18]. These induced electrons inside the channel of the FET allow current to flow from drain to source. These kinds of MOSFETs are known as inversion mode (INV) MOSFETs.

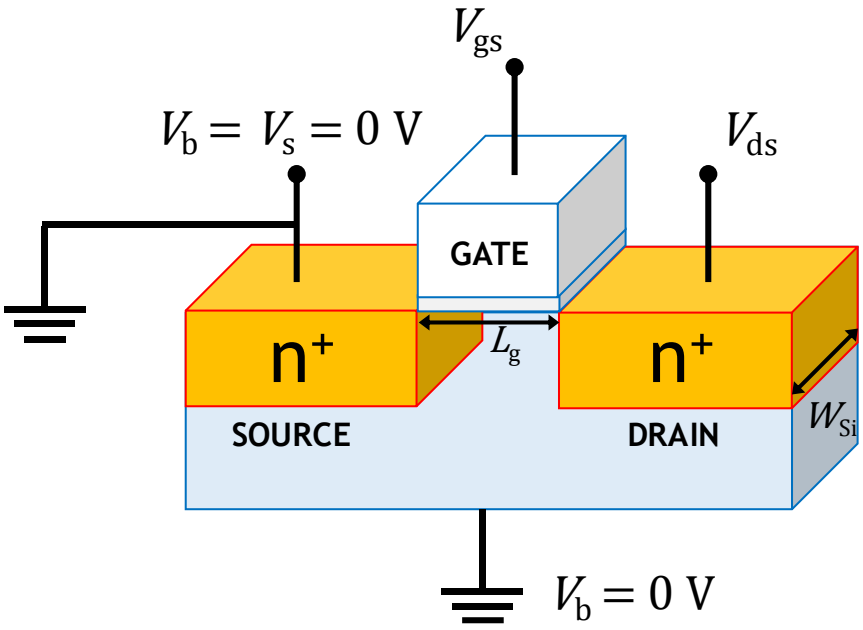

Figure 1.1: Schematic of conventional bulk *n*–channel MOSFET. V_{gs} and V_{ds} are gate to source and gate to drain voltage respectively. L_g is gate length and W_{Si} is the width of MOSFET [16].

The name field-effect transistor (FET) refers to the fact that the gate turns the transistor on and off with an electric field through the oxide. A transistor offers a high input resistance to the signal source, drawing little input power, and a low resistance to the output circuit, capable of supplying a large current to drive the circuit load.

1.2.2 Characteristics of MOS Transistor

The simulations for the project work are performed on Atlas Silvaco TCAD software suit. It takes a coded structure as input to generate the device structure and calculates the value of the device parameters by solving equations using numerical methods on mesh points. Mesh is a 2-D grid on whose intersection points are the equations solved. We generate the output characteristics of a MOS transistor by increasing the gate voltage to 1.0 V. The plots are generated and analyzed by using TonyPlot tool which is a part of the software suit.

Figure 1.2 shows the I_{ds} – V_{ds} characteristics at drain bias (V_{ds}) = 50 mV (log and linear scale both) of conventional inversion mode MOSFET. Depending on the gate voltage, the MOSFET can be turned off (conducting only a very small off-state leakage current, I_{off}) or on (conducting a large on-state current, I_{on}).

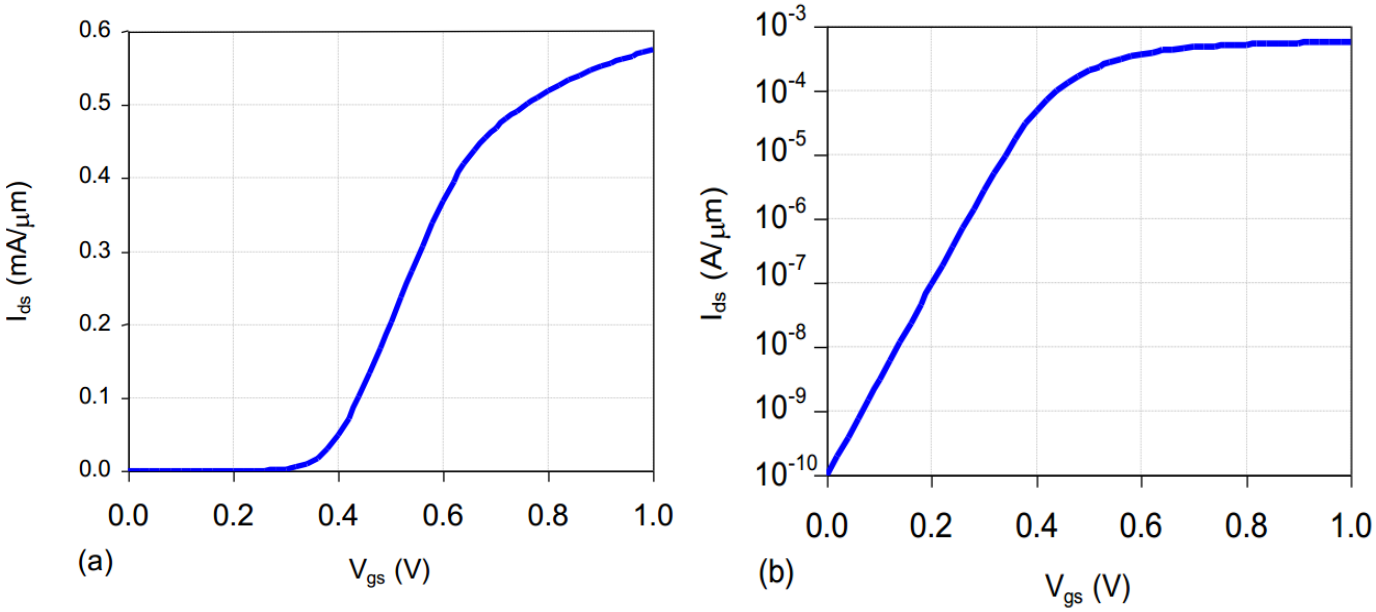

Figure 1.2: I_{ds} – V_{gs} characteristics of an INV mode MOSFET at V_{ds} = 50 mV (a) Y – axis is in linear scale. (b) Y – axis is in log scale.

1.3 Conventional Multi-Gate FETs

1.3.1. Overview

Since scaling trends impose a reduction in the characteristic device dimensions of approximately 30% at each generation technology [1]. With such reduced dimensions bulk or SOI planar MOSFETs may not be able to efficiently control the conduction channel. To overcome this challenge several configurations with the gate electrode surrounding or wrapping the channel region in different ways have been explored.

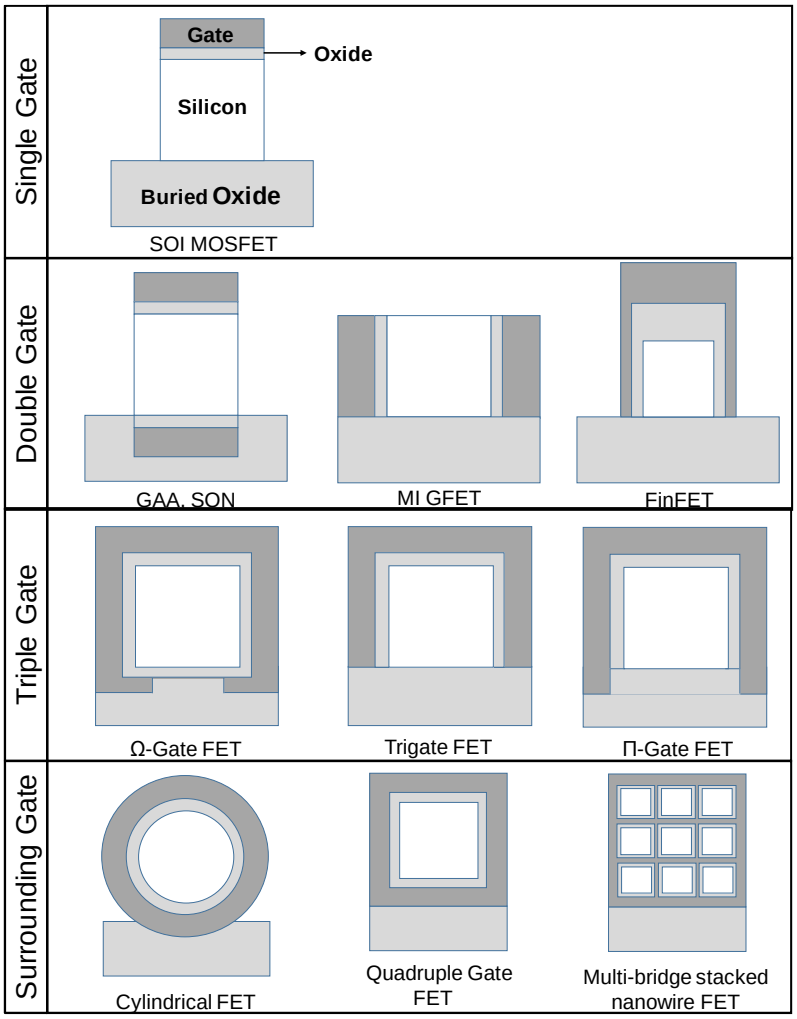

Figure 1.3: Cross sections of different gate structures [19].

The main types are represented by double-gate FET, where the channel region is sandwiched between the two gate electrodes, tri-gate, and quadruple gate FETs, where a single electrode is folded on three sides of the channel or wrapped all around the channel, respectively. Fig. 1.3 depicts the cross sections of the principal families of Multi-Gate devices [19].

1.3.2 Advantages of Multi-Gate FETs

The issues where the gate controllability is affected in downscaled devices are commonly referred to as Short Channel Effects (SCEs). In SCEs the electric field from source to drain propagate through the depletion region, which extends in the channel as the device dimensions are reduced, hence competing with gate electrode over the channel electrostatics [20].

In sub-100 nm regime, the Multi-Gate FETs are less affected by the DIBL as compared to single gate FETs [21]. This is due to the enhanced control of gate over the electric field lines from source and drain regions. The reduction in V_{th} as the effective gate length L_{eff} is reduced is referred to as threshold voltage roll off and it is another type of SCE. Multi-gate FETs have another advantage that they exhibit a lower decrease in threshold voltage as the device is scaled down.

Multi-Gate FETs are less affected by SCEs and they also have larger drive current. I_{ds} increase approximately linearly with the number of gates [19].

1.3.3 Challenges in Multi-Gate FETs

As the gate length of the device approaches 10 nm in next-generation technology, devices will require ultra-sharp profiles in the junction between source/drain and the channel region. These processes will require ultra-fast annealing. The development of such advanced and costly techniques, which can stand up to the limits of low thermal budget presents a severe limitation of further scalability of Multi-Gate FETs [21].

It is for this reason that recent studies ([5], [22] and [23]) have considered device structures that avoid the above-mentioned difficulty of forming junctions between source/drain and the channel region, with abrupt doping concentration gradients. Hence, the name junctionless transistor, that is the object of our study and refers to a device exhibiting a uniform doping polarity all over the channel, source and drain regions.

1.4 Junctionless Transistor

1.4.1 Overview

Nearly all existing devices work on the principles of junctions, whether it is to allow the current or to stop it. As these devices are downscaled the requirement of junctions becomes a necessity. It poses challenges to fabricate such ultra-sharp junctions due to laws of diffusion and statistical variation. The junctionless transistor is a transistor with no concentration gradient.

Junctionless Transistor (JT) is a heavily doped semiconductor device with uniform doping of 5×10^{18} to 10^{19} cm^{-3}. The junctionless transistor was first fabricated in 2010 by J.P. Colinge's group, where they displayed full CMOS functionality [3]. Junctionless transistor has a single type of dopant atom and hence no *pn* junction. The channel region concentration is controlled by the gate terminal. A high work-function material is used in gate terminal of the device. This depletes the electrons presentation in the channel region of the device. Hence with a suitable gate work-function, the device can be switched off for zero bias.

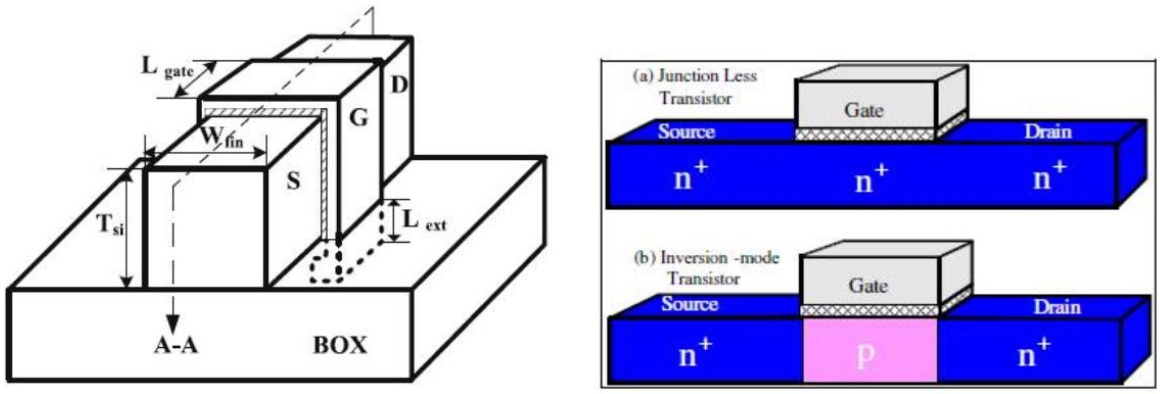

Figure 1.4: Scheme of a MuGFET (left) and longitudinal cross sections of a junctionless (a) and a conventional (b) FET [5].

1.4.2 Characteristics

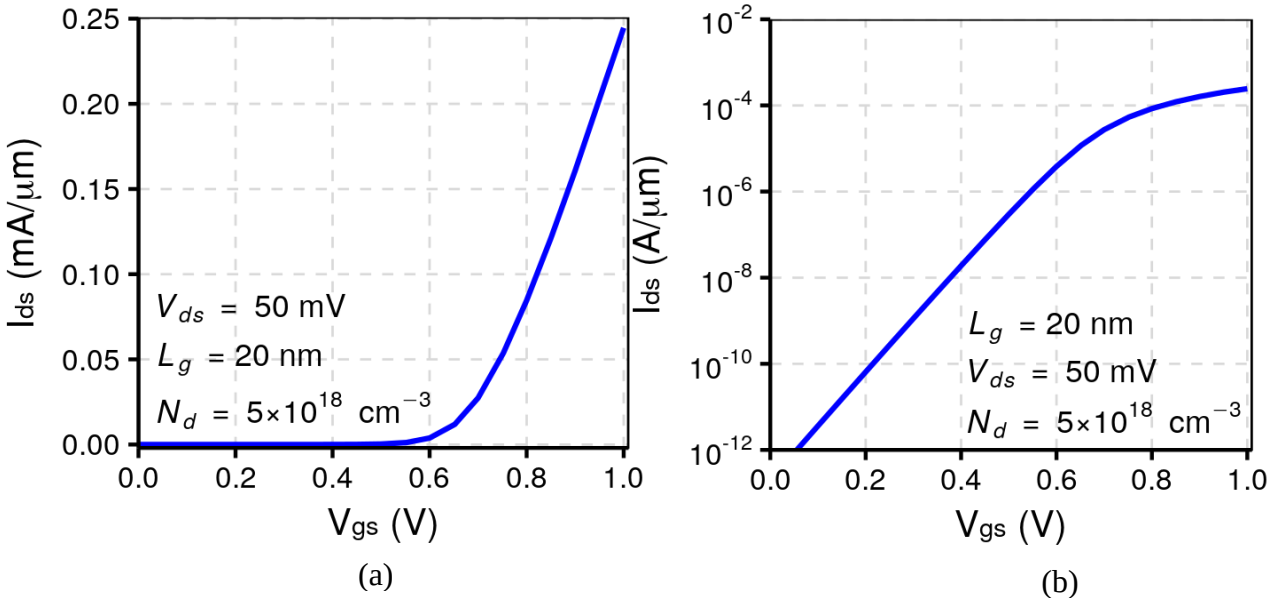

Figure 1.5: I_{ds} - V_{gs} characteristics of the junctionless transistor (a) Y-axis in linear scale, (b) Y-axis in log scale.

Fig 1.5 shows the I_{ds} - V_{gs} characteristics of the Junctionless transistor. The device can be turned off at 0.0 V on using gate metal of higher work-function (conducting a very small leakage current, I_{off}).

Chapter 2

Random Dopant Fluctuation (RDF)

2.1 Literature Survey

2.1.1 Variability

All the available technology relies on the device with abrupt junctions between source/drain and channel regions. As the scaling regime approaches sub-22 nm, the fabrication process for such devices requiring abrupt junction becomes more and more complex [3]. The novel device which bypasses the requirement of junctions is a heavily doped transistor with uniform doping of 5×10^{18} to 10^{19} cm^{-3} of *n*-type dopant atom. Before the device is produced in large scale it must be tested against variability, which has become a major issue in the device with small dimensions [3-4]. In this project, we are specifically focused on the phenomenon of random dopant fluctuations, which is a critical source of variability for conventional MOSFETs.

Variability is defined as how the statistical variations in design parameters affect the performance of a large number of devices [21]. This study is focused on the variability caused by the random placement of dopant impurities inside the channel region. This is commonly referred to as Random Dopant Fluctuations (RDF) [24-25].

RDF is produced by the placement of the dopant atoms in the channel region, which obeys the statistical laws of nature and hence the ideal doping profile corresponding to the device is unattainable. Additionally, the discreteness of charge does not allow for a uniform concentration gradient and such effects become more and more pronounced when the device is downscaled.

2.2 Methodology

2.2.1 TCAD Simulation

The project aims to understand the phenomenon of random dopant fluctuations, its causes, and impacts of the devices. The second objective is to select a mathematical model which can be used in device simulation to express the effect of random dopant fluctuations. Random dopant variation is a statistical variation and hence require a large number of simulations to extract the results. Hence the model was so chosen which was simpler and captured the phenomenon with good accuracy, and which could be simulated on a large number of devices within the given time frame to complete the project. Since Junctionless transistor is one of the possible devices for future technology nodes. It needs to be inspected for variability issues. Thus the third objective of the project is to use the model so selected on downscaled Junctionless transistors and inspect the criticalness of the issue of variability in the device due to random dopant fluctuations. We have represented variability by standard deviation as previous works represent it in the same terms [26-29]. Thus, in this work, simulation of random dopant fluctuations in Junctionless transistors is performed via technology computer-aided design (TCAD) software [30].

2.2.2 The Shin Model

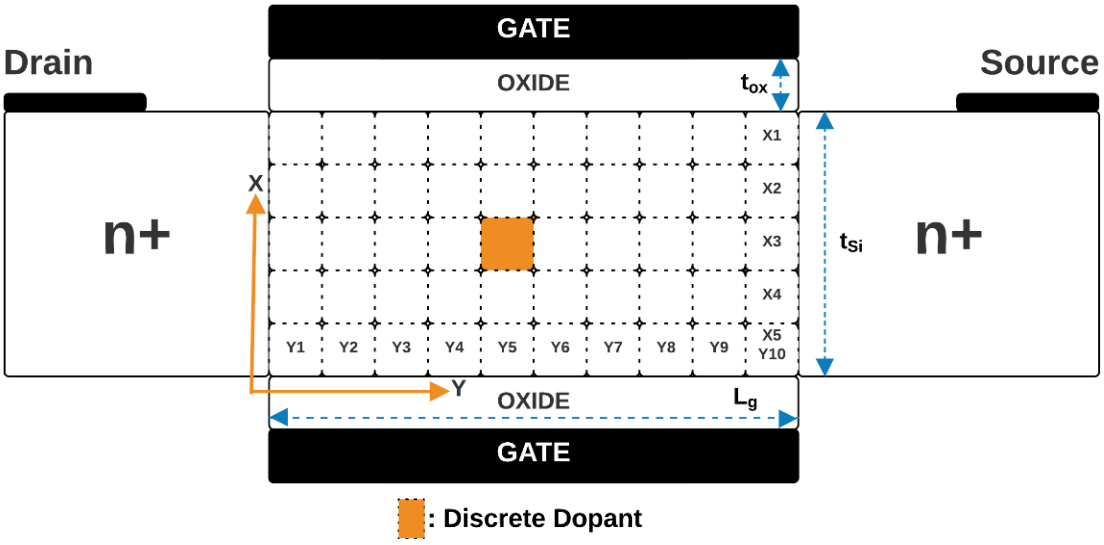

Figure 2.1: Schematic diagram showing Shin's model for a DG-Junctionless transistor with channel divided into 50 regions.

In order to capture the effect of the random dopant fluctuations, we have used a macroscopic model developed by Shin [31] using atomistic modelling [32]. Fig .2 shows the schematic structure of the double gate Junctionless Transistor.

As shown in the above diagram the channel region is divided into 50 regions. The locations from gate to the gate are marked X1 to X5 from the top. The location from source to drain is marked with Y1 to Y10. Each square location denotes a possible position of random dopant and when a random dopant is present in the square region then the square in uniformly doped.

2.2.3 Device Parameters

In the above diagram, the L_g is 20 nm, t_{Si} is 10 nm, t_{ox} is 1 nm and for all the simulations V_{ds} is 50 mV. The source and drain regions are heavily doped with an *n*-type dopant and uniform doping of 10^{20} cm^{-3}. The doping in the channel region consists of both the doping of the square region when the dopant is present and the doping in the remaining region in the channel. If the channel is uniformly doped with the presence of some dopants from the source or drain region, the average channel doping will increase. Thus in order to compare simulation results, we must first fix the average doping of the channel region. This is taken care of by equations given by Tang's group who developed device parameters distribution models [8].

$$N_d = \frac{N}{l^3} \tag{2.1}$$

$$N_{avg} = \frac{N_d}{N_{cube}} \tag{2.2}$$

In the above equations, N_d is doping value of the square region which is uniformly doped to represent the random dopant, N is a number of dopants in the channel region, l is the length of the side of the square region, N_{avg} is average channel doping. The remaining channel is intrinsically doped.

2.2.4 Workflow

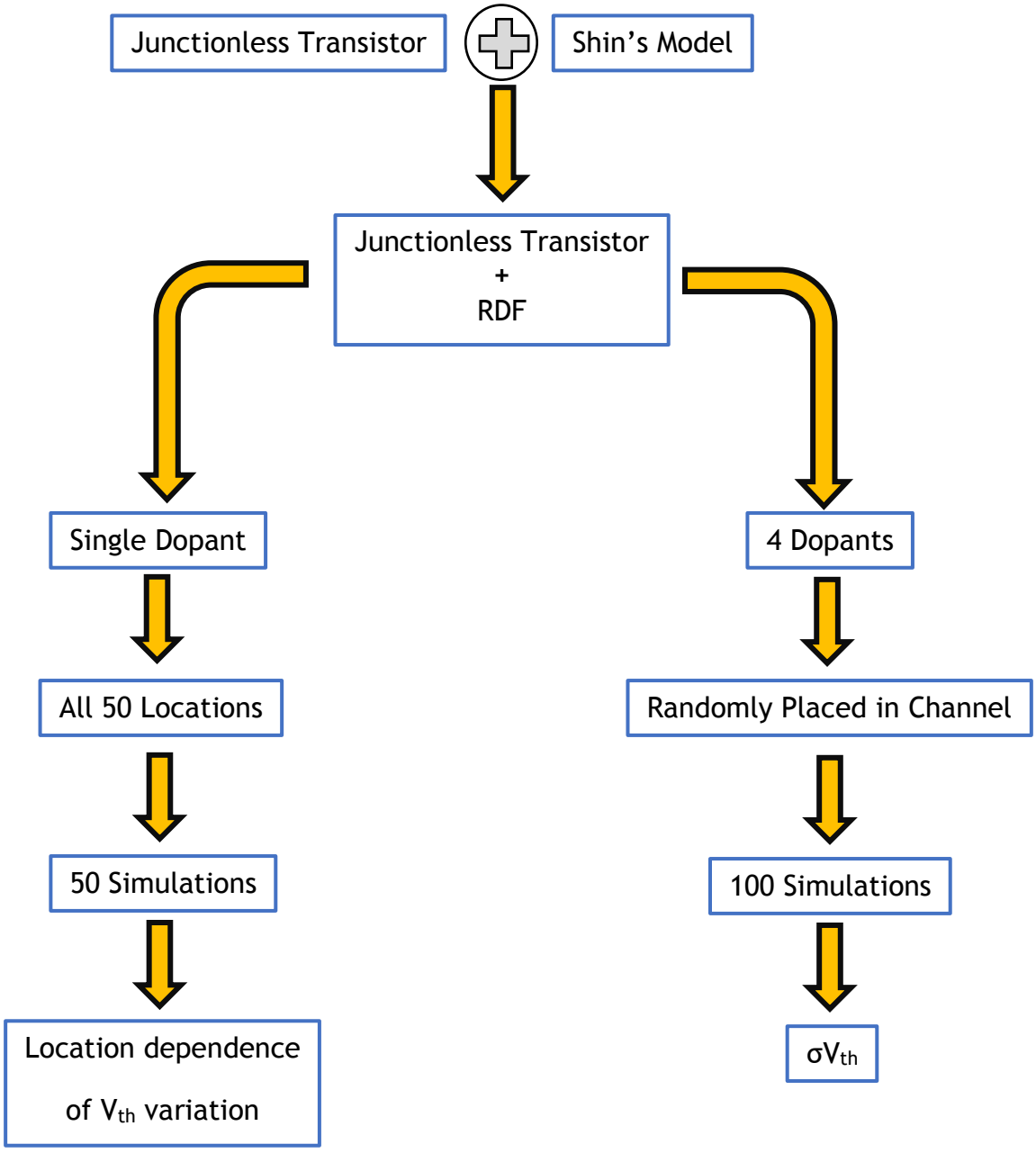

Figure 2.2. Flowchart of the work undertaken in the analysis of RDF in Junctionless transistor.

Chapter 3

Threshold Voltage Variation in Junctionless Transistor

3.1 Cause of Variation

In this project, we have attempted to understand the phenomenon of random dopant fluctuation in Junctionless transistor. In order to understand why the introduction of the dopant atom in the channel causes the change in threshold voltage, simulations with a single impurity dopant were done. The simulation was performed for all 50 dopant positions as shown in figure 3.1.

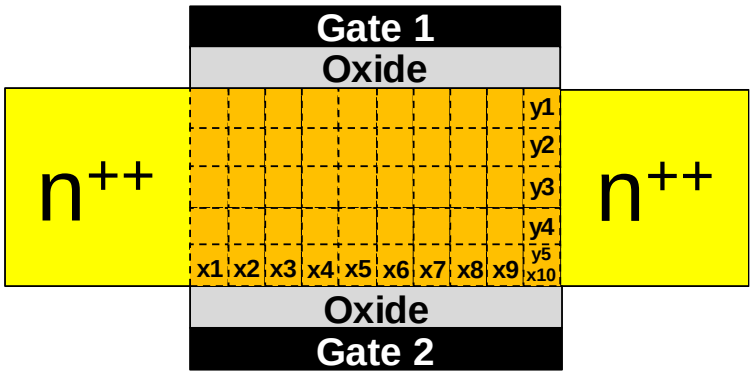

Figure 3.1: All 50 possible dopant location in the channel of Junctionless transistor.

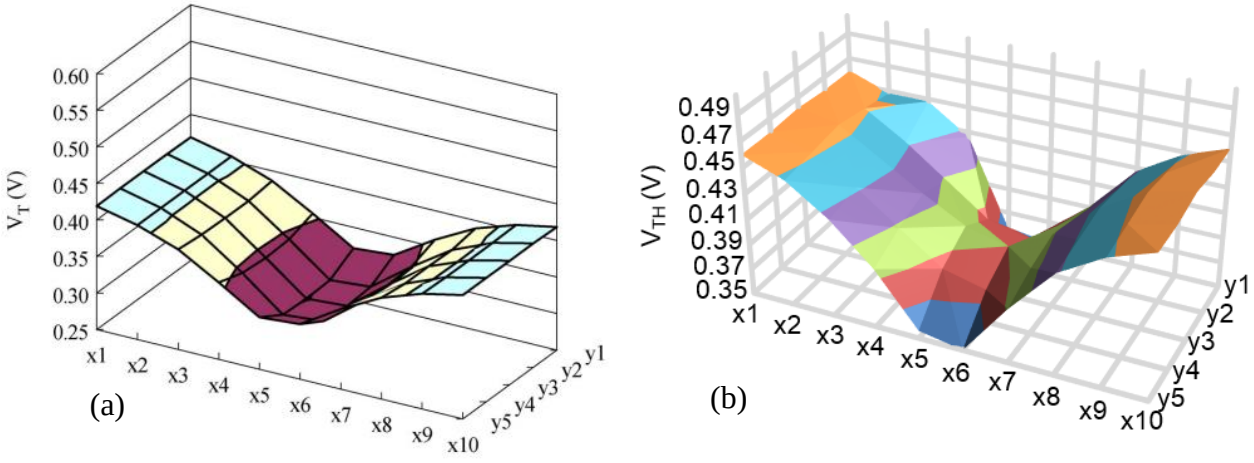

Figure 3.2: Threshold voltage variation for all 50 possible dopant position in (a) DG-MOSFET [33], (b) Junctionless Transistor.

One such analysis for DG-MOSFET has already been reported by Chiang as shown in figure 3.2 (a) [33]. The threshold voltages corresponding to all the 50 dopant locations were plotted in a 3-D contour. To first understand the effect of introducing a dopant in the channel we did the same analysis with Junctionless transistor and the plot is shown in figure 3.2 (b).

If we compare the two contour plots we observe that the variation is almost similar in both the plots. The following comments can be made by comparing them. The threshold voltage for the DG-MOSFET is 0.42 V and 0.46 V for the Junctionless transistor.

1. There is negligible change in the threshold voltage when the dopant location varies from gate to gate.
2. The change in the threshold voltage is maximum when the dopant lies in the center of the channel.
3. The change in the threshold voltage in minimum when the dopant lies nearer to the source/drain region.

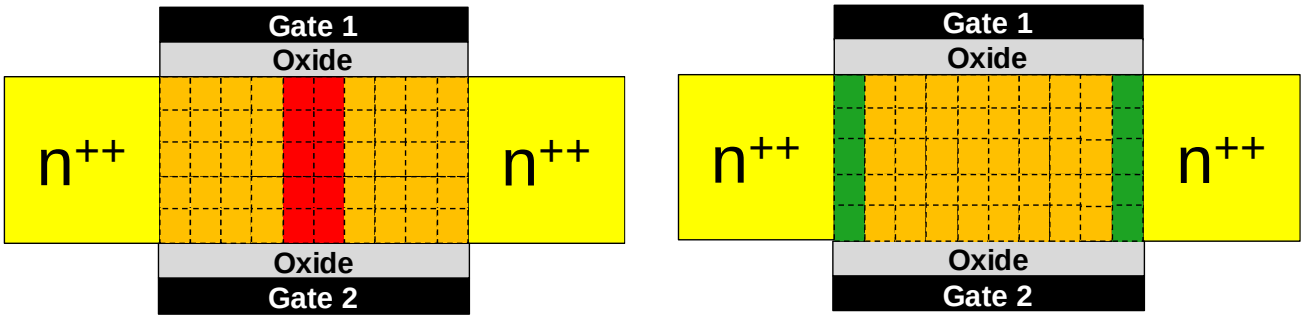

Figure 3.3: Positions of dopant atoms corresponding to (a) maximum variation and (b) minimum variation.

3.1.1 Analysis with a Single Dopant

In order to understand how the threshold voltage is influenced by the presence of dopant, we compare the potential distribution of the structures in the case when the dopant is present in the center of the channel (which causes a maximum change in the threshold voltage) and when it is present near the source/drain region.

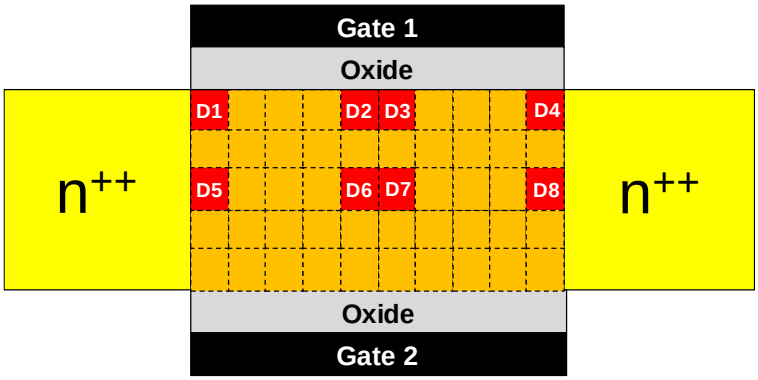

Figure 3.4: Dopant location at center (D2, D3, D6, and D7) and near source/drain (D1, D4, D5, and D8).

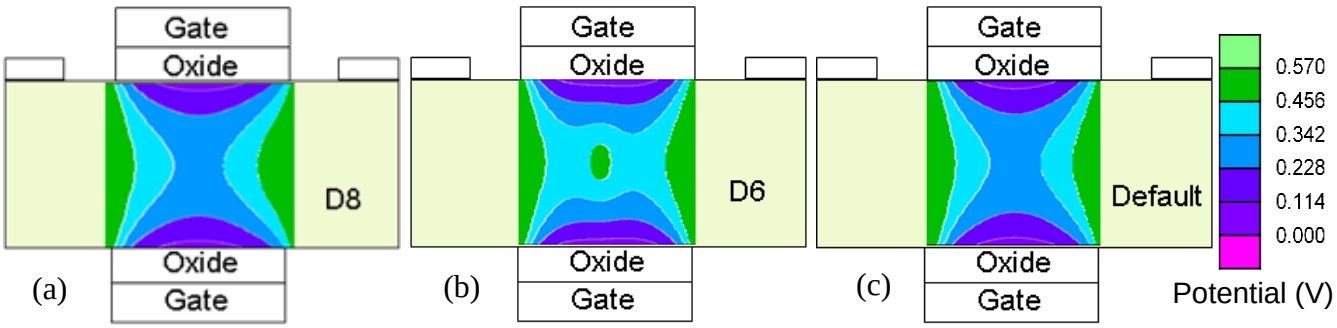

Figure 3.5: Potential distribution contour for positions (a) D8, (b) D6, (c) Default structure with no dopant.

When the dopant atom is present in the center of the channel it is not depleted by the gate electrode and thus the electron concentration at the center becomes even higher than it was in absence of dopant. This is seen in figure 3.3 (b) as a localized higher potential at the center of the film. Since the potential in the channel is increased, the threshold voltage is lowered i.e. the channel formation takes places at lower gate bias.

Now to further understand the nature of distortion in potential profile, simulations were done by taking 4 dopant atoms in the channel region. On solving the equations (2.1) and (2.2) for $N_{avg} = 10^{19}$ cm^{-3}, we get the parameter $N_d = 5\times10^{20}$ cm^{-3}. N_d is the doping of the square region which represents the presence of the random dopant. The dopants were now deliberately put in the four positions [D2, D3, D6, and D7] and [D1, D4, D5, and D8], which correspond to the structure of maximum and minimum change.

3.1.2 Analysis with 4 Dopants in the Channel Region

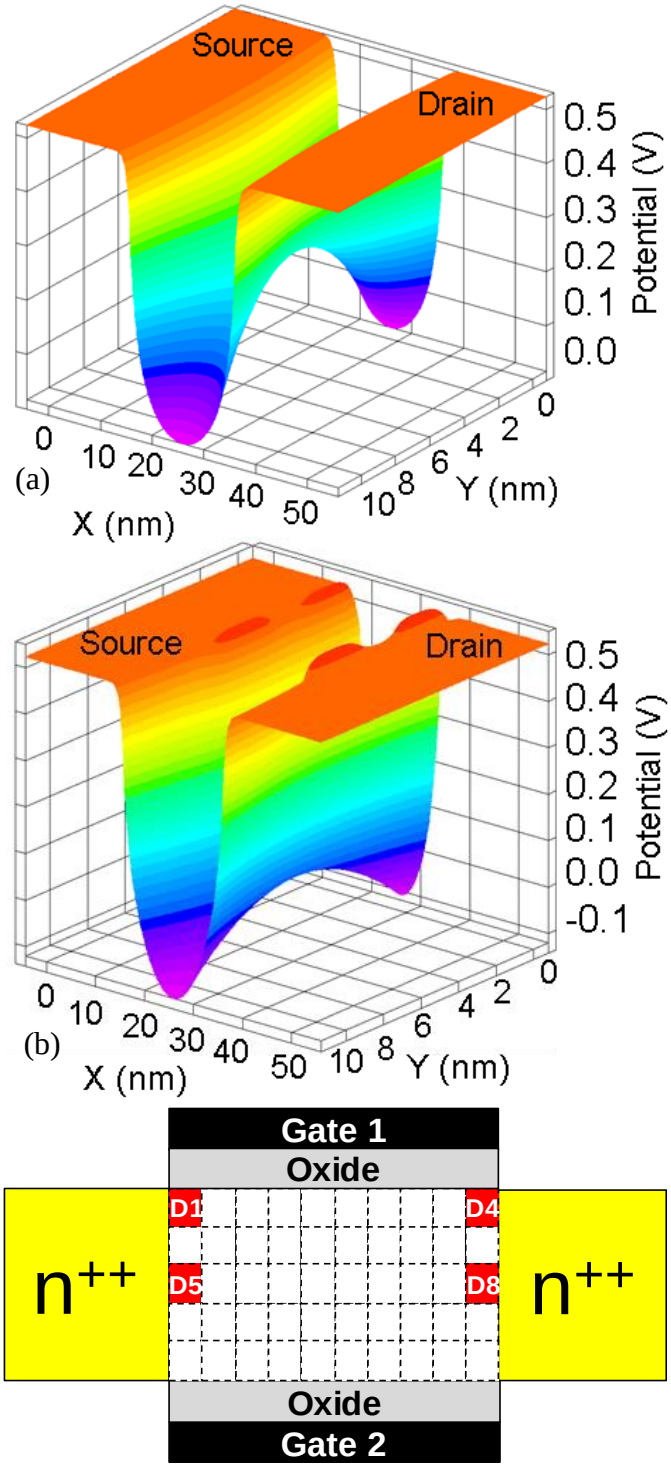

Figure 3.6: Potential distribution of the device with (a) uniform doping and (b) random dopants at (c) location D1, D4, D5, and D8.

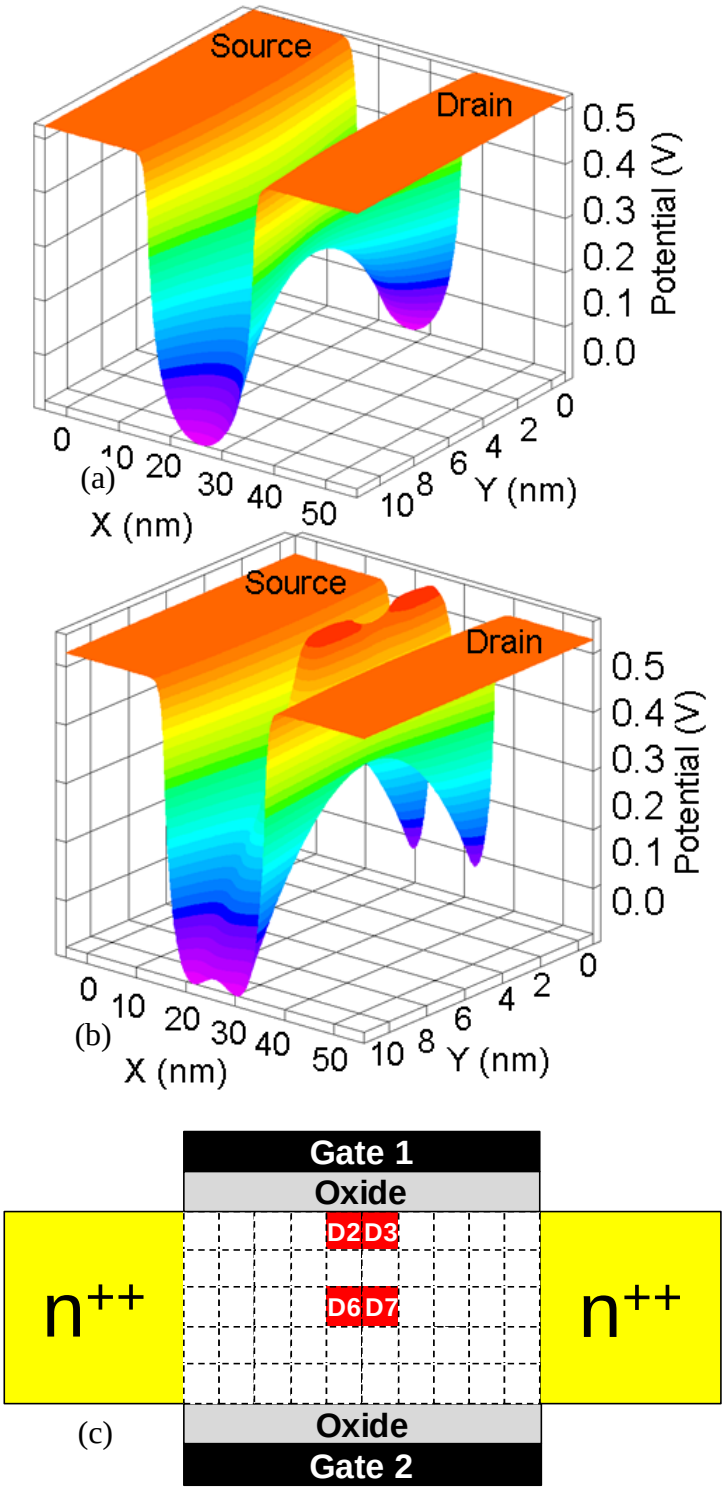

Figure 3.7: Potential distribution of the device with (a) uniform doping and (b) random dopants at (c) location D2, D3, D6, and D7.

We now compare the 3-D potential contour of the ideal structure with uniform doping profile and structure where random dopants are present at the positions D2, D3, D6, and D7. These locations correspond to the positions where the change is maximum. This can be clearly

observed in the potential contour that there increase in potential at the center of the channel region. The channel region has high potential due to the presence of higher electron concentration. This causes a significant reduction in threshold voltage because the channel formation starts at the center and presence of high potential i.e. high electron concentration aids in the process of channel formation. Thus the threshold voltage is lowered and hence the variation is maximum.

We now compare the 3-D potential contour of the ideal structure with uniform doping profile and structure where random dopants are present at the positions D1, D4, D5, and D8. These locations correspond to the positions where the change in minimum. It clearly observed in the potential contour that there is almost no change in potential distribution in the channel region except near the source/drain region where the dopants are present. The center of the channel remains unaffected. Since the source and drain regions have a very high doping, the dopants closer to them match their doping and potential. Thus the effect registered in a change in threshold voltage in minimum. In other words, the presence of dopants near the source or drain region do not aid or hinder the channel formation for conduction, hence the variation in threshold voltage is negligible.

3.2 Variability in Junctionless Transistor

The junctionless transistor has been reported to experience the phenomenon of RDF when they are downscaled. Thus it becomes important to check their susceptibility to variability before they mass produced. Hence the next step is to evaluate whether RDF is a critical issue for variability when considering device scaling.

To analyze the effects of RDF we adopt the same methodology as adopted above and work with the same numbers. We now have four dopants in the channel region. In contrast to earlier simulations where the dopants atoms were deliberately placed in the channel region to produce maximum and minimum variation in threshold voltage, we now place them randomly at four different positions in the channel region as shown in figure 3.5.

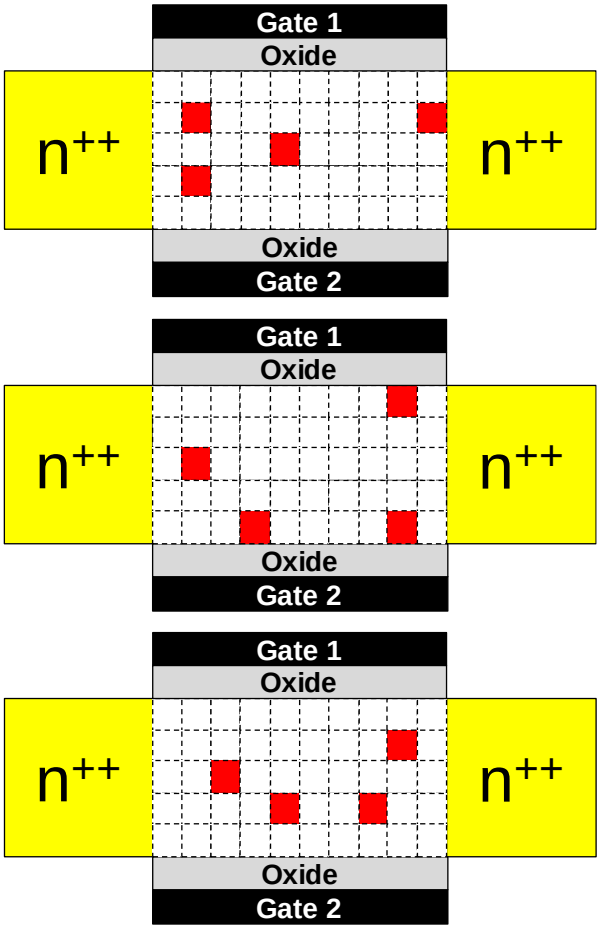

Figure 3.8: Possible configuration when 4 atoms are randomly placed in the channel.

We performed hundred such simulations where we allow the random distribution of the dopant atoms. This was achieved by using a random number generator which generates integer with uniform distribution in the range desirable. From figure 3.1 we get that the random place for

Y-coordinate for the dopant is 1-5 and for X-coordinate is 1-10. The integers are selected with equal probability i.e. it follows a uniform distribution. The plot of I_{ds} - V_{gs} spread for hundred simulations is shown in figure 3.6.

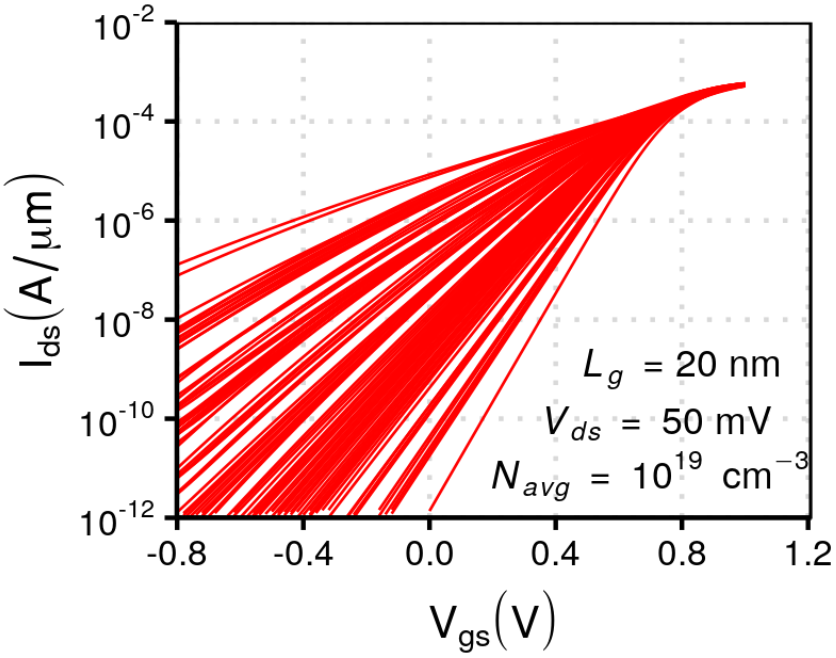

Figure 3.9: I_{ds} - V_{gs} spread for 100 simulations in the junctionless transistor.

It is clear from observing figure 3.6 that output characteristics significantly vary when the random dopants are placed in the channel region. When the dopant atoms are present near the center of the channel the change in threshold voltage is more but when the dopants lie near to the source or drain region their effect is lessened due to the device properties as discussed in section 2.1.2.

We then extracted the threshold voltage from each of the output characteristics to calculate the value of threshold voltage variation (σV_{th}). The threshold voltage variation (σV_{th}) is the standard deviation of the threshold voltages obtained.

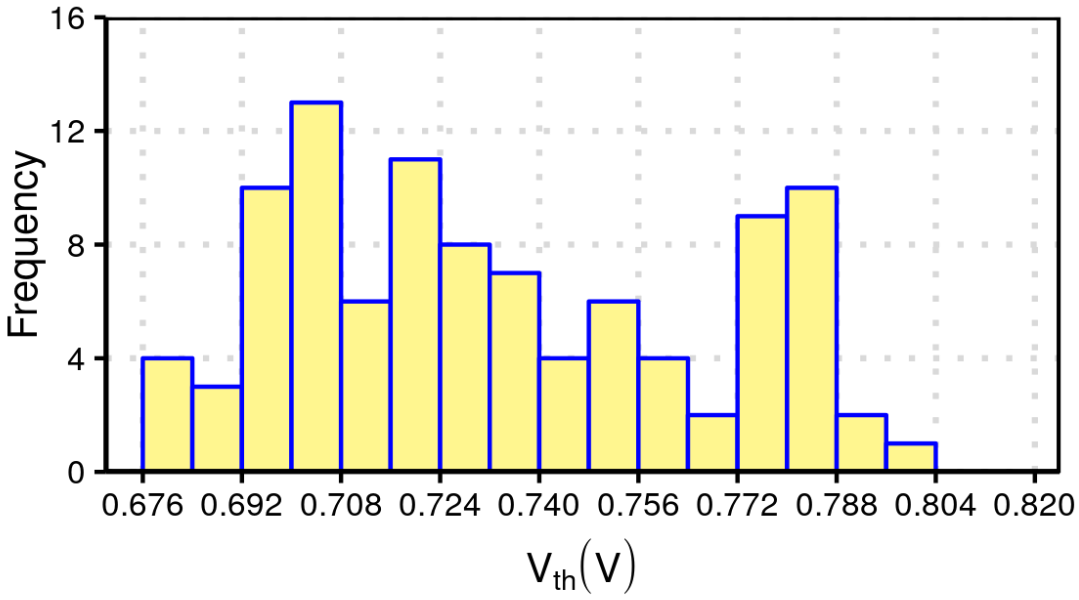

Figure 3.10: Threshold voltage (V_{th}) frequency distribution for 100 simulations in the junctionless transistor.

The value of threshold voltage variation for these 100 simulations come out to be 32.91 mV and the complete range of values is 120 mV. It is clear from such large spread of threshold voltage values and variation that RDF is a critical issue in junctionless transistors. The next part of the project will focus on a way to reduce such high variability.

Chapter 4

Silicon vs. Germanium

4.1 Comparison

In contrast to conventional MOSFETs which is mostly dominated by silicon, junctionless transistors can have germanium devices with feasible output characteristics as shown in figure 4.1.

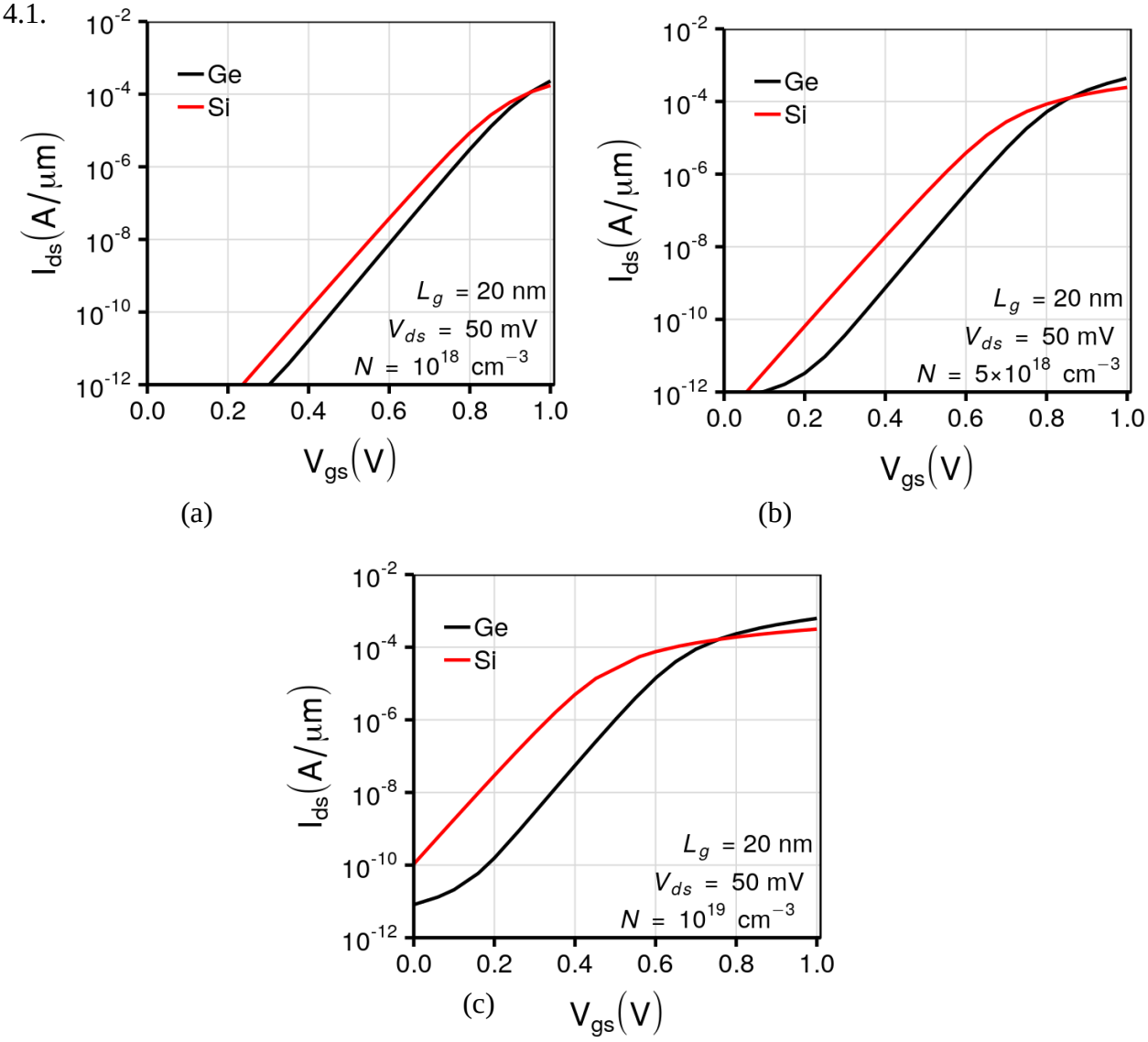

Figure 4.1: I_{ds} - V_{gs} characteristics of Si-JL transistors and Ge-JL transistor for doping levels of (a) 10^{18} cm^{-3}, (b) 5×10^{18} cm^{-3}, and (c) 10^{19} cm^{-3}.

The subthreshold current is higher in silicon than in germanium in junctionless transistors. This happens because of higher κ (dielectric constant) value of germanium (16.2) than silicon (11.7). The gate electric field depletes the electrons in the channel region and higher dielectric constant means that the gate field is more amplified in germanium than in silicon making electron concentration in channel even less in germanium. Thus in germanium junctionless transistors, the subthreshold current is lower than silicon whereas the saturation current is still higher in germanium.

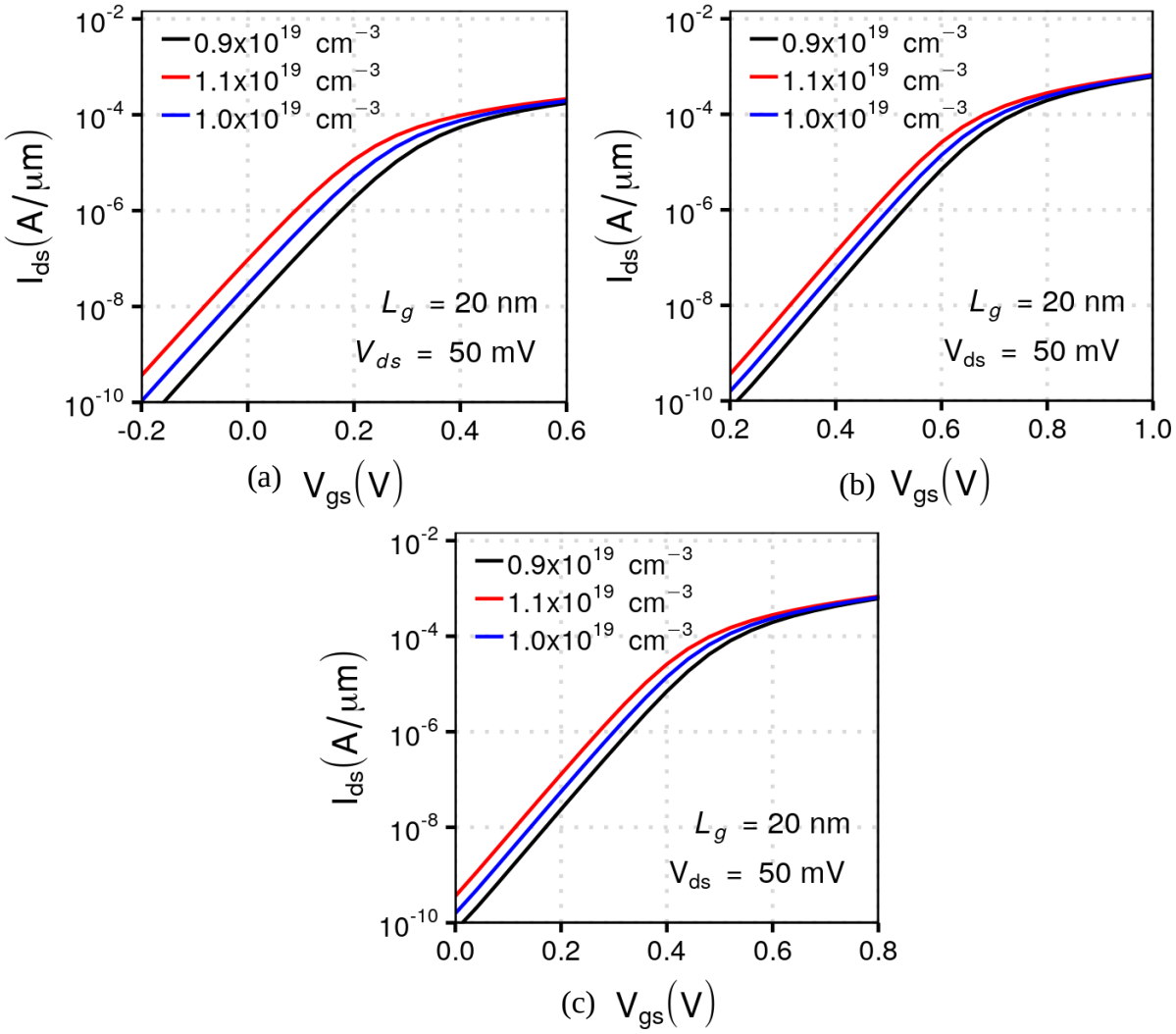

Figure 4.2: I_{ds} - V_{gs} characteristics junctionless transistors for ±10% change in doping levels for (a) silicon (wf = 5.0 eV), germanium ((b) wf = 5.2 eV, (c) 5.0 eV).

Variability depends on three parameters, which are doping levels, material, and scaling of the device dimensions. In order to understand in a very classical sense the effect of changing

material and doping levels, we calculated the sensitivity of threshold voltage (V_{th}) to changing doping levels. This quantity is a ratio of relative change in threshold voltage (V_{th}) to the relative change in doping levels. This was calculated for both silicon and germanium junctionless transistors for ±10% change in doping levels. Figure 4.2 shows the I_{ds} - V_{gs} characteristics for silicon and germanium devices for changing gate work-function (*wf*).

Material	**Silicon (*wf* = 5.0 eV)**	**Germanium (*wf* = 5.0 eV)**	**Germanium (*wf* = 5.2 eV)**
Sensitivity	1.6	0.46	0.90

Table 4.1: Threshold Voltage sensitivity calculated for different work-function (*wf*) and materials for ±10% change in doping levels.

The sensitivity parameters are tabulated in table 4.1 as shown. We see that the value for silicon is much higher compared to germanium for both values of work function. This indicates that threshold voltage is more susceptible to change in silicon junctionless transistor than in germanium. The I_{ds} - V_{gs} characteristics of silicon are more spread out in silicon than in germanium, reaffirming the higher threshold voltage sensitivity of silicon junctionless transistor.

If we look at the I_{ds} - V_{gs} characteristics of germanium junctionless transistor for two different work-functions, we observe that changing the work function resulted in only a shift in the current characteristics and its spread remains the same.

Thus in a very classical sense, the variability seems to decrease when we switch from silicon to germanium as the channel material. With these results as a basis, we try to incorporate the analysis for RDF in germanium junctionless transistors and then compare to see whether there is a decrease in the variability.

4.2 Variability in Ge-Junctionless Transistors

We observe in section 4.1 that germanium junctionless transistor are less sensitive to threshold voltage change. We also understand how the introduction of dopant changes the threshold voltage. In order to understand how the perturbation caused by the dopant differs in both the materials, we compare the potential distribution corresponding to maximum variation.

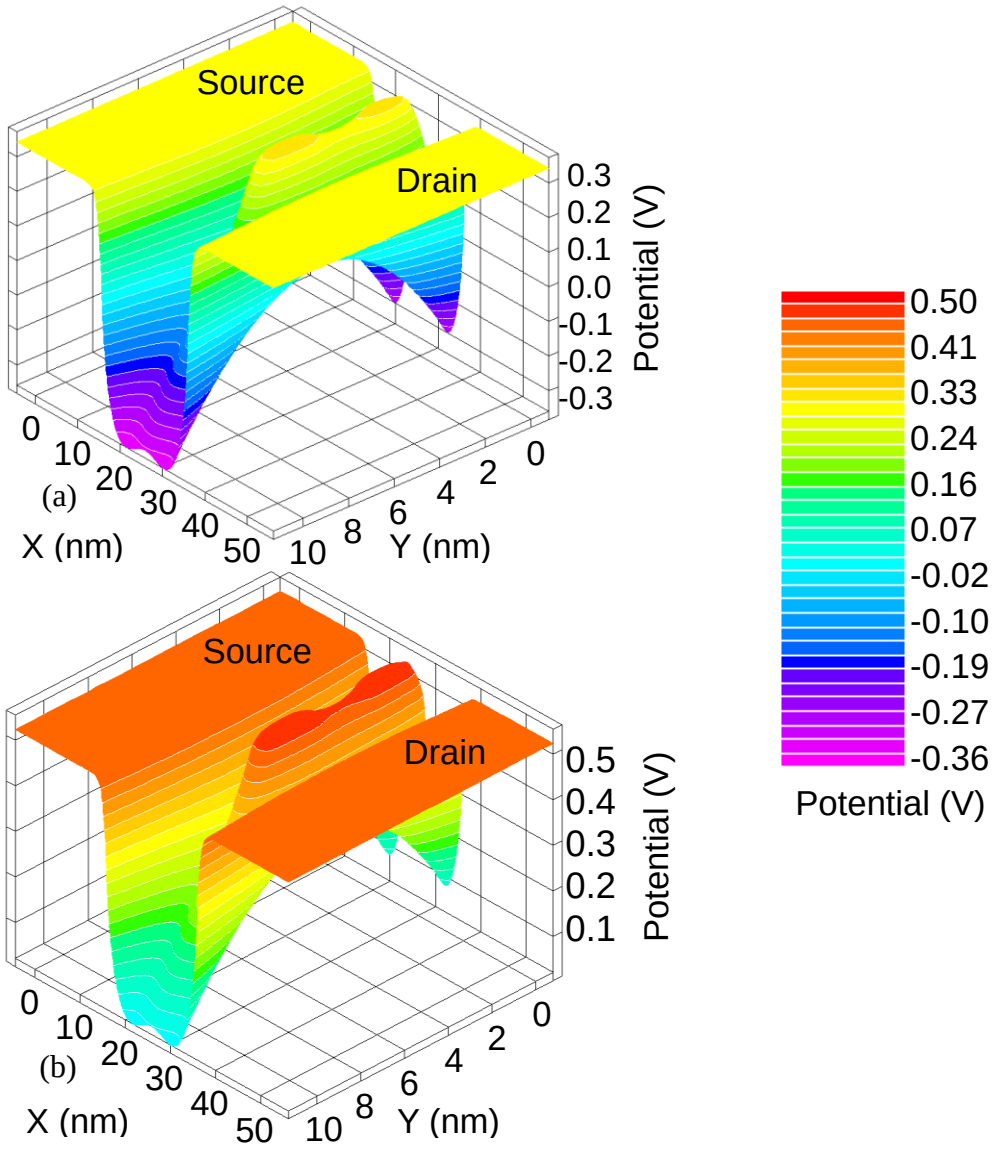

Figure 4.3: Potential distribution comparison for the dopant location corresponding to a maximum change in (a) Germanium and (b) Silicon.

The potential profiles in figure 4.3 appear similarly distorted for silicon and germanium except that their absolute values are much higher in silicon than germanium. So in order to find out how much the variation in Ge-JL Transistor is, we performed one hundred simulations on germanium device. Additionally, in order to completely compare the variation in threshold voltage (V_{th}), we performed a hundred simulations in silicon and germanium at the same position of dopant atoms. The simulation result is plotted in figure 4.4.

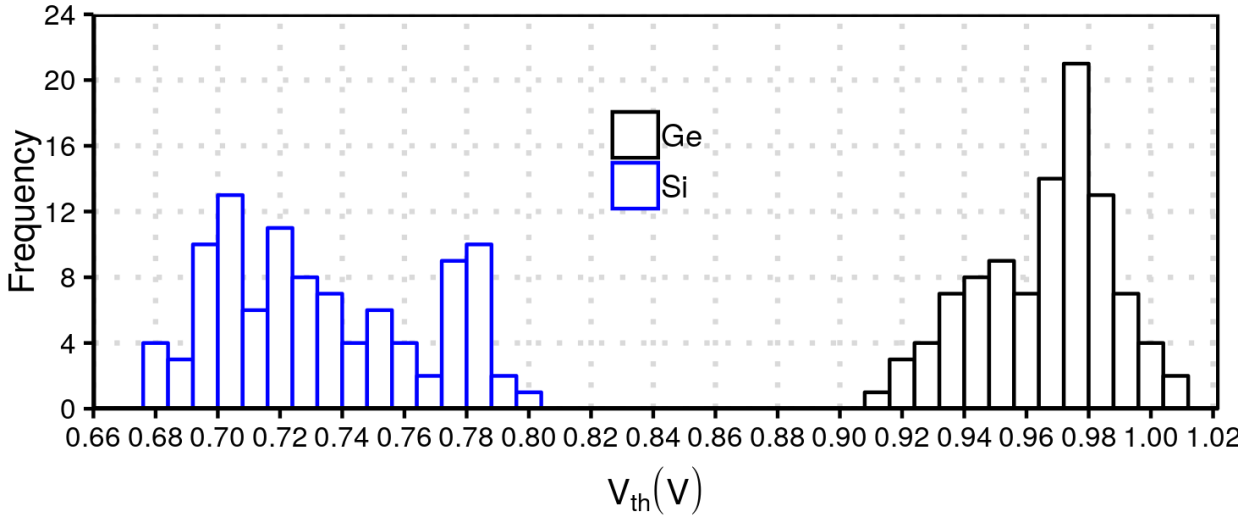

Figure 4.4: Threshold Voltage distribution for 100 simulations in germanium and silicon.

Material	**σV_{th} (mV)**	**ΔV_{th} (mV)**
Silicon	32.97	120.00
Germanium	21.50	96.00

Table 4.2: Threshold voltage variation (σV_{th}) and total spread (ΔV_{th}) for 100 simulations for silicon and germanium.

Threshold voltage variation (σV_{th}) is the standard deviation of all the hundred observations and total spread (ΔV_{th}) is the difference between the minimum and maximum values of the observation for the material. In both, these parameters germanium shows an improved performance than the silicon junctionless transistors.

4.3 Analysis of Variation Difference in Silicon and Germanium

To understand why the change in germanium is less as compared to silicon, we compare the change in electron concentration of RDF structure from the uniformly doped ideal device (n_e). This is shown in figure 4.4 and figure 4.5 which structures for maximum and minimum variation respectively. This shows the perturbation by the dopant atom in both the structures.

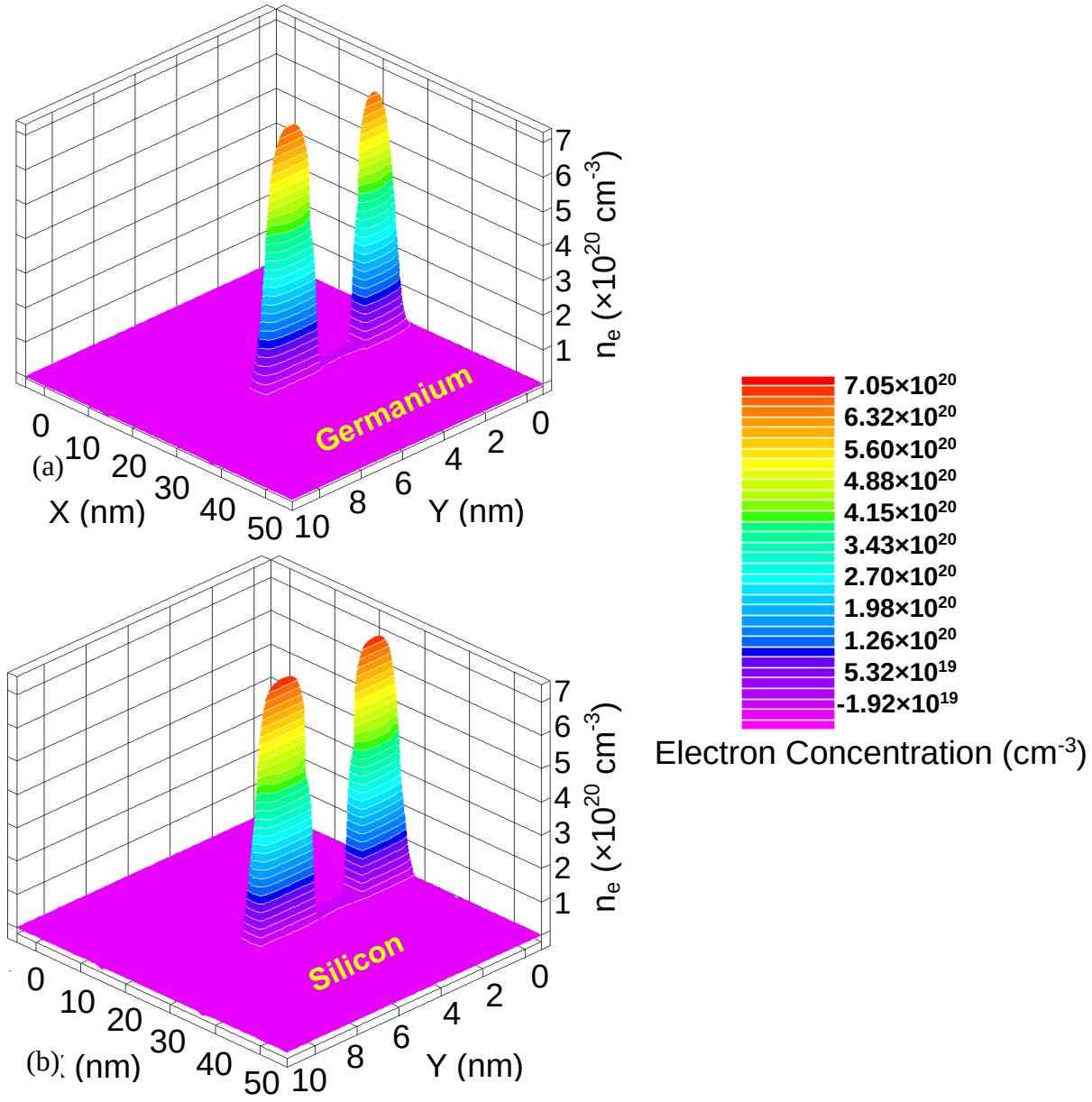

Figure 4.5: Electron concentration difference between RDF simulation and uniformly doped ideal device for dopant positions for maximum variation in (a) Germanium and (b) Silicon.

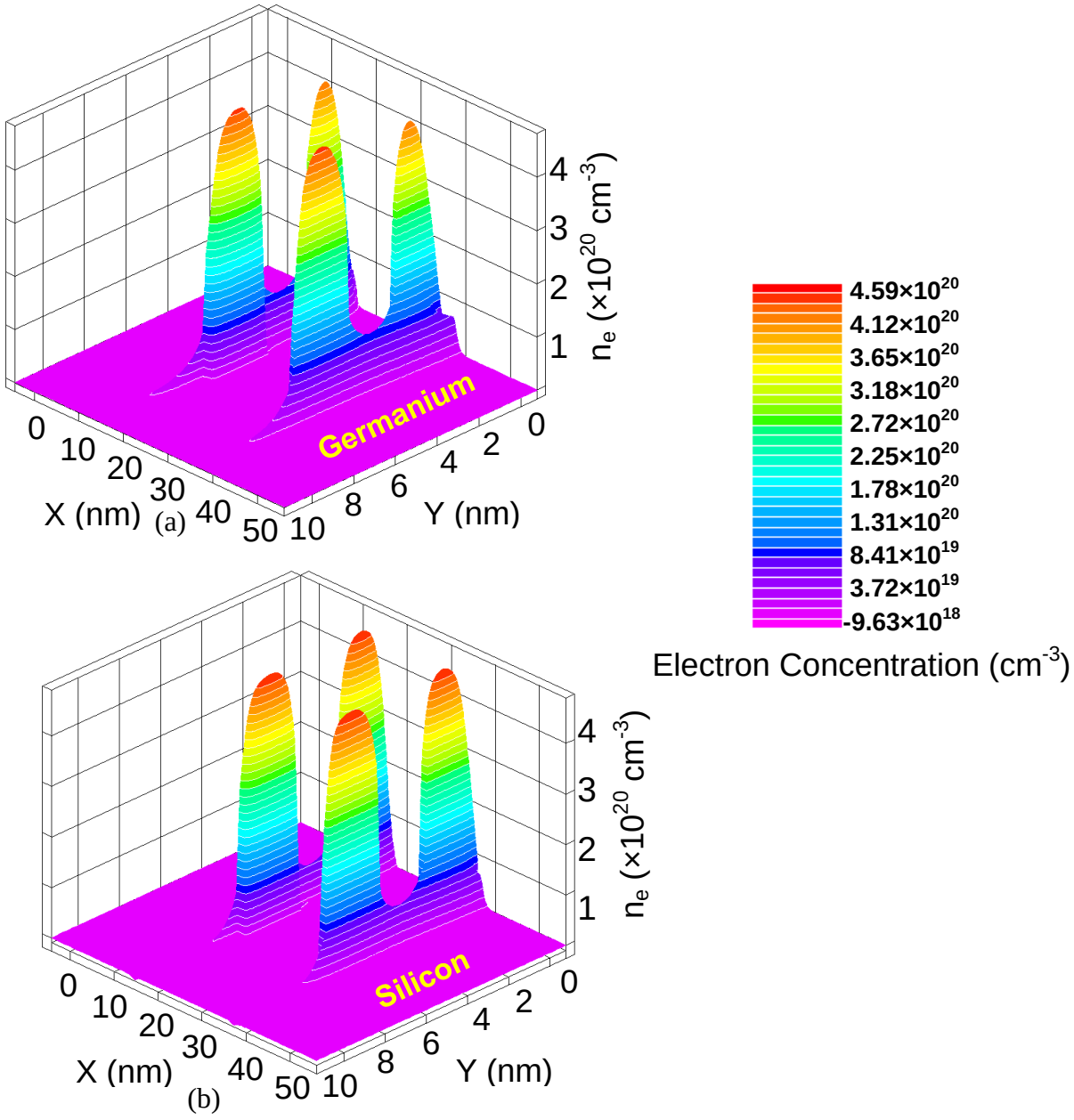

Figure 4.6: Electron concentration difference between RDF simulation and uniformly doped ideal device for dopant positions for minimum variation in (a) Germanium and (b) Silicon.

We observe from figure 4.4 and figure 4.5 that maximum value of the difference in electron concentration (n_e) is more in silicon, for both the dopant locations corresponding to the minimum or maximum variation, than germanium. Even the width of the electron concentration profile at the top is more in silicon than in germanium. These observations essentially suggest that change or variation due to the presence of a dopant is profoundly expressed in silicon whereas in germanium it is less than silicon.

4.4 Conclusion

In this chapter, we have compared the Si-JL transistor with Ge-JL transistor. By studying the output characteristics for Ge-JL transistor we observe that the device with germanium channel material is feasible, unlike conventional MOS transistor. The Ge-JL transistors have lower subthreshold current due to their high κ value but still, have a higher saturation current.

When variability is studied in the classical sense as in section 4.1 we find that the change in threshold voltage is more in silicon with the same change in doping level. With this idea in mind, we explore the effect of scaling the device dimensions in JL transistors and study the effect of RDF. We compare the threshold voltage variation (V_{th}) for both the materials. Our finding reveals that both the threshold voltage variation (σV_{th}) and absolute spread of the values (ΔV_{th}) is much lower in germanium.

We have also tried to understand why the change is less in case of germanium in section 4.3 where we use the difference in the electron concentration of RDF structure and ideal uniformly doped device as a measure of perturbation. We find that the perturbation is suppressed in case of germanium. One of the reasons for this is the higher κ values of germanium which causes the localized higher concentration to deplete more. Thus with germanium as a choice of device material and choosing appropriate gate work-function (*wf*), the variability due to the presence of random dopant can be reduced.

Chapter 5

Conclusion and Future Work

5.2 Conclusion

In the analysis, we have focused on the Junctionless transistors which bypasses the requirement of the concentration gradient in the doping profile. Thus, these transistors can be used in future technology nodes due to their simpler fabrication and full CMOS functionality.

In the work, we first discussed about the conventional MOS transistors which are used in almost all nanotechnology applications. These transistors use junctions to start or stop the current in the channel. The conventional MOS transistor suffered many drawbacks when their dimensions were scaled. In chapter 1, we discussed the SCEs and the variation in threshold voltage they cause because of lesser gate controllability in the channel region. This issue was mitigated by using Multi-Gate FETs which suppressed the SCEs and increased the gate control over the channel region by surrounding the channel with gate contact. However, as the current technology drive is towards miniaturization continues even Multi-Gate FETs face issues in downscaling. The two major issues being threshold voltage (V_{th}) variation and requirement of ultra-sharp doping profiles. The requirement of ultra-sharp doping profile is a major hurdle when the gate length approaches 10 nm. It is due to statistical and diffusion laws of nature that the abrupt doping profile is either unattainable or process is too complex and costly to be carried out for manufacturing the transistors. J.-P. Colinge's group [3] have proposed a novel device which bypasses this requirement of the concentration gradient in the channel region. This device has no junctions and hence the name junctionless transistor. The device displays full CMOS functionality and has a simpler fabrication process which makes it a possible candidate for future technology nodes.

Before these devices are mass produced they must be checked for variability. The variability in junctionless in due to the phenomenon of RDF (Random Dopant Fluctuation). In chapter 2 we have discussed the phenomenon and tried to select a mathematical model whose simulation results accurately represent the variation due to RDF. One such model is Shin's model [31] which divides the channel region into square regions and uniformly dopes the regions where the dopant is present in the channel. The equations of the other parameters required are also

worked out by Tang's group [8]. Our workflow uses Shin's model on the junctionless transistor to analyze the effect of RDF. We did two separate analysis, one with a single dopant atom to reveal the effect of position on the change in threshold voltage (V_{th}) and other with 4 dopants to evaluate the criticalness of the issue.

Analysis with a single dopant has been done on DG-MOSFET by Chiang's group [33]. We used a similar approach to understand the effect of location of dopant in the channel in JL transistors. Our analysis reveals that dopant when present in the center of the channel causes larger variation in the threshold voltage (V_{th}) than the dopant present near the source or drain. We then decide 8 locations on the basis of the previous analysis, 4 corresponding to maximum variation and 4 corresponding to minimum variation. We analyze the potential contour plots to reveal that source or drain region can influence the perturbation caused by the dopant. Thus when the dopant is present near to the source or drain region, it being close to an equipotential wall with almost the same electron concentration has its perturbation 'absorbed' the source/drain region. But when the dopant is present at the center of the channel the source/drain region cannot influence the perturbations and it causes a localized increase in the potential which aids in channel formation. This lowers the threshold voltage considerably.

One of the aims of the project was to evaluate whether this threshold voltage variation is a critical issue. To achieve that we used the Shin's model but this time allowed the random positioning of dopant atoms. We performed 100 such simulations are evaluated the threshold voltage variation (σV_{th}) is nearly 33 mV and the spread of the values is 120 mV, which is quite high. To reduce this variability we revisited our idea of classical checking of variability. So we performed the same analysis with the Ge-JL transistor and we report the values for threshold voltage variation (σV_{th}) is nearly 22 mV and the spread of the values is 96 mV. This is a considerable decrease in the variability from the Si-JL transistor.

In chapter 4 we have compared the Si-JL transistor with Ge-JL transistor. By studying the output characteristics for Ge-JL transistor we observe that the device with germanium channel material is feasible, unlike conventional MOS transistor. The Ge-JL transistors have lower subthreshold current due to their high κ value but still, have a higher saturation current.

When variability is studied in the classical sense as in section 4.1 we find that the change in threshold voltage is more in silicon with the same change in doping level. With this idea in mind, we explore the effect of scaling the device dimensions in JL transistors and study the effect of RDF. We compare the threshold voltage variation (V_{th}) for both the materials. Our

finding reveals that both the threshold voltage variation (σV_{th}) and absolute spread of the values (ΔV_{th}) is much lower in germanium.

We have also tried to understand why the change is less in case of germanium in section 4.3 where we use the difference in the electron concentration of RDF structure and ideal uniformly doped device as a measure of perturbation. We find that the perturbation is suppressed in case of germanium. One of the reasons for this is the higher κ values of germanium which causes the localized higher concentration to deplete more. Thus with germanium as a choice of device material and choosing appropriate gate work-function, the variability due to the presence of random dopant can be reduced.

5.2 Future Work

In the future, further analysis of different architecture [34] and materials [35] which reduce the variability can be explored. This analysis can be used to better the performance of nanoscale transistors for upcoming technology by suitable choice of material. The analysis must not be limited in one dimension, and hence, the understanding device physics, as well as the challenges in designing, will go hand in hand to contribute innovative ideas which are both simpler and feasible.

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