Effect of Parasitic Capacitance on Analog/RF Performance of MOS Transistors

A PROJECT REPORT

Submitted in partial fulfillment of the requirements for the award of the degrees

of
BACHELOR OF TECHNOLOGY
in

ELECTRICAL ENGINEERING

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INDIAN INSTITUTE OF TECHNOLOGY INDORE
December, 2018

CANDIDATE'S DECLARATION

I hereby declare that the project entitled **"Effect of parasitic capacitance on analog/RF performance of MOS transistors"** submitted in partial fulfillment for the award of the degree of Bachelor of Technology in 'Electrical Engineering' completed under the supervision of **Abhinav Kranti, Professor** IIT Indore is an authentic work.

Further, I declare that I have not submitted this work for the award of any other degree elsewhere.

Signature and name of the student(s) with date

CERTIFICATE by BTP Guide(s)

It is certified that the above statement made by the students is correct to the best of my knowledge.

Signature of BTP Guide(s) with dates and their designation

Preface

This report on “Effect of parasitic capacitance on analog/RF performance of MOS transistors" is prepared under the guidance of Professor Abhinav Kranti.

The aim of this paper is to calculate the MOSFET parasitic capacitances, and then based on the results obtained we can further see the impact of parasitic capacitance on analog/ RF properties of MOS transistors.

Parasitic capacitances have a direct impact in the operation of MOSFET designed for analog/RF and logic applications. Therefore, in order to increase functioning of a MOS transistors, it is necessary that the parasitic capacitances are reduced to a minimum possible level that the technological process allows. Analysis has been done with respect to various technological parameters and efforts have been made to reduce the effect of parasitic capacitance for better analog/RF performance.

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Abstract

As the transistor dimensions are continuously scaled down to nanoscale regime, various factors govern the performance of the transistor. Among all undesirable effects, parasitic capacitance has shown considerable effect on the analog/RF performance of the transistor. Therefore, the aim of the project is to successfully evaluate the various parasitic capacitances present in a Metal Oxide Semiconductor Field Effect Transistor (MOSFET). For this, the MOS devices have been analyzed with comprehensive simulations considering numerous technological parameters and their effect on parasitic capacitance. After analyzing the effect of structural parameters on the parasitic capacitance, the MOS structure is optimized and its analog/RF performance is compared with non-optimized transistor. Results indicate that the cut-off frequency, a crucial analog/RF metric, can be improved significantly by lowering the parasitic capacitance.

Table of Contents

Chapter 1

1.1 INTRODUCTION

MOS ICs have met the world's growing needs for electronic devices for computing, communication, entertainment, automotive, and other applications with steady improvements in cost, speed, and power consumption. Such steady improvements in turn stimulate advancements in technologies and applications [1]. There is now an entrenched expectation that this trend of rapid improvements will continue.

Gordon Moore made an empirical observation in the 1960's that the number of devices on a chip doubles every 18 months or so [2]. The "Moore's Law" is an accurate description of the continual increase in the series of miniaturization. Reductions in size, weight, and cost of power supplies are continuously being demanded by the miniaturization trend of industrial and consumer electronics. The primary engine that powered the ascent of electronics is "miniaturization". By making the transistors and interconnects smaller, more circuits can be fabricated on each silicon wafer, and therefore, each circuit becomes cheaper. Miniaturization has also been an auxiliary to the improvements in speed and power consumption. This practice of periodic size reduction is called scaling. MOSFETs are a core of integrated circuit and can be designed and fabricated in a single chip because of these very small sizes. To summarize, scaling has improved cost, speed, and power consumption with every new technology generation since its start.

With the rapid growth of CMOS (Complementary Metal Oxide Semiconductor) technology due to its scaling, it has evolved as the mainstream of analog/RF technology due to its low cost, low power and high integration. The MOSFET is widely used for switching and amplifying electronic signals in the electronic devices. The advanced performance of CMOS is attractive for RF circuit design in view of a system-on-chip realization, where digital, mixed-signal baseband and RF transceiver blocks would be integrated on a single chip [3]. Recently, with the development of a highly-information-oriented society, the RF (Radio-Frequency) wireless communications market dramatically grows up. In the future, the demands of RF wireless technology will continue to increase all the more in various areas, e.g. our daily life, industrials and medicals. These demands are realized by the development of semiconductor products. Thus, MOS technology comes to be important for the RF technology of wireless applications.

But the constant downscaling leads to certain unwarranted problems such as DIBL, sub-threshold current, parasitic capacitance, V_t roll-off to name a few. In this thesis we examine the

various parameters that affect the parasitic capacitance and the effect of parasitic capacitance on analog/RF properties of MOS transistors.

1.2 INTRODUCTION TO PARASITIC CAPACITANCE

1.2.1 MOS Transistors

MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) is a voltage controlled FET where the current flow through the channel between the source and the drain is controlled by the voltage applied to the gate which is isolated from the channel by an insulator. MOS transistors are an integral component of today's digital electronics world. They are used widely as switches, oscillators, amplifiers and mixers.

The MOSFET's working is based on the MOS capacitor. The MOS capacitor works in accordance with the gate-source voltage which forms a channel between the drain and source. Thus, it has three modes of operation namely:

(i) **Accumulation** in which same type of carriers accumulate at the surface

(ii) **Depletion** in which the surface does not have presence of any charge carriers and is empty

(iii) **Inversion** in which the surface has charges of opposite character accumulated at the bottom of the plate.

Additional capacitances existing in the device are examined in this paper and analytical modelling of MOSFET is done for accurate extraction of various stray capacitances.

1.2.2 Characteristics of a MOS transistor

Fig 1.1 shows the I-V characteristic of a MOSFET with gate length 50 nm, V_{ds}=50 mV, and height of electrodes at 50 nm. Fig 1.1a is in logarithmic scale while Fig1.1b is in linear scale.

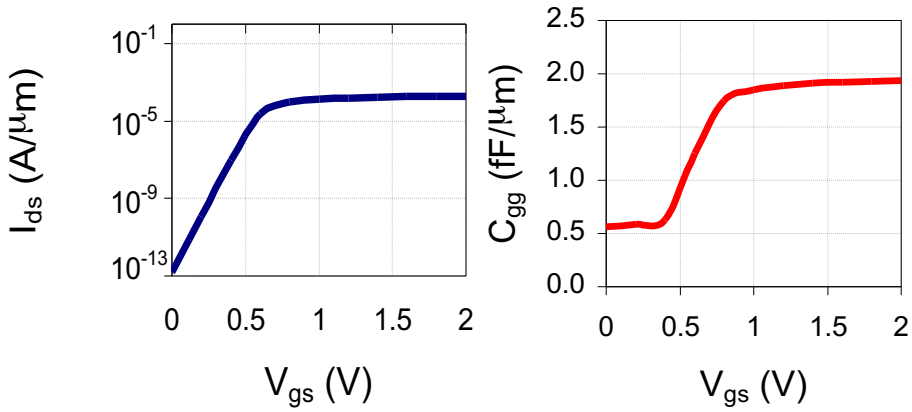

Fig 1. I_{ds} vs V_{gs} and C_{gg}-V_{gs} graph for a MOSFET

1.2.3 Parasitic Capacitance

Parasitic capacitance or stray capacitance is an unavoidable and usually unwanted capacitance that exists between the parts of an electronic component or circuit simply because of their proximity to each other. With persistent reduction of MOS transistor dimensions, the parasitic capacitances are becoming an overbearing issue for designing logic circuits. Consequently, the effect of parasitic capacitance should not be neglected anymore, as it could begin to dominate the total gate capacitance behavior below a certain technology node. For example, the gate parasitic capacitances would degrade the ring oscillator delay by more than 30% in a 45 nm technology node [4].

For analog application, a negative feedback through them will influence the gain-bandwidth product and transconductance. For RF applications, these capacitances can affect the transport delays, cut-off frequency, and maximum frequency of oscillation. This can be critical to the functioning of a MOSFET. Hence, the focus of the project is to analyze the impact of parasitic capacitance on analog/RF properties of the MOS transistors in the sub-100 nm technologies.

Considering the MOSFET's structure, these capacitances are distributed in nature and their exact calculation is quite complex. Various models have been previously developed such as the *Elmasry and Centner Model (EC model)* [5], [6], *Shrivastava Model (S Model)* [7] and the *Kamakouchi* model for capacitance modelling.

For the gate fringe capacitances, various analytical models have been presented in our work, with the consideration of physical dimension and device structure. Using simple

approximations, the parasitic capacitances can be extracted from the total gate capacitance of MOSFET. The parasitic capacitance can be divided into two components i.e., fringe capacitances and inter-electrode capacitance. The fringe capacitance is related to outer fringing capacitance and inner fringing capacitance. The total gate capacitance is given by:

$$C_{gg} \approx \text{Series}\,(C_{ox}, C_{si}) \,||\, C_{of} || \, C_{if} || \, C_{ov} \,||\, C_{int1} \,||\, C_{int2}$$

Where C_{ox} is the oxide capacitance, C_{si} is the silicon body capacitance, C_{if} is the inner fringing capacitance and C_{of} is the outer fringing capacitance, gate-to-source/drain overlap (C_{ov}) and inter-electrode capacitance (C_{int1}/C_{int2}) between gate to-source/drain electrodes, as shown in Fig. 2.

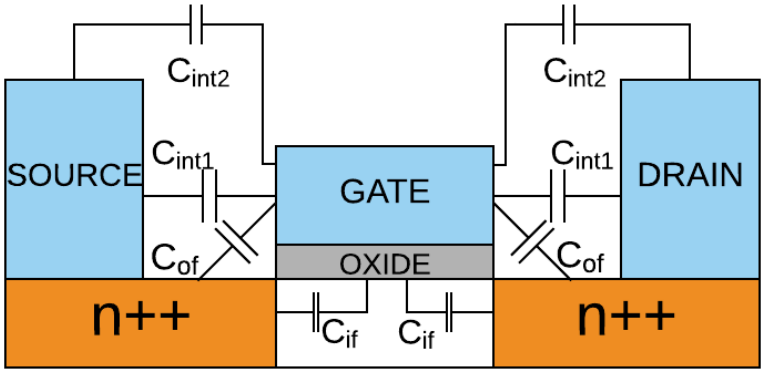

Fig 2. MOSFET with various parasitic capacitances

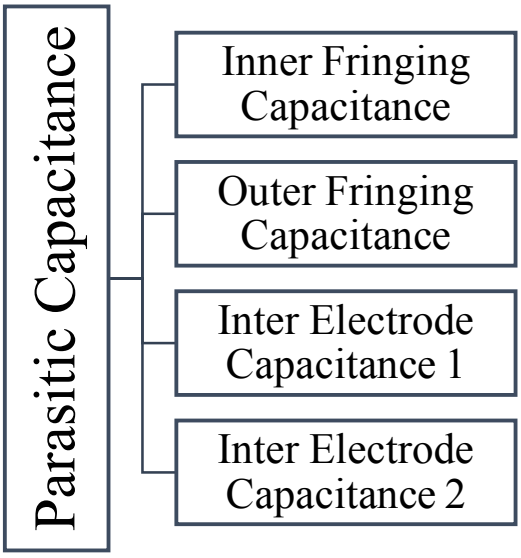

Fig 3. Schematic showing breakdown of parasitic capacitance

In this work, we present an analytical gate fringe capacitance model for sub-100 nm MOSFET technology, considering process fluctuations with the aim of properly determining the fringing extrinsic components. The increasing contribution of parasitic capacitances and series resistances has become a challenge since the 90-nm technology node [8]. Fig. 3. Shows the various capacitances studied in this paper. After evaluation of the various components its effect on analog/RF properties is observed and the suitable variations are adopted that give the least parasitic capacitance.

Chapter 2

2.1 METHODOLOGY

The first step in our analysis is to create a MOSFET structure which provides the basis for the various process fluctuations to be observed. A MOSFET device is simulated in which gate length(L_g) of 50 nm and oxide thickness (t_{ox}) of 1 nm is observed. Further the source-drain voltage(V_{ds}) is kept at 50 mV. Gate Capacitance is observed at V_{gs} ranging from -0.5 to 2 V and necessary data is extracted. Other parameters such as height of source/drain electrodes, height of gate electrode, distance between electrodes etc., are varied to get the best case scenario.

2.2 EXTRACTION OF PARASITIC CAPACITANCE

2.2.1 Inner Fringing Capacitance

An analytical model for inner fringe capacitance has been developed in which the height of all the three electrodes viz. source, gate and drain is fixed at 0 nm. C_{gc} only appears when the device is turned on, i.e., when an inversion layer is formed and shields the substrate from the gate [9]. The parallel plate capacitance model is used to model inner fringing capacitance (C_{if}).

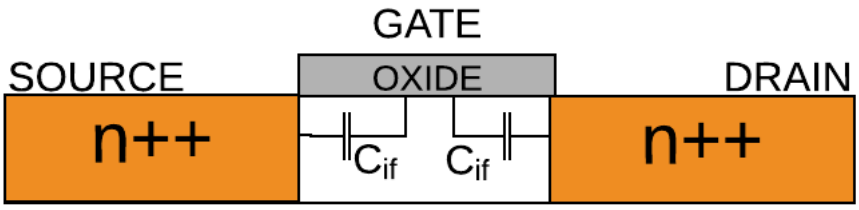

Fig. 4. Device schematic of inner fringing capacitance

Gate Capacitance at -0.5 is observed when no channel exists in the transistor. Ideally the capacitance should be 0, but experimental data shows that a capacitance is existing in the device. This is known as the inner fringing capacitance. The gate capacitance at -0.5 V is 0.355 fF/μm which is the total inner fringing capacitance present in the device.

2.2.2 Inner Fringing Capacitance at Overlap

In order to understand the effect of various factors on parasitic capacitance, an overlap is introduced in the device to observe its effect on the inner fringing capacitance. The gate overlap on the source and drain wells is varied from 0-15 nm. The source and drain overlap regions are usually equal due to the symmetry of the MOS devices.

$$L_{eff}=L_g-2L_o$$

(Where L_{eff} is effective channel length)

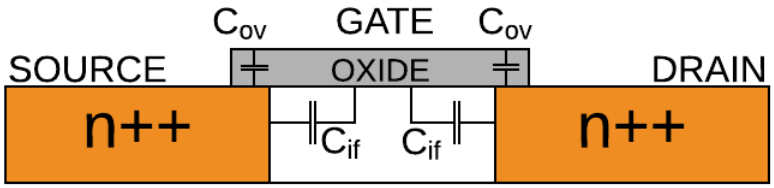

Fig. 5. Device schematic for inner fringing capacitance at overlap

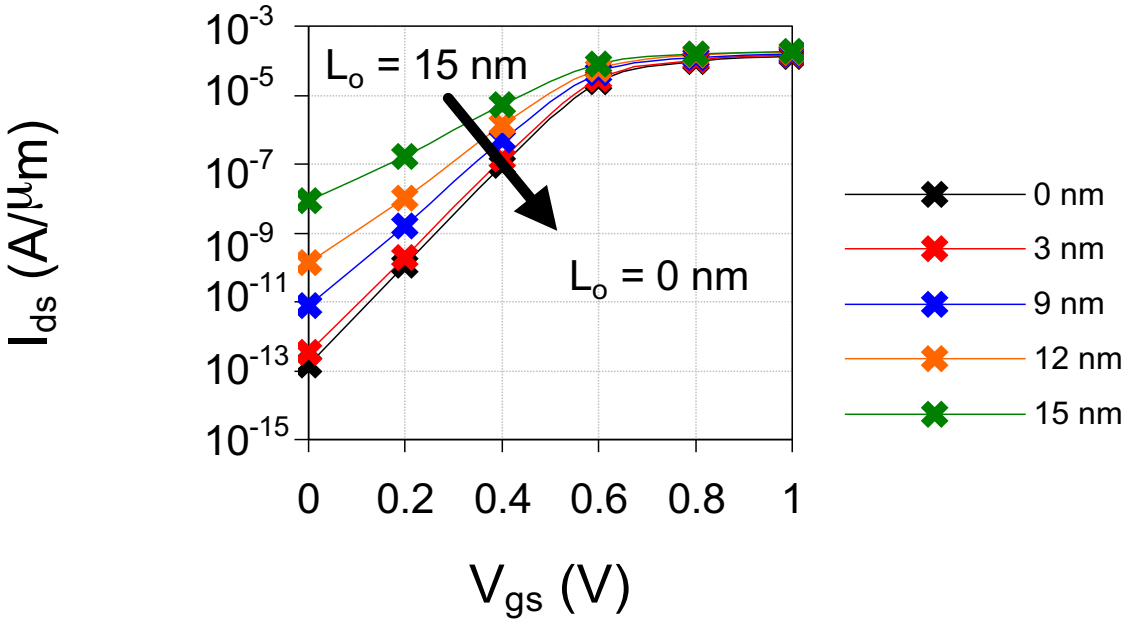

Fig. 6. I_{ds}-V_{gs} characteristics of MOSFET with overlap (Logarithmic scale)

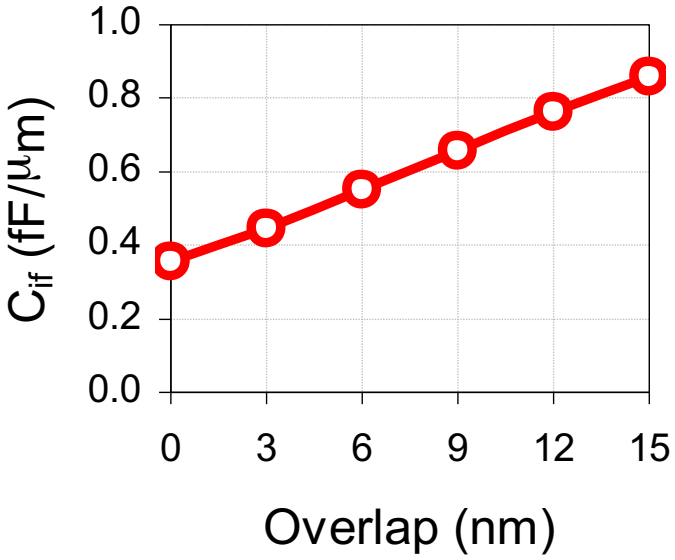

Fig. 7. C_{if} vs Overlap characteristics

1. From Fig. 6. it is observed that with the introduction of overlap in device the current in the OFF-state becomes prominent as the overlap increases.
2. From Fig. 7. It can be seen that with increasing overlap, the inner fringing also increases.

   Thus, introducing an overlap contributes to parasitic capacitance which is contrary to our purpose of study. This is not a desirable effect in MOSFET working.

2.2.3 Inner Fringing Capacitance at Underlap

Fringe capacitance modelling is now observed by introducing an underlap in the device. This underlap is varied from 0-15 nm. The source and drain underlap regions are usually equal due to the symmetry of the MOS devices.

$$L_{eff}=L_g+2L_u$$

(Where L_{eff} is effectice channel length)

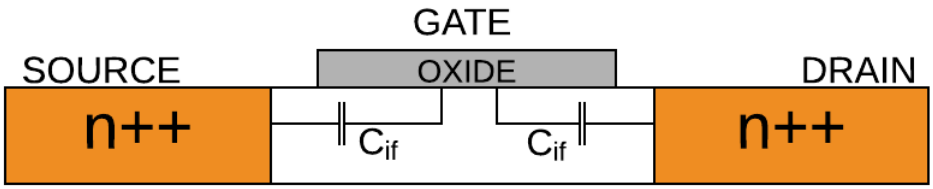

Fig. 8. Device schematic for inner fringing capacitance at underlap

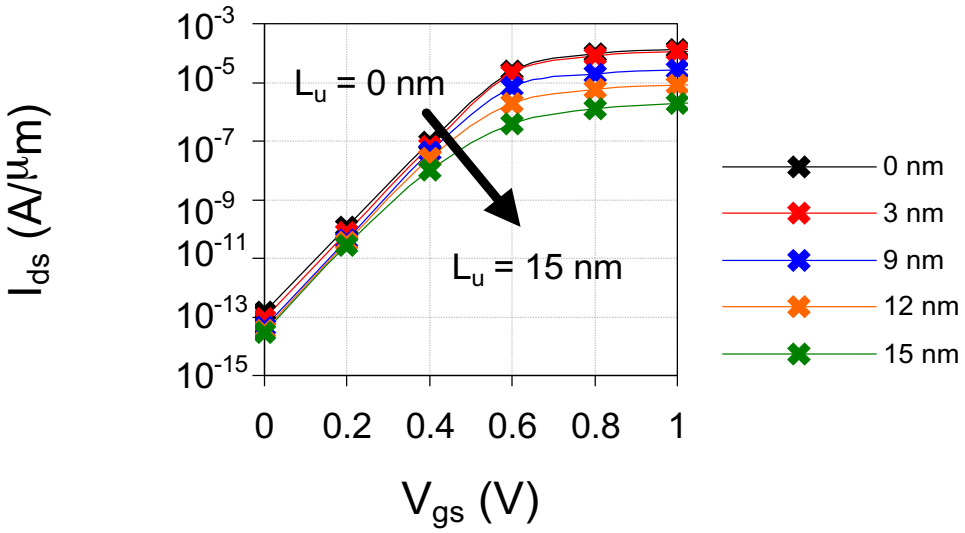

Fig. 9. I_{ds}-V_{gs} characteristics of MOSFET with underlap (Logarithmic scale)

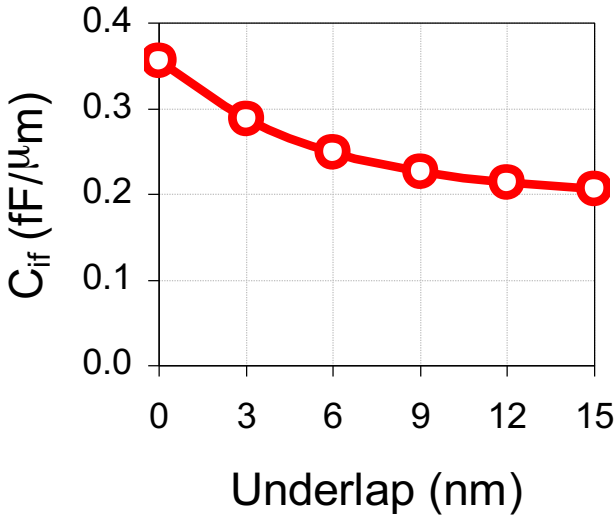

Fig. 10. C_{if} vs Underlap characteristics

From Fig. 9 and Fig. 10 it can be concluded that although at 15 nm the inner fringing capacitance is the least but the ON- state current is also very low as compared to no overlap. Thus, there is a trade-off between the inner fringing capacitance and the ON-state current.

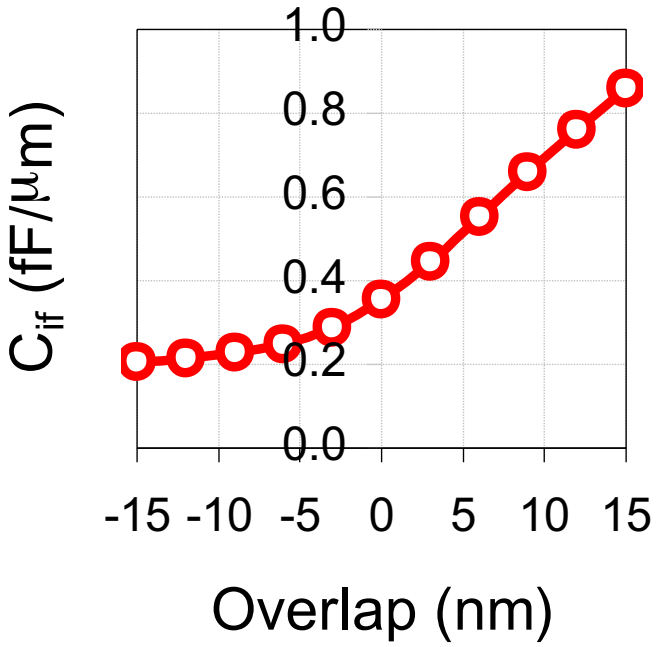

Fig. 11. C_{if} vs Overlap-Underlap characteristics

2.2.4 Outer Fringing Capacitance

Next we move on to our second parameter in study i.e., outer fringing capacitance. To evaluate outer fringing capacitance, the height of the source-drain electrodes is kept at 0 nm while the height of the gate electrode (H_g) is varied from 0-50 nm. Gate Capacitance is observed at -0.5 V for various values oh H_g and a graph is plotted as shown in Fig. 13.

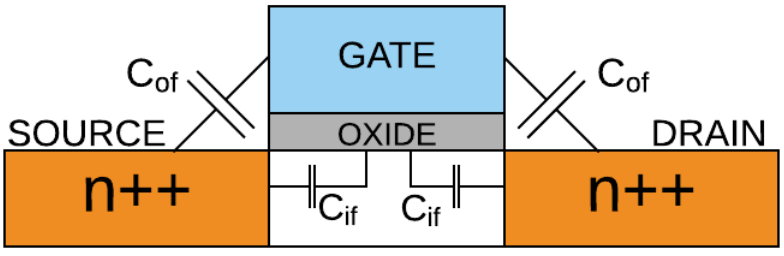

Fig. 12. Device schematic for outer fringing capacitance

The gate capacitance is observed at -0.5 V and inner fringing capacitance is subtracted to extract outer fringing capacitance.

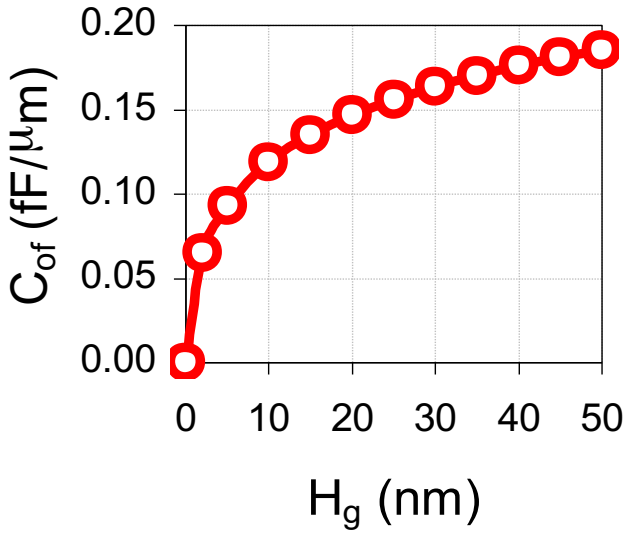

Fig. 13. C_{of} vs H_g characteristics

With increasing gate height, it is observed that the outer fringing capacitance is increasing. This holds in accordance with the fact that capacitance is directly proportional to the length of the plates.

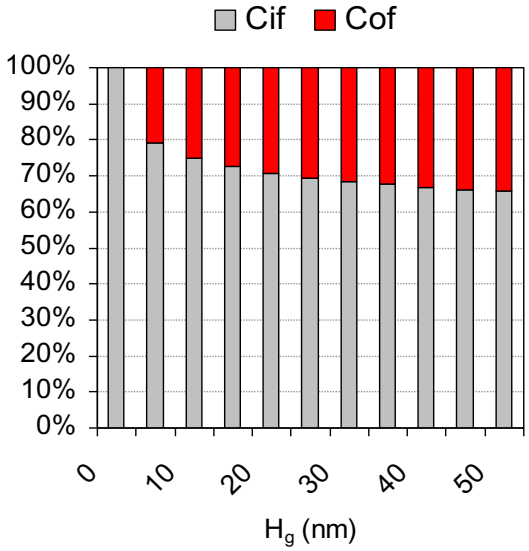

Fig. 14. Bar-graph showing percentage-wise breakdown of the various capacitances

A look at Fig. 14. shows that a major contributor of parasitic capacitance is inner fringing capacitance and as the height of gate electrode is increased the outer fringing capacitance becomes constant.

2.2.5 Inter Electrode Capacitance 1

As the height of source-drain electrode is increased from 0 nm another type of capacitance called inter-electrode capacitance (C_{int1}) comes into play. This capacitance is observed by varying the distance between the gate-source and gate-drain electrodes and keeping the height of the electrodes constant at 50 nm.

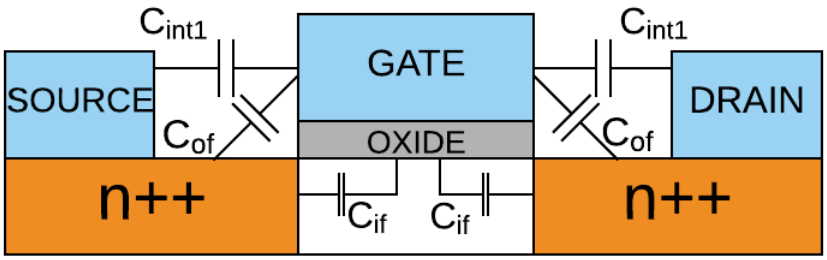

Fig. 15. Device schematic for outer fringing capacitance

The gate capacitance is observed at -0.5 V and (inner + outer) capacitance is subtracted to extract inter-electrode capacitance. Further the the spacer dielectric is kept as silicon dioxide which has about 3.9X- higher permittivity, thus C_{int} is even more significant than implied.

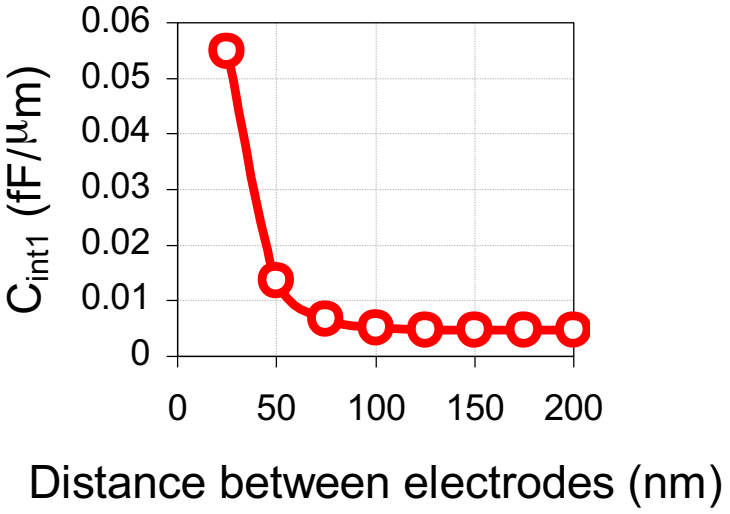

Fig. 16. (a) C_{int1} vs $L_{s,d}$

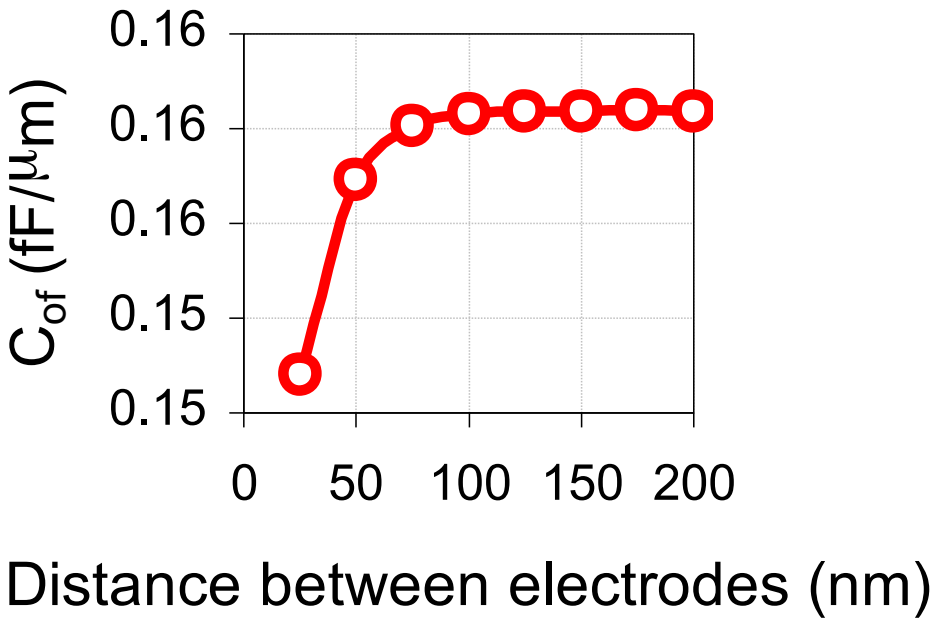

Fig. 16. (b) C_{of} vs $L_{s,d}$

Fig. 16. shows the variation of inter-electrode capacitance and outer fringing capacitance with respect to the distance between the electrodes. C_{int1} decreases as the distance between the electrodes increases. This holds up with the property of capacitance as it is inversely proportional to the distance between the plates.

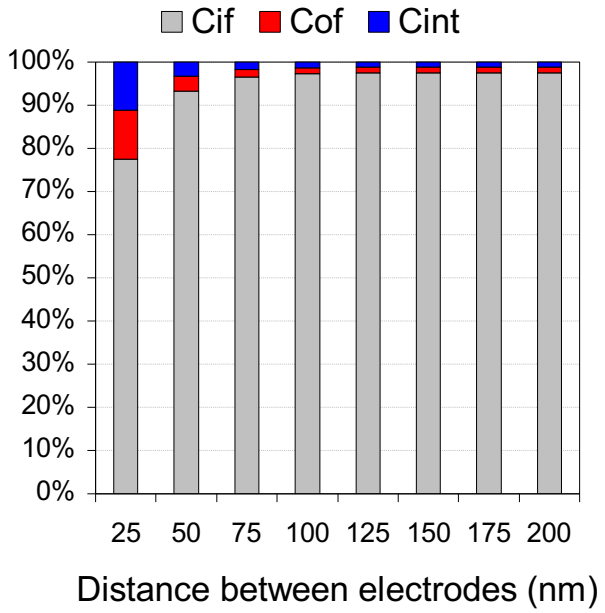

Fig. 17. Bar-graph showing percentage-wise breakdown of the various capacitances

From Fig. 17. We infer that a major contributor of parasitic capacitance is inner fringing capacitance. This data follows the same trend as observed in Section 2.2.4.

2.2.6 Inter Electrode Capacitance 2

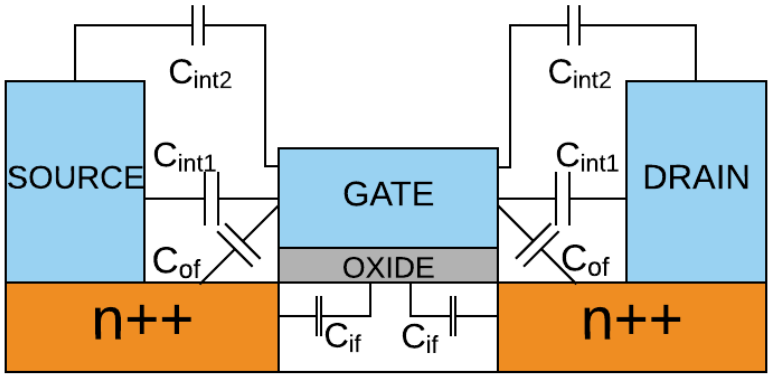

Fig. 18. Device schematic for inter-electrode capacitance 2

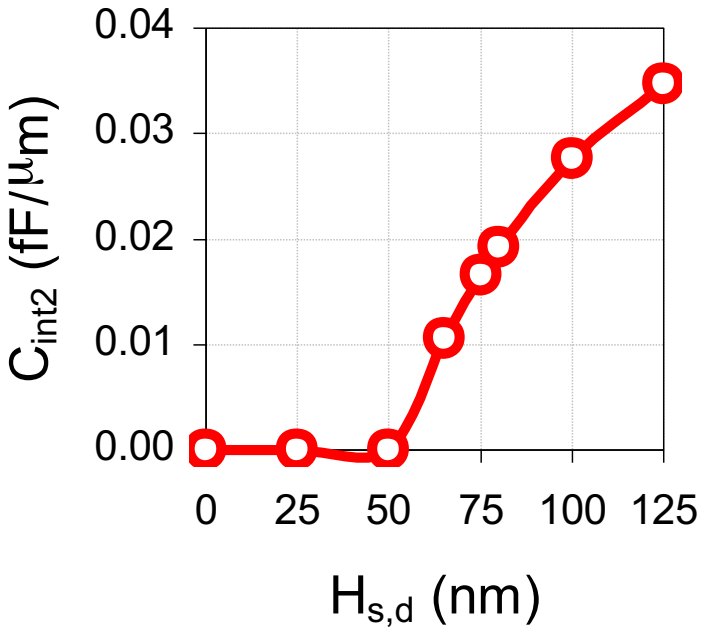

Fig. 19. C_{int2} vs H_g characteristics

Fringe capacitance model is observed when height of source-drain electrodes becomes greater than gate electrodes. A new capacitance called inter electrode capacitance 2 contributes to the total

parasitic capacitance. The parasitic capacitance observed at 50 nm is deducted from the gate capacitance at -0.5 V when the height is increases beyond 50 nm. This gives the inter electrode capacitance 2 depicted in Fig. 18.

Fig. 19. shows the graph between Cint2 and $H_{s,d}$ at a gate electrode height (H_g) of 50 nm and distance between electrodes ($L_{s,d}$) of 100 nm.

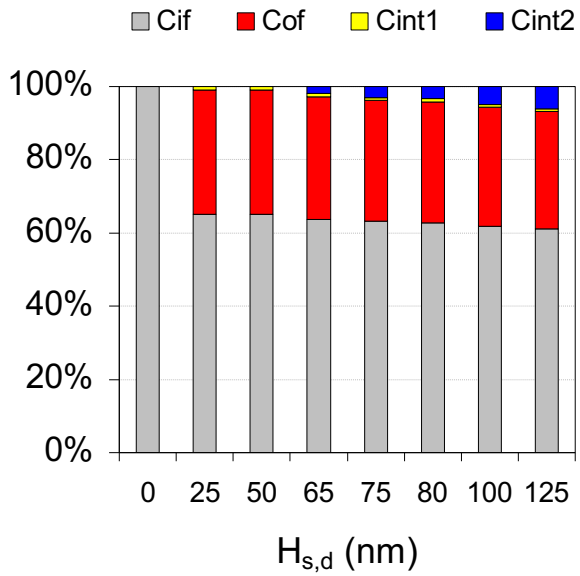

Fig. 20. Bar-graph showing percentage-wise breakdown of the various capacitances

The percentage wise breakdown of the various capacitances is shown in Fig. 20. The value of C_{int1} is negligible as compared to other capacitances.

2.3 CONCLUSION

- As overlap increases the inner fringing capacitance increases. Also the OFF-state current is greater at 15 nm as compared to 0 nm. Typically, this *overlap* is made as small as possible in order to minimize its parasitic capacitance.
- By introducing underlap, we observe that the inner fringing capacitance since it is inversely related to the distance between two electrodes.
- The ON-state current with underlap is less as compared to 0 nm. Thus, there is trade-off between parasitic capacitance and I_{ON}.
- It can be observed that inner fringing capacitance is a major contributor of parasitic capacitance in all the cases.

- Height of source-drain electrodes beyond 50 nm leads to introduction of additional inter-electrode capacitance.
- It should be noted that the above gate capacitances C_{gg}, C_{if}, C_{of}, C_{int1} and C_{int2} all originate from the coupling between the gate electrode and another region.

Chapter 3

3.1 RELATION BETWEEN PARASITIC CAPACITANCE AND GATE CAPACITANCE

The values of parasitic capacitance are crucial to the working of a MOSFET. The value of parasitic capacitance should not overpower the channel capacitance. In the following analysis we have examined the relation between parasitic capacitance and channel capacitance with respect to the various analytical parameters. Values where the ratio is greatest are favorable as it shows that the parasitic capacitance is negligible as compared to the channel capacitance which is the desired result. C_{gg} is observed at 2 V where a constant gate capacitance exists thus, indicating that a channel is formed. Parasitic capacitance is deducted from this to extract $C_{channel}$.

3.1.1 Varying Overlap-Underlap

A graph depicting the ratio of gate and parasitic capacitance is plotted versus the overlap in the device. The electrode heights are kept at 0 nm and the distance between the electrodes is kept constant at 100 nm.

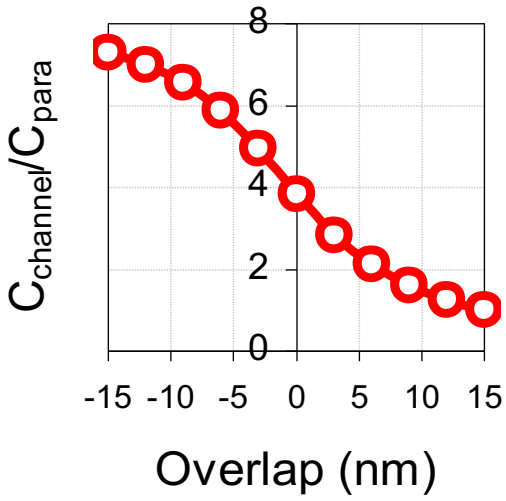

Fig. 21. Ratio of $C_{channel}/C_{para}$ vs Overlap-Underlap characteristics

3.1.2 Varying Gate Height

A graph depicting the ratio of gate and parasitic capacitance is plotted versus the height of gate electrode in the device. The height of source/drain electrodes is 0 nm and the distance between the electrodes is kept constant at 100 nm.

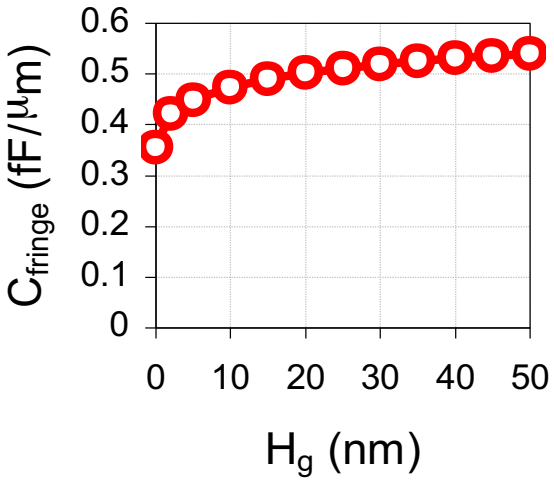

Fig. 22. C_{fringe} vs H_g characteristics

C_{fringe} is the total parasitic capacitance observed when the height of the gate is varied. This capacitance is subtracted from the total gate capacitance at 2 V to obtain $C_{channel}$.

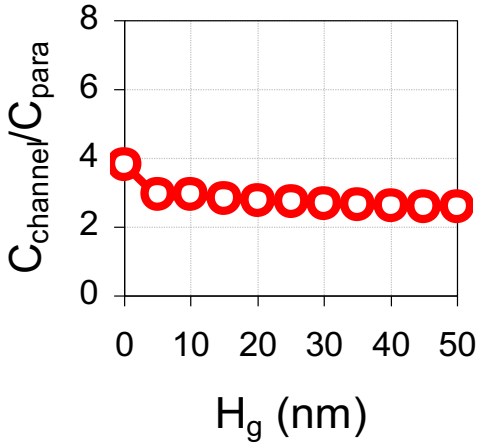

Fig. 23. Ratio of $C_{channel}/C_{para}$ vs H_g characteristics

3.1.3 Varying Distance between the electrodes

A graph depicting the ratio of gate and parasitic capacitance is plotted versus the distance between the electrodes. The height of the electrodes is kept constant at 50 nm.

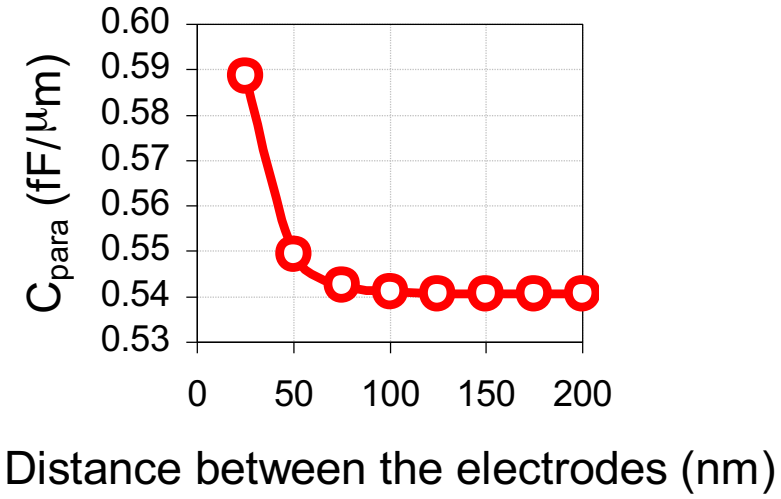

Fig. 24. C_{para} vs $L_{s,d}$ characteristics

C_{para} is the total parasitic capacitance observed when the distance between the electrodes is varied. This capacitance is subtracted from the total gate capacitance at 2 V to obtain $C_{channel}$.

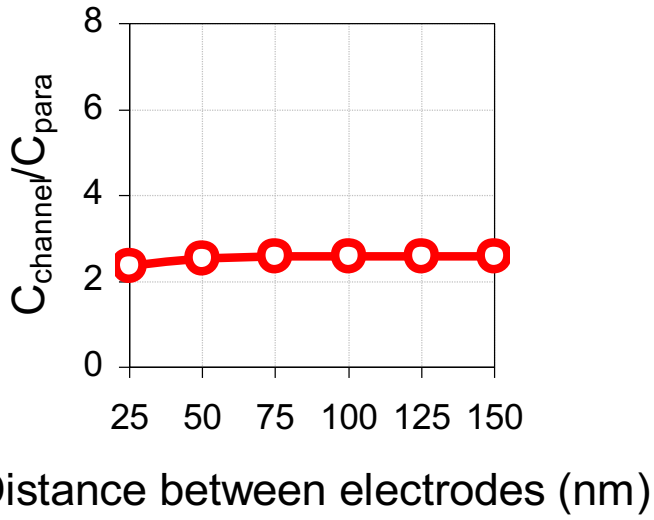

Fig. 25. Ratio of $C_{channel}/C_{para}$ vs Distance between electrodes characteristics

3.1.3 Varying Height of the electrodes

A graph depicting the ratio of gate and parasitic capacitance is plotted versus the height of source-drain electrodes in the device. Distance between the electrodes($L_{s,d}$) is kept constant at 100 nm and the height of the gate electrode(H_g) is fixed at 50 nm.

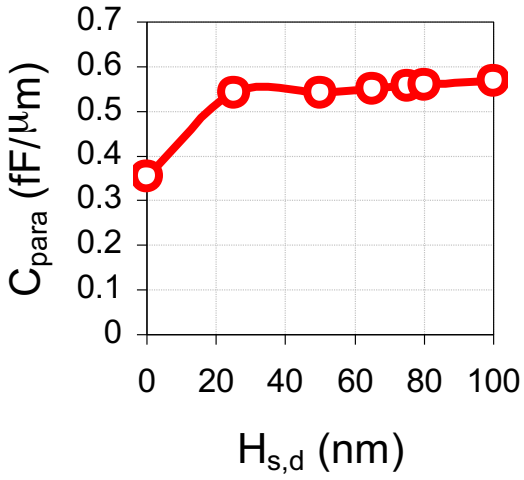

Fig. 26. C_{para} vs $H_{s,d}$ characteristics

C_{para} is the total parasitic capacitance observed when the height of the electrodes exceeds the height of the gate electrode. This capacitance is subtracted from the total gate capacitance at 2 V to obtain $C_{channel}$.

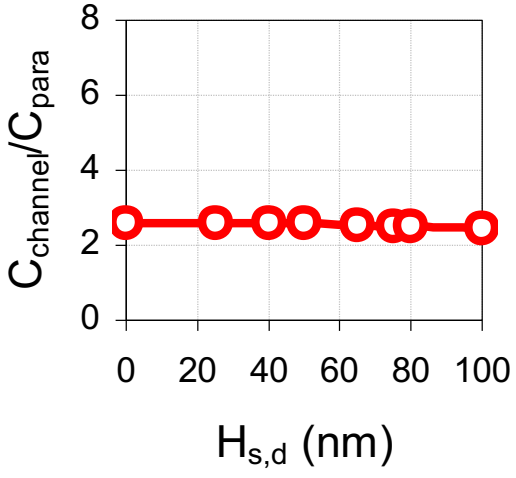

Fig. 27. Ratio of $C_{channel}/C_{para}$ vs Height of source-drain electrodes characteristics

3.2 CONCLUSION

- An underlap of 15 nm provides the highest ratio of channel to parasitic capacitance.
- As the height of gate electrode increases the parasitic capacitance increases and shows minimal change after 25 nm.
- Increasing distance between the electrodes leads to reduction in parasitic capacitance which becomes constant after 75 nm.
- Increasing height of source-drain electrodes beyond 50 nm decreases the ratio as it introduces an inter-electrode capacitance component.

Chapter 4

4.1 EFFECT OF PARASITIC CAPACITANCE ON ANALOG PERFORMANCE

Certain important analog parameters of MOSFET devices are its drain current (I_{ds}), gate capacitance (C_{gg}), transconductance (g_m) and transconductance generation factor (g_m/I_{ds}). In this section, all these parameters are discussed for various devices. Efforts have been made for device optimization to achieve favorable results. The optimization has been done with respect to parasitic capacitance (C_{para}).

Two devices have been simulated with the following dimensions:

PARAMETERS	OPTIMIZED DEVICE (nm)	NON-OPTIMIZED DEVICE (nm)
Overlap	-15	15
Gate Electrode Height(H_g)	50	50
Source-Drain Electrode Height($H_{s,d}$)	50	125
Distance between electrodes($L_{s,d}$)	75	25

Table 1. Device dimensions for the two cases

4.1.1 Drain Current(I_{ds})

MOSFET is a switching device driven by a channel at the semiconductor's surface due to the field effect produced by the voltage applied to the gate electrode, which is isolated from the semiconductor surface. When the device is biased in active region, $V_{gs}>V_{th}$ and $V_{ds}>0$, a channel is formed between the drain and source such that there is a current flow. This is known as drain current. In the non-optimized device, we observe that there is a very high OFF-state current as compared to our optimized device. No current should flow when no voltage is supplied at the

gate. Thus, there is lesser subthreshold current in our device as compared to the non-optimized device, which is good for power consumption.

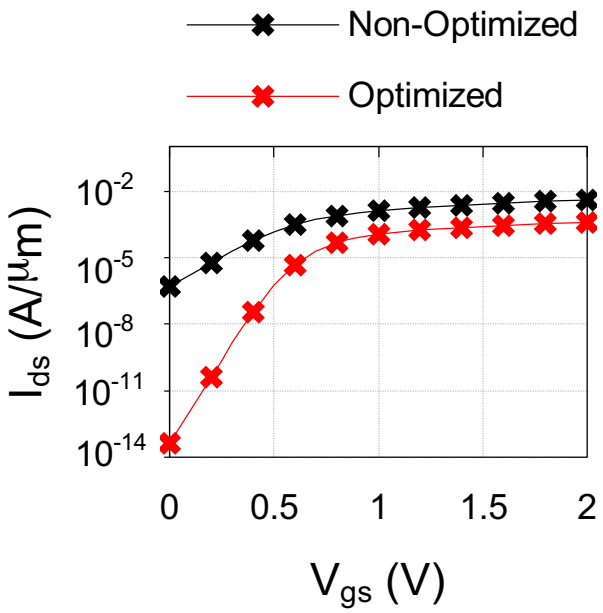

Fig. 28. I_{ds} vs V_{gs} characteristics (Logarithmic form)

4.1.3 Gate Capacitance (C_{gg})

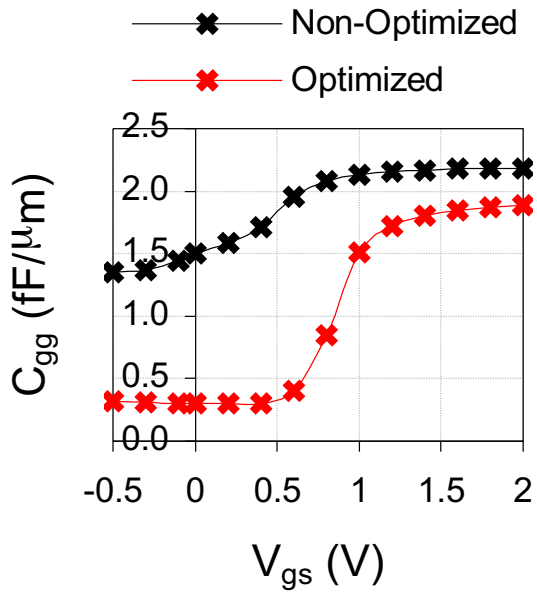

Fig. 29. C_{gg} vs V_{gs} characteristics

The gate capacitance (C_{gg}) shows the value of the channel capacitance when the threshold voltage is crossed. The intrinsic gate capacitance is considered as an important parameter in RF

analysis. Before this voltage ideally no capacitance should exist in the device. These unwanted capacitances are known as parasitic capacitances. Our aim is to reduce this parasitic capacitance. Our optimized device shows very less parasitic capacitance as compared to the non-optimized device. A lower parasitic capacitance is good for device performance and power stabilization. It can be verified from our simulations that that total gate capacitance reduces with increase in underlap length which is of great importance for RF applications [10].

4.1.2 Transconductance (g_m)

Transconductance (g_m) is the change in drain current with respect to gate voltage. If high transconductance can be achieved in a MOS transistor, which offers high linearity at the same time, simpler circuit design solutions and lower power consumption are achievable at the same performance specifications. [11] Higher transconductance gives more current and higher operating frequency. It is basically the property of a device to amplify a signal.

$$g_m = \frac{dyI_{ds}}{dxV_{gs}}$$

Fig. 30. shows that devices with higher underlap length has decreased g_m, owing to increase in effective channel resistance and decreased on current [12].

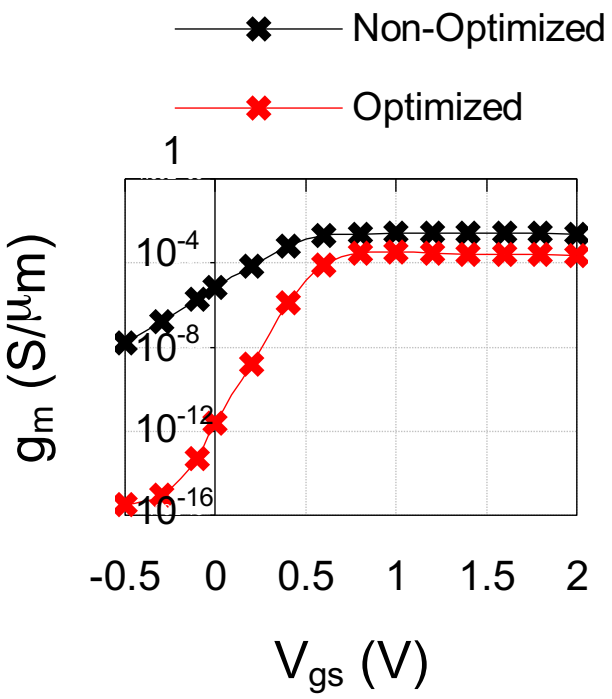

Fig. 30. g_m vs V_{gs} characteristics (Logarithmic form)

4.1.3 Transconductance Generation Factor(g_m/I_{ds})

Transconductance generation factor of a device determines the productive use of drain current to obtain an accepted value of transconductance. The transconductance generation factor is plotted against gate voltage (V_{gs}). The optimized device shows a higher value of Transconductance Generation Factor as compared to the non-optimized device. For a device, having higher transconductance generation factors is considered to be highly efficient. [13]

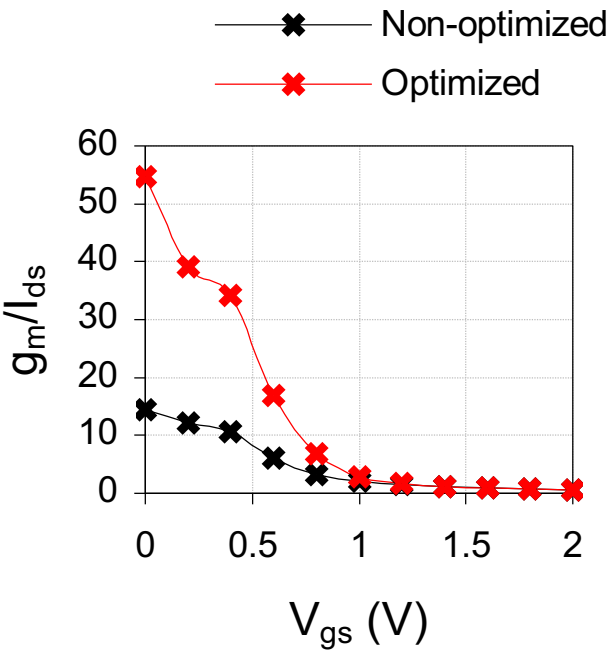

Fig. 31. g_m vs V_{gs} characteristics (Logarithmic form)

4.2 EFFECT OF PARASITIC CAPACITANCE ON RF PERFORMANCE

The advancement of technology has made wireless communication omnipresent and the constant downscaling of MOS transistors leads to excellent FOM. As a consequence, MOS transistors have entered the field of RF which was previously dominated by BJT technologies. It is well-known that accurate RF measurement on wafer is difficult due to parasitic components of system and device. Moreover, the effect of the surrounding parasitic components come to be bigger for device characteristics with continuous downscaling of the device dimensions. In evaluating RF

properties certain parameters such as cut-off frequency (f_T) are taken into consideration. In this section these values are appraised and necessary changes have been made to optimize the device to get higher FOM.

4.2.1 The cut-off frequency (f_T)

f_T is defined as the frequency where drain and gate current becomes equal. It is a measure of the intrinsic speed of the device. For high-speed digital applications (speed and high swing) f_T is the parameter of prime importance. [14]

$$f_T = \frac{g_m}{2\pi \times C_{gg}}$$

Thus, these MOSFETs have been established suitable for RF application nowadays as their cut-off frequency has reached a very high range which is verified by our simulations. f_T depends on the ratio of gm and total gate capacitances and from the equation, it is evident that the FOM is greatly influenced by geometrical parameters and parasitic capacitances have to be as low as possible to achieve a higher f_T.

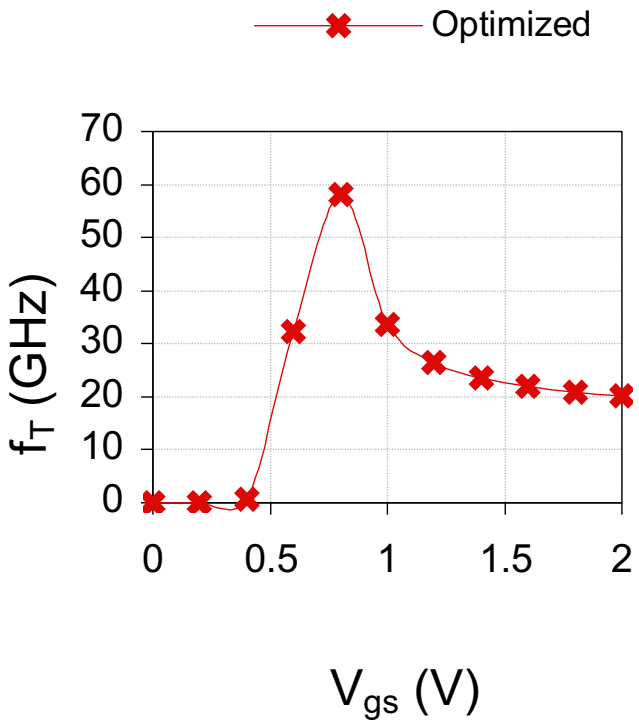

Fig. 32. f_T vs V_{gs} characteristics

In this work, we have achieved frequency in GHz range in optimized device as depicted in Fig. 32

4.3 CONCLUSION

- Although the non-optimized device has smaller dimensions it performs poorly in most of the cases.
- It is found that to suppress parasitic capacitances, the device having increased underlap length is desired.
- Our optimized device shows considerably lower subthreshold current as compared to the non-optimized device.
- The non-optimized device has almost three times the parasitic capacitance as opposed to the non-optimized device. A lower parasitic capacitance is desired as per our research.
- The device with underlap shows lower transconductance owing to increase in effective channel resistance and decreased on current.

Chapter 5

5.1 CONCLUSION

In spite of the several benefits of scaling, the major issue that remains in the MOS transistor, is its susceptibility to increase parasitic capacitance that affect the eventual circuit performance. In this study, a comprehensive analysis was done of the various parasitic capacitances present in the MOS transistors. Variegated capacitances namely inner fringe capacitance, outer fringe capacitance, inter-electrode capacitance 1 and inter-electrode capacitance 2 were extracted individually. The behaviors of these capacitances were analytically observed for varying MOS transistor models.

A simple MOS transistor was simulated and its C_{gg} vs V_{gs} characteristics were observed. Even though the threshold voltage had not been achieved (approx.0.4 V) there exists certain gate capacitance in the device. This capacitance is known as inner fringing capacitance. Our work shows that in the numerous cases observed, inner fringing is always the major contributor of parasitic capacitance. To reduce this value two viable options i.e., Overlap and Underlap were explored. The presence of overlap increases the parasitic capacitance and has greater OFF-state current. This is contrary to our purpose of study where we want to reduce the parasitic capacitance. Thus, overlap can be eliminated as a beneficial parameter.

Underlap leads to considerable decrease in the parasitic capacitance. Our results show that parasitic capacitance decreases with increasing underlap. The results follow the trend that by device and circuit modeling and simulation, the implied underlap design tradeoff for ultimate CMOS speed is affected significantly by parasitic G–S/D capacitance, i.e., fringe capacitance, in nanoscale devices .

The parasitic capacitance showed a decreasing trend when the distance between the electrodes on either side was increased. After performing the various simulations, it was concluded that the effect of parasitic capacitance was maximum at close proximity (≅25 nm) and showed no considerable change after a certain point (≅75 nm). For better results this distance was kept greater than 75 nm for our optimized device.

After our analysis, we use the typical gate thickness of (50 nm) because, though reducing thickness of gate electrode metals reduces outer fringing capacitance C_{of}, it, however, considerably increases the gate resistance.

This will significantly affect the performance as well as the power consumption in a circuit [15].

The parasitic capacitance showed an increasing trend when the height of the source-drain electrodes was increased. A thorough analysis was done where variations were started from 0 nm and increased to a value greater than the height of the gate electrode. To reduce the impact of electrode heights on parasitic capacitance it was kept at a minimum value as long as the technological processes allowed.

After successful extraction of the various elements of parasitic capacitances, its effect on analog and RF properties of MOS transistors is observed. Accurate extraction of parasitic capacitance is critical in RF circuit simulation and accurate modelling of intrinsic device. There are analog properties that are observed (i) drain current(I_{ds}) (ii) gate capacitance (C_{gg}) (ii) transconductance (g_m) and (iii) transconductance generation factor. For RF, f_T is an important FOM (figure of merit) that has been analyzed in our work.

The first analog property analyzed was drain current. By careful scaling of device dimensions, we achieved a lower subthreshold current in our optimized device as compared to the non-optimized device although the latter had smaller dimensions. The next property in study was gate capacitance. The optimized device shows considerably low parasitic capacitance as contrary to the non-optimized device. A lower parasitic capacitance is desired for better RF simulations and modelling of devices. This shows that the presence of underlap is imperative to both the subthreshold current and parasitic capacitances.

We next observed the transconductance in our device. The optimized device showed a lesser value of transconductance owing to the underlap introduced in the device. The presence of underlap led to increase in effective channel resistance and decreased ON current. Although a higher transconductance is desired the difference is minimal as compared to a device with overlap. A higher transconductance generation factor has been achieved in our optimized device implying that our device has a higher efficiency. Thus, to achieve a higher transconductance it is beneficial to use a device with overlap but a trade-off exists between higher transconductance and higher parasitic capacitance of which the latter is not desirable. To reduce parasitic capacitance a device with underlap has been used.

The next topic of study in our project is the analysis of RF property and its variations with respect to parasitic capacitances. The optimized device with an underlap of 15 nm provides a cut-off frequency in GHz range. Such high cut-off frequency makes it suitable for use in

wireless communication.

To summarize, parasitic capacitances greatly affect analog and RF properties of a MOS transistor. To reduce the effect of parasitic capacitance underlap is of vital importance. The dimensions of the device should not be reduced beyond or increased to a certain point as it has drastic impact on parasitic capacitance. Considerable optimization techniques have been adopted in our project work to provide the best case scenario for device simulations.

5.2 FUTURE WORK

The simulations done in this project work provide a solid ground for examination of other analog and RF properties. Further other parameters of a MOSFET device can be varied to find other ways of reduction of parasitic capacitance. Device scaling is also an important issue which should be studied to maintain a steady balance between scaling and reduced parasitic capacitance.

List of Figures

List of Tables

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