An Insightful Methodology for CMOS Logic and Analog Circuit Design with 500 mV Supply Voltage

M.Tech. Thesis

By
MADHUR SACHDEV

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

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MADHUR SACHDEV

DEPARTMENT OF ELECTRICAL ENGINEERING
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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **An Insightful Methodology for CMOS Logic and Analog Circuit Design with 500 mV Supply Voltage** in the partial fulfillment of the requirements for the award of the degree of **MASTER OF TECHNOLOGY** and submitted in the **DEPARTMENT OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from July 2023 to May 2024. Thesis submission under the supervision of Prof. Abhinav Kranti, IIT Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

24/05/2024

Signature of the student with date
(MADHUR SACHDEV)

This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

May 24, 2024

Signature of the Supervisor of
M.Tech. thesis (with date)
(Prof. Abhinav Kranti)

MADHUR SACHDEV has successfully given his M.Tech. Oral Examination held on **May 7, 2024.**

Signature of Supervisor of M.Tech. thesis
Date: 24/05/2024

Convener, DPGC
Date:

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Dedicated to my family

Abstract

An Insightful methodology for CMOS Logic and Analog Circuit Design with 500 mV Supply Voltage

Over the past few decades, there has been significant progress in developing ultra-low power (ULP) devices, circuits, and systems. The scientific community has focused on developing technologies that consume less energy, which is essential for extending battery life, fast tracking the development of portable and wearable devices, and Internet of Things (IoT) deployments. The development of ULP circuits is driven by the need for energy-efficient electronics that can support sustainable technology. Understanding the basics of power consumption in integrated circuits is central to this effort. However, designing ULP circuits presents challenges such as minimizing energy use without sacrificing performance. Simulation and modeling tools are crucial in overcoming these challenges, allowing for the testing and optimization of ULP circuits.

In this thesis, the designing of ULP subthreshold logic blocks such as inverter, and two-input NAND and NOR gates has been carried out by utilizing double gate (DG) MOSFET. The operation is limited to supply (V_{DD}) of 0.5 V, which is lower than the threshold voltage (V_{TH}) of the transistor. Performance evaluation of ULP logic blocks has been carried out through the evaluation of relevant figures of merit (FoM) and delay. These efforts aim to optimize energy efficiency of DG MOSFET and circuits, all of which is essential for improving sustainability of modern electronics.

The work also dwells on analog design at 0.5 V through the implementation of simple and cascode current mirrors. A common source (CS) amplifier, a differential amplifier with a resistive load (single and double stage), and a differential amplifier with a current mirror load were also designed at a supply voltage of 0.5 V. The differential amplifier with

the current mirror load showed the best performance, operating at a relatively higher frequency and effectively driving the load with an unbalanced output. The work also demonstrates the advantages of using current mirror load in differential amplifiers for improved performance. These findings are valuable for minimizing trade-off between speed and power in analog circuits.

A non-linear voltage transfer characteristics curve with three distinct slopes was implemented using CMOS technology at 0.5 V. Through a closed loop feedback, this circuit can function as a random number generator, and finds utility in secure communication. The findings of this work contribute towards developing energy-efficient ULP solutions for logic and analog applications in the existing and mature CMOS technology.

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NOMENCLATURE

L	*Gate length*	*nm*
W	*Width*	*nm*
T_{OX}	*Oxide thickness*	*nm*
T_{SI}	*Silicon thickness*	*nm*
V_G	*Gate voltage*	*V*
V_D	*Drain voltage*	*V*
V_S	*Source voltage*	*V*
V_{DD}	*Supply voltage*	*V*
I_{ON}	*On current*	*mA*
I_{OFF}	*Off current*	*nA*
I_{ON} / I_{OFF}	*On-current to off-current ratio*	*Unitless*
I_{DS}	*Drain current*	*A*
P_{avg}	*Average power*	*watt*
I_{avg}	*Average current*	*A*
V_{DS}	*Drain to source voltage*	*V*
V_{GS}	*Gate to source voltage*	*V*
S_{SWING}	*Subthreshold swing*	*mV/decade*
V_T	*Thermal voltage*	*V*
V_{TH}	*Threshold voltage*	*V*
V_{IN}	*Input voltage*	*V*
V_O	*Output voltage*	*V*
V_{OH}	*Output high voltage*	*V*
V_{OL}	*Output low voltage*	*V*
V_{LT}	*Logic threshold voltage*	*V*
A_V	*Voltage gain @ V_{LT}*	*Unitless*
η	*Technology parameter of MOSFET*	*Unitless*

T_{PLH}	*Delay when output transits from low to high*	*S*
T_{PHL}	*Delay when output transits from high to low*	*S*
V_C	*Controlling voltage*	*V*
CMRR	*Common mode rejection ratio*	*Unitless*
β_N (β_P)	*Strength of transistors*	*V*

ACRONYMS

IC	*Integrated circuit*
MOSFET	*Metal oxide semiconductor field effect transistor*
DG-MOSFET	*Double gate metal oxide semiconductor field effect transistor*
MOS	*Metal oxide semiconductor*
CMOS	*Complementary MOS*
nMOS	*n-type MOS*
pMOS	*p-type MOS*
DG-NMOS	*Double gate n-type MOS*
DG-PMOS	*Double gate p-type MOS*
SCE	*Short channel effect*
DIBL	*Drain induced barrier lowering*
SiO_2	*Silicon dioxide*
SIO	*Silicon on insulator*
FDSOI	*Fully depleted SOI*
FET	*Field effect transistor*
ULP	*Ultra-low power*
VTC	*Voltage transfer characteristics*
Si	*Silicon*
TCAD	*Technology Computer Aided Design*
VLSI	*Very Large-Scale Integration*
RCE	*Ratio change error*
CS	*Common source*
LNA	*Low noise amplifier*

RFA	*Radio frequency amplifier*
GND	*Ground*

Chapter 1

Introduction

1.1 Introduction to Ultra-Low Power Circuit Design

The considerable usage of portable electronic gadgets in daily life necessitates the development of technologies which consume minimum power. In this aspect, ultra-low power (ULP) technology can play a crucial role. ULP technology helps to extend the battery life of our gadgets while also contributing to the development of environmentally friendly electronic systems [1]. This study sets out to explore the fascinating field of ULP circuit design, aiming to understand its basic principles, methods, and impact on the future of electronics. This chapter explores approaches to reduce energy consumption while maintaining the desired functionality of devices. In this chapter, techniques like adjusting voltage and frequency are discussed, using device and circuit designs. ULP circuit design provides a comprehensive way to tackle the energy efficiency challenges in modern electronics [1].

Despite the advantages, there are significant challenges in ULP operation. When circuits function at ULP levels, they become more sensitive to disturbances like noise and variation. Also, ULP operation often means making careful choices between circuit size, speed, and efficiency [2]. Yet, it is these challenges that spur innovation, leading to new device and circuit designs along with strategies for improvement in the performance of systems and products. ULP technology impacts many sectors such as healthcare, environmental monitoring, smart cities, and self-driving systems. ULP technology is crucial in the development of medical devices that can be placed inside our body. ULP circuit design is of paramount importance for Internet of Things (IoT) deployments [3]. ULP technology is truly changing the future of product development. The

continuous shrinking of CMOS technology has driven the creation of powerful minituarized systems [4]. However, not all applications or systems need high speeds. For devices like wireless gadgets and medical tools, saving power is more important [5]. In these cases, using lower voltages can be better, which can give a good balance between power and speed [6]. Step into the domain of low-voltage circuit design, where the extreme is exemplified by subthreshold circuits. These circuits operate with supply voltages (V_{DD}) lower than the threshold voltage (V_{TH}) of transistors [7]. While this approach capitalizes on subthreshold current as the operating current, it comes with inherent limitations in performance. As a result, subthreshold circuitry finds its niche in ULP applications, where extremely low operating frequencies – often in the range of hundreds of kilohertz are sufficient [8].

1.2 Motivation and Importance of ULP Circuits

In today's rapidly evolving technological landscape, the motivation behind ULP circuit design is as compelling as it is multifaceted. At the forefront of this drive is the escalating demand for portable electronics, Internet of Things (IoT) devices, and wearables [3]. These gadgets have become integral parts of our daily lives, seamlessly integrating into our routines. However, with this ubiquity comes a pressing need for energy efficiency. Today's smartphones are packed with hi-tech features, but they are only as good as their battery life [9]. The problem with battery operated devices is always a scramble to charge devices or find outlets, disrupting the smooth experience desired. The problem is that as technology improves, there is a desire for gadgets to do more without their batteries dying quickly. There are lots of other gadgets now, like smart thermostats and connected toothbrushes, all hooked up to the internet [9]. They make life easier, but they also use up a lot of power. Many of these gadgets run on batteries or need to be powered in an eco-friendly way. Hence, these gadgets must be

designed to use as little power as possible to last longer without needing maintenance [10].

Beyond consumer electronics, ULP circuit design holds immense promise in critical areas such as healthcare and environmental monitoring. Imagine implantable medical devices that can continuously monitor vital signs without the need for frequent battery replacements [11] or sensor networks deployed in remote locations, powered by renewable energy sources, and operating autonomously [12]. ULP circuit design goes beyond technical expertise. It is about sustainability and efficiency. When power usage is cut down, not only the device life is extended but the environmental impact of products is suppressed. This approach fuels innovations that improve quality, drive scientific progress, and narrow the digital gap. ULP circuit is a force for good in the ever-connected world.

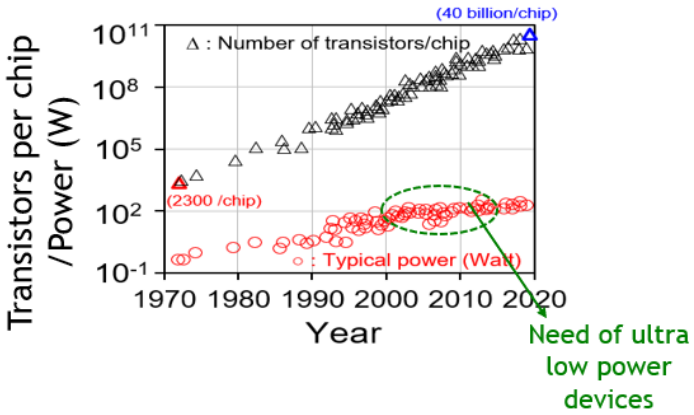

Fig. 1.1 Variation of ratio of number of transistors per and power consumed over last fifty years (1970 to 2020) [12]. Available online at https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/.

In Fig. 1.1, the observation of the ratio of transistor number per chip to power consumption over last fifty years is shown [12]. Notably, there is a consistent rise in transistor count alongside a corresponding increase in power usage. Consequently, there arises a pressing need for ULP circuitry to address the escalating power dissipation and consumption. By implementing such circuits, we can mitigate these challenges effectively.

Reducing the power supply can substantially alleviate both dissipation and consumption, thus highlighting the importance of adopting ULP solutions in modern electronics.

1.3 Power Consumption in Integrated Circuits

At the core of ULP circuit design lies a delicate balancing act between minimizing energy consumption and maintaining acceptable performance levels. This intricate problem is governed by several fundamental principles that underpin the design process [6]. First and foremost, it is important to realize that the usual ways of designing circuits, which focus on speed and performance, might not work well for situations where saving power is the main goal [6]. Instead, designers need to think about saving energy while still making sure things work properly.

One key technique in ULP circuit design is voltage scaling. This means lowering the voltage supplied to circuits, which can significantly cut down on power use. However, lowering the voltage brings its own challenges, like making circuits more sensitive to noise and reducing how well they work in different situations. Hence, designers need to be careful to make sure the circuits still work reliably [13],[14]. Frequency scaling is another important technique. It involves changing how fast circuits work based on how much computing they need to do [8]. This way, circuits can run slower when they are not doing much, which saves even more power without making them slower overall. Another important aspect of ULP design is using circuit architectures and layouts that save energy [15]. These designs are made to use as little power as possible while still working well. For instance, asynchronous circuits do not need a main clock signal, which can save a lot of power. Adiabatic logic is another example, where energy is reused when circuits switch on and off [13], [10].

Moreover, using specific design methods is crucial for obtaining the best power efficiency. Methods like design abstraction and hierarchical

design help designers explore different design options efficiently, making it easier to find energy-saving solutions. Also, advanced simulation and modeling tools help designers predict and improve power use at different points during the design process.

Overall, the fundamentals of ULP circuit design revolve around the careful balance of voltage and frequency, the adoption of energy-efficient architectures, and the utilization of specialized design methodologies [13]. By embracing these principles, designers can unlock new levels of power efficiency, enabling the development of innovative electronic systems that consume minimal energy while delivering maximum performance.

1.4 Existing ULP Circuit Techniques and Technologies

Looking closely at the current techniques and technologies for ULP circuits, a wide range of strategies are found. These are all aimed at making electronics use power as efficiently as possible while manifesting an acceptable level of performance. This investigation looks at different methods and new ideas that have come up to meet the demand for electronics that use less energy.

A notable method in ULP circuits is voltage scaling. The voltage supplied to circuits is lowered well below normal levels, cutting down on power use [14]. This works best when performance needs can be adjusted, letting designers balance power efficiency and computing speed carefully [13], [16]. Complementing voltage scaling is frequency scaling, which involves dynamically adjusting the operating frequency of circuits based on workload demands. By scaling down the frequency during periods of low activity, circuits can conserve energy without sacrificing responsiveness. Frequency scaling is often employed in conjunction with voltage scaling to achieve synergistic power savings while maintaining acceptable levels of performance [15]. Additionally, energy-efficient circuit architectures play a crucial role in ULP circuit design. These architectures are specifically

engineered to minimize power dissipation while meeting functional requirements [13], [16].

In the realm of ULP design, MOSFETs play a pivotal role, necessitating specific qualities to ensure optimal performance and minimal energy consumption [17]. Additionally, MOSFETs with ideal subthreshold slope is critical for facilitating efficient operation in low-voltage regimes and enabling better control over current [2]. This is crucial for minimizing power loss during standby or idle states. High carrier mobility is another key attribute sought after, as it enables faster charge carrier transport, leading to faster switching and reduced power dissipation [7]. Moreover, reducing parasitic capacitance in MOSFET structures is imperative to diminish switching losses, particularly in high-frequency applications [17]. Advanced process technologies, such as FinFET or nanowire MOSFETs offer further enhancements by providing better control over device dimensions and characteristics, thus contributing to improved performance and reduced power consumption [18]. Stability over a wide temperature range is also desirable to ensure reliable operation in varying environmental conditions. Furthermore, MOSFETs with a high on-to-off current ratio (I_{ON}/I_{OFF}) exhibit efficient switching behavior with minimal current in the off state, contributing to overall energy efficiency [13]. Finally, minimizing leakage current is paramount to reducing static power consumption and enhancing energy efficiency across diverse applications, ranging from portable electronics to IoT devices and energy-efficient systems [18].

In short, the review of existing ULP circuit techniques and technologies reveal diverse approaches aimed at maximizing power efficiency in electronic systems. By leveraging voltage scaling, frequency scaling, energy-efficient architectures, and advanced design methodologies, designers can unlock new levels of energy efficiency, paving the way for sustainable and environmentally friendly electronic devices.

1.5 Challenges in ULP Circuit Design

Designing ULP circuits offer significant energy savings and longer battery life, but it comes with many challenges. Designers must find the right balance between power use, and address critical questions such as – how well the circuit works, and how reliable it is. Additionally, ULP circuits have their own specific issues related to acceptable performance levels for the desired applications under diverse conditions [19].

One of the primary challenges in ULP circuit design is the trade-off between power consumption and performance [2]. Operating circuits at ultra-low voltages and frequencies inherently limit their speed and computational throughput. As a result, designers must carefully balance these factors to ensure that power consumption is minimized without sacrificing functionality [6]. This delicate balancing act requires sophisticated optimization and thorough characterization of circuit behavior under varying operating conditions [11]. Moreover, the reliance on subthreshold operation in ULP circuits introduces additional challenges related to variability and reliability. Subthreshold operation, where transistors operate below V_{TH} can be sensitive to process variations and operating conditions. This sensitivity can lead to fluctuations in circuit performance and reliability, necessitating robust design techniques to mitigate these effects [20].

Another significant challenge in ULP circuit design is the management of the off-current. As V_{DD} is reduced to minimize power consumption, off-current become a more significant proportion of total power dissipation [1], [15], [21]. Off-current, which flows when transistors are not actively switching, can contribute significantly to overall power consumption in ULP circuits. Managing off-current effectively requires careful transistor sizing, layout optimization, and power gating techniques to minimize power dissipation while maintaining reliability.

Achieving ULP consumption often requires trade-offs in terms of circuit area and complexity [2]. Energy-efficient circuit architectures and design techniques may necessitate increased circuit area or more complex design methodologies, which can impact manufacturing costs and design complexity. Balancing these trade-offs requires careful consideration of design constraints and performance requirements to ensure that the resulting circuits are both energy-efficient and practical to implement.

ULP circuit design must address the growing demand for functionality and connectivity in modern electronic devices [22]. As IoT devices and wearables become increasingly pervasive, designers face the challenge of integrating energy-efficient wireless communication and sensor technologies into ULP circuits [22]. This integration requires careful power management and optimization strategies to minimize energy consumption while enabling seamless connectivity and data transmission.

The challenges in ULP circuit design stem from the complex interplay of power consumption, performance, reliability, and functionality. Addressing these challenges requires a careful approach that combines advanced design techniques, robust optimization methodologies, and thorough characterization of circuit behavior. By overcoming these challenges, designers can unlock the full potential of ULP circuit design, enabling the development of energy-efficient electronic systems for a wide range of applications.

1.6 Simulation and Modeling of ULP Circuits

Simulation and modeling play a pivotal role in the development and optimization of ULP circuits, providing designers with invaluable insights into circuit behavior in terms of performance and power consumption alongside troubleshooting. This section explores the importance of simulation and modeling in ULP circuit design and highlights key methodologies and techniques used in ULP domain. Simulation and

modeling enable designers to explore the behavior of ULP circuits under various operating conditions, helping to predict performance metrics such as power consumption, timing, and signal integrity [23]. By simulating circuit operation using specialized software tools, designers can analyze the effects of different design parameters, optimization strategies, and environmental factors on circuit behavior [24].

One of the primary uses of simulation and modeling in ULP circuit design is in the evaluation of different circuit architectures and design choices [17]. Designers can use simulation tools to compare the performance and power consumption of various circuit topologies, helping to identify the most energy-efficient solutions. This allows designers to iterate rapidly through design iterations, optimizing circuit performance while minimizing power consumption.

Furthermore, simulation and modeling is essential for characterizing the effects of process variations and environmental conditions on circuit behavior. ULP circuits are often highly sensitive to process variations, which can lead to fluctuations in performance and power consumption [25]. By incorporating statistical analysis techniques into simulation models, designers can assess the impact of process variations on circuit yield and reliability, enabling robust design optimization. In addition to device and circuit-level simulation, system-level modeling is also critical in ULP circuit design. System-level models capture the interactions between different components of a larger electronic system, allowing designers to evaluate the overall system performance and power consumption. This holistic approach enables designers to optimize system-level parameters such as communication protocols, sensor placement, and power management strategies to maximize energy efficiency [23].

Simulation and modeling facilitate the exploration of advanced power management techniques and optimization strategies in ULP circuits. By simulating dynamic power management schemes such as power gating,

clock gating, and voltage scaling, designers can assess their effectiveness in reducing power consumption while maintaining performance requirements [14]. This allows designers to make informed decisions about the most appropriate power management techniques for a given application.

Simulation and modeling is pivotal in the development of ULP MOSFETs, guiding engineers through the intricate process of optimizing these devices for maximum efficiency. Initially, engineers meticulously characterize the MOSFET's electrical properties, establishing a foundation for subsequent simulation work. Leveraging sophisticated Technology Computer Aided Design (TCAD) tools, engineers then delve into detailed simulations, examining the behavior of MOSFET across the desired operating conditions. Through these simulations, engineers can analyze everything from current-voltage characteristics to dynamic behavior, crucial for understanding the performance under various scenarios.

Armed with these models, engineers embark on optimization endeavors, fine-tuning MOSFET design to enhance performance and minimize power consumption. This iterative process involves adjusting device dimensions, material properties, and operating conditions to meet specific design goals. Verification and validation are then conducted to ensure that the simulated results align with empirical data, validating the model's accuracy and reliability [13].

Overall, simulation and modeling is an indispensable tool in the design and optimization of ULP circuits. By enabling designers to explore circuit behavior, evaluate design choices, and optimize power consumption, simulation and modeling play a crucial role in realizing energy-efficient electronic systems for a wide range of applications.

1.7 Conclusion

In conclusion, looking closely at ULP circuit design indicates many challenges and probable solutions. The importance of saving energy when

designing electronic devices is of paramount importance. Learning about the different ways designers can accomplish the same while still making sure devices work well is the hallmark of an efficient ULP design. Throughout this chapter, several key points have emerged.

The most important aspect to understand is that ULP circuit design is a key area in making electronics more energy efficient. By using techniques like adjusting voltage and frequency, as well as designing energy-efficient circuits, designers can make electronic systems that use very little energy but still work well. This opens possibilities for creating new and innovative electronics that performs great without draining power.

The exploration of challenges in ULP circuit design has shed light on the complexities inherent in balancing power consumption, performance, and reliability. From managing leakage currents to addressing process variations and environmental conditions, designers must deal with lots of challenges to realize ULP circuits as energy efficient as possible.

The discussion on simulation and modeling has underscored the indispensable role of these tools in the design and optimization of ULP circuits. By enabling designers to explore circuit behavior, evaluate design choices, and optimize power consumption, simulation and modeling play a crucial role in realizing energy-efficient electronic systems for a wide range of applications.

1.8 Organization of The Thesis

This study starts with chapter 1 which discusses motivation, applications, and challenges of ULP circuit design. Further, the relevant equations for the subthreshold region and data extraction process for a double gate (DG) metal oxide semiconductor field effect transistor (MOSFET) is presented in chapter 2. The design and operation of complementary metal oxide semiconductor (CMOS) inverter, and universal logic gates are also discussed. Chapter 3 presents ac as well as DC analysis

of simple and cascode current mirrors. Analysis of gain of different analog circuits such as single stage common source amplifier, resistive load differential amplifier, double stage resistive load differential amplifier, and current mirror load single stage differential amplifier are reported in chapter 4. Finally, the findings of this work are summarized in chapter 5 with suggestions on the further scope of the work.

Chapter 2

CMOS Logic Design

2.1 Double Gate (DG) MOSFET

It is widely acknowledged that the demand for nanoscale transistors is driven by the necessity to develop low-power circuits with increased packing density [26], [27]. However, a significant challenge arises at shorter gate lengths due to the emergence of short channel effects (SCEs) [28]. These effects, compounded by the requirement of low supply voltages (such as V_{DD} = 500 mV or lower), have the potential to exacerbate issues related to subthreshold swing, I_{ON}/I_{OFF}, and transition from logic HIGH to logic LOW in digital circuits.

To address this issue, a multi-gate transistor, specifically a DG-MOSFET, is employed in this work for the design of logic and analog circuits [29]. By adopting the DG concept, significant improvements can be achieved in mitigating SCEs at reduced channel lengths [29] as compared to conventional planar CMOS technology as shown in Fig. 2.1 [30]. The utilization of dual gates effectively enhances the coupling between the gate and channel, thereby facilitating the suppression of SCEs [29]. Furthermore, DG-MOSFET, shown in Fig. 2.2, allow for the use of very lightly doped or even undoped channels. This characteristic enhances carrier mobility in smaller dimensions, leading to improved intrinsic switching times [31]. Moreover, DG-MOSFET exhibit reduced off-current, contributing to overall enhanced performance and efficiency in circuit design [32].

DG-MOSFETs boast twice the current driving capability of planar CMOS transistors, enabling operation at substantially lower input and threshold voltages [30]. Consequently, this translates to reduced power consumption. The proximity of the channel to both gates in DG-MOSFETs enables precise control of the electric field by the voltage applied to the gate

terminals. This control mechanism dictates the magnitude of current flowing through the channel. Such a characteristic results in an optimal inverse subthreshold slope, thus facilitating an efficient subthreshold operation and allowing DG-MOSFETs to function effectively at significantly diminished voltages.

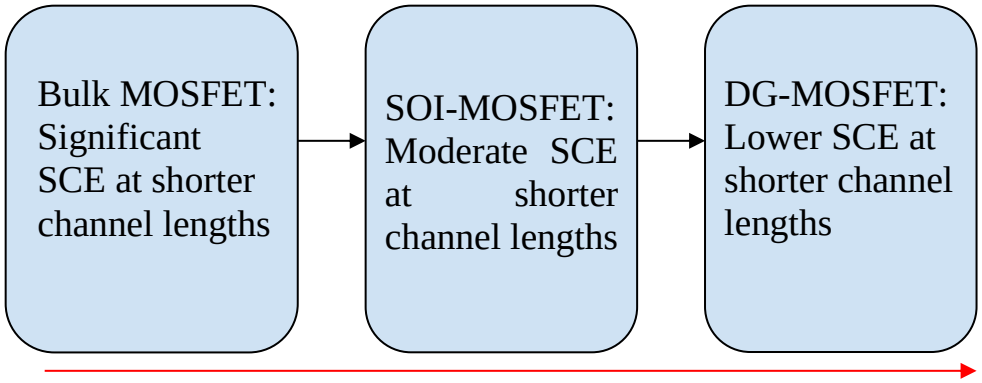

Fig. 2.1 Reduction in SCEs due to innovation in transistor architecture.

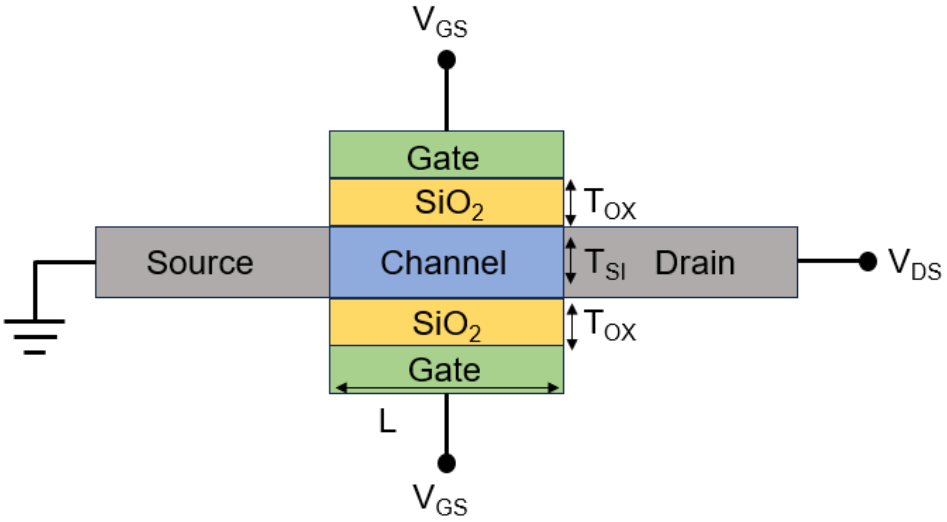

Fig. 2.2 Schematic diagram of a DG-MOSFET.

Table 2.1 Dimensions of DG-MOSFET used in this work.

W (nm)	L (nm)	T_{OX} (nm)	T_{SI} (nm)
1000	50	1	8

Table 2.1 shows the dimensions of DG-MOSFET used in this work, W is width, L is the gate length, T_{OX} is oxide thickness of SiO_2 layer, and T_{SI} is the silicon thickness of the transistor.

This thesis focuses on subthreshold operation, where the control of the subthreshold current is a key consideration [33]. Unlike the super threshold current, which predominates in operations above threshold, the subthreshold current is of primary interest for ULP applications. The ensuing section will delve into the subthreshold drain current, as well as leakage currents of a MOSFET. Advances in MOS transistor technology has made achieving subthreshold operation feasible [34]. In this mode, the primary current source is the flow from the source to the drain, which exponentially depends on the gate-to-source voltage (V_{GS}). Particularly noteworthy is that at low supply voltages, the current (I_{DS}) [35] can be expressed as

$$I_{DS} = \beta e^{(V_{GS}/\eta V_T)} . e^{(\delta V_{DS}/\eta V_T)} . \left(1 - e^{(-V_{DS}/V_T)}\right) \tag{2.1}$$

$$\beta = I_0 \frac{W}{L} e^{(-V_{THO}/\eta V_T)} \tag{2.2}$$

where, β is the strength of the current, δV_{DS} is Drain Induced Barrier Lowering (DIBL) parameter, η is technology parameter which is related with subthreshold swing [35]. V_{GS} is the gate to source voltage and V_{DS} is drain to source voltage. Also, I_O in equation (2.2) is technology parameter of current (I_{DS}), V_{THO} is threshold voltage at a small V_{DS} (= 10 mV), V_T

denotes the thermal voltage, while W/L represents the aspect ratio (width-to-length ratio) of transistor.

2.1.1 Junction Leakage Current

Between the source/drain diffusion regions and substrate, p-n junctions are formed in a bulk MOSFET [36]. Additionally, another diode is formed between well and substrate. To establish a reverse-bias condition, the wells and substrate are biased to either V_{DD} or ground [37]. Nevertheless, even under reverse-bias conditions, these diodes still permit a small amount of current to flow, which is referred to as junction leakage [38]. Modern CMOS technology integrates low-power transistor variants to mitigate this leakage, aiming to minimize power consumption and enhance overall efficiency [36].

2.1.2 Gate Leakage Current

Through a phenomenon referred to as gate tunneling, the charge carriers can traverse through the gate oxide [36]. Thinner oxides substantially elevate the probability of tunneling. Like junction leakage, specialized low-power transistor variants are engineered with the purpose of minimizing gate leakage current [38]. This strategy is essential for optimizing power efficiency and ensuring reliable performance in state-of-the-art semiconductor technology.

2.1.3 Subthreshold Swing

The subthreshold swing is defined as the gate voltage which can alter the subthreshold drain current by a factor of ten when device is operated below threshold [35]. The subthreshold swing (S_{SWING}) can be computed by using equation (2.3) as

$$S_{SWING} = \frac{\Delta V_{GS}}{\Delta \log_{10}(I_{DS})} \text{ mV/decade} \quad (2.3)$$

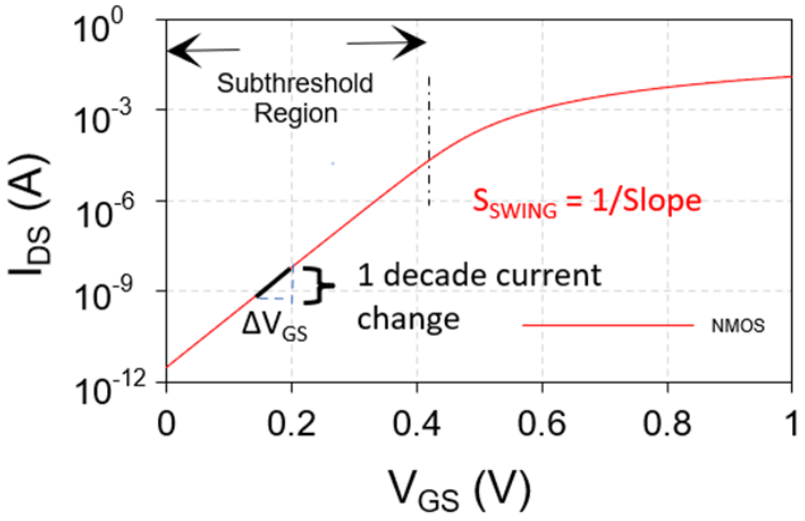

Fig. 2.3 Evaluation of subthreshold swing for DG-MOSFET by using the semi-logarithmic curve of $I_{DS} - V_{GS}$ graph.

The minimum value of S_{SWING} for conventional MOSFET is 60 mV/decade at room temperature (300 K).

2.1.4 I_{ON} and I_{OFF} Current

Two important parameters for transistor are on-current (I_{ON}) and off-current (I_{OFF}). I_{OFF} is a drain to source current when gate to source voltage at 0 Volt and drain to source voltage at V_{DD}. I_{ON} is a drain to source current when gate to source voltage and drain to source voltage at V_{DD}. Mathematically, the same can be expressed as

$$I_{OFF} = I_{DS} @ (V_{GS} = 0 \text{ V and } V_{DS} = V_{DD}) \quad (2.4)$$

$$I_{ON} = I_{DS} @ (V_{GS} = V_{DS} = V_{DD}) \quad (2.5)$$

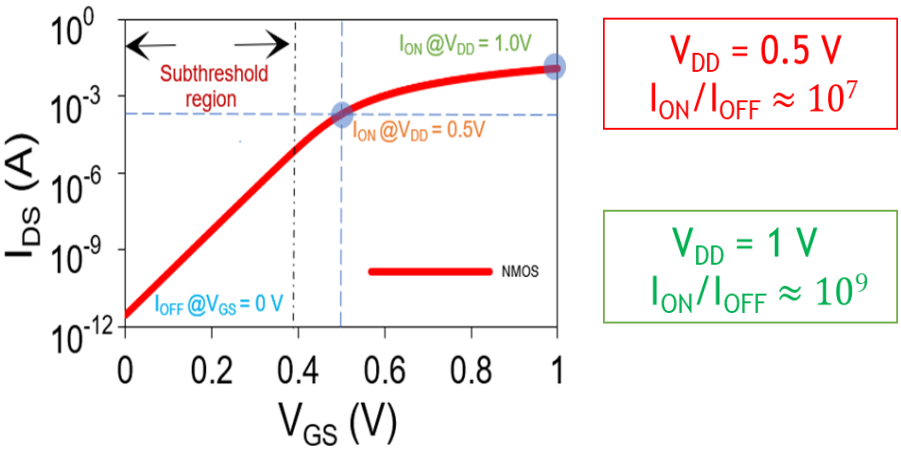

Fig. 2.4 Representation of I_{ON}/I_{OFF} ratio of DG-MOSFET at different V_{DD} values through I_{DS}-V_{GS} semi-logarithmic curve.

2.1.5 Extraction Process

After modelling/simulating DG-MOSFET, the followed process for the extraction of key device parameters such as V_{TH}, δ_{DS}, I_{OFF}, and S_{SWING} including the technology dependent parameters (I_O, and η) is shown in Fig. 2.5.

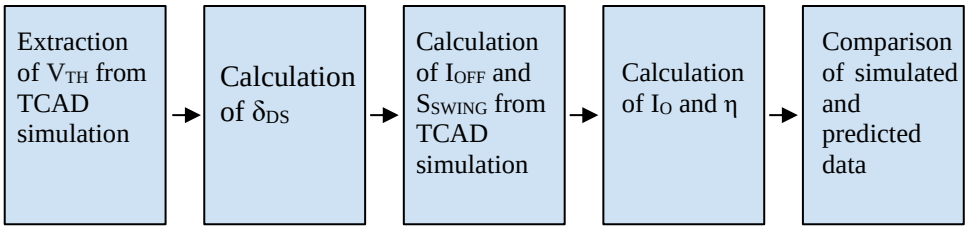

Fig. 2.5 Process for extraction of key parameters of DG-MOSFET from I_{DS} – V_{GS} characteristics.

2.1.5.1 V_{TH} Extraction

V_{TH} can be extracted by many methods such as constant current, transconductance-to-current (g_m/I_{DS}) ratio, linear extrapolation method [39]. In this work, constant current method has been used to extract (V_{TH}), as the gate voltage corresponding to a defined threshold current (I_{TH}).

Calculation of δ_{DS} is required to check the variation of V_{TH} with respect to V_{DS}. The extraction was carried out using equation (2.8) given below. The obtained variation of V_{TH} (absolute value) is plotted in Fig. 2.6 for both simulated and modelled data for nMOS and pMOS transistors.

$$I_{TH} = \left(\frac{W}{L}\right) 100 \text{ nA} \tag{2.6}$$

$$V_{TH} = V_{GS} @ I_{DS} = I_{TH} \tag{2.7}$$

$$V_{TH} = V_{THO} - \delta_{DS} V_{DS} \tag{2.8}$$

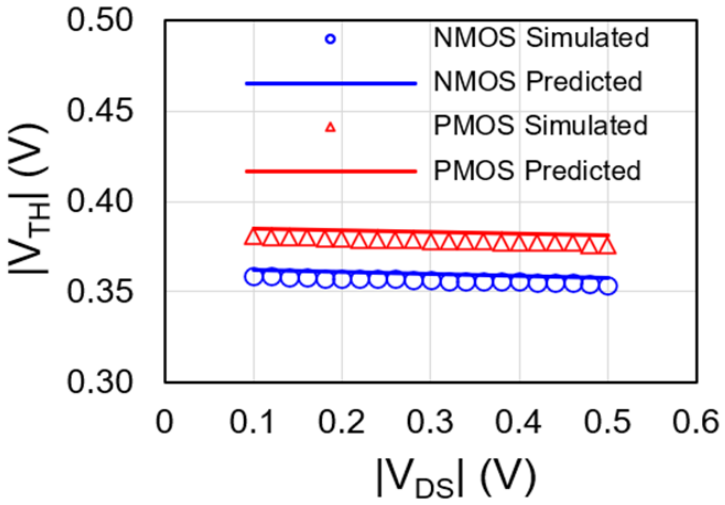

Fig. 2.6 The slope of V_{TH} versus V_{DS} curve for DG-MOSFET provides an indication of DIBL.

The technology parameter, η, characterizes the degradation in S_{SWING} as the gate length of MOSFET decreases. SCEs become more prominent as the gate length shrinks, leading to increased leakage and degraded performance. The logarithm of equation (2.1) can be used to calculate η. The obtained equation is given as

$$\log_e(I_{DS}) = \log_e(\beta) + \frac{V_{GS}}{\eta V_T} + \frac{\delta_{DS} V_{DS}}{\eta V_T} + \log_e\left(1 - e^{\left(\frac{-V_{DS}}{V_T}\right)}\right) \tag{2.9}$$

The graph between $(\log_e(I_{DS}))$ and $\left(\frac{V_{GS}}{\eta V_T}\right)$ gives the value of η through its slope. I_O can be calculated with the help of equation (2.1) by substituting the values of all extracted parameters $(\eta, V_{THO}, \delta_{DS})$. The values of parameters extracted for DG-nMOS and DG-pMOS devices are shown in table 2.2.

Table 2.2 Extracted parameters of n and p type DG-MOSFET.

Type of DG-MOSFET	η	I_0 (A)	V_{THO} (at V_{DS} = 10 mV) (V)	δ_{DS}
nMOS	1.03	2.1 x 10^{-07}	0.393	0.009
pMOS	1.03	2.2 x 10^{-07}	-0.416	0.01

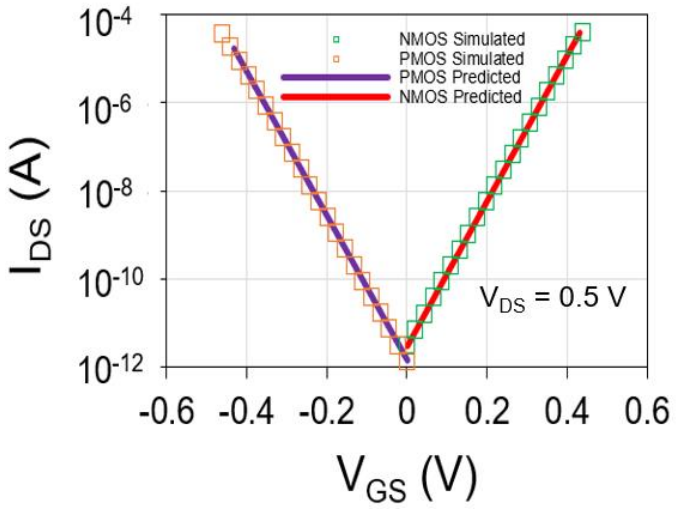

Fig. 2.7 Comparison of simulated and modeled subthreshold drain current as a function of gate voltage for DG-nMOS and DG-pMOS devices.

The extracted values permit a straightforward and accurate model applicable for ULP applications for DG-pMOS and DG-nMOS. The model compares well with Technology Computer-Aided Design (TCAD) data [40]. The comparative analysis of the same is illustrated in Fig. 2.7. The modelled data, using equation (2.1) agrees well with the simulated data as shown in Fig. 2.7.

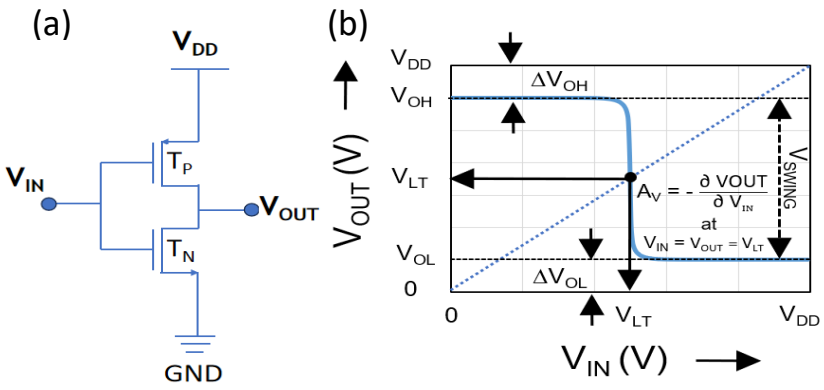

Fig. 2.8 (a) Schematic of CMOS inverter. (b) DC voltage transfer characteristic (VTC) curve of CMOS inverter.

2.2 Subthreshold CMOS Inverter

Despite the advancements in integrated circuits (ICs) aimed at enhancing speed and design efficiency, the issue of power consumption has emerged as a significant concern [41]. Particularly in battery-operated devices like wristwatches, implantable pacemakers, hearing aids, and compact laptops, low-power technology (LPT) has seen limited evolution [42]. As electronic systems strive for greater capabilities, power demands pose a formidable barrier to further progress in microelectronic technology. To address this challenge, there is a push towards smaller transistor size to boost processor speed and accommodate additional features, inevitably leading in higher power density. However, switching devices to subthreshold operation holds promise for mitigating the challenges of power consumption.

2.2.1 Schematic of CMOS Inverter

The CMOS inverter is shown in Fig. 2.8(a) where T_p represents DG-pMOS transistor and T_n represents DG-nMOS [35]. In Fig. 2.8(b), V_{IN} is the input voltage, V_{OUT} is the output voltage and V_{DD} is the supply voltage [35]. The width, W_P, of transistor T_P is maintained at 100 nm, while the width, W_n, of transistor T_n is maintained at 50 nm (which is also equal to gate length L).

For the shown circuit in Fig. 2.8(a), the corresponding voltage transfer characteristic (VTC) is shown in Fig. 2.8(b) [42]. The VTC curve encompasses essential figures of merits (FOMs) such as output high voltage (V_{OH}), output low voltage (V_{OL}), voltage swing (V_{SWING}), logic threshold voltage (V_{LT}), and voltage gain of inverter at V_{LT} (A_v). These FOMs are dependent upon various parameters, including transistor dimensions and $V_{DD.}$ V_{OH} represents the high output voltage when V_{IN} is 0 V. V_{OL} indicates the low output voltage when V_{IN} equals V_{DD}. V_{SWING} refers to the output voltage swing, denoting the disparity between V_{OH} and V_{OL}. V_{LT} denotes the logic threshold voltage of the circuit, signifying the point at which the output voltage transitions from high to low. At this juncture, both V_{IN} and V_{OUT} are equal to V_{LT}. Gain, A_V, signifies the rate of change of output voltage (V_{OUT}) concerning input voltage (V_{IN}) $(-\partial V_{OUT}/\partial V_{IN})$ when V_{IN} equals V_{LT}. This point marks the apex of gain within the circuit [42].

2.2.2 Equivalent Representation of MOSFET

In the subthreshold CMOS inverter circuit, DG-MOSFET can be replaced by current source or resistor according to output and input voltages [36]. Whenever V_{DS} of MOSFET is higher than V_T then it acts as a constant current source, and MOSFET can be represented as shown in Fig. 2.9(a). Similarly, whenever the V_{DS} of MOSFET is lower than V_T, then it acts as a resistor, and MOSFET can be represented as shown in Fig. 2.9(b) [36]. These transformations are indicated by equations (2.10-2.11) are shown below.

$$I_{DS} \simeq \beta\, e^{\frac{V_{GS}}{\eta V_T}} \tag{2.10}$$

$$R_{eq} = \frac{V_T}{\beta\, e^{\left(\frac{V_{GS}}{\eta V_T}\right)}} \tag{2.11}$$

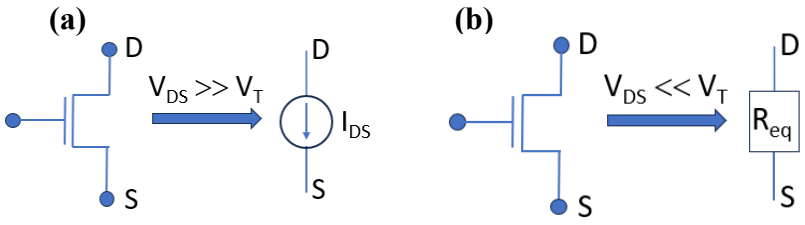

Fig. 2.9 Behavior of MOSFET as (a) constant current source, and (b) resistor [36].

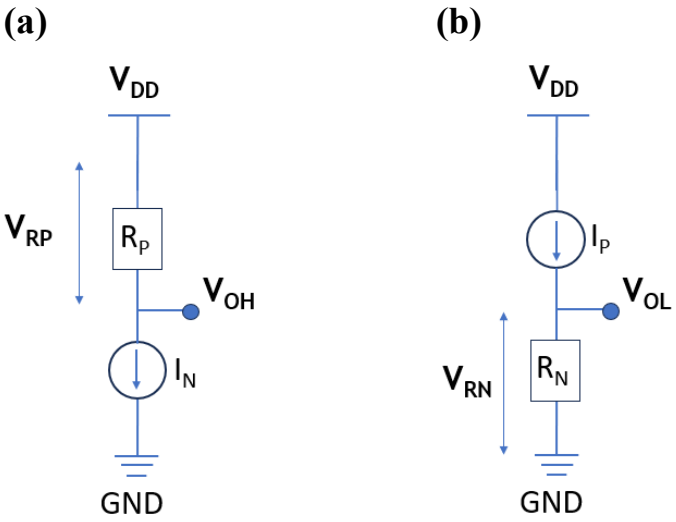

Fig. 2.10 Replacement of T_p and T_n with (a) resistor and constant current source, respectively, and (b) current source and a resistor, respectively [36].

For the high output voltage condition (shown in Fig. 2.10(a)), T_p can be replaced by a resistor and T_n can be replaced by current source. For the

low output voltage (shown in Fig. 2.10(b)), T_p can be replaced by a current source and T_n can be replaced by a resistor. The simulated and modelled data of the above FOMs are discussed below.

2.2.2.1 Output High Voltage

The modeled equation for V_{OH} is given below, where β_N, and β_P are the strengths of transistor T_n and T_p, respectively [36]. Using equation (2.12), modeled V_{OH} is plotted against the simulated data. Fig. 2.11 shows a good match between model and simulation. The output high voltage mainly depends on two parameters, V_{DD} and the ratio of the strengths of transistors. When V_{DD} increases, V_{OH} also increases. Similarly, a stronger pMOS in comparison to nMOS causes V_{OH} to increase.

$$V_{OH} = V_{DD} - V_T \left(\frac{\beta_N}{\beta_P}\right) e^{\left(\frac{-V_{DD}}{\eta_P V_T}\right)} \qquad (2.12)$$

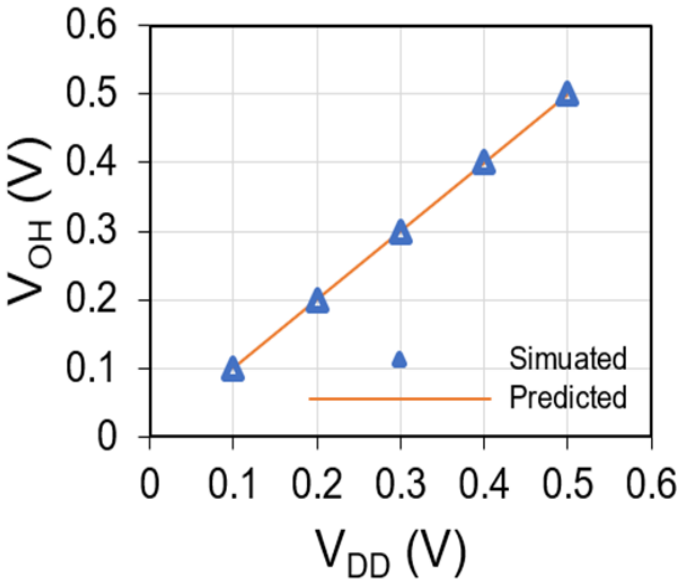

Fig. 2.11 Dependence of simulated and modelled V_{OH} on V_{DD}.

2.2.2.2 Output Low Voltage

The modeled equation for V_{OL} is given below, where β_N, and β_P are the strengths of transistors T_n and T_p, respectively [42]. Using the equation (2.13), modeled V_{OL} is plotted modelled data against the simulated data. The modelled and simulated data of V_{OL} shows a good match in Fig. 2.12. The V_{OL} mainly depends on two conditions, V_{DD}, and the strength of transistors. When supply voltage V_{DD} increases, V_{OL} decreases, and when pMOS is weaker than nMOS, then V_{OL} decreases.

$$V_{OL} = V_T \left(\frac{\beta_P}{\beta_N}\right) e^{\left(\frac{-V_{DD}}{\eta_N V_T}\right)} \tag{2.13}$$

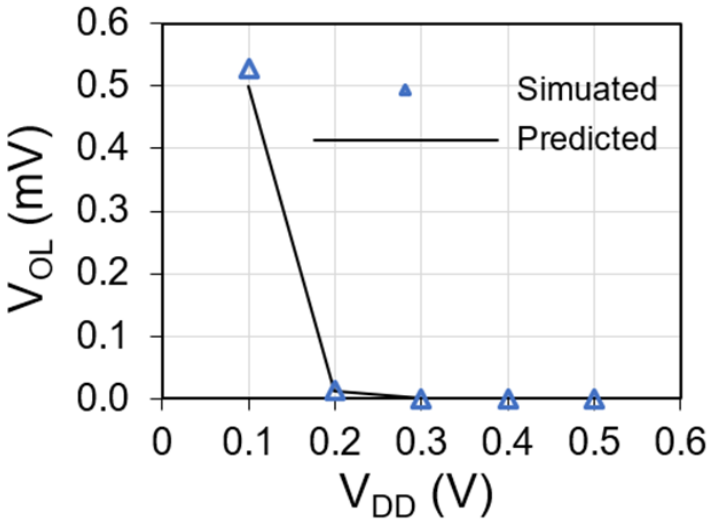

Fig. 2.12 Dependence of simulated and modelled V_{OL} on V_{DD}.

2.2.2.3 Voltage Swing

V_{SWING} refers to the output voltage swing, denoting the disparity between ideal values of V_{OH} and V_{OL}, which is shown in equation (2.14). V_{SWING} is the difference between output high voltage and the output low voltage [42]. When V_{DD} increases, V_{SWING} also increases, and the same is shown in Fig. 2.13.

$$V_{SWING} = V_{OH} - V_{OL} \quad (2.14)$$

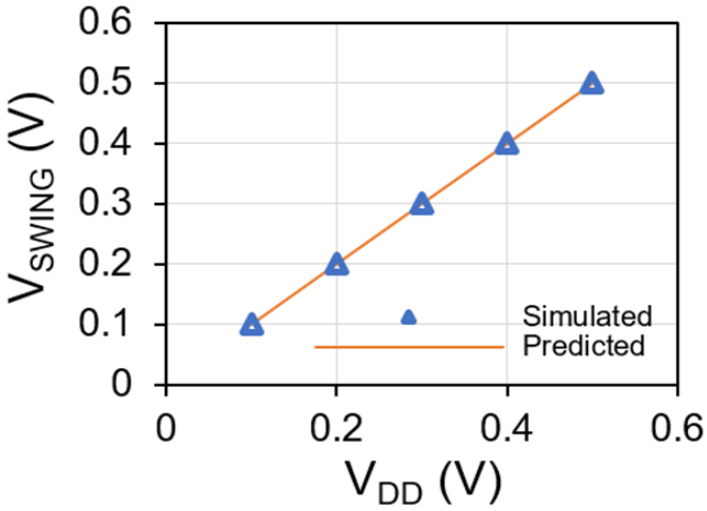

Fig. 2.13 Dependence of simulated and modelled V_{SWING} on V_{DD}.

2.2.2.4 Logic Threshold

This logic threshold voltage (V_{LT}) depends on various factors including the characteristics of transistors, process variations, temperature, and supply voltage. In practical terms, V_{LT} is crucial for determining the operating conditions and performance of CMOS circuits, as it affects the speed, power consumption, noise margin, and overall reliability of the system.

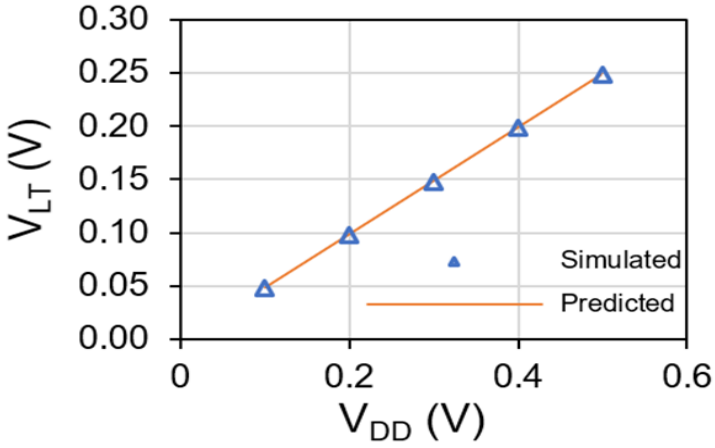

Fig. 2.14 Dependence of simulated and modelled V_{LT} on V_{DD}.

V_{LT} mainly depends on V_{DD} and the strengths of both pMOS and nMOS transistors. When V_{DD} increases, then V_{LT} also increases, which can be seen from the Fig. 2.14, which shows the simulated and modelled data of V_{LT} plotted with V_{DD} for the subthreshold CMOS inverter. When pMOS is stronger than nMOS then V_{LT} shifts to the right side, and if nMOS is stronger than pMOS then V_{LT} shifts to the left side of the ideal mid value of $\left(\frac{V_{DD}}{2}\right)$, which can be observed in Fig. 2.15. V_{LT} was calculated using equation (2.15), which is given as

$$V_{LT} = \frac{V_{DD}}{2} + \frac{\eta V_T}{2} \log_e \left(\frac{\beta_P}{\beta_N}\right) \qquad (2.15)$$

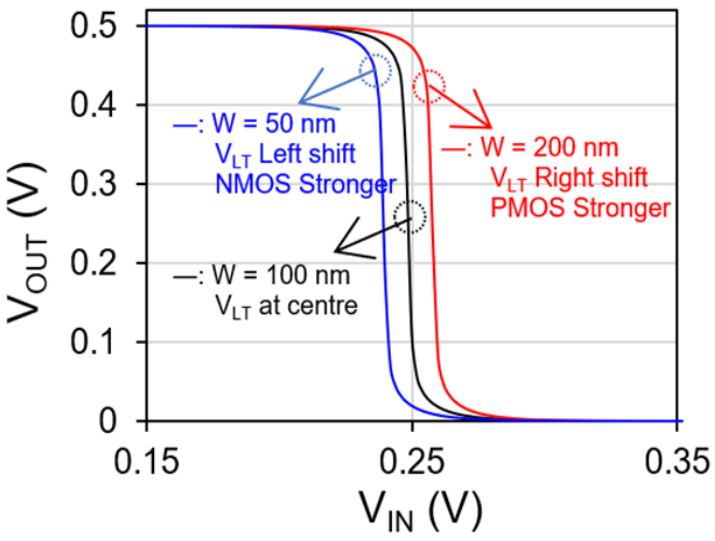

Fig. 2.15 Representation of V_{LT} shifting according to the strength of pMOS and nMOS transistor.

2.2.2.5 Gain of CMOS Inverter at V_{LT}

At V_{LT}, the gain (A_V) of a CMOS inverter is highest. This is because the slope of the transfer curve is steepest at this voltage. A_V depends on many parameters like imbalance factor (U), V_{DD}, η, and δ_{DS}. A_V is maximum when both transistors are at same strength. In this condition, U

will become minimum, as indicated in equation (2.16). When V_{DD} is small then gain is also small and upon increasing the V_{DD}, A_V also increases and its value attains a constant level at higher V_{DD} because the term $\frac{\eta}{\sqrt{1+4(\frac{e^{\frac{V_{DD}}{\eta V_T}}}{U}-1)}}$ becomes much smaller than the δ_{DS}. For the smaller values of η, A_V will always be high.

$$U = \max\left(\frac{\beta_P}{\beta_N}, \frac{\beta_N}{\beta_P}\right) \geq 1 \tag{2.16}$$

$$A_V = \frac{1}{\delta_{DS} + \frac{\eta}{\sqrt{1+4\left(\frac{e^{\frac{V_{DD}}{\eta V_T}}}{U}-1\right)}}} \tag{2.17}$$

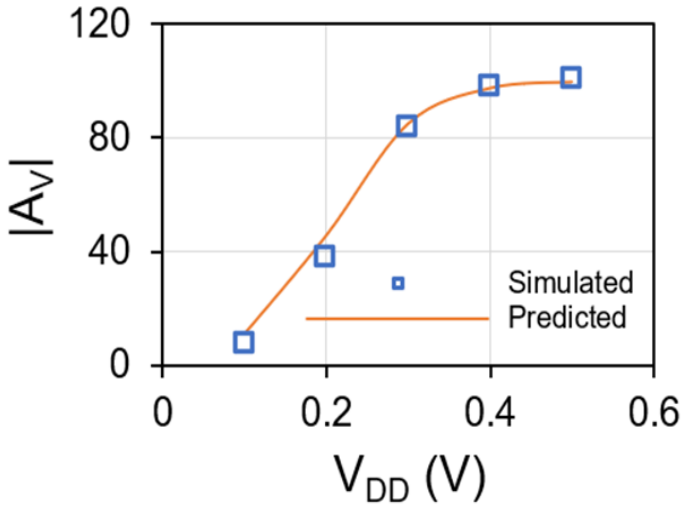

Fig. 2.16 Variation of simulated and modeled A_V as a function of V_{DD}.

2.2.3 Variation of Gain with V_{DD}

The non-linear VTC of CMOS inverter is shown in Fig. 2.17 for different V_{DD} values. When V_{DD} increases then it is observed that sharpness of VTC at V_{LT} increases, which signifies an improvement in A_V with V_{DD}. The same is observed in Fig. 2.16.

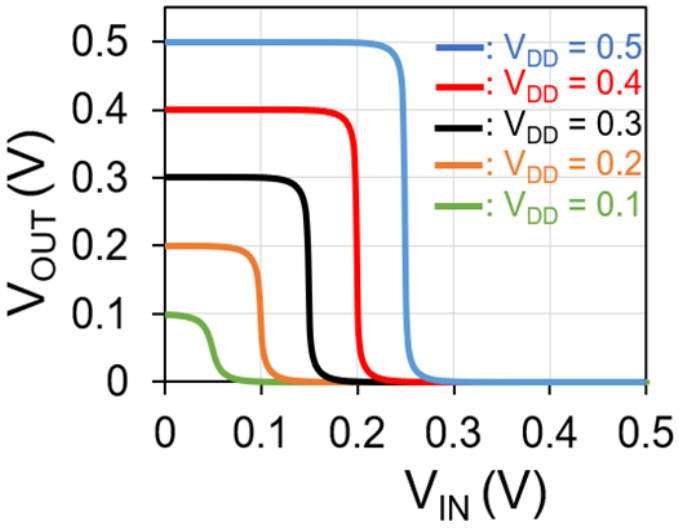

Fig. 2.17 The variation of A_V with respect to V_{DD}.

2.3 Subthreshold Universal Logic Gate

In recent years, circuits operating in the subthreshold region have garnered significant attention due to the increasing demand for low-voltage and low-power solutions [43]. This trend is particularly pronounced in the realm of battery-powered circuits for human implantable biomedical devices. Subthreshold logic is a technique used in low-power VLSI design to reduce circuit V_{DD} to the level of V_{TH} or even below. Subthreshold universal logic gates are used to perform many types of digital operations. In this study, the evaluation is performed for two types of CMOS universal gates: NAND and NOR.

2.3.1 Subthreshold Two-Input CMOS NAND Gate

A two-input NAND gate is a basic digital logic gate that produces high output only when either or both inputs are low [43]. For all other conditions, the output of NAND is low (0). The schematic representation of two-input CMOS NAND gate is shown in Fig. 2.18, where two inputs are A, and B, and output is represented by V_{OUT}. Q1 and Q2 are DG-pMOSFETs whereas Q3 and Q4 are DG-pMOSFETs. Next state for the inputs are A^+ and B^+. If A and B are the inputs then $V_{OUT} = \overline{A.B}$. The truth table of two-input CMOS NAND is shown in table 2.3. If a CMOS two-input NAND gate has Q3 and Q4 transistors on, and Q1 and Q2 transistors off, the output is a logic 0. This condition happens when both inputs, A and B, at logic 1.

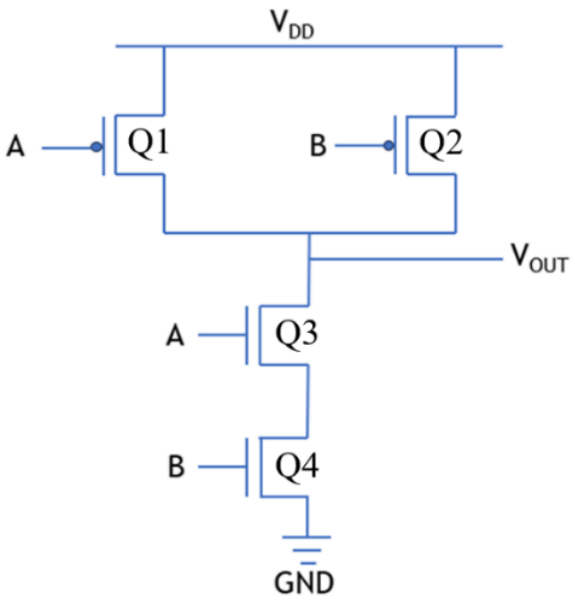

Fig. 2.18 Circuit of two-input CMOS NAND gate [42].

Table 2.3. Truth table of two-input CMOS NAND gate [42].

A	B	V_{OUT}
0	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	0	V_{DD}
V_{DD}	V_{DD}	0

2.3.1.1 Propagation Delay of CMOS NAND Gate

The propagation delay time are defined as the time delay between the 50% crossing of the input and the corresponding 50% crossing of the output [42]. There are six types of propagation delay for two-input CMOS NAND gate. Out of these, three delays are for output low (0) to high (1) conditions (T_{PLH}), and three are for output high (1) to low (0) conditions (T_{PHL}). These T_{PLH} and T_{PHL} delays are shown in Table 2.4-2.5.

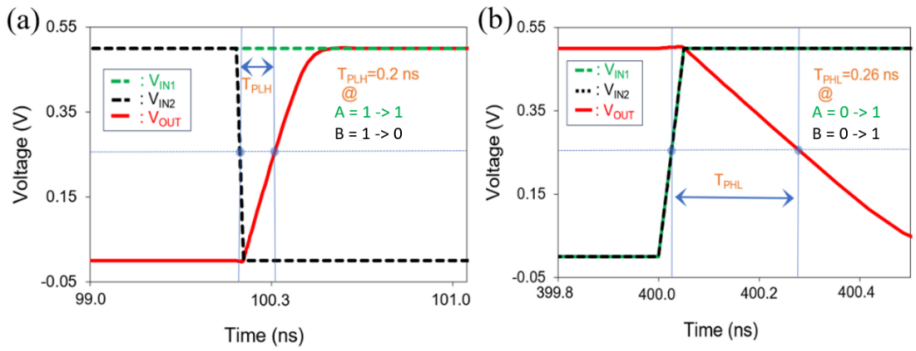

Fig. 2.19 Propagation delay of CMOS NAND gate (a) when output voltage transits from low to high (T_{PLH}). (b) when output voltage transits from high to low (T_{PHL}).

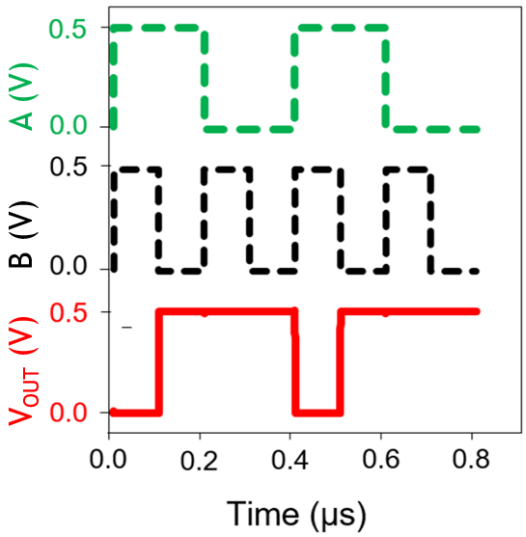

Fig. 2.20 Input and output waveform of V_{OUT} for CMOS NAND gate at 5 MHz.

The propagation delay (T_{PLH}) when output voltage transits from low (0) to high (1) is shown in Fig. 2.19(a), in which the inputs transit from 1→1 and 1→0. In this condition, T_{PLH} is evaluated to be 0.2 ns. The propagation delay (T_{PHL}) when output voltage transits from high (1) to low (0) is shown in Fig. 19(b), in which the inputs transit from 0→1 and 0→1. In this condition, T_{PHL} is evaluated to be 0.26 ns. Fig. 2.20 shows the timing diagram for CMOS NAND gate. In this figure, waveforms of both inputs (A and B) and V_{OUT} are in megahertz frequency range.

Table 2.4 Propagation delay of CMOS NAND when output voltage transits from low (0) to high (1).

A	**B**	**A^+**	**B^+**	**T_{PLH} (ns)**
V_{DD}	V_{DD}	0	0	0.13 (Best)
V_{DD}	V_{DD}	0	V_{DD}	0.22
V_{DD}	V_{DD}	V_{DD}	0	0.20

Table 2.5 Propagation delay of CMOS NAND when output voltage transits from high (1) to low (0).

A	B	A^+	B^+	T_{PHL} (ns)
0	0	V_{DD}	V_{DD}	0.26
0	V_{DD}	V_{DD}	V_{DD}	0.21 (Best)
V_{DD}	0	V_{DD}	V_{DD}	0.25

In table 2.4, the best T_{PLH} delay time is 0.13 ns which is achieved when transition happens from both inputs at high (1) to both inputs at low (0). In this condition, the combination of Q1 and Q2 pMOS transistors give smallest value of equivalent resistance. Similarly, in table 2.5, the best T_{PHL} is 0.20 ns which is obtained when the inputs transit from 0→1 to 0→1. In this condition, the bottom transistor Q4 in on (in present state). Hence, its drain capacitance is already discharged to ground, and in the future state, Q3 and Q4 both are on. Hence, there is no need to discharge capacitance of Q4 transistor again. Therefore, the circuit requires less time to achieve the desired low output voltage.

2.3.1.2 Average Power of CMOS Two-Input NAND Gate

The average power (P_{avg}) of subthreshold CMOS two-input NAND gate can be calculated by taking the product of V_{DD} and the average current through V_{DD} during all logic operations of inputs according to the truth table.

$$P_{avg} = V_{DD}. I_{avg} \qquad (2.18)$$

Substituting the values of V_{DD} and I_{avg}, P_{avg} is obtained to be 65 nW.

2.3.2 Subthreshold Two-Input CMOS NOR Gate

For a two-input NOR gate, the logic is somewhat different compared to a NAND gate [43]. A two-input NOR gate produces a high output only when both inputs are low. The schematic of a two-input CMOS NOR gate is similar to that of the NAND gate, but the transistors are arranged differently to achieve the NOR logic functionality. The schematic of two-input CMOS NOR gate is shown in Fig. 2.21, in which A and B are the inputs, and output is represented by V_{OUT}. Q1 and Q2 are DG-pMOSFETs whereas Q3 and Q4 are DG-pMOSFETs. Next state of the inputs A and B is A^+ and B^+ , respectively. If A and B are the inputs then $V_{OUT} = \overline{A + B}$. The truth table of two-input CMOS NAND is shown in Table 2.6.

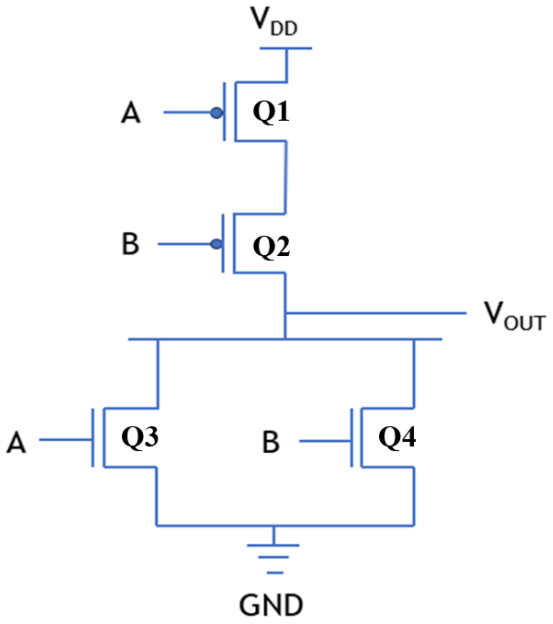

Fig. 2.21 Circuit of two-input CMOS NOR gate [42].

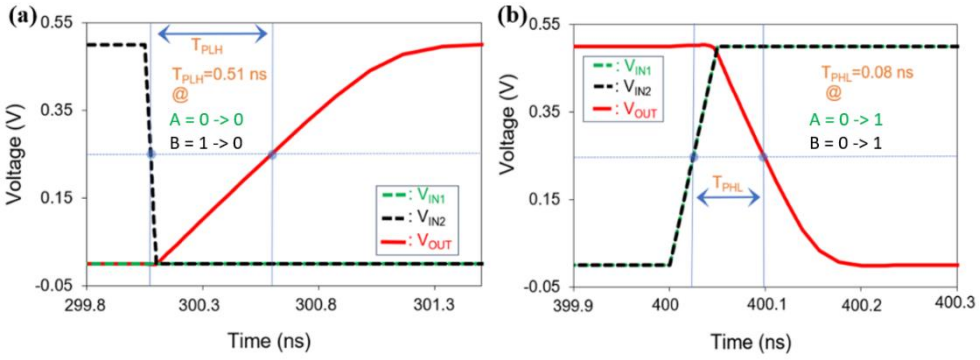

Fig. 2.22 Propagation delay of CMOS NOR gate (a) when output voltage transits from low (0) to high (1). (b) when output voltage transits from high (1) to low (0).

Table 2.6 Truth table of two-input CMOS NOR gate [42].

A	B	V_{OUT}
0	0	V_{DD}
0	V_{DD}	0
V_{DD}	0	0
V_{DD}	V_{DD}	0

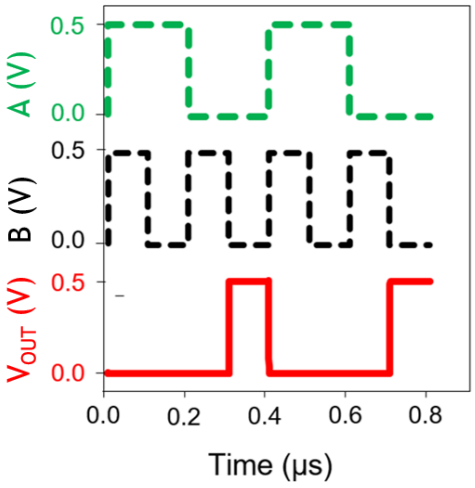

Fig. 2.23 Input and output waveforms of V_{OUT} for a two-input CMOS NOR gate.

2.3.2.1 Propagation Delay of CMOS NOR Gate

There are six types of propagation delay for two-input CMOS NOR gate. Out of these, three delays are for output low (0) to high (1) transitions, and three are for output high (0) to low (1) transitions. These delays are shown in table 2.7-2.8. The propagation delay (T_{PLH}) when output voltage transits from low (0) to high (1) is shown in Fig. 2.22(a), in which the inputs transits from 0→0 and 1→0. In this condition, T_{PLH} is evaluated to be 0.51 ns. The propagation delay (T_{PHL}) when output voltage transits from high (1) to low (0) is shown in Fig. 2.22(b), in which the inputs transits from 0→1 to 0→1. In this condition, T_{PHL} is evaluated to be 0.08 ns. Fig. 2.23 shows the timing diagram for CMOS NOR gate, in which all types of logic combinations are considered using two inputs. In this figure waveforms of both inputs (A and B) and V_{OUT} have megahertz frequency range.

Table 2.7 Propagation delay of CMOS NOR when output voltage transits from low (0) to high (1).

A	B	A^+	B^+	T_{PLH} (ns)
0	V_{DD}	0	0	0.51 (Best)
V_{DD}	0	0	0	0.54
V_{DD}	V_{DD}	0	0	0.55

In table 2.7, the best T_{PLH} is 0.51 ns which is achieved when transition happens from 0→0 and 1→0. In this condition, the combination of Q1 and Q2 pMOS transistors give smallest value of equivalent resistance and capacitor of A is already charged up to V_{DD}. Hence, there is a reduction in time delay. The important point to note is that during T_{PLH} analysis, the focus should be on pull up network of CMOS logic gate circuit, and during the analysis of T_{PHL}, the focus should be on pull down network because pull up network is used to charge the output capacitance and pull-down network is used to discharge the output capacitance.

Table 2.8 Propagation delay of CMOS NOR when output voltage transits from high (1) to low (0).

A	B	A^+	B^+	T_{PLH} (ns)
0	0	0	V_{DD}	0.13
0	0	V_{DD}	0	0.14
0	0	V_{DD}	V_{DD}	0.08 (Best)

Similarly, in table 2.8, the best T_{PHL} is 0.08 ns which is obtained when both the inputs transit from low (0) to high (1) voltage level as the circuit provides the smallest value of equivalent resistance by the parallel combination of Q3 and Q4 nMOS transistors.

2.3.2.2 Average Power of CMOS Two-Input NOR Gate

The average power of subthreshold CMOS two-input NOR gate can be calculated by taking the product of V_{DD} and average current through V_{DD} during all logic operations of inputs according to the truth table.

$$P_{avg} = V_{DD}.I_{avg} \qquad (2.19)$$

Substituting the values of V_{DD} and I_{avg}, P_{avg} is obtained to be 62.9 nW.

2.4 Conclusion

In this chapter, a complete DC analysis of subthreshold CMOS inverter using DG-MOSFET has been described. Simulated and modeled key figure of merits like V_{OH}, V_{OL}, V_{SWING}, V_{LT} and A_V have been computed. V_{OH} depends on transistor strength and supply voltage. The logic threshold voltage remains at half of the supply voltage value (when both transistors have same strength). However, if the strength of T_n is higher than the T_p, then the logic threshold shifts left, otherwise it shifts right with respect to mid value of $\frac{V_{DD}}{2}$ when the strength of T_p is greater than T_n. The

voltage gain is maximum when the strength of both transistors is same, and gain increases with an increase in V_{DD}. This increase in gain is prominent at lower V_{DD} values.

The subthreshold operation of CMOS universal logic gates (NAND and NOR) has been analyzed in respect of operating frequency, propagation delays and average power. Both CMOS NAND and NOR gates are working well up to megahertz frequency, and the average power for the given sequences of logic is 65 nW and 63 nW, respectively.

Chapter 3

Subthreshold Current Mirror

3.1 Simple Current Mirror

As the name suggests, a subthreshold current mirror is designed to operate in the subthreshold region of DG-MOSFET [45]. Subthreshold current mirror find applications in low-power analog and mixed-signal circuits such as in sensor interfaces, biomedical implants, and energy-efficient integrated circuits for Internet of Things (IoT) devices [46], [47]. A simple current mirror circuit consists of two MOSFETs configured to mirror the current flowing through one transistor to the other. This arrangement is commonly used in integrated circuits for various applications, including biasing circuits, current sources, and differential amplifiers [48], [49].

The circuit diagram in Fig. 3.1 illustrates a simple current mirror configuration featuring two identical nMOS transistors, M1 and M2, each with a width (W) of 1 μm. The circuit is powered by a V_{DD} of 0.5 V. A current source, denoted as I_1, is integrated into the circuit, with the output current ranging from 1 nA to 1 μA. This current source is connected with a 1 kΩ resistor, labeled as R_1. The nMOS transistors have their source terminals connected to ground, while their gate terminals are interconnected. Additionally, the drain terminal of M1 is connected to both of the gate terminal. M1 is configured as a diode-connected transistor, which ensures that its gate-to-source bias is equivalent to its drain-to-source bias. Consequently, any fluctuations in the current supplied by I_1 cause corresponding adjustments in the biasing voltages (V_{GS} and V_{DS}) of M1. This configuration allows for precise current replication, as variations in I_1 result in proportional changes in the operating conditions of M2. Thus, M2 effectively mirrors the current flowing through M1, producing an output current that closely resembles the input current (I_1).

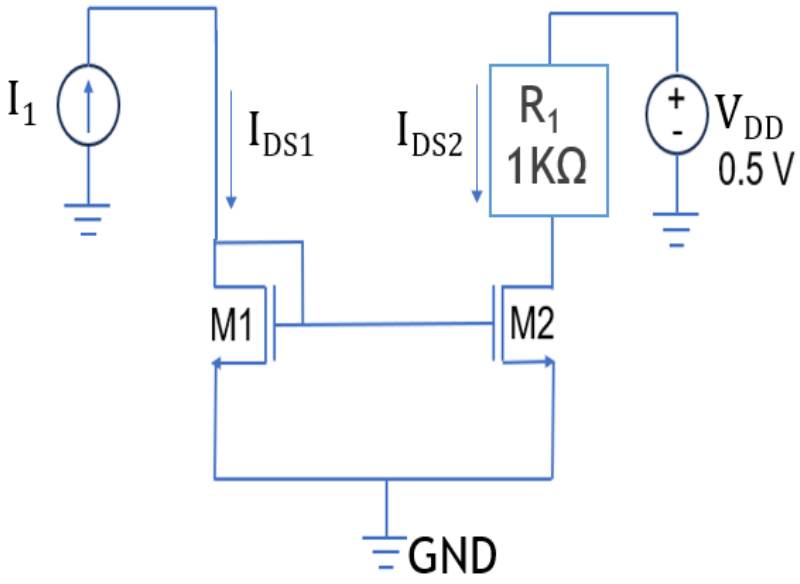

Fig. 3.1 Circuit of simple current mirror at V_{DD} of 0.5 V.

In Fig. 3.1, $I_{IN} = I_{DS_1}$, $I_{OUT} = I_{DS_2}$, and $V_{GS_1} = V_{GS_2} = V_{DS_1}$. Since both the transistors here are identical ($L_1 = L_2$, $\delta_{DS_1} = \delta_{DS_2} = \delta_{DS}$, $\eta_{01} = \eta_{02} = \eta$), therefore $I_{01} = I_{02}$. Also, V_{DS_1} is the drain to source voltage of M_1 nMOS, V_{DS_2} is the drain to source voltage of M_2 nMOS, V_{GS_1} is the drain to source voltage of M_1 nMOS and V_{GS_2} is the drain to source voltage of M_2 nMOS. To analyze the current mirror there is a need to calculate output to input current ratio. The calculation of ratio is carried out using equation (3.1) [35] as

$$\frac{I_{DS_1}}{I_{DS_2}} = \frac{\beta_1}{\beta_2}\left[e^{(\delta_{DS}(V_{DS_1}-V_{DS_2})/\eta VT)}\right]\left[\frac{1-e^{(-V_{DS_1}/VT)}}{1-e^{(-V_{DS_2}/VT)}}\right] \qquad (3.1)$$

As δ_{DS} is very small (value shown in table 2.2 in chapter 2), therefore $e^{(\lambda_{DS}(V_{DS1}-V_{DS2})/nVT)}$ approaches 1. For the subthreshold current (I_1) with range in between 1 nA to 1 µA and V_{DD} = 0.5 V, the last term in

equation (3.1) i.e. $\left[\frac{1-e^{(-V_{DS_1}/VT)}}{1-e^{(-V_{DS_2}/VT)}}\right]$ approaches 1. Therefore, the output to input current ratio can be expressed as

$$\frac{I_{DS_2}}{I_{DS_1}} = \frac{\beta_2}{\beta_1} \tag{3.2}$$

where β_1 and β_1 are the strengths of transistors M_1 and M_2 respectively. Using equation (2.2), the following expression can be obtained

$$\frac{\beta_2}{\beta_1} = \frac{W_2}{W_1} \tag{3.3}$$

where W_1 and W_2 are the widths of transistors M_1 and M_2, respectively. Therefore, the approximated linear equation for simple current mirror circuit is given as

$$I_{DS_2} = \frac{W_2}{W_1} . I_{DS_1} \tag{3.4}$$

Equation (3.4) shows the relation between output and input currents of simple current mirror with some possibility of mismatch error because of difference between V_{DS_1} and V_{DS_2}.

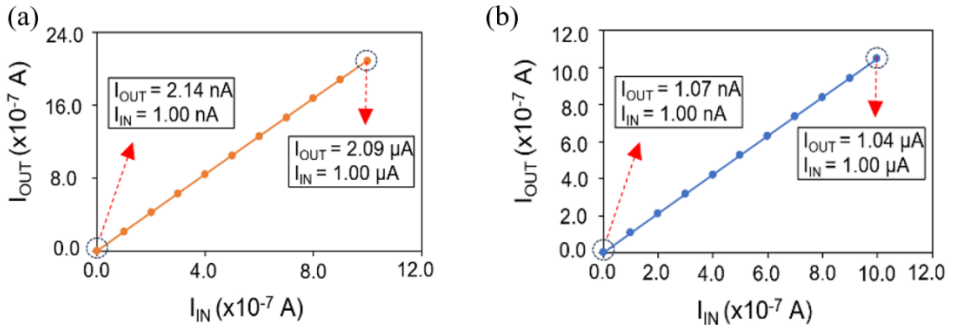

Fig. 3.2 DC output (I_{OUT}) and input (I_{IN}) current curves of simple current mirror at (a) $W_2 = 2W_1$, and (b) $W_2 = W_1$.

Fig. 3.2(a) shows the relationship between output and input currents for simple current mirror which follows the equation (3.4), where the ratio of both currents should be equal to two because W_2 is twice that of W_1. However, from Fig. 3.2(a) it can be concluded that the ratio is not exactly equal to two because of different drain to source voltages of M_1 and M_2. This ratio is also found to change with a change in input current. Also, Fig. 3.2(b) shows the relationship between output and input current. The ratio of both currents should be equal to one because W_2 and W_1 are equal. However, from Fig. 3.2(b) it can be concluded that the ratio is not exactly equal to one because of different drain to source voltages of both transistors M_1 and M_2.

3.2 Cascode Current Mirror

ULP cascode current mirror using nMOS transistors is a circuit configuration commonly employed in integrated circuit design to generate a copy of an input current with high precision and minimal power consumption [50]. In a cascode current mirror, two transistors are arranged in a stacked or cascode configuration to improve performance [51]. In this configuration, M_1 and M_2 form the main current mirror, while M_3 and M_4 serve as the load transistor to improve the output impedance and stability. The input current (I_{IN}) flowing through M_1 is mirrored in the output current (I_{OUT}) flowing through M_2. By carefully designing the circuit, it is possible to create ULP cascode current mirror using nMOS transistors suitable for various applications, especially in battery-powered devices or energy-constrained environments.

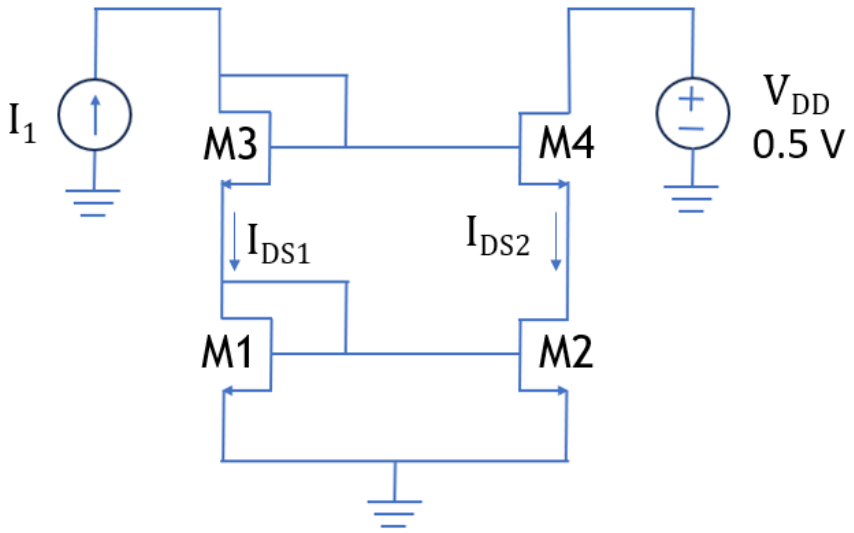

Fig. 3.3 Circuit of cascode current mirror built using four nMOS transistors with a V_{DD} of 0.5 V.

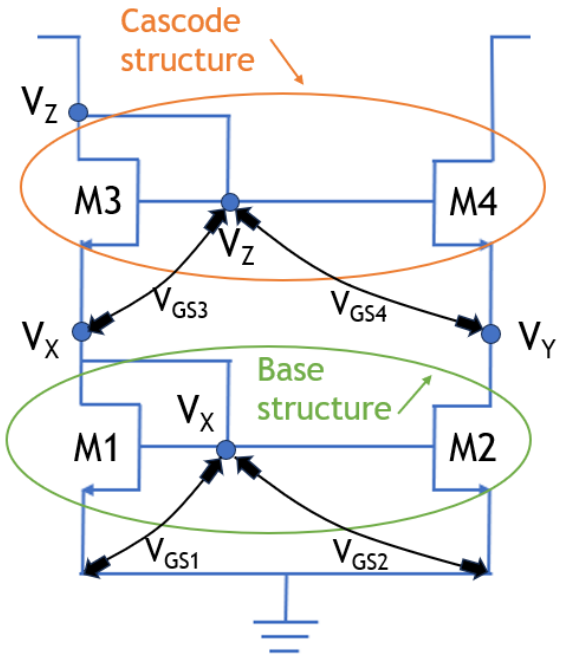

Fig. 3.4 Cascode structure (M3 and M4) and base structure (M1 and M2) part of schematic of cascode current mirror.

In Fig. 3.3 $I_{IN} = I_{DS_1}$, and $I_{OUT} = I_{DS_2}$. Also, $V_{GS_1} = V_{GS_2} = V_{DS_1}$. Since all transistors here are identical, $I_{01} = I_{02}$. V_{DS_1} is the drain to source voltage of M1 nMOS, V_{DS_2} is the drain to source voltage of M2 nMOS, V_{DS_3} is the drain to source voltage of M3 nMOS, V_{DS_4} is the drain to source voltage of M4 nMOS and $V_{DS_1} = V_{DS_2}$.

Cascode current mirror also follows the same output – input current relation as derived in equation (3.4). However, it is more accurate, because both drain to source voltages of M1 and M2 transistors are equal, which is shown in Fig. 3.4. The cascode current mirror shows accurate results as compared to the results of simple current mirror. In Fig. 3.4,

$$V_{GS_1} = V_X \tag{3.5}$$

Since, gate terminal of M1 and M2 transistors are connected, and M1 is diode connected transistor, the following can be written

$$V_{GS_1} = V_{DS_1} = V_{GS_2} = V_X \tag{3.6}$$

The gate to source bias of M1 and M3 transistors will be equal (M1 and M3 are in series). Therefore,

$$V_{GS_3} = V_{GS_1} = V_X \tag{3.7}$$

and

$$V_Z = (2)V_X \tag{3.8}$$

Since M3 and M4 are part of the current mirror, the following relationship is obtained.

$$V_{GS_4} = V_{GS_3} = V_X \tag{3.9}$$

Applying KVL, V_Y can be related to V_Z and V_X as

$$V_Y = V_Z - V_X = V_X \tag{3.10}$$

Equation (3.10) shows that $V_{DS_1} = V_{DS_2}$ because $V_X = V_{DS_1}$ and $V_Y = V_{DS_2}$. Hence, substituting these values in equation (3.1), a relationship between I_{DS_1} and I_{DS_2} is obtained as

$$I_{DS_2} = \frac{W_2}{W_1} . I_{DS_1} \tag{3.11}$$

where $V_{DS_1} = V_{DS_2}$ or $V_Y = V_X$.

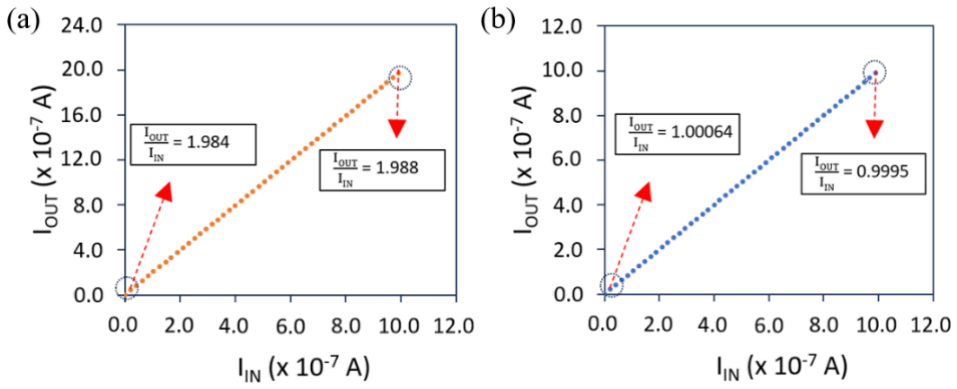

Fig. 3.5 DC output and input currents of cascode current mirror at (a) $W_2 = 2W_1$, and (b) $W_2 = W_1$.

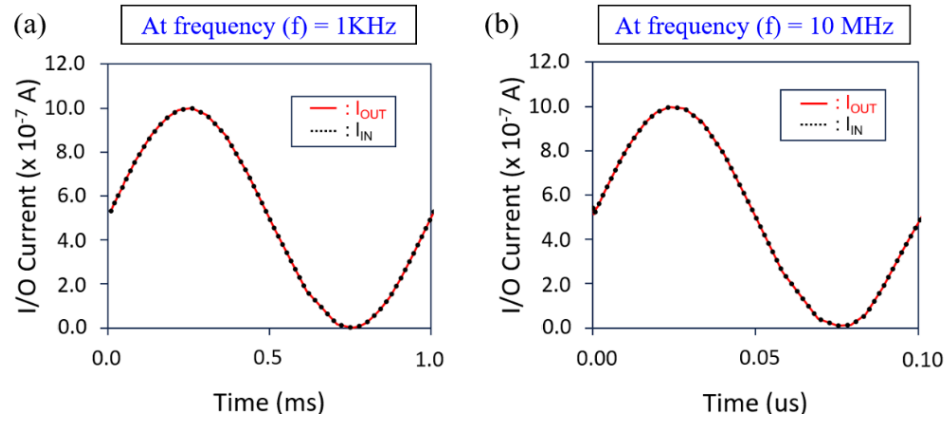

Fig. 3.6 Output and input current waveforms of cascode current mirror at $W_2 = W_1$ (a) at frequency (f) = 1 KHz, and (b) at frequency (f) = 10 MHz.

Fig. 3.5(a) shows the relationship between output and input currents for cascode current mirror which obeys equation (3.4), where the ratio of both currents should be equal to two because W_2 is twice that of W_1. This ratio is remains constant with the change in input current. Also, Fig. 3.5(b) shows the relationship between output and input current for simple current mirror which follows equation (3.4), where the ratio of both currents should be equal to one because W_2 and W_1 are equal. This ratio remains constant with change in input current.

The variation of output current with respect to ac input current at W2 = W1 for two different frequencies (f) 1 KHz and 10 MHz is shown in Fig. 3.6 (a-b). It can be observed that the output current matches well with the input current. It is because drain to source bias voltages of M1 and M2 transistors are equal.

3.3 Comparison Between Current Mirrors

3.3.1 Waveform Comparison

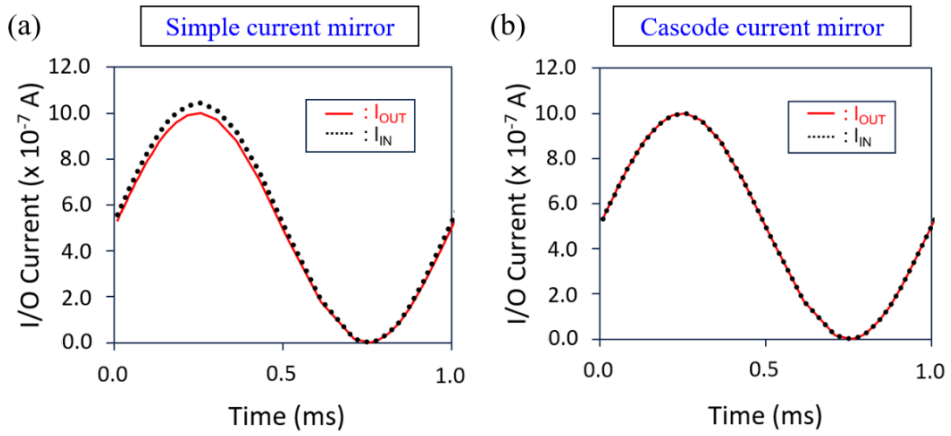

Fig. 3.7 ac output and input current waveform (at 1 KHz frequency) of (a) simple, and (b) cascode current mirrors.

The variation of output waveform with respect to ac input waveform is shown in Fig. 3.7. For simple current mirror, the output current variation with respect to ac input current variation at 1 kHz frequency is not well matched because V_{DS_1} is not exactly equal to V_{DS_2}. This problem is resolved by cascode current mirror and shows an exactly matched ac input and output current variation at 1 kHz frequency in Fig. 3.7(b).

3.3.2 Ratio Change Error Comparison

If the ratio of output and input current varies with a change in input current, then this is defined as the ratio change error [52]. It occurs because of the difference between drain to source biasing of M1 and M2 transistors, and can be calculated by equation (3.6) as

$$\text{Ratio change error (RCE in percentage)} = \left(\frac{\text{initial ratio of } \frac{I_{OUT}}{I_{IN}} - \text{final ratio of } \frac{I_{OUT}}{I_{IN}}}{\text{initial ratio of } \frac{I_{OUT}}{I_{IN}}} \right) \times 100\% \quad (3.6)$$

3.3.3 Ratio Change Error in Simple Current Mirror

If I_{DS_1} varies from 1 nA to 1μA, then at W2 = W1, the initial ratio of $\frac{I_{OUT}}{I_{IN}} = 1.07$, and final ratio of $\frac{I_{OUT}}{I_{IN}} = 1.04$. This can be computed from Fig. 3.2(b). Hence, RCE $= \left(\frac{1.07-1.04}{1.07}\right) \times 100\% = 2.8\%$.

3.3.4 Ratio Change Error in Cascode Current Mirror

If I_{DS_1} varies from 1 nA to 1μA, then at W2 = W1, the initial ratio of $\frac{I_{OUT}}{I_{IN}} = 1.00064$, and final ratio of $\frac{I_{OUT}}{I_{IN}} = 0.9995$. This can be obtained from Fig. 3.4(b). Hence, RCE $= \left(\frac{1.00064-0.9995}{1.00064}\right) \times 100\% = 0.11\%$.

3.4 Conclusion

Based on the results, a comparison between simple and cascode current mirror designed with subthreshold DG-MOSFETs at 500 mV has been carried out. The cascode current mirror gives the better results with lower error as compared to the simple current mirror. This is because of improved V_{DS_1} and V_{DS_2} matching. The ratio change error for simple current mirror is 2.8% while the same for cascode current mirror is calculated to be 0.11%.

Chapter 4

Analog Circuit Design

4.1 Single Stage Amplifiers

Amplifiers designed with subthreshold MOSFETs are relatively simple circuits that can amplify input signals [53]. In these circuits, the current flows between two terminals of MOSFET, and is controlled by the voltage applied at the gate terminal. By the application of voltage to the gate terminal, an electric field is created in the channel between source and drain. This electric field essentially controls the amount of current. To make sure MOSFET works properly for amplification, biasing is used to set the DC operating point. This means using resistors and sometimes a voltage source to set the right DC voltage levels at the gate and drain terminals. Single stage amplifiers have mainly three types of configurations, namely, common source amplifiers, common drain amplifier, and common gate amplifier [53], [54]. Out of these, common source (CS) configuration is most commonly used for amplification.

4.1.1 Common Source (CS) Amplifier

The CS Amplifier with a resistive load is a fundamental configuration in electronic circuits that employs a MOSFET to amplify input signals [54]. In this setup, the input signal is applied to the gate terminal of the MOSFET, and the output is measured from the drain terminal. The source terminal is connected to ground for ac signals, and thus, provides a shared reference point. One of the distinctive features of the CS amplifier is its voltage gain. The voltage gain can be relatively high, especially when a resistive load is used. The voltage gain is primarily determined by the ratio of the load resistor (connected between the drain terminal and the supply) to the internal output resistance of the MOSFET.

By adjusting the values of these components, the voltage gain of the amplifier can be tailored to meet the requirements of an application.

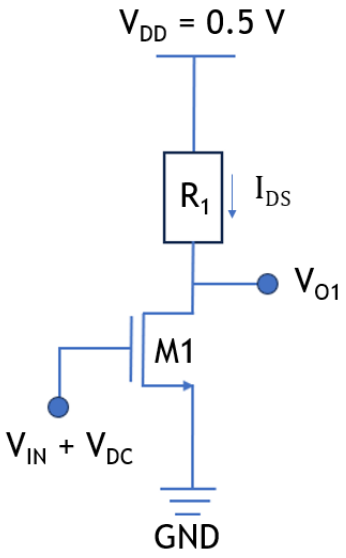

Fig. 4.1 Circuit of single stage common source (CS) amplifier with resistive load at V_{DD} = 0.5V.

Another key characteristic of the CS amplifier with a resistive load is its input and output impedance [55]. The input impedance of the amplifier is relatively high and is primarily determined by capacitance of the MOSFET at input side, along with biasing resistors. This high input impedance allows the amplifier to interface effectively with signal sources without loading them significantly. On the other hand, the output impedance of the amplifier is relatively high as well and is primarily determined by the internal output resistance of the MOSFET [56]. This high output impedance can lead to signal attenuation when driving low impedance loads directly. To mitigate this effect, impedance matching techniques or additional buffer stages may be employed.

Biasing plays a crucial role in the operation of CS amplifier with a resistive load. Biasing establishes the DC operating point of the MOSFET, ensuring it operates within its linear region for proper amplification of ac signals. Typically, a biasing network consisting of resistors and a DC voltage source is employed to set the appropriate DC voltage levels at the gate and drain terminals. In short, the CS amplifier with a resistive load offers relatively high voltage gain, high input impedance, and moderate output impedance. These characteristics make it suitable for various applications where voltage amplification is required, such as in audio amplifiers, instrumentation, and communication systems. However, careful consideration of biasing and impedance matching is essential to achieve optimal performance and efficiency in MOSFET amplifier circuits.

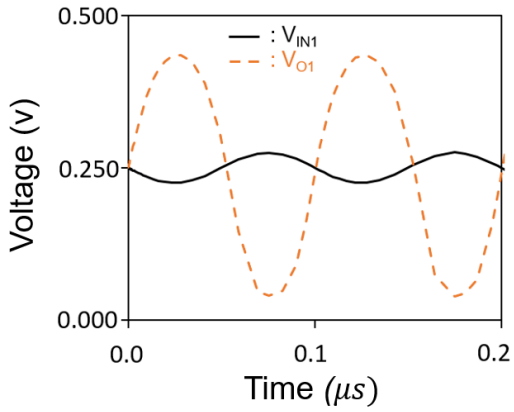

Fig. 4.2 Output and input voltage waveforms of single stage CS amplifier with resistive load at V_{DD} = 0.5 V.

Fig. 4.1 shows the schematic of single stage CS amplifier with a resistive load in which DG-nMOS is denoted by M1 and V_{DD} of 0.5 V is applied. R_1 is biasing resistor, V_{IN} is ac input signal which needs to be amplified, and V_{DC} is DC input voltage to maintain the transistor in desired region, which is subthreshold for this study. I_{DS} is drain to source current

which is flowing through biasing resistor R_1 and output V_{01} is taken from the drain terminal of M1 transistor. An input ac voltage V_{IN}= (0.025) sin(ωt) V, where ω = 2πf is angular frequency in radian per second, f (= 10 MHz) is frequency, and t is time in seconds (s) has been applied. The output (V_{O1}) voltage follows the equation $V_{O1} = V_{DD} - I_{DS_1} R_1$, where R_1 is 7.5 MΩ. The output and input voltage waveforms are plotted in Fig. 4.2. According to the selected parameters, the output voltage swing is calculated to be 0.379 V. Since $\Delta V_{01} = 0.379$ V and $\Delta V_{IN_1} = 0.05$ V, the gain is found to be 7.58, at f = 10 MHz.

CS amplifiers with resistive loads encounter several challenges that can be mitigated by using a differential amplifier configuration [54], [57]. Some common problems faced in CS amplifiers with resistive loads can be improved using a differential amplifier. These issues are outlined below.

(a) Common-Mode Rejection Ratio (CMRR): CS amplifiers are susceptible to common-mode noise, which refers to noise that is present in both the inputs. This can result in unwanted signals being amplified along with the desired signal. Differential amplifiers, by design, amplify the difference between two input signals while rejecting common-mode signals [54]. Therefore, they inherently offer superior common-mode rejection compared to single-ended amplifiers.

(b) Input and Output Impedance Matching: CS amplifiers may suffer from a mismatch between the input impedance of the amplifier and the impedance of the signal source, as well as between the output impedance of the amplifier and the load impedance [54], [57]. This can lead to signal reflections, attenuation, and poor frequency response. Differential amplifiers, especially when configured in a fully-differential topology offer balanced input and output impedances, providing better impedance matching with the source and load.

(c) Noise Rejection: Differential amplifiers can provide better noise rejection as compared to single-ended amplifiers [54], [57]. By amplifying the voltage difference between two input signals, any noise that is common to both inputs (common-mode noise) get cancelled out, resulting in a noise free output signal. This is particularly beneficial in applications where noise is a significant concern, such as in high-gain amplification or low-level signal processing.

(d) Dynamic Range and Linearity: Differential amplifiers can offer improved dynamic range and linearity compared to single-ended amplifiers. By amplifying the difference between two input signals, differential amplifiers can provide a larger output swing without reaching saturation, thus increasing the dynamic range of the amplifier [54], [57]. Additionally, the balanced operation of a fully-differential amplifier can help mitigate even-order harmonic distortion, leading to improved linearity.

(e) Power Supply Rejection Ratio (PSRR): Differential amplifiers typically exhibit better PSRR compared to single-ended amplifiers [54], [57]. This means they are less susceptible to variations in the power supply voltage, resulting in a more stable output signal. Differential amplifiers achieve this through common-mode feedback, which helps attenuate common-mode voltage variations present in the power supply.

By employing a differential amplifier configuration, the problems faced in CS amplifiers with resistive loads can be effectively addressed, leading to improved performance, noise rejection, linearity, and stability in various electronic applications.

4.2 Differential Amplifiers Using DG-MOSFET

A low-power differential amplifier utilizing double-gate MOSFETs (DG-MOSFETs) can significantly enhance noise reduction in electronic circuits. Differential amplifiers are designed to amplify the difference between two input signals while suppressing common-mode signals that are

present on both inputs, effectively minimizing noise and interference. DG-MOSFETs, with their dual-gate structure, offer superior electrostatic control compared to traditional single-gate MOSFETs, leading to enhanced performance and lower power consumption [56]. Featuring two gates (primary and secondary), these transistors offer enhanced control over current flow. In a differential amplifier setup, the primary gates of DG-MOSFET pair receive the differential input signal. This input voltage disparity modulates currents through the respective channels. Due to their symmetrical structure and independent control of the primary and secondary channels, DG-MOSFETs exhibit high linearity, reducing distortion and improving signal fidelity [45].

Moreover, their dual-gate design enables a wide dynamic range operation without significant signal degradation. Consequently, the amplifier can operate over a broad range without compromising performance. Additionally, differential amplifiers employing DG-MOSFETs boast superior common-mode rejection compared to their single-gate counterparts. The secondary gate empowers better control over common-mode signals, enhancing rejection of unwanted noise or interference. Beyond improved rejection and linearity, DG-MOSFET based differential amplifiers offer enhanced transconductance (g_m). The dual-gate architecture effectively increases the effective transconductance, resulting in heightened gain and sensitivity. Such characteristics render them suitable for various applications demanding high performance and low distortion. These applications span communication systems, RF amplifiers, instrumentation, signal processing circuits, and low-noise amplifiers (LNAs), along with integrated circuits designed for wireless communication [54].

4.2.1 Resistive Load Single Stage Differential Amplifier

In a resistive load single-stage differential amplifier utilizing dual-gate DG-nMOSFET. Differential inputs are applied to the primary gates of DG-nMOS pair, inducing current variations through the respective channels. The circuit of resistive load single stage differential amplifier using DG-nMOS is shown in Fig. 4.3, where M1 and M2 are DG-nMOS transistors which operate in subthreshold region using a DC input voltage of V_{DC} and biasing resistors R_1 and R_2. The drain to source currents, I_{DS_1} and I_{DS_2}, flowS through R_1 and R_2, respectively. Input voltages, V_{IN_1} and V_{IN_2}, are applied to the gate terminals of M1 and M2 transistors, respectively, in opposite phases to calculate the differential gain. R_3 is biasing resistor to maintain the common mode rejection ratio. A supply voltage of 0.5 V is applied to the circuit. $|V_{IN_1}| = |V_{IN_2}| = (0.025).\sin(\omega t)$ V, $R_1 = R_2 = 7.5$ MΩ, and $R_3 = 10$ KΩ. Also, $V_{DC} = 0.25$ V.

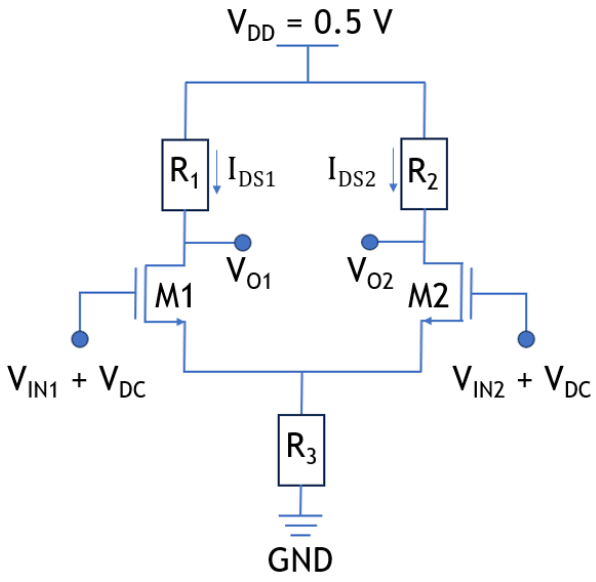

Fig. 4.3 Circuit of single stage differential amplifier with resistive load at $V_{DD} = 0.5$ V.

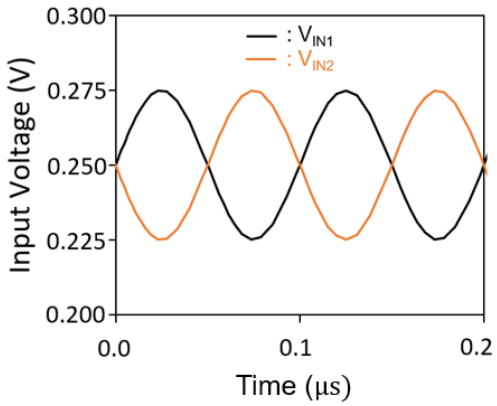

Fig. 4.4 Waveforms of V_{IN_1}, and V_{IN_2} at a frequency of 10 MHz**.**

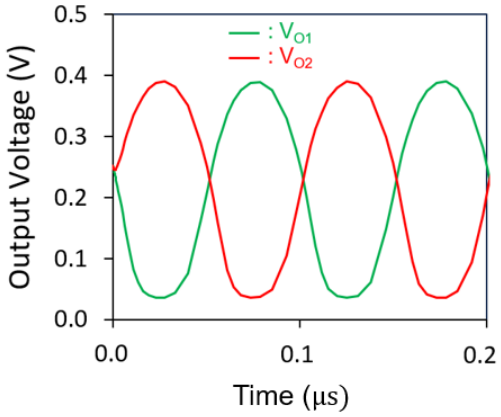

Fig. 4.5 Waveform of V_{O1}, and V_{O2} at a frequency 10 of MHz.

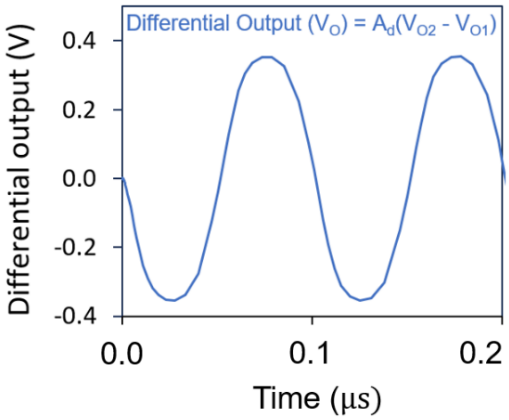

Fig. 4.6 Waveform of differential output voltage (V_O) at frequency of 10 MHz.

To calculate voltages, V_{O1} and V_{O2}, the following equations are used

$$V_{O1} = V_{DD} - I_{DS_1}.R_1 \quad (4.1)$$

$$V_{O2} = V_{DD} - I_{DS_2}.R_2 \quad (4.2)$$

The differential output voltage (V_O) of the circuit shown in Fig. 4.3 is given as

$$V_O = V_{O2} - V_{O1} \quad (4.3)$$

The waveform of V_O is shown in Fig. 4.6. The differential gain A_d of given circuit in Fig. 4.3 is calculated as

$$|A_d| = \frac{|V_{O2} - V_{O1}|}{|V_{IN_1} - V_{IN_2}|} \quad (4.4)$$

After substituting all relevant values, $|A_d| = 7.1$ at 10 MHz.

4.2.2 Resistive Load Double Stage Differential Amplifier

The single stage differential amplifier (shown in Fig. 4.3) is modified to implement a double stage differential amplifier. This was carried out to achieve a higher differential voltage gain (A_d) as compared to that achieved by a single stage differential amplifier. Applied input voltages, $V_{IN_1} = V_{IN_2}$, is $(1)\sin(\omega t)$ mV. The values of all parameters like R_1, R_2, R_3 are same as those used for single stage differential amplifier. However, the value of DC input voltage V_{DC} is different i.e. V_{DC} = 0.25 V. The waveforms of input, output voltages, and differential output voltage are shown in Fig. 4.7 (a-c). The value of differential output voltage V_0 is calculated to be 0.166 V (equation 4.3). Therefore, the differential gain A_d of double stage differential amplifier is evaluated to be 83 at 10 kHz frequency. The gain of double stage differential amplifier with resistive load

is higher than that of single stage differential amplifier with resistive load. However, the operating frequency is reduced from 10 MHz to 10 kHz.

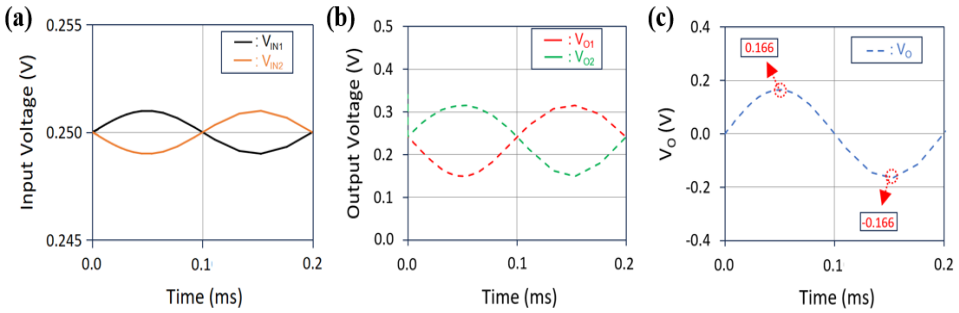

Fig. 4.7 Waveforms at frequency 10 kHz for (a) input voltages (V_{IN_1}, and V_{IN_2}), (b) output voltages (V_{O1}, and V_{O2}), and (c) differential output voltage (V_O).

4.3 Current Mirror Load Single Stage Differential Amplifier

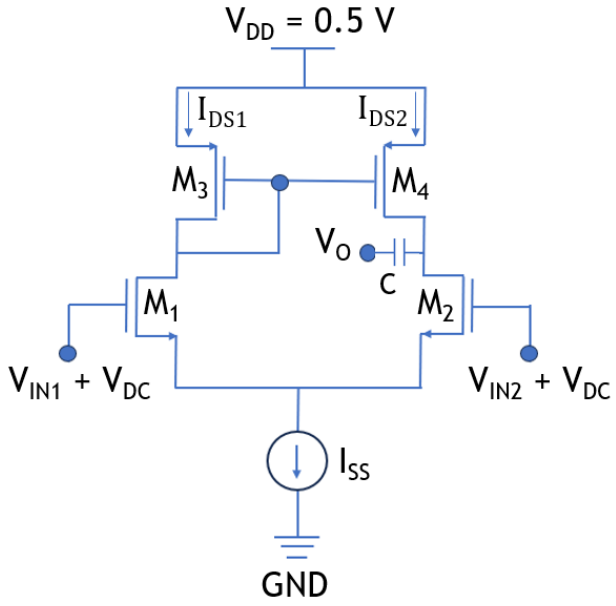

Fig. 4.8 Circuit diagram of current mirror load differential amplifier.

In a current mirror load single-stage differential amplifier utilizing shown in Fig. 4.8, pMOS transistors (M_3 and M_4) are used for the current mirror load, and nMOS transistors (M_1 and M_2) for the differential circuit. The differential amplifier operates by amplifying the voltage difference between two input signals. The two nMOS transistors, M_1 and M_2, form differential pair, with the input signals applied to their gates. Currents generated through M1 and M_2 are mirrored by pMOS transistors M_3 and M_4, constituting the current mirror load. This mirroring ensures balanced differential operation, with the current through M_1 mirrored in M_3, and the current through M_2 mirrored in M_4. The supply voltage is fixed at 500 mV. The output voltage is V_0 which is taken from the drain terminal of M_2 and M_4 transistors. The applied ac input voltages are $V_{IN_1} = V_{IN_2} = 1.\sin(\omega t)$ mV. DC input voltage is same as applied in Fig. 4.3.

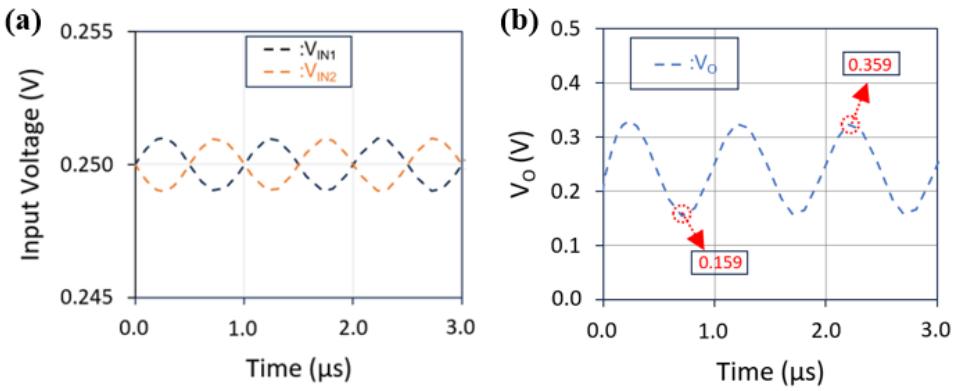

Fig. 4.9 Waveforms at frequency 1MHz of (a) ac input (V_{IN_1} and V_{IN_2}), and (b) ac output (V_O) voltages.

The waveforms of input and output voltages are shown in Fig. 4.9 (a)-(b). The value of differential output voltage V_0 is calculated as

$$|A_d| = \frac{V_0}{|V_{IN_1} - V_{IN_2}|} \tag{4.5}$$

$$V_{0P}(\text{Peak to peak}) = 359 - 189 = 200 \text{ mV} \quad (4.6)$$

$$V_0 = \frac{V_{0P}}{2} = 100 \text{ mV} \quad (4.7)$$

Therefore, the differential gain (A_d) of current mirror load differential amplifier is 50 at 1 MHz frequency.

4.4 Multiple Slope Non-Linear Transfer Function

The circuit shown in Fig. 4.10 is non-linear transfer function circuit which is obtained through a modification of CMOS inverter (shown in Fig. 2.8(a)) [58]. In this circuit, input voltage is connected to the gate terminals of both M1 and M2 (DG-nMOS) transistors. The gate terminal of DG-pMOSFET (M3) is connected to control voltage (V_C). The output voltage (V_O) is taken from the drain terminal of M2 and M3 transistor and source terminal of M1 transistor. The supply voltage is fixed at 0.5 V.

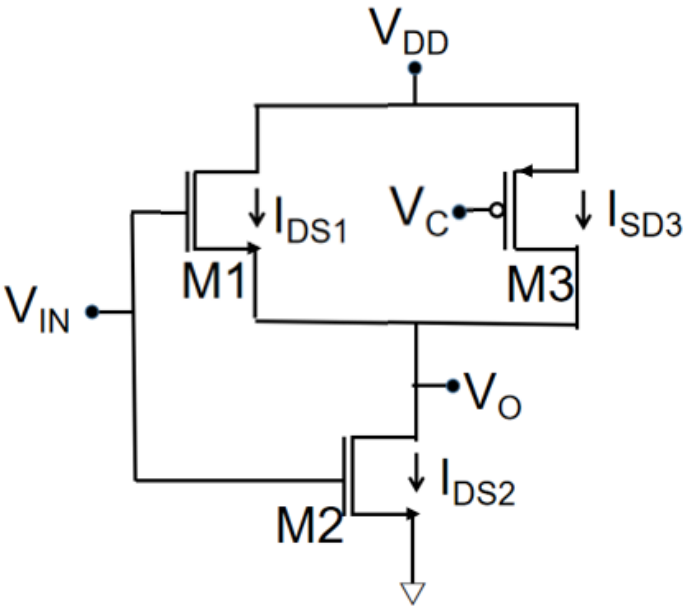

Fig. 4.10 CMOS circuit used to generate VTC with three slopes.

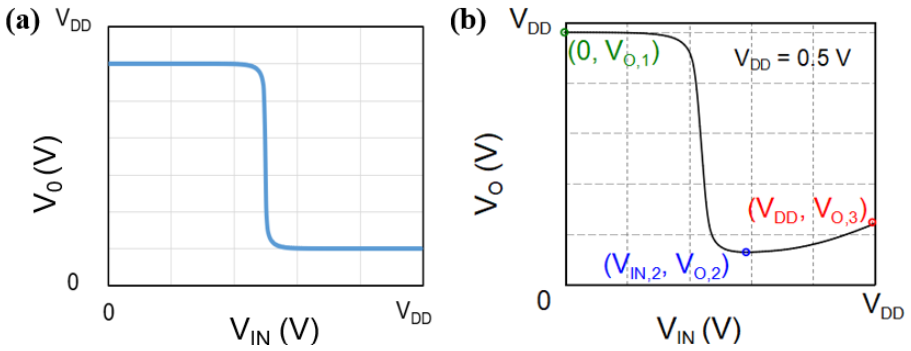

Fig. 4.11 VTC curve of (a) CMOS inverter, and (b) triple slope non-linear transfer function circuit shown in Fig. 4.10.

Two different VTC curves are shown in Fig. 4.11 (a)-(b). Fig. 4.11(a) shows the DC VTC of CMOS inverter with two slopes. However, Fig. 4.11(b) shows three different slopes in the VTC of Fig. 4.11(b) due to the presence of third transistor M1 connected in parallel with M3 transistor.

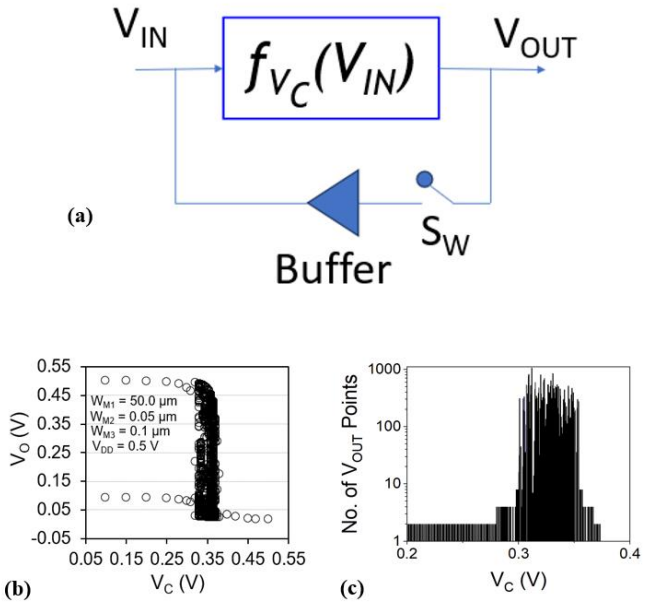

Fig. 4.12 (a) Closed loop feedback circuit with non-linear three slope transfer function. (b) Output voltage (V_O) versus control voltage (V_C) curve, and (c) Variation of V_O with V_C on semi-logarithmic scale.

Fig. 4.12(a) shows the closed loop feedback system using non-linear three slope transfer function circuit shown in Fig. 4.10. The output voltage of this feedback system gives variable number of stable output points at a particular controlling voltage (V_C) and the number of stable output points are shown in Fig. 4.12(b). For initial values of V_C, there are only two stable output points but within the range of 0.32 V to 0.38 V, a significant number of V_O values are generated as shown in Fig. 4.10. As shown in Fig. 4.12(c), only single stable V_O value is obtained at high V_C values.

Random numbers	Converting decimal to 32-bit binary number (using IEEE 754 standard)
0.480367	'00111110111101011111001010101010'
0.110923	'00111101111000110010101110011001'
0.068118	'00111101100010111000000101110011'
0.454822	'00111110111010001101111001101110'
0.099188	'00111101110010110010001100010100'
0.100063	'00111101110011001110110111010101'
0.095712	'00111101110001000000010010100111'
0.124967	'00111101111111111111011010110011'
0.056128	'00111101011001011110011001111001'
0.477627	'00111110111101001000101110000111'
0.109603	'00111101111000000111011110001010'
.	.
.	.
.	.
.	.

Fig. 4.13 Generated random numbers through Fig. 4.12(a), and (b) corresponding 32-bit binary numbers using IEEE-754 standard.

The application of the three-slope non-linear transfer function circuit (Fig. 4.10) is used as a random number generator. The sequence of random numbers can be adjusted through V_C. The random numbers generated at V_C = 0.32 V are shown in Fig. 4.13.

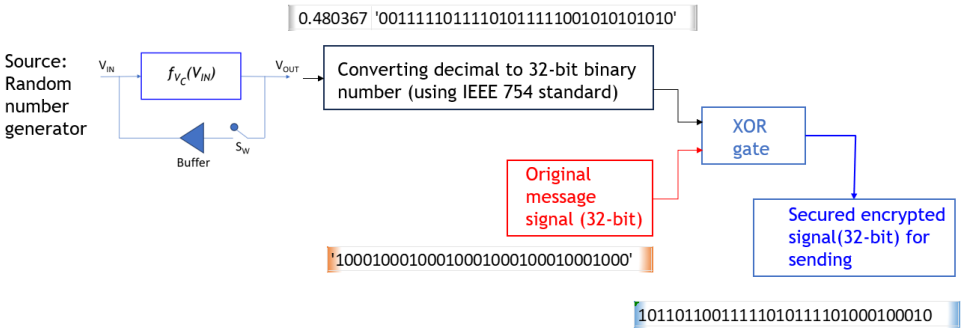

Fig. 4.14 Encryption of 32-bit message signal using non-linear three slope transfer function circuit and XOR gate.

Fig. 4.14 shows the block diagram for encryption in which 32-bit dummy message signal is the input to XOR gate. Another input to the XOR gate is the 32-bit random number (IEEE 754 standard [59]). After this procedure, the output is encrypted 32-bit data.

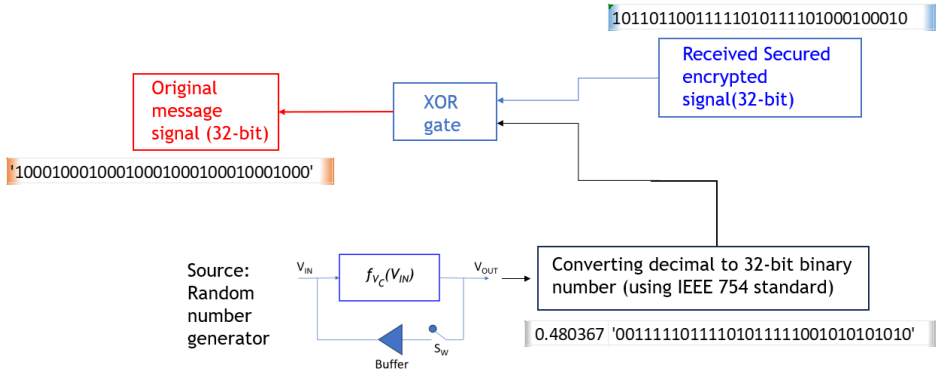

Fig. 4.15 Decryption of 32-bit message signal using non-linear three slope transfer function circuit and XOR gate.

Fig. 4.15 shows the block diagram for decryption of 32-bit data. In this figure, the encrypted data is received and XOR gate is utilized to retrieve the 32-bit message signal.

4.5 Conclusion

This chapter discusses the design of single stage CS amplifiers with DG-MOSFETs. As the gain of CS amplifier at 0.5 V is very low, a double stage differential amplifier is utilized to achieve a higher gain of 83 for the input signal in kilohertz range. Therefore, to maintain reasonable values of frequency and gain, a current mirror load single stage differential amplifier can be utilized as the gain of 50 was achieved at an operating frequency of 1 MHz. The three-slope non-linear transfer function circuit is analyzed, and its application in generating random numbers is described to illustrate encryption and decryption of 32-bit message data.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In this thesis, circuit design challenges are discussed with a focus on ULP applications. ULP circuits are in demand because of low power dissipation in integrated circuits with high packing density. Different types of design techniques such as – voltage scaling, frequency scaling and modern transistors are also discussed to optimized ULP circuit performance.

ULP circuits were analyzed for digital applications through modelling and simulation framework for a subthreshold CMOS inverter through various FoMs. Also, two input subthreshold CMOS universal logic gates (NAND and NOR) were analyzed with their worst and best delays calculations. The average power (P_{avg}) consumption of both universal gates was also analyzed.

For the analog design, simple as well as cascode current mirrors were analyzed. In simple current mirror, the output current was not well matched with input current due to mismatching between drain to source biases of M1 and M2 transistors. In the case of cascode current mirror, the matching between input and output currents was considerably better due to better synchronization between drain to source biases of M1 and M2 transistors.

The operation of CS single stage amplifier at 500 mV was discussed. The low gain of CS amplifier was a matter for concern. Thereafter, single and double stage resistive load differential amplifiers were analyzed, in which single stage amplifier could perform up to megahertz frequency but with a lower value of gain. The double stage amplifier could perform up to kilohertz frequency range with a comparatively higher value of gain. To

maintain appreciable gain and input frequency, a single stage differential amplifier (with current mirror load) could perform up to megahertz frequency range with decent (moderate) gain. The three-slope nonlinear VTC through CMOS circuit at 500 mV was investigated for application as random number generator for encryption and decryption in secure communication systems

5.2 Future Work

Although this thesis work has analyzed ULP circuit based logic families such as CMOS inverter, NAND and NOR gate to work at 500 mV, it would be interesting to explore the minimum supply voltage at which ULP circuits could function. Understanding the intricacies of ULP logic circuit design and balancing the same with efficient approaches could pave way forward for a further reduction in power consumption.

The modeling of non-linear VTC could be another interesting work and the same can be applied to predict the characteristics of closed loop feedback circuit discussed in chapter 4.

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