DESIGN OF LOW POWER FLASH ADC

M.Tech Thesis

By

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DESIGN OF LOW POWER FLASH ADC

A THESIS

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requirements for the award of the degree
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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **DESIGN OF LOW POWER FLASH ADC** in the partial fulfilment of the requirements for the award of the degree of **MASTER OF TECHNOLOGY** and submitted in the **DEPARTMENT OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore,** is an authentic record of my own work carried out during the time period from June 2023 to May 2024 under the supervision of Professor Vipul Singh, Professor, Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

24/05/2024

Signature of the student with date
(Puranjeet Pahari)

This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

24/05/2024
(Prof. Vipul Singh)

PURANJEET PAHARI has successfully given his/her MTech. Oral Examination held on **May 7,2024**.

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Dated: **Puranjeet Pahari**

Dedicated to

Vipul Singh

ABSTRACT

An analog-to-digital converter (ADC) is a circuit that converts continuous analog signals into discrete digital values. It takes an analog signal as input, which is continuously variable over time or amplitude, and converts it into a digital signal, which consists of a series of discrete numerical values.

In the real world computers work with digital data. Analog signals, such as those from sensors, microphones, or cameras, need to be converted to digital form for processing by these digital systems.

Analog signals are susceptible to noise, interference, and degradation over distance. ADCs help in accurately capturing and digitizing these signals, enabling precise measurements and analysis.

Digital data can be easily stored, transmitted, and manipulated as compared to analog signals. ADCs are used for the conversion of analog signals into digital format for storage on digital media like hard drives or transmission over digital communication networks.

ADCs are used over a wide range of resolutions and dynamic ranges for different application requirements.

Digital systems are flexible and reconfigurable. ADCs allow analog signals to be processed and manipulated digitally, making it easier to implement changes and updates in software.

ADCs can be integrated into various devices and systems, ranging from consumer electronics like smartphones and cameras to industrial automation systems and medical devices. Integration simplifies system design, reduces component count, and lowers manufacturing costs.

This project is based on design of low power 3 bit Flash ADC. A 3 bit Flash ADC requires 7 comparators and a thermometer code to binary code encoder. The major issue in the design of Flash ADC is the large power consumption due to the large number of comparators used.

So in order to reduce the power consumption of Flash ADC, we have to design a comparator with very low power consumption.

In this project different comparators were designed and their power consumptions were observed. The comparator with lowest power consumption was selected in the design. Encoder was designed using pass transistor MUX.

Both comparator and encoder were designed and simulated in CMOS 180nm technology. The schematic of the all circuits are designed using LtSpice.

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Chapter 1

Introduction

1.1 Overview

The need for Analog-to-Digital Converters (ADCs) stems from the ubiquitous presence of analog signals in the real world and the growing demand for digital processing, storage, and transmission of information. Several key factors drive the necessity of ADCs:

Compatibility with Digital Systems: Many modern electronic systems, including computers, smartphones, and digital communication networks, are inherently digital. To interface with these systems, analog signals originating from sensors, transducers, or communication channels must be converted into digital format.

Digital Processing and Analysis: Digital signal processing (DSP) techniques offer significant advantages over analog processing, including greater flexibility, precision, and the ability to implement complex algorithms. ADCs facilitate the conversion of analog signals into a digital format that can be manipulated, analyzed, and processed using software and hardware algorithms.

Storage and Transmission Efficiency: Digital data can be stored, transmitted, and processed more efficiently than analog signals. ADCs enable the conversion of analog signals into digital data streams that can be easily stored in memory, transmitted over communication networks, and retrieved without loss or degradation.

Improved Accuracy and Precision: Digital systems can achieve higher accuracy and precision compared to analog systems, particularly over long distances or in noisy environments where analog signals are susceptible to interference and degradation. ADCs enable the precise quantization and representation of analog signals in digital form, allowing for robust signal recovery and processing.

Standardization and Interoperability: Digital communication and data storage standards rely on the use of digital signals. ADCs play a critical role in converting analog signals into standardized digital formats that can be easily interpreted, processed, and exchanged between different devices and systems.

Integration with Digital Control Systems: Many control and automation systems rely on digital signals for precise control and monitoring of processes and equipment. ADCs enable the integration of analog sensors and actuators into digital control systems, allowing for real-time feedback, analysis, and adjustment of system parameters.

Overall, ADCs are essential components in modern electronics, enabling the seamless integration of analog and digital technologies across a wide range of applications, including telecommunications, medical instrumentation, industrial automation, audio processing, and scientific research. Their ability to accurately and efficiently convert analog signals into digital data forms the foundation for the digital revolution that has transformed industries and society as a whole.

1.2 Analog to Digital converters

Analog-to-digital converters (ADCs) are crucial components in modern electronics, enabling the conversion of continuous analog signals into discrete digital representations. This process is essential for capturing real-world phenomena, such as sound, temperature, or voltage, and converting them into a format that digital systems can process and manipulate.

At their core, ADCs function by sampling the analog signal at regular intervals and quantifying its amplitude into binary code. This conversion involves two main stages: sampling and quantization.

Sampling: ADCs sample the analog signal at predetermined intervals, capturing its amplitude at each sampling point. The sampling rate, measured in samples per second (or hertz), determines how frequently the signal is measured and affects the accuracy of the digital representation. Higher sampling rates allow for more precise reconstruction of the original analog signal.

Quantization: Once sampled, the analog signal's amplitude is quantified into a digital representation. This process involves dividing the analog signal's range into discrete levels and assigning a binary code to each level. The number of quantization levels determines the ADC's resolution, with higher resolutions yielding more accurate digital representations of the analog signal.

ADCs come in various types, including successive approximation ADCs, delta-sigma ADCs, and flash ADCs, each with its unique operation principles and applications. These devices play a critical role in numerous fields, including telecommunications, audio processing, medical instrumentation, and industrial automation, where accurate digitization of analog signals is essential for data analysis, control, and communication.

1.3 Types of ADC

Different types of ADC are :

Successive Approximation ADC: This type of ADC operates by iteratively approximating the analog input voltage with a digital value. It starts with the most significant bit (MSB) and successively narrows down the range until the digital output converges to a value close to the analog input. Successive approximation ADCs are known for their relatively high accuracy and moderate conversion speed, making them popular in various applications.

Flash ADC: Flash ADCs are renowned for their high-speed operation. They use a series of voltage comparators to quickly determine the input voltage's approximate level. The output of these comparators directly corresponds to the digital output, with each comparator representing one bit of the digital word. While flash ADCs offer excellent speed, they often require a significant number of comparators, leading to increased power consumption and complexity.

Delta-Sigma ADC: Delta-sigma ADCs excel in applications requiring high resolution and low noise. They utilize oversampling and noise shaping techniques to achieve high-resolution conversion. Delta-sigma ADCs sample the input signal at a frequency much higher than the Nyquist rate, which allows them to suppress quantization noise effectively. While delta-sigma ADCs offer excellent resolution and noise performance, they typically operate at slower speeds compared to other types.

Pipeline ADC: Pipeline ADCs combine the speed of flash ADCs with the resolution of successive approximation ADCs. They achieve this by dividing the conversion process into multiple stages, each handling a portion of the conversion. Each stage contributes a bit to the final digital output, allowing pipeline ADCs to achieve high-speed conversion while maintaining respectable resolution. Pipeline ADCs are commonly found in applications requiring both speed and accuracy, such as high-speed data acquisition systems and telecommunications equipment.

Chapter 2

Literature Review

1. Design of Low Power 0.8V Flash ADC using TIQ in 90nm Technology

This paper present a design of a 4-bit low power Flash ADC using Threshold inverting Quantization (TIQ) Comparators. The proposed TIQ comparator based ADC does not require resistor ladder and therefore leads to area and power saving. TIQ comparator compared input signal with internally generated switching voltage and produce thermometer code. An efficient thermometer to binary converter has been design using transmission gate based 2:1 multiplexer. The design is operated at 800mV of input frequency 1KHz, with reduced power consumption of 14.08uW and 200us delay.

2. Inverter Threshold Comparator based optimized 3-bit Flash ADC

In this work Inverter Threshold Comparator based topology is combined with a mux-based encoder, thereby limiting the total number of transistors to 36 and yielding an area of 0.0039 mm2 and power consumption of 27.44 uW for a 10 MS/s sampling rate, after layout extraction.

3. A 7GS/s, 1.2 V. Pseudo logic Encoder based Flash ADC Using TIQ Technique

In this paper, a novel architecture implementation for the 4-bit flash ADC is proposed. The design is suitable for low power high-speed applications.

The architecture utilizes Threshold Quantization technique (TIQ), the gate sizes are carefully selected so that the input and output rise- and falltimes are about equal. The TIQ technique has been utilized here

in order to meet low power requirements and for better implementation in SoC applications. The circuit is designed in CMOS 90 nm technology.

4. A Low-Power Hybrid ADC Architecture for High-Speed Medium-Resolution Applications

In this paper a low-power hybrid analog-to-digital converter (ADC)

architecture for high-speed medium-resolution applications is introduced. The architecture is a subranging timeinterleaved ADC. In the first stage, a fast flash ADC resolves the three most significant bits. The remaining bits are generated by four time-interleaved low-power successive approximation register (SAR) ADCs, leading to 8-bit 1GS/s operation overall.

Chapter 3

Flash ADC

3.1 What is Flash ADC

A Flash ADC, or Flash Analog-to-Digital Converter, is a type of analog-to-digital converter known for its high-speed operation. It's particularly suitable for applications where speed is paramount, such as in communication systems and data acquisition.

In a Flash ADC, the analog input voltage is simultaneously compared against multiple reference voltages using a series of voltage comparators. Each comparator compares the input voltage to a different reference voltage level. The outputs of these comparators represent the digital code corresponding to the input voltage.

The key characteristic of a Flash ADC is its parallelism. Unlike other ADC types that use sequential approximation or iterative techniques, a Flash ADC produces its output in a single clock cycle. This parallelism enables extremely fast conversion times, making Flash ADCs ideal for applications requiring real-time data processing or high-speed sampling.

However, one of the primary challenges of Flash ADCs is their complexity and power consumption. As the resolution of the ADC increases, the number of comparators required grows exponentially. This can lead to significant power consumption and chip area, making Flash ADCs less practical for high-resolution applications compared to other ADC architectures like successive approximation or delta-sigma ADCs.

Despite these challenges, Flash ADCs remain widely used in applications where speed is critical and resolution requirements are moderate. Their ability to deliver high-speed, simultaneous conversion makes them indispensable in various fields, including telecommunications, radar systems, and high-speed instrumentation.

3.2 Need of Flash ADC

The need for Flash ADCs stems primarily from the demand for high-speed analog-to-digital conversion in various electronic systems and applications. Here's a breakdown of the key reasons why Flash ADCs are essential:

High-Speed Conversion: Flash ADCs are renowned for their ability to provide ultra-fast conversion times. Unlike other ADC architectures that use sequential or iterative techniques, Flash ADCs operate in parallel, enabling them to convert analog signals into digital data within a single clock cycle. This high-speed operation is crucial in applications such as telecommunications, where rapid data processing and transmission are essential.

Real-Time Signal Processing: Many systems require real-time processing of analog signals, where delays in conversion can lead to performance degradation or even system failure. Flash ADCs excel in these scenarios by offering instantaneous conversion, allowing systems to respond rapidly to changing input signals. For example, in radar systems or medical imaging devices, where split-second decisions are critical, Flash ADCs ensure timely and accurate data acquisition.

High-Frequency Signal Sampling: In applications dealing with high-frequency signals, such as wireless communication or radio frequency (RF) systems, traditional ADCs may struggle to keep up with the signal bandwidth. Flash ADCs overcome this limitation with their parallel architecture, enabling them to sample high-frequency signals directly without the need for complex frequency down-conversion or decimation techniques.

Digital Communication Systems: The increasing demand for high-speed data transmission in modern communication systems necessitates ADCs capable of quickly digitizing analog signals. Flash ADCs play a vital role in digital communication systems, including wireless networks, fiber-optic communication, and high-speed internet, where they facilitate the conversion of analog signals into digital data for processing, modulation, and transmission.

Instrumentation and Test Equipment: In fields like test and measurement, where accurate and high-speed data acquisition is essential for analyzing signals and troubleshooting electronic systems, Flash ADCs are indispensable. They enable the rapid capture of analog waveforms with minimal distortion, allowing engineers and researchers to analyze signal characteristics and diagnose performance issues effectively.

Overall, the need for Flash ADCs arises from the growing demand for high-speed, real-time analog-to-digital conversion in a wide range of applications spanning telecommunications, signal processing, instrumentation, and beyond. Their ability to deliver instantaneous conversion makes them invaluable in modern electronic systems where speed, accuracy, and efficiency are paramount.

3.3 Components of Flash ADC

The different components of Flash ADC are

Comparator Array: The heart of a Flash ADC is its comparator array. This array consists of a set of comparators, each of which compares the input voltage with a reference voltage. The comparators operate simultaneously, allowing for high-speed conversion.

Reference Voltage Generator: A Flash ADC requires a precise set of reference voltages against which the input voltage is compared. The reference voltage generator generates these reference voltages, typically using resistor divider networks or other precision voltage reference circuits.

Encoder: Once the input voltage has been compared against the reference voltages, the digital output needs to be encoded. This is usually done using a priority encoder. The priority encoder identifies the highest reference voltage that the input voltage exceeds and produces a binary output corresponding to that reference voltage.

Latch or Register: The binary output from the encoder needs to be held stable while it is processed or transmitted. This is typically achieved using a latch or register circuit.

Clocking Circuitry: A clocking circuitry is used to synchronize the operation of the comparators, encoder, and latch/register. This ensures that all components operate in harmony and produce accurate digital outputs.

Digital Output Interface: The digital output from the Flash ADC needs to be interfaced with external devices or circuits. This may involve level shifting, buffering, or other signal conditioning to match the requirements of the downstream components.

3.4 Block diagram of Flash ADC

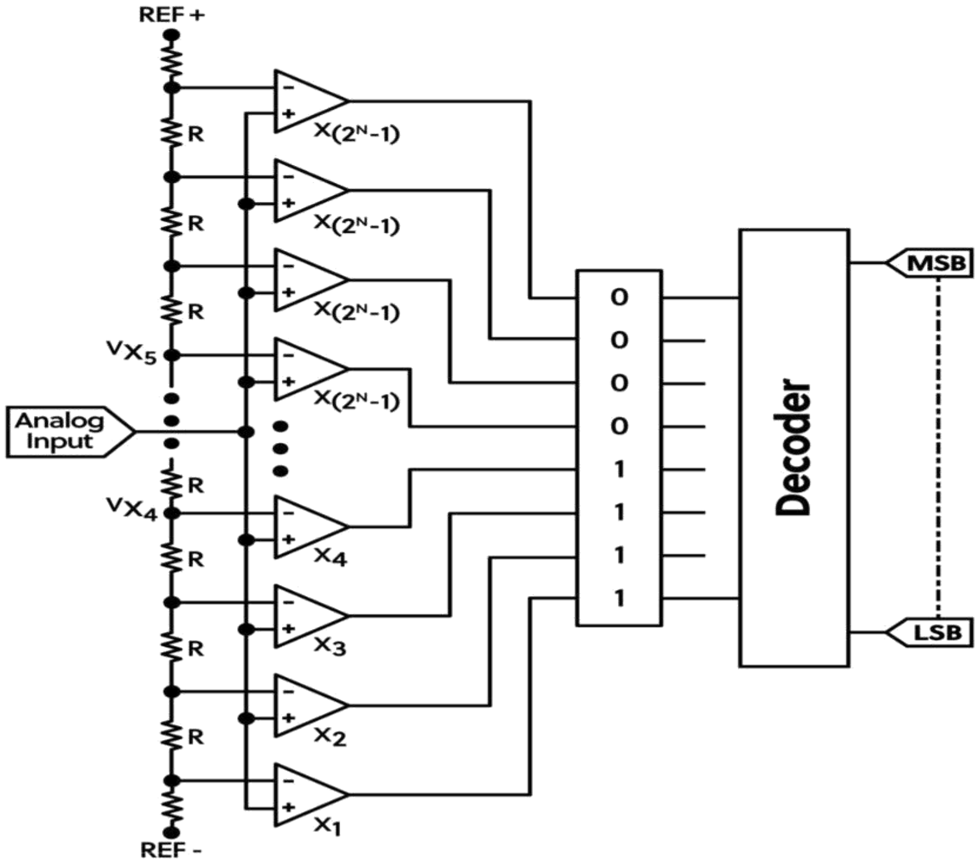

Fig. 3.1 Block diagram of Flash ADC

Chapter 4

Comparators

4.1 What are Comparators

Comparators are essential components in electronics. Comparators are decision-making circuits that compare two analog voltages and produce a digital output based on their relative magnitudes. They're like judges in the realm of electronics, determining whether one voltage is greater than, less than, or equal to another.

Comparators consist of different stages which are input stages, gain stages, and output stages. We can think of them as having three main areas of responsibility: sensing, amplifying, and deciding.

The sensing part is where comparators 'observe' the input voltages. In this stage the comparators typically employ differential input pairs, akin to having two pairs of eyes, to detect the voltage difference between the inputs. This stage acts like the eyes of the comparator, taking in the voltages and preparing them for scrutiny.

Next comes the amplification stage, comparable to a megaphone, where the voltage difference detected by the input stage is amplified. This amplification ensures that even subtle differences in input voltages are magnified enough for the comparator to make a clear decision.

Finally, there's the decision-making part, which is the comparator's main role. Here, it determines whether the amplified voltage difference indicates that one input voltage is higher than the other or vice versa. It's akin to the comparator rendering a verdict based on the evidence provided by the amplified voltage difference.

4.2 Characteristics of Comparators

Speed: Comparators are known for their high speed, enabling them to quickly respond to changes in input voltages. This characteristic is crucial in applications where real-time decision-making is required, such as in high-frequency signal processing or data acquisition systems.

Accuracy: Accuracy is referred as how closely the comparator's output matches the ideal response for a given input. It is essential for reliable decision-making, especially in precision measurement and control applications. Minimizing offset voltage and reducing noise are key factors in improving accuracy.

Resolution: Resolution in comparators is the ability to distinguish between small differences in input voltages. Higher resolution comparators can detect smaller voltage differentials, making them suitable for applications requiring fine-grained discrimination, such as in data conversion systems.

Power Consumption: Power consumption is a critical consideration in comparator design, especially in battery-powered or energy-efficient applications. Low-power comparators are designed to minimize energy consumption while maintaining adequate performance, making them ideal for portable devices or low-power sensor networks.

Input Common-Mode Range: The input common-mode range defines the range of input voltages over which the comparator operates correctly. It is essential to ensure that the input signals fall within this range to prevent distortion or malfunctioning of the comparator.

Offset Voltage: Every comparator has an inherent offset voltage, which is the voltage difference between its two input terminals when their voltages are equal. Minimizing offset voltage is crucial for achieving accurate comparisons, especially when dealing with small input signal levels.

Noise Immunity: Noise immunity refers to the comparator's ability to reject unwanted variations or disturbances in the input signals. Hysteresis and noise filtering techniques are often employed to improve noise immunity, ensuring reliable operation in noisy environments.

Output Swing: The output swing of a comparator refers to the total range of output voltage levels it can provide. It's essential for ensuring compatibility with downstream circuitry and for driving loads effectively.

Temperature Stability: Comparator performance can vary with temperature changes, so maintaining stability across temperature ranges is crucial, especially in industrial or automotive applications where operating conditions can vary widely.

Size and Package: The physical size and package of comparators can vary depending on the application requirements and constraints. Surface-mount packages are common for compact and integrated designs, while larger packages may be used for high-power or high-voltage applications.

4.3 Proposed comparators

4.3.1 Differential comparators

Differential comparators are specialized circuits used in electronics to compare the difference between two input voltages. Unlike basic comparators that compare a single voltage against a reference, differential comparators consider the relative voltage between two inputs, making them particularly useful in applications where precise measurement of the voltage difference is required. Different applications of differential comparators are [6] [7]:

Dual Input Configuration: Differential comparators have two input terminals, often labeled as non-inverting and inverting inputs. These inputs allow for the comparison of two different voltage levels. The non-inverting input typically receives one voltage signal, while the inverting input receives another. The output of the comparator then indicates the relative relationship between these two input voltages.

Precision Measurement: One of the primary applications of differential comparators is in precision measurement systems. By comparing the difference between two voltages, these comparators can accurately determine variations or deviations, making them suitable for applications such as instrumentation, sensor interfaces, and feedback control loops.

Common-Mode Rejection: Differential comparators are designed to reject common-mode signals, which are signals that appear equally on both input terminals. This feature is essential in environments where noise or interference may introduce common-mode voltages, as it allows the comparator to focus on the differential component of the input signals, enhancing accuracy and reliability.

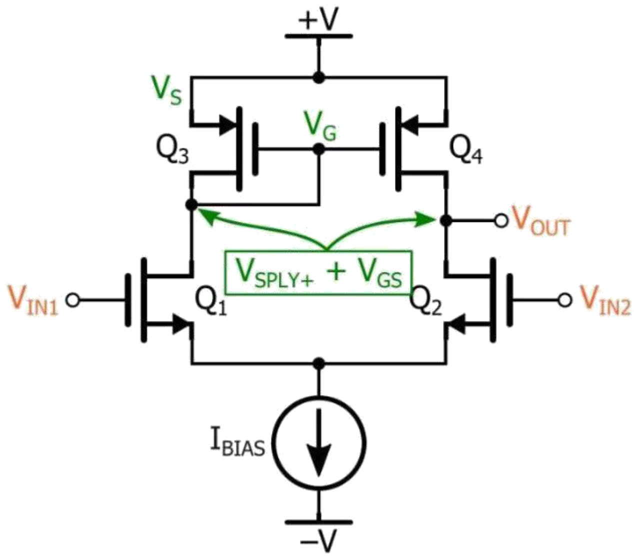

Fig. 4.1 Differential comparator circuit diagram

4.3.2 Open-Loop comparators

Open-loop comparators are essential components in electronics used to compare two input voltages and produce a digital output based on the relative magnitudes of these voltages. Unlike closed-loop comparators, which incorporate feedback to stabilize their operation, open-loop comparators operate without feedback, making them simple and fast but potentially susceptible to issues like oscillation and metastability. Here's an original description of open-loop comparators [6] [7]:

Basic Operation: Open-loop comparators consist of an input stage, amplification stage, and output stage, much like their closed-loop counterparts. However, they lack the feedback mechanism found in closed-loop comparators, meaning that the output is solely determined by the instantaneous difference between the input voltages.

Fast Response: One of the primary advantages of open-loop comparators is their fast response time. Without the need for feedback stabilization, these comparators can quickly respond to changes in input voltages, making them suitable for high-speed applications such as signal conditioning, waveform shaping, and digital-to-analog conversion.

High Gain: Open-loop comparators typically have high gain, amplifying the voltage difference between the input signals to produce a digital output. This high gain allows them to detect small voltage differentials accurately, making them suitable for precision measurement and detection tasks.

Limited Precision: While open-loop comparators offer speed and simplicity, they are often less precise than closed-loop comparators. Without feedback to regulate their operation, they may suffer from issues like offset voltage, noise, and sensitivity to temperature variations, which can degrade their accuracy in some applications.

Single-Ended or Differential Inputs: Open-loop comparators may accept single-ended or differential input signals, depending on the specific application requirements. Single-ended inputs compare a signal against a fixed reference voltage, while differential inputs compare the difference between two input signals.

Applications: Open-loop comparators find use in a wide range of applications, including voltage level detection, signal conditioning, window comparators, and pulse-width modulation (PWM) generation. Their simplicity and speed make them suitable for tasks where precision is not critical, or where external circuitry can compensate for their limitations [6] [7].

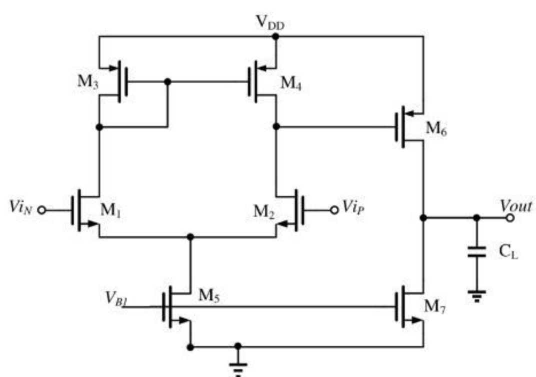

Fig. 4.2 Open-Loop comparator circuit diagram

4.3.3 Threshold Inversion Quantization Comparators

Threshold inversion quantization (TIQ) comparators are essential components in analog-to-digital converters (ADCs) used to convert continuous analog signals into discrete digital representations. These comparators play a crucial role in determining the accuracy and efficiency of the conversion process [4] [5].

In traditional ADC architectures, comparators are typically designed with fixed threshold levels, meaning that the analog input signal must exceed a predetermined threshold to trigger a digital output. However, this approach can be limited in its ability to accurately represent signals with varying amplitudes or in the presence of noise.

Threshold inversion quantization comparators offer a solution to this challenge by dynamically adjusting their threshold levels based on the input signal. Instead of having fixed thresholds, TIQ comparators invert their thresholds depending on the direction of the input signal, hence the term "threshold inversion."

The operation of a TIQ comparator involves comparing the input signal to multiple threshold levels, which are adjusted dynamically. When the input signal crosses a threshold, the comparator output changes accordingly. By adapting the threshold levels to the signal characteristics, TIQ comparators can achieve higher accuracy and better performance compared to traditional comparators.

One of the key advantages of TIQ comparators is their ability to mitigate the effects of noise and signal variations. By dynamically adjusting the thresholds, TIQ comparators can maintain accurate digital representations even in challenging signal conditions. This makes them particularly useful in high-resolution ADCs where precise signal quantization is crucial.

TIQ comparators are commonly used in various applications, including communication systems, sensor interfaces, and instrumentation. Their ability to improve ADC performance makes them an integral part of many analog and mixed-signal designs.

In summary, threshold inversion quantization comparators are dynamic comparators that adjust their threshold levels based on the input signal. This adaptive behavior allows them to achieve higher accuracy and better performance compared to traditional fixed-threshold comparators, making them essential components in modern analog-to-digital conversion systems [4] [5].

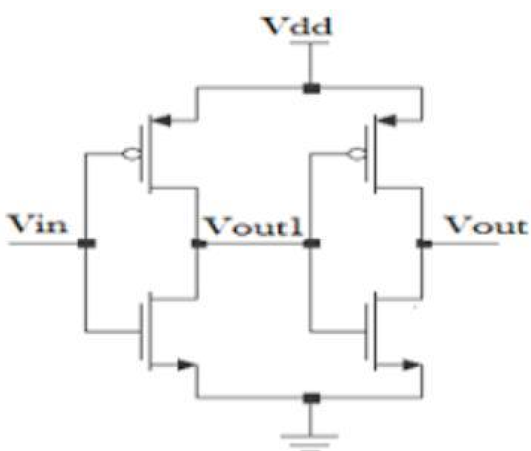

Fig. 4.3 TIQ comparator circuit diagram

Chapter 5

Encoders

5.1 Introduction

Encoders are devices or circuits that transform input data into a specific format suitable for transmission or processing. They are commonly used in digital electronics and communication systems to convert various types of information into binary or digital form. Encoders play a critical role in encoding data such as text, numbers, or signals for transmission over communication channels, storage in memory devices, or processing by digital systems.

Encoders are essential components in digital systems and communication networks, enabling the efficient encoding and processing of data in various formats. They are used in a wide range of applications, including telecommunications, industrial automation, robotics, and consumer electronics, where accurate data encoding and transmission are crucial for system performance and reliability.

5.2 Proposed encoders

5.2.1 NOR Based Encoders

A 3-bit NOR gate-based encoder is a digital circuit that encodes three input lines into a binary code using NOR gates. NOR gates are basic logic gates with two or more inputs and one output. The output of a NOR gate is low (logic 0) only when all of its inputs are high (logic 1); otherwise, the output is high (logic 1).

We can design a 3-bit NOR gate-based encoder using [7] [8]:

Inputs: The encoder has three input lines (A, B, and C), which represent the data to be encoded.

Output Selection: The encoder produces a 3-bit binary output, which can represent up to eight unique combinations (000, 001, 010, 011, 100, 101, 110, and 111).

Logic Implementation: Each output bit of the encoder is generated by a NOR gate.

Output Bit 1 (Y1): This bit is produced by a NOR gate that takes inputs from lines B and C. If both B and C are low (0), indicating that neither input is active, the output of this NOR gate will be high (1).

Output Bit 2 (Y2): This bit is produced by a NOR gate that takes inputs from lines A and C. If both A and C are low (0), the output of this NOR gate will be high (1).

Output Bit 3 (Y3): This bit is produced by a NOR gate that takes inputs from lines A and B. If both A and B are low (0), the output of this NOR gate will be high (1).

Encoding: The combination of the output bits (Y1, Y2, and Y3) represents the encoded binary output based on the active input lines.

If all input lines are low (A = B = C = 0), all output bits will be high (Y1 = Y2 = Y3 = 1), indicating the binary code 111.

If only the first input line (A) is high (A = 1) and the rest are low, the first output bit (Y1) will be low (0), and the other output bits will be high (1), representing the binary code 001.

Similarly, other combinations of active input lines will produce corresponding binary output codes.

3-bit NOR gate-based encoders are straightforward and commonly used in digital systems where simplicity and efficiency are important. They provide a compact and efficient method for encoding multiple inputs into binary format using basic logic gates, making them suitable for various applications such as address encoding, data multiplexing, and control signal generation in digital circuits [7] [8].

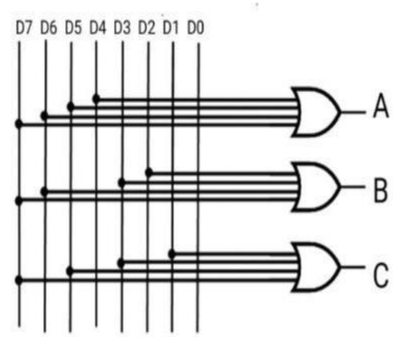

Fig. 5.1 3-bit NOR gate based encoder

5.2.1 MUX-Based Encoders

A MUX (Multiplexer) based encoder is a digital circuit that encodes multiple input lines into a binary code using a multiplexer. Multiplexers are combinational logic circuits that select one of many input lines and direct it to the output based on a set of control signals. MUX-based encoders offer a versatile and efficient method for encoding data into binary format, especially when dealing with a large number of input lines.

Here's a description of how a MUX-based encoder can be designed [11]:

Inputs: The encoder has multiple input lines, denoted as D0, D1, D2, ..., Dn, where n is the number of input lines.

Output Selection: The encoder produces a binary output code corresponding to the active input line.

MUX Configuration: The MUX is configured to have 2^n input lines, where n is the number of bits needed to represent the total number of input lines. For example, if there are 8 input lines (D0 to D7), a 3-to-8 MUX would be used.

Control Signals: The control signals for the MUX are generated based on the binary representation of the active input line. These control signals select the appropriate input line and direct it to the output.

Encoding: The output of the MUX represents the binary code corresponding to the active input line. Each input line is associated with a unique binary code.

For example, if input line D3 is active (high), the binary code 011 (in a 3-bit representation) would be selected by the MUX, indicating that D3 is the active input.

MUX-based encoders offer several advantages:

Flexibility: MUX-based encoders can accommodate varying numbers of input lines by selecting an appropriately sized MUX. This flexibility makes them suitable for applications with a large number of input signals.

Efficiency: By utilizing a single MUX, MUX-based encoders can efficiently encode multiple input lines into a binary output, reducing circuit complexity and component count.

Scalability: As the number of input lines increases, MUX-based encoders can scale easily by using MUXes with a larger number of input lines.

Speed: MUX-based encoders can operate at high speeds, making them suitable for applications requiring fast data encoding and processing.

MUX-based encoders find applications in various digital systems, including address encoding in memory systems, data multiplexing in communication systems, and control signal generation in digital circuits. Their versatility, efficiency, and scalability make them valuable components in digital design [11].

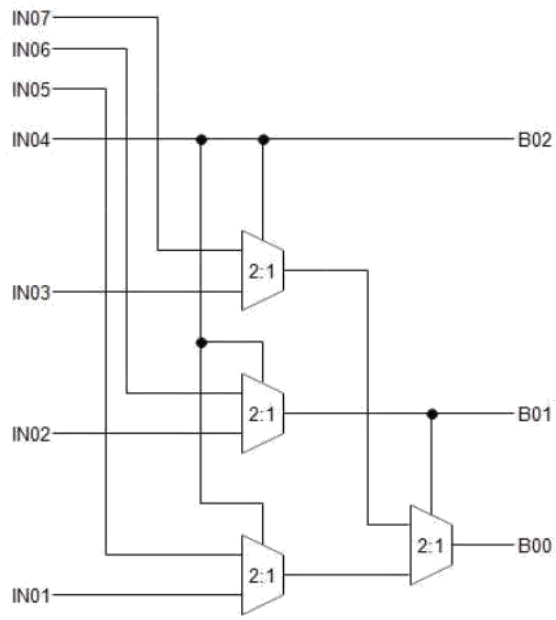

Fig. 5.2 MUX-Based encoder

Chapter 6

Simulation Results

6.1 Comparators

6.1.1 Differential comparator

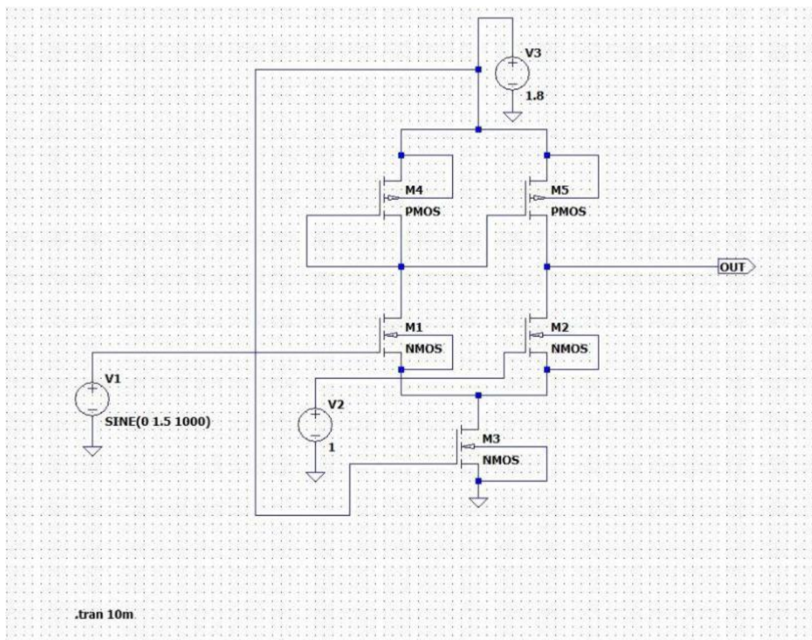

Fig. 6.1 Schematic of Differential comparator

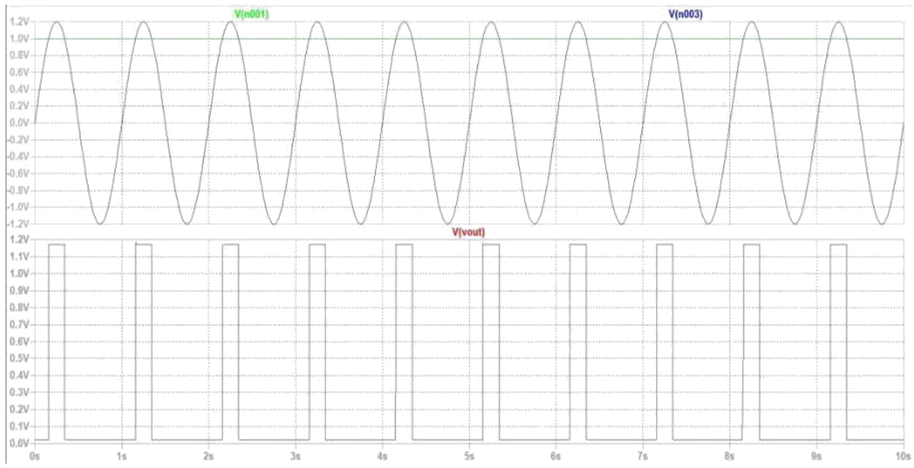

Fig. 6.2 Output waveforms of Differential comparator

6.1.2 Open-Loop comparator

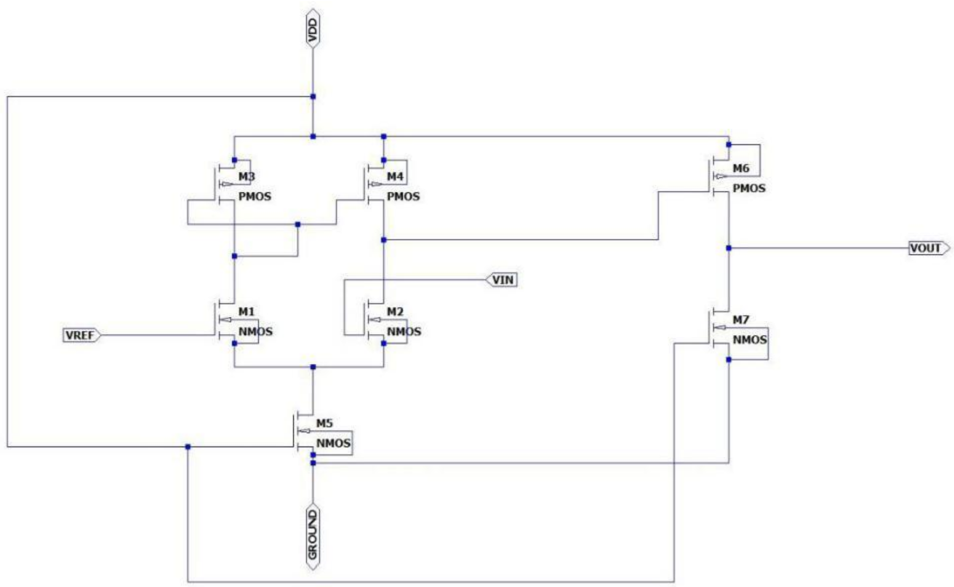

Fig 6.3 Schematic of Open-Loop comparator

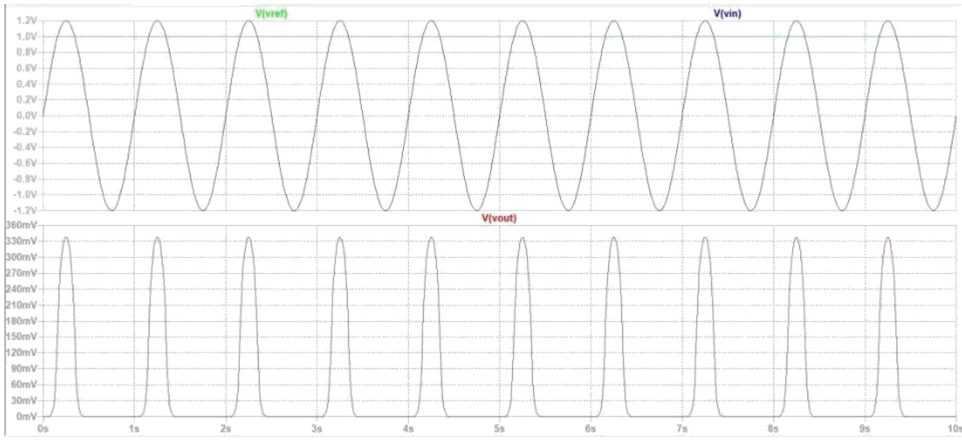

Fig. 6.4 Output waveforms of Open-Loop comparator

6.1.3 TIQ comparator

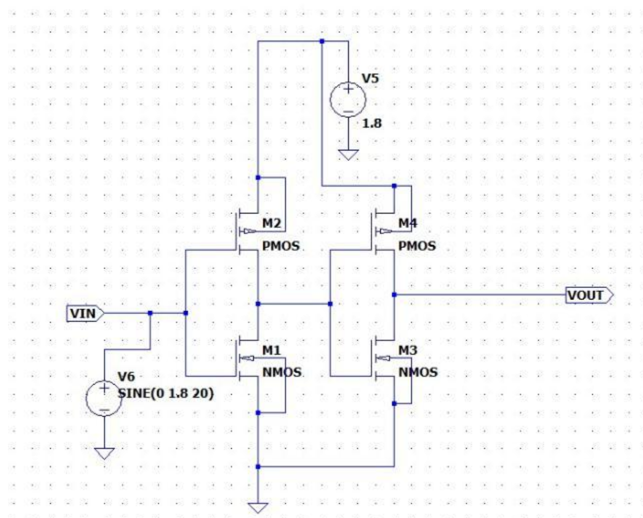

Fig. 6.5 Schematic of TIQ comparator

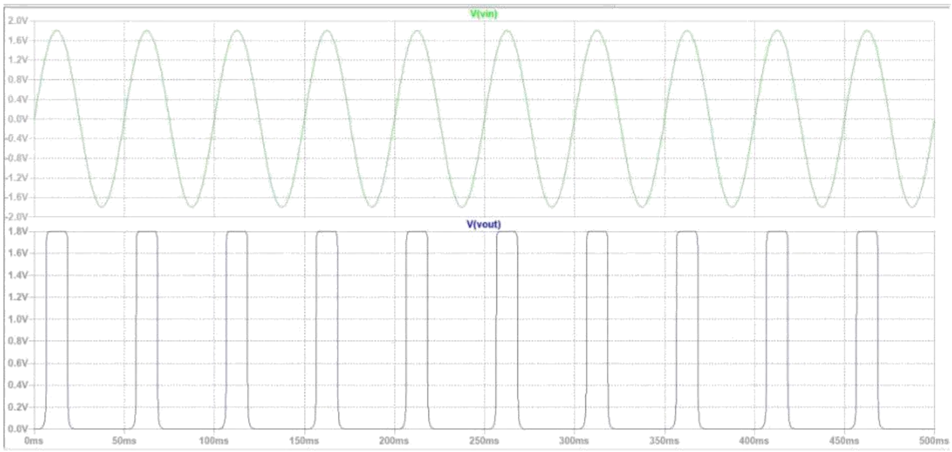

Fig. 6.6 Output waveforms of TIQ comparator

6.2 Flash ADC

6.2.1 Flash ADC using Open-Loop comparator and NOR based encoder

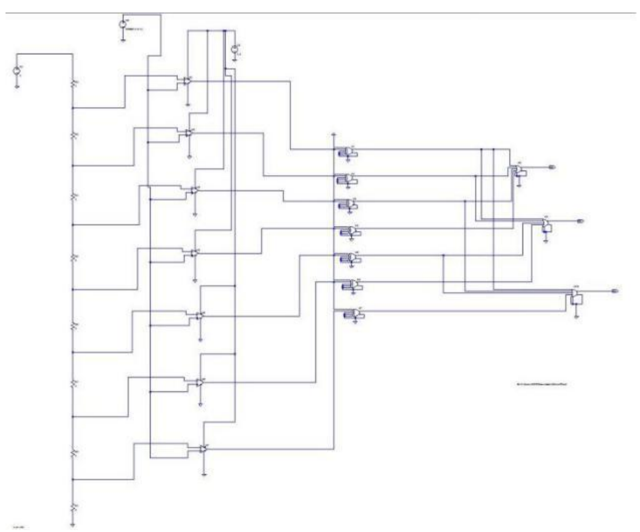

Fig. 6.7 Schematic of Flash ADC using Open-Loop comparator and NOR based encoder

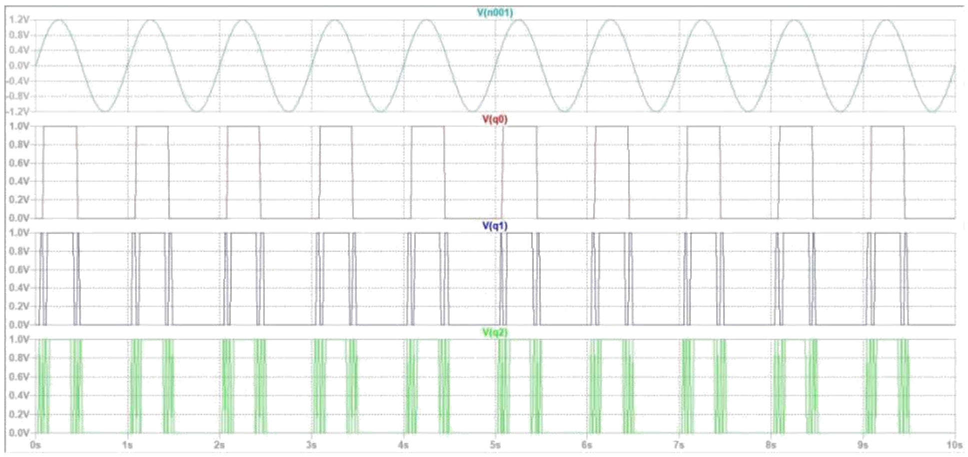

Fig. 6.8 Output waveforms of Flash ADC using Open-Loop comparator and NOR based encoder

6.2.1 Flash ADC using TIQ comparator and MUX based encoder

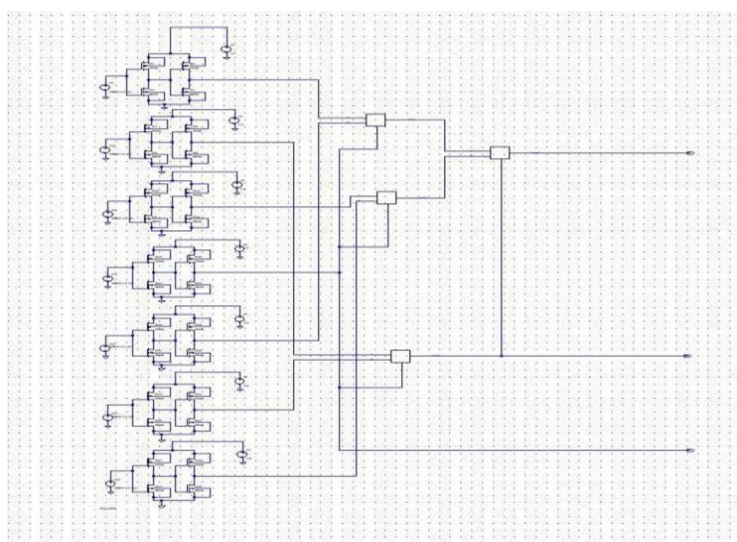

Fig. 6.9 Schematic of Flash ADC using TIQ comparator and MUX based encoder

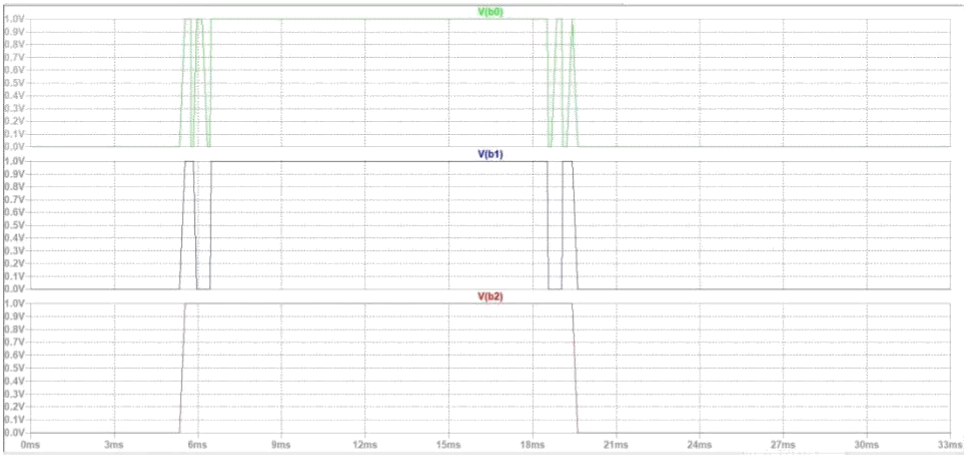

Fig. 6.10 Output waveforms of Flash ADC using TIQ comparator and MUX based encoder

5.3 Power Dissipation

	Differential Comparator	Open-Loop Comparator	TIQ Comparator
NOR based Encoder	**10.06 mW**	**6.67 mW**	**92.6 µW**
MUX based Encoder	**1.61 mW**	**1.04 mW**	**38.4 µW**

Chapter 7

Future work and conclusion

7.1 Future work

Different comparator design can be implemented to make the Flash ADC more power efficient.

Also different encoders can be implemented in such a way that the power consumption can be reduced.

We can use some other circuitry which uses less number of transistors such that less power is consumed by the circuit.

7.2 Conclusion

Different comparators were implemented along with different encoders in the Flash ADC design and the power consumption were observed. The minimum power was observed to be 38.4 µW using TIQ comparator using MUX based encoder.

Chapter 8

References

[1] Chen, C.Y., Le, M.Q. and Kim, K.Y., 2009. A low power 6-bit flash ADC with reference voltage and common-mode calibration. *IEEE Journal of Solid-State Circuits*, *44*(4), pp.1041-1046.

[2] Sireesha, R. and Kumar, A., 2015, May. Design of low power 0.8 V Flash ADC using TIQ in 90nm technology. In 2015 International Conference on Smart Technologies and Management for Computing, Communication, Controls, Energy and Materials (ICSTM) (pp. 406-410). IEEE.

[3] Stojcevski, A., Le, H.P., Singh, J. and Zayegh, A., 2003. Flash ADC architecture. Electronics letters, 39(6), p.1.

[4] Hsuan-Yu Chang and Ching-Yuan Yang, "A Reference Voltage Interpolation-Based Calibration Method for Flash ADCs", IEEE Transactions On Very Large Scale Integration (VLSI) Systems , Volume: 24, Pages:1728 - 1738,Year:2016.

[5] Kar, A., Majumder, A., Mondal, A.J. and Mishra, N., 2015, January. Design of ultra low power flash ADC using TMCC & bit referenced encoder in 180nm technology. In 2015 International Conference on VLSI

Systems, Architecture, Technology and Applications (VLSI-SATA) (pp. 1-6). IEEE.

[5] Xiaochen Yang, Guoping Cui, Yang Zhang, Jiajun Ren, Jin Liu, “A Metastability Error Detection and Reduction Technique for Partially Active Flash ADCs”, IEEE Transactions on Circuits and Systems II, Volume: 63,Pages: 331 - 335,Year:2016.

[6] Yogendra Kumar Upadhyaya, Mohit Kumar Gupta, Mohammad Hasan and Sudhanshu Maheshwari, “High-Density Magnetic Flash ADC Using Domain-Wall Motion and Pre- Charge Sense Amplifiers”, IEEE Transactions on Magnetics, Volume: 52, Article : 4100110 ,Year:2016.

[7] Nazir, L., Khurshid, B. and Mir, R.N., 2015, December. A 7GS/s, 1.2 V. pseudo logic encoder based flash ADC using TIQ technique. In 2015 Annual IEEE India Conference (INDICON) (pp. 1-6). IEEE.

[8] Chia-Chun tsai, kai-wei hong, yuh-Shuyan Hwang. Wen-Ta Lee,Trong-Yen Lee, “New power saving design method for CMOS flash ADC”, in the proceedings of the 47th IEEE international Midwest symposium on circuits and systems, 2004.

[9] C Sander, M.Clara, A.Santner, T.Hartig, F.Kuttner, “A 6bit, 1.2GSps Low-Power Flash-ADC in 0.13um Digital CMOS”, in proceedings of the Design, Automation and Test, pp 1530-1591, 2005.

[10] P.Rajeshwari, R.Ramesh, A.R.Ashwatha, “An approach to design Flash Analog to Digital Converter for High speed and Low power Application”, in international journal of VLSI design and Communication Systems, Vol 03, No.02, April 2012.

[11] Nazir.L, Mir.R.N, Hakeem.N, “A 4 GS/s 1.8 V Multiplexer encoder based Flash ADC using TIQ technique”, In proceedings of International conference on Signal processing and integrated networks, Feb 2014.