B. TECH. PROJECT REPORT

On

Simulation of FET for Nanophotonic devices

BY

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Guided by:

Dr. Mukesh Kumar

DISCIPLINE OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

December 2018

Simulation of FET for Nanophotonic devices

A PROJECT REPORT

Submitted in partial fulfilment of the requirements for the award of the degrees

of
BACHELOR OF TECHNOLOGY
in

ELECTRICAL ENGINEERING

Submitted by:
Amit Kumar Kabat

Guided by:
Dr. Mukesh Kumar

INDIAN INSTITUTE OF TECHNOLOGY INDORE
December 2018

CANDIDATE'S DECLARATION

I hereby declare that the project entitled **"Simulation of FET for Nanophotonic devices"** submitted in partial fulfilment for the award of the degree of Bachelor of Technology in 'Electrical Engineering' completed under the supervision of **Dr. Mukesh Kumar (Associate Professor)** IIT Indore is an authentic work.

Further, I declare that I have not submitted this work for the award of any other degree elsewhere.

AMIT KUMAR KABAT

CERTIFICATE by BTP Guide(s)

It is certified that the above statement made by the students is correct to the best of my knowledge.

Dr. Mukesh Kumar (Associate Professor)

Preface

This project report on “Simulation of FET for nanophotonic devices" is prepared under the guidance of Dr. Mukesh Kumar.

This report is about Integrated CMOS photonics and its applications with MOSFET being the focused device.

I have tried to the best of our abilities and knowledge to explain the content in a lucid manner. I have added figures and experimental results to make it more illustrative.

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Acknowledgements

I wish to thank Dr. Mukesh Kumar for his kind support and valuable guidance. This work has been done in the framework of the IIT Indore project. I would like to acknowledge Sulabh Srivastava, Lalit Jain, Sourabh Jain, Swati Rajput, Surbhi Tidke & Vishal Kaushik for providing their sincere cooperation and guidance to carry out thisresearch.

It is their help and support, due to which I was able to complete the design and technical report. Without their support, this report would not have been possible.

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Abstract

Considering the integration density it is necessary to design smaller On-chip photonic transistor operable for high speed data transfer with minimum loss. In silicon-based photonic circuits, it is possible to combine photonic and electronic components on a single chip to perform multiple functions.CMOS is the building block of many integrated circuits. So combining CMOS with photonic devices is a huge leap in technology. As MOSFET is the primary component of CMOS interface this work deals with the optical analysis of MOSFET. The optical character of mode transition from pure optical mode to plasmonic and then hybrid plasmonic mode is studied by varying the dimensions of Metal-Insulator-Semiconductor (MIS) device structure. The implementation of optical mode character onto the bulk of transistor is observed by varying effective refractive index. The MOSFET electrical characteristics in combination with coupling of optical mode with gate length of 180 nm, 500 nm and 1 um is studied. Later the MRR-loaded MOSFET helps in phase shift by coupling of light and enabling light matter interaction having high propagation distance.

List of Figures

List of Tables

TABLE OF CONTENTS

CHAPTER 1

Integrated Photonics

1.1 Introduction

Integrated photonics brings together multiple photonic components on a single chip to create multipurpose devices. Photonic components are micro to nanoscale devices with some optical functionalities. These devices can be lasers, photodiodes, optical modulators, input couplers, optical waveguides, ring resonator, splitters, gratings, polarizers etc [1]. These components are the building blocks to create devices to perform a wide range of optical functions [2].

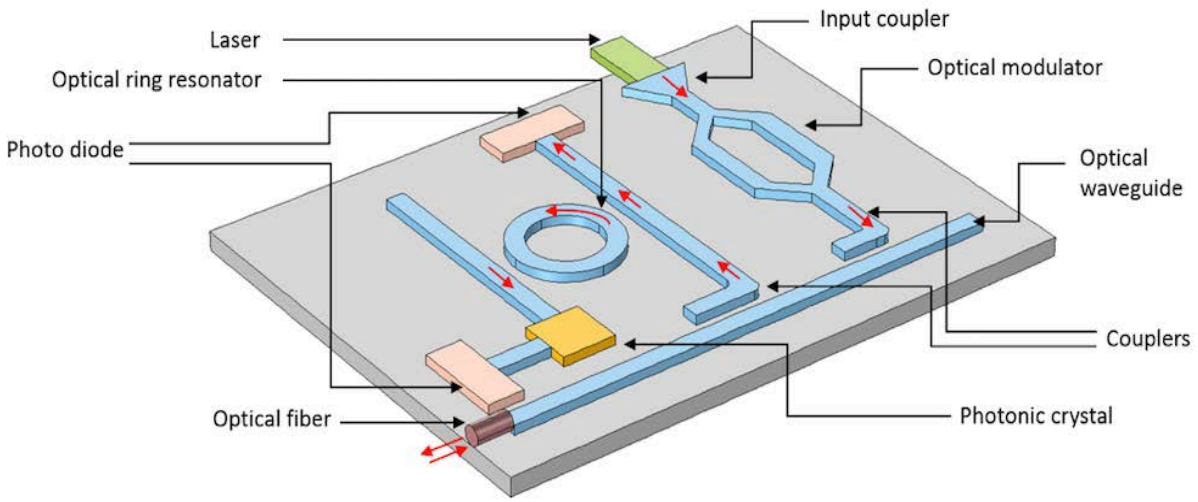


Fig.1.1 Photonics components on a single chip

Source: comsol.com

Photonics basically deals with photons and takes the advantages of particle natures of light. It includes sources of light, guiding medium and then various optoelectronic devices to execute various optical operations [1]. Lasers and LEDs are used as primary sources of light whereas waveguides are used to guide light. Guiding the light has come a long way with optical fibres and revolutionized the way of transferring data. Further development in nanotechnology is helping photonics to manipulate photons on the nanometre scale. Photonics has brought together various branches of science together. Mainly Electrical and Electronics engineering

is now combined with photonics to fabricate new devices and many functions are now possible to be executed on a single chip.

Now even semiconductor physics is combined with photonics to create a new area of science like Silicon photonics. The primary objective is to reduce the manufacturing cost by creating semiconductor and photonic devices on a single chip using techniques like lithography [3]. Optoelectronic devices are now connected using integrated waveguides to make them compact and faster. The pace of manufacturing and developing photonics has increased further with the help of industries and government [4]. Communication using photonic devices has reached a new height. Devices like Dense Wavelength Division Multiplexed (DWDM) [5] has the capability of simultaneously transmitting and receiving ten wavelengths at 10 Gb/s on a DWDM wavelength grid. Similarly, many other devices are improving to raise the data rate further. In wavelength scale more compact devices are being formed using CMOS processing technology with the help of deep UV lithography [6]. Optical fibres and photonic circuits are successfully overcoming the limitations of electronic circuits in case of transferring digital information [7]. New methods in optical communication are using surface plasmonic mode and hybrid mode based circuits to make the photonic devices compatible with nanoscale chips.

1.2 Ring Resonator

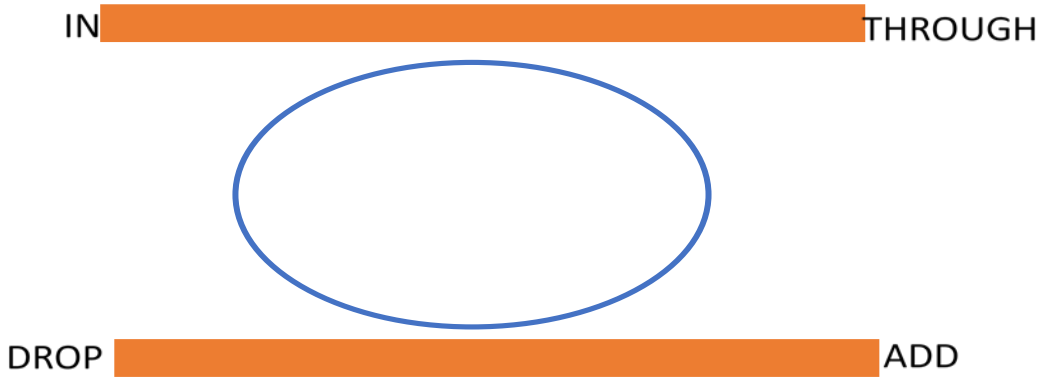


Fig.1.2 Ring resonator

Ring resonator is a photonic device mainly used as a filter as it resonates only a few selected wavelengths entering at its input. Optical ring resonators [8] [9] are promising building

blocks for photonic integrated circuits. Due to the high refractive index contrast, they are used to build very small circuits, specifically in silicon photonics

Fig.1.2 shows the structure of a basic ring resonator. The input received at the IN port is a mixture of a number of wavelengths.The ring and the waveguide are kept close enough to each other so that coupling of light between the waveguide and the ring is possible. The wavelength coupled with the ring is dependent upon the effective index of the ring and its cross-section. The radius of the ring is designed such that light starts resonating at the circumference of the ring. The resonating wavelength is determined by [10]

$$\text{Resonating wavelength} = \frac{n_{eff}L}{M} \qquad \text{eq.(1.1)}$$

Where n_{eff} is the effective index of the ring, 'L' is the optical length of the ring and 'M' is any natural number starting from 1. So the resonant occurs when the optical propagation length around the ring is an integral number of wavelengths. At resonant a strong field builds up in the ring. So some of the wavelengths get coupled with the ring and resonate while others are directed towards the THROUGH port. After completing the ring waveguide path, some light couples and interferes with the incident light. So at resonance, completely destructive interference can be obtained. In that case, there is no transmitted light and the ring resonator becomes a perfect notch filer [11]. From equation 1.1 resonating wavelength of the ring resonator can be altered by changing n_{eff}. Applied voltage changes effective index of a structure, so we will use that property to control the resonating wavelength of the ring resonator.

CHAPTER 2

Integrated CMOS Photonics

2.1 Introduction

Even if the technical barriers increased at each generation, electrical interconnect speed has increased dramatically over the years. The density of components on a single chip is now millions of times as compared to when the first chip was made. As the data rate is scaling upwards rapidly, the electrical signalling over copper cable is starting to show its limitations. Effects like the skin effect and impedance mismatches are affecting more and more as device scale is coming down. This means losses due to attenuation, crosstalk, and signal reflections have been increasing in each new generation.

However, there are different approaches to tackle this situation, one of such approaches is integrated CMOS photonics which primarily focuses on providing optical solutions with a direct interface to CMOS chips [12]. In CMOS both n-type and p-type transistors are used to build logic gates. The main advantage of CMOS technology is that it has high speed, high noise margin and it dissipates low power. It will help to take full advantage of photons while overcoming the limitations of electrons. Integrating CMOS technology with photonics devices will result in Manufacturing optical and electrical circuits monolithically using lithography and other ongoing processes same as electronic circuits.[13]

In the field of data communication Silicon photonics is anticipated to be a huge branch as optical communication will take over the field. From intra-chip interconnects to supercomputers, it has widespread applications in every field. In addition to that it has helped in miniaturization of integrated circuits and forming multifunctional devices. In future, integrated CMOS photonics can bring electronic and photonic components together to form faster and more efficient chips than ever. Guiding and controlling light through optical fibres, enabling single-chip trans-receiver will fill the lack of high-speed devices on wavelength standards. Increasing conventional packing density of waveguides and electronic chips will enable a faster communication system.

2.2 CMOS Integrated Ring Resonator

Integrating CMOS with photonic devices has increased dramatically over the years. Many photonic devices are manufactured monolithically with CMOS devices to reduce manufacturing cost and to create multipurpose devices. As Ring resonator is the photonic device we desire to integrate with MOSFET, we will review some of the earlier works related to the integration of CMOS devices with a ring resonator.

Ring resonator basically works as a filter for optical inputs. In [14] ring resonator is combined with two CMOS cross-coupled pairs symmetrically to create a dual-mode active bandpass filter (BPF). Dual mode filter has narrowband and high -selectivity characteristics. Integrating the resonator with CMOS enhances the quality factor and also reduces the size efficiently.In [15] ring resonator is combined with silicon photonics to describe intermodel coupling. Basically ring resonator is coupled with waveguides with CMOS interface. Also the work in [16] uses ring resonator to realize the priority encoder where 4-bit input electrical signal is encoded to a 2-bit optical signal.

Still using ring resonator with CMOS interface is new. Changing the resonating wavelength of ring resonator by applying voltage where MOSFET is part of the ring resonator has never been tried before. There are instances where the resonating wavelength of the ring resonator is changed by varying the optical window, but MOSFET and a ring resonator as a monolithic device is new as per our knowledge.

2.3 Objective and Motivation behind the project

The demand for high-speed devices in compact form is neverending. But maintaining the compactness as well as evolving the technology for better-performing devices is a challenge. In many areas light has already been proven to be the ultimate solution. Communication systems took a massive leap with optical fibre. Suddenly data transfer rate reached sky high. Even in microelectronic circuits are manufactured using lithography [17]. Lasers, optical modulators, resonators etc. are some of the most efficient devices because of the fact that they

operate on the light. The next big step would be to make an entire circuit using only photonic devices. It will make the device extremely efficient, and it will function in the fastest way possible. Already there is progress in optoelectronic circuits to combine electronic circuits with photonic devices. But there is a long way to go. Challenge is that the nanoscale is considered between 1 to 100 nanometers. On the other hand light waves have wavelengths in microns range. So to interact with nanoscale devices which are present today integrated photonics still needs improvement. That's the reason in the nanoscale level there are not many fast-performing devices. But rigorous research and inventions are going on to fill that gap pretty soon. The motivation behind this project was to contribute towards that goal and bring electronic and photonic circuits on a single chip by using photons as the primary mode of interaction between matters and devices.

Optical interconnection [18] is the solution to manufacture the fastest and most efficient integrated circuits possible. There are instances of hybrid electrical-optical interconnection for electronic devices [19]. In this project, we are trying to optically couple the MOSFET and the ring resonator so that they can be a part of an integrated circuit which can perform both electrical and optical operations. As mentioned in section 1..2 there is a scope to change the resonance wavelength of the ring resonator by changing its refractive index. If we consider changing the refractive index of Silicon which is the primary material of the ring resonator, we will have to apply an extremely high voltage which is not suitable for nanoscale devices. But the refractive index of Silicon can also be changed by doping. So we will try to apply both voltage and high doping on Silicon to observe the change. In addition to that as Silicon is the substrate of MOSFET , it can replace the ring part of the resonator. It will give us two devices on a single platform. We can make the device monolithically which will reduce the manufacturing cost.

By applying voltage on a heavily doped MOSFET, we will be able to change the effective index of the structure and therefore change the resonance wavelength of the ring resonator. If the change in effective index observed comes significantly high, it could even be used as an optical modulator. MOSFET can perform normal electrical operations by carrying current from source to drain while being a part of the ring resonator. To be able to select the resonating wavelength just by the applied voltage will make it a perfect device to form a filter circuit.

CHAPTER 3

Analysis of MOSFET for Optoelectronic devices

3.1 Proposed Device design

The primary objective to combine MOSFET and ring resonator monolithically to form a device which can be part of a circuit performing both electrical and optical operations. The process follows the analysis of electrical and optical properties of MOSFET so that it can fit into the ring resonator and react to the optical input. We will analyse the Metal-Insulator-Semiconductor (MIS) structure to observe and understand the mode pattern in response to the variation of the oxide layer thickness. As the effective index is the most dominant optical property of a structure, we will see its variation corresponding to drain voltage and drain doping at different dimensions, so that we can design the optimum MOSFET for the ring resonator. During all these analyses optical input of 1550 nm is provided to the substrate of the MOSFET.

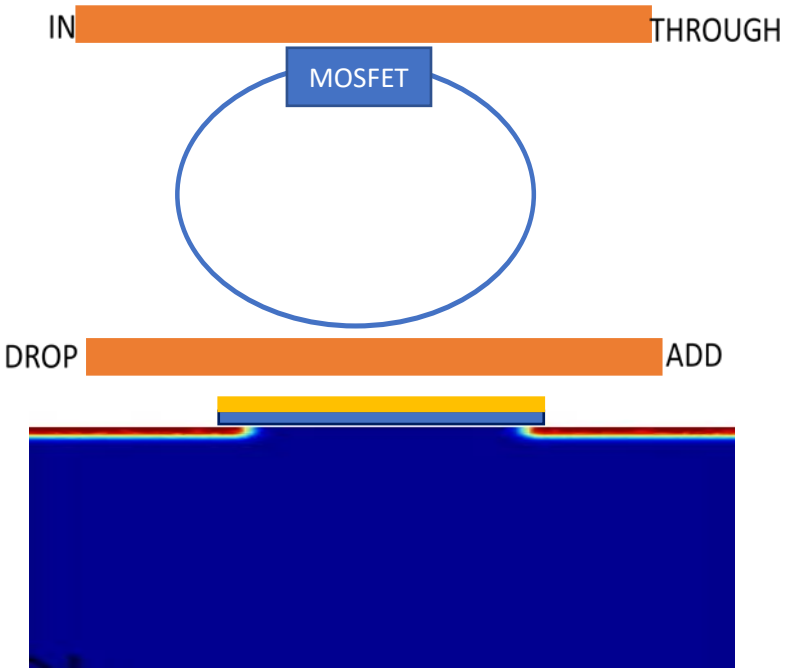


Fig. 2.1 Design of the device

In the proposed design as shown in fig.2.1 the MOSFET is situated in the ring part of the device.

There were two options ; either put the MOSFET at a distance from ring resonator or make it a part of the ring resonator. Keeping the MOSFET at a distance would have given the opportunity to change the phase of the input light. However, the motive is to change the resonance wavelength of the ring resonator by changing the effective index of MOSFET. Change in the phase of the input has no effect on the resonance wavelength of the ring resonator. In addition, the ring resonator is made entirely of Silicon, so making MOSFET a part of it is easier, and it will lower the manufacturing cost.

In integrated photonic circuits Silicon-On-Insulator (SOI) [20] is used a lot. But to be able to generalize the device, a more common device among electronic circuits like MOSFET is best suited due to its wide range of usage and simplicity. To produce optimum coupling between MOSFET and ring resonator, and maximum change in effective index we will analyse the optical response of MOSFET.This will help us to understand conditions at which optical behaviour of the MOSFET matches that of the ring resonator.

3.2 Analysis of Metal-Insulator-Semiconductor (MIS) structure

MOSFET is also an MIS type structure if we neglect minor irregularities. Analysing an MIS structure will help us to understand different mode patterns and will give an idea about the desired thickness of the oxide layer for the MOSEFT meant for ring resonator. The mode is basically a single path or way the light can propagate through the structure. There can be many modes for a single input. For analysis purpose, we are considering only optical mode as it is considered the most fundamental mode in rectangular waveguides and other optical communication methods.

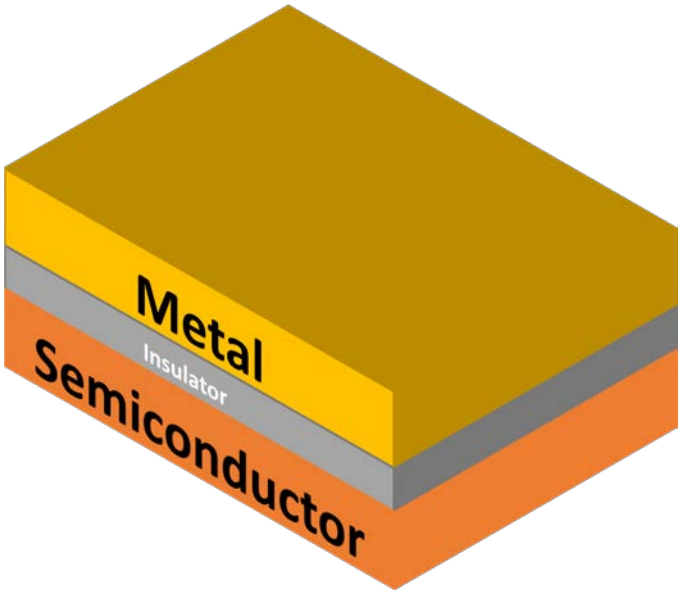


Fig.3.1: Metal Insulator Semiconductor (MIS) structure

Fig.3.1 shows the Metal-Insulator-Semiconductor (MIS) structure. In the structure Gold (Au) is used as the metal layer. In MOSFETs also Gold (Au) is used for metal contacts due to its malleable nature which makes it easier to apply the thin coating onto the surface. In addition to that, it has good resistance against wear and tear which lengthens the contacts' lifespan. Similarly, SiO_2 is used in the insulation layer similar to that of MOSFET. It's a good dielectric material and provides good isolation. The primary reason to use SiO_2 is that only oxidation of Si layer is needed to produce SiO_2.

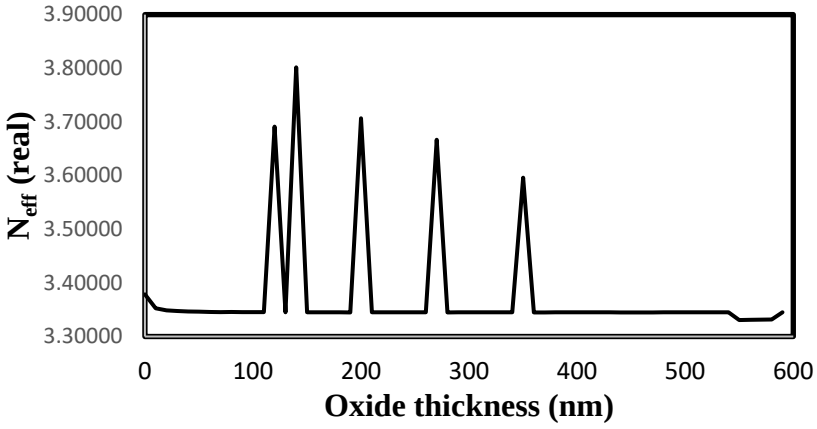


Fig.3.2: Effective index (real) vs Oxide thickness

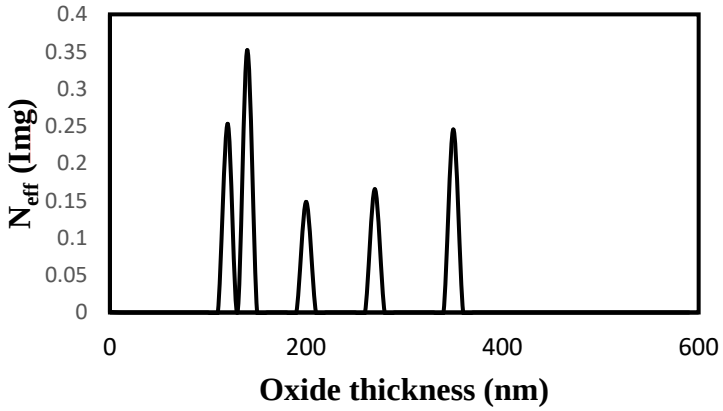
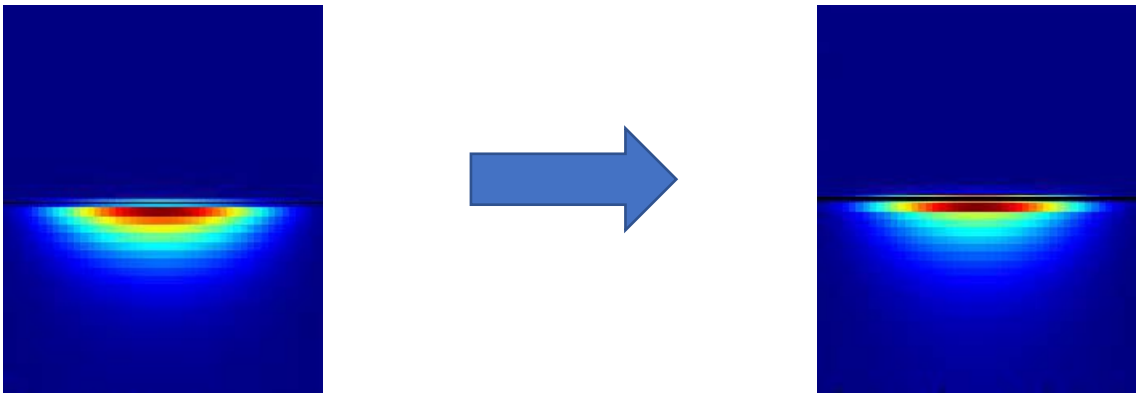


Fig.3.3: Effective index (real) vs Oxide thickness

The thickness of the oxide layer (SiO_2) varied from 0 to 600 nm, and the effective index (real and imaginary) observed for the same in fig.3.2 and fig.3.3.

Different modes are observed for the variation of the thickness of oxide which correlates to the plot of effective index.Initially, when there is no Oxide layer, surface plasmonic mode or surface mode is visible at the interface between metal (Au) and semiconductor (Si). When Oxide thickness is increased to 5 nm Hybrid plasmonic mode appears as light can be seen inside the Oxide layer. The further increment of layer thickness shows that mode pattern is



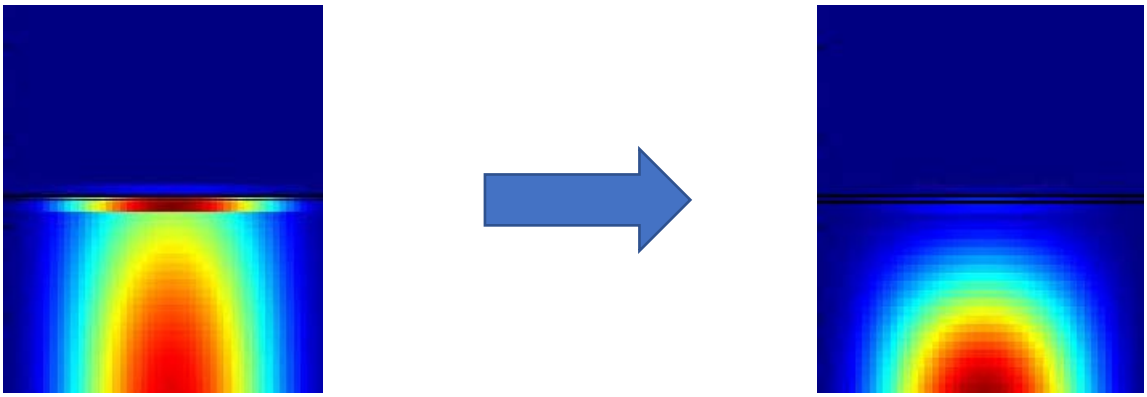
a: surface plasmonic mode

t_{ox} = 0 nm

b: Hybrid Plasmonic mode

t_{ox} = 5 nm

gradually shifting towards the Si region giving a leaky Hybrid plasmonic mode at 10 nm and optical mode at 20 nm.

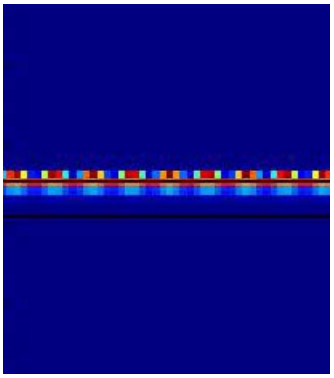


c: Leaky Hybrid plasmonic mode
t_{ox} = 10 nm

d: Optical mode
t_{ox} = 20 nm

Fig.3.4 (a,b,c,d): Transition of modes as per Oxide thickness

Fig.3.4 (a,b,c,d) shows a gradual change of the mode structure for the variation of Oxide thickness. After shifting to the Silicon region, the mode stays optical irrespective of oxide layer thickness, but at certain points, the mode is lost completely. The imaginary part of the effective index corresponds to the loss associated with the propagating wave, so the spikes at certain points justify the sudden loss of modes in the structure.



e: No significant mode
t_{ox} = 130 nm

Fig.3.5: No significant mode for 130 nm Oxide thickness

Fig.3.5 shows the condition when no mode is visible at 130 nm oxide thickness. This condition can be found in other higher oxide thickness as well. Although there is no direct relation between the thickness of the Oxide layer and effective index of the structure, the sudden change in the effective index is used to shift the resonance wavelength of the ring resonator where the insulator may be air or any other material [21].

3.3 Electrical and optical analysis of MOSFET

MetaL-Oxide-Semiconductor-Field Effect Transistor (MOSFET) is the most common type of transistor used in everyday circuits. It is used in almost all types of electronic circuits. MOSFET is a voltage controlled device and mostly used for amplification purpose. The main advantage of this device is the availability of a gate electrode which is electrically insulated from the main semiconductor. Channel is basically the path between two highly doped regions. Depending upon the doping MOSFET is named as n-type or p-type. Applying gate voltage causes inversion in the channel region and creates a path to allow the flow of current in the circuit. Due to the presence of insulation of gate and channel MOSFET is able to control the flow of current and hence can act as a controlled switch in many circuits. Basically we are able to control MOSFET parameters [22]. MOSFET can be treated as a voltage controlled resistor as the current flowing through the channel is directly proportional to the applied gate voltage. This behaviour is efficiently used in power converter circuits to reduce loss and fluent conversion [23]. CMOS logic gate technology uses the opposite switching property of both p-type and n-type MOSFET, hence named as complementary metal-oxide-semiconductor (CMOS).

MOSFET can be further classified into two types depending upon its switching property. Depletion type MOSFETs require gate voltage to switch OFF mode while enhancement type MOSFETs require gate voltage to switch to ON mode. Depletion type MOSFET [24] is called as “Normally Closed” switch and Enhancement type MOSFET is called as “Normally Open” switch. Depletion type MOSFET has some unique characteristics similar to that of Junction Field Effect Transistor (JFET) and triode and is used in special cases, but in general, a device which is normally closed (ON) is rarely used in everyday circuits. On other hand enhancement

type MOSFET is used vastly as it blocks the flow of current and only by applying voltage it switches to ON stage.

The dimensions of MOSFET and ring resonator should be same in order to form a monolithic device, so electrical and optical characteristics of MOSFETs are analysed at three different dimensions. Each MOSFET is an n-type enhancement MOSFET having both source and drain doping of 2e20 cm^{-3}. The metal contacts used to apply voltage are that of gold(Au). The Oxide layer used is of SiO_2. The 2-D view of MOSFET is shown in below figure.

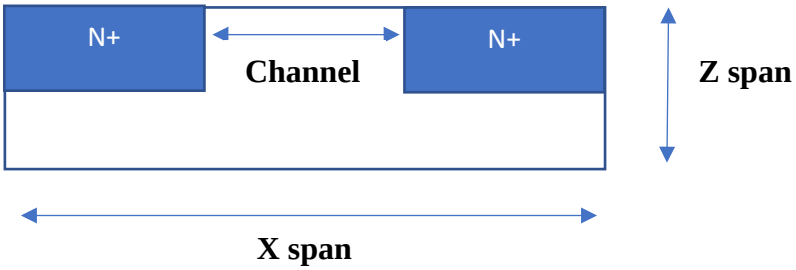
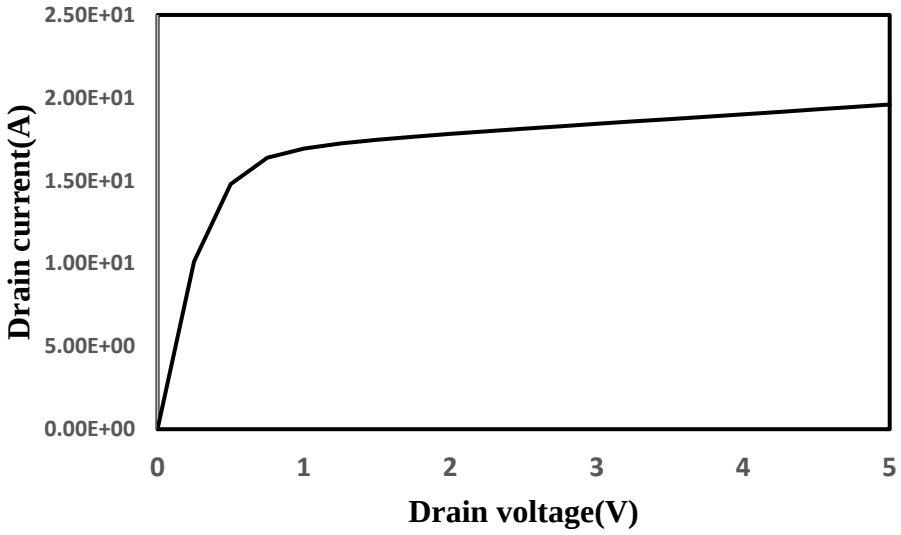


Fig.4.1: 2-D MOSFET

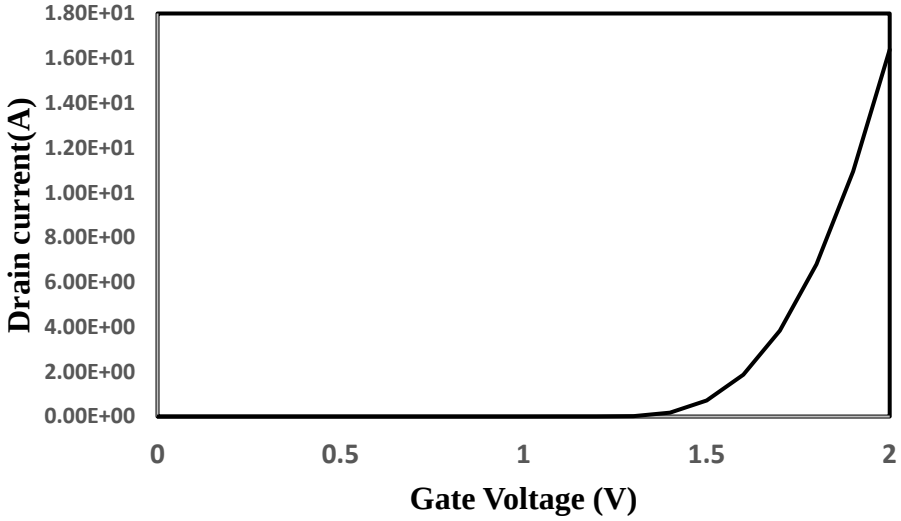
As shown in the fig.4.1 X span is the overall length of the MOSFET, Z span is the height of the MOSFET and Y represents the channel width of the MOSFET. The dimensions of all 3 MOSFETs are shown in below table.

Channel length	X span	Y span	Z span
180 nm	600 nm	650 nm	300 nm
500 nm	1000 nm	1500 nm	700 nm
1000 nm	4000 nm	5000 nm	2500 nm

Table 4.1: MOSFET dimensions



a: Output characteristic



b: Transfer characteristic

Fig.4.2 (a,b): Characteristic curves of 180 nm MOSFET

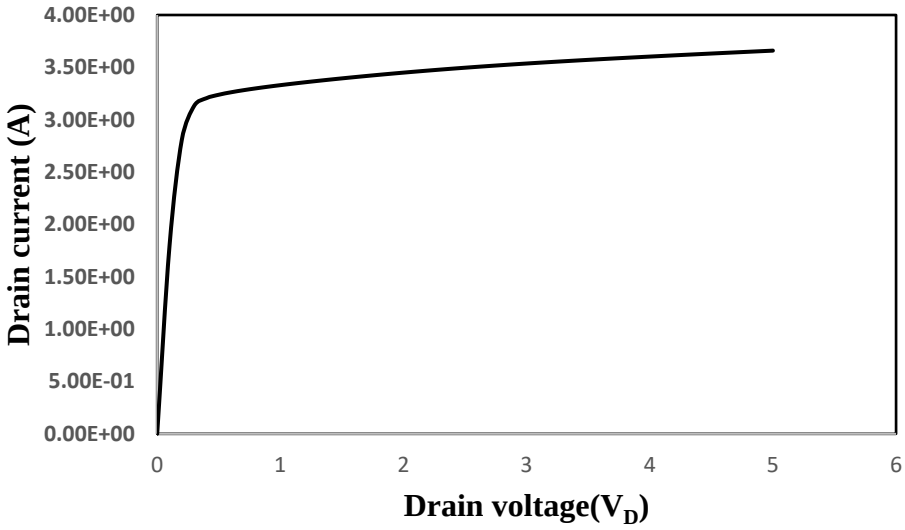
Table 4.1 shows the dimensions of all the MOSFETs used for analysis purpose. In general channel width / channel length ratio is kept above 2.5 performance purpose. We have kept the ratio 3 or above 3 in all cases. In case of 1 µm MOSFET, we kept it 5000 nm as the MOSFET is too large compared to the other two. We used LUMERICAL DEVICE tool to analyze the electrical characteristics of the MOSFETs.

Fig.4.2 shows the characteristic curves of 180 nm MOSFET. The plot between Drain current (I_D) and Drain voltage(V_D) is called as the output characteristic of the MOSFET as it shows the output current with respect to the drain voltage(V_D) which controls the amount of current through MOSFET.As shown in figure 4.2(a) the curve follows a linear pattern till some voltage, then it saturates. The region where current is almost is called the saturation region. Saturation occurs when the channel pinches off. In channel region there are two electric fields acting together, the gate to source voltage(V_{GS}) and drain to source voltage(V_{DS}). As the drain voltage (V_D) increases the minimum voltage required to form the inversion layer in the drain side is not present. In saturation $V_{GS} \geq Vt$ and $V_{DS} \geq (V_{GS}-Vt)$. The Voltage at the Drain end is $V_{GD} = V_{GS}-V_{DS}$, and this voltage $V_{GD} \leq Vt$. So the channel pinches off as we move from Source end where Voltage is $V_{GS} \geq Vt$ towards the Drain end where we have $V_{GD} \leq Vt$. The number of electrons decreases due to this, but the velocity increases significantly. So the current saturates in case of long channel MOSFET and very slowly increases in short channel MOSFET. The linear region is called the Ohmic region as it resembles the V-I curve for ohmic conductors. This is the region where most of the circuits operate as there is no point to move to the saturation region and waste energy The region of no current when no sufficient Gate voltage (V_G) is applied is called the Cut-Off region. The Drain voltage(V_D) at which Drain current(I_D) saturates is called the saturation voltage for the MOSFET. The saturation voltage also depends upon the applied Gate voltage (V_G). For different Gate voltage (V_G), the saturation voltage changes. If a higher Gate voltage (V_G) is applied the curve shift upwards to give higher current for the same Drain voltage. If drain voltage (V_D) is increased even after saturation the MOSFET breaks down and the current suddenly rises to a very high value. So very high heat is generated and MOSFET blows up. This voltage is called the breakdown voltage.

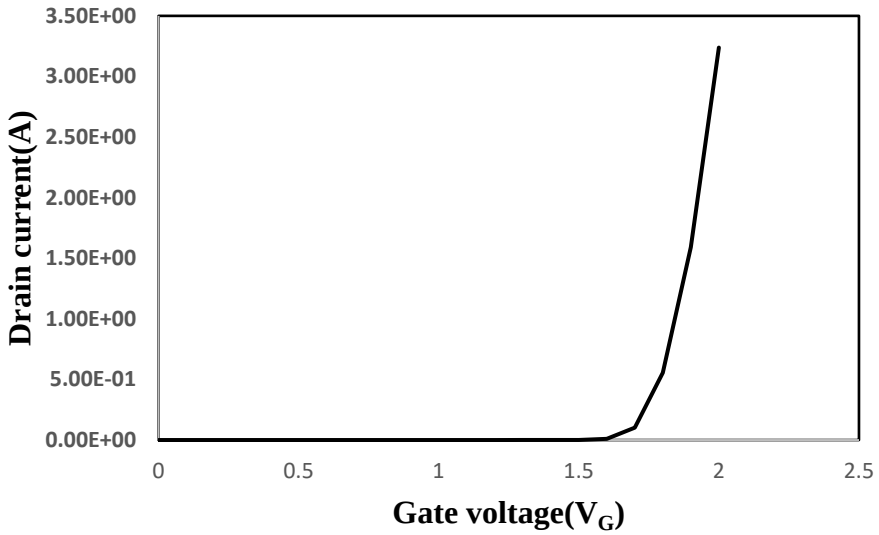
Similarly, if we observe figure.4.2(b) the drain current is zero up to certain Gate voltage (V_G) and then increases exponentially. The region where there is no current is known as Cut-Off region. In this region, the channel is not formed yet so no current can flow. The Gate voltage (V_G) at which the MOSFET starts conducting is known as the Threshold voltage [25]. This plot between Drain current (I_D) and gate voltage (V_G) is called as the Transfer characteristics. The drain voltage is kept constant in this case. If Drain voltage (V_D) is increased the curve shifts leftward to give a higher value of current.

From the plots, for 180 nm MOSFET saturated drain current (I_d) is almost 17.5 A, the saturation drain voltage (V_D) is 5 V. From the I_d -V_g curve threshold voltage obtained is 1.25

V. The constant Gate voltage (V_G) is kept at 2 V for Output characteristic while Drain voltage (V_D) is kept constant at 0.75V for Transfer characteristic.



a: Output characteristic

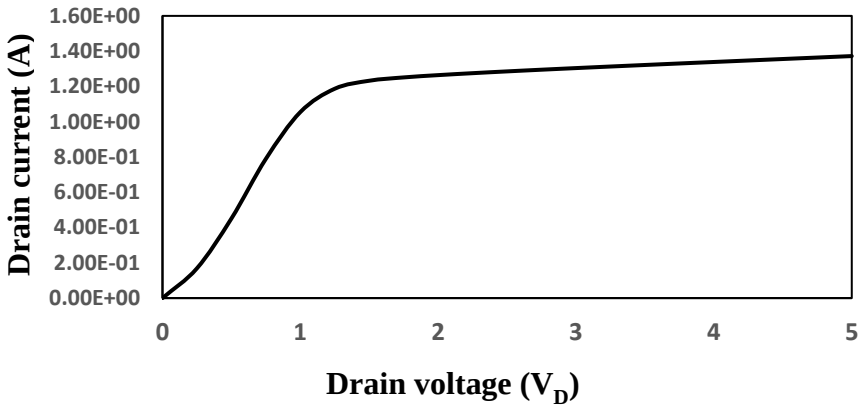


b: Transfer characteristic

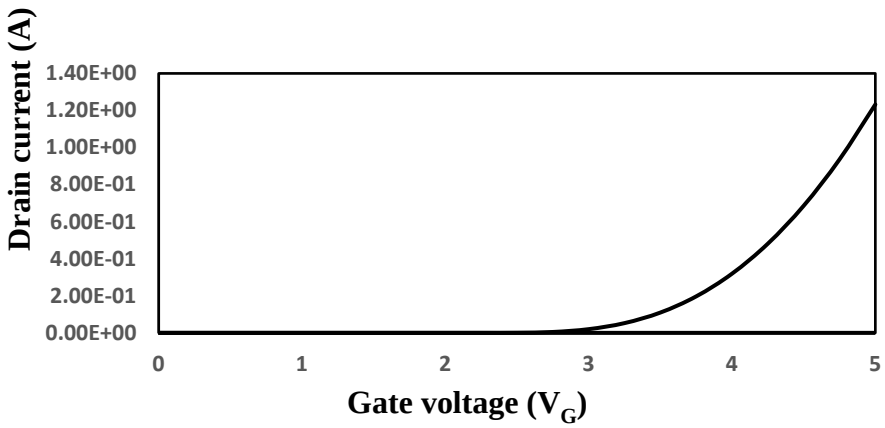
Fig.4.3 (a,b) : Characteristic curves of 500 nm MOSFET

Fig.4.3 (a,b) shows the characteristic curves of 500 nm MOSFET. From the plots saturated drain current (I_d) is 3.5 A, saturation drain voltage (V_D) is 4 V. From the I_d -V_g curve threshold

voltage obtained is 1.5 V. Gate voltage (V_G) is kept constant at 2 V, and V_D is kept at 0.5 V for Output and Transfer characteristic curves respectively.



a: Output characteristic



b: Transfer characteristic

Fig.4.4 (a,b): Characteristic curves of 1 µm MOSFET

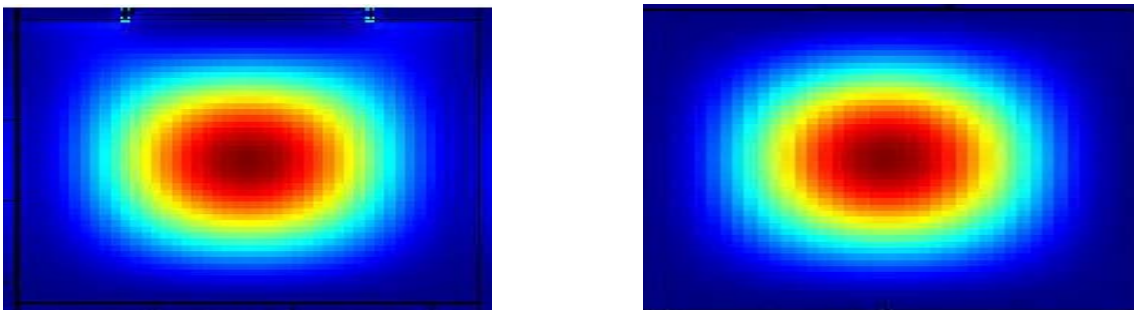
Fig.4.4 shows the characteristic curves of 1 µm MOSFET. From the plots saturated drain current (I_d) is 1.4 A, saturation drain voltage (V_D) is 3 V. From the I_d -V_g curve threshold voltage obtained is 3 V. Gate voltage (V_G) is kept constant at 2 V, and V_D is kept at 2 V for Output and Transfer characteristic curves respectively.

As per the obtained results, by comparing at a constant Drain voltage(V_D), it can be concluded that drain current(I_d) increases as the dimension of MOSFETs decreases. Having shorter

channel lengths for a particular drain voltage(V_d) helps electrons to cover shorter length, and it increases current. Similarly, the threshold voltage decreases with decreasing channel length of the MOSFET as less voltage is required to form a channel in small devices. MOSFET current also depends upon doping. Higher doping concentrations mean a high number of charge carriers and higher current.

Optical input of 1550 nm is fed to the substrate(Si) of the MOSFET, and optical modes are fetched in all cases. The reason to use 1550 nm is due to its dominance in optical communication systems; primarily in waveguides where SiO_2 is the medium of propagation and the loss is extremely low [26]. In Si also loss through the medium decreases with increasing wavelength. Also using the same wavelength as other photonic devices makes the proposed device more compatible in an integrated circuit.

LUMERICAL device is only capable of giving electrical characteristics, so to calculate the optical modes np density which stores the electrons distribution as per voltage variation is exported to LUMERICAL mode solutions.



a: 500 nm MOSFET **b: 1 µm MOSFET**

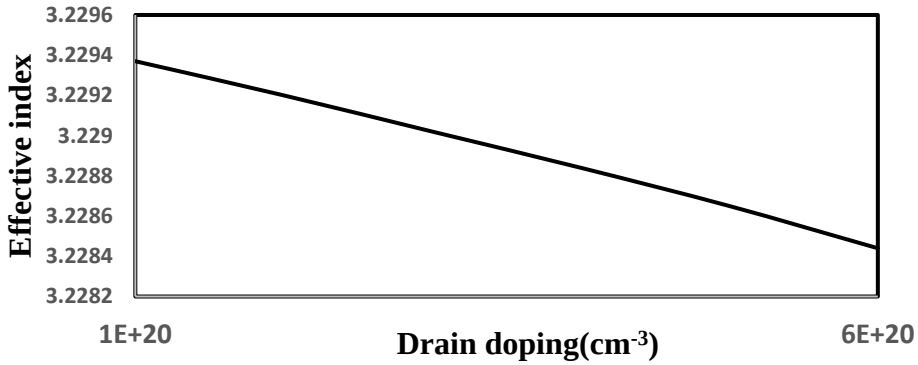
Fig.4.5: Optical modes in MOSFETs

Fig.4.4 (a,b) show optical modes in 500 nm MOSFET and 1 µm MOSFET respectively. However, for MOSFET having a channel length of 180 nm, the width of the MOSFET is only 500 nm. As the dimension of the smallest MOSFET is less than half of the input wavelength optical mode is not feasible. The reason is optical mode which is TE_{10} mode is feasible only when the broader side of the rectangular waveguide is at least half of the wavelength. Here silicon substrate is treated as a rectangular waveguide, hence no optical mode for below half

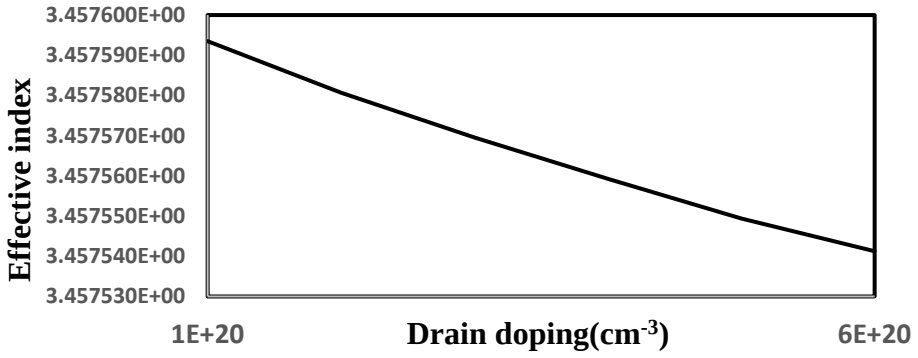
wavelength. This is the main disadvantage of the optical mode as it restricts the evolution towards smaller on-chip devices.

3.4 Results and Analysis

With 1550 nm optical mode as the input to the substrate of the MOSFET variation in the effective index (real) of MOSFET is shown in below figures corresponding to the sweep of drain voltage and drain doping. The voltage sweep is done at constant doping of 2e20 cm^{-3} for both source and drain. Similarly, during the sweep of doping drain voltage (V_d) and gate voltage(V_g) is kept constant. The constant V_d and V_g are determined from the characteristic curves of each MOSFET. V_d being the saturation voltage and V_g being the breaking point or extreme point from the I_d-V_g curve.



a. 500 nm MOSFET



b. 1 µm MOSFET

Fig.5.1 Effective index(real) vs drain doping of MOSFETs

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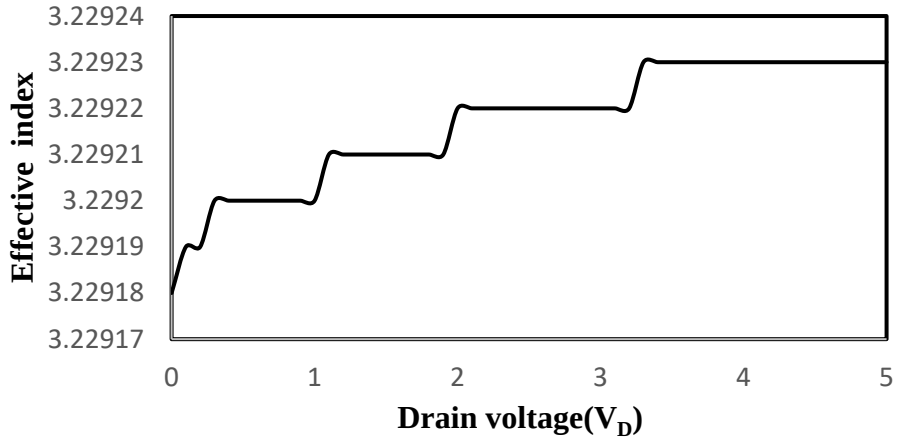
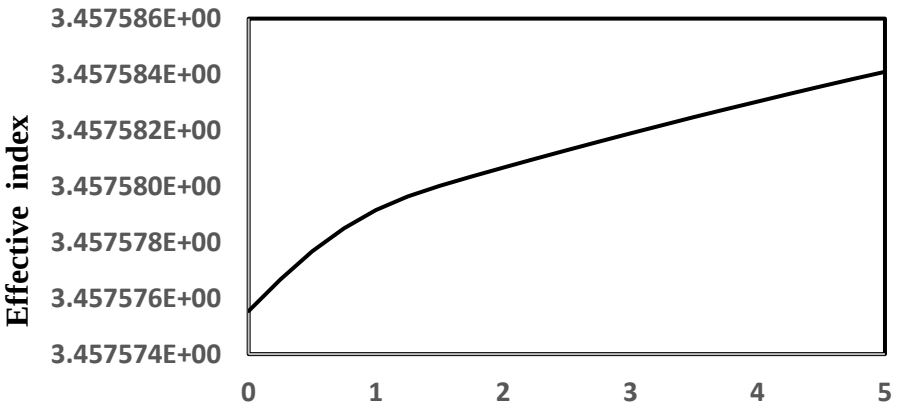


a. 500 nm MOSFET



b. 1 µm MOSFET

Fig.5.2(a,b) Effective index(real) vs drain voltage of MOSFETs

Fig.5.1 a and b show the variation of the effective index (real) with respect to drain voltage of 500 nm MOSFET and 1µm MOSFET respectively. There are numerous references to the effects of doping on the optical properties of Si. But the obtained results are compared to Soref and Bennet model which describes the electrooptic effect of silicon(Si). Most of MOSFET is silicon so comparing its behaviour to a model of pure silicon can give a fair idea about its nature. Soref considered three carrier effects to conclude his analysis. The effects are traditional free carrier absorption, Burstein-Moss band filling and Coulombic interaction of carriers with

impurities. These act simultaneously. For the effect of the electric field, he primarily considered the electro-absorption at the indirect band gap of Si (E_g). He concluded that the refractive index would increase when carriers are depleted from doped material; conversely, the index will decrease when carriers are injected [27].

The observed plots follow the similar trend as per the Soref model [27]. From the plot 5.2(a) Δn_{eff} of 7e-5 for 500 nm channel length MOSFET with 5 volts sweep is better compared to 1.3e-5 Δn_{eff} of Soref model with 10e5 V/cm applied field on pure silicon. The changes observed in 500nm MOSFET (7e-5) is higher than that of 1µm MOSFET(1.2e-5). If we compare our plot to that of Pockel and Kerr effect, then the trend is same ,but Kerr effect shows more linearity in its variation as compared to the results obtained from our proposed device.

Reason to focus more on Δn_{eff} is due to the fact that the resonating wavelength of ring resonator depends on the effective index of the ring, so larger the change in effective index (Δn_{eff}) larger will be the range of wavelengths to be resonated. Another reason is its use in optical phase modulation [28] where

$$\Delta\phi = \frac{2\pi \Delta n_{eff}}{\lambda} L \qquad \text{Eq. 5.1}$$

The final MOSFET designed is of 800 nm having a channel length of 300 nm due to dimension constraint of the optical mode.It is difficult to maintain the long channel MOSFET property in a smaller MOSFET [29]. The Z span (height) of the MOSFET is kept 1500 nm while the channel width is kept 700 nm. As higher current shows a better change in effective index, we used the Newton solver method instead of Gummel model to solve for current in LUMERICAL device. Although it results in less saturation of the MOSFET the purpose of higher n_{eff} is served. Higher the n_{eff} higher will be the range of wavelengths available to resonate for the ring resonator.

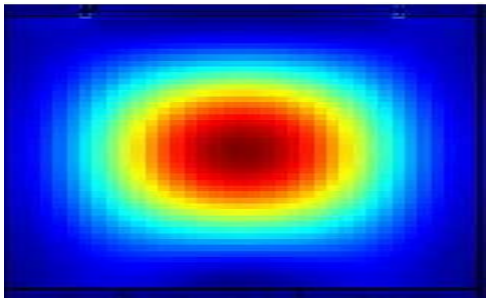


Fig.5.3

optical mode (800 nm MOSFET)

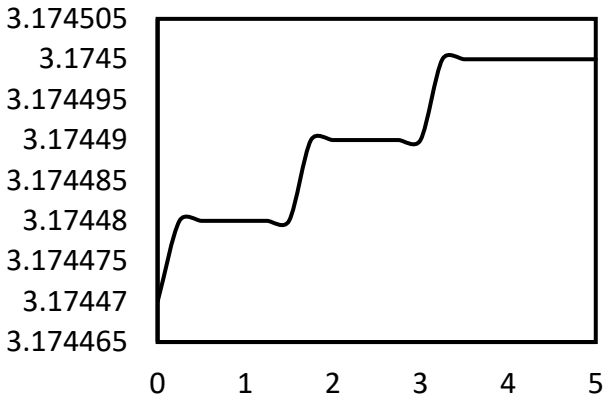


Fig.5.4

effective index vs drain voltage (800 nm MOSFET)

The optical mode is shown in fig.5.3. Effective index variation is shown in fig.5.4. It showed Δn_{eff} of 3e-5. The change is quite low compared to the requirement of the ring resonator to shift the resonating wavelength. Its even lower than the 500 nm channel length MOSFET. So it can be further optimised to get a better result using the consclusions derived from the project.

CHAPTER 4

Conclusions and Future scope

From the analysis, it can be concluded that effective index decreases when carriers are injected; conversely, increases when carriers are depleted from the doped material . The voltage sweep in the 500 nm MOSFET gave higher Δn_{eff} than pure silicon with 10e5/cm applied field. As only difference was doping, it can be concluded that doping improves the Δn_{eff}.
Also higher doping results in a lower effective index which means higher propagation speed. So overall high doping concentration is preferable. The smaller MOSFET showed better Δn_{eff} compared to the larger one, so the dimension of MOSFET should be as low as possible to get the optimum result. In that regard, the choice of 800 nm MOSFET for the final MOSFET satifies the condition to get optical mode and also can provide a better result. From the MIS mode pattern, we observed that hybrid mode was seen in between surface plasmonic mode and hybrid mode. It justifies the fact that hybrid mode is the coupling of surface plasmonic mode and optical mode .

The optical mode has been used for a long time now. Exploring surface plasmonic mode and hybrid mode can provide new insight for integrated photonics. Also, surface plasmonic mode and hybrid mode can overcome the dimension constraint of the optical mode, and the device dimension can be much smaller than the ones analysed. The MOSFET can be optimised further to get better changes in the effective index, which can not only be used in ring resonator but also for optical phase modulation. Other materials like crystalline silicon specifically used for integrated circuits can be used to get better results . More electronic and photonic devices can be combined to form new devices to be part of integrated circuits. Knowledge of VLSI circuits and MOSFET integration with analog devices can be used to shrink the MOSFET further.

Reference

1. Chuang, S.L., 2012. *Physics of photonic devices* (Vol. 80). John Wiley & Sons.
2. Pollock, C.R. and Lipson, M., 2003. *Integrated photonics* (Vol. 20, No. 25, p. 30).
3. Koch, T.L. and Koren, U., 1991. Semiconductor photonic integrated circuits. *IEEE Journal of Quantum Electronics*, *27*(3), pp.641-653.
4. Soref, R., 2006. The past, present, and future of silicon photonics. *IEEE Journal of selected topics in quantum electronics*, *12*(6), pp.1678-1687.
5. Nagarajan, R., Joyner, C.H., Schneider, R.P., Bostak, J.S., Butrie, T., Dentai, A.G., Dominic, V.G., Evans, P.W., Kato, M., Kauffman, M. and Lambert, D.J., 2005. Large-scale photonic integrated circuits. *IEEE Journal of Selected Topics in Quantum Electronics*, *11*(1), pp.50-65.
6. Bogaerts, W., Taillaert, D., Luyssaert, B., Dumon, P., Van Campenhout, J., Bienstman, P., Van Thourhout, D., Baets, R., Wiaux, V. and Beckx, S., 2004. Basic structures for photonic integrated circuits in silicon-on-insulator. *Optics Express*, *12*(8), pp.1583-1591.
7. Ozbay, E., 2006. Plasmonics: merging photonics and electronics at nanoscale dimensions. *science*, *311*(5758), pp.189-193.
8. Yariv, A., 2002. Critical coupling and its control in optical waveguide-ring resonator systems. *IEEE Photonics Technology Letters*, *14*(4), pp.483-485
9. Dong, P., Chen, Y.K., Duan, G.H. and Neilson, D.T., 2014. Silicon photonic devices and integrated circuits. *Nanophotonics*, *3*(4-5), pp.215-228.
10. Bogaerts, W., De Heyn, P., Van Vaerenbergh, T., De Vos, K., Kumar Selvaraja, S., Claes, T., Dumon, P., Bienstman, P., Van Thourhout, D. and Baets, R., 2012. Silicon microring resonators. *Laser & Photonics Reviews*, *6*(1), pp.47-73.
11. Pradeep, A., Mridula, S. and Mohanan, P., 2011. Design of an edge-coupled dual-ring split-ring resonator. IEEE Antennas and Propagation Magazine, 53(4), pp.45-54.

12. Gunn, C., 2006. CMOS photonics for high-speed interconnects. *IEEE micro*, *26*(2), pp.58-66.
13. Pinguet, T., Analui, B., Balmater, E., Guckenberger, D., Harrison, M., Koumans, R., Kucharski, D., Liang, Y., Masini, G., Mekis, A. and Mirsaidi, S., 2008, September. Monolithically integrated high-speed CMOS photonic transceivers. In *Group IV Photonics, 2008 5th IEEE International Conference on* (pp. 362-364). IEEE.
14. Su, L. and Tzuang, C.K.C., 2012. A narrowband CMOS ring resonator dual-mode active bandpass filter with edge periphery of 2% free-space wavelength. *IEEE Transactions on Microwave Theory and Techniques*, *60*(6), pp.1605-1616.
15. Ramiro-Manzano, F., Biasi, S., Bernard, M., Mancinelli, M., Chalyan, T., Turri, F., Ghulinyan, M., Borghi, M., Samusenko, A., Gandolfi, D. and Guider, R., 2016. Microring Resonators and Silicon Photonics. *MRS Advances*, *1*(48), pp.3281-3293.
16. Xiao, H., Li, D., Liu, Z., Han, X., Chen, W., Zhao, T., Tian, Y. and Yang, J., 2018. Experimental realization of a CMOS-compatible optical directed priority encoder using cascaded micro-ring resonators. *Nanophotonics*, *7*(4), pp.727-733.
17. Lin, B.J. and Lin, B.J., 2010, February. Optical lithography: here is why. Bellingham: SPIE.
18. Sampsell, J.B. and McDonald, T.G., Texas Instruments Inc, 1991. *Optical interconnection network*. U.S. Patent 5,037,173.
19. Griese, E., 2001. A high-performance hybrid electrical-optical interconnection technology for high-speed electronic systems. *IEEE Transactions on advanced packaging*, *24*(3), pp.375-383.
20. Choi, Y.K., Asano, K., Lindert, N., Subramanian, V., King, T.J., Bokor, J. and Hu, C., 1999, December. Ultra-thin body SOI MOSFET for deep-sub-tenth micron era. In *International Electron Devices Meeting 1999. Technical Digest (Cat. No. 99CH36318)* (pp. 919-921). IEEE.
21. Du, J. and Wang, J., 2018. Hybrid Plasmonic Microring Nano-Ruler. *Scientific reports*, *8*(1), p.9219
22. Ghibaudo, G., 1988. New method for the extraction of MOSFET parameters. *Electronics Letters*, *24*(9), pp.543-545.
23. Xiong, Y., Sun, S., Jia, H., Shea, P. and Shen, Z.J., 2009. New physical insights on power MOSFET switching losses. *IEEE Transactions on Power Electronics*, *24*(2), pp.525-531.
24. Harrison, L., 2006. An introduction to Depletion-mode MOSFETs

25. Ortiz-Conde, A., Sánchez, F.G., Liou, J.J., Cerdeira, A., Estrada, M. and Yue, Y., 2002. A review of recent MOSFET threshold voltage extraction methods. *Microelectronics Reliability*, *42*(4-5), pp.583-596.
26. Keiser, G., 2008. *Optical fiber communications*. McGraw-Hill.
27. Soref, R.I.C.H.A.R.D.A. and Bennett, B.R.I.A.N.R., 1987. Electrooptical effects in silicon. *IEEE journal of quantum electronics*, *23*(1), pp.123-129..
28. Maldonado, T.A., 1995. Electro-optic modulators. Handbook of optics, 2, pp.13-11
29. Brews, J.R., Fichtner, W., Nicollian, E.H. and Sze, S.M., 1979. Generalized guide for MOSFET miniaturization. In *Electron Devices Meeting, 1979 Internationa* (pp. 10-13). IEEE.