PERFORMANCE ENHANCEMENT OF 3D CYLINDRICAL GATE-ALL-AROUND TUNNEL FET AND ITS APPLICATIONS FOR ULTRA LOW POWER CROSS COUPLED VOLTAGE DOUBLER CIRCUIT DESIGN

Ph.D. Thesis

By

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DISCIPLINE OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE

MARCH 2018

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A THESIS

Submitted in partial fulfillment of the
requirements for the award of the degree

of
DOCTOR OF PHILOSOPHY

By

ANKUR BEOHAR

DISCIPLINE OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE
MARCH 2018

INDIAN INSTITUTE OF TECHNOLOGY INDORE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled "**Performance Enhancement of 3D Cylindrical Gate-all-around Tunnel FET and Its Applications for Ultra Low Power Cross Coupled Voltage Doubler Circuit Design**" in the partial fulfillment of the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY** and submitted in the **DISCIPLINE OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from December 2014 to March 2018 under the supervision of
Dr. Santosh Kumar Vishvakarma, Associate Professor, Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Signature of the Student with Date
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This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

Signature of Thesis Supervisor with date
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Ankur Beohar has successfully given his Ph.D. Oral Examination held on

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Signature of PSPC Member #1 Date:	Signature of PSPC Member #2 Date:	Signature of Convener, DPGC Date:

Signature of Head of Discipline
Date:

ACKNOWLEDGEMENTS

First and Foremost, I thank God Almighty for enlightening my mind to undertake this research work. Then, I would like to express my sincere thanks of gratitude to my PhD supervisor **Dr. Santosh Kumar Vishvakarma** for accepting me as a Ph.D. candidate in his research group at IIT Indore. **Dr. Vishvakarma's** guidance, support, tireless motivation, care and intellectual helped me to see the light at the end of the tunnel. He constantly encouraged me to focus on most important and challenging research problems, and stimulated me in finding innovative solutions. It has been a enriching and a great learning experience for me throughout my doctoral work under his supervision at IIT Indore. In addition, he gave me an opportunity to work as a **Research Associate-I** under the Council of Scientific & Industrial Research **(CSIR)** sponsored project. As a **Principal Investigator,** he guided me in every stage of solutions for methodologies used throughout the entire progress of the Project objectives set out.

I would like to express my sincere thanks to **Prof. Pradeep Mathur**, Director, IIT Indore and **Prof. N. K. Jain,** Dean of Academic Affairs, IIT Indore, who has been highly encouraging during the entire course of my doctoral work.

I am extremely grateful to my PSPC committee members, **Prof. Ram Bilas Pachori** and **Dr. Shaikh M. Mobin,** for their encouragement, insightful suggestions and valuable comments, which helped in improving my research work. Furhter, I gratefully acknowledge the contribution of all the faculty members of Electrical Engineering and staff members of IIT Indore for their kind help with the academic and research work. I would like to express my sincere gratitude to **Madhya Pradesh Council of Science & Technology (M.P.C.S.T)** for sanctioned international travel **grant no. 1890/CST/R&D/2017** regarding International Symposium at Hsinchu, Taiwan. Besides, I would like to express my sincere acknowledge to **HRDG, EMR Division**, **C.S.I.R**., Government of India for providing the fellowship during the course of the Ph.D. programmed. I would also like to thank **IIT Indore** for providing the essential research facilities for my thesis work.

I express my profound appreciation and wholehearted thanks to my seniors **Dr. Bhupendra Singh Reniwal**, **Dr. Vikas Vijayvargiya**, **Dr. Pooran Singh Bisht, Dr. Deepika Gupta, Dr. Dheeraj Sharma**, **Dr. Chandrabhan Singh Khushwah** and my colleagues, **Mr. Abhishek Kumar Upadhayay, Mr. Mahesh Kumawat, Mr. Maisagalla Gopal, Mr. Vishal Sharma, Mr. Gaurav Singh, Mr. Ravi Kumar, Ms. Pooja Bohara, Mr. Sajid Khan, Mr. Gopal Raut, Ms. Neha Gupta, Ms. Gunjan Rajput** and **Mr. Dipesh Monga** for their trustworthy help, constant encouragement and moral support during the tough time of research work.

Further, I would like to express sincere thanks to **Dr. Nandakishor Yadav** and **Mr. Ambika Prasad Shah** for very important and helpful technical discussions.

Above all, I am indebted to my beloved family members especially my father **Shri Indra Bhushan Beohar**, my mother **Smt. Sarupa Beohar**, and my brother **Mr. Ashish Beohar**, they helped me in every ways to be the person that I am today.

Besides, my sweat sisters **Mrs. Nidhi Shrivasrtava**, **Mrs. Vidhi Rawat**, **Mrs. Salty Saxena,** and my brother-in-laws **Mr. Ajay Shrivastava**, **Mr. Abhishek Rawat**, **Mr. Ankit Saxena**, **Mr. Akash Shrivastava.** My parent-in-laws **Shri Hari Prasad Shrivastava,** and **Dr. Sunita Shrivastava**, who nurtured me through their boundless love, affection, and encouragement at every stage of my personal and academic life, and longed to see this achievement come true.

Most importantly, this journey would have not been possible without the love and support of my wife **Mrs. Neera Beohar**. Her constant motivation through this time inspired me to achieve greatest milestones in life.

Finally, I want to express my heartiest gratefulness to my loving children **Aditri** and **Amogh** for their infinite love and deep affection.

ANKUR BEOHAR

Dedicated To My Parents,

My Wife

&

My Kids : Aditri & Amogh

ABSTRACT

Today's market of semiconductor industry influenced by assertive scaling leads to the requirement of low power devices. However, conventional MOS field effect transistor (*MOSFET*) scaling in order to maximize on-die functionality has had a significant detrimental impact on leakage-dominated OFF-current. This is because of its sub threshold slope (*SS)*, governed by thermionic emission-carrier diffusion over a thermal barrier being limited to 60 mV/decade ($SS = (kT/q) \times ln10$) at room temperature. Further the demand of circuit application needs ultra-low power consumption to utilize battery for longer duration. Although, scaling down of MOSFET supply voltage is very difficult without significantly increasing the subthreshold leakage current. As a result, a tradeoff exists between the ability to operate in the subthreshold regime while simultaneously maintaining low-power dissipation. This limitation is challenging for low supply voltages and making it unsuitable for analog/RF applications. Therefore, for next generations of integrated circuits, there is a need for ultra-low-power and energy-efficient transistors with steepest *SS*.

In this regard, the devices based on the inter-band tunneling such as Tunnel Field effect transistor (*TFET*) appear as a prominent novel device for low-power application over conventional MOSFET. This is because of their attractive properties of low *SS*, caused by the different carrier conduction mechanism based on band-to-band tunneling (*BTBT*). This enables low standby leakage currents and further scaling of supply voltage (V_{dd}), makes it suitable for low power module of *IoT* applications contains analog/RF and digital blocks. In addition with low off current, high current driving capability is also required to produce attractive analog/RF characteristics. In this concern, an optimized Tunnel FET structure that can improve driving current as well as analog/RF characteristics without an increase in I_{OFF} is of great importance for low power module of *IoT* applications. Therefore, in this thesis, we have investigated the device design and circuit performance of a 3D Cylindrical (*Cyl*) gate all around (*GAA*) Tunnel *FET*. In this *3D* structure, gate is wrapped all around the channel, which increases the tunneling rate between source/channel junction and significantly, supports for high driving current. Here, we will explore methods to improve analog/RF performances of the 3D Cyl Gate-All-Around Tunnel FET using a spacer and underlap engineering for low power applications. Further, we

have extended our analysis towards the analog/RF performances and circuit design for a low power Cross Coupled Voltage Doubler (*CCVD*).

Initially, we have calibrated the examined device with experimental published data and investigated the comparative device performance for the three structures of Cyl GAA-Tunnel FET in terms of DC characteristics such as I_{ON}, I_{OFF}, *SS, and* I_{ON}/I_{OFF}. Here the design and physics of the examined device was mainly focused to achieve low subthreshold leakage and ambipolar behavior without affecting high $I_{ON,}$ using the concept of low spacer width and asymmetry in underlap. Here, it is found that asymmetry in underlap with low spacer width produces the best device performance regarding DC characteristics.

In continuation of chapter 2, we have presented the investigations of Cyl GAA-TFET based on *Ge*-source for improved analog/RF characteristics. Here, physics of fringing field was implemented using hetero-spacer dielectric with merits of low band gap material such as *Ge*, which increases the tunneling rate by reducing the barrier width of junction and is a feature for enhanced DC and Analog/RF characteristics such as I_{ON}, I_{OFF}, *SS,* C_{gs}, C_{gd}, g_m, f_t, *and* f_{max}.
Besides, the high performances of the examined device, reliability is also an important concern, Therefore, we have presented the effects of Trap-Assisted Tunneling (*TAT*) on Cylindrical GAA-Tunnel FET based on hetero-spacer engineering for improved device reliability. Here, impact of trap charges have been studied while incorporation of TAT physical model for the analysis of experimental/ fabrication non-idealities caused by heavy doping, phonons and high radiations.

Finally, I have comprehensively investigated the circuit performance parameters of the proposed device using device-circuit co-approach while design a *CCVD* for low power *IoT* sensor node.

LIST OF FELLOWSHIPS AND PUBLICATIONS

Fellowships (03)

[1] Recipient of **Senior Research Associate (SRA) under Scientist Pool scheme** awarded by the Council of Scientific and Industrial Research (C.S.I.R.), HRDG, New Delhi, Govt. of India for the period from 15-11-2018 to 14-11-2020.

[2] Recipient of **Research Associate-I** for the **CSIR HRDG** Sponsored Project entitled "Investigation of Analog/RF and Digital Performance of Cylindrical (Cyl) Gate All-Around (GAA) Tunnel Field Effect Transistor (TFET) for Ultra Low Power Applications," for the period of **3.5 years** with effect from 01-10-2014 to 31-03-2018.

[3] Recipient of International Travel Grant no. **1890/CST/R&D/2017**, Sanctioned by M.P. Council of Science and Technology (**M.P.C.S.T**.), Bhopal.

Publications Based on Thesis work

***Peer Reviewed Journals* (05)**

[1] **Ankur Beohar**, Nandakishor Yadav, Ambika Prasad Shah and Santosh Kumar Vishvakarma, "Analog/RF characteristics of a 3D Cyl underlap GAA-TFET based on a Ge-Source using fringing field engineering for low power applications," *Springer Journal of Computational Electronics*, vol. 17, no. 4, Dec. 2018, pp 1650–1657 (**SCI**, **Impact factor: 1.43).**

[2] **Ankur Beohar**, Nandakishor Yadav, and Santosh Kumar Vishvakarma, "Analysis of Trap Assisted Tunneling in Asymmetrical Underlap 3D-Cylindrical GAA-TFET based on Hetero-Spacer Engineering for Improved Device Reliability," *IET Micro & Nano Letters*, vol. 12, no. 12, Dec. 2017, pp. 982-986 **(SCI, Impact factor: 0.84).**

[3] **Ankur Beohar** and Santosh Kumar Vishvakarma, "Performance Enhancement of Asymmetrical Underlap 3D Cylindrical GAA-TFET with low Spacer Width," *IET Micro & Nano Letters*, vol. 11, no. 8, May 2016, pp. 443-445 **(SCI, Impact factor: 0.84).**

[4] Santosh Kumar Vishvakarma, **Ankur Beohar**, Vikas Vijayvargiya and Priyal Trivedi, "Analysis of DC and Analog/RF performance on Cyl GAA-TFET using distinct device geometry," *IOPScience, Journal of Semiconductor*, vol. 38, no.7, July 2017, pp. 074003 (1-5) (**Scopus Index**, **Cite factor: 0.87).**

[5] **Ankur Beohar**, Nandakishor Yadav, Ambika Prasad Shah and Santosh Kumar Vishvakarma, "A Low Power Cross Coupled Voltage Doubler Design based on 3D Cyl GAA-TFET for low power applications: A Device Circuit Co-design," *IEEE Trans. on Semiconductor Manufacturing,* under review **(SCI, Impact factor: 1.33).**

Peer Reviewed International Conferences **(03)**

[1] **Ankur Beohar**, Santosh Kumar Vishvakarma, "Performance Enhancement of 3D Cylindrical (Cyl) Gate All Around (GAA) Tunnel Field Effect Transistor (TFET) With Asymmetrical Spacer Width," *18th International Workshop on Physics of Semiconductor Devices (IWPSD)*, IISc, Bangalore, India, Dec. 7th-10th, 2015.

[2] **Ankur Beohar**, Ambika Prasad Shah, Nandakishor Yadav, and Santosh Kumar Vishvakarma," Design of 3D Cylindrical GAA-TFET Based on Germanium Source with Drain Underlap for Low Power Applications," *13th IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, National Tsing Hua University, Hsinchu, Taiwan, Oct. 18th-20th, 2017.

[3] Shraddha Thakre, **Ankur Beohar**, Vikas Vijayvargiya, and Santosh Kumar Vishvakarma, "Investigation of DC Characteristic on Tunnel FET with High-K Dielectric using Distinct Device Parameter," *2nd IEEE International Symposium on Nanoelectronic and Information systems (iNIS)*, IIITM Gwalior, India, Dec. 19th-21th, 2016.

Publications besides thesis work

Peer Reviewed Journals **(06)**

[1] Ambika Prasad Shah, Nandakishor Yadav, Ankur Beohar and Santosh Kumar Vishvakarma, "Process Variation and NBTI Resilient Schmitt Trigger for Stable and Reliable Circuits," *IEEE Transactions on Device and Materials Reliability*, vol. 18, no. 4, Dec. 2018, pp. 546-554 **(SCI, Impact factor: 1.51).**

[2] Ambika Prasad Shah, Nandakishor Yadav, **Ankur Beohar** and Santosh Kumar Vishvakarma, "On-chip Adaptive Body Bias for Reducing the Impact of NBTI on 6T SRAM Cells," *IEEE Transactions on Semiconductor manufacturing*, vol. 31, no. 2, May 2018, pp. 242-249 **(SCI, Impact factor: 1.33).**

[3] Ambika Prasad Shah, Nandakishor Yadav, **Ankur Beohar** and Santosh Kumar Vishvakarma, "An Efficient NBTI Sensor and Compensation Circuit for Stable and Reliable SRAM Cells," *Elsevier Microelectronics Reliability*, vol. 87, no. 8, August 2018, pp. 15-23 **(SCI, Impact factor: 1.23).**

[4] Ambika Prasad Shah, Nandakishor Yadav, **Ankur Beohar** and Santosh Kumar Vishvakarma, "NMOS Only Schmitt Trigger for NBTI Resilient CMOS Circuits," *IET Electronics Letters*, vol. 54, no. 14, July 2018, pp. 868-870 **(SCI, Impact factor: 1.23).**

[5] Nandakishor Yadav, Ambika Prasad Shah, **Ankur Beohar** and Santosh Kumar Vishvakarma, "Symmetric dual Gate Insulator based FinFET Module and Design Window for Reliable Circuits,*" IET Micro & Nano letters*, "Accepted" **(SCI, Impact factor: 0.84).**

[6] Ambika Prasad Shah, Nandakishor Yadav, Ankur Beohar and Santosh Kumar Vishvakarma, "SUBHDIP: Process Variations Tolerant Subthreshold Darlington Pair Based NBTI Sensor Circuit," *IET Computers & Digital Techniques*, "Accepted" **(SCI, Impact factor: 0.63).**

Peer Reviewed International Conferences (04)

[1] Nandakishor Yadav, Ambika Prasad Shah, **Ankur Beohar** and Santosh Kumar Vishvakarma, "Source Drain Gaussian Doping Profile Analysis for High ON Current of InGaAs Based HEMT,"*13th IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, National Tsing Hua University, Hsinchu, Taiwan, Oct. 18th - 20th, 2017.

[2] Ambika Prasad Shah, Nandakishor Yadav, **Ankur Beohar** and Santosh Kumar Vishvakarma, "Subthreshold Darlington Pair Based NBTI Sensor for Reliable CMOS Circuits," *13th IEEE International Conference on EDSSC*, National Tsing Hua University, Hsinchu, Taiwan, Oct. 18th -20th, 2017.

[3] Ambika Prasad Shah, Nandakishor Yadav, **Ankur Beohar** and Santosh Kumar Vishvakarma, "On-Chip NBTI Sensor Circuits for Stable and Reliable CMOS Circuits," *31st International Conference on VLSI Design*, Pune, Maharashtra, India, Jan. 6th -11th, 2018.

[4] Nandakishor Yadav, **Ankur Beohar,** Ambika Prasad Shah, and Santosh Kumar Vishvakarma, "Analytical Single Trap-Induced Threshold Voltage shift Modeling for Asymmetric high-k spacer FinFET," *4th International Conference on Production & Industrial Engineering (CPIE)*, Dr. B R. Ambedkar National Institute of Technology, Jalandhar, Dec. 19th -21th, 2016.

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LIST OF ABBREVIATIONS

FET	Field Effect Transistor
DG	Double Gate
SS	Subthreshold Swing
I_{ON}	ON-state Current
I_{OFF}	OFF-state Current
I_{amb}	Ambipolar Current
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
TFET	Tunnel Field Effect Transistor
MuGFET	Multiple Gate MOSFET
GAA	Gate-all-around
SCEs	Short Channel Effects
DIBL	Drain Induced Barrier Lowering
RF	Radio Frequency
SoC	System on Chip
IoT	Internet of things
CCVD	Cross Coupled Voltage Doubler
ε_0	Permittivity of Vacuum
ε_{Si}	Relative Permittivity of Silicon
ε_{ox}	Relative permittivity of Gate Insulator
t_{ox}	Oxide Thickness
W	Device Width of Silicon for DG-TFET
L	Channel Length of Silicon for DG-TFET

$\mathbf{t_{Si}}$	Silicon Thickness for DG-TFET
k	Boltzmann Constant
T	Temperature
Q	Electron Charge
$\boldsymbol{V_{th}}$	Threshold Voltage
$\boldsymbol{V_{gs}}$	Gate to Source Voltage
$\boldsymbol{V_{ds}}$	Drain to Source Voltage
$\boldsymbol{C_{gs}}$	Gate to Source Capacitance
$\boldsymbol{C_{gd}}$	Gate to Drain Capacitance
$\boldsymbol{C_{gg}}$	Gate to Gate Capacitance
LAD	Lateral Asymmetric Drain
$\mathbf{L_{extd}}$	Source-Drain Extension Length
UL	Underlap Length
HG	Hetero-Gate
HK	High-k Dielectric
$\mathbf{g_m}$	Transconductance
$\mathbf{g_d}$	Conductance
$\mathbf{R_{dcr}}$	Distributed Channel Resistance
$\mathbf{f_t}$	Cut-off Frequency
$\mathbf{f_{max}}$	Maximum Oscillation Frequency
GBW	Gain Bandwidth Product

CHAPTER 1

Introduction

Over the past century, the world of scientific research in the field of electronics has been revolutionized by the introduction of the integrated circuits *(ICs)*. The basic component of an *IC* is the transistor leading to useful commercial products for the benefit of mankind [1–4]. The first invention of the field effect transistor (FET) by *Prof. Julius Edgar Lilienfeld* was patented in 1926 [5]. This patent illustrated a three terminal device, where the current was controlled by a field from a gate. However, the technology of that time faced difficulty to fabricate the successful device based on *Lilienfeld* concept. The first working point contact transistor was invented and demonstrated by the three American Physicist *John Bardeen, Walter Houser Brattain*, and *William Bradford Shockley* at Bell laboratory on December 16, 1947 and honored with the Nobel Prize in 1956 [6]. Further, *Prof. M. M. Attalla* and his team reported the first successful *Si-*SiO_2 metal oxide semiconductor field effect transistor (MOSFET) at Bell Labs in 1959 [7]. Regrettably, the invented transistor was slow and need some more advanced feature. Inventions happened motivated the industries since the 1950s to learn the art of semiconductor manufacturing and explore a revolution in the growth of semiconductor industries [6], [8]. The semiconductor industry's workhorse technology is silicon complementary metal oxide semiconductor (CMOS) and the building block of CMOS is the MOSFET.

Nowadays, MOSFETs are aggressively scaled down to put the MOS devices into nanometer regime [9], [10]. The aim of scaling is to achieve high chip density, speed, low power, and cost per chip density. These are the requirements for today's portable device such as smart phone and electronic gadgets [11], [12]. Besides, during scaling the reductions in device capacitance increases the both speed as well as analog/RF performances of the device and the range of radio frequency reached into *GHz* as well. However, aggressive scaling reduces the capability of gate electrode to control the potential distribution and the bulk-silicon transistor faces serious issues such as short channel effects (*SCEs*). Further, scaling down the supply voltage of conventional MOSFET is very difficult without significantly increasing the OFF-state current (I_{OFF}). As a result, a tradeoff exists between the ability to operate in the sub-

threshold regime while simultaneously maintaining low-power dissipation. In this regard, an optimized device based on tunneling is of great importance. It can improve driving current as well as analog and radio frequency (RF) characteristics without an increase in leakage current for a low power module of Internet of Things (*IoT*) sensor node.

In 1978, J. J. Quinn *et al.* proposed a surface channel tunnel junctions (SCTJ), which can be fabricated by replacing the usual degenerate n-type source contact on a weakly p-type substrate by a highly degenerate p-type source. In this work, he demonstrates the physics of a quasi-two-dimensional surface channel. However, it was found that the current based on tunneling was much lower than the MOS current. Moreover in tunneling, a higher current density is important for the high speed performance of circuit applications [13]. The other main difference of tunneling device with MOS device at low bias was that tunneling device falls in the off-state, whereas, the MOS device was in the ON state always. This concludes that the current in the tunneling device flows only in a strong inversion regime, where the tunneling distance becomes too small. Further, E. Takeda *et al* in [14] proposed and characterized experimentally a band to band tunneling MOS device (B^2-MOSFET). However, it was found that this band to band tunneling induced a hot-carrier-generation, which decreases the threshold voltage (V_{th}) and increases the transconductance (g_m) due to hole trapping in n-channel MOSFETs.

Koga *et al* proposed a negative differential conductance in three-terminal silicon surface tunneling device for the low power, high-speed functional devices below 100 nm VLSI circuits [15]. The device is fabricated on a SIMOX wafer to achieve a very small bulk leakage current. Although, one big concern with Tunnel FETs is that they may not exhibit high drive currents due to a high tunneling resistance. We have experimentally demonstrated s-Ge, DG TFETs exhibiting record high drive currents. However, they exhibit ambipolar behavior, which leads to high off-state leakage.

In continuation with this core literature, W. Hansch *et al.* fabricated for the first time a vertical, MOS gated Esaki tunneling transistor in silicon. Here, the doping profile structure is created by means of molecular beam epitaxy (MBE) [16], [17]. It combining the advantages of both bipolar and MOS devices: fast switching due to an exponential increase in current with current consumption. In addition, K. K. Bhuwalka *et al* in [18] proposed a vertical tunnel field-effect transistor (FET). The device, a gated P-I-N diode based on silicon, showed gate-controlled band-to-band

tunnelling from the heavily doped source to the intrinsic channel. An exponentially increasing input characteristic and off-currents of the order of 1 fA/um for sub-100-nm channel lengths were observed, which is quiet high and cannot be accepted for high analog/RF and circuit Performances [9].

Therefore, in this thesis, we have investigated three dimensional (3D) n channel cylindrical (Cyl) gate-all-around (GAA) Tunnel FET for improved DC, analog/RF performances and its circuit applications.

1.1 Attributes of MOSFET

Over the past few decade, attributes of MOSFET produces various notification in semiconductor industries:

1.1.1 Moore's Law

In 1965, Gordon Moore, the co-founder of Fairchild Semiconductor and Intel observed that the number of transistors in a dense integrated circuit is increasing exponentially with time, doubling approximately every two years [19]. This prediction of *Prof. Moore* become a well-known law as Moore's law and has been remarkably followed by the semiconductor industry for the last forty years. Moore's prediction proved accurate for several decades, and has been used in the semiconductor industry to guide long-term planning and to set targets for research and development [20]. Almost every measure of the capabilities of digital electronic devices is linked to Moore's law, for example processing speed and memory capacity, sensors and even the number and size of pixels in digital cameras. All of the above parameters are improving at roughly exponential rates as well. The doubling of performance every second year has created market driven demand of expectations that the future will give the same increase in performance. This has dramatically increased the usefulness of digital electronics in nearly every segment of the world economy.

1.1.2 MOSFET Scaling

Over the past few decades, the MOSFET plays an essential role in semiconductor industries. As discussed, the dimensions of MOSFET are shrunk; the performances of transistor have been drastically improved in terms of high density, , speed, and battery

life. However, aggressive transistor feature size scaling in order to maximize on-die functionality has had a significant detrimental impact on leakage-dominated OFF-state power dissipation and reduces the chip functionality, Therefore, the single gate *bulk* MOSFET is almost at the end of the roadmap as scaling the close proximity between source and drain reduce the capability of gate electrode to control the potential distribution and causes serious issues such as *SCEs* that start plaguing the *bulk* MOSFET technology [21]. As a result, the *OFF* state current increases and the *ON-OFF* current ratio degraded, significantly causes degradation in analog/RF characteristics. Therefore, the device performance was worsened and for all practical purposes, it seems further impossible to scale the dimensions of classical bulk MOSFETs [10]. So, it seems to replace the bulk single gate MOSFET by changing device architecture or Multigate MOSFETs.

1.1.3 Multigate MOSFETs

As discussed, the design of analog/RF devices for ultra-low-power circuit applications have become increasingly challenging and difficult with the rigorous downscaling in standard planar digital CMOS technologies in the deep sub micrometer [22], [23]. The introduction of multi-gate device architectures (MuGFET) and novel material (high-k, metal gate) will significantly change analog/RF device properties and hence will also impact circuit design performance [24]. The MuGFETs have a strong potential to extend the *CMOS* scaling into the sub-30 nm regime [25]. They offer superior electrostatic gate control over the channel and low screening length due to multiple gates; they suppress *SCEs* and leakage current. The optimized structure also helps to alleviate several other issues of nanoscale MOSFETs e.g. mobility degradation, random dopant fluctuation, and compatibility with mid-gap material gate, etc. [26]. Further, the use of strained silicon, a metal gate and high-k dielectric as gate insulator can also enhance the driving current of the device. The screening length can also be reduced by decreasing the gate oxide thickness or either by using the low band gap material. The circuit performance also benefits from novel gate stack material, reduced parasitic capacitance and hole mobility improvement [23]. Therefore, the MuGFETs are strong candidates for replacing conventional single gate MOSFET in future.

Further, the transconductance (g_m) of the MOSFET describes how efficient a small voltage signal at the transistor gate is converted into a drain current signal. The g_m of the MuGFET is mainly high due to the lower source/drain resistances than that of bulk FET. The situation gets worse for short channel lengths and increasing overdrive voltage, while MuGFET has high gain because it has very low output conductance due to the undoped fins. The intrinsic transistor gain relates the effectiveness of the transistor as controlled current source in regard to the output resistance. The intrinsic gain limits the open-loop gain of operational amplifier for specified bandwidth as well as the resolution of analog to digital converters. Therefore, for analog perspective, the high intrinsic gain is a strong argument to use MuGFET device in future technology nodes, as it overcomes one of the most critical scaling issues in planar bulk CMOS.

Among all MuGFETs, Cylindrical (Cyl) Gate-all-around (GAA) FET structures are used to be the ideal devices to achieve the highest degree of electrostatic gate control over the channel suitable for low power analog/*RF* applications. This is due to low screening length, volume inversion, and better scaling options. However, low power device engineering is still a need for efficient circuit applications.

1.1.4 Device Engineering

As discussed, the continuous downscaling of the conventional MOSFET inevitably leads to fundamental physical limits that can no longer be overcome by technology innovation alone. Therefore, the concepts of device engineering have been introduced to minimize *SCEs* and high analog/*RF* performances. The reported devices engineering are underlap (*UL*) architecture with Source/Drain extension length (SDE) [9], [21] channel [23], [27], band gap and spacer engineering [21], [28]. Further, it has been reported that parasitic capacitance is a dominating factor. Therefore, in order to reduce parasitic capacitance, underlap feature has been introduced in the source/drain extension region. The *UL* is the length between metallurgical source-channel/drain-channel junctions to starting edge of doping segregation length in source/drain region. This architecture improves circuit performance due to reduction in parasitic capacitances. Although, the *UL* feature produces parasitic resistance causes decrease in ON-state current (I_{ON}) and degrade the analog/RF performances. In this context, a trade-off exists between minimum parasitic capacitance and high *RF* performances [9], [29]. Furthermore, spacer engineering is proposed to increase the fringe coupling

between gate electrode and *UL* architecture to reduce the parasitic resistance. Despite of higher fringing capacitance, this device engineering has shown its suitability for improving the analog/*RF* performances [21].

In channel engineering, asymmetric channel doping profile [9], [30], [31] was employed in channel region. In this engineering, high doping concentration is proposed near the source side in the channel region and low doping concentration is used for the drain side. This reduces *SCEs* and improves analog/RF performances due to reduction in series gate capacitance. In order to reduce the fringing capacitance, Pal *et al.* in [28] employed dual-k spacer based tri-gate field effect transistor for the improvement in digital performance at 14 nm technology node. Authors proposed the concept of device engineering to improve device performance in terms of I_{ON}, I_{ON}/I_{OFF}, subthreshold swing (*SS)*, *SCEs*, and capability for the improved analog/*RF* as well as digital performance.

Also, the optimized device will give better performance with low power circuits. However, the power consumption is going to be the major issue in sub-nanometer dimension [28], [32], [33]. Hence, supply voltage (V_{dd}), threshold voltage (V_t) and OFF voltage (V_{off}) must be reduced and simultaneously overdrive factor (V_{dd} -V_{off}) must be high to meet the best device performance.

Further, it was reported that OFF-state current increases more than tenfold increase for every 60 *mV* scaling of V_{dd} at room temperature [12], [33–36]. When gate overdrive decreases, ON-current decreases, leads to low I_{ON}/I_{OFF} ratio, and high dynamic delay. To overcome the problem for needing a high gate overdrive: either V_{dd} can stay higher than it should with constant field scaling, or V_t can be scaled down more aggressively. Both of these options, and their repercussions, will be discussed.

In order to maintain the acceptable levels of gate overdrive, V_{dd} scaling has slowed down drastically. The dynamic delay can be expressed as:

$$\tau = (C_{gg} \times V_{dd})/I_{on} \tag{1.1}$$

When the supply voltage decreases along with device dimensions, then the power density remains constant, which means that the energy needed to drive the chip, and the heat produced by the chip, remains constant. This assumes that when the devices scale down, we added more complexity and functionality with each generation, and chip size remains more or less constant.

The power consumption in MOSFET can be categorized in two parts namely dynamic power consumption and static power consumption. When V_{dd} doesn't scale down, power density increases instead. For each MOSFET, the dynamic and static power consumption can be expressed as:

$$P_{dynamic} = C_{total}(V_{dd}^2)f \quad (1.2)$$

$$P_{static} = I_{leak}V_{dd} \quad (1.3)$$

Where V_{dd} is the supply voltage, C_{total} is the total switched capacitive load, and I_{leak} is the sum of the leakage currents in the device when the MOSFET is in OFF-state [33]. Static power consumption is defined as the circuit logic operation corresponding to inputs but not in switching state and the device continuously consumes power from the supply voltage. The power consumption is also referred as leakage power consumption.

The power consumption is going to be dominating factor over dynamic power consumption especially below 0.5 V of supply voltage [37]. Further, short channel effects in MOSFET nanometer regime needed to discuss are threshold voltage roll off (due to charge sharing), *SS,* and drain induced barrier lowering effects.

1.1.5 Short Channel Effects in MOSFET

As discussed to meet with the customer demand of small area and low cost handhold devices, scaling of MOSFET has become inevitable. The scaling of MOSFET introduces SCEs, which falsely modify the device characteristics [11], [26]. Specifically, following parameters defines the *SCEs* in any MOS devices.

1.1.5.1 Threshold voltage roll-off

The threshold voltage roll-off (ΔV_t) is an effect, where there is a reduction in threshold voltage with decrease in channel length. Therefore, at shorter channel length, the device may turn on erroneously and may degrade its performance. Importantly, ΔV_t occurs in MOS based devices due to charge sharing between source/drain and gate terminals of the device [38]. Further, this effect will cause the reduced gate control over the channel under the presence of the higher lateral electric field between source and drain terminal. This lateral electric field forces the threshold voltage reduction with scaling, even without gate intervention. Therefore, smaller

change in threshold voltage of MOS based devices with technology reduction may serve the purpose of scaling.

1.1.5.2 Drain Induced Barrier Lowering

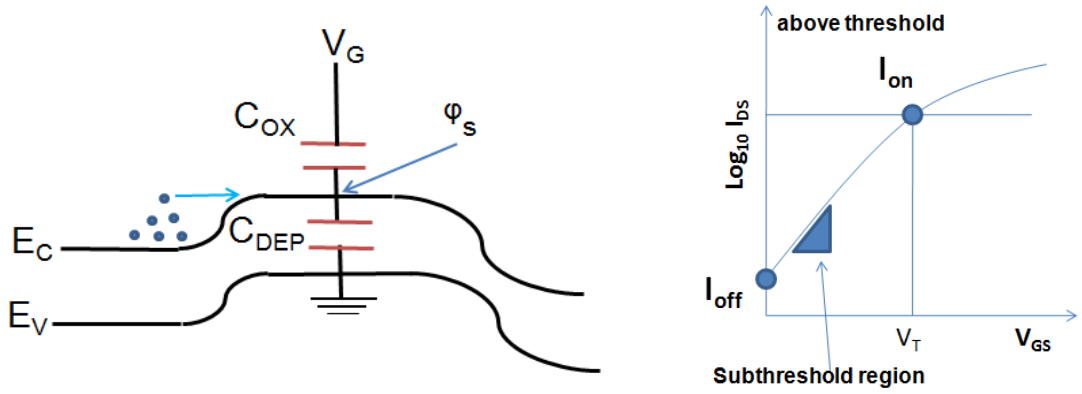
Drain Induced Barrier Lowering (*DIBL*) is a secondary effect in MOS based devices referring originally to a reduction of threshold voltage of the transistor at higher drain voltage. Here, as the drain voltage is increased, the depletion region of the PN-junction between the drain and the body increases in size and extends under the gate. So, the drain occupies a larger portion of the burden of balancing depletion region charge, leaving a smaller burden for the gate. As a result, the charge present near the gate retains charge balance by attracting more carriers into the channel. It lowers the threshold voltage of the device. Hence, the *DIBL* effect could be defined as the decrease in threshold voltage when the drain voltage is increased from a low value of V_d to a high value V_d. However, for fully depleted device, the potential profile underneath the gate terminal is controlled by field lines originating from the source and drain instead of front gate. Also, the field lines inside the buried oxide changes the *DIBL* with drain bias [39].

Therefore, the source-drain lateral field coupling causes *DIBL* in fully depleted MOS devices. In conclusion, for a MOS based device, *DIBL* is a negative phenomenon and it must be as small as possible to improve the reliability. Also, the *DIBL* increases with the scaling of MOS device which presents the provocation for device performance.

1.1.5.3 Subthreshold Swing

The energy band-diagram of n channel-MOSFET in OFF state is shown in Figure 1.1 (a). A large energy barrier exist between source and channel when the device in OFF state corresponding to a flow of very small amount of leakage current (I_{OFF}) as shown in Figure 1.1 (b).

On applying the positive voltage to the gate terminal, conduction band of channel region aligns with the valance band of source region and the energy barrier between source and channel reduces, causes electrons in the source conduction band through thermionic injection into the channel conduction band through diffusion process reaches towards drain side.



(a) (b)

Figure 1.1 n-channel MOSFET (a) Energy band diagram model with associated capacitances (b) Transfer characteristics corresponding to ON-state current [33], [36].

Subthreshold conduction is a phenomenon which represents drain current below the threshold voltage. This current appears due to the weak inversion in the channel between at band and threshold voltage. Hence, a diffusion current flows from source to drain, even below the threshold voltage. This sub-threshold conduction should be minimizing for any MOS devices. To investigate the sub-threshold conduction, sub-threshold swing (*SS*) is used. The average sub-threshold swing (SS_{AVG}) defines the requirement of the minimum power supply voltages and minimum power dissipation of a device. Also, it is defined as the gate voltage required to changing the drain current by one order of magnitude per decade, defined by the equation as follows [33]:

$$SS_{AVG} = \frac{(V_t - V_{off})}{log(I_{V_t}) - log(I_{V_{off}})} \tag{1.4}$$

Here, V_{off} is the gate source voltage from which the drain current starts to take off (source channel tunnelling), I_{V_t} is the drain current of the device at $V_{gs} = V_t$, $I_{V_{off}}$ is the drain current at $V_{gs} = V_{off}$.

Therefore devices with a steep *SS* called steep slope switches are expected to enable V_{dd} scaling. It was reported that OFF-state current increases more than tenfold increase for every *60 mV* scaling of V_{dd} at room temperature [12], [33], [34], [40]. Consequently, with the small value of *SS*, the MOS device will act as better switch. In contrast, with the scaling, *SS* of MOS based devices increases which poses a

limitation and slows down the speed of the device. While scaling, smaller *SS* is important to obtain for the reliability of the considered MOS device. In the MOSFET, the *SS* is limited to *(kT/q) ln10* or 60 *mV/dec* at room temperature, and with scaling, the *SS* increases. This region also measures the capability of MOSFET for digital performance in terms of *SS*. It is modeled by the equation as follows [33], [36]:

$$SS = \frac{dV_g}{d(log_{10} I_d)} \tag{1.5}$$

$$= In\ 10 \frac{kT}{q} \left(1 + \frac{C_{dep}}{C_{ox}} + \frac{C_{ss}}{C_{ox}}\right) \tag{1.6}$$

$$= \frac{kT}{q} \text{In } 10 \ = \ 60\ mV/\ dec \tag{1.7}$$

Here, V_g is the gate voltage, I_d is the drain current, *kT/q* is the thermal voltage, where *k* is Boltzmann's constant, *q* is the electron charge, and *T* is the temperature. C_{dep} and C_{ox} are the depletion and the oxide capacitance, respectively. *SS* value becomes 60mV/decade at room temperature when C_{ox} is infinite for ideal case of MOSFET. It reflects that at least 60 mV of gate voltage required to change the drain current by one order of magnitude when the transistor is operated in the sub threshold region. The sub threshold swing limitation of MOSFETs becomes limiting factor [34], [35] for further scaling of supply voltage below 0.5 V.

Thus in short, scaling down the supply voltage of conventional MOSFET is very difficult without significantly increasing the OFF-state current. To manage these severely constrained trade-off, the MOS devices must be specially designed with low power features in future generations of *ICs* and therefore, there is a need for ultra-low-power and energy-efficient transistors with steepest *SS*. Furthermore, the foremost corporate companies like TSMC, Samsung, and Intel, etc. are few among semiconductor companies, those are working towards the design and development of low power emerging devices used in consumer electronics product. In this regard, transistors based on interband tunneling mechanism such as Tunnel field effect transistor (TFET) considered as a promising novel device for future low-energy electronic circuits [36], [39].

1.2 Tunnel Field Effect Transistor (TFET)

Tunnel FET is being explored as a novel alternative device over conventional MOSFET for low-power application. This is because of the low *SS* of the Tunnel FET, which is not limited to 60 *mV/dec* at 300 K ($SS = (kT/q) \times ln10$) and produces low OFF current (I_{OFF}) unlike conventional MOSFET [41] [26]. It also exhibits high immunity to SCEs due to their charge carrier mechanism based on band to band tunneling (*BTBT*) over thermionic emission. Here BTBT means tunneling of minority charge carriers (electrons) from the valence band of the source to the conduction band of the channel-region in n-channel TFET. Note that Tunnel FETs have a high electric field in the channel, mainly in the tunneling region at the source end due to enhanced electric fields of the source than conventional MOSFET. Optimized Tunnel FET structure plays an important role in high tunneling probability at source/channel junction to enables low standby leakage currents on further scaling of supply voltage (V_{dd}) [12], [34], [35], [42], [43].

1.2.1 Working of TFET

TFET is merely a gated p-i-n diode working under reverse bias at low voltage (< 1 *V*). For TFET, ITRS-2018 targets for low power of 0.57 *V*, which is most important for low dynamic power of circuits and low power module of Internet of Things (*IoT*) applications. The drain is always biased with positive voltage to make sure the operation takes place in the reverse bias for gated p-i-n diode.

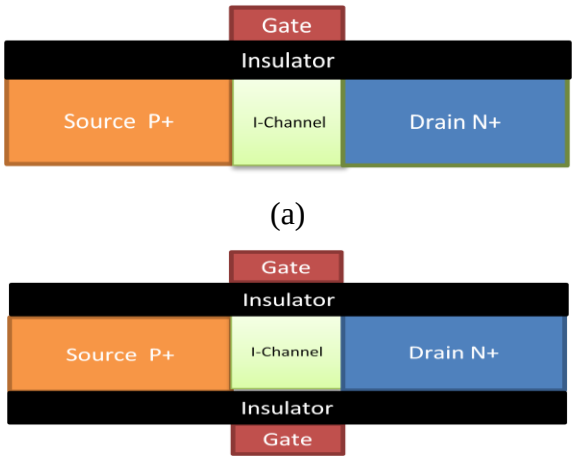


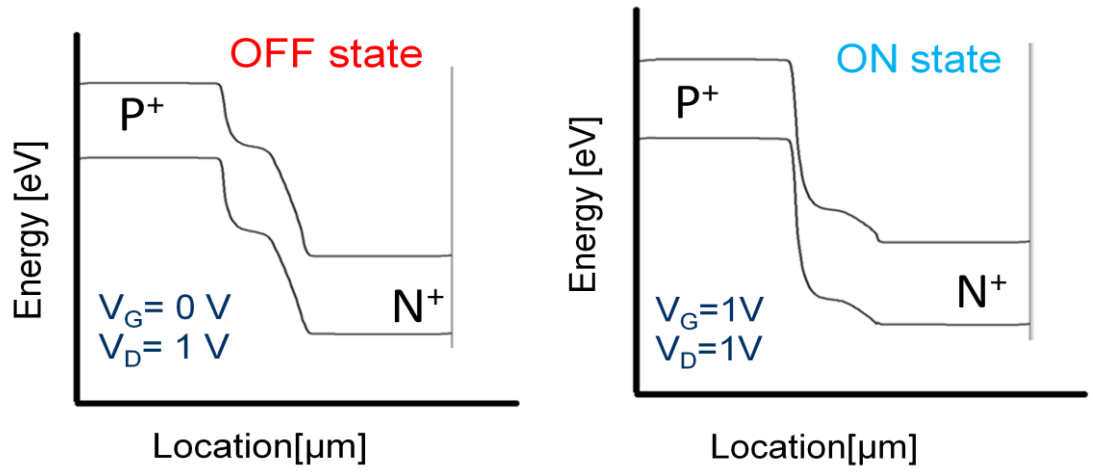
Figure 1.2 n-channel Tunnel FET device structure with (a) Single gate (SG), and (b) Double gate (DG)

In an n-type tunnel FET, n-region is referred to as its drain, and p+ region as its source, whereas for p-type Tunnel FET, the source would be doped n+ and the drain would be doped p+. The n-TFET operates when positive voltages are applied to the drain and gate. Further, Figure 1.2(a) and (b) shows the device structure of single and double gated n channel-Tunnel FET, respectively. The structures consist of p+ source and an n+ drain. The drain region is connected to the positive drain voltage (V_{DS}), whereas source region is grounded (0V).

1.2.1.1 OFF-state

The TFET is in OFF-state when the drain voltage $V_{ds} > 0$ and the gate voltage $V_{gs} = 0$, which is similar to the OFF-state of a MOSFET. In this state no BTBT occurs since the high depletion barrier width exists between the source and the channel as shown in Figure 1.3 (a). Further, any charge carriers present in the conduction band of the channel would have a tendency to drift to the drain and thus generates a current. However, as the source is p-type, very few free electrons in the conduction band exist and therefore very few electrons can be injected into the channel [44].

This leads to a negligible OFF-state current. Whereas in the case of a MOSFET, the source is n-type and has free electrons in its conduction band. During thermionic emission, a few electrons of conduction band will be injected into the channel over the potential barrier at the source-channel junction. This leads to a higher OFF-state in a MOSFET as compare to a Tunnel FET.



(a) (b)

Figure 1.3 Energy band diagram of n-channel Tunnel FET (a) during OFF state (b) during ON state.

1.2.1.2 ON-State

The TFET is in ON-state when the drain voltage $V_{ds} > 0$ and the gate voltage $V_{gs} > 0$, In this state, as we increase the gate voltage (V_{gs}), the energy bands in the channel change with respect to the source or the gate voltage pulls down the energy band of the channel region. The inter-band tunneling starts when bottom of the conduction band in the channel aligns with top of the valance band in the source. At a certain value of the gate voltage (V_{gs}), the valence band of the source get aligned with the conduction band in the channel since the gate voltage pulls down the energy band of the channel region and width of the tunnelling barrier reduces.

Therefore, charge carriers can tunnel from the valence band of the source to the conduction band of the channel region as shown in Figure 1.3 (b). As the gate bias is further increased, the bands in the channel are further lowered in energy, and electrons occupying energy levels from the valence band edge of the source to the conduction band edge of the channel can tunnel to the conduction band in the channel [44]. This leads to a steep increase in the current.

1.2.2 Wentzel Kramer's Brillion (WKB) approximation for TFET

The BTBT probability (T_{WKB}) is varying with the variation in I_{ON} of the TFET, which is defined by the Wentzel-Kramers-Brillouin (*WKB*) approximation [34], [36]. Band to band tunneling in tunnel FET through tunneling barrier can be approximated by a triangular potential barrier as shown in Figure 1.4 with the *WKB* approximation, the band to band tunneling transmission is given by:

$$T(E) = exp\left(-2\int_{x\ start}^{x\ end} k(x)dx\right) \tag{1.8}$$

T(E) is calculated with a two-band approximation for the evanescent wave vector, where *k(x)* is the quantum wave vector of the electron inside the barrier. Inside a triangular barrier, the quantum wave vector *k(x)* is represented as:

$$k(x) = \sqrt{\frac{2m^*}{h^2}(PE - E)} \tag{1.9}$$

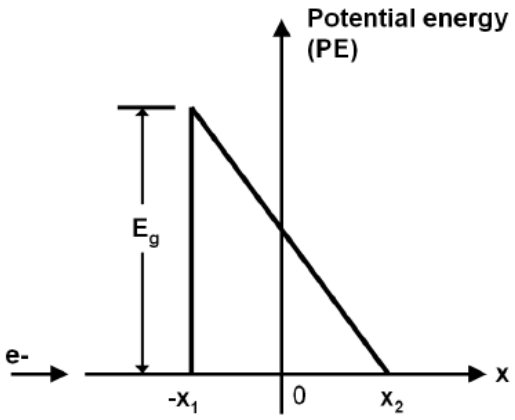


Figure 1.4 Triangular potential energy barrier approximation for band to band tunneling in TFET [45].

Here, PE is the potential energy, and E is the energy of incoming electron energy at the widest part of triangle, where *E=0 and PE* can be $E_g/2 - qE_x$ replaced by the equation for the triangle, E_x is the electric field. E_g is the band gap of the semiconductor material at the tunnel junction and E_x is the electric field.

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}\left(\frac{E_g}{2} - qF_x\right)}\,dx \tag{1.10}$$

On Putting the equation (1.10) in equation (1.8), we get the general expression for band to band tunneling Transmissions as follows:

$$I_{ON} \propto T_{WKB} \approx exp\left(\frac{-4\lambda\sqrt{2m^*}\sqrt[3]{E_g}\,)}{3q\hbar\left(E_g+\Delta\emptyset\right)}\right) \tag{1.11}$$

Here, λ is the geometrical-dependent tunneling length and m^* is the effective carrier mass. E_g is the energy band gap, q is the electron charge carrier, and $\Delta\emptyset$ represents energy difference between the valence band of the source and the conduction band of the channel. The WKB approximation, shown in equation (1.11) suggests that the E_g, m* and λ should be minimized for high barrier transparency.

In particular, Sze in [46] well-defined the drain current equation (1.12) in an interband tunneling transistor. He described that the drain current flows across a degenerated doped p^+-n^+ tunnel junction, whose transport mechanism in the reverse, Zener tunneling direction can also be written as:

$$I = a\, V_{eff} \xi \exp\left(-\frac{b}{\xi}\right) \tag{1.12}$$

Here, V_{eff} is the tunnel–junction bias, ξ is the electric field. a and b are the coefficients determined by the materials properties of the junction as follows:

$$a = Aq^3 \sqrt{2m^*/E}_g / 4\pi^2 \hbar^2$$

$$b = 4\sqrt{m^*}\, E_g^{3/2} / 3q\hbar$$

m^* is the carrier effective mass, E_g is the energy band gap, q is the electron charge, and h is Planck's constant divided by 2π. A is the cross-sectional area of the device.

1.2.3 Attributes and challenges of Tunnel FET

Despite the above advantages, the low ON current (I_{ON}) and ambipolar behavior (conduction at both polarities) are the two major limitations of the Tunnel FET [12], [47]. This is due to *BTBT* at both source channel and drain channel junctions. As discussed, the Tunnel FET is an ambipolar device, [34–36], which also conducts for $V_{gs} \leq V_{off}$ with *BTBT* occurring at metallurgical drain channel junction. To realize high tunneling current, the transmission probability of the source tunneling barrier should become close to unity for small change in gate voltage. It indicates, a high transparency of the tunneling barrier is required. Most importantly, this switch the device towards ON-state, only for energy window $\Delta\Phi$ as explained in *WKB* approximation in the previous subsection. This is mainly due to the electron in the tail of the Fermi distribution cannot tunnel because no empty states are available in the channel as their energy. This filtering function makes TFET possible to achieve an *SS* below the 60 *mV/dec*. Unlike MOSFET, *SS* in a TFET is not linear on a logarithmic scale and highly depends on the applied gate-to-source voltage. This is mainly due to the tunneling current depends on the transmission probability through the barrier as well as on the number of available states determined by the source and channel Fermi functions. The *SS* of tunnel FET is modeled by following equation [44].

$$SS = I\text{n } 10 \left[\frac{1}{V_{eff}} \frac{dV_{eff}}{dV_{gs}} + \frac{\xi+b}{\xi^2} \frac{d\xi}{d\,V_{gs}}\right]^{-1} \quad (1.13)$$

In order to achieve a low sub threshold swing, two terms in the denominator of equation (1.13) can be maximized and these terms are not limited by *kT/q*. Based on the first term, the transistor should be engineered so that the gate–source voltage directly controls the tunnel-junction bias (V_{eff}). In this concern, transistor geometry with a thin high-k gate dielectric and an ultrathin body to enable that the gate field directly modulates the channel. Further, for an equivalent oxide thickness approaching 1 nm, $dV_{eff}/dV_{gs} \approx 1$ and the first term in the denominator of equation (1.14) is inversely related to V_{gs}. Accordingly, the *SS* in a tunnel transistor increases with gate–source voltage, a characteristic that has been observed in both measurements [12] and simulations [10], [37] are given by the equation (1.14) as follows:

$$SS_{TFET} = \frac{V_{gs}^2}{5.75(V_{gs} + Const)} mV/_{dec} \quad (1.14)$$

This model equation (1.14) suggests that the subthreshold region does not appear as a linear line when I_{ds}-V_{gs} is plotted on a log scale as shown in Figure 1.1 (b), and the SS does not have one unique value. *SS* is smallest at the lowest V_{gs}, and increases as V_{gs} increases. Tunnel FET has two type of *SS* considered in the literature such as point subthreshold swing and average subthreshold swing due to nonlinear behavior in the subthreshold region. Point swing is the smallest value of the subthreshold swing anywhere on the I_{ds}-V_{gs} curve and average swing is taken from the point where the device starts to turn on, up to threshold, often defined using the constant current technique (10^{-7} Amp/μm).

Unlike MOSFET, gate capacitance formation of TFET is different in ON-state [39]. It was reported for a MOSFET, operating in the linear region, both source/drain regions are connected to the inversion layer and gate capacitance is equally contributed by gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}). In saturation region, C_{gg} is dominated by C_{gs}. However in TFET, the drain is connected to the inversion layer. Therefore, C_{gd} constitutes a larger fraction of C_{gg} in both linear and saturation regions.

Another issue with TFET, which leads to an increase of the OFF-current, is the presence of trap states within the band gap [48]. These states located at the junction impact the tunneling process. Typical kinds of traps are lattice point-defects which are caused by ion implantation damage. The relatively low activation temperature that was used does not heal all the lattice damage by crystal re-growth, so we assume there are a high number of defects in the implanted area that can act as traps. Traps in the source can be occupied by an electron due to the thermal broadening of the Fermi function. Electrons can tunnel from these traps directly into the valence band of the channel even for very low V_{ds} when no gate source voltage (V_{gs}) is applied and the bands of source and drain are not aligned. At lower temperatures these states are not occupied and do not contribute to the OFF-current, thus I_{OFF} decreases for lower temperatures. These traps states within the exponential Fermi tail contribute to the current flow, and thus they degrade the slope.

1.3 Simulation Tool

Simulations are required to optimize the device performance when hands on calculation and fabrication methods become too complicated or impose unacceptable assumptions. Sentaurus TCAD tool from Synopsys is an advanced commercial computational environment with a collection of tools, which is used for performing simulations of electronic devices and to understand advanced-device physics [49]. It also helps to investigate scaling analyses of device and may provide different design rules. In addition, it also allows us to interact with the fabrication methodology using process manufacturing. Importantly with a Sentaurus Synopsys 3D TCAD, the device behavior is obtained from the solution of the appropriate differential equations describing the device physics on a given geometrical domain. Here, the physics of the considered device is obtained from different models already available with the tool. After including the appropriate models, the considered device can be ramped with necessary electrical stimulation to get the final results. Furthermore, Synopsys Sentaurus 3D TCAD provides two methods for the device design:

1. **Device TCAD**: It deals with the modeling of electrical, thermal, optical and mechanical behavior of semiconductor devices.

2. **Process TCAD**: It aims to the modeling of semiconductor-chip process-manufacturing steps like lithography, deposition, etching, ion implantation, diffusion, oxidation, silicidation, mechanical stress, etc. In this thesis, we have worked with device Synopsys Sentaurus 3D TCAD for the modeling of electrical behavior of TFET devices. Further, different steps for Sentaurus simulations with device TCAD are given in Figure. 1.5.

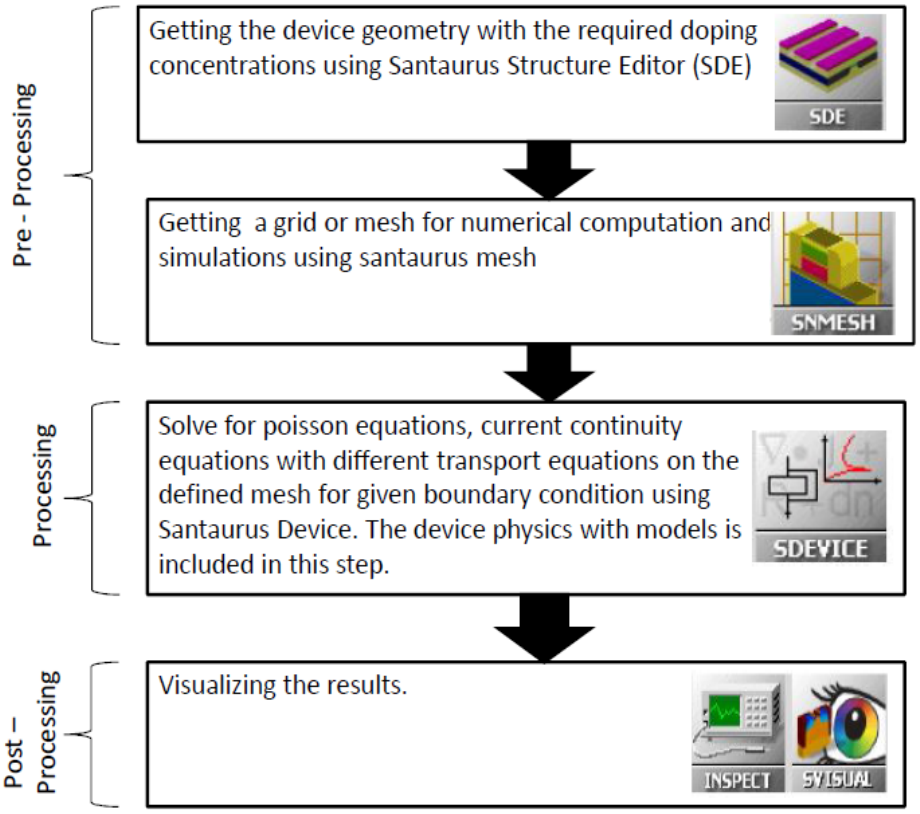


Figure 1.5: Device simulation steps with Synopsys Sentaurus Device TCAD [49].

1.3.1 Sentaurus Device

The description of deferent tools used for simulation with device TCAD can be given as follows:

1.3.1.1 Sentaurus Structure Editor (SDE)

Sentaurus Structure Editor can be used as a two-dimensional (2D) or three-dimensional (3D) structure editor. Here, the required structures are generated or

edited interactively using the graphical user interface (GUI). Doping profiles strategies for different regions of the considered device can also be defined with structure editor tool. In addition, Sentaurus Structure Editor provides an interface to call the Synopsys meshing tool i.e. Sentaurus Mesh to generate required grid points. Importantly, it provides the necessary input for the meshing tool and provides the way for the device simulation using Sentaurus Device.

1.3.1.2 Sentaurus Mesh (SNMESH)

Sentaurus Mesh is a mesh generator that produces rectangular or hexahedral elements for use in applications such as semiconductor device simulation, process simulation and electromagnetic simulation. The points where these elements intersect each other are known as the grid points. The physical equations of the considered device are solved corresponding to these grid points only. The mesh generation tools are composed of two mesh generators:

1.3.1.2.1 Sentaurus Mesh: Sentaurus Mesh is a robust mesh generator capable of producing axis-aligned meshes or grid points in 2D and 3D. In the 2D MOS type of devices, Sentaurus Mesh works is recommended. Importantly, the simulated devices where the most important surfaces are the axis aligned surfaces, Sentaurus mesh is used. Although Sentaurus Mesh works very well with MOS type devices, the effective and optimized numerical meshes in which the problem can be solved assuring convergence and, at the same time, with the reasonable simulation times, is a difficult to obtain. However, some general rules can be applied:

A. The grid spacing must be sufficiently dense so that all the relevant features of the geometry are accurately represented. However, it will increase the grid points and consequently the simulation time. Therefore, it is recommended that to create the most suitable mesh, the mesh must be densest in those regions of the device where High current density, High electric fields and High charge generation event occurs.

B. Points must be allocated to accurately approximate the physical quantities of interest.

1.3.1.3 Sentaurus Device (SDEVICE)

Sentaurus Device simulates numerically the electrical behavior of a semiconductor device in isolation or several physical devices combined in a circuit. The terminal currents, voltages, and charges are computed based on a set of physical device equations that describes the carrier distribution and conduction mechanisms. A real semiconductor device, such as a transistor, is represented in the simulator as a virtual device whose physical properties are discredited onto a no uniform grid points. Therefore, a virtual device is an approximation of a real device in Sentaurus TCAD. For this purpose, the Poisson equation with electron and hole continuity equation are solved using Newton iteration method for the whole range of electric stimulation with different physical models.

The SDEVICE has extensive set of models of physics for semiconductor devices, general support for different device geometries and mixed-mode support of electro-thermal net lists with mesh-based device models and SPICE circuit models. Importantly, in SDEVICE, continuous properties such as doping profiles are represented on the mesh and therefore, are only defined at a finite number of points. The doping at any point between these grid points (or any physical quantity calculated by SDEVICE) can be obtained by interpolation. The Sentaurus Device command can be organized in commands or sections that can be of any order. A Sentaurus Device command file has following sections:

1.3.1.3.1 File Section: File section consist \input files" that define the device structure i.e. .tdr file along with parameter .par file. In addition, the \output files" such as .plt, .log file are also defined in the file section for the simulation.

1.3.1.3.2 Electrode Section: With Sentaurus Device, it is necessary to specify which of the contacts are to be treated as electrodes. Electrodes in Sentaurus Device are defined by electrical boundary conditions and contain no mesh. Any contacts that are not defined as electrodes are ignored by Sentaurus Device.

1.3.1.3.3 Physics Section: The physics section of Sentaurus command file allows a selection of the physical models to be applied in the considered device simulation.

The selection of physical model strongly influences the accuracy of the simulation result.
The physical models used are explained in details later in this thesis:

1.3.1.3.4 Plot Section: The Plot section specifies all of the solution variables that are to be saved in the output plot files (.tdr). Only data that Sentaurus Device is able to compute, based on the selected physics models, is saved to a plot file.

1.3.1.3.5 Math Section: Sentaurus Device solves the device equations (which are essentially a set of partial differential equations) self-consistently, on the discrete mesh, in an iterative fashion. In this section, for each iteration, an error is calculated and Sentaurus Device attempts to converge on a solution that has an acceptably small error. For this purpose, one needs to define a few settings for the numeric solver in Math section.

1.3.1.3.6 Solve Section: The Solve section defines a sequence of solutions to be obtained by the solver. The Quasi-stationary command is used to ramp a device from one solution to another through the modification of its boundary conditions or parameter values in the solve section.

1.3.1.4 Sentaurus Visual (SVISUAL)

It is plotting software for visualizing data output from simulations. Sentaurus Visual enables users to work interactively with data using both a graphical user interface and a scripting language for automated tasks.

1.3.2 Simulation Methods

In device TCAD, following methods are available for electrical simulations of the device:

1.3.2.1 Study State Simulations

In steady-state conditions, for each property of the systems, its partial derivative with respect to time is zero, i.e. nothing is changing with time. To perform steady-state

simulations, the Sentaurus TCAD keyword is Quasistationary. The Quasi stationary command is used to ramp a device from a solution to another through the modification of the boundary conditions that can be Voltage, Current, or Temperature.

1.3.2.2 Transient Simulation

A transient response or natural response is the time-varying response of a system to a change from equilibrium. In Sentaurus, the keyword that must be used to perform transient simulation is "Transient". The command must start with a device that has already been solved under stationary conditions. The simulation then proceeds by iterating between incrementing times and re-solving the device.

1.3.2.3 AC simulations

Performing a small signal or AC analysis means simulate the behavior of system when a relatively small harmonic signal is superimposed to a steady-state condition or DC bias point. The keyword for AC analysis in Sentaurus SDEVICE is AC Coupled.

1.3.3 Physical Models

Synopsys Sentaurus TCAD tool others an extensive set of models to represent the virtual device as an approximation of the actual device. These models are included in the SDEVICE script for the considered device simulation. Some of the important models are listed as follows:

1.3.3.1 Carrier Transport Model

The entire carrier transport model supported by Sentaurus TCAD follows the charge conservation law in active region of the considered device. Here, carrier concentrations in any region of the device must never be negative during the Newton iteration. If during Newton iteration a concentration erroneously becomes negative, the tool provides the message that the Newton is not able to converge. After this, SDEVICE applies damping procedures (i.e. using the smaller step size) to make it positive. If the Newton iteration converges for the whole range of electrical stimulation, simulation gets complete. Here, following model for carrier transport is used in Sentaurus TCAD.

1.3.3.2 Generation Recombination Model

The drift diffusion model is used to calculate the electrostatic potential and electron/hole concentration. Apart from that the generation recombination processes are the methods that exchange carriers between the conduction band and the valence band. For each individual generation or recombination process, the electrons and holes involved appear or vanish at the same location. Following generation recombination models are used in this thesis.

1.3.3.3 Shockley Read Hall (SRH)

In general, recombination of charge carrier through deep defect levels in the gap is depicted as Shockley Read Hall recombination. Net recombination with SRH is dependent on the energy difference between defect level and intrinsic level, the carrier lifetime for electrons and holes, intrinsic concentration and electron/hole charge carrier density in the considered device. Hence, SRH model takes many important features of the simulated device into consideration. In addition, the electron and whole concentration with SRH is doping dependent, field dependent, and temperature dependent. Therefore, the SRH can be made to handle variability accounted from doping, electric field and temperature variation also. The generation recombination model can be selected in the physics section of Sentaurus Device command as an argument to the Recombination keyword i.e. Physics (Recombination (SRH (doping dependence...))...)).

$$R_{\text{net}}^{\text{SRH}} = \frac{np - n_{i,eff}^{l}}{\tau_p\,(n + n_1) + \tau_n (p + p_1)} \tag{1.15}$$

$$n_1 = n_{i,eff} \exp\left(\frac{E_{trap}}{kT}\right) \tag{1.16}$$

$$p_1 = n_{i,eff} \exp\frac{-\mathrm{E}_{trap}}{\mathrm{kT}} \tag{1.17}$$

Here, n, p, and $n_{i,eff}$ describe the electron, hole, and effective intrinsic density, respectively.

1.3.4 Mobility Model

Sentaurus Device uses a very modular approach for the explanation of the carrier motilities in the Sentaurus Device command file. For the simplest case, a constant mobility model is used with the undoped materials. For doped materials, the carriers

scatter with the impurities and this leads to the degradation of the mobility. To justify this effect, following mobility model can be used with doped materials:

1.3.4.1 Doping Dependent Mobility Degradation

In doped semiconductors, the scattering of charge carriers by impurity ions leads to the degradation of the carrier mobility. The model to justify this mobility degradation due to impurity scattering are activated by specifying the Doping Dependence on Mobility in the physics section of Sentaurus Device command file i.e. Physics (Mobility (Doping Dependence ...)).

If Doping Dependence is specified without options, Sentaurus Device uses a material dependent default model. In silicon material, the default doping dependent mobility model is the Masetti model where the mobility is given by the following equation:

$$\mu_{dop} = \mu_{min1} e^{-\left(\frac{p_c}{N_{A,0}+N_{D,0}}\right)} + \frac{\mu_{const}-\mu_{min2}}{1+\left((N_{A,0}+N_{D,0})/C_r\right)^{\alpha}} - \frac{\mu_1}{1+\left(\frac{C_s}{(N_{A,0}+N_{D,0})}\right)^{\beta}} \qquad (1.18)$$

Here, the motilities μ_{min1} , μ_{min2} and μ_1 are the reference motilities, which along with doping concentrations P_C, C_r, C_s, and their exponents are accessible in the parameter set Doping Dependence in parameter file.

1.3.4.2. Field Dependent Mobility Degradation

In high electric fields, the carrier drift velocity is no longer proportional to the electric field, instead, the velocity saturates to a finite speed v_{sat}. In Sentaurus device, actual field dependent mobility model is selected by the word High Field Saturation. To include high field saturation effect, default canal model is used in this thesis with default parameters applicable to the silicon material

1.3.5 Non-Local Tunneling

In non-local tunneling, the tunneling current depends on the band edge profile along the entire path between the points connected by tunneling. This means the electric field at each point in the tunneling path is dynamically changing. This makes tunneling a nonlocal process; hence model is dynamic non-local tunneling model. Previously, the local tunneling models were given by *Kanes, Hurkx* and *Schenk* assumed a constant electric field throughout the tunneling path. However, the

assumption fails to deliver the accurate results with tunneling. Therefore, the non-local tunneling model is included due to its properties as follows:

- Handles arbitrary barrier shapes.
- Includes carrier heating terms.
- Allows describing tunneling between the valence band and conduction band.
- Offers several different approximations for the tunneling probability.

Further, the specifications of trap distributions with non-local tunneling model arrive in the physics section of the device command file. In contrast to other models, most model parameters with non-local tunneling are specified in the device command file only. Importantly, using the physics section of the sentaurus device command file, traps can be coupled to nearby interfaces and contacts by tunneling. In this thesis, the non-local tunneling model is used to interface traps of nitride charge trap layer with channel-dielectric interface. In general, the non-local tunneling model requires the following:

1.3.5.1. Defining Non-local Mesh

The non-local mesh consists of non-local lines that represent the tunneling paths for the charge carriers. To control the construction of the nonlocal mesh, Sentaurus Device uses the keyword Non Local in math section of the device command file. The construction of non-local mesh can be controlled by using Length and Permeation parameters. Further, for the definition, the keyword Non Local specifies the barrier region over which the non-local mesh has to be defined. The non-local lines form a box over the barrier, and connect the upper vertices and lower interface for tunneling. Further, Sentaurus device introduces a coordinate along each Non local line. The interface is at coordinate zero, the vertex for which the nonlocal line is constructed is at a positive coordinate.

1.3.5.2. Non-Local Tunneling Model

The nonlocal tunneling model is activated and controlled in the Physics section of the device command file. Non-local tunneling model is specified by keyword *e* Barrier Tunneling and h Barrier Tunneling as shown in Figure 1.6.

Here, *e* Barrier tunneling defines all electrons tunneling to the conduction band at the lower point from the conduction band at the upper point. Similarly, *h* Barrier

Tunneling causes all whole tunneling to the valance band at the lower point from the valance band at the upper point. Here, valance to conduction band component has been discarded.

The computation of the tunneling probabilities (for carriers tunneling to the V_t shifted conduction band at the interface or contact) and (for tunneling to the V_t shifted valence band) is, by default, based on the *WKB* approximation. The *WKB* approximation uses the local (imaginary) wave numbers of particles at position and with energy:

$$k_{C,v}r,\varepsilon = \sqrt{2\, m_C(r)\left|E_{C,v}\,(r) - \ \varepsilon\right|}\ \ominus \frac{\left[E_{C,v}(r)-\varepsilon\right]}{\hbar} \tag{1.19}$$

$$k_{V,v},r,\varepsilon = \sqrt{2\, m_V(r)\left|\varepsilon - E_{V,v}\,(r)\right|}\ominus \frac{\left[E_{V,v}(r)-\varepsilon\right]}{\hbar} \tag{1.20}$$

Where, m_C is the conduction-band tunneling mass and m_V is the valence-band tunneling mass.

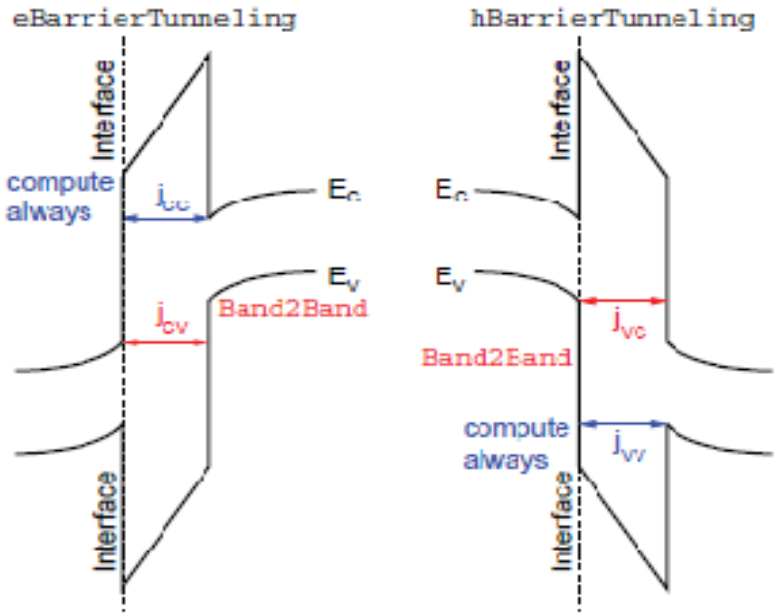


Figure 1.6: Non-local Tunneling [49].

Both tunneling masses are adjustable parameters) and $E_{C,v}$ *and* $E_{V,v}$ are the conduction and valence bands energies shifted by the fifth value in e_{offset} and h_{offset}.

Using the local wave numbers and the interface transmission coefficients $T_{CC,v,}$ $T_{VV,v}$ and, the tunneling probability between positions for a particle with energy can be written as:

$$\Gamma_{CC,v}(u,l,\varepsilon) = T_{CC,v}(l,\varepsilon)\exp\left(-2\int_l^u K_{C,v}(r,\varepsilon)dr\right)T_{CC,v}(u,\varepsilon) \quad (1.21)$$

$$\Gamma_{VV,v}(u,l,\varepsilon) = T_{VV,v}(l,\varepsilon)\exp\left(-2\int_l^u K_{V,v}(r,\varepsilon)dr\right)T_{VV,v}(u,\varepsilon) \quad (1.22)$$

1.3.5.3 Non-Local Tunneling Parameter

The nonlocal tunneling model has several fit parameters. Therefore, tunneling masses are either specified in region-specific or material-specific parameter sets. The definition of tunneling masses can take the following form:

Material = "Oxide"(Barrier Tunneling (m_t = 0:42; 1:0))

This equation specifies the electron tunneling mass as $0.42m_0$ and hole tunneling mass as $1m_0$. The non-local tunneling model has several fit parameters, which specified in the barrier tunneling parameter file are mass of electrons (m_e) and mass of holes (m_h). These masses are properties of the materials that form the tunneling barrier. In case of silicon, it has been taken as 0.32 and 0.54, respectively, $A_{path} = A = 4\times10^{14}$ $cm^{-3}s^{-1}$, and $B_{path} = B = 1.9\times10^{7}$ Vcm^{-1}, Here A and B are material dependent parameters. The values of other parameters for the nonlocal model are kept to their default value as projected for silicon (*Si*), since the tunneling process is nonlocal therefore this model requires a special fine mesh to be applied around the area where tunneling can take place. Syntax of some parameter file is as follows:

```
Material = “Silicon" {
Band 2 Band Tunneling
{
    A_gen = 4e14 # [1/ (cm^3s)]
    B_gen = 1.9e7 # [V/cm]
    P_gen = 0.037   # [1]
    alpha = 0    # [1]
}
Barrier Tunneling {
m_t = 0.322, 0.549
}}
```

1.3.6 Nonlocal Path Trap-assisted Tunneling (TAT)

Sentaurus device provides dynamic nonlocal path Schenk and Hurkx TAT models. These models take into account nonlocal TAT processes with the *WKB* transmission coefficient based on the exact tunneling barrier. In this model, electrons and holes are captured in or emitted from the defect level at different locations by the phonon-assisted tunneling process. As a result, the position-dependent electron and hole recombination rates as well as the recombination rate at the defect level are all different. For each location and for each carrier type, the tunneling path is determined dynamically based on the energy band profile rather than predefined by the nonlocal mesh. Therefore, the present models do not require user's specification of the nonlocal mesh.

1.4 Cylindrical (Cyl) Gate-all-around (GAA) Tunnel FET

Among all planar and *MuG*-structures of Tunnel FET limits the further scaling of devices due to shrinkage in BTBT causes reduction in device performance. In this prospect, 3D Cyl GAA-TFET structures with small nanowire dimensions are expected to have a beneficial impact on the tunneling behavior suitable for low power analog/*RF* applications [50]. This is because of their low screening length (λ), highest degree of electrostatic gate control over the channel, robustness against *SCEs*, better scaling options, no floating body effect, larger number of equivalent number of gates (ENG), ideal sub threshold slope, no confinement of carriers near to oxide-semiconductor interface when compared to other multiple-gate MOSFETs [51]. Note that in GAA-TFET, the gate of the device is wrapped all around the channel, which increases the tunneling rate between source/channel junction and significantly, supports for high driving current [52] as shown in Figure 1.7. Hence in GAA-TFET, the gate electric field penetrates the body center, and inversion charge exists throughout the body.

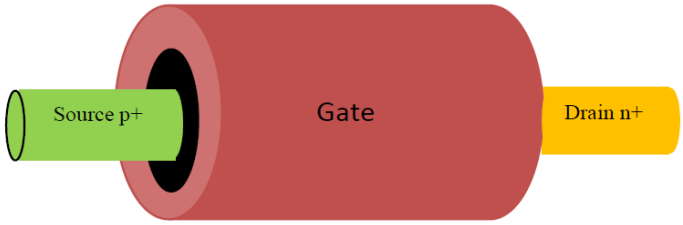


Figure 1.7 3D view of Cylindrical (Cyl) Gate-all-around (GAA) n-channel TFET

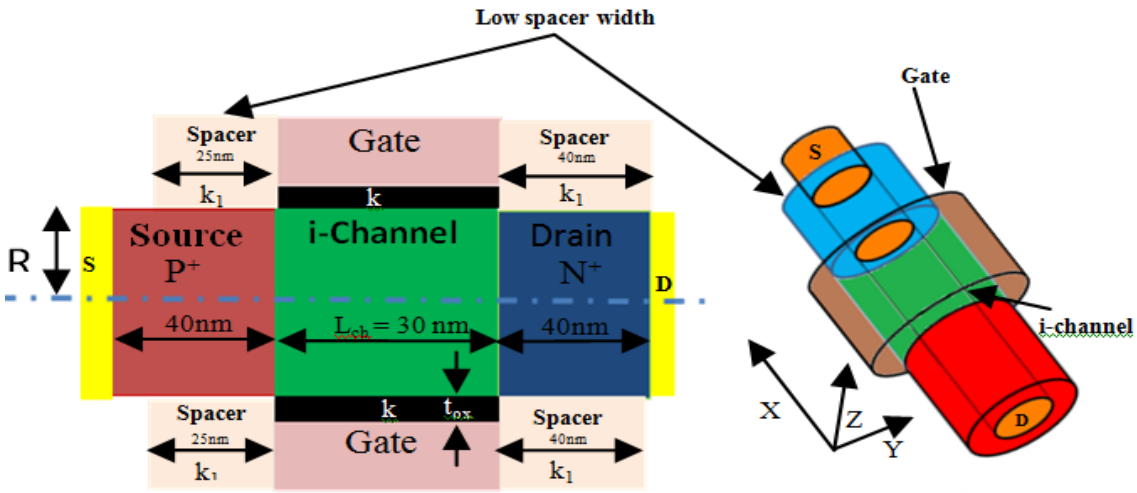
Further, the transconductance (g_m), intrinsic gain, transconductance generation factor (g_m/I_d) ,output resistance, ON-state current (I_{ON}), and parasitic capacitances *(C_{gs}, C_{gd}, and C_{gg})* are figures of merit for both analog and DC performance, while the cut-off frequency (f_t), maximum oscillation frequency *(f_{max})* and gain bandwidth product *(GBW)* are key figures of merit for RF circuit design, The transconductance generation factor is also a key parameter in design of analog circuits that measures the transconductance generation efficiency. It shows the available gain per unit value of power dissipation because g_m represents the gain, I_d represents the power dissipated to obtain that amplification. However, the excellent short channel behavior of GAA TFET helps to reduce the output conductance. In case of RF analysis, f_t is defined as the frequency when the current gain is unity, while f_{max} is the frequency when the power gain is unity. As continuous scaling of the minimum channel length, consequently increases f_t and have made Cyl GAA-TFET as an attractive option for wireless communication and low power analog/RF application.

1.5 Motivation

The demand for low power circuit escort innovative use of low OFF current devices. In this regard, various structures and materials with novel ideas have been proposed. Among them double-gate TFET with high-k gate dielectric in [44] is one of the efficient structure to achieve the merits of fringing field [42]. Also, Jhan *et al*. in [53] proposed nanowire TFET with asymmetry gate for high I_{ON}. Note that Tunnel FETs have a high electric field in the channel, mainly in the tunneling region at the source end due to enhanced electric fields of the source than conventional MOSFET. Few researchers have also worked on TFET devices with optimization of source/drain underlap to suppressed ambipolar characteristics. Besides, Anghel *et al.* [54] proposed

underlap in gate and drain to suppress ambipolar characteristics and Lee *et al*. in [55] predicted that drain underlap on GAA-TFET improve the I_{OFF}. However, they also found that channel length (L_{ch}) scale below 40 nm causes a gradual decrease in driving current and significantly degraded I_{ON}/I_{OFF} ratio and *SS*. It is also a major hurdle for device performance in terms of DC and analog/RF characteristics. Moreover, other approaches actually increase drain to source channel length, and significantly reduces chip density.

Further, the hetero-gate dielectric approach was also employed for the improved device performance [56–58]. Although limited to analyze the impact of hetero-spacer on the GAA Tunnel FET. In addition to this, Anghel *et al.* and Chattopadhyay *et al.* analyzed that low-k spacer with high-k gate dielectric are responsible to enhance ON current [54], [59]. However they were limited in further detail investigations of spacer engineering. Note that spacers are insulator required for isolation to prevent carrier leakage over the gate edge, and thus the structure with placement of tuned spacer plays a vital role in high BTBT across source-channel junction with non-depletion of the source/drain fringing field towards the edge of the gate. Further, most of the discuss works are based on planar technology, which limits the device performances for circuit applications.



(a) (b)

Figure 1.8 (a) Cross-Sectional view, and (b) 3D view of Cylindrical Gate-All-Around n-channel Tunnel FET based on low spacer width (LSW) along channel length direction. Here S-Source, D-Drain, C-Channel, R-radius and k and k1 are the gate/spacer dielectric.

In this regard, an optimized 3D structure that can improve driving current as well as analog/RF characteristics without an increase in I_{OFF} is of great importance for low

power module of *IoT* applications. Therefore, in this thesis, we will optimize the design and explore methods to improve analog/RF performances 3D Cylindrical GAA Tunnel FET structure, whose cross-sectional and 3D View are shown in Figure 1.8 (a) and (b). Further, we have extended our analysis towards the circuit design for low power cross coupled voltage doubler (*CCVD*) using a spacer and underlap engineering. Initially, we have investigated the comparative performances of three optimized structures of 3D Cyl GAA TFET in terms of DC characteristics such as I_{ON}, I_{OFF}, *SS,* and I_{ON}/I_{OFF} [52]. In this work, we employed the concept of spacer and asymmetry in underlap (*AU*) using 3D Synopsys Sentaurus TCAD. The design and physics of the examined device were mainly focused to achieve low sub threshold leakage current and ambipolar behavior without affecting high $I_{ON.}$ Here, we have design the underlap structure using shifting or change in the coordinate value of gate length while constant the other remaining geometrical parameters constant i.e. drain, source and channel length. Thus, the proposed *AU* method does not increase drain to source channel length, which is a significant factor for high chip density and reduces the complexity of fabrication using CMOS compatible flow.

In addition, the merits of low band gap material are also employed for high *BTBT*, which is significant for high merits of analog/RF behavior. Recently, Kim *et al.* in [60] proposed Germanium (*Ge*)-source TFET applications. Besides, Kao *et al.* proposed the direct and indirect BTBT in Ge-TFETs in [61] and also analyzed the modeling approach for tensile strained Ge-TFET [62]. The Ge-source design achieves much higher ON-state drive current (I_{ON}) due to narrow band gap and high BTBT rate as compared to *Si* for high analog/RF characteristics. However, it causes high leakage current known as OFF state current (I_{OFF}) due to their large intrinsic charge carrier concentration. At small gate biases, the lateral tunneling at the drain-channel junction was a dominant factor due to low band gap, which effectively increases the OFF-state (leakage current). Thus, it is difficult to satisfy the performance requirement of low power application by using small band gap hetero-junction only. In this context, a trade-off exists between an analog/*RF* characteristics and leakage current.

To overcome the above issues, a drain underlap (*DU*) 3D Cyl GAA TFET based on Ge-source with hetero-spacer dielectric is being presented as an alternative to the conventional Tunnel FET devices for high merits of analog/*RF* performances such as C_{gs}, C_{gd}, g_m, cut-off frequency (f_t) and maximum oscillation frequency (f_{max}). Further,

it has been found that the examined device of underlap structure based on Ge-source with hetero-spacer reduces the leakage current and produces the superior analog/*RF* Performances. Here, hetero-spacer dielectric (HTS) comprises of different spacer dielectric at the drain and source side, respectively i.e. low-k spacer is placed over source side of the gate and high-k spacer is placed across drain side to improve the fringing field across the surface.

Despite of high performances, device reliability is also a major concern. Previously, most of the works have been investigated, assuming an ideal direct tunneling in semiconductor body without any defects. Thus, the works was not adequately addressed the non-idealities behavior within the semiconductor body [63]. Note that during the device fabrication, it induces phonons and radiations that damage the results in the conception of interface defects assisted tunneling causes a reduction in device reliability and lifetime. Therefore, in this thesis, we have also investigated the impact of trap-assisted tunneling (*TAT*) on Cyl GAA-Tunnel FET based on hetero-spacer engineering for improved device reliability. In this work, we have considered experimental nonidealities such as interface defects and phonons while included the *TAT* model in the 3D simulations of the examined device.

Furthermore, the Tunnel FET has recently gained massive research interest owing to its application in Internet of Things (*IoT*). Since *IoT* era promotes low power design, high driving, process optimization, and smart peripherals with improved reliability approach within device, circuits to architecture levels. In particular, such designs are best suitable for the utilization at remote location for longer period. Furthermore, *IoT* system needs high speed with high energy efficiency design based on low power device [64]. Recently, many researchers have been specifically focus towards the development of smart and small devices with their peripheral circuit to the external world for emerging *IoT* [43], [65]. However, very few works have been directed their attention towards the applications of TFET for driving the target system.

In this regard, the cross coupled voltage doubler is the most suitable circuit for the requirement of applications that used as energy harvesting circuit with *IoT* system at remote locations. It can be used to enhance the available low supply voltage up to required supply voltage to operate the system. In short, the *CCVD* is basically a type of switched capacitor DC-DC converter in which the output voltage is about twice of the input voltage. It also reduces the ripple in voltage with the same frequency as

compared to the conventional charge pump [66]. This is mostly used with DC to DC converter over small battery source to power the applications.

The efficiency of the voltage doubler leads to low power dissipation and higher switching speed over conventional CMOS technology [67]. However, the power efficiency of the *CCVD* is limited due to reversion loss. The charges move from higher voltage nodes to lower voltage nodes causes the output voltage to deviate from its ideal boosting level with switching ripple are known as reversion loss. Although, the topology has been an issue of voltage drop due to high threshold voltage of the diode. The similar topology was implemented using MOSFETs in [68] even though, it has a similar issue of voltage drop. In addition, the issue has been overcome using *CCVD* [69], although it has high on chip resistance and reversion loss. Further, to overcome the issue of reversion loss, an area-efficient *CCVD* with no reversion loss using first-level gate-control mechanism was presented by Mui *et al.* [66]. Moreover, authors implemented the work on 350 nm CMOS technology. The cross-coupled voltage multiplier based on CMOS for boost DC to DC converter applications was proposed by Yu *et al*. in [70].

Furthermore, Kim *et al.* in [71] proposed the transfer blocking technique which has no reversion loss. However, all of the above designs are based on conventional MOSFET technology that reflects an issue of high power consumption. Therefore, low power device plays an important role to power such systems having limited energy capacity of batteries or to increases the lifetime of batteries. Therefore, we have comprehensively investigated the circuit performance parameters of the *CCVD* based on 3D Cyl GAA-TFET using device circuit co-design approach. This cross-coupled DC-DC converter reduces the reversion leakage loss and increases the power efficiency using HSPICE and 3D TCAD mixed-mode simulation. In addition, it also reduces the significant power loss and increases the conversion efficiency along with very small energy consumption. It can also be used for many other applications such as DRAM memories, wireless and implantable circuits to obtain various values of supply voltage from single fixed voltage supply. Accordingly, we have used the proposed device to design and develop a cross coupled voltage doubler for *IoT* applications.

1.5.1 Research Objectives

- Device optimization of Cylindrical (Cyl) Gate-all-around (GAA) Tunnel FET for improved ON-current and suppress OFF-current using spacer and underlap engineering.
- Attributes of analog/*RF* performances of the 3D Cyl GAA TFET based on hetero-spacer and band-gap engineering as well as distinct device geometry.
- Impact of trap assisted tunneling on the proposed device for improved device reliability.
- Circuit analysis of low power cross coupled voltage doubler circuit (*CCVD*) based on the proposed device for low power module of *IoT* applications.

1.6 Thesis Outline

This thesis aims to investigate the performance of 3D Cyl GAA Tunnel FET from device level to circuit level. In particular, Chapter 2, 3 and 4 analyze the performance of 3D Cyl GAA-Tunnel FET in terms of DC and analog/*RF* characteristics with improved reliability, whereas Chapter 4 examines the Circuit performance of the proposed device, whose specific details are as follows.

Chapter 1: Introduction and thesis outline: This chapter presents a brief introduction about the MOSFET and TFET, merits of TFET, tunneling mechanism, architectural classification of Tunnel FETs, various important parameters to be considered while optimization of the proposed 3D Cylindrical (Cyl) Gate all around (GAA) TFET structure, motivation of the work and the various contributions in the thesis.

Chapter 2: Device design and analysis of 3D Cyl GAA-TFET using spacer engineering: In this chapter, we have investigated the comparative analysis of three optimized structures of 3D Cyl GAA Tunnel FET in terms of DC characteristics such as I_{ON}, I_{OFF}, *SS,* and I_{ON}/I_{OFF} using 3D Synopsys TCAD to overcome the limitations of the device using spacer engineering. Further, we have also extended our analysis towards the asymmetric underlap structure of 3D Tunnel FET device. It has

been found that drain underlap with low spacer width produces the best device performance in terms of DC characteristics.

Chapter 3: Attributes of analog/RF performance of the 3D Cyl GAA-TFET: This chapter presents the comparative investigations of the analog/RF performance parameters such as C_{gs}, C_{gd}, transconductance (g_m), cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) for the examined three structures. Further, it has been found that the examined device of underlap structure based on Ge-source with hetero-spacer dielectric reduces the fringing field and produces the superior analog/*RF* Performances.

Chapter 4: Impact of trap assisted tunneling (TAT) on 3D Cyl GAA-TFET for improved device reliability: In this chapter, we have investigated the impact of trap assisted tunneling (*TAT*) on 3D Cyl GAA TFET. The device under study was based on hetero-spacer and asymmetric underlap engineering to enhance the device performance with improved reliability. Here, the impact of trap charges has been studied, which include the physical model of *TAT* for the validation of experimental/fabrication results.

Chapter 5: Performance analysis of cross coupled voltage doubler (*CCVD*) circuit based on 3D Cyl GAA-TFET using device circuit co-design approach: In this chapter, we have analyzed the circuit performance of *CCVD* circuit based on 3D Cyl GAA-TFET at low drain voltage for *IoT* applications using device circuit co-design approach. Further, the considered device based on Ge-source with low spacer width for high performance parameters. The investigated circuit of *CCVD* achieves the power efficiency up to 95.4% implemented using HSPICE simulation. Further, we have extended circuit analysis of the proposed circuit for the output voltage, energy consumption, and life performances.

Chapter 6: Conclusions and future scope: This chapter summarizes all the contributions made in the thesis and presents conclusions and future research direction.

CHAPTER 2

Device Design and Analysis of 3D Cylindrical (Cyl) Gate-All-Around (GAA) Tunnel FET using Spacer Engineering

As discussed in previous chapter, the ongoing downsizing of the MOSFET in nanometer regime resulted in severe *SCEs*, which promote high leakage and significantly degrade the device performance in terms of DC characteristics. In this regard, Tunnel FET appears as a prominent novel device and alternative of MOSFET for low-power applications.

Asymmetric source/drain doping engineering in Tunnel FET suppresses ambipolar conduction. However, Tunnel FET suffers from low ON current [3] due to different conduction concept as compare to conventional MOSFET. This causes degradation in analog/*RF* performances and consequently limited utilization of Tunnel FET for low power applications. It was also reported that leakage current is a dominating factor in nanometer dimension [26]. So drain design optimization is an important concern for improving the device performance and its RF figures of merit without increase in OFF-state current. In addition spacer engineering plays an important impact on the TFET for the improved DC characteristics. Please note that spacers are basically insulator required for isolation to prevent carrier leakage over the gate edge. Based on the literature of fabricated device [43], [64], spacers prevent source/drain dopants from being implanted through any thinner faceted regions.

Therefore, in this chapter, a comparative investigation on the three structures of Cylindrical (Cyl) Gate-all-around (GAA) Tunnel FET has been made for the improvement of driving current and associated parameters. Here impacts of spacer and underlap engineering have been analyzed for the improvement of the device performances. We have investigated the examined devices in terms of DC characteristics such as I_{ON}, I_{OFF}, *SS*, and I_{ON}/I_{OFF}. Besides, we evaluated the influence of asymmetrical spacer (*AS*) width on 3D Cyl GAA-n-channel TFET with same equivalent oxide thickness and compared the performance with symmetrical spacer width. Here in *AS* width means low spacer width is placed over source region, while high spacer width is placed over drain region. It turns out that the fringing field effect

with asymmetrical spacer width produces a high I_{ON} when compared with the device based on symmetrical spacer width. Finally, for the improvement of high analog/RF Performances, we have also investigated the device performance based on low band gap material such as *Ge*.

2.1 Device Design based on Spacer and Underlap Engineering

We have investigated the three structures of 3D Cyl GAA-Tunnel FET using spacer and underlap engineering. Here it is demonstrated that the asymmetrical underlap (*AU*) with low spacer width suppresses the ambipolar behavior, and OFF state current with steepest *SS*. This is because of low spacer width (LSW) placed over source region causes a reduction in the width of depletion region, improves the driving current characteristics, and consequently beneficial for high analog/RF characteristics. Further, some researchers shows the fabrication steps of GAA structures based on silicon [72–74], [50] and germanium [75], [76]. However, the most important property of the proposed device is that it reduces the complexity of fabrication. Here, due to all around cylindrical symmetry across the source, drain, and channel, it can be easily process as compared to other existing GAA structures. Choi *et al* in [56] proposed heterogate gate structure. While Jhan *et al* in [53] proposed source side as nanowire structure and drain side as planar structure, whereas in [77] proposed a gate source as arc based structure. All of these structures are asymmetrical in geometrical feature, which is complex to process**.** In our work, asymmetric Source/Drain has been used in terms of spacer material only. Further, symmetrical source/drain of GAA-TFET has been used for geometrical specification of the structure, which support for ease of fabrication.

2.1.1 Device Structure and Analysis

3D Cyl GAA-Tunnel FETs is merely a gated-all-around p-i-n diode operating under a reverse bias as shown in Figure 2.1 (a), (b), and (c).

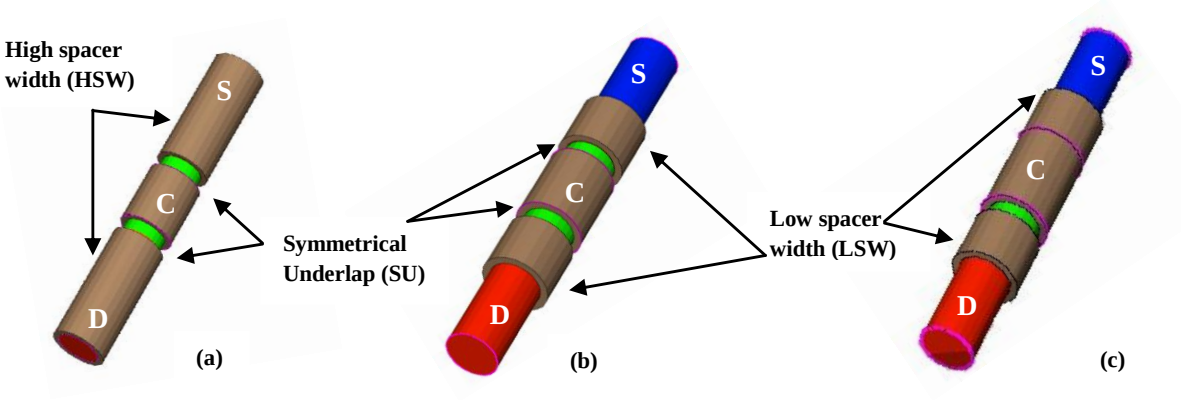


Figure 2.1 3D views of Cyl GAA Tunnel-FET, (a) Symmetrical underlap (*SU*) with full spacer width (FSW), (b) *SU* with low spacer width (*LSW*), and (c) Asymmetrical underlap with *LSW*. Here S-Source, D-Drain, and C-Channel.

The examined device has following parameters; asymmetrical doping profile is used for source, channel and drain region to make abrupt junction. P-type source ($1\times10^{20}/cm^3$), n-type drain ($5\times10^{18}/cm^3$), and p-type channel region ($10^{17}/cm^3$) as shown in Figure 2.2 (a), (b), and (c) with magnitude of doping concentrations. Because of increased oxide capacitance, HfO_2 is used as a gate dielectric as well as spacer dielectric (k=25) with gate work function = 4.53 e*V* [52].

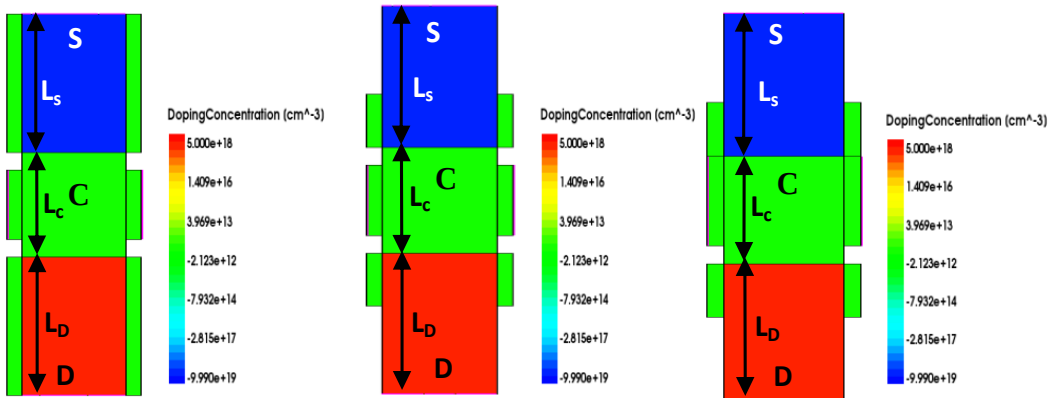


Figure 2.2 Cross-sectional views of Cyl-GAA-TFETs along channel length direction with magnitude of doping concentration. (a) *SU-FSW*, (b) *SU- LSW*, (c) *AU-LSW*. Here L_d, L_s, and L_{ch} represents the drain, source and channel length.

Here, the use of low work function material of gate electrode and source pocket creates a band bending on the channel/source interface, which leads to enhancement in the ON state current of the device, reflects in the analog/RF parameters. Whereas the use of high work function on the drain side of gate material increases the depletion width at drain/channel section, results into decrement in the leakage current. This is lateral silicon nanowires. Here, cross-sectional GAA devices are presented in the vertical figures due to simultaneous close comparison of three GAA structures.

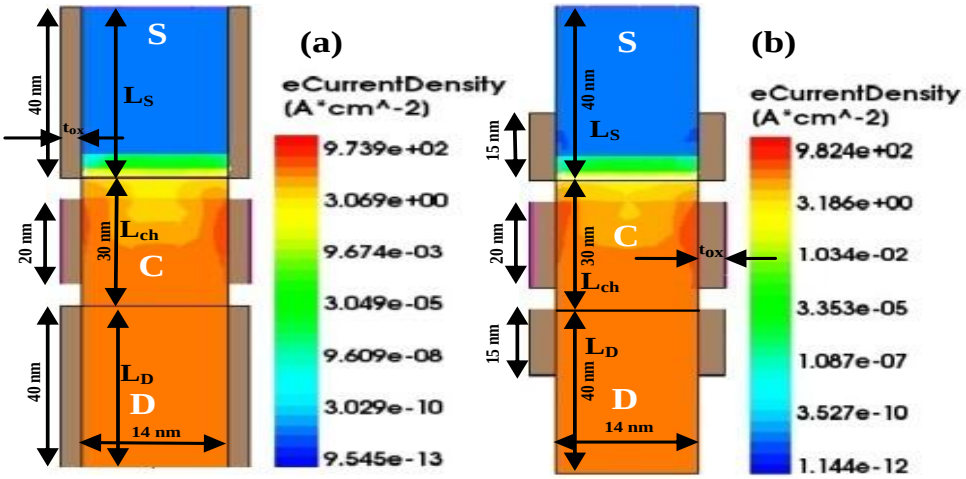


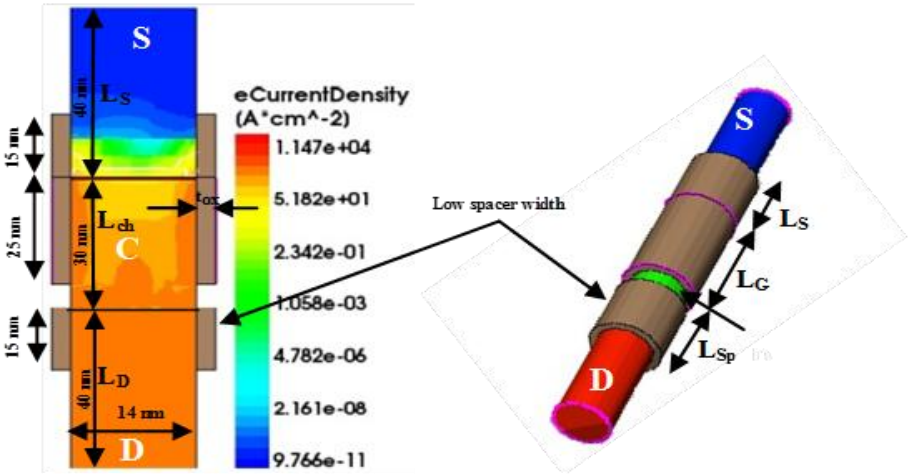
Figure 2.3 Cross-sectional views of symmetrical underlap (SU) Cyl-GAA-TFETs with (a) full spacer width (FSW), and (b) low spacer width (LSW) along channel length direction with magnitude of electron (*e*) current density.

Furthermore, Figure 2.3 shows the cross-sectional views of Cyl GAA-n channel Tunnel FET (a) symmetrical underlap (SU), i.e. identical underlap across source and drain with full and (b) low spacer width (F/LSW), respectively. In addition, Figure 2.4 (a) and (b) shows the cross-sectional, and 3D view of asymmetric underlap of Cyl GAA-nTFET with low spacer width (LSW). For fair comparison, we have used the same device parameters such as gate dielectric (k), gate work function, and doping concentrations with the same gate source voltage (V_{gs}) scale for all the three structures, respectively.

Generally, it has been found that formation of high-k dielectric layer on Si surface without oxide layer increases interface trap charges. However, the case literature is applicable for the case of MOSFET. Since the gate dielectric is confined to the channel region, this is known to lead particularly to fringing fields, which are known to deteriorate device performance in the case of the conventional MOSFET. Their

effect on the tunnel FET will be evaluated in this work. It turns out that the fringing field improve the characteristic of the TFET significantly, which can be attributed to the totally different working principle of TFET [42]. Moreover, we have assumed ohmic contacts at the source and drain regions and therefore, we have not considered the presence of interface traps at the germanium- silicon interface in our simulations as done in the previous works [78]

The values of the threshold voltage (V_t) is extracted using constant current method (10^{-7} A/μm) and found to be 0.81 V, 0.72 V, 0.62 V for the three structures, respectively.



(a) (b)

Figure 2.4 (a) Cross-sectional view, and (b) 3-D view of asymmetrical underlap (*AU*)-Cyl GAA-TFET with *LSW*. Here, gate length (L_g) =25 nm, spacer width (L_s) = 15 nm, oxide thickness (t_{ox}) = 2 nm is used.

2.1.2 Simulation Model and Parameters

The results presented in this work are obtained by using a non-local BTBT model combined with a Shockley-Read-Hall (SRH) recombination, field-dependent mobility, and band gap narrowing (BGN) model performed by three-dimensional device simulations using Synopsys Sdevice [42] and same simulation models are validated using [37]. The existing parameters involved in the calibration of nonlocal BTBT model are mass of electrons (m_e) and mass of holes (m_h) for *Si*, which have been taken as 0.32 and 0.54, respectively. A_{path} = A = 4×10^{14}/cm^{3}s, and B_{path} = B = 1.9×10^7 V/cm. Here, A and B are material dependent parameters. The values of other parameters for the nonlocal model are kept to their default value as projected for *Si*,

since the tunneling process is nonlocal therefore this model requires a special fine mesh to be applied around the area where tunneling can take place.

Initially, the proposed device has been calibrated with the experimental data of [79]. This is shown well in Figure 2.5. Further, the presented method uses spacer engineering to improve fringing field across the surface with asymmetry in underlap. Extensively, simulation results show that asymmetrical underlap of GAA-TFET with low spacer width enhances the fringing field within the spacer. The proposed device structure has high I_{ON} (6.9×10^{-4} A/μm), low I_{OFF} (2.5×10^{-17} A/μm), and an enhanced I_{ON}/I_{OFF} (10^{13}) as shown in Figure 2.6. This is due to low-k spacer width placed over a small distance causes non-depletion of fringing field of the source towards edge of the gate, which leads to carrier tunneling at the surface only and not inside the body, as a result enhanced the electric field, decreases the tunneling barrier width, significantly, leads to high source channel tunneling rate and significantly, high I_{ON} has been achieved [35]. At the same time, low I_{OFF} was maintained due to the high series resistance at drain channel junction caused by AU. Furthermore, the proposed structure exhibits a steepest *SS* (*30mV/dec*) when compared with SU- Cyl GAA TFET based on high and low spacer width.

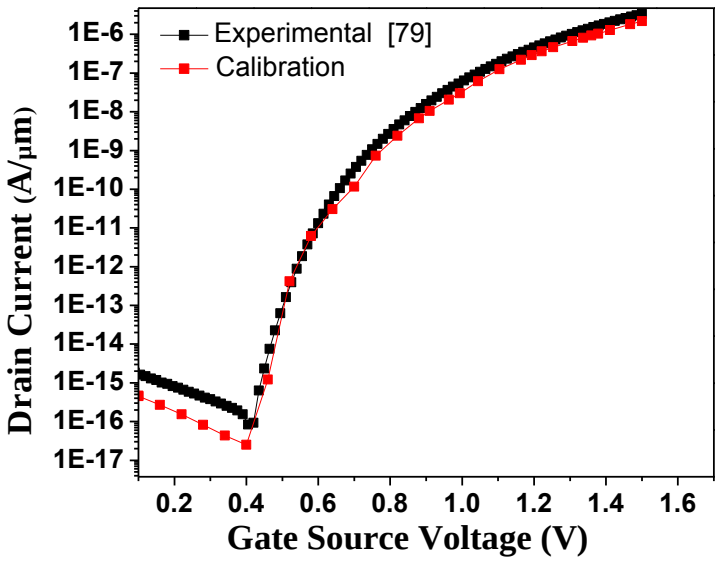


Figure 2.5 shows the calibration of our simulation result of the examined device with experimental data of [79].

2.1.3 Results and Discussion

Figure 2.6 compares the transfer characteristics of n channel-SU/AU-GAA-TFETs with varying spacer widths. The ON current (I_{ON}) and I_{ON}/I_{OFF} for AU-Cyl-GAA-TFET with LSW is 57× and 1452×, when compared with SU-Cyl-GAA-TFET with FSW and 5.2 and 35 times, compared with SU-Cyl-GAA with LSW at V_{gs} = 1.5 V, as shown in Table 2.1. Here, low OFF-state current is obtained due to the physics of drain underlap, which is defined by the series resistance consisting of barrier resistance and channel resistance. The channel resistance is further divided into gate resistance (R_{gate}) and resistance of the gate-less channel region ($R_{gate\text{-}less}$) [80]. Because of drain underlap, an extension of the drain region occurs, which causes decrease in R_{gate}, and as a result increases the enhanced gate control over the source-channel and simultaneously the $R_{gate\text{-}less}$ of the channel region increases, which causes variation in e-current density across the drain channel length and depth [55]. As a result, we found that electric field by the gate voltage over the drain channel region is gradually weakened, which has no effect on I_{ON}. It has been also observed that tunneling at the drain channel junction is reduced and hence low I_{OFF} with suppressed ambipolar behavior was achieved as shown in Figure 2.6.

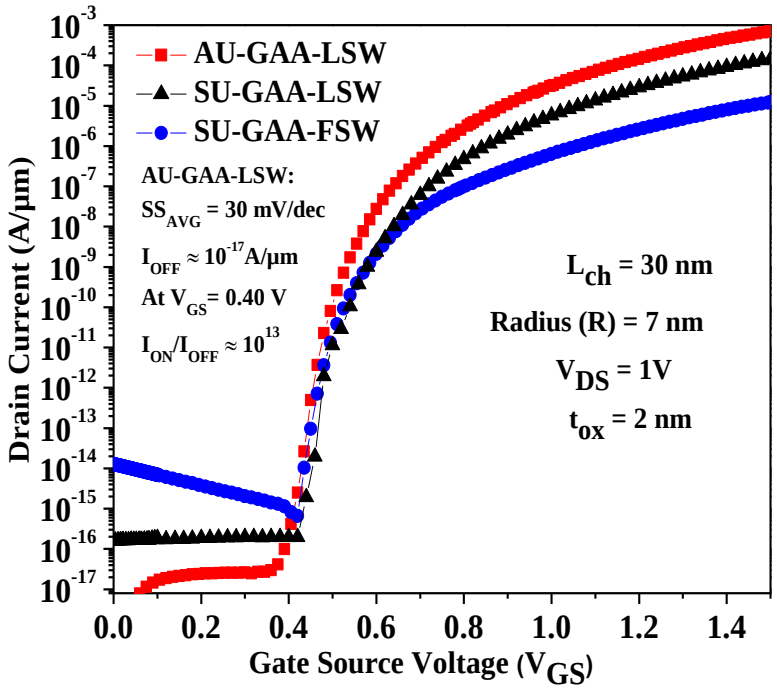


Figure 2.6 Transfer characteristic of AU, SU-Cyl-GAA with LSW/FSW of TFET.

Simultaneously, low spacer width with dielectric (k = 25) is placed across the source, drain region, due to which gate potential coupled to source over a small distance causes non-depletion of the source on the gate side. Also enhance the fringe field within the spacer [42], leads to carrier tunneling at the surface only and not inside the body, resulting in high electric field that occurs across source-channel junction as shown in Figure 2.7. This also causes high source channel tunneling, and consequently increases I_{ON}. Further, Figure 2.8 shows the energy band diagram of simulated device in I_{ON} at which applied V_{gs} reduces the source-channel barrier width. This is further reduced by placing low spacer width, resulting in more band lowering near the source channel tunneling junction, and leads to more carrier tunneling when compared with SU and AU-GAA-nTFET with high spacer width. An increase in the spacer width increases the coupling between the gate metal and the source through the spacer, thereby causing degradation in the device performance [59]. Thus, it has been found that AU with LSW produces the best device performance when compare to other two structures of GAA-TFET based on SU and FSW.

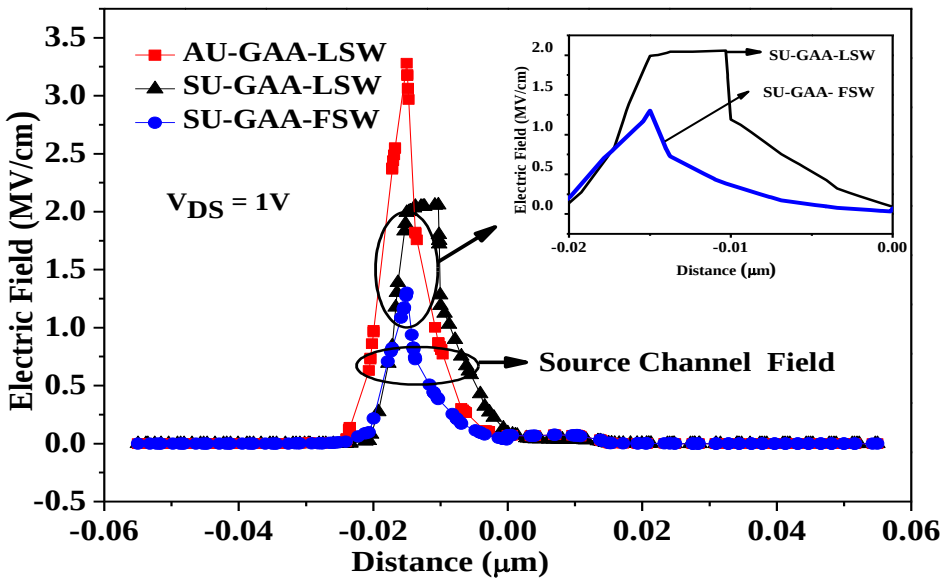


Figure 2.7 Comparison of simulated lateral electric field strengths for the three examined devices.

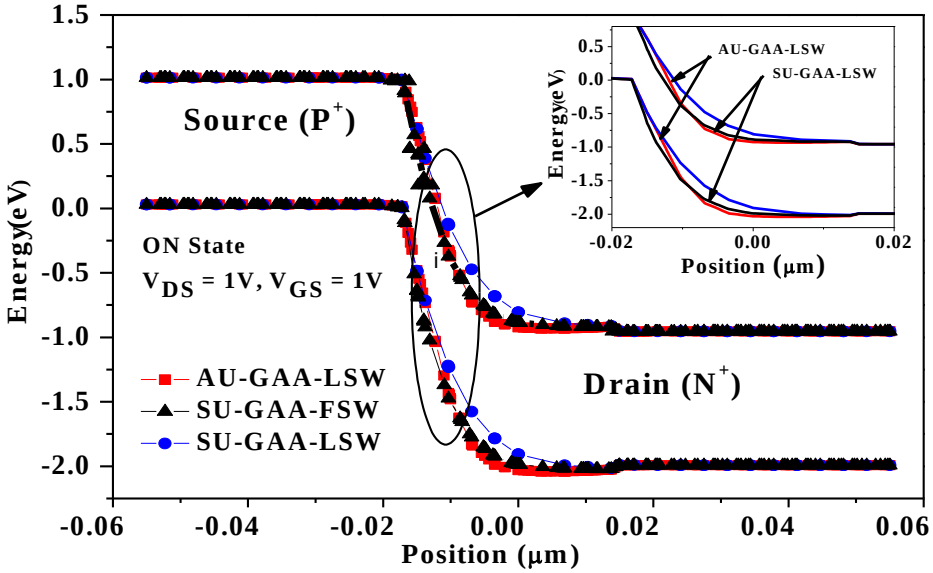


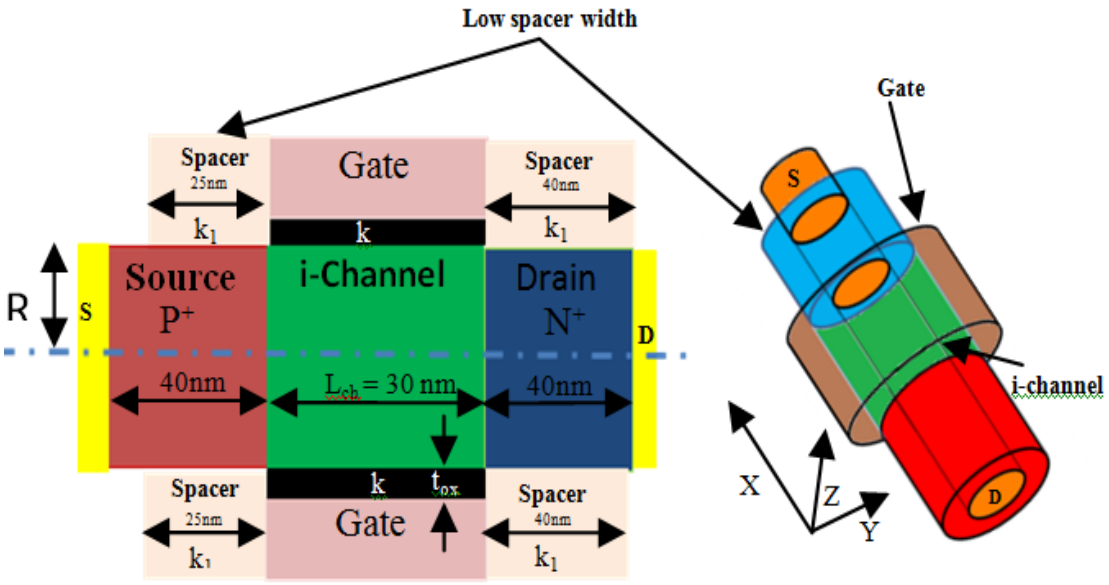
Figure 2.8 Energy band diagram in the case of AU, SU-Cyl GAA with LSW and FSW of Tunnel FET.

Table 2.1 Comparison of device parameter for underlap Cyl GAA-structure based on different spacer width

Parameter	**AU-GAA-LSW-TFET**	**SU-GAA-LSW-TFET**	**SU-GAA-FSW-TFET**
I_{ON} **(A/μm)**	6.9×10^{-4}	1.4×10^{-4}	1.2×10^{-5}
I_{OFF} **(A/μm)**	2.5×10^{-17}	1.8×10^{-16}	6.4×10^{-16}
I_{ON}/I_{OFF}	2.7×10^{13}	0.7×10^{12}	0.1×10^{11}
SS **(mV/dec)**	30	35	47

2.2 Device Design based on Asymmetrical Spacer Width

Device design of 3D Cyl GAA-n channel TFET based on asymmetrical spacer width (*AS*) has been investigated for ultra low power applications as shown in Figure 2.9 (a) and (b). Here asymmetrical spacer width means that low spacer width is placed towards source side and high spacer width is placed for drain side.



(a) (b)

Figure 2.9 (a) Cross-Sectional view, and (b) 3D View of Cyl GAA-n-channel Tunnel FET based on asymmetrical spacer width (ASW) along channel length direction.

2.2.1 Device Structure and Model Simulation

We have presented the impact of an AS width on n-channel Cyl GAA-Tunnel FET with same equivalent oxide thickness and compared to the same device based on symmetrical spacer width. Here symmetrical spacer width means that same spacer width is placed across both sides of the gate *i.e.* source and drain. It turns out that the fringing field effect with low spacer width [42], [59], while deteriorating conventional MOSFET characteristics, leads to a high I_{ON} comparable to SS-GAA-TFET. Asymmetrical doping of p-type source ($1x10^{20}/cm^3$), n-type drain doping ($5x10^{18}/cm^3$) and channel region doping ($10^{17}/cm^3$) is used as shown in Figure 2.9 (a), and (b). HfO_2 with a dielectric constant of 25 was used as a gate dielectric with gate work function = 4.53 e*V*. The Synopsys Sdevice was used to perform 3-D simulations, which included nonlocal band-to-band tunneling model (*BTBT*) combined with a field-dependent mobility, band gap narrowing and Shockley-Read-Hall recombination model.

2.2.2 Results and Discussion

The V_g is coupled all around to the source-channel junction, low spacer width with dielectric ($k_1=21$) is placed near source which enhance the fringe field within the spacer.

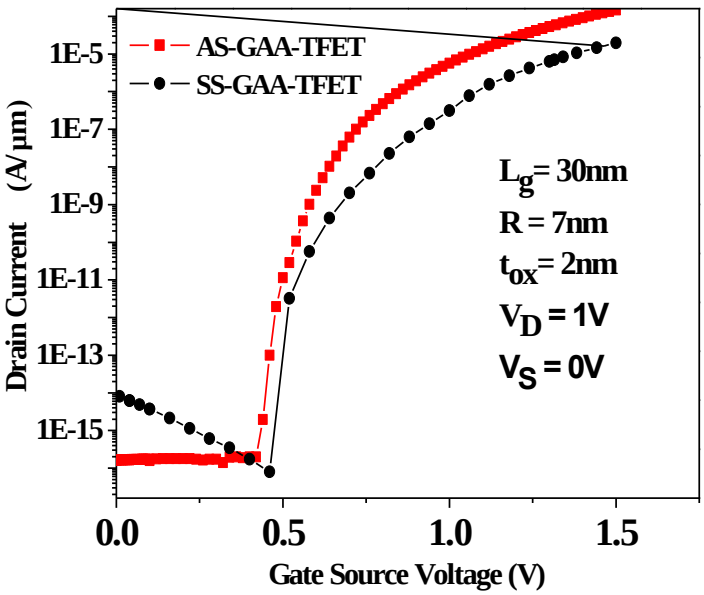
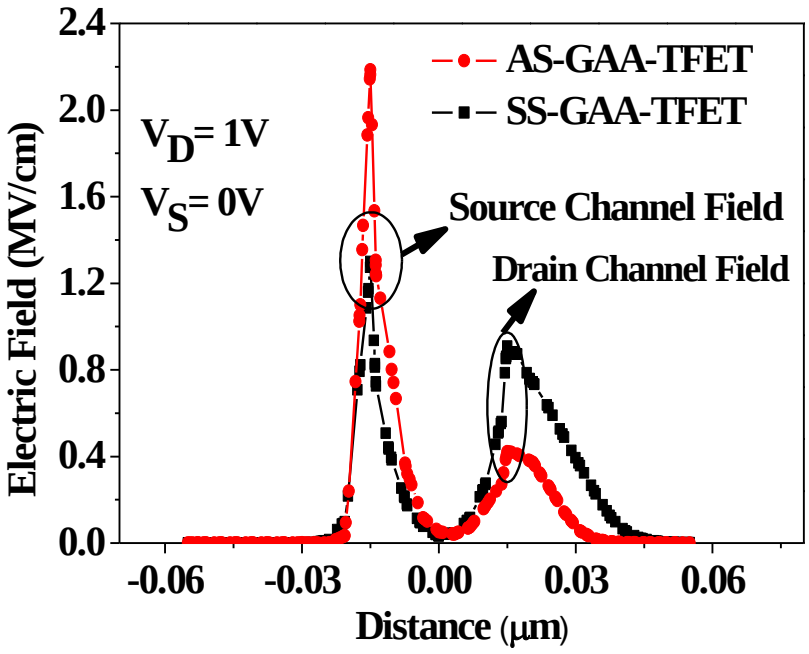
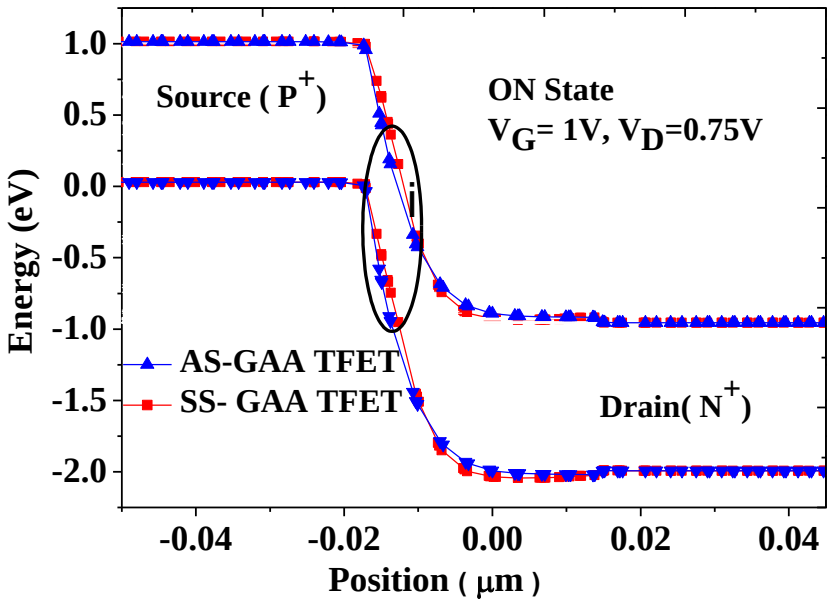


Figure 2.10 Transfer Characteristic of AS and SS-GAA-TFET at V_G=1.5V.

Here, the gate potential is coupled to source over a small distance causes non-depletion of the source on the gate side, which leads to carrier tunneling at the surface only and not inside the body, which enhance the electric field decreases tunneling barrier width, high source channel tunneling and consequently, increases I_{ON} [59] as shown in Figure 2.10.



(a)



(b)

Figure 2.11 (a) Comparison of Electric field strengths in the case of AS and SS-GAA-TFET (b) Simulated energy-band diagram of AS and SS-GAA-TFET.

Simultaneously high spacer width with same dielectric is placed towards drain side, where the fringe field coupling through it spreads; drain-to-channel electric field (ambipolar) was gradually weakened due to increased depletion width at the drain junction as shown in Figure 2.11 (a). Hence I_{OFF} decreases and suppressed ambipolar behavior. Figure 2.11 (b) shows energy band diagram of simulated device in on state in which applied V_g reduces the tunneling barrier width, which is further reduced by placing low width spacer at the source side results in more band lowering near the tunneling junction, causes carrier tunneling as compare to SS-GAA-TFET. The value of threshold voltage (V_t) is extracted using the constant current of 10^{-7} A/μm and found to be 0.72 V.

The impact of a gate dielectric on the device performance of AS-GAA-TFET is studied by varying the values of the dielectric as 3.9, 7.5, 11.5, and 21 on keeping its physical thickness constant. It is evident that an increase in the k value of the gate dielectric results in better device performance in terms of I_{ON} due to the increased oxide capacitance. It is also observed that I_{ON}/I_{OFF} decreases below 30 nm channel length due to *SCEs* as shown in Figure 2.12.

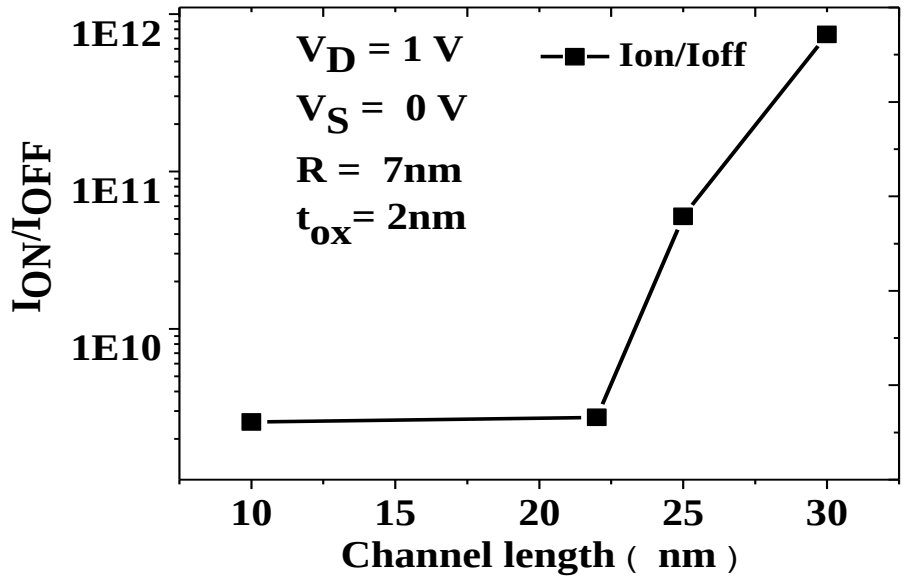


Figure 2.12 ON-OF ratio of AS-GAA-TFET.

2.3 Device Design based on Germanium (Ge)-Source

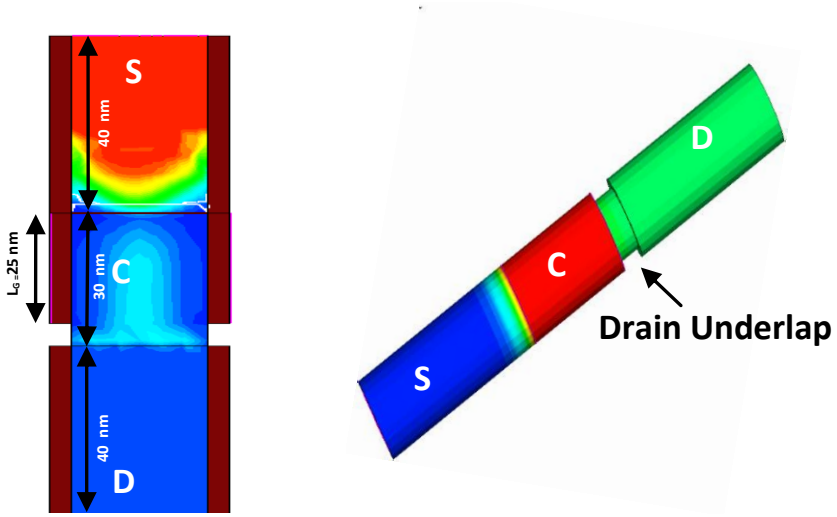
In this section, a Cylindrical GAA TFET based on germanium source for low power applications is presented. The proposed device used the merits of low band gap material such as germanium, which is used as a material in the source region. The *Ge*-source design achieves much higher ON-state drive current (I_{ON}) due to the smaller band gap of the *Ge* and high band-to-band tunneling rate as compared to *Si* for low voltage operation [60], [62]. However, as discussed in previous section despite its higher I_{ON}, Ge-TFET suffers from excessive off-state leakage current and causes degradation in the device performance. Further, based on the literature of fabrication papers, it was observed that I_{ON} can be improved by using a smaller-band gap material such as *Ge* and *SiGe* [81], [60], [78], [82]. However, it was found that experimental demonstrations have failed to achieved higher I_{ON}/I_{OFF} performance for low operating voltages (<1V) [83], [84], [85], [86] [87].

Therefore, in this work, The Ge-source design based Cyl GAA-TFET is investigated for high performance and low power logic applications using 3D TCAD Sentaurus Synopsys. Here, OFF-state (I_{OFF}) was effectively suppressed using the structure of drain underlap. Here, device investigations have been made in terms of DC characteristics like I_{ON}, I_{OFF}, *SS*, I_{ON}/I_{OFF}, C_{gs}, *and* C_{gd}. The proposed device increases ON-current as high as 1.9×10^{-5} A/μm, which corresponds to 7× improvements in I_{ON}/I_{OFF} ratio when compared with the Si-GAA-TFET.

Whereas, drain underlap causes increase in series resistance across drain-channel junction, who reduces the electric field by increasing the tunneling barrier width at the drain side, significantly reduces off-state leakage current. This shows the better device performance to address the requirement of ultra-low power and high analog/*RF* applications.

2.3.1 Device Structure and Simulation Model

Figure 2.13 (a) and (b) shows the cross-sectional and 3-D view of Drain underlap (*DU*), i.e. drain side underlap of Cyl GAA-nTFET with *Ge* based source.



(a) (b)

Figure 2.13 (a) Cross-sectional view (b) 3-D view of electrostatic potential of drain underlap (DU) Cyl-GAA-TFET with Ge Source. Here, S-Source, D-Drain, and C-Channel, gate length (L_g) = 25 nm, oxide thickness (t_{ox}) = 2 nm.

For fair comparison, we have used the same device parameters like gate dielectric (k), gate work function, and doping concentrations with the same gate source voltage (V_{gs}) scale for both the structures based on *Si* and *Ge*. The doping concentration used are P-type source ($1\times10^{19}/cm^3$), n-type drain ($5\times10^{17}/cm^3$), and p-type channel region ($10^{18}/cm^3$), HfO_2 is used as a gate dielectric as well as spacer dielectric (k =*22*) with gate work function = *4.53 eV*. To calibrate the non-local BTBT model, mass of electron (m_e) and mass of hole (m_h) for *Ge* have been taken as 0.32 and 0.52, respectively, The fitted A and B coefficients are A_{path} = A =1.46 $\times10^{17}/cm^3s$, and B_{path} = B = 3.59×10^6 V/cm.

2.2.2 Results and Discussion

Figure 2.14 shows the DC characteristics of the proposed device. It has high I_{ON} (1.95×10^{-5} $A/\mu m$), low I_{OFF} (2.5×10^{-16} $A/\mu m$), and an enhanced I_{ON}/I_{OFF} (10^{11}) with low *SS* as 58.1 m*V*/decade at low drain voltage of 0.75V as found in Table 2.2. This optimized result is obtained due to the implementation of *Ge* material in the source region since the *Ge*-source design achieves much higher ON-state drive current (I_{ON}) due to the smaller band gap of the *Ge* and high band-to-band tunneling rate as compared to *Si* for very low voltage operation, which reduces the tunneling width and thus, results to the high source channel tunneling at the device surface, which increases the I_{ON} [59].

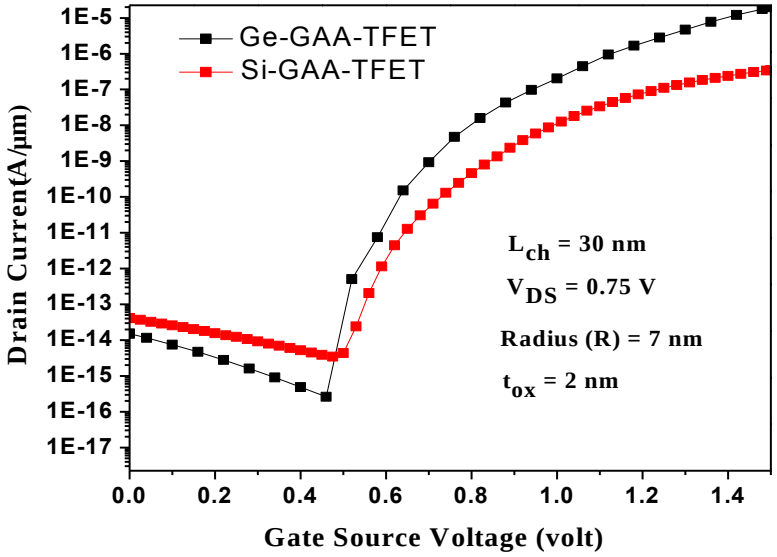


Figure 2.14 Transfer Characteristic of I_d-V_g of the examined device

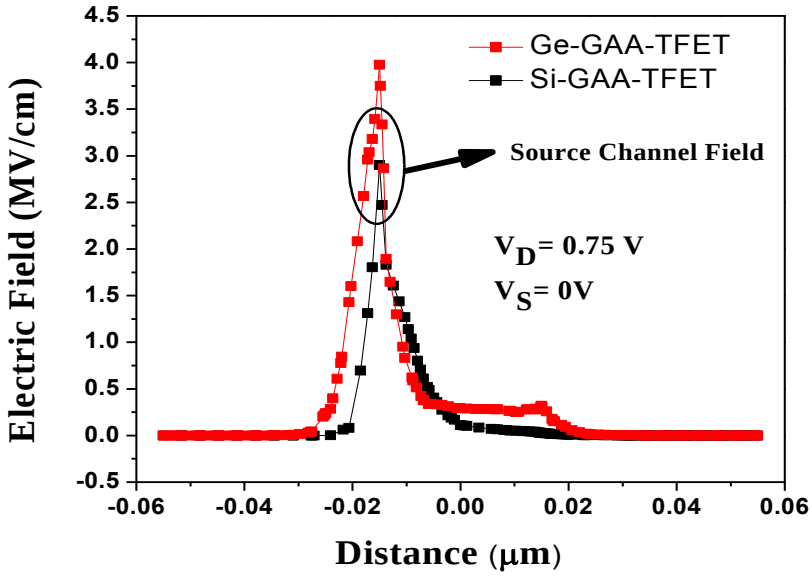


Figure 2.15 Comparison of electric field strengths in the case of Si and Ge- Cyl GAA-TFET.

At the same time in Figure 2.15, drain underlap across drain-channel junction increases the series resistance and causes increase in tunneling width and thus, electric field by the gate voltage over the drain-to-channel electric field (ambipolar) is gradually weakened as shown in Figure 2.15, which has no effect on I_{ON}. Accordingly, it reduces the drain channel tunneling and thus, low I_{OFF} with suppressed ambipolar behavior was achieved.

Table 2.2 Performance comparison of Ge and Si-TFET

Parameters	**I_{ON} (A/μm)**	**I_{OFF} (A/μm)**	**I_{ON}/I_{OFF}**
Ge-TFET	1.9×10^{-5}	2.5×10^{-16}	0.7×10^{11}
Si-TFET	3.5×10^{-7}	3.4×10^{-15}	1.0×10^{8}

2.4 Summary

A systematic investigation of the impact of the underlap structure with varying spacer widths on the device performance of a GAA-TFET has been made terms of DC characteristics like I_{OFF}, I_{ON}, I_{ON}/I_{OFF} and *SS*. It is found that drain underlap with low spacer width produces the best device performance in terms of DC characteristics. The observed comparative improvement in the I_{ON} is 57×, I_{ON}/I_{OFF} is 1452×, and 25× suppression of ambipolar current characteristics was achieved when compared with SU-GAA-FSW-TFET. In another work impact of asymmetrical spacer on the device performance has been made in terms of DC characteristics and it was found that low space width over source region and high spacer width over drain region produces the best device performance. Besides, another design of Cyl GAA-TFET based on Ge source is investigated to achieve higher I_{ON} and lower I_{OFF} as compared to Si-TFET using band-gap engineering and drain underlap. Here, the issue of high I_{OFF} was addressed by using drain underlap in geometrical structure of the Ge-TFET. A drain underlap increases the series resistance at the drain side during off state, and hence I_{OFF} decreases effectively. The Ge-TFET has high band-to-band tunneling rate at very low voltage operation. Furthermore, the proposed device would be useful in circuit design for analog-RF application.

CHAPTER 3
Attributes of Analog/RF Characteristics of 3D Cylindrical GAA-Tunnel FET

According to *WKB* approximation for BTBT of Tunnel FET, low band gap material plays an important role for high driving capability and analog/RF performances of the Tunnel devices. This is because low band gap material such as Germanium (*Ge*) based structure achieves much higher ON-state drive current (I_{ON}) due to narrow band gap and high BTBT rate as compared to silicon (*Si*) for high analog/*RF* characteristics [60], [88]. However at small gate biases, the lateral tunneling at the drain-channel junction was a dominant factor for low band gap material due to their high carrier concentration, which effectively increases the OFF-state (leakage current). Thus, it is difficult to satisfy the performance requirement of low power applications by using small band gap hetero-junction only [60], [61].

In this context, a trade-off exists between an analog/RF characteristics and leakage current. Therefore, in this work, a drain underlap (*DU*) 3D Cyl GAA-TFET based on Ge-source using fringing field effects with suppressed subthreshold leakage current is being presented as an alternative to the conventional Tunnel FET devices for high merits of analog/*RF* applications. The presented device used the merits of low band gap material such as Ge, which is used as a material in the source region with low spacer width of 12 nm.

3.1. Device Design of 3D Cylindrical GAA-Tunnel FET based on *Ge* Source

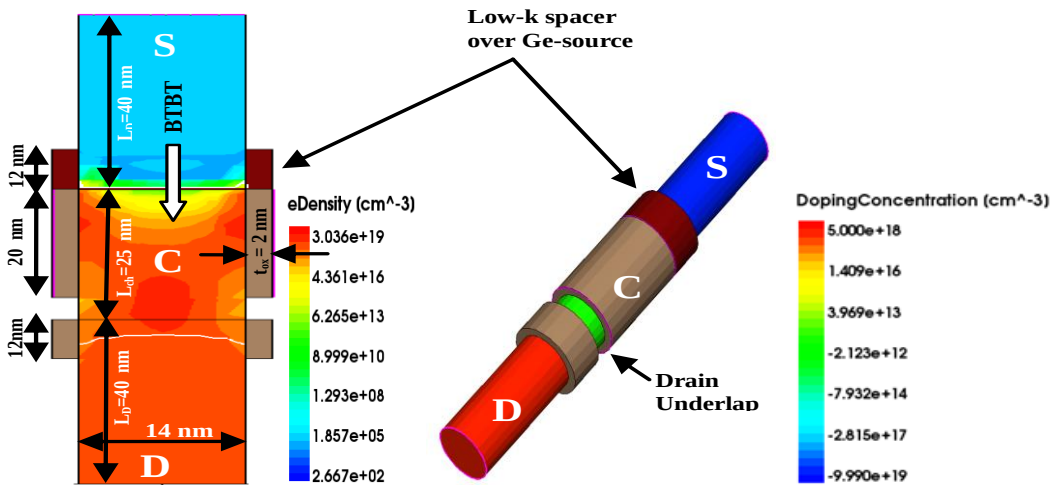
As discussed, we have investigated a drain underlap *(DU)* 3D Cyl GAA-TFET based on Ge-source. Here physics of fringing field is optimized using hetero-spacer dielectric, which is placed over the proposed device based on Ge-source, which is a feature for enhanced DC and analog/RF characteristics such as I_{ON}, I_{OFF}, *SS*, C_{gs}, C_{gd}, transconductance (g_m), cut-off frequency (f_t) and maximum oscillation frequency (f_{max}). Further, it has been also found that the ambipolar behavior and miller capacitance (C_{gd}) are minimized with high BTBT rate when compared with devices based on homo-spacer dielectric (*HS*) placed over Si-source. At the same time, the

design of drain underlap increases the series resistance across the drain-channel junction overlaps by high-k fringing field, which supports to reduce the I_{OFF}. Simulation results exhibit that the behavior of RF figure of merit of the proposed device is better as compared to the other conventional Tunnel FET structure.

Further, the device has been well calibrated BTBT model with the experimental data [79] and found better analog/*RF* performances matrix with low-k spacer width. In addition, asymmetry in spacer dielectric introduced between the source and drain reduces the ambipolar character of the proposed device.

3.1.1 Device Structure

The presented device used the merits of low band gap material such as germanium (*Ge*), which is used as a material in the source region with low spacer width of 12 nm as shown in Figure 3.1 (a) and (b) shows the cross-sectional and 3D view of drain underlap Cyl GAA Tunnel FET based on Ge-source using hetero-spacer (*HTS*) engineering with magnitude of electron current density.

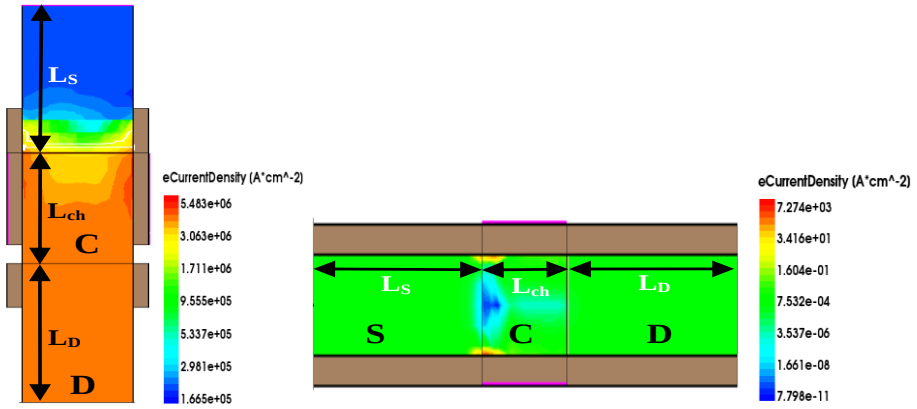


(a) (b)

Figure 3.1 (a) A Cross-sectional view and (b) 3-D view of Drain Underlap (DU) Cyl-GAA-TFET based on Ge-Source overlapped with hetero-spacer (HTS) dielectric along channel length direction with magnitude of electron (e) current density and doping concentrations. Here S-Source, D-Drain, and C-Channel. Also, L_d, L_s, and L_{ch} represent the drain, source, and channel length.

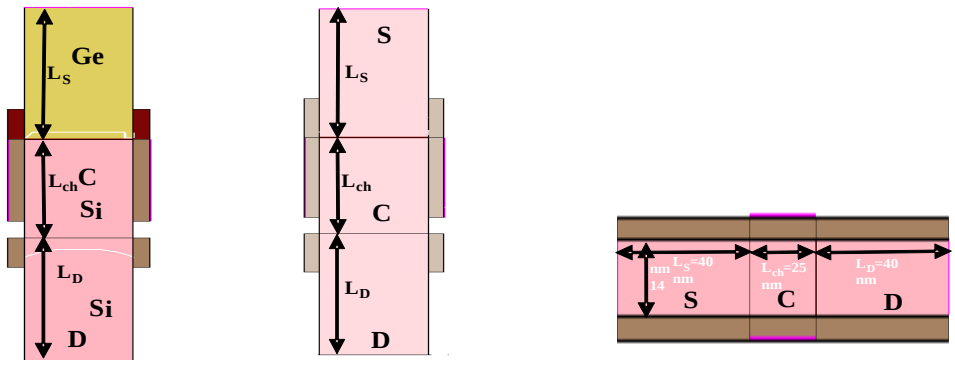
In this chapter, the concept of hetero-spacer width over *Ge*-source is used. Here implementation of HTS means that low-k spacer dielectric (SiO_2) is placed over Ge-source region and high-k spacer (HfO_2) over drain region. Whereas in homo-spacer dielectric (*HS*), the high-k spacer be placed on both sides of the gate. To evaluate the

merits of the proposed *HTS* over Ge- source of GAA-TFET, it has been compared with GAA-TFET and Double Gate-TFET based on HS dielectric over Si-source as shown in Figure 3.2 (a) and (b). The cross sectional views of material regions for all the three proposed structures are shown in Figure 3.3 (a), (b), and (c), respectively. Here, Structure 1 consists of *Ge*-source, which can be depicted in the regions of Figure 3.3 (a). For the fair comparison, we have used the same device parameters such as gate dielectric (k), gate work function, drain-source voltage (V_{ds}) and doping concentrations with the same gate-source voltage (V_{gs}) scale for all the three structures of the Tunnel FET. Gate leakage is neglected in our simulations. The threshold voltage (V_t) is defined as the gate voltage when I_{ds} is 1×10^{-7} A/μm.



(a) (b)

Figure 3.2 (a) Cross-sectional views of (a) DU Cyl-GAA-Tunnel FET, and (b) Double Gate-Tunnel FET based on *Si*-Source overlapped with HS along channel length direction with magnitude of electron current density.



(a) (b) (c)

Figure 3.3 (a) Cross-sectional views of material regions of (a) DU Cyl-GAA-TFET based on Ge-Source overlapped with HTS, (b) DU Cyl-GAA-TFET, and (c) Double Gate-TFET based Si-Source overlapped with HS. Here, the gate length (L_G) =20 nm, spacer width (L_s) = 12 nm, oxide thickness (t_{ox}) for both the spacers and gate are 2 nm

3.1.2 Device Model and Parameters

The Sentaurus Synopsys TCAD software was used to perform 3-D simulations, which included nonlocal BTBT model combined with a field-dependent mobility, and Shockley-Read-Hall recombination is activated for the effects of minority recombination [49]. Non-local BTBT model is used, which reflects the space carrier transport across the tunneling path and potential extraction at the individual mesh point. The band-gap narrowing model is enabled due to heavily doped concentrations in the source and drain regions. In addition, quantum confinement is enabled for the analysis of effects of quantum and trap. Please note that it has been important to include trap model for high accuracy of simulation since it is a dominant factor that deteriorate the device characteristics in the sub-threshold region. To calibrate the non-local BTBT model with experimental data of [60], the mass of an electron (m_e) and mass of hole (m_h) for *Ge* have been taken as 0.32 and 0.52, respectively.

The fitted *A* and *B* coefficients are A_{path} =1.46×10^{17}/cm^3s, and B_{path} = B = 3.59×10^6 V/cm were then used to simulate the DC and AC characteristics for the various Tunnel FET designs. A and B are material dependent parameters. Whereas a Si material, m_e and m_h have been taken as 0.32 and 0.54, respectively. A_{path} = 4×10^{14}/cm^3s, and B_{path} = B = 1.9×10^7 V/cm. Here, the tunneling process is nonlocal, therefore this model requires a special fine mesh to be applied around the area, where tunneling can take place. The doping concentration used are P-type source (1×10^{20}/cm^3), n-type drain (10^{17}/cm^3), and a p-type channel region (5×10^{18}/cm^3), silicon dioxide (SiO_2, k = 3.9) and hafnium dioxide (HfO_2, k = 21) was used as a low-k and high-k dielectric, respectively. HfO_2 is also used as a gate dielectric with gate work function = 4.53 eV.

3.1.3 DC Characteristics of the Device

This section presents a comparative optimum DC performance for all the three devices. Figure 3.4 compares the transfer characteristics of three n-channel TFET structures based on band gap and spacer engineering. Here, it has been observed that Ge-GAA-HTS has high I_{ON} (2.42 ×10^{-4} $A/\mu m$), which is 1.8× and 73× higher than structure I and II. Whereas low I_{OFF} (2.54 ×$10^{-18}$$A/\mu m$) was obtained, this is 73 and 320 times suppressed when compared to the structure I and II at low drain voltage of

0.75V. Also, the structure I achieve an enhanced I_{ON}/I_{OFF} (10^{14}) with steepest *SS* as low as 30 m*V/dec* was achieved, which can be observed in Table 3.1.

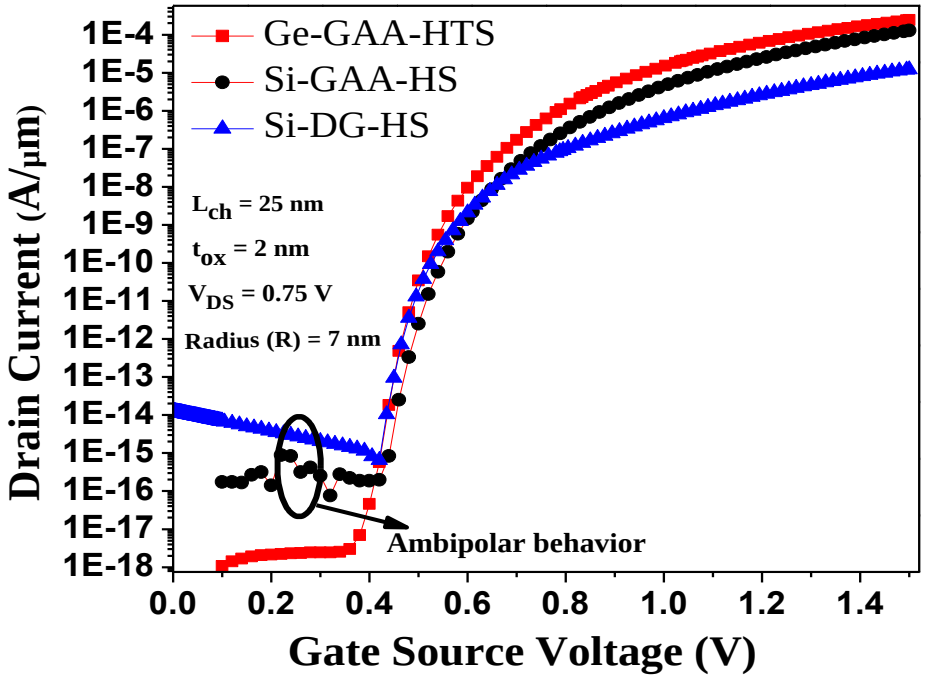


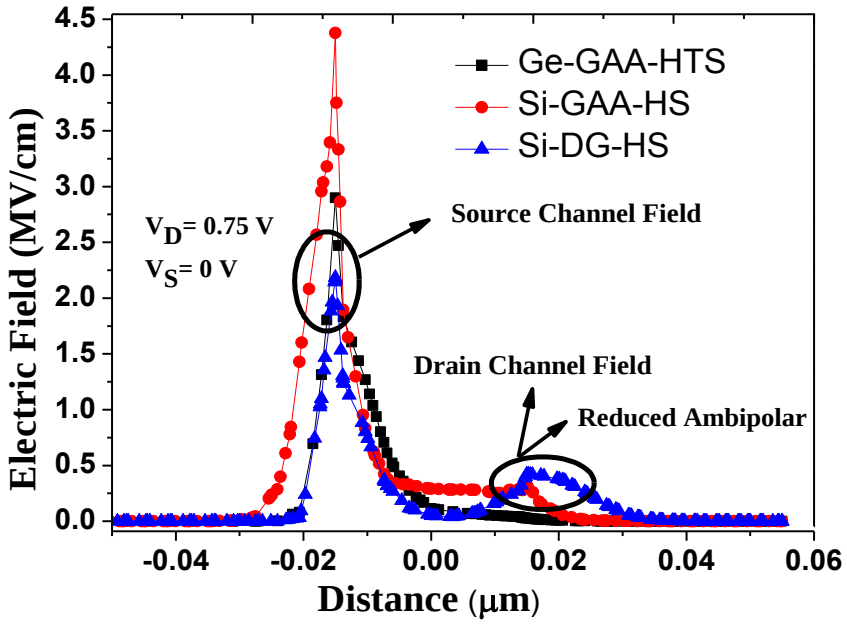
Figure 3.4 Transfer characteristics of DU GAA-TFET and DG-TFET based on Si/Ge Source overlapped with hetero and homo spacer dielectric at Vg=1.5 V. The effective channel length is 25 nm. The inset shows the calibration of our simulation result with [60].

Table 3.1 Comparison of device parameters for TFET structure based on different band gap and spacer engineering

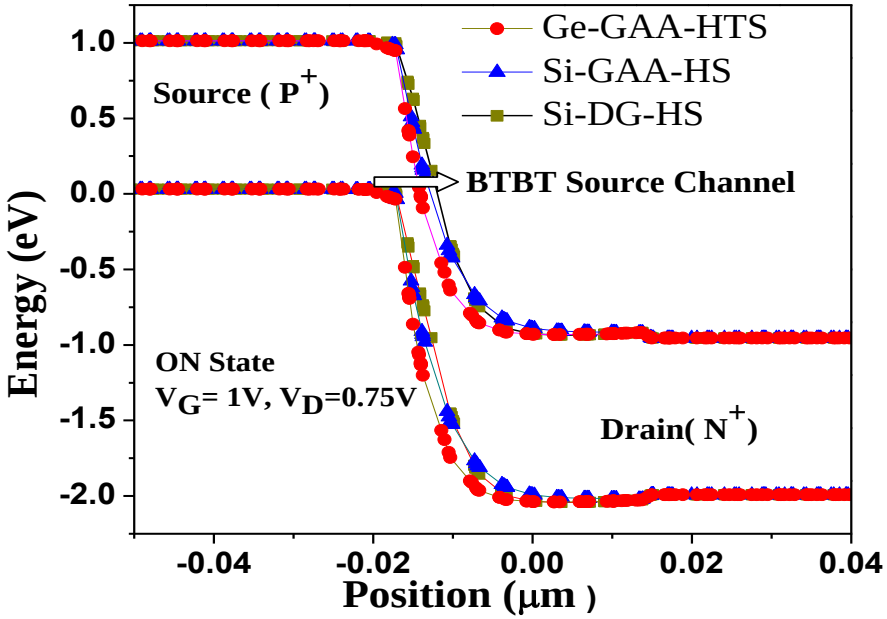
Parameters	**DU GAA-HTS**	**DU GAA-HS**	[89]
I_{ON} (A/μm)	2.10 × 10-6	3.50 × 10-7	0.3×10^{-6}
I_{OFF} (A/μm)	2.51×10^{-17}	4.32×10^{-15}	0.30×10^{-13}
I_{ON}/I_{OFF}	0.83×10^{11}	0.81×108	10^{7}
SS (mV/dec)	52.6	55.9	90
C_{gd} (F)	1.75×10^{-15}	6.15×10^{-15}	-
C_{gs} (F)	0.48×10^{-15}	0.09×10^{-15}	-

This optimized result is obtained due to the implementation of *Ge* material in the source region with spacer engineering. The *Ge*-source design achieves much higher I_{ON} drive current due to the narrow band gap of the *Ge* and high BTBT rate as

compared to *Si* for very low voltage operation, which reduces the tunneling barrier width. At the same time, the low fringing field is arising within the spacer due to low-k spacer width (k = 3.9) placed over *Ge*-source, reduces the formation of depletion zones in the source near the gate edge and supports to the high source channel tunneling at the device surface [59].



(a)



(b)

Figure 3.5 (a) Simulated lateral electric field strengths of all the three proposed structures of TFET, and (b) Comparison of energy band diagram for the three structures of Tunnel FET based on **Si/Ge**-source overlapped with HTS and HS dielectric in the case of ON state of the devices.

In the ON state, the valence band of the source is more aligned to the conduction band of the channel due to the small band gap of *Ge*-source, thereby reduction of the tunneling barrier width as shown in Figure 3.5 (a). This small tunneling width in *Ge*-source ensures more probability of *BTBT* of charge carriers, resulting in the reduction of tunneling barrier width. This small tunneling width over *Ge*-source ensures more probability of BTBT of charge carriers with minimized fringing effects and significantly leads to high I_{ON} as shown in Figure 3.4.

This is mainly because of the non-depletion of the source towards gate side by low-k spacer within low band gap material [54], [59]. Please note that the fringing field through the spacer is seen to have a strong influence on the total electric field in the source channel junction region [42] Simultaneously, a combined effect of high-k spacer over *Si*-Drain with *DU* structure reduces the I_{OFF}. DU comprises the channel resistance to be divided into gate resistance (R_g) and without gate resistance of the channel region (R_{wg}) [55]. Therefore, an extension of the drain-channel region without gate occurs, which causes an increase in R_{wg} of the drain-channel region with a decrease in R_g. Hence, DU increases the series resistance at the drain-channel junction [59]. While due to a high-k spacer, the fringing field is arising out of the spacer towards gate side, which concentrates the field near the junction and causes the formation of depletion zones near the gate edge. Significantly, the drain channel tunneling rate drops rapidly by widening the tunneling barrier width at the drain-channel junction and thus, electric field by the gate voltage over the drain-channel junction (ambipolar) is gradually weakened as shown in Figure 3.5 (b), which does not affect I_{ON}.

Further, it can be clearly observe in Fig. 3.6 that the device of a double gate Tunnel FET has highest input resistance during ON state while it shows lowest resistance path during OFF state current. Whereas, the Ge-source GAA-TFET based on hetero-spacer dielectric produces the lowest resistance path during ON state while it shows highest input resistance during OFF state for low power devices.

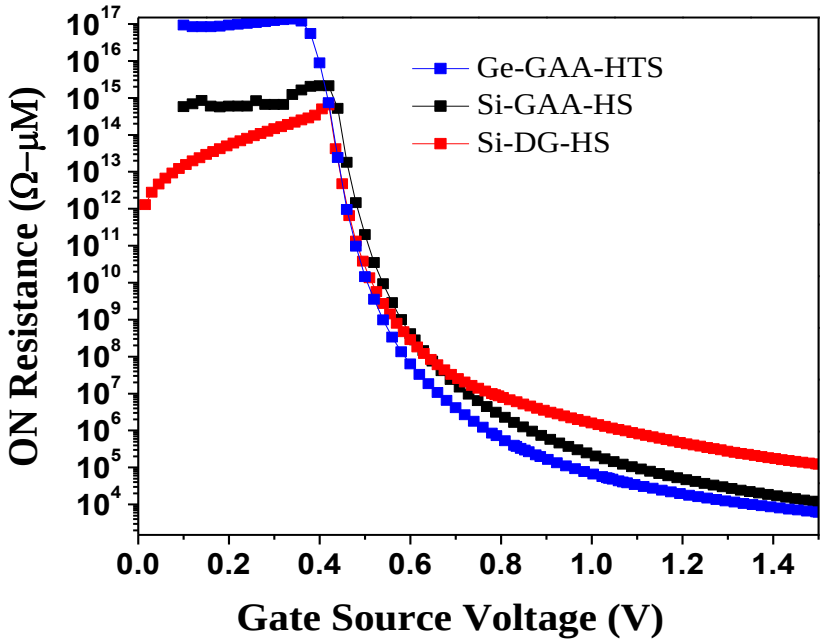


Fig. 3.6 Transfer characteristics of ON Resistance with respect to gate source voltage

Conclusively, drain underlap structure with low-k spacer width placed over *Ge*-source produces the better performance in terms of both i.e. I_{ON} and I_{OFF}. Here, on the basis of spacer width analysis, it has been found that gate potential coupled to source over small distance enhance the fringe field within the spacer, leads to high source channel tunneling, and improved the device performance. An increase in the spacer width increases the coupling between the gate metal and the source through the spacer, thereby causing degradation in the device performance. Due to low sub threshold leakage (I_{OFF}), suppressed *SS* was achieved, which plays an important role in low power applications.

3.1.4 Analog/RF Performances of the Device

The design of analog and RF devices for ultra low-power circuit applications has lead to popular research as it is becoming difficult with the rigorous downscaling in CMOS technology in the deep sub micrometer regime. In this part, the RF performances are investigated such as cut-off frequency (f_t), maximum frequency of oscillations (f_{max}) and Gain Bandwidth Product (GBP).

Figure 3.7 (a) and (b) investigate the variation of C_{gs} and C_{gd} for the various values of V_d, respectively on the proposed structure I. Here, C_{gd} is the miller capacitance, and in

order to improve the analog performance of the device, miller capacitance should be reduced. We know that $C_{gd} = C_{dif} + C_{dov} + C_{of} + C_{gdinv}$ and $C_{gs} = C_{of} + C_{sif}$. Where, C_{sif} and C_{dif} are the inner fringing capacitances at source and drain side, respectively. C_{dov} is the drain overlap capacitance. C_{of} *is* the outer fringing capacitance between the gate metal and the channel.

It has been observed that on increasing the value of gate to source voltage (V_{gs}), C_{gd} increases due to the formation of an inversion layer, which increases towards the source from drain region below gate oxide and reduces channel to drain potential barrier for an increase in the value of V_d [90]. However, the desired value of C_{gd} at 0.75 V is low as compared to another conventional Tunnel FET.

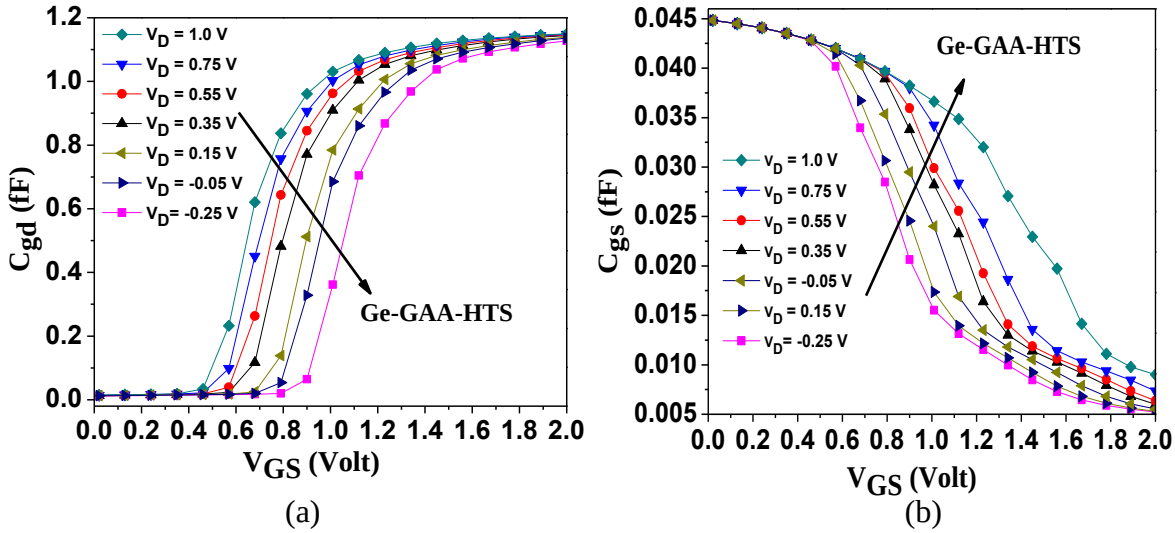
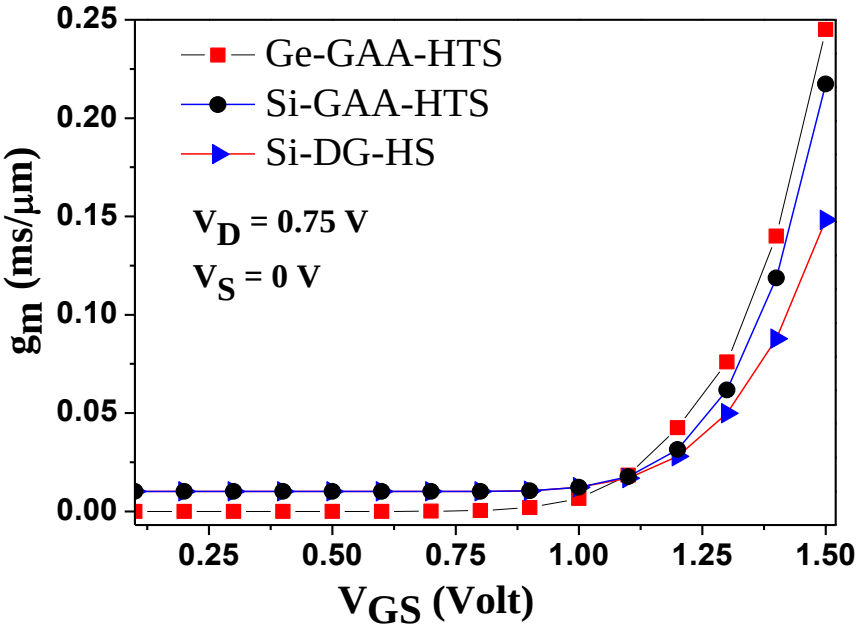
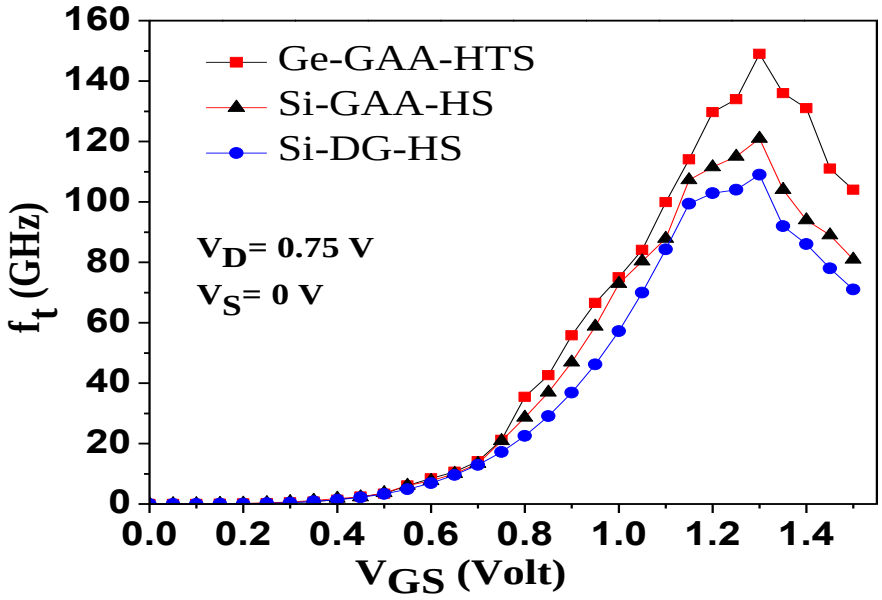


Figure 3.7 (a) Analysis of gate-to-drain capacitance (C_{gd}), and (b) Gate to source capacitance (C_{gs}) as function of the gate to source voltage (V_{gs}) for different value of V_{ds} for Ge-GAA-HTS.

Whereas in C_{gs}, falls slightly with an increase in the value of V_{gs} as shown in Figure 3.7 (b). This phenomenon occurs due to reduction in coupling between the source and the gate due to the extension of the inversion layer as well as potential barrier. Therefore, due to different gate to channel coupling strength between channel regions significant by a low value of gate resistance (R_g) with high value of without gate resistance (R_{wgi}). Bseides, a C_{gd} is reduced to 11.4×10^{-16} F.



(a)



(b)

Figure 3.8 (a) Comparison of extracted transconductance, and (b) RF characteristics for all the three structures of Tunnel FET

The cut-off frequency f_t is the frequency when the current gain is unity, f_t can be computed as:

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{3.1}$$

Here it can be observed that low value of C_{gd} with high gm significant for high values of f_t. Further, g_m plays an important parameter for analog circuit design, gm of a device is a measure of the current driving capability of the device, and it should be high in order to obtain an efficient design. Here Ge-GAA-HTS has also higher gm of 0.24×10^{-3} S/μm than conventional TFET due to higher drain current driving capability as shown in Figure 3.8 (a).

Here, f_t extracted as high value of 149 GHz for structure I, due to high value of g_m and lower C_{gd} as shown in Figure 3.8 (b). Here f_t starts increasing with gate-to-source voltage until it reaches its maximum value at a specific gate to source voltage. The reason behind such behavior is that, as gate to source voltage increases, the number of electrons injected from source to channel via band to band tunneling increases and consequently, gm increases. Therefore, Cut-off frequency increases and reaches at maximum value. Thus, the proposed device consists of Ge-source with low-k spacer produces low leakage sub threshold current, and low C_{gd} with reduced ambipolar behavior. It leads to abrupt control switching. Hence our device also satisfies the requirement of low power circuit applications.

3.2 Device Design based on Distinct Device Geometry

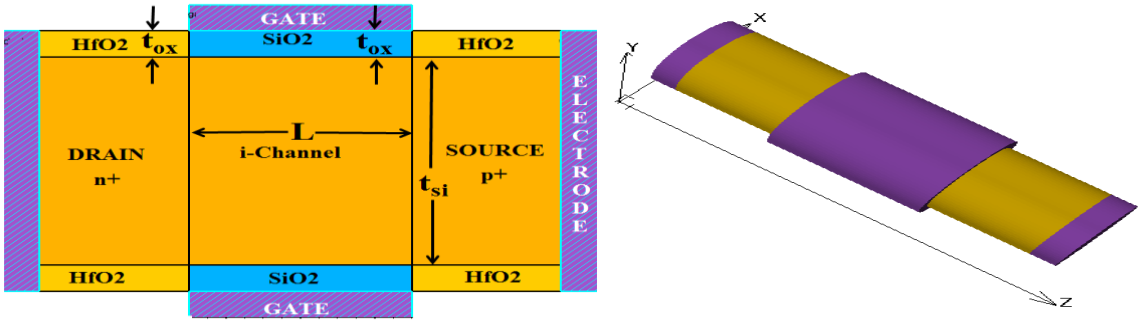
As discussed, the MOSFET device has demanded scaling into the nanoscale region in order to realize high chip density like silicon on chip (*SoC*) designs, high speed and improved radio frequency (*RF*) performance [91]. In order to accomplish effective scaling of the device various novel device structures were employed like MuGFETs [24], [70], fully depleted silicon-on-insulator MOSFETs and Silicon Nanowire MOSFETs [11], [88]. Although these devices have increased the gate controllability and *RF* performance of MOSFET, however, the limitation possessed by excessive scaling of MOSFETs is the saturation of sub threshold swing to 60 m*V*/*decade* at room temperature [12]. Due to this limitation, *SCEs* and high leakage currents come into process when operating the device below 1*V*. Further, device geometrical optimization plays an important role in superior DC and analog/*RF* Performances. Since in Tunnel FET, device optimization with accordant meshing are highly significant for high tunneling zone across the drain channel junction.

Motivated by the above statement, we have also investigated DC and analog/*RF* performances on cylindrical GAA tunnel TFET based on distinct device geometry.

Firstly, performance parameters of GAA-TFET are analyzed in terms of drain current, gate capacitances (C_{gg}), transconductance (g_m), source-drain conductance (g_{ds}) at different radii and channel length. Furthermore, we also produces the geometrical analysis towards the optimized investigation of radio frequency (*RF*) parameters like cut-off frequency (f_t), maximum oscillation frequency (f_{max}) and gain bandwidth product (*GBW)* using a 3D TCAD Simulation. Due to band to band tunneling based current mechanism unlike MOSFET, gate-bias dependence values as primary parameters of TFET differ. It is also analyzed that the maximum current occurs when radii of Si is around 8 nm due to high gate controllability over the channel with reduced fringing effects and also there is no change in the current of TFET on varying its length from 100 nm to 40 nm. However current starts to increase when channel length is further reduced for 40 nm. Both of these trade-offs affect the *RF* performances of the device, which is analyzed in this chapter.

3.2.1 Device Structure and Simulation Model

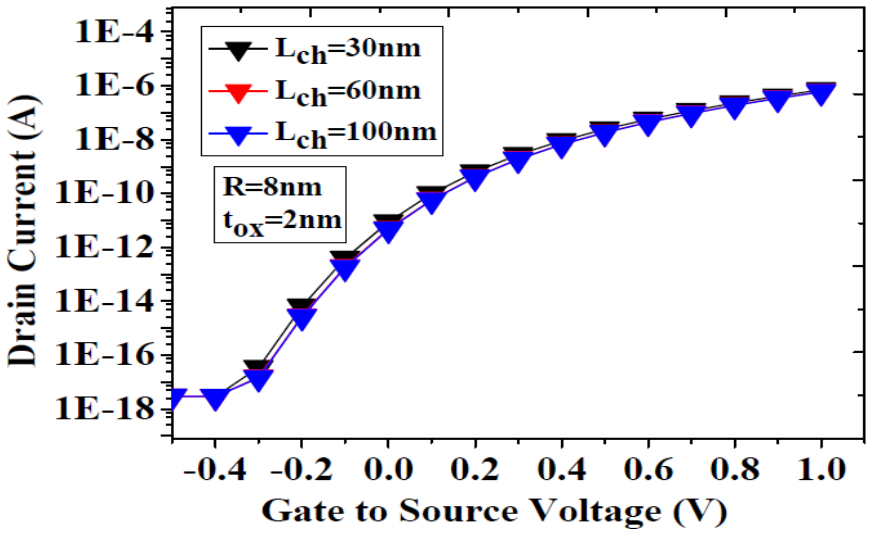
The device structure under simulation has following parameters; channel region doping P-type source (1×10^{20}/cm^3), n-type drain (10^{17}/cm^3), and a p-type channel region (5×10^{18}/cm^3), Source-channel junction is kept perfectly abrupt for improving the performance of the device and drain doping profile is optimized according to work [92] to reduce ambipolar behavior. Channel radius (R) is ranging from 7 to 10 nm, oxide thickness (t_{ox}) = 2 nm a low-k gate insulator with a relative permittivity of silicon dioxide (SiO_2, k=3.9) with gate work function=4.53 eV, channel length (L_{ch}) is varying from 30 to 100 nm and source drain extension length (L_{ext}) = 40 nm.



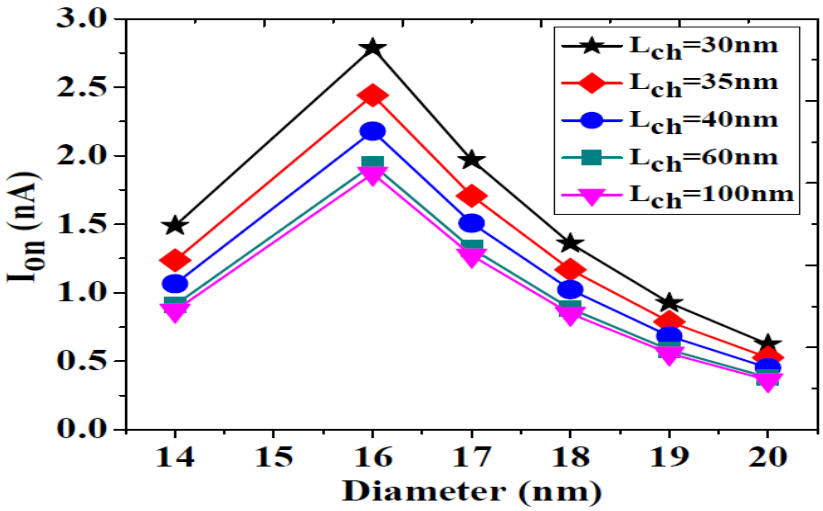
(a) (b)

Figure 3.9 (a) 3D view, and (b) Cross-sectional view of simulated Cylindrical GAA- n channel-Tunnel FET along z axis

Here, Figure 3.9 (a) and (b) shows the 3D and cross-sectional views of n channel cylindrical GAA-Tunnel FET. In this analysis nonlocal band to band tunneling (BTBT) model was employed and have validated simulation model using [44]. Further, taking into account the high doping concentration in the source and the drain regions, band gap narrowing model was also included with other physical models such as concentration, field dependent, mobility, Shockley-Read Hall (SRH) recombination model and Fermi Dirac statistics. Furthermore, the analog/*RF* figures of merit have been extracted from the Y-parameter matrix generated by performing the small signal AC analysis using TCAD tool. The *RF* parameter such as f_t is extracted when current gain drops to unity and f_{max} is extracted when mason's unilateral gain drops to unity.



(a)



(b)

Figure 3.10 (a) I_{ds}-V_{gs} characteristics for GAA-TFET at different channel length, and (b) ON current values for different channel length at varying radius.

3.2.2 Impact of Device Geometry on DC characteristics

For DC analysis plots are obtained by varying the dimensions (length and radius) and then analyzing the I_d with V_{gs} characteristics. Series resistance in Tunnel FET composed of channel resistance and tunneling barrier resistance [56]. On varying the channel length, it affects channel resistance whereas in varying the cross-section area affects the tunneling barrier resistance. For the variation with length, I_{ON} is observed to be nearly constant with the change in length from 60 *nm* to 100 *nm* as shown in the Figure 3.10 (a), and (b) since they overlap. However, for channel length of 30 *nm*, it is slightly higher. Further, in Figure 3.10 (b) we also observed that there is no significant change in the value of current from 60 *nm* to 100 *nm* since decrease in channel length causes decrease in channel resistance, which does not vary the overall series resistance much. However, current rises between 30 nm to 40 nm. This can be attributed to the decrease in channel resistance due to decrease in channel length, which starts to dominate at lower channel lengths. Thus, ON-current increases around these lengths.

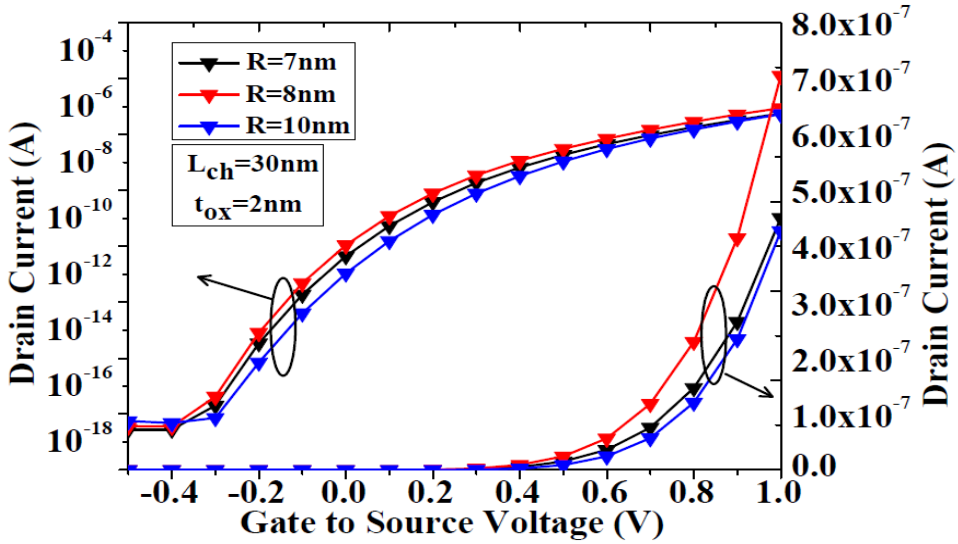


Figure 3.11 I_{ds}-V_{gs} characteristics of GAA-TFET for different radius on linear scale and logarithmic scale

As we vary the radius, we observe that drain current is maximum when R= 8 nm. This is because of some quantum effects that below R=8 nm, the cross-section area becomes small enough to effectively reduces the tunnelling area, increases the energy of the barrier width and thus reduce the number of charge carriers tunnelling from source to channel. Above R=8 nm, the cross-section area becomes large enough to prevent proper coupling of bands hindered in the tunnelling effects and thus increases

the energy of tunnelling barrier width as compared to the energy of the charge carriers to cross the barrier width and hence reducing the ON-current.

Table 3.2 Comparison of Device DC characteristics of GAA-TFET for different channel length

Channel Length	**$I_{on}/I_{off} \times 10^8$**			**SS (mV/dec)**
L_{ch} (nm)	**Diameter (nm)**			**(Diameter = 16nm)**
	14	16	20	Up to 4 order of drain current
30	0.1346	9.6733	1.6329	54.42
60	4.118	6.7644	0.9924	55.00
100	0.948	6.551	0.948	55.00

The Table 3.2 summarizes the I_{ON}/I_{OFF} ratio at L_{ch} = 30 *nm*, 60 *nm*, 100 *nm* and diameters being 14 *nm*, 16 *nm*, 20 *nm*. Further, it can be observed clearly from Figure 3.11 that the I_{ON}/I_{OFF} ratio is maximum for radii 8 *nm*. It was also computed that *SS* of 54.52 *mV/dec* was achieved for four order of drain current of diameter 16 nm and channel length 30 *nm*. Since below 30 *nm*, it suffers from short channel effects and fringing field effect. In ON state, partitioning of C_{gg} in a TFET is significantly different from that in a MOSFET and is fundamental due to the difference in inversion charge (Q_{in}) distribution.

3.2.3 Impact of Device Geometry on Analog Performances

To study the effect of geometry variation on analog/*RF* performance of GAA-TFET, understanding its effect on the gate-capacitance and conductance values are quintessential. These parameters are influential in determining behavior of f_t, f_{max} and GBW. The values of gate-to-drain capacitance (C_{gd}), gate-to-source capacitance (C_{gs}), transconductance (g_m) and drain-to-source conductance (g_{ds}) which strongly affect f_t and f_{max} can be evaluated from imaginary and real part of admittance parameters y_{12} y_{11} y_{21} and y_{22} respectively.

C_{gd}, C_{gs}, g_m and g_{ds} can be extracted as follows:

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega}; \qquad g_m = \mathrm{Re}(Y_{21})|_{\omega 2=0}; \tag{3.2}$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{12}) + \mathrm{Im}(Y_{11})}{\omega} \qquad g_{ds} = \mathrm{Re}(Y_{22})|_{\omega^2=0} \tag{3.3}$$

Based on understanding of device physics and capacitance components from numerical simulation, the total capacitance (intrinsic + extrinsic) of a double gate tunnel FET, gate-source (C_{gs}) and gate-drain (C_{gd}) capacitance (without considering overlap capacitances) are calculated as $C_{gd} = C_{of} + C_{dif} + C_{gd,inv}$ and $C_{gs} = C_{of} + C_{sif}$, where C_{of} is the outer fringing capacitance, C_{dif} and C_{sif} are the inner fringing capacitances at drain and source side respectively [90]. These are related to the source doping abruptness. The two fringing capacitance calculations are performed by adjusting expression reported in [16], and are approximated by total input capacitance ($C_{gg} = C_{gs} + C_{gd}$), which can be extracted from AC simulations as:

$$C_{gg} = \left| \frac{|\mathrm{Im}(Y_{11} + Y_{12})|}{\omega} \right| \qquad \text{Where } \omega = 2\pi f_0 \tag{3.4}$$

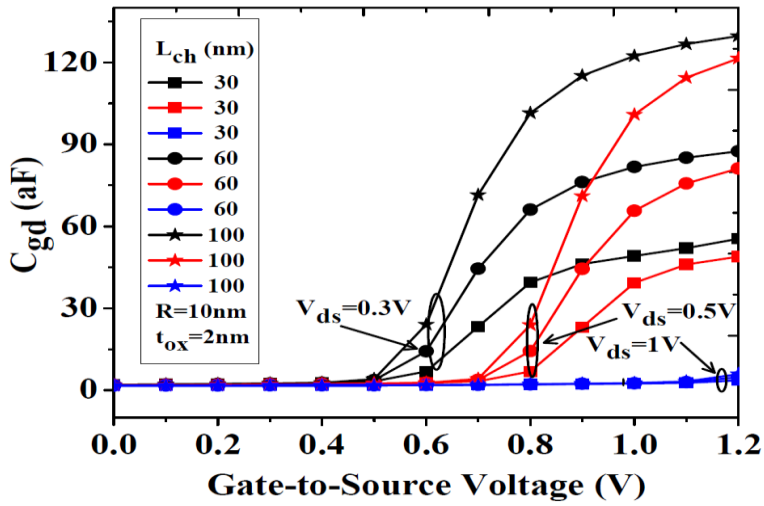
We can define C_{gg} in the first order as $C_{in} + C_{frin}$ (total fringing capacitance including external and internal fringing components). The C_{frin} can simply be identified by limiting total gate capacitance (C_{gg}) at zero or negative V_{gs}.

Furthermore, Figure 3.12 (a) and (b) analyzed the intrinsic gate drain capacitance and gate source capacitance, respectively for GAA-TFET with different gate length as a function of gate to source voltage, which are extracted from small signal AC analysis performed at frequency of 1MHz from numerical simulation. As V_{gs} increases, C_{gd} increases because of accumulation of more and more charge carriers, which form inversion layer from the drain to source. On increasing gate to source (V_{gs}) voltage, inversion layer formation occurs, which going to increases towards the source from drain below gate oxide for constant value of drain voltage [93].

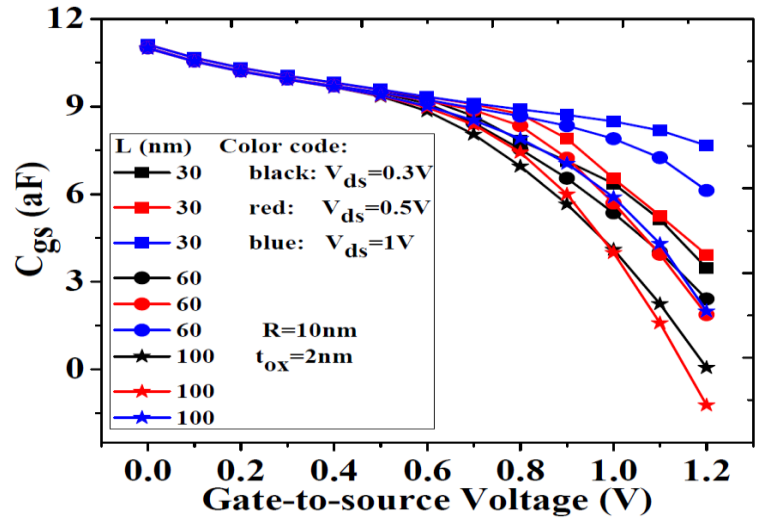
The length of the inversion layer formed increases with V_{gs} and so gate-to-drain capacitance is also increasing with V_{gs},, which is confirmed in Figure 3.12 (a). It is also evident in curve that as V_{ds} increases, C_{gd} decreases. This is due to the reason that as V_{ds} increases from 0.3 V to 1 V, while keeping $V_{gs} = 1V$ the value of

Potential difference between gate and drain (V_{gd}) decreases which decreases the electric field and pulls the carriers from drain side to channel side to construct the inversion layer.

Hence, C_{gd} is reduced on increasing V_{ds}. In case of same radius and varying channel length, we observe that as channel length increases, gate-drain capacitance also increases owing to the increase in channel length. Also, as we observe in Table 3.3, C_{gd} is maximum for highest radius i.e. 10 *nm* as the cross section area increases and so does the tunneling width increases.



(a)



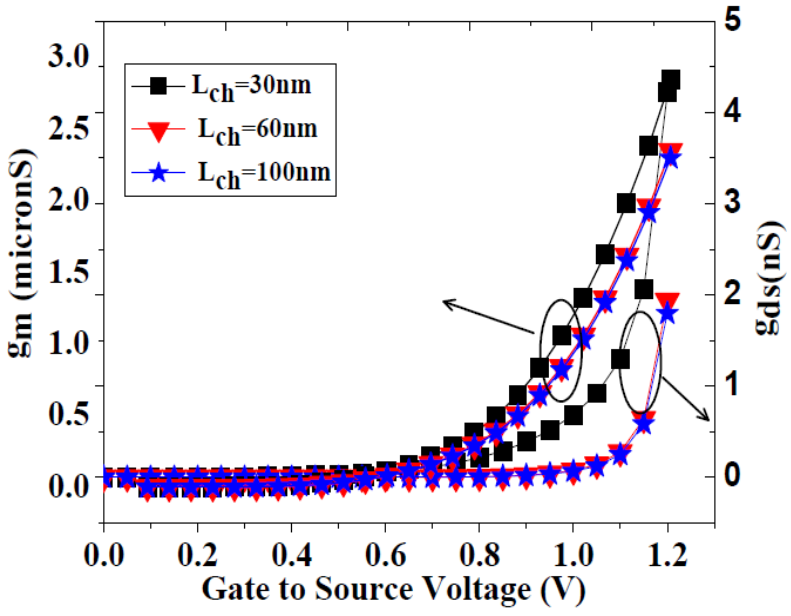
(b)

Figure 3.12 Transfer characteristic of gate capacitance values for GAA-TFET as a function of V_{gs} for different lengths at different radii, (a) gate to drain capacitance, and (b) gate to source capacitance.

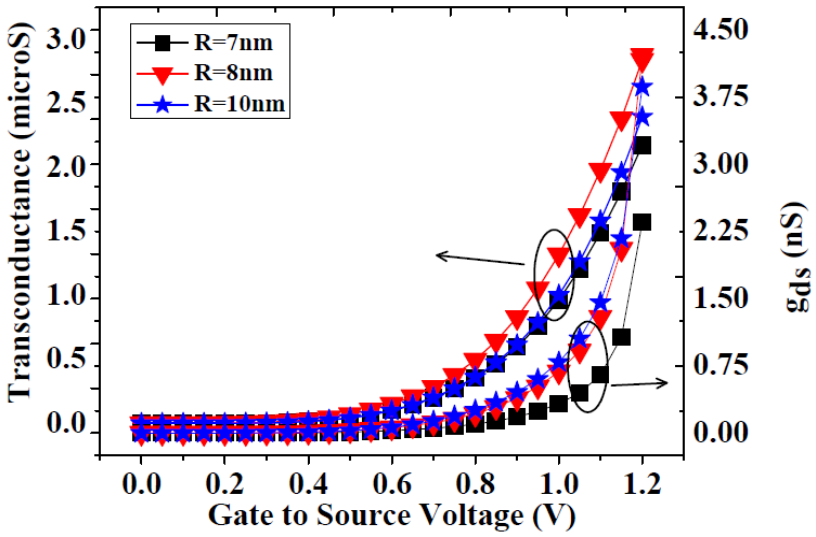
Table 3.3 Comparison of Device gate capacitance of GAA-TFET for different channel length and radii

R(nm)	L_{ch} = 30 nm		L_{ch} = 60 nm		L_{ch} = 100 nm	
	C_{gd}(aF)	C_{gs}(aF)	C_{gd}(aF)	C_{gs}(aF)	C_{gd}(aF)	C_{gs}(aF)
7	5.59002	4.45561	10.3973	3.46785	15.9795	1.29343
8	6.58724	5.43456	12.7369	4.048	19.6167	1.13476
10	7.16881	8.13562	14.8662	7.13128	24.258	4.80083

Whereas in Figure 3.11 (b), we observe, that C_{gs} decreases on increasing V_{gs}. The reason behind this being that the coupling reduces between the source and the gate due to the extension of the inversion layer. For same radius and varying length, gate-source capacitance decreases with increasing length. This is due to the formation of longer channel which increasingly screens the gate-source capacitive coupling. As for the variation with V_{ds}, Figure 3.12 (b) shows that increase in V_{ds} corresponds to increase in C_{gs}. Increasing V_{ds} accounts for lower V_{gd} leading to shorter inversion layer. This decreases the screening caused in coupling of source and gate by inversion layer and thus increasing the C_{gs} [90].



(a)



(b)

Figure 3.13 Transfer characteristics of transconductance and gate drain conduction for GAA-TFET as a function of V_{gs} (a) For varying length, and (b) For varying radius

The g_m and g_{ds} at V_{ds} =1V with different silicon radius and gate lengths as a function of gate to source voltage for GAA-TFET are shown in Figure 3.13 (a) and (b). These conductances depend on the number of carriers that contribute to I_{ON}. As V_{gs} increases, the number of carriers injected from the source increases due to which the on-current increases and hence transconductance and gate-drain conductance increases as it is confirmed from the curve. We observe that g_m and g_{ds} remain almost constant even on varying channel length of L_{ch} = 100 *nm* to L_{ch} = 40 *nm*. It is due to the invariability in tunneling phenomenon in the channel, that there is no change in the number of carriers or on current. Also g_m and g_{ds} increases below 40 *nm* due to decrease in channel resistance [22], [94]. On changing the radius while keeping the length constant, we observe that g_m and g_{ds} vary as the overall tunneling area is changed, which changes the number of carriers that can tunnel from source to channel and hence changing the ON-current. As the cross-section area is increased, number of injected carriers through tunneling increases and so does the ON-current increases. Also, as observed earlier ON-current is maximum in case of diameter = 16 *nm* and hence g_m and g_{ds} are also maximum in those cases. As discussed g_m of a device is a measure of current driving capability of the device.

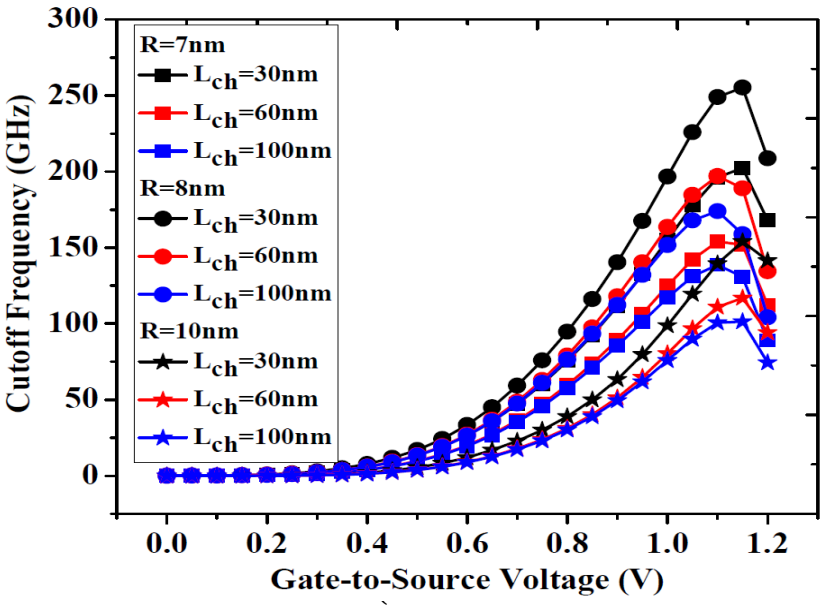
3.2.4 Impact of Device Geometry on RF Performances

The design of analog and *RF* devices for ultra low-power circuit applications has lead to popular research as it is becoming difficult with the rigorous downscaling in CMOS technology in the deep sub micrometer regime. In the coming part, the RF performances are investigated such as cut-off frequency (f_t), maximum frequency of oscillations (f_{max}) and Gain Bandwidth Product (*GBW*).

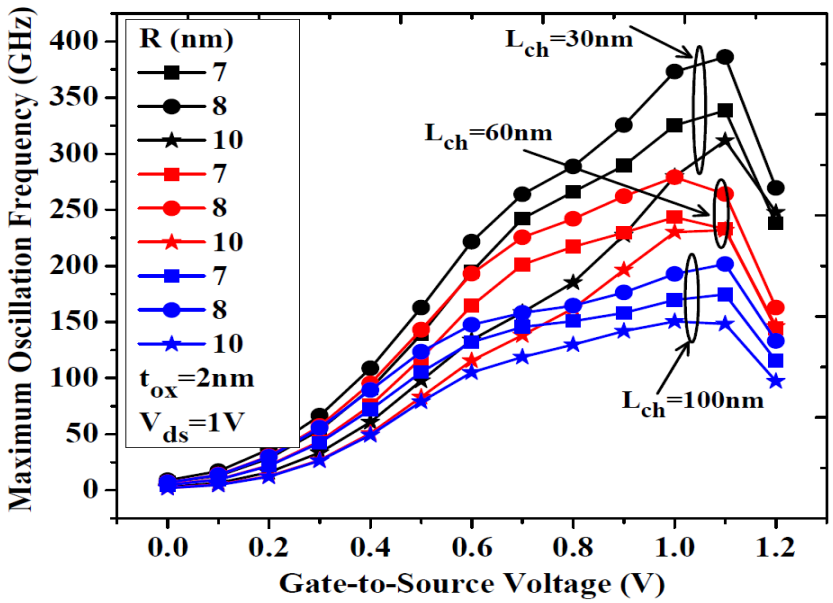
The parameters f_t and GBW are primary figure of merit (*FOM*) in the design feature of *RF* applications. The f_t is the frequency when the current gain is unity. f_t is the frequency at which the short circuit current gain of the device falls to unity, which depends upon ratio of g_m to the total capacitance. In the case of conventional MOSFETs, f_t is defined by [10]

$$f_t = \frac{g_m}{2\pi C_{gg}} \tag{3.5}$$

Further, Figure 3.14 (a) and (b) shows the f_t and f_{max} of GAA-TFET, demonstrated for different channel thickness (t) while keeping other parameters constant. The results are also compared with the same device of different radii. In order to fix the threshold voltage for different channel length at different radii are shown in Table 3.4. f_t and f_{max} are found to be increased with the increase in the channel thickness.



(a)



(

(b)

Figure 3.14 (a) Characteristics of cut-off frequency, and (b) Maximum oscillation frequency of Cylindrical GAA-Tunnel FET for different channel lengths at varying radii as a function of $V_{gs.}$

Table 3.4 Comparison of analog performance of DG-TFET for different channel length at different radii

L_{ch} ↓	R(nm) →	7	8	10
30nm	f_T	155.112	196.796	98.7
	f_{max}	325.116	373.175	279.826
	GBW	25.665	32.611	16.473
60nm	f_T	124.862	163.594	80.259
	f_{max}	243.354	279.125	230.177
	GBW	20.691	27.126	13.424
100nm	f_T	117.09	151.668	75.791
	f_{max}	169.528	192.678	150.596
	GBW	19.405	25.148	12.679

For all channel thickness variation *Si*-n channel TFETs show a superior performance. However , as we decrease the channel length in MOSFETs, g_m increases and gate capacitance values are decreased. Consequently, f_t of a MOSFET is inversely proportional to L_{ch}^2. In TFETs, g_m is nearly invariable with the change in channel length above 40 nm and so cut-off frequency depends only on gate

capacitances values and mainly C_{gd} which increases with increasing channel length, hence f_t is inversely proportional to L_{ch} i.e. above 40 nm channel length. As below it g_m starts to increase with respect to decreasing in length, due to which L_{ch} = 30 nm has highest cut-off frequency around 248.99 GHz at V_{gs}=1V and V_{ds}=1V as can be verified from Figure 3.14 (a).

It is also observed from the curve that initially cut off frequency starts increasing with gate-to-source voltage until it reaches its maximum value at specific gate to source voltage. The reason behind such behavior is that, as gate to source voltage increases, the number of electrons injected from source to channel via band to band tunneling increases and consequently g_m increases. Therefore, cut off frequency increases and reaches at its maximum value. It then falls with gate bias due to the combined effect of the increasing of the total gate-to-drain/source capacitance and limiting of g_m due to mobility reduction by the gate field. The peak point of *RF* figures of merit corresponds to the point between the minimum gate-drain/source capacitance and peak of g_m. Also, on varying the radius of the structure, in each case of *L* being 30 *nm*, 60 *nm*, and 100 *nm*, cut-off frequency is maximum at *R* = 8 nm at V_{gs} = 1.1V and V_{ds} = 1V in all the above three cases. As we vary the radius, g_m also varies as f_t is proportional to g_m and inversely proportional to L_{ch}. Earlier analysis shows that g_m is maximum at R= 8 nm as shown in the Figure 3.13 (b). The second important RF parameter is $f_{\max}$ which can be defined as the frequency when the power gain is unity. The $f_{\max}$ of a conventional MOSFET is computed as [80], [95]:

$$f_{max} = \frac{g_m}{2\pi C_{gs}\sqrt{4\left(R_g + R_s + R_i\right)\left(g_{ds} + g_m\left\langle\frac{C_{gd}}{C_{gs}}\right\rangle\right)}} \tag{3.6}$$

Where, R_g is the effective gate resistance, which is sum of the gate electrode resistance and distributed channel resistance. Gate electrode resistance could be neglected in this paper because a metal gate was used. Distributed channel resistance decreases as we decrease the length. Figure 3.14 (b) shows the comparison of f_{max} as function of gate to source voltage for different value of channel length for different radius. It is observed that f_{max} increases on decreasing the channel length as f_t increases as shown in Figure 3.14 (a). Further, on varying the radius, f_t produces maximum value for *R* = 8 *nm*, significantly, f_{max} is maximum for the same. The values of f_{max} for channel length 30 *nm*, 60 *nm* and 100 *nm* are 373 GHz, 279 GHz and 193

GHz respectively at R = 8 nm and V_{gs} = 1V. The graph also shows that the variation in f_{max} is more with respect to length and to the radius.

Another very important *RF* parameter is Gain Bandwidth Product (GBW). For MOSFETs, GBW is expressed as:

$$\text{GBW} = \frac{g_m}{20\pi C_{gd}} \tag{3.7}$$

On decreasing channel length in MOSFETs, g_m is increased and gate capacitance values are decreased and thus f_A is increased. Whereas, in TFETs g_m is invariable with respect to channel length but gate-drain capacitance increases on increasing channel length, and hence f_A is inversely proportional to channel length as can be seen in Figure 6. Where L_{ch} = 30 nm has maximum GBW i.e. 4.11×10^{10} Hz at R = 8 *nm* and V_{gsv} = 1.1 V. For radius, as observed earlier, current is maximum for R = 8 *nm* and so is $g_{m,}$ which dominates over gate capacitance value and thus GBW is also maximum for R = 8 *nm*, its values being 32.611 GHz, 27.126 GHz and 25.148 GHz for lengths 30 *nm*, 60 *nm* and 100 *nm*, respectively. Furthermore, Table 3.3 displays the values of *RF* figures of merit at V_{gs} = 1V. From the table, we observe that f_t, f_{max} and GBW are maximum for R = 8 *nm* at L_{ch} = 30 nm. On keeping fixed L_{ch} = 30 *nm*, the percentage decrease in f_t when compared to R = 8 *nm* is of 21.18 % and 49.84 % for R = 7 *nm* and 10 *nm*, respectively, whereas for f_{max} values of decrease being 12.88 % and 25.01 %, and the same being 21.30 % and 49.48 % for GBW. Similarly, on keeping R = 8 nm, the decrease in the *RF* figures of merits on comparing the lengths to 30 nm, f_t was found out to be decrease by 16.85 % and 22.93 % for lengths 60 *nm* and 100 *nm*, respectively. Whereas 25.20 % and 48.36 % for f_{max} with 16.80% and 22.88 % for GBW.

3.3 Summary

In this chapter, we systematically presented the comparative investigations on three structures of Tunnel FET using a spacer and band gap engineering for improved analog/*RF* performances. Here, the BTBT model is calibrated with the experimental data for accurate simulation. It was found that high analog/*RF* performance was achieved by employing low-k spacer width over Ge-source on drain underlap GAA-Tunnel FET. The design and physics of the examined device are mainly focused to achieve low sub threshold leakage and ambipolar behavior without affecting high I_{ON}.

A huge reduction of I_{OFF} and ambipolar behavior was noticed due to the combined effect of the spacer and band gap engineering in underlap structure. Thus, the proposed device would be beneficial in circuit design for a low power module of *SoC* applications**.** In addition, we analyzed for DC and Analog/*RF* parameters of Cyl GAA-Tunnel FET based on distinct device geometry. The device was confirmed to exhibit properties quite different from GAA-MOSFET because of the difference in their basic principles as tunnel–FET involves tunneling of carriers through the band gap barrier. During DC analysis drain current was found to be maximum at silicon radius of 8 nm, which was further influential in determining the variation of g_m and g_{ds} as well as *RF* parameters such as f_t, f_{max}, *GBW*, C_{gd} and C_{gs} with radius. ON-current did not seem to change much with length from 40 nm-100 nm. The simulation results successfully demonstrate the scaling effects of GAA-TFET on DC and *RF* performance. The investigation of device behavior would be useful for device analytical modeling and circuit design for high analog/*RF* application.

CHAPTER 4

Impact of Trap Assisted Tunneling (TAT) on 3D Cyl GAA-Tunnel FET for improved Device reliability

Despite high performance of the device, reliability is also a major concern. Previously, most of the simulated work has been studied and presented while assuming ideal direct tunneling for semiconductor body without any defects. Thus, not adequately explained and considered non idealities behavior within the semiconductor body. Note that during the device fabrication, it induces phonons and radiation that damage the results in conception of interface defects assisted tunneling causes reduction in device reliability and life time [35],[96]. Thus, large disparity was observed between experimental and simulation results. Therefore, in this work, we have presented the impact of trap-assisted tunneling (TAT) on 3D Cylindrical GAA-Tunnel FET for improved device reliability in terms of DC and analog performances such as I_{ON}, I_{OFF}, SS, I_{ON}/I_{OFF}, C_{gs}, and C_{gd}.

Here, performance analysis of the device with improved reliability has been focused, while included TAT physical model using 3D simulations of Synopsys Sdevice TCAD. Further, the design of device used the concept of hetero-spacer engineering (HTS) with drain underlap for improved DC and Analog/*RF* characteristics with reliability concern is examined. Moreover, the proposed device has been compared with the GAA-Tunnel FET based on homo spacer dielectric (HS).

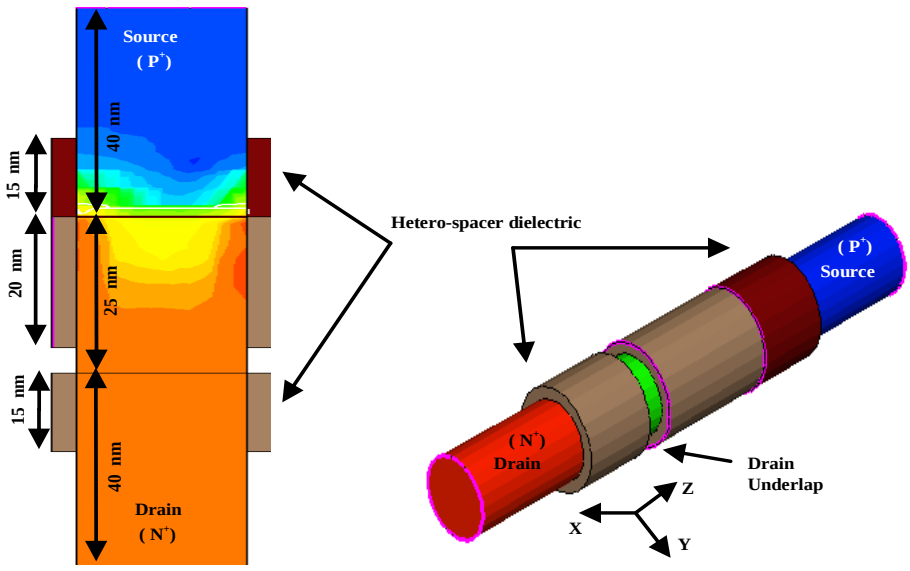
As discussed, TAT model included effects of trap charges i.e. band tails, defect assisted tunneling. It may exist during fabrication process like heavy doping and phonons. Hence, it also contributes to slightly larger *SS*. Although the given effects are minimize when compare to improve DC/Analog characteristics achieved in drain underlap (*DU*) based GAA-HTS.

4.1 Impact of Trap Assisted Tunneling on 3D Cylindrical GAA-Tunnel FET

In this work, we have systematically investigated the impact of trap assisted tunneling on the examined device performance of the 3D Cylindrical GAA-Tunnel FET regarding DC and analog performance. As discussed, spacers are basically insulator required for isolation to prevent carrier leakage over gate edge. Please note that dynamic non-local model offers the possibility to used three tunneling path such as TAT, direct tunneling path, and non-local TAT model. When adding the TAT model to the physics of the simulation, a tail at lower gate voltage appears due to the dominant TAT component at low electric field [63], [97]. In all the cases, default parameters for silicon (*Si*) are used in order to achieve high thermal stability and consistency. This is because *Si* act as a masking layer to prevent the diffusion of the dopants in the region it protects.

4.1.1 Device Structure and Analysis

The device structures along with various device parameters are shown in Figure 4.1(a) and 1(b). It shows the cross-sectional and 3D view of *DU* Cyl-GAA-nTFET based on hetero spacer engineering. Here *DU* means drain side underlap only.



(a) (b)

Figure 4.1 (a) Cross-Sectional view, and (b) 3D view of drain underlap (DU)-Cyl-GAA-TFET with HTS. Here, gate length (L_g) = 20 *nm*, spacer width (L_s) = 15 *nm*, oxide thickness (t_{ox}) = 2 *nm*, and thickness of high-k dielectric (HfO_2) = 2 *nm* are used.

Here, HTS means low-k spacer dielectric (SiO_2) is placed over source region and high-k spacer (HfO_2) over drain region. To evaluate the merits of the proposed HTS based GAA-TFET, it has been compared with the homo-spacer dielectric (*HS*) of GAA-TFET with the same device geometry. Whereas in *HS*, high-k spacer dielectrics (HfO_2) are placed over both sides of the gate i.e. source and drain. For fair comparisons we have used the same geometrical structure and device parameters such as gate work function, doping concentrations, gate dielectric with the same gate source voltage (V_{gs}) scale for both the structures. The threshold voltage (V_t) is extracted using constant current method ($10^{-9}A/\mu m$).

The physical models comprises the device simulations based on BTBT are kane's model, schenk model, hurkx BTBT model and the dynamic non-local BTBT model. Here non-local trap-assisted tunneling (TAT) model and non local BTBT model was used with field-dependent mobility, and band gap narrowing (BGN) model.

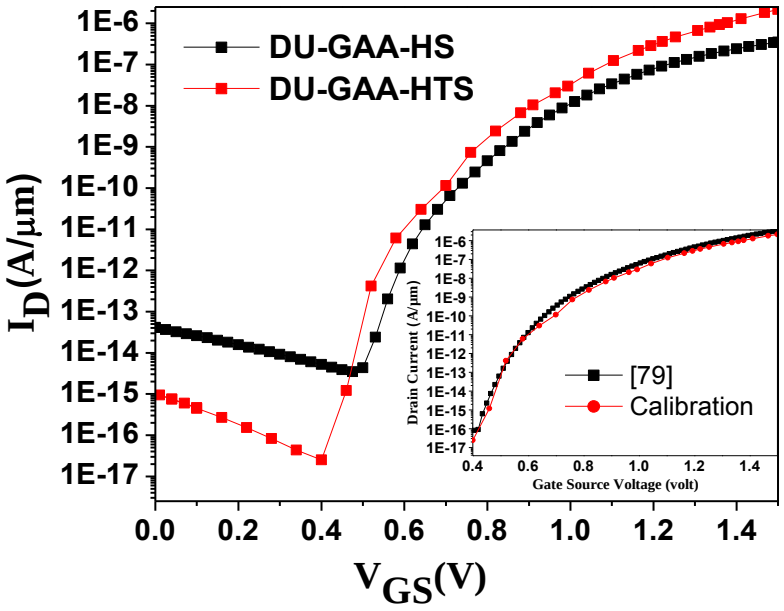
4.1.2 Device Model and Parameters

In this device, when the TAT model is included, the simulations are much closer to the experimental data. To calibrate the non-local BTBT model, mass of electron (m_e) and mass of hole (m_h) for silicon (*Si*) are taken as 0.24 and 0.34, respectively. $A_{path} = A = 4\times10^{14}$ $cm^{-3}s^{-1}$, and $B_{path} = B = 1.9\times10^{7}$ Vcm^{-1}, where *A* and *B* are material dependent parameters. The values of other parameters for the non-local model are kept to their default value as projected for *Si*. Since the tunneling process is non-local, therefore the mesh was carefully refined in the applied zone, where tunneling can take place in order to assure both convergence and correct simulation of the device. Asymmetrical doping profiles are used for all the regions to make abrupt junction. P-type source ($1\times10^{20}/cm^3$), N-type drain ($1\times10^{18}/cm^3$), and P-type channel region ($5\times10^{17}/cm^3$) are shown in Figure 4.1(b). Because of the increased oxide capacitance, HfO_2 is used as a gate dielectric (k = 21) with gate work function = 4.53 e*V*.

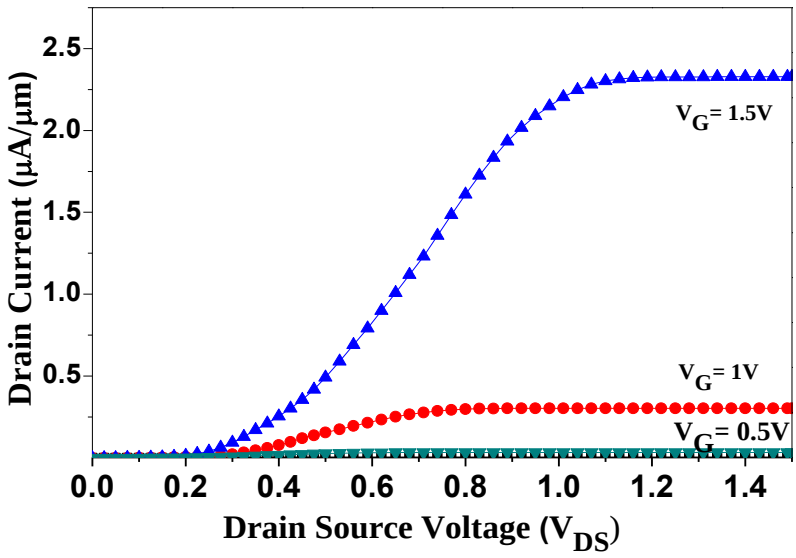
4.1.3 Impact of Trap Charges on DC Characteristics

In this work, we have investigated Cylindrical GAA-TFET based on hetero-spacer engineering with asymmetry in underlap, while incorporating TAT physical model during three-dimensional (3D) simulation. This is because it includes experimental non-idealities like defects and phonons on tunneling zone using trap analysis of

charge carriers. To calibrate the models, the GAA-TFET has been designed with the same device parameters as shown in experimental work of [79].



(a)



(b)

Figure 4.2 Transfer characteristics of DU GAA-TFET with hetero and homo spacer dielectric at Vg = 1.5V. The effective channel length is 25 nm. The inset shows the calibration of our simulation result with [79], and (b) Id-Vds Characteristic of DU GAA-TFET with HTS for different value of gate voltage while keeping source voltage (Vs) = 0.

In our proposed device, the hetero-spacer dielectric (HTS) comprises different spacer dielectric at the drain and source sides i.e. low-k spacer is placed over source side of the gate and high-k spacer is placed across drain side to improve fringing field across the surface.. The proposed device also supports for fabrication by reducing the

complexity of process of fabrication. This is because of its structure having all around cylindrical symmetry across the source, drain, and channel. Hence it can be easily process when compared to other existing GAA structures of [53], [56], [77].

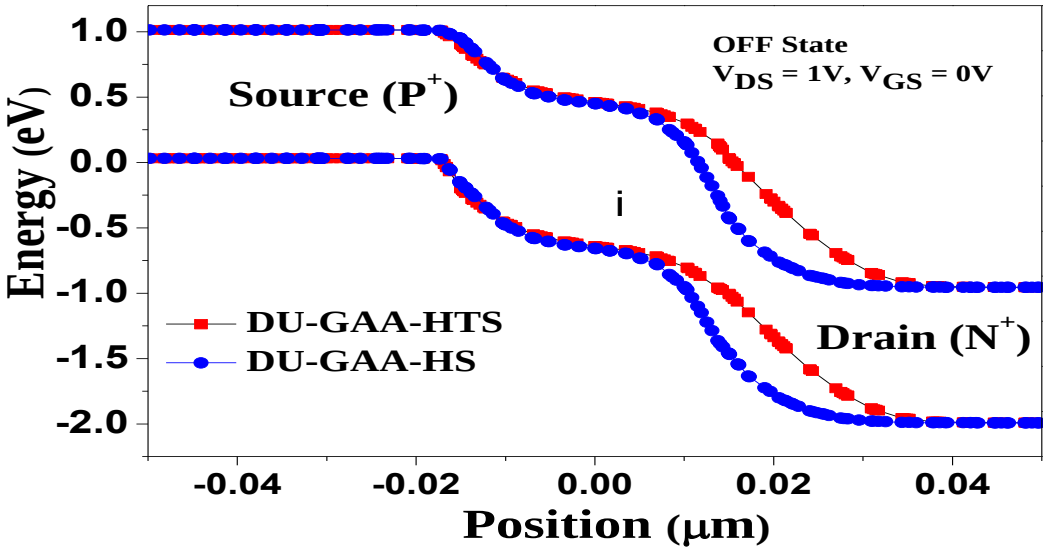
Here, we have investigated the device performance in terms of DC and AC characteristics such as I_{ON}, I_{OFF}, *SS, and* I_{ON}/I_{OFF} with associated gate source (C_{gs}) and gate drain capacitance (C_{gd}). All of the capacitances are extracted from the small-signal AC simulations at a moderate frequency of 1MHz. The proposed channel length is considered as 25 nm In Gate-all-around structures, gate is wrapped around all sides over the channel, which may contribute depletion of the source/drain towards gate. In this concern, spacer engineering plays an important role to prevent carrier leakage over the gate edge. Further, Figure 4.2 (a) shows the comparison of the transfer characteristics of drain current for n-channel DU GAA-TFETs with varying spacer dielectric. The ON current (I_{ON}) and I_{ON}/I_{OFF} for DU GAA-TFET with HTS are 6 and 1024× when compared with homo-spacer dielectric (HS) at Vgs = 1.5 V. The experimental results are also studied and found that I_{ON} and I_{ON}/I_{OFF} for GAA-HTS are 0.6× and 83× high when compared with [89]. Also low gate drain capacitance of 1.75 fF can be extracted using AC simulation with low *SS* of 52 *mV/decade* as shown in Table 4.1.

Table 4.1 Comparison of device parameter values for DU GAA TFET with hetero and homo-spacer dielectric

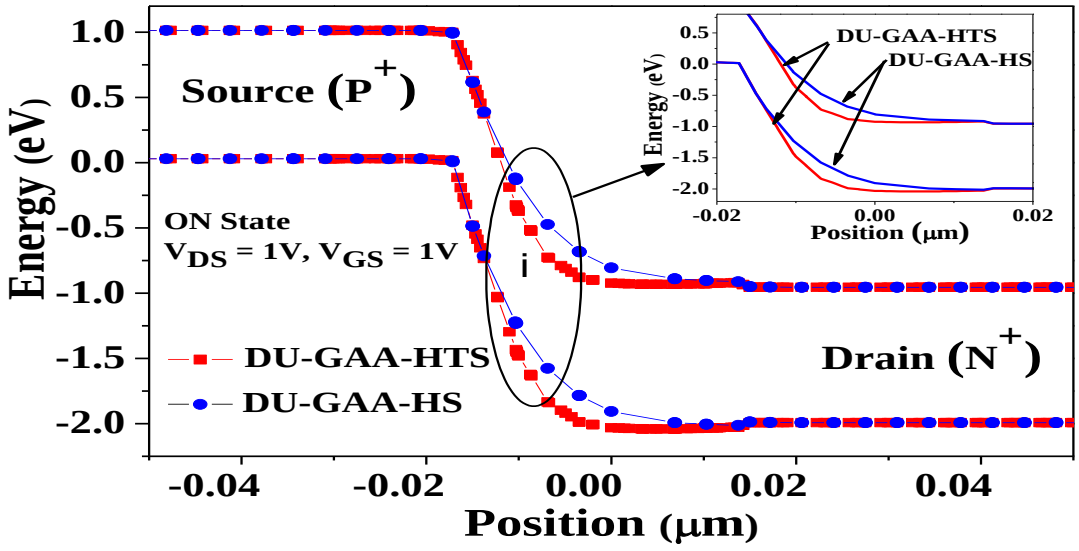
Parameters	**DU GAA-HTS**	**DU GAA-HS**	**[89]**
I_{ON} (A/µm)	2.10×10^{-6}	3.50×10^{-7}	0.3×10^{-6}
I_{OFF} (A/µm)	2.51×10^{-17}	4.32×10^{-15}	0.30×10^{-13}
I_{ON}/I_{OFF}	0.83×10^{11}	0.81×10^{8}	10^{7}
SS (mV/dec)	52.6	55.9	90
C_{gd} (F)	1.75×10^{-15}	6.15×10^{-15}	-
C_{gs} (F)	0.48×10^{-15}	0.09×10^{-15}	-

Figure 4.3 (a) shows the OFF state operation of Tunnel FET, where no BTBT occurs, since the potential barrier exists between the source and the channel. Whereas, during ON state, the gate voltage pulls down the energy band of the channel region and width of the tunneling barrier reduces. Therefore, charge carriers can tunnel from the

valence band of the source to the conduction band of the channel region as shown in Figure 4.3 (b). At the same time, drain underlap compromises the channel resistance to be divided into gate resistance ($R_{with\text{-}gate}$) and without gate resistance of the channel region ($R_{without\text{-}gate}$). Therefore, an extension of the drain-channel region without gate occurs, which causes increase in $R_{without\text{-}gate}$ of the drain-channel region with decrease in $R_{with\text{-}gate}$. Hence, it enhances the gate controllability over the source-channel and causes variation in electron-current density across the drain channel length and depth [56], [59].



(a)



(b)

Figure 4.3 Comparison of energy band diagram for DU Cyl-GAA with hetero and homo spacer dielectric in the case of (a) OFF state, and (b) ON state. The inset shows the position of band bending between the valence band of the source and conduction band of the channel during tunneling of charge carriers.

This optimized result is obtained due to the implementation of hetero-spacer dielectric i.e. low-k spacer placed at the source side, which reduces the fringing fields, and the depletion zone does not form at the source–gate edge. Hence the suppression of the depletion zone results to the high source channel tunneling at the device surface, and consequently, it increases the I_{ON} that flows through the device. Specifically, we found that electric field by the gate voltage over the drain channel region is gradually weakened, which has no effect on $I_{ON.}$ Accordingly, it is observed that pushing of the gate end away from the drain junction reduces the tunneling at the drain channel junction. Therefore, low I_{OFF} with steepest ambipolar behavior and subthreshold swing was achieved as shown in Figure 4.2 (a). It may also be verified from the transfer characteristics in Figure 4.2 (b) that drain current (I_d) increases for a further increase in gate-source voltage (V_{gs}). Conclusively, it is observed that low source-spacer dielectric (k = 3.9) with drain underlap causes less fringing field in the source near the gate edge. This is because of the non depletion of the source towards gate side by low-k spacer as shown in Figure 4.4.

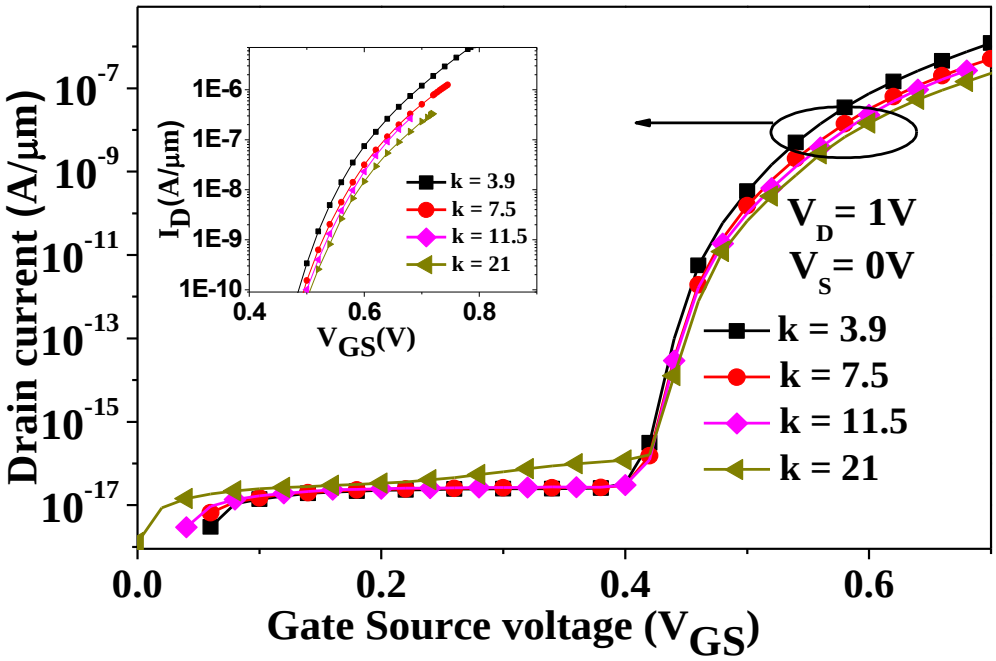


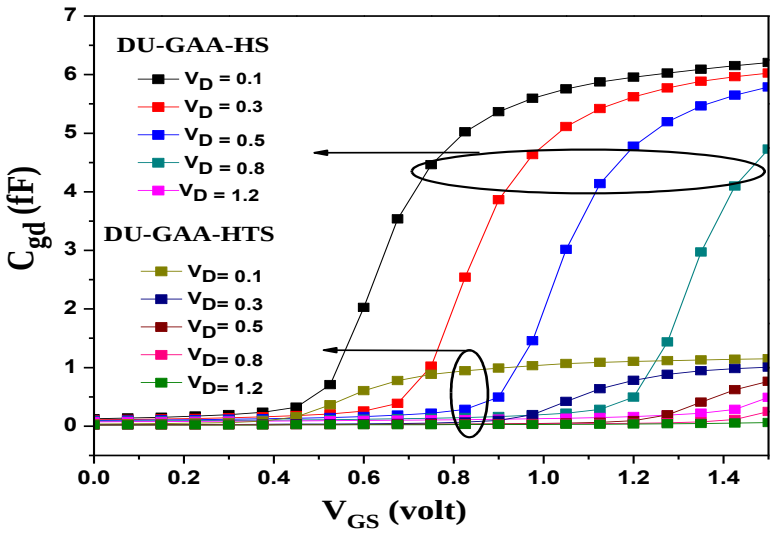
Figure 4.4 Transfer Characteristic of DU GAA-TFET for different values of the source spacer dielectric on V_{gs} scale of 0.8 *V*. The inset shows the output characteristics in defined gate source voltage of drain current for increase in value of source spacer dielectric (k).

Significantly, it shows gradual fall in I_d with increase in values of the source spacer-dielectric Low-k spacer enhances the fringe field within the spacer as compared with that of high-k spacer dielectric placed across drain side. This phenomenon leads to carrier tunneling at the surface only and not inside the body. As a consequence, it

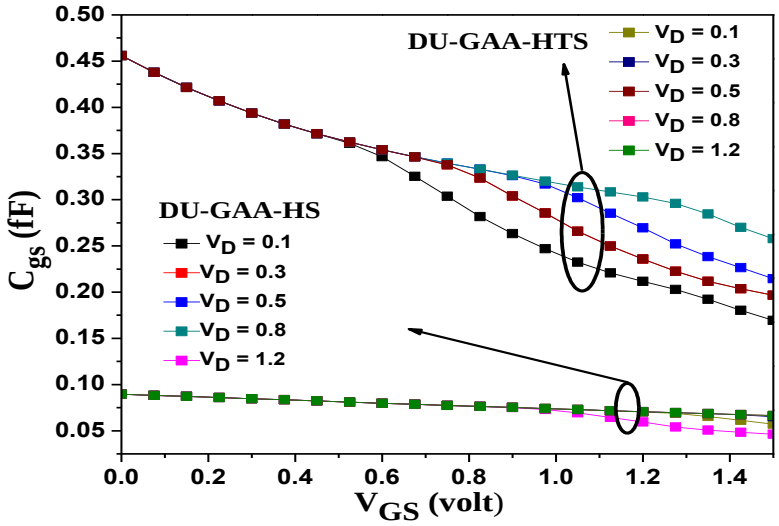
leads to high electric field occurs across source-channel junction with reduced ambipolar behavior and gate drain capacitance due to asymmetry in underlap based structure.

4.1.4 Impact of Trap Charges on Parasitic Capacitances

Here, Figure 4.5 (a) and (b) analyze the gate drain capacitance and gate source capacitance, respectively of both the devices for different value of drain voltage (V_d). C_{gd} is the miller capacitance and in order to improve the TFET switching speed with low dynamic power, parasitic capacitances should be reduced. Now, $C_{gd} = C_{of} + C_{dif} + C_{dov} + C_{gdinv}$, and $C_{gs} = C_{of} + C_{sif}$ [90].



(a)



(b)

Figure 4.5 (a) Analysis of gate-to-drain capacitance (C_{gd}), and (b) Gate to source capacitance (C_{gs}) as a function of the gate to source voltage (V_{gs}) for different value of V_{ds} for Ge-GAA-HTS.

Where, C_{of} is the outer fringing capacitance related to the fringing field effects between the gate electrode and the channel. Cdov is the drain overlap capacitance. C_{dif} and C_{sif} are the inner fringing capacitances at drain and source side, respectively.

Sometimes parasitic capacitances may vary due to charge variation in the channel close to source or drain. However, on varying the position of the drain body junction with respect to the gate edge, e.g. by controlling the drain doping profile, C_{of} and C_{dov} can be adjusted. It is observed that on increasing the value of gate to source voltage (V_{gs}). C_{gd} increases owing to the formation of inversion layer increases towards the source from drain below gate oxide for increasing value of drain voltage or in other terms due to reduction in channel to drain potential barrier. Whereas C_{gs} in figure 4.5 (b), drops slightly with an increase in V_{gs}. The reason behind this being that the coupling reduces between the source and the gate due to the extension of the inversion layer and presence of potential barrier. The forgoing observations are also in consistence with that reported in [98]. As a consequence, the proposed device consists of *Si* semiconductor produces low leakage current, low miller capacitance (C_{gd}), which leads to abrupt control switching with concern of reliability and consistency. Thus, our device also satisfies the requirement of low power applications with improved device reliability.

4.2 Summary

A systematic investigation of the impact of the underlap structure with hetero and homo spacer dielectric on the device performance of a GAA-TFET has been made. Whereas, experimental non-idealities of real device fabrication have been analyzed when included TAT model. Thus, it is found that the combination of drain underlap with low-k spacer placed over source region reduces the fringing field within the spacer with increase in resistance of drain channel junction produces the best device performance in terms of DC and AC characteristics with suppressed ambipolar behavior, and abrupt ON-OFF transition. These performances are mainly achieved due to non depletion of the source towards gate side and better gate controllability over the channel, which leads to source-channel tunneling inside the surface instead of tunneling towards the body influence by low spacer dielectric placed over source region. Further, we have analyzed the real device fabrication condition by using the

trap assisted tunneling (TAT) model that allows the trapping of charge carriers inside the oxide of the device and analyzed the impact of trap charges during tunneling of charge carriers of the device and significantly its effects on the device performance for improved reliability. Hence, the proposed can also be very attractive for low power applications with improved reliability.

CHAPTER 5

Performance Enhancement of Cross Coupled Voltage Doubler Design based on 3D Cyl GAA-Tunnel FET using Device Circuit Co-design Approach

The ongoing development of internet of things (*IoT*) era promotes low power design, high driving capability, process optimization, and smart peripherals design with reliability approach within device, circuits to architecture levels. In particular, such designs are best suitable for the utilization at remote location for longer period. Therefore, an *IoT* design required energy harvesting circuit or device level techniques under a low range of voltage [99]. Further, energy harvesting comprises energy utilize from the environment and convert it to electrical energy. The energy sources are basically hydraulic, solar, kinetic, electromagnetic and thermal energy. In addition, *IoT* system needs high speed with high energy efficiency design based on low power device to fulfill the requirement of ultra low power applications [100]. Recently, many research have been specifically focus towards the development of smart and small devices with their peripheral circuit to the external world for emerging *IoT*, which is mainly possible due to extremely low power consumption of the devices that acquire information from sensors and transmit the information towards destination deploy at remote location for *IoT* perspective [64], [65]. It also has an ever increasing demand for longer battery life and low power emerging devices while maintaining high performance [101].

Therefore, to satisfy the requirement of *IoT* system, the low power emerging devices have been analyzed and scaled continuously in order to achieve high density, high speed, and low operating power. However as discussed, assertive device scaling produces severe *SCEs*, which promote high leakage current and significantly leads to high power consumption [92]. In this regard, Tunnel FET considered as a promising novel device for future low power circuits [34]. However, low power device with reliability concern is not only the solution of *IoT* system.

Here, we need high efficient circuits based on low power for driving the target system. In this regard, the cross coupled voltage doubler (*CCVD*) is the most suitable circuit for the requirement of applications that used as energy harvesting circuit with *IoT* system at remote locations. It can also be used to enhance the available low supply voltage up to required supply voltage to operate the system. In short, the *CCVD* is basically a type of switched capacitor DC-DC converter in which the output voltage is about twice of the input voltage. It also reduces the ripple in voltage with the same frequency as compared to the conventional charge pump [66]. This is mostly used with DC to DC converter over small battery source to power the *IoT* applications. The efficiency of the voltage doubler leads to low power dissipation and higher switching speed over conventional CMOS technology [67]. However, the power efficiency of the *CCVD* is limited due to reversion loss. The charges move from higher voltage nodes to lower node produces some leakage current known as reversion loss.

Therefore, in this chapter, a low *CCVD* based on Cyl GAA-TFET with improved reliability is presented for *IoT* applications. Here device circuit co-design investigations have been made for circuit performance parameters such as Power efficiency, Output voltage, and Energy consumption using 3D TCAD mixed-mode simulations. Further, the proposed circuit nullifies the reverse leakage current due to the arrangement of two non-overlapping clock signals with the tunnel transistors based on hetero-material. Initially, we have optimized the device as per required circuit applications. Moreover, the proposed device was well calibrated and investigated under the influence of trap charges while included *TAT* physical model in the 3D simulations of the proposed device for improved reliability towards the *CCVD* Circuit.

5.1 Device Design based on *Ge* Source

As discussed in device literature, the *Ge*-source based Tunnel FET design achieves much higher I_{ON} due to the smaller band gap of the *Ge* and effective mass produces high band-to-band tunneling rate as compared to *Si* at low voltage. However, *Ge*-TFET suffers from excessive off-state leakage current despite its high (I_{ON}) and causes degradation in the device performance. Therefore, in this work, The *Ge*-source based on Cyl GAA-TFET with low spacer width is investigated for low power circuit applications as shown in Figure 5.1. Note that the TFET in combination with *Si* and

Ge material causes superiority in their performances in such a way that TFET works under reverse biasing and *Si* is the only material to provide highest reverse saturation current during reverse biasing. Thus, it promotes ease of fabrication processing, and lower cost due to its structure of all around cylindrical symmetry across the source, drain, and channel. As discussed in previous chapter, the high performance result is obtained due to the implementation of low spacer width placed over the *Ge* based source region, which reduces the fringing fields, and causes non-formation of the depletion zone at the source¸ gate edge. Hence the suppression of the depletion zone, results to the high source channel tunneling at the device surface only, not inside the body, leads to high I_{ON} as shown in Figure 5.2. At the same time, drain underlap increases the drain-channel resistance, and causes the electric field weakened, which has no effect on I_{ON}. Consequently, it reduces the rate of tunneling at the drain channel junction and thus, low I_{OFF} with steepest *SS* as shown in Table 5.1 and compared with experimental data [89].

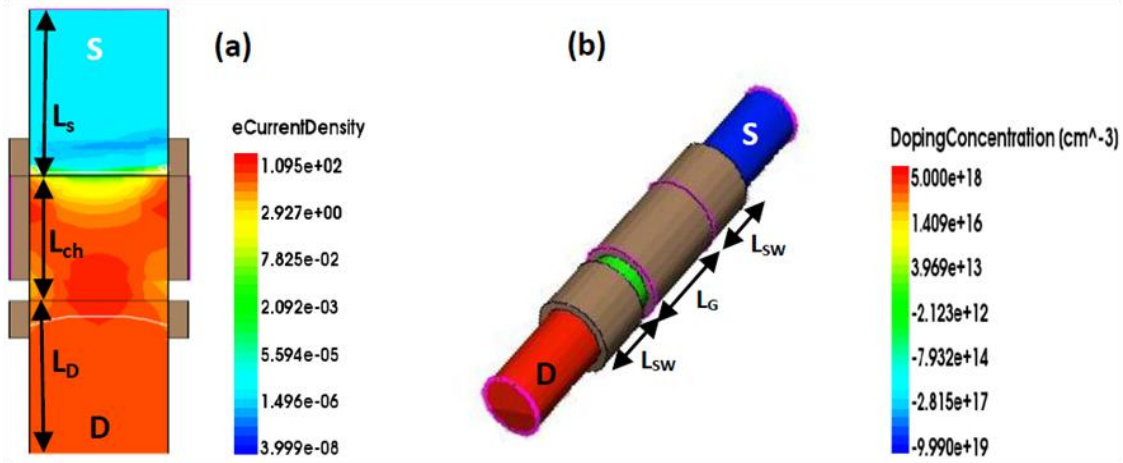


Figure 5.1 (a) Cross-sectional view and (b) 3D view of asymmetrical underlap (*AU*) Cyl-GAA-TFET based on Ge-source with low spacer width (*LSW*) along channel length direction with magnitude of e-current density and doping concentrations.

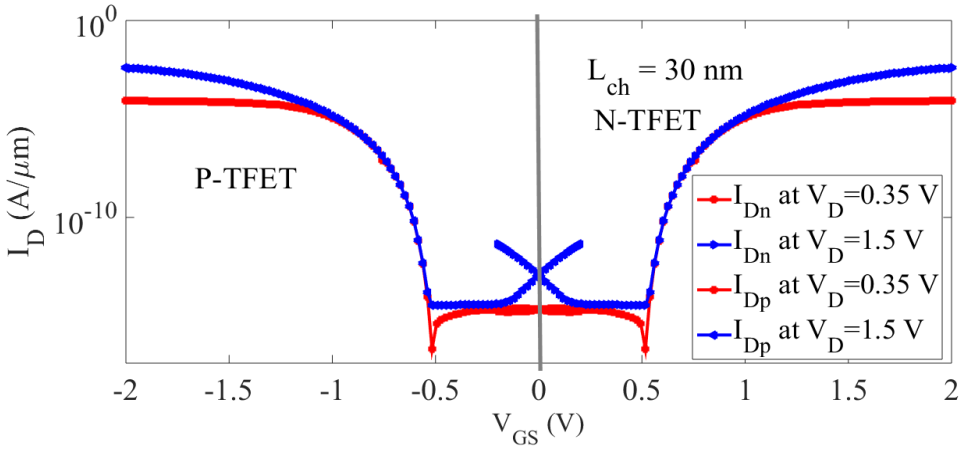


Figure 5.2 Transfer characteristics of Cyl GAA-Tunnel FET.

Table 5.1 Device design parameters of proposed structure with experimental data

Parameters	**Our work at V_{DD} = 0.35 V**	**Our work at V_{DD} = 1.5 V**	[89]
I_{ON} (Amp/μm)	0.83×10^{4}	3.8×10^{4}	0.3×10^{-6}
I_{OFF} (Amp/ μm)	2.09×10^{-17}	3.43×10^{-15}	9.2×10^{-13}
I_{ON}/I_{OFF}	0.39×10^{13}	1.10×10^{11}	10^{7}
SS(mV/dec)	25.8	28.3	90

Although as discussed, most of the simulated work assumes ideal direct tunneling. Thus, not address the disparity between experimental and simulation results. Therefore, they were not adequately explained non idealities mechanism within the semiconductor body such as interface defects and phonons [96]. Note that during device fabrication, the process induced phonons and radiations that damage results in conception of interface defects assisted tunneling causes reduction in device reliability and life time [35], [63]. Furthermore, presence of interface traps at the Si/SiO_2 interface results into degradation of electric field along the channel length at the tunneling junction and significantly results in degradation of DC and analog/*RF* performance of the device [102].

Thus, the device reliability issue is always a major concern. Here to address the above issues, we have analyzed experimental non idealities, while included trap assisted tunneling (*TAT*) model and phonon assisted tunneling (*PAT*) paths in the 3D simulation of our proposed device at low voltage. Further, Table 5.1 shows the DC characteristics of the optimized device. It has high I_{ON} (0.83×10^{4}A/μm), low I_{OFF} (2.09×10^{17}A/m), and an enhanced I_{ON}/I_{OFF} (10^{13}) with low *SS* of 25.8m*V*/decade achieved at low drain voltage of 0.35 *V*. The proposed results are well analyzed using *TAT* model at drain voltage of 0.35 *V*, 1.5 *V*.

5. 2 Device Models and Parameters

Recently based on the International technology roadmap for semiconductor (ITRS) report of Tunnel FET, ITRS-2018 targets for low power of 0.57 V, which is most important for low dynamic power circuits in *IoT* perspective [103]. The physical

models comprises the device simulations based on BTBT are kane's model, schenk model, hurkx BTBT model and the dynamic non-local BTBT. Here, non-local BTBT model is included combined with a field-dependent mobility, band gap narrowing, and Shockley-Read-Hall recombination model at 300 K via 3-D simulations of the TCAD Sentaurus Sdevice [49]. In addition, e-quantum model, TAT and PAT model are included to analyze quantum and trap analysis effects over the optimized device. The non-local BTBT models are fitted with the experimental data of [60]. The fitted *A* and *B* coefficients are $A_{path} = A = 1.46\times10^{17}/cm^3s$ and $B_{path} = B = 2.59\times10^{6}$ *V*/cm. The doping concentrations used are P-type source 1×10^{19} /cm^3, n-type drain 5×10^{17} /cm^3, and p-type channel region 1×10^{18}/ cm^3. The HfO_2 is used as a gate dielectric as well as spacer dielectric (k = 21) with gate work function = 4.53 e*V*. Here, we have developed a Verilog-A device model for the proposed device. Furthermore, Figure 5.3 shows the flow chart of circuit evaluation from the proposed device.

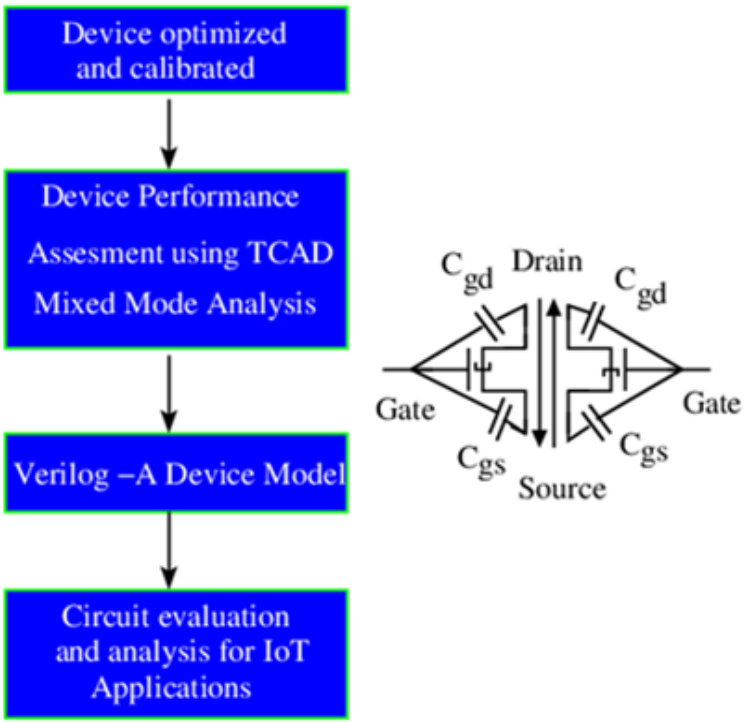


Figure 5.3 Flowchart for the simulation methodology used in the design and modeling of the *CCVD* design based on Cyl GAA-Tunnel FET.

5.2.1 Capacitance Extraction of the Device

Figure 5.4 (a) and (b) analyze the gate drain capacitance (C_{gd}) and gate source capacitance (C_{gs}), respectively for p and n-channel cylindrical GAA Tunnel FET under different value of drain source voltage (V_{ds}).

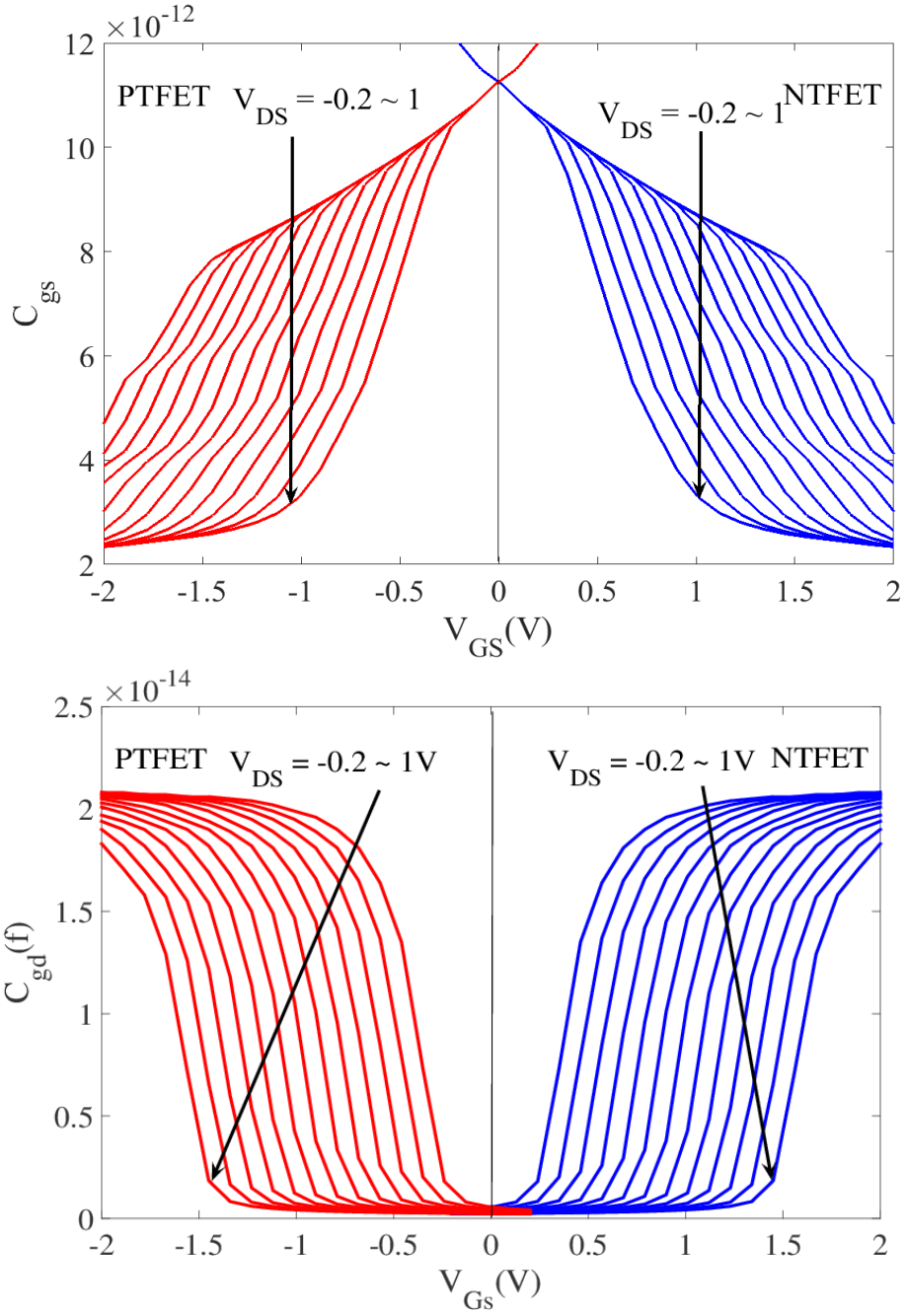


Figure 5.4 Device capacitance extraction (a) Characteristics of gate-to-drain capacitance and (b) gate-to-source capacitance as a function of gate to source voltage (Vgs) for different value of Vds on p and n channel Cylindrical (Cyl) GAA-Tunnel FET.

Here, $C_{gd} = C_{of} + C_{dif} + C_{do}v + C_{gdinv}$ and $C_{gs} = C_{of} + C_{sif}$. Where, C_{of} is the outer fringing capacitance related to the fringing field effects between the gate electrode and the channel. C_{dov} is the drain overlap capacitance. C_{dif} and C_{sif} are the inner fringing capacitances at drain and source side, respectively [90].

The Verilog-A model used herein is comprised of look-up tables tabulating I_{ds} (V_{gs} and V_{ds}), I_{gs} (V_{gs} and V_{ds}), C_{gs} (V_{gs} and V_{ds}), and C_{gd} (V_{gs} and V_{ds}) characteristics of the Cyl GAA-Tunnel FET device within the working bias range are investigated in this work. Using this custom Verilog-A model, circuit analysis was then performed via HSPICE circuit simulator [104]. Furthermore, Figure 5.5 (a) shows the symbolic representation of n-type Cyl GAA-TFET, and (b) shows the Cyl GAA-TFET based Inverter, and (c) shows the voltage transfer characteristics of proposed inverter, respectively.

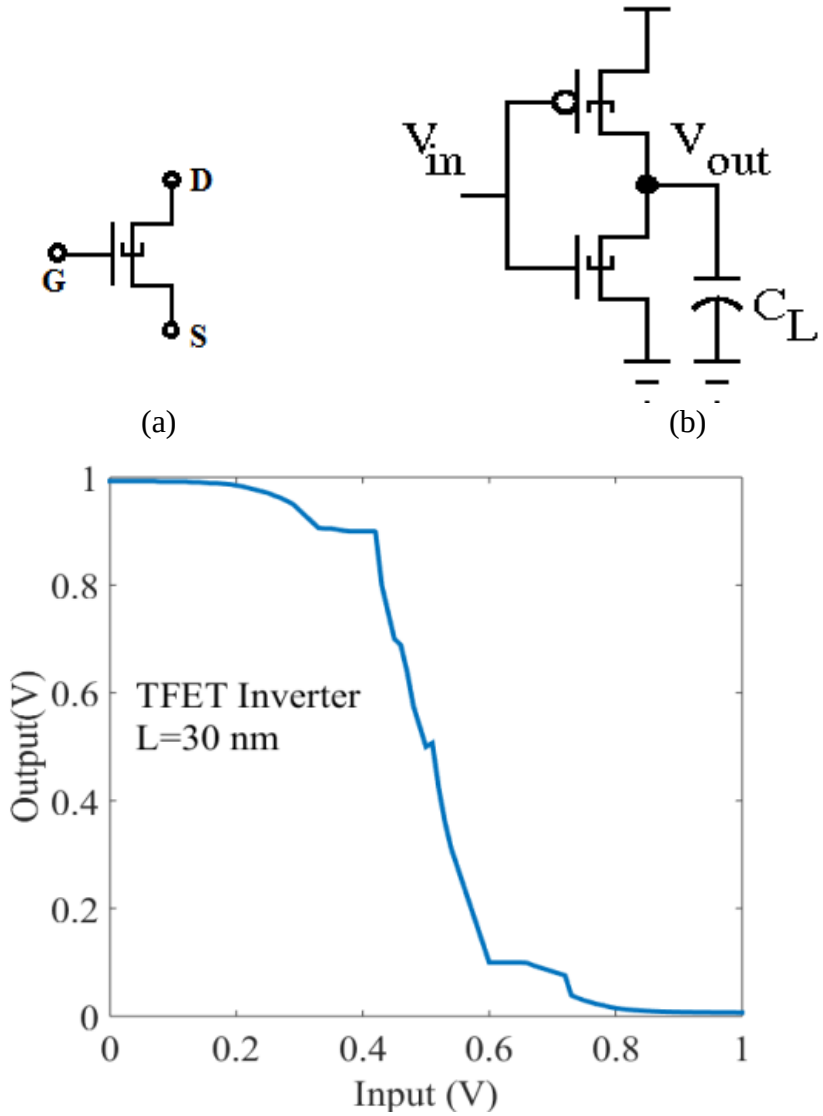


Figure 5.5 Circuit characteristics (a) symbolic representation of n-channel Cyl GAA-Tunnel FET, (b) Cyl GAA-Tunnel FET based Inverter circuit with load capacitance, and (c) Voltage transfer characteristics of proposed device based Inverter.

5.3 Cross Coupled Voltage Doubler based on 3D Cyl GAA-Tunnel FET

Figure 5.6 (a) shows the schematic circuit of *CCVD* based on Cyl GAA-Tunnel FET with non overlapping clock scheme. In the circuit, T_1 and T_3 are the two transistors based on the proposed tunneling device form the first inverter, whereas T_2 and T_4 form the second inverter for the cross-coupled operation. These two inverters are connected in cross-coupled mode and storing nodes are connected with the charging capacitors, Here C_1 and C_2 are the two flying capacitors and C_L is the load capacitor. The switches Q_1 and Q_2, which can close and open the capacitors controlled by the two phase non-overlapping clock are shown in Figure 5(b).

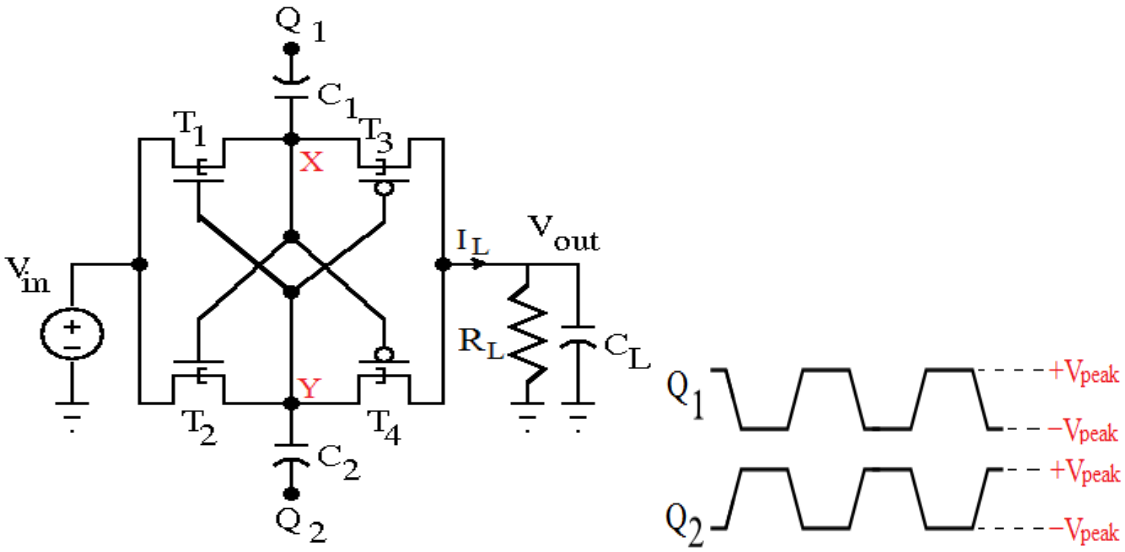


Figure 5.6 (a) Schematic diagram of the Cross Coupled Voltage Doubler (CCVD), (b) Non-overlapping control scheme

The operating frequency is set as 50 MHz for the non-overlapping clock signal. These clock signals must operate in the break-before make fashion to reduce the shoot-through current during switching. In the steady state, the transistors are operated in the linear region. In the first phase, when switch Q_1 is ON, T2 will ON and T_4 will come under cut-off mode. Meanwhile, Q_2 is OFF and charge voltage across C_2 causes the transistor T_3 to be ON. In this circuit, C_2 is charge by V_{in} voltage and Q2 will also charge by V_{in} voltage through transistor T_2 and therefore, C_2 voltage will be $V_{in} + V_{in}$. At the same time T_3 is ON and it passes output voltage through the C1 capacitor to the R_L. Significantly, switch Q_2 is ON, it makes T_1 ON and T_3 OFF, leads to the charging

of capacitor C_1 through additional voltage V_{in} and T_4 is ON through Q_1 that passes the C_2 charge to the output that is $2V_{in}$. In the proposed design, to simplify the analysis for two-phase non-overlapping clock signal in order the ensure that duty cycle should be less than 50 %, the duty cycle of the clock is assumed to be 50%. During the steady state for complete a clock cycle; the charges supplied by the power supply must be equal to the charges delivered to the load. Because the load current (I_L) is non-zero, the computations of charges delivered in one clock cycle are given by $Q_T = I_L T$, here T is the clock period. The charges can be transferred to the flying capacitors C_{F1} and C_{F2}. The drain current (I_D) of the transistors are near to I_L. Also, the current through the transistors have two components, which are defined as charging current of the capacitor (I_C) and I_L. The time constant at the output is defined as $C_L R_L$.

5.4 DC Model of the Cross Coupled Voltage Doubler Design

To understand the working of the rectifier, we have bisected the cross coupled voltage doubler as shown in Figure 5.7.

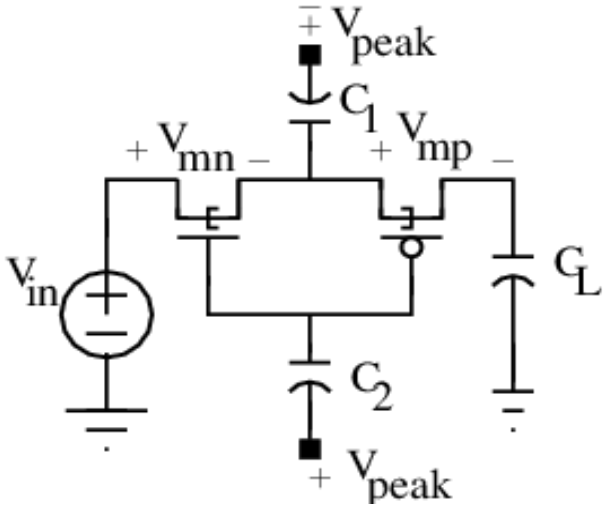


Figure 5.7 Bisector view of the *CCVD* circuit.

Here, $+V_{peak}$ and $-V_{peak}$ are the peak amplitude at Q_1 and Q_2. V_{mp} and V_{mn} is the voltage drop across PMOS and NMOS transistor, respectively. The analysis is performed for peak amplitude of Q_1 input. This peak amplitude is considered to be greater than threshold voltage (V_t) of the transistor. Charging and discharging phase activation depends on the switch conditions. The charging phase is activated, when positive signal appears at the terminal Y, which turns ON the NMOS transistor. Whereas, the discharge phase is activated when negative signal appears at the terminal Y, which

turns ON the PMOS transistor. The charging and discharging phases of bi-sectional view are shown in Figure 5.8 (b) and (c). Further, Figure 5.9 shows the Input-output characteristics of the model and simulation of the CCVD design.

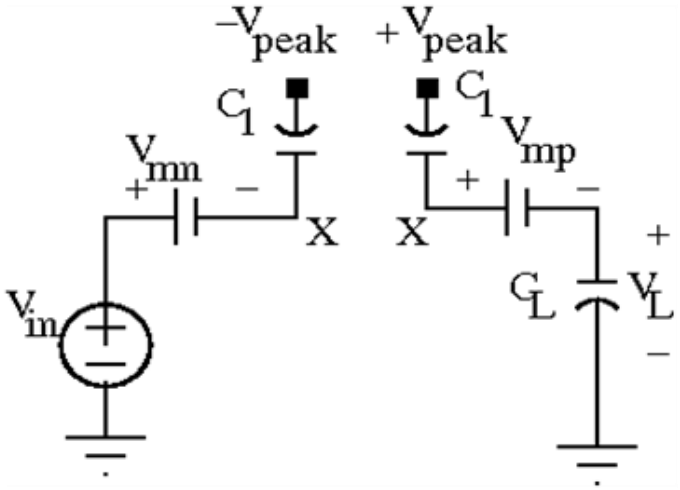


Figure 5.8 modeling of the proposed *CCVD* Design for charging phase and discharging phase

On apply KCL during charging phase,

$$-V_{peak} = V_{C1} - V_{mn} + V_{in} \tag{5.2}$$

During charging phase, the voltage across capacitor C_1 for peak amplitude V_{peak} is given by:

$$V_{C1} = -V_{peak} + V_{mn} - V_{in} \tag{5.3}$$

Similarly, apply KCL during discharging phase. In this phase, charges are stored in C_1 will be transfer to the load capacitor (C_L). Hence

$$+V_{peak} = V_{C1} - V_{mp} + V_L \tag{5.4}$$

From equations (5.2) and (5.3)

$$+V_{peak} = -V_{peak} + V_{mn} - V_{in} + V_{mp} + V_L \tag{5.5}$$

$$V_L = 2V_{peak} + V_{in} - (V_{mn} + V_{mp}) \tag{5.6}$$

For the first stage of rectifier $V_{in} = 0$. Hence output of single stage cross coupled rectifier is given by:

$$V_L = 2V_{peak} - (V_{mn} + V_{mp}) \tag{5.7}$$

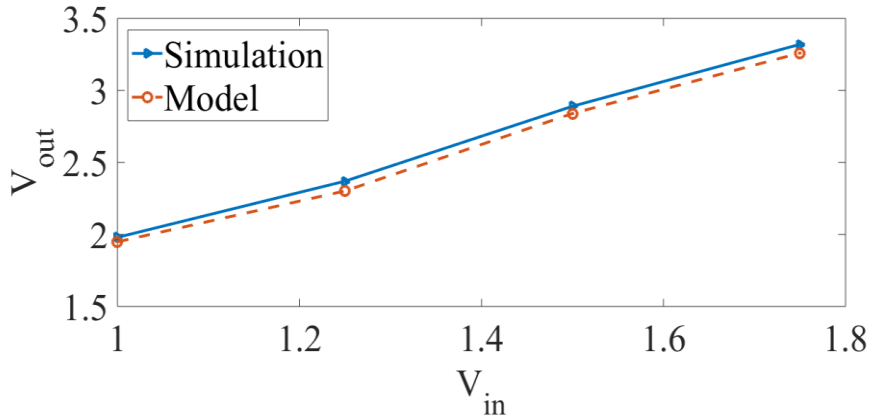


Figure 5.9 Input-output characteristics of the model and simulation of the proposed design

5.5 Circuit Parameters of the CCVD Design

In this design, each of the flying capacitors say C_1 and C_2 are 10 pF and the load capacitor (C_L) are 1000 pF. The two auxiliary capacitors are 5 pF, respectively. The output voltage of the proposed design with respect to time for the different values of input voltage while keeping fixed value of load resistance (R_L) of 80 MΩ is shown in Figure 5.10.

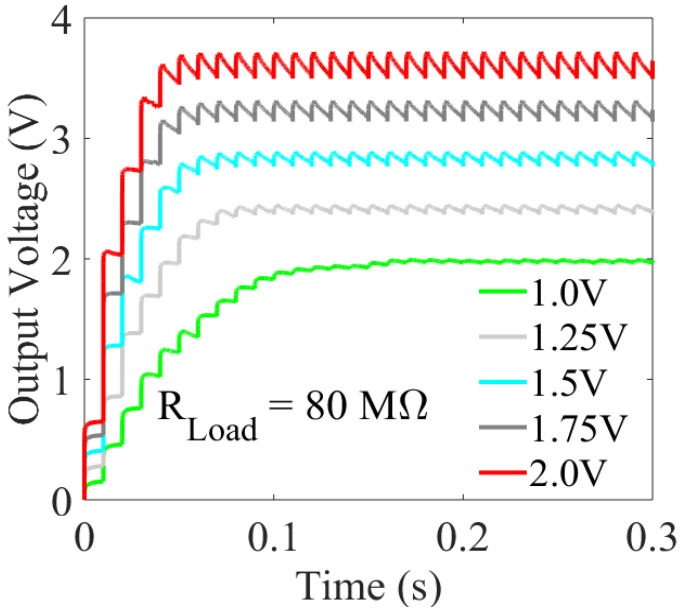


Figure 5.10 Transfer characteristics of the output voltage of the *CCVD* design for five different values of input voltage (V_{in}).

Here it is found that the settling time decreases with increase in input voltage. The observed settling time is 150.4 ms, 72.9 ms, 60.5 *ms*, 50.76 *ms* and 43.4 *ms* for input

voltage of 1 *V*, 1.25 *V*, 1.5 *V*, 1.75 *V* and 2 *V*, respectively. Moreover, the maximum unloaded output voltage of the proposed design is 3.89 *V*, which is 97.25 % of the ideal output voltage (i.e. 4*V*). Furthermore, Figure 5.11 shows the characteristics of output voltage of the proposed *CCVD* design with respect to time for the fixed value of R_L along with non overlapping clock signals. It shows that the process of input voltage modulated with clock signals and capacitors used to double the input voltage after a minimum clock pulse count.

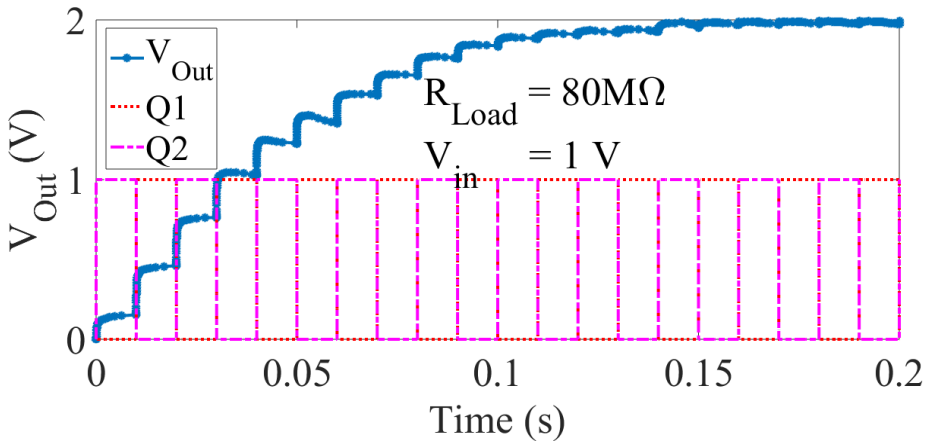


Figure 5.11 Transient response of the *CCVD* for the fixed value of load resistance R_L with non-overlapping control scheme

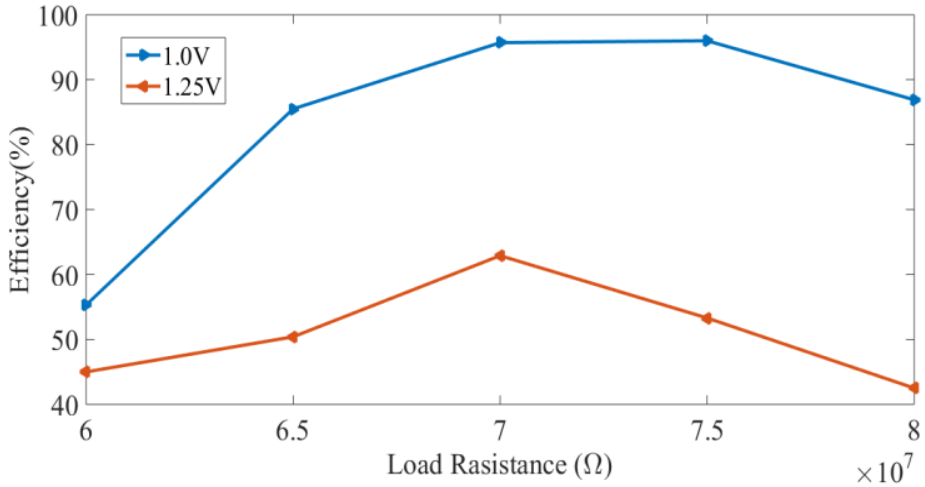


Figure 5.12 shows the efficiency of the proposed design for varying R_L under different values of drain voltage.

Further in Figure 5.12, the efficiency of the proposed design under different R_L is demonstrated for various values of drain voltage. Here, the design is dedicated to low power applications, the load sweeps from 60 *MΩ* to 80 *MΩ*. The examined design performs better than other available designs when the R_L is approximately 75 *MΩ*. In

this regard, comparative transfer characteristics of output voltage with respect to V_{in} is analyzed for the proposed design based on TFET and MOSFET as shown in Figure 5.13.

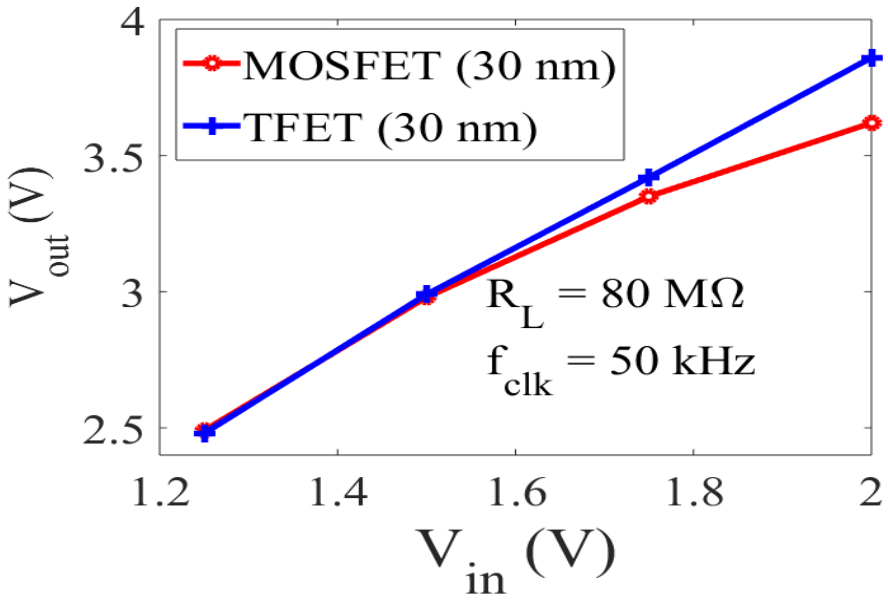


Figure 5.13 shows the comparison of transfer characteristics of output voltages for the proposed design based on TFET and MOSFET.

5.6 Load Parameters of the Proposed Design

It is observed in Figure 5.14 about the maximum output voltage, which has been achieved by the proposed design for different R_L such as 60 *MΩ*, 70 *MΩ* and 80 *MΩ*.

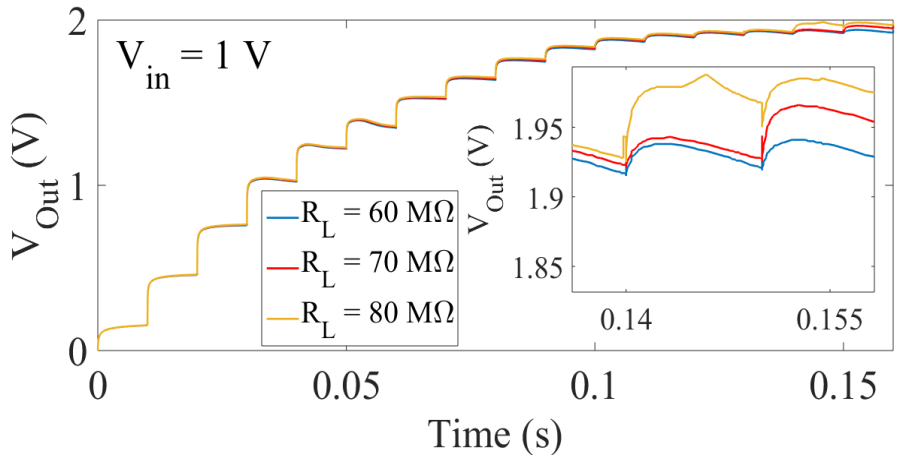


Figure 5.14 Output voltage characteristics of the proposed design for different values of R_L= 60, 70, 80 *MΩ*, the inset shows the detail variation of output voltage for different R_L in the given time slot

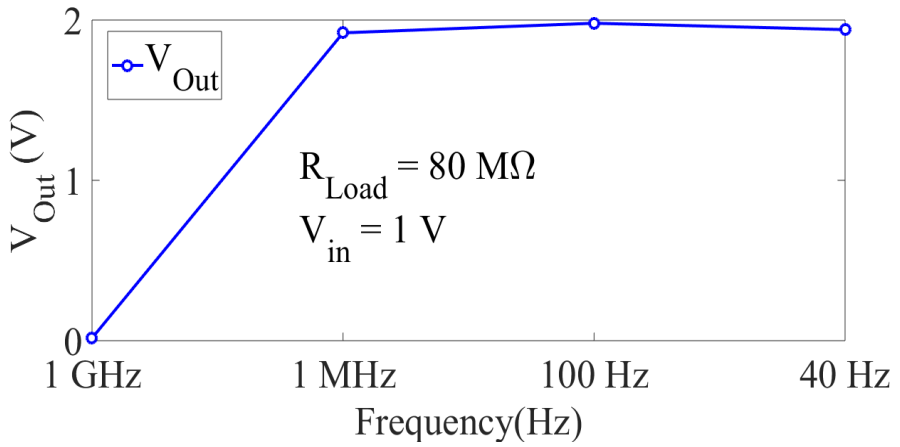


Figure 5.15 The output voltage of the proposed design under different frequency range (i.e. 40 Hz to 1 GHz) while keeping fixed value of R_L.

Table 5.2 Circuit parameter comparison of various voltage doubler circuits

Specifications	[71]	[66]	[105]	[106]	[70]	**This work**
CMOS process (nm)	45	350	1200	45	130	30
Switching Frequency (MHz)	10	10	NA	60	50	100
Maximum power efficiency (%)	57	60	69.3	NA	88.1	95.4
Flying capacitors (pF)	48	30x4	12	2100	210	10
Output capacitors (pF)	24	60	NA	500	200	1000
Maximum voltage conversion ratio	NA	NA	3.75	2.94	1.99	1
Area (mm^2)	0.03	0.49	0.7	NA	0.37	0.09

Furthermore, the effects of frequency variation (i.e. 1 *GHz* to 40 *Hz*) on the proposed design are investigated and it is observed that on decreasing the frequency up to 1 *MHz*, the output voltage decreases and then it remains constant till frequency of 40 Hz as shown in Figure 5.15. On the basis of results, we can observe that the examined design is well suited for the frequency ranges from 40 *Hz* to 1 *MHz*.

Similarly, Figure 5.16 shows the Power efficiency of the proposed design under different input voltage. Here, it has been also observed that the power efficiency increases continuously with increase in input voltage from 0 to 1.8 *V* for the fixed value of R_L and then slightly decreases. In addition, the proposed design shows the significant improvement in power efficiency compared to previous designs due to implementation of the low sub threshold leakage device with negligible reversion leakage loss as shown in Table 5.2. The maximum power efficiency of the proposed design under a load ranging from 70 *MΩ* to 75 *MΩ* is 95.4%, while the maximum

power efficiency of the designs are 88.16%, 57%, 69.3%, 74.45% and 60% in [70], [71], [105–107], respectively.

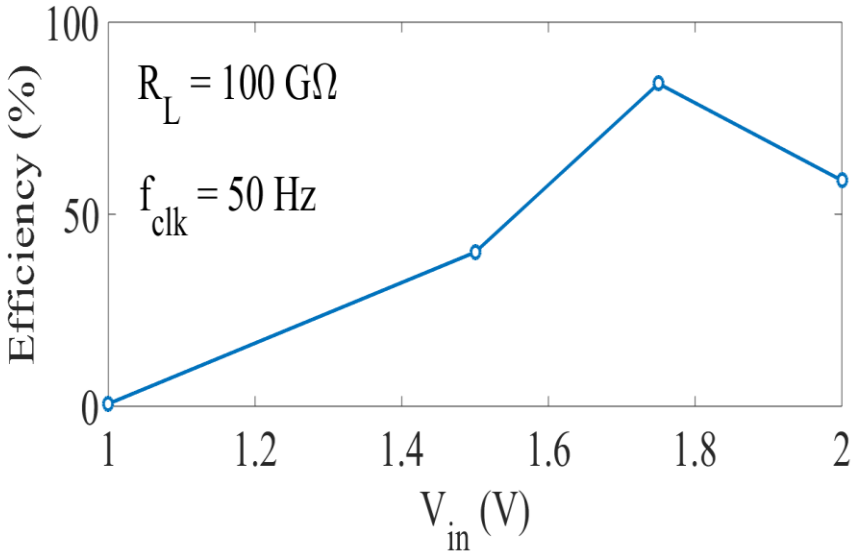


Figure 5.16 Efficiency of the proposed design with varying input voltage under the fixed value of R_L = 100 *GΩ*.

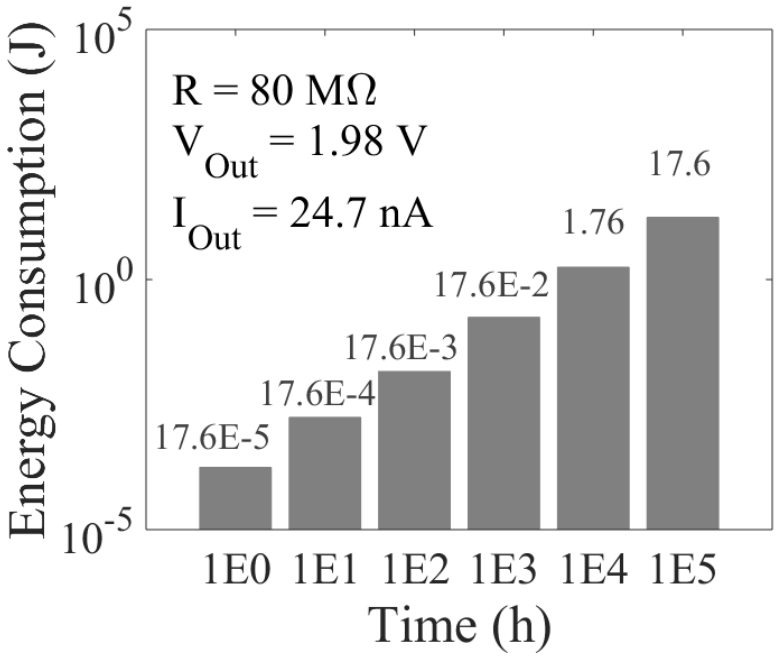


Figure 5.17 Energy consumption of the proposed design for the different time cycles

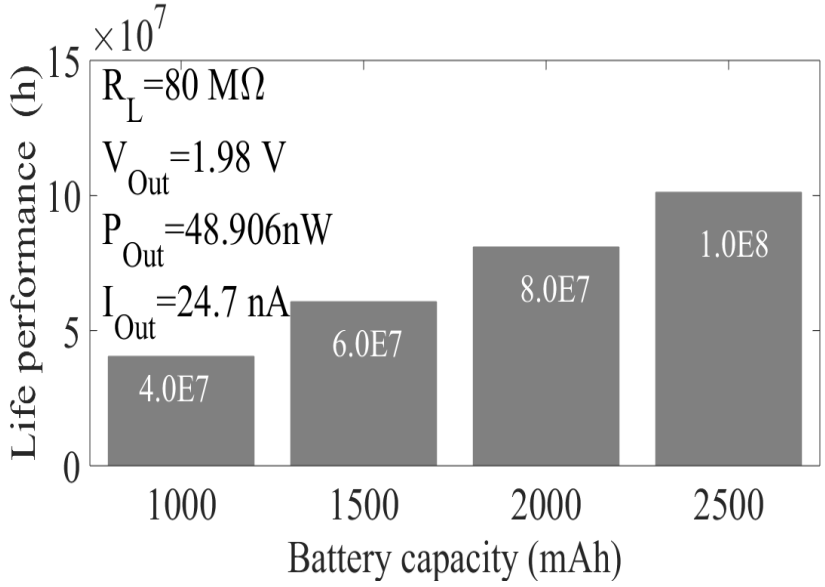


Figure 5.18 Life time performances of the proposed *CCVD* design under different battery capacity (*mAh*).

Recently the voltage doublers are proposed to deploy at remote locations for *IoT* era. Therefore, it would be analyzed at minimum power for maximum applied load of 100 *GΩ* at the output. Besides, the energy consumed by the proposed circuit for 80 *MΩ* load is shown in Figure 5.17. The output current of the proposed circuit is very low for the output voltage at 1.98 *V* and thus, it consumes very less energy. The energy consumption also increases with increase in time period. The proposed circuit mostly powered by battery or *RF* generated supply voltages and therefore total energy consumption will decide the life cycle of the doubler at remote location. Therefore, the total life time performance for different battery capacity is extracted systematically, which can be observed in Figure 5.18. Results reveal that the proposed circuit required small battery consumption of 2500 *mAh* for a life period of 11.5 years. The total life performance increases exponentially with varying small change in battery capacity. Thus, it can be concluded that the *CCVD* based on Cylindrical GAA-Tunnel FET used less energy as compared to *CCVD* based on conventional MOSFET, due to its low sub-threshold leakage current and implementation of non-overlapping clock schemes at low drain voltage of 0.35 *V*. The voltage doubler design for *IoT* applications would be more beneficial for the system deploy at remote locations. Hence, low power consumption and energy utilization of the proposed design are the two important parameters for any circuit assessment, which can be analyzed in the proposed work for *IoT* applications.

5.7 Summary

In this work, an energy efficient *CCVD* based on asymmetrical underlap (*AU*) Cyl GAA-TFET with improved reliability has been investigated systematically in terms of device circuit Co-design performance for *IoT* perspective. The presented design nullify the reversion leakage current and improves high driving capability using two non-overlapping clock signals on the transistors based on BTBT mechanism with optimized device physics. In short, it would be concluded that the proposed design based on low power is energy efficient, cost effective, and simple in fabrication. In addition, the energy consumption of the proposed design is 17.6 J for a continuous life performance of 11.5 years. The comparison reports and results also indicate that the maximum power efficiency of the proposed design is 95.4%. Here, without the need of any extra power FETs, buffers or extra capacitors, it produces low leakage current, high driving current and life performances when compared to the latest report.

CHAPTER 6

Conclusions and Future Works

6.1 Conclusions

In this thesis, we have investigated the Cylindrical GAA-n channel Tunnel FET for improved DC and analog/*RF* characteristics without increase in leakage current using underlap, band-gap and spacer engineering. Further, the proposed device has implemented on circuit applications such as TFET Inverter and *CCVD* design for low power *IoT* sensor node.

Initially, we have presented the comparative investigations of impact of underlap and spacer engineering on the three structures of a 3D Cylindrical GAA-n channel Tunnel FET based on *Si/Ge*-source for improved DC characteristics such as ON State Current *(I_{ON})*, OFF State Current (I_{OFF}), I_{ON}/I_{OFF}, and Subthreshold Swing *(SS)* without a decrease in I_{OFF}. We demonstrate that the considered device with low spacer width and asymmetrical underlap can attain improved DC as well as analog characteristics for low power applications. Further, it has been found that structure of drain underlap with low spacer width achieved 57 times improvement in the I_{ON} and 25 times suppression of ambipolar current characteristics when compared with *SU*-GAA-FSW-TFET.

Furthermore, we have analyzed for high merits of analog/*RF* behavior on the proposed device based *Si/Ge*-source using hetero-spacer and distinct device geometry. It is found that the combination of drain underlap with low-k spacer placed over Ge-source region reduces the fringing field and produces the superior analog/RF performances. It has been found that I_{ON} and I_{ON}/I_{OFF} for GAA-TFET based on a hetero-spacer dielectric are 6 and 73 times high when compared with the device based on homo-spacer dielectric. This thesis also presented the behavior of *RF* figure of merit of the proposed device, where the issue of low driving current and analog/*RF* performances have been resolved by employed Ge-source in the considered device. Here Miller capacitance (C_{gd}) is minimized with high BTBT rate. It is worth noting that with this approach the improvement in analog/*RF* and steepest ambipolar behavior can be achieved without a decrease in I_{OFF}.

Despite the improved DC and analog/*RF* performances, the reliability of the examined device is also investigated while employed the impact of trap assisted tunneling on the DC and analog performances of the 3D Cyl GAA-TFET.

Furthermore, an energy efficient Cyl GAA-Tunnel FET based *CCVD* for *IoT* perspective has been investigated in terms of the Output voltage, Power efficiency, Energy consumption, and life performances using device circuit co-design approach. The presented design nullify the reversion leakage current and improves high driving capability using two non-overlapping clock signals with tunnel transistors based on optimized device physics.

6.2 Future Works

In future, the proposed design of cross Coupled voltage Doubler would be beneficial in a two stage implementation for low power module of system on chip (*SoC*) applications due to low power consumption and small area at the same time. Further, the developed Verilog A model of the examined device of Cyl GAA Tunnel FET would be implemented to design memory circuits such as static random access memory (*SRAM*) cell using HSPICE simulations. The investigation of digital parameters of the SRAM architecture would be performing using EDA and TCAD tool. The digital parameters of the proposed cell would be evaluated in terms of leakage power, read static noise margin (*RSNM)*, write static noise margin (*WSNM*), read–write energy, delay time, and power efficiency, respectively. Furthermore, the reliability analysis of the memory design based on the proposed device will be analyzing using the effects. In this concern, effects of Negative bias temperature instability *(NBTI*) and Positive bias temperature instability (*PBTI*) on the memory circuit can be analyze using small signal model [3-4]. The small signal model comprises the modeling of the proposed device including NBTI and PBTI concern.

Further, study of phonon and charge trap assisted tunneling (*TAT*) on the proposed device can be perform in details, while included TAT physical model using 3D TCAD Simulations. Besides, the comprehensive investigations made for the examined device of Cyl GAA TFET using numerical simulation, would be beneficial for a new generation of *RF* circuits and systems in a broad range of frequencies covering *RF* spectrum. In addition, the results will be useful to other works for the development of robust compact models for analog/*RF* parameters. In a developing field, where

experimental results are still limited, the available simulation data of the work can be helpful for further applications required for the progress of future Tunnel FET in terms of fabrication and model development. In addition, The developed device can be utilized as fast switching device due to low operating power (< 0.5 *V*), for multi-circuit applications and the developed emerging device in a nano-regime can be utilize for experimental results under fabrication for industries like IBM, INTEL, TSMC.

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