PERFORMANCE ENHANCEMENT OF CMOS DIGITAL CIRCUITS USING STRAIN ENGINEERED ASYMMETRIC DUAL-*k* SPACER FINFETs

Ph.D. Thesis

By

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DISCIPLINE OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE

DECEMBER 2018

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A THESIS

Submitted in partial fulfillment of the

requirements for the award of the degree

of

DOCTOR OF PHILOSOPHY

by

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DISCIPLINE OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled "**PERFORMANCE ENHANCEMENT OF CMOS DIGITAL CIRCUITS USING STRAIN ENGINEERED ASYMMETRIC DUAL-*k* SPACER FINFETs**" in the partial fulfillment of the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY** and submitted in the **DISCIPLINE OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from July 2014 to December 2018 under the supervision of Dr. Santosh Kumar Vishvakarma, Associate Professor, Indian Institute of Technology Indore, Indore, India.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

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(MAISAGALLA GOPAL)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Signature of Thesis Supervisor with date
(Dr. SANTOSH KUMAR VISHVAKARMA)

MAISAGALLA GOPAL has successfully given his Ph.D. Oral Examination held on 1^{st} May 2019.

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Date:

Acknowledgements

First and foremost, I am grateful to the God Almighty for letting me through all the difficulties and I keep on trusting you for my entire life and I thank for this great opportunity to pursue Ph.D. from the institution like IIT Indore. It is my proud privilege to express deep sense of gratitude towards my supervisor Dr. Santosh Kumar Vishvakarma for his immense support, keen interest, encouragement and valuable guidance during the entire Ph.D. I am extremely thankful to my guide, for the encouragement, insightful suggestions and valuable comments, which helped me in exploring my research work. The completion of this undertaking could not have been possible without the assistance of my supervisor.

I acknowledge with thanks for the kind of patronage, loving inspiration, valuable comments and suggestions to my PSPC committee members Dr. Vipul Singh and Dr. Anirban Sengupta during my research and my special thanks to Prof. Pradeep Mathur, Director IIT Indore, who has been highly supporting during the entire course of my doctoral work. I express my appreciation and indebtedness to my colleagues Mr. Ambika Prasad Shah, Mr. Vishal Sharma, Mr. Mahesh Kumawat, Mr. Ankur Beohar, Mr. Abhishek Upadhyay, Mr. Gaurav Singh, Mr. Ravi Kumar, Ms. Pooja Bohara, Mr. Sajid Khan, Mr. Gopal R Raut, Ms. Neha Gupta and Ms Gunjan Singh Rajpoot. Also, I would like to thank my seniors Dr. Deepika Gupta, Dr. Nand Kishore Yadav, Dr. Vikas Vijayvargiya, Dr. Pooran Singh, Dr. Bhupendra Singh Reniwal, Dr. Chandrabhan Kushwah, who helped me in several ways during my thesis work, their contributions are sincerely appreciated and gratefully acknowledged. I record cordial appreciation to my parents and family members for constant attention, affectionate patronage and highly inspiring attitude, which had made it possible to bring the work in its present form and to achieve one of the greatest milestones in my life.

MAISAGALLA GOPAL

Dedicated

to

My Parents

Abstract

In scaled technologies multi-gate MOSFETs are become the promising candidates to replace the bulk MOSFET due to their reduced Short Channel Effects (SCEs) and higher current driving capabilities. Among all the multi-gate MOSFETs, quasi planar double gate (FinFET) device architecture has attracted much attention of today's VLSI industry because of it's fabrication simplicity and scalability. We propose silicongermanium (SiGe)/Si carbide (SiC) source/drain (S/D) asymmetric dual-k spacer underlap Fin-Field-Effect Transistor (SiGe/SiC-AsymD-k FinFET) with Si channel. Strain-induced mobility enhancement due to the $Si_{1-x}Ge_x/Si_{1-y}C_y$ S/D leads to a significant drive current enhancement of the proposed device. The introduced dual-k at source side helps to achieve unequal magnitudes in current driving capabilities based on the applied positive and negative drain bias. In this thesis, we particularly focused on 6T SRAM cell to mitigate the read-write conflict. We show that using this unique technology feature of the proposed device, the read-write conflict can be mitigated in 6T SRAM cell and achieve higher cell stability. Simulation results show that SiGe/SiC-AsymD-k FinFETs based SRAM offers 14.28% and 18.06% improvement in read and write mode respectively over conventional FinFET based 6T SRAM bit cell. When compared to conventional FinFET 6T SRAM bit cell, the proposed 6T SRAM bit cell shows lesser temperature sensitivity of cell stability. We report the reliability aspects of the proposed deice. We also explore the SiGe channel based AsymD-k FinFET for high performance and robust SRAM cell. The amalgamation of channel mobility enhancement and asymmetric dual-k, offers high current drive capabilities while preserving lower short channel effects. This results in improvement of Static Noise Margin (SNM) of all possible modes of SRAM. Compared to conventional FinFET SRAM, SiGe based AsymD-k FinFET SRAM exhibits 9.16% enhancement in hold SNM, 18.22% in read and 5.96% in write SNM. Furthermore, the read and write access times reduced by 48.6% and 32.4% respectively.

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List of Abbreviations

2D	:	Two Dimensional
3D	:	Three Dimensional
BL	:	Bit Line
ADSE	:	Asymmetric Drain Spacer Extension
BLB	:	Bit Line Bar
BOX	:	Buried Oxide
DG	:	Double Gate
DIBL	:	Drain Induced Barrier Lowering
DSL	:	Dopant Segregation Length
FDSOI	:	Fully Depleted Silicon On Insulator
FinFET	:	Fin Field Effect Transistor
GFIBL	:	Gate Fringe Induced Barrier Lowering
GUI	:	Graphical User Interface
HCI	:	Hot Carrier Injection
HP	:	High Performance
IC	:	Integrated Circuit
ITRS	:	International Technology Road map for Semiconductors
MOSFET	:	Metal-Oxide-Semiconductor Field Effect Transistor
NM	:	Noise Margin
PBTI	:	Positive Bias Temperature Instability
PC	:	Personal Computer
PDA	:	Personal Digital Assistant
PDSOI	:	Partially Depleted Silicon On Insulator
RCS	:	Remote Coulomb Scattering
RPS	:	Remote Phonon Scattering

RSNM	:	Read Static Noise Margin
S/D	:	Source/Drain
SCE	:	Short Channel Effect
SSE	:	Sentaurus Structure Editor
SiC	:	Silicon Carbide
SiGe	:	Silicon Germanium
SOI	:	Silicon On Insulator
SRAM	:	Static Random Access Memory
SRH	:	Shockley Read Hall
SNM	:	Static Noise Margin
SS	:	Subthreshold Swing
TCAD	:	Technology Computer Aided Design
UTB	:	Ultra Thin Body
UTBB	:	Ultra Thin Body and BOX
VTC	:	Voltage Transfer Characteristics
WL	:	Word Line
WSNM	:	Write Static Noise Margin

List of Symbols

G_m	:	Transconductance
N_A	:	Channel doping
C_{fr}	:	Fringe capacitance
C_{GC}	:	Gate-to-channel capacitance
C_{GD}	:	Gate-to-drain capacitance
C_{GG}	:	Gate-to-gate capacitance
C_{GS}	:	Gate-to-source capacitance
N_{DOSS}	:	Source doping
N_{DOSD}	:	Drain doping
I_D	:	Drain current
I_{OFF}	:	OFF-current
I_{ON}	:	ON-current
k	:	permittivity
L_{ext}	:	Extension length
L_g	:	Physical gate length
L_{hk}	:	Length of high-k spacer material
L_{lk}	:	Length of low-k spacer material
L_{un}	:	Underlap length
$R_{S/D}$	:	Source/Drain series resistance
t_{ox}	:	Physical oxide thickness
t_{si}	:	Body thickness
V_{DD}	:	Supply voltage
V_{GS}	:	Gate-to-source voltage

V_{DS}	:	Drain-to-source voltage
V_Q	:	Node volage at Q
V_{QB}	:	Node volage at QB
V_{th}	:	Threshold voltage
ΔV_{th}	:	Shift in threshold voltage
τ_{LH}	:	Low-to-high delay time
τ_{HL}	:	High-to-low delay time

Chapter 1

Introduction

In recent years, electronic gadgets such as hand held mobile devices, Personal Digital Assistants (PDAs) and battery operated tablets, Personal Computers (PCs) are become the centre of our daily lives. Since mid of twentieth century, the development in electronic industry growing rapidly, to satisfy the growing demands of today's electronic industry, various functionalities has to be fabricated on a single semiconductor wafer, generally known as chip or Integrated Circuits (ICs). The main building block of IC is Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). These are the indispensable part in electronic devices to build high-density ICs such as semiconductor memories and microprocessors.

1.1 History of Transistor and Moore's Law

The principles of field-effect-transistor was proposed and patented by Austrian-Hungarian physicist Julius Edgar Lilienfeld in 1926 [2] and by Oscar Heil in 1934 [3]. William Shockley, John Bardeen and Walter Brattain invented the germanium based point contact transistor at bell laboratories on December 16, 1947 [4]. The first integrated circuit *aka* the microchip was invented by Robert Noyce [5], co-founder of Fairchild and Jack Kilby [6], electrical engineer of Texas Instruments during 1958 to 1959. The first MOSFET was invented by Kahng [7] and Atalla [8] in 1960 at bell laboratories, which brings the revolution in electronics industry. In 1965, Gordon E. Moore, co-founder of the Intel Corporation predicted that the number of transistors in a chip will become double for every 18 months [9], called

Moore's law. The Moore's law still followed by current semiconductor industries to improve the packaging density in order to fulfill the growing demands of present electronic market.

1.2 Issues in Bulk MOSFET at Nanoscale Regime

As MOSFET gate length (L_g) continue to shrink year after year, drain starts to compete with the gate terminal to control the channel potential that results in Short Channel Effects (SCEs) as shown in Figure 1.1, which are undesirable and degrades the device performance.

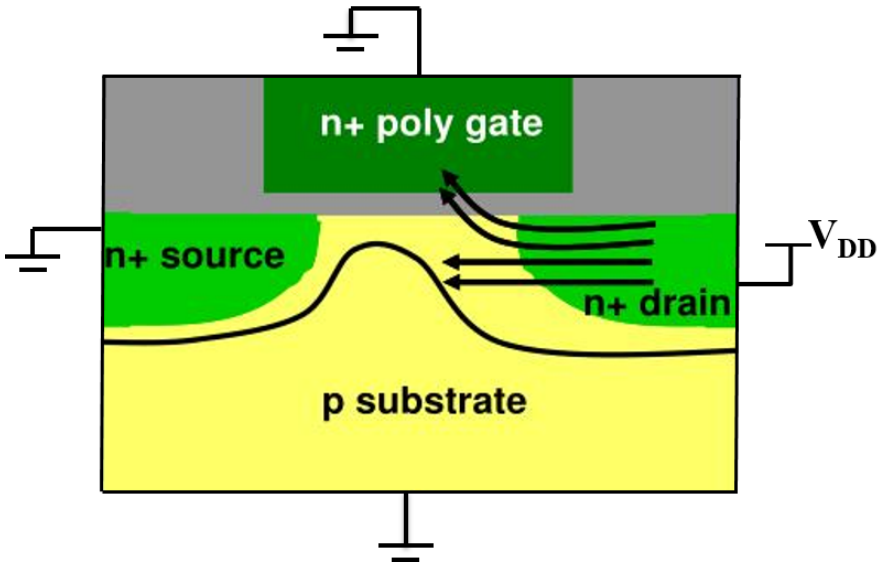


Figure 1.1: Mechanism of short channel effects in bulk MOSFET.

The following are the some of the short channel effects:

(a) Drain-Induced Barrier Lowering (DIBL) : In short channel MOSFETs, the gate-to-source voltage (V_{GS}) and the drain-to-source voltage (V_{DS}) are the responsible to control the potential barrier. If V_{DS} is increased, drain electric field affects the channel region without influence of the gate voltage that results in decrease in potential barrier in channel region as shown in Figure 1.2, leading to Drain-Induced-Barrier-Lowering (DIBL) [10]. Infact, the gate voltage has to lower the potential barrier in the channel region.

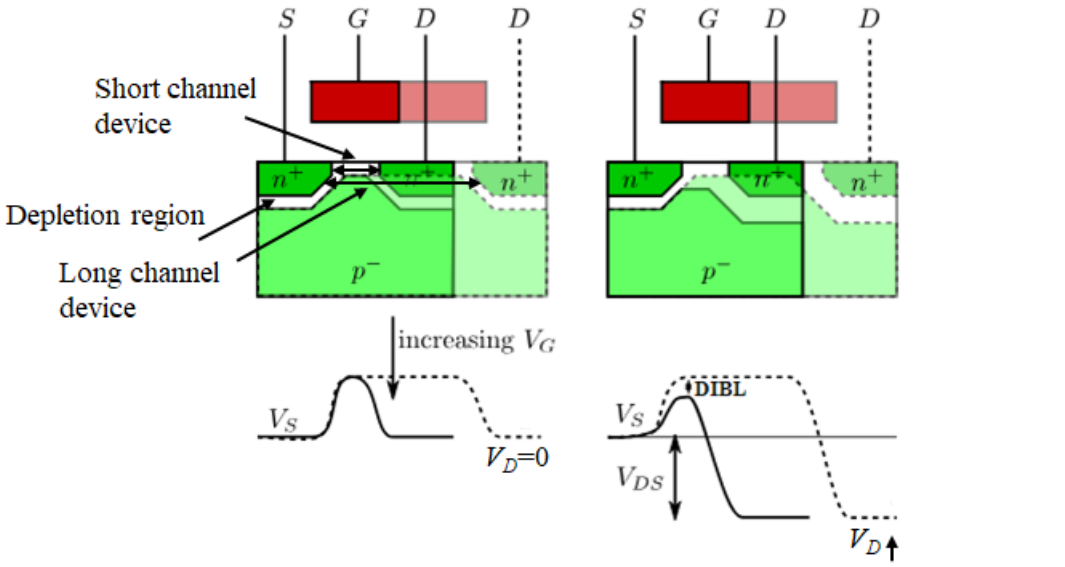


Figure 1.2: Demonstration of DIBL effect in short channel MOSFET.

(b) Surface Scattering : When the charge carriers (holes or electrons) travel along the channel, the applied gate voltage establishes the electric field that attracts the charge carriers towards the surface, as a result they move in zig-zag path as shown in Figure 1.3.This effectively reduces the mobility of the charge carriers than the bulk carriers [11].

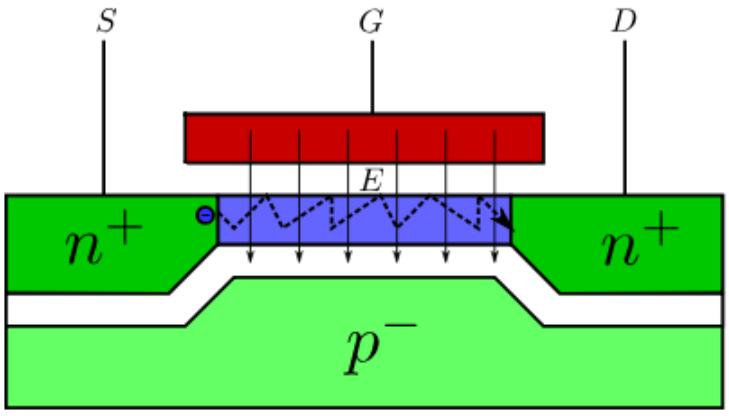


Figure 1.3: Carrier surface scattering effect in short channel MOSFET.

(c) Velocity Saturation : In short channel MOSFETs, the velocity of the charge carriers is proportional to the electric field that drives them. When strong electric fields prevail, the electron velocity is no longer proportional to the field, and can thus no longer be described by a field-independent mobility. However, in a short

channel, due to excessive collisions suffered by the carriers, their velocity saturates after a critical electric field. Since current is the rate of flow of electrons, it also attains a saturated value once the velocity saturates. [12]-[14].

(d) Impact Ionization : As shown in Figure 1.4, in short channel MOSFET, the distance between source and drain is very small and it has strong electric field that causes the charge carriers with high velocity and therefore high energy to cause troubles are called hot carriers.

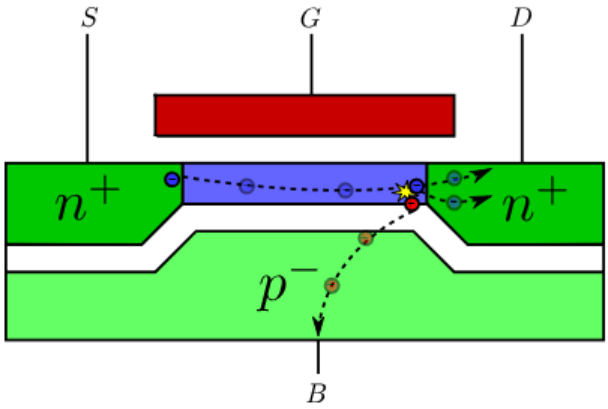


Figure 1.4: Impact ionization in short channel MOSFET.

When these charge carriers are travelling through a silicon lattice, there may be possibility of collision with an atom of the structure. As a result electron-hole pair will be generated [15]. The hole is attracted to the bulk while the generated electron moves near to drain.

(e) Hot Carrier Injection (HCI) : As device dimensions are reduced, electric

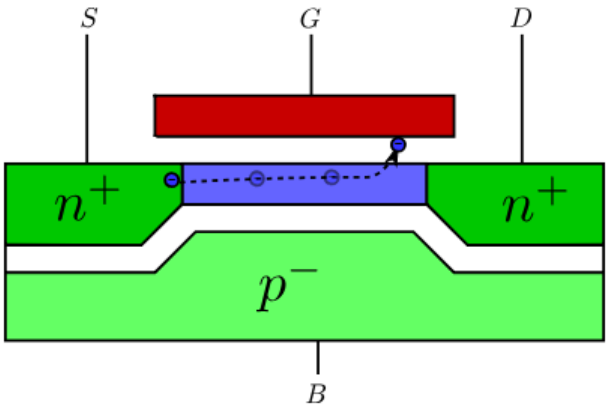


Figure 1.5: Hot carrier mechanism in short channel MOSFET.

fields tend to increase that results in hot carrier acceleration. These hot carriers has the sufficient energy to enter into oxide layer and get trapped in it which is demonstrated in Figure 1.5. The increased trapped charges in the oxide layer increases the threshold voltage of the device [16][17].

Scaling of CMOS device causes the interaction between devices which results in unwanted parasitics effects such as:

- Increased capacitance between the substrate and diffused source/drain [18].
- **Latch-up:** The inadvertent creation of low-impedance path that exists between the power supply rails and ground. It leads to severe problems in CMOS structures and circuit failures due to uncontrolled high currents [19].

To overcome the above mentioned increased parasitic effects, and to improve the subthreshold characteristics, a new device architecture has been investigated which is known as Silicon-On-Insulator(SOI) technology [20].

1.3 Silicon-On-Insulator (SOI) Technology

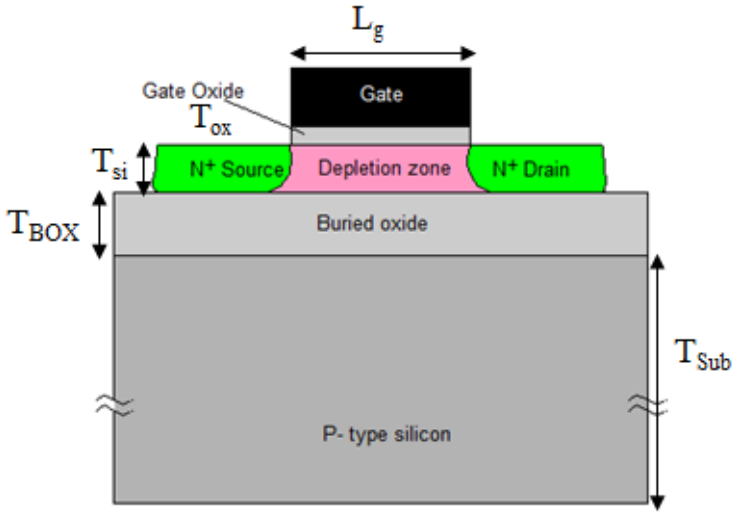


Figure 1.6: Structure of SOI MOSFET.

The structure of SOI devices are similar to bulk CMOS except the Buried Oxide (BOX) which is placed under the silicon layer as shown in Figure 1.6. This buried oxide insulation layer separates the conducting channel from the substrate; as a

result SOI device exhibits low capacitance and reduced the current leakage from drain/source junction to substrate [21]. This renders the SOI MOSFET an outstanding silicon device applicable for high-speed and low-power applications. With compared to bulk MOSFETs, SOI MOSFETs are more reliable to transient radiation effects. Based on the magnitude of the depletion layer, SOI MOSFETs can be categorised as [22]:

(i) Partially Depleted Silicon-On-Insulator (PDSOI) MOSFET

(ii) Fully Depleted Silicon-On-Insulator (FDSOI) MOSFET

In PDSOI MOSFET, the silicon layer thickness is larger than the depletion regions formed at the back and front oxide-semiconductor interfaces as shown in Figure 1.7. As the silicon layer is larger than the depletion region, there exists a neutral part of silicon layer called body. if the body is grounded, it reflects the bulk

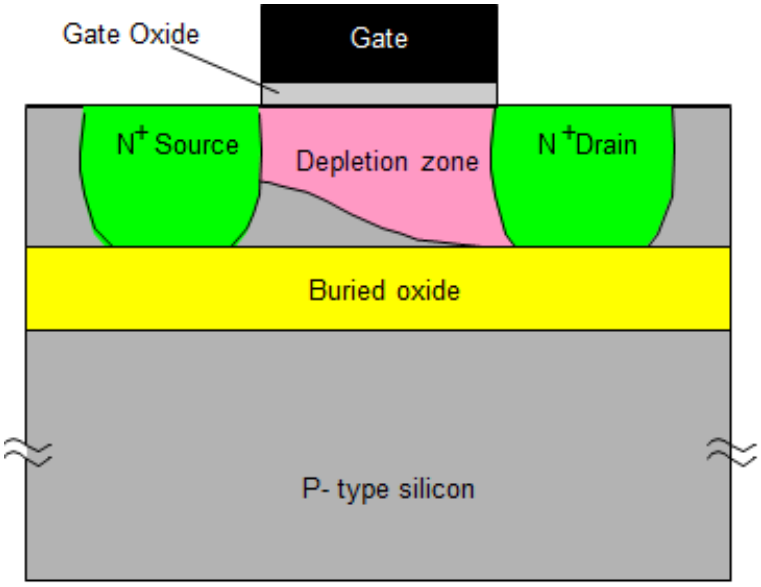
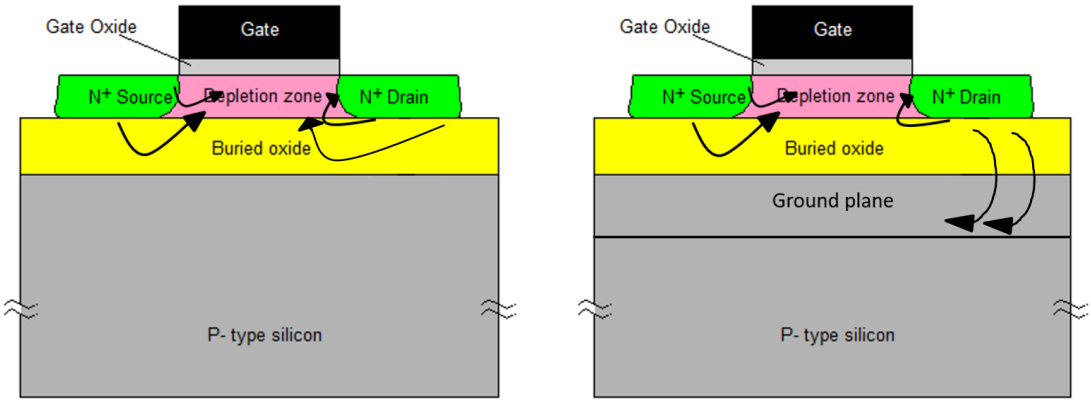


Figure 1.7: Schematic of PDSOI MOSFET .

MOSFET characteristics. But, if the body is left electrically floating, it suffers from parasitic effects, such as kink effect or floating body effect [23][24]. This is due to majority carriers accumulation in body and it raises the body potential.

FDSOI MOSFET has a thinner top silicon layer as shown in Figure 1.6 and it is entirely depleted of majority carriers. The gate voltage does not affect the depletion layer. These type of devices has a strong coupling between the two oxide-semiconductor inter faces that leads to improved drain current. It is very sensitive to silicon thickness variations than PDSOI MOSFET. FDSOI MOSFET offers several

advantages over PDSOI MOSFETs such as: no kink effect, improved SCEs, higher saturation current, better Subthreshold Swing (SS), better radiation tolerance and low parasitic capacitances [25]. Although FDSOI MOSFET has several advantages, as device dimensions are reduced, it suffers from SCEs. To improve the gate control over the channel, the silicon layer thickness is to be reduced, the resultant device architecture is called as Ultra-Thin-Body (UTB) SOI MOSFET shown in Figure 1.8 (a). By reducing the silicon layer thickness, the electric field lines enter through



(a) (b)

Figure 1.8: Device architectures of (a) ultra thin body and (b) ultra thin body and box FD SOI MOSFETs showing encroachment of electric field lines from source and drain on the channel region.

BOX. To reduce the influence of electric field lines on the channel region, BOX layer thickness need to be reduced [26]. The structure with thinned silicon layer and reduced BOX thickness is called as Ultra-Thin-Body and BOX (UTBB) shown in Figure 1.8 (b). In this case most of the electric filed lines from drain and source terminate on the buried ground plane instead of channel region. However, reducing the BOX thickness results in increased junction capacitance and body effect [27]. As technology scaling, the above mentioned are the issues in bulk MOSFETs and SOI MOSFETs, application of these devices in digital circuits result in performance degradation of the circuits. To overcome these drawbacks and to continue the Moore's law, advanced CMOS device architectures has been investigated.

1.4 Multiple Gate MOSFET Technology

1.4.1 Double Gate (DG) MOSFET

The concept of DG MOSFET structure was first proposed by Sekigawa and Hayashi in 1984 [28]. It composed of two gates (bottom gate and front gate) that are connected together. Two gates are collectively control the channel potential as a result DG MOSFET exhibits superior SCEs. If we observe the encroachment of electric field lines from source and drain, they terminate on the bottom gate and cannot reach the channel region as shown in Figure 1.9. Because of its advantages, DG MOSFETs are the promising candidate to replace bulk MOSFETs at nano scale regime [29]. As double gate MOSFET structure demands for gate-channel-gate stack formation, it leads to fabrication difficulty. But among all DG MOSFETs quasi planar Fin-Field Effect Transistor (FinFET) has attracted much attention of today's semiconductor industry because of it's fabrication simplicity and scalability.

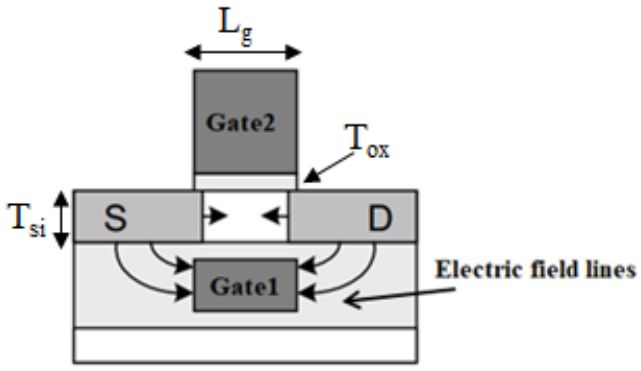


Figure 1.9: Structure of Double-gate MOSFET.

1.4.2 FinFET: A Self-Aligned Double-Gate MOSFET

The FinFET is a double gate structure in which conducting channel is formed in vertical *Si* fin and it is controlled by a self-aligned double gates. These self-aligned gates control the channel potential to reduce the SCEs [30][31] and conduction current direction is parallel to the wafer surface. The 3D structure of FinFET is shown in Figure 1.10. A thin *Si* fin which acts as body of MOSFET is the heart of FinFET. A heavily doped polysilicon film wraps around the fin and makes electrical

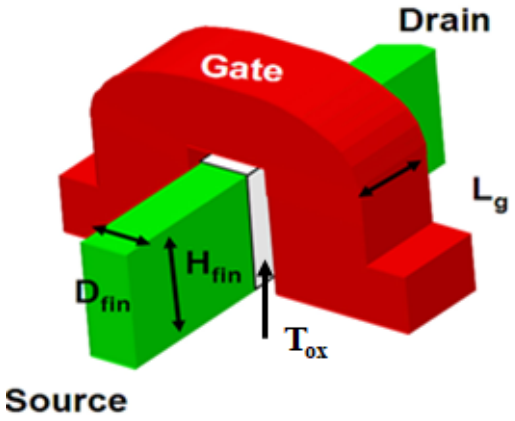


Figure 1.10: 3D-view of FinFET [30].

contact to the vertical faces of the fin, known as self-aligned gate. This heavily doped polysilicon helps to reduce the channel resistance. Generally, in FinFET the channel width is sum of twice the fin height and fin width. FinFET has several advantages over bulk MOSFET such as fabrication simplicity, reduced SCEs and scalability than any other DG MOSFETs [30].

1.5 Conventional 6T Static Random Access Memory (SRAM) Cell

SRAM is a most common embedded memory and it uses "Bi-stable Latching circuitry" to store a bit of information. It consists of a latch therefore the cell data remains as it is as long as power is turned on (volatile type memory) and refresh operation is not required. Each bit is stored on four transistors that form two cross coupled inverters. The demand for SRAM is increasing with large use of SRAM in System-On-Chip (SOC) and high performance VLSI circuits. Figure shows the schematic of conventional 6T SRAM cell.

Conventional 6T SRAM cell composed of two cross coupled inverters (M1, M2, M3 & M4) and two access transistors (M5 & M6). Gate terminals of the access transistors are connected to the Word Lines (WL), which is used to select the cell. Source/Drain terminals are connected to the Bit Line (BL) and Bit Line Bar (BLB), which are used to perform the read and write operations on the cell. Internally, the cell holds the stored value on one side and its complement on the other side.

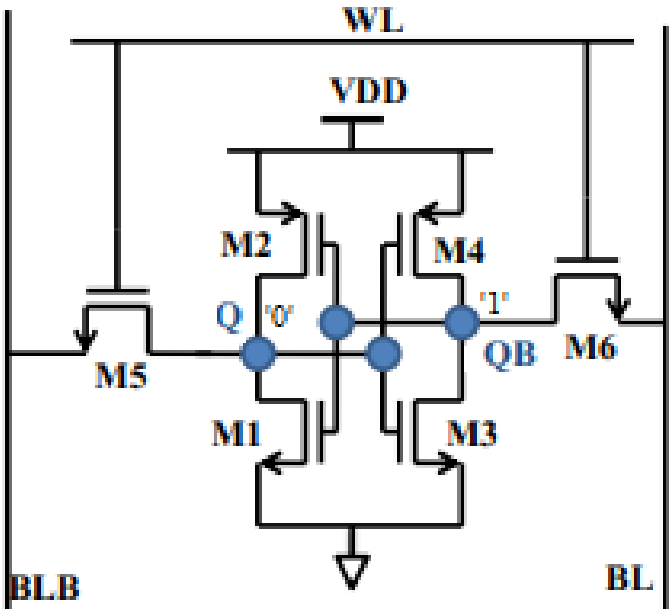


Figure 1.11: Schematic of conventional 6T SRAM cell.

1.5.1 Read Operation

The row decoder and column decoder decode the address of the SRAM cell from where data has to read. Without loss of any generality, assume that at node Q, '0' is stored and at node QB '1' is stored. Therefore, M1 is on and M3 is off. Before the read operation BL & BLB are precharged to V_{DD}. When the WL goes high, current begins to flow through M5 and M1 to ground. The resulting cell current slowly discharges the corresponding bit line capacitance. Meanwhile, on the other side of the cell, the voltage on the BLB remains high since there is no path to ground through M3. The difference between BL and BLB is fed to sense amplifier to generate a valid output, which is then stored in a data buffer. Upon completion of the read cycle, the word line is returned to zero and the column lines can be pre charged back to a high value.

The problem associated with bulk MOSFET based 6T SRAM cell during read operation is, on asserting the WL, it raises the voltage at node Q, which could turn ON the M3 transistor, when this happens the voltage at node QB, which stores '1'will be reduced. This voltage may drop little, but it should not drop below the trip point of other inverter. If it drops below the trip point, it leads to read destructive operation which degrades the stability of the 6T SRAM cell.

1.5.2 Write Operation

The data to be written into a cell is provided by the external devices, row decoder and column decoder provide the address of a cell where data has to be written. To write '0' into the cell, BL should be grounded and BLB maintained at V_{DD}. Value '1' can be written into the cell by inverting the values of the bit lines.

1.5.3 Stability of SRAM Cell

Static Noise Margin (SNM) is a standard method to measure the stability of the SRAM cell. It is defined as the maximum DC noise voltage that can be tolerated by SRAM cell without disturbing the stored data. SNM of the SRAM cell can

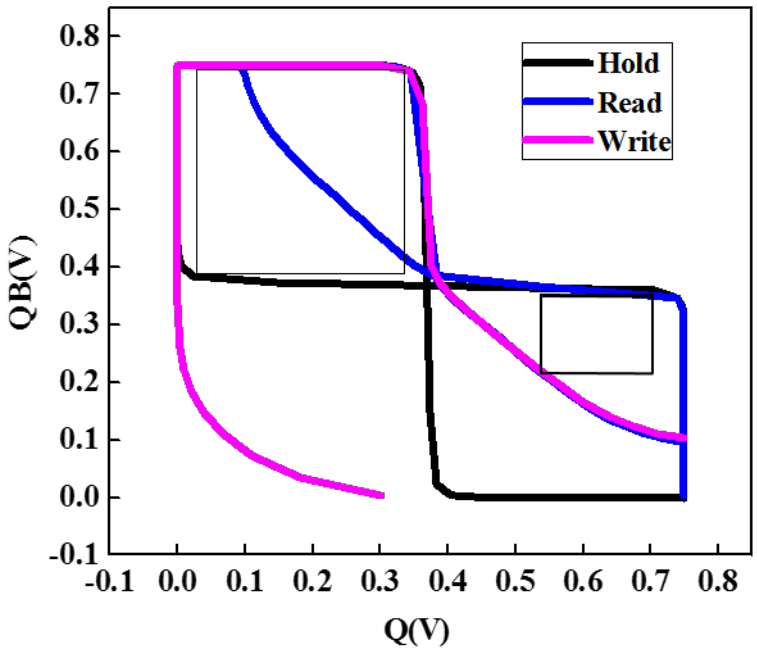


Figure 1.12: Calculation of HSNM, RSNM and WSNM of conventional 6T SRAM cell.

be calculated by drawing the Voltage Transfer Characteristics (VTC) of the cross coupled inverters. The resulting two-lobed graph is called as butterfly curve. The SNM has three key factors associated with the SRAM cell, i.e., Read SNM (RSNM), Hold Static Noise Margin (HSNM) and Write SNM (WSNM). The RSNM/HSNM can be extracted by nesting the largest possible square inside the two VTC of the CMOS inverters [32] as shown in Figure 1.12. The RSNM is defined as the length of

the side of a square, given in volts. The WSNM is measured by plotting the VTC of write '0' operation by sweeping QB from 0 to V_{DD} and VTC of write '1' operation by sweeping QB from V_{DD} to 0. The WSNM is measured as the smallest square plotted into the VTC curve as shown in Figure 1.12.

1.6 Motivation and Objectives

Motivation: The performance of a Static Random Access Memory (SRAM) cell depends on the stability. In order to achieve desired performance characteristics, the relative strengths of the various transistors has to be optimized. the major concern of 6T SRAM cell is read stability, write failures have become also important in deep sub-100nm technologies. In conventional 6T SRAM cell, during the read operation, both the bit-lines (bit line (BL) and bit line bar (BLB)) are precharged to supply voltage (V_{DD}) and word line is asserted to turn on the access transistors (AXL and AXR). On asserting the WL, the voltage at node Q (V_Q) rises. If V_Q is greater than the trip point of other inverter, it leads to read failure. Hence, for higher read stability weak access transistor is desired. During the write operation BL and BLB are maintained at V_{DD} and GND respectively. The voltage at QB (V_{QB}) is discharged on asserting the WL. If V_{QB} is less than the trip point of other inverter, successful write operation achieved. For higher write ability strong access transistor is desired.

This read/write conflict occurs due to the antithetical sizing necessity of access transistors. if the access NFETs are weak, it is difficult to write into the cell. However, access NFETs of 6T SRAM cell cannot be made arbitrarily large since a stronger access NFET will lead to serious read disturbance during the read operation. Thus, there exist conflicting requirements for the strength of the access transistor between read stability and writability. The conflict in access transistor sizing between read and write can be relaxed with the use of asymmetric transistors. Many novel device architectures have been investigated in the past to explore the technology-circuit co-design approach [33]-[34]. Although these devices have the ability to improve the subthreshold characteristics at the cost of poor current driving capabilities.

Here, we made the FinFET asymmetric by placing dual-k (high-k spacer and low-k spacer) spacers at source side and single low-k spacer at drain side, also introduced strain by replacing S/D pads with SiC/SiGe materials. As a result the proposed device exhibits different current driving capabilities for $V_{DS} > 0$ and $V_{DS} < 0$. This asymmetry in the current driving capabilities offer to achieve the improvements in both read and write stability of 6T SRAM cell.

Objectives: The major objectives of this thesis are

Device Level:

- To design a FinFET device that exhibits unequal magnitudes in current driving capabilities.
- To analyze various capacitances associated with SiGe/SiC AsymD-k FinFETs.
- To study the device characteristics of SiGe/SiC AsymD-k FinFETs by varying Ge/C mole fractions.

Circuit Level:

- To reduce read/write conflict in 6T SRAM cell using proposed devices.
- To analyze the performance metrics of SiGe/SiC AsymD-k FinFETs based 6T SRAM cell with supply voltage scaling.

1.7 Organization of Thesis

This thesis aims to investigate the performance of SiGe/SiC AsymD-k FinFETs from device level to circuit level. In particular, we analyzed the performance metrics of 6T SRAM cell and inverter using the proposed devices.

The thesis is organized as follows :

Chapter 1. Introduction : This chapter presents, a brief introduction about multi gate MOSFETs, AsymD-k FinFETs, issues in 6T SRAM cell, motivation, objectives, and main contribution of work carried out in the thesis.

Chapter 2. Effect of Asymmetric Doping on Asymmetric underlap Dual-*k* Spacer FinFET : This chapter extensively analyzes the effect of asymmetric source/drain doping on AsymD-k FinFET. The proposed unequal doping concentration of source and drain leads to superior short-channel characteristics that alleviate the OFF-current (I_{OFF}) of the device. I_{ON}/I_{OFF} evaluated by varying the device parameters about its projected value.

Chapter 3. Impact of Varying Carbon Concentration in SiC S/D Asymmetric Dual-*k* Spacer for High Performance and Reliable FinFET : In this chapter, we propose a reliable asymmetric dual-k spacer with SiC source/drain (S/D) pocket as a stressor for a Si channel. Analyzing the device performance in terms of electron Mobility (eMobility), current driving capabilities, transconductance (G_m) Subthreshold Swing (SS) and reliability.

Chapter 4. Strain Engineering for Performance Enhancement of AsymD-*k* FinFETs for Digital Circuit Applications : This chapter aims to investigate the device performance of silicongermanium (SiGe)/Si carbide (SiC) source/drain (S/D) asymmetric dual-k spacer underlap Fin-Field-Effect Transistor (SiGe/SiC-AsymD-k FinFET) with Si channel for high performance SRAM cell.

Chapter 5. SiGe channel based Asymmetric Dual-*k* Spacer FinFETs-based 6T SRAM Cell to Mitigate Read-Write Conflict : This chapter presents, silicon-germanium (SiGe) channel based asymmetric underlap dual-k spacer Fin-field effect transistor (AsymD-k FinFET) for robust SRAM cell.

Chapter 6. Conclusions and Future Works: In this chapter, all the contributions made in this thesis are summarized, and conclusions and suggestions for future research are provided.

Chapter 2

Effect of Asymmetric Doping on Asymmetric Underlap Dual-k Spacer FinFET

2.1 Introduction

As discussed in chapter 1, scaling of conventional bulk MOSFETs have led to short channel effects (SCEs) in the device due to loss of gate control over the channel. This chapter extensively analyzes the effect of asymmetric source/drain doping on Asymmetric underlap Dual-k spacer Fin-Field Effect Transistor (AsymD-k FinFET). The Proposed unequal doping concentration of source and drain leads to superior short-channel characteristics that alleviate the OFF-current (I_{OFF}) of the device. Recently, high-k spacer materials are attracted much attention because introduction of high-k spacer material enhances the electrostatic control and suppresses the SCEs in nanoscaled devices. Introducing high-k spacer at source side restricts the source underlapped barrier. Thus, performing asymmetric doping on AsymD-k FinFET results in significant reduction in I_{OFF}, as a result there is amelioration in I_{ON}/I_{OFF} of the device.

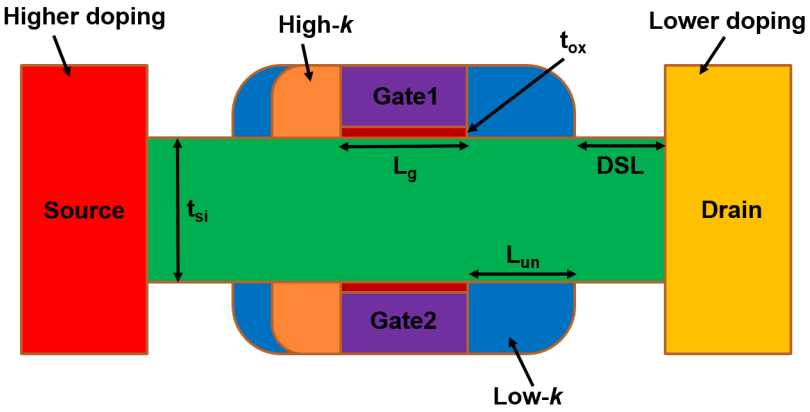


Figure 2.1: 2-D structure of AD-AsymD-k underlap FinFET.

2.2 Device Architecture and Simulation Frame Work

Figure 2.1 shows the 2-D structure of AD-AsymD-k underlap FinFET. The contrast between conventional FinFET (SD-FinFET) and presented structure here is, in SD-FinFET single silicon dioxide is used as a spacer material on both sides, source/drain both are symmetrically doped where as AD-AsymD-k underlap FinFET has different spacer material at source side (inner high-k (HfO_2) and outer low-k (SiO_2)) and asymmetric doping has performed. Table 2.1 shows the device parameters and electrical properties to satisfy the International Technology Roadmap for Semiconductors (ITRS) projections. The channel and underlap regions are lightly doped

Table 2.1: ITRS projections for High Performance (HP) device in year 2017 [1]

Device parameters	**ITRS projection value**
Physical gate length (L_g)	$14nm$
Body thickness (t_{si})	$9.4nm$
Physical oxide thickness (t_{ox})	$0.72nm$
Supply voltage (V_{DD})	$0.75V$
Channel doping (N_A)	$10^{16}/cm^3$
Source doping (N_{DOPS})	$10^{20}/cm^3$
Drain doping (N_{DOPD})	$10^{19}/cm^3$
Dopant straggle	3nm/decade

with boron concentration of $10^{16}/cm^3$ and dopant segregation length (DSL) maintained 12nm. Underlap length (L_{un}) is 8nm and work function is tuned to 4.45eV to achieve the threshold voltage of 220mV. Sentaurus TCAD tool suite has been used [48]. The quantum potential and Lombardi mobility models were activated.

2.3 Electrostatics of AD-AsymD-*k* Underlap FinFET

The conduction band profiles of AD-AsymD-k underlap FinFET and SD-FinFET are shown in Figure 2.2 at V_{GS}=V_{DD} and various values of V_{DS} (0 to V_{DD}). The conduction band profile of both the devices considered along source-channel-drain. It is perceived that, at V_{DS}=0V the conduction band edge of AD-AsymD-k underlap FinFET is at higher energy level than the SD-FinFET which shows the lower I_{OFF}.

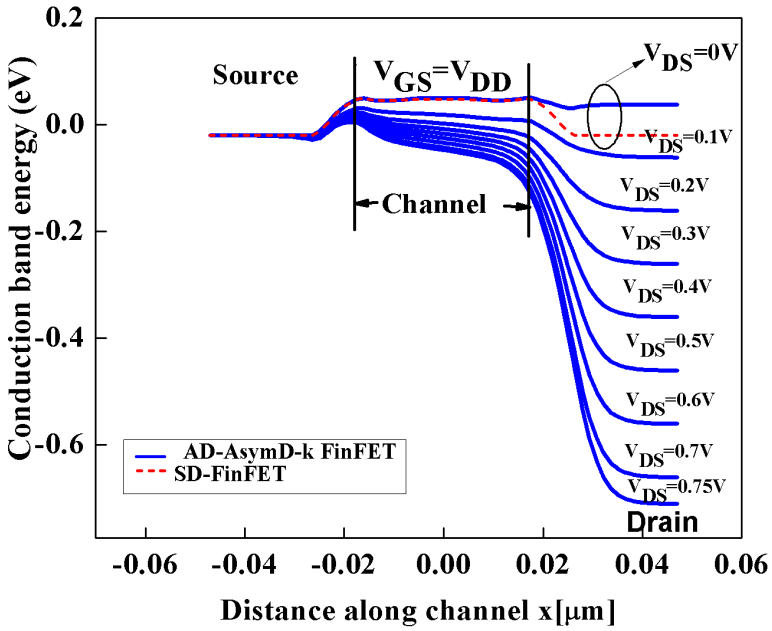


Figure 2.2: Conduction band profile of SD-FinFET and AD-AymD-k FinFET at V_{GS}= V_{DD} by varying V_{DS}.

Depletion width is nonlinearly and inversely proportional to the doping $W \propto \frac{1}{\sqrt{doping}}$. Therefore, lower doping concentration of drain terminal results in

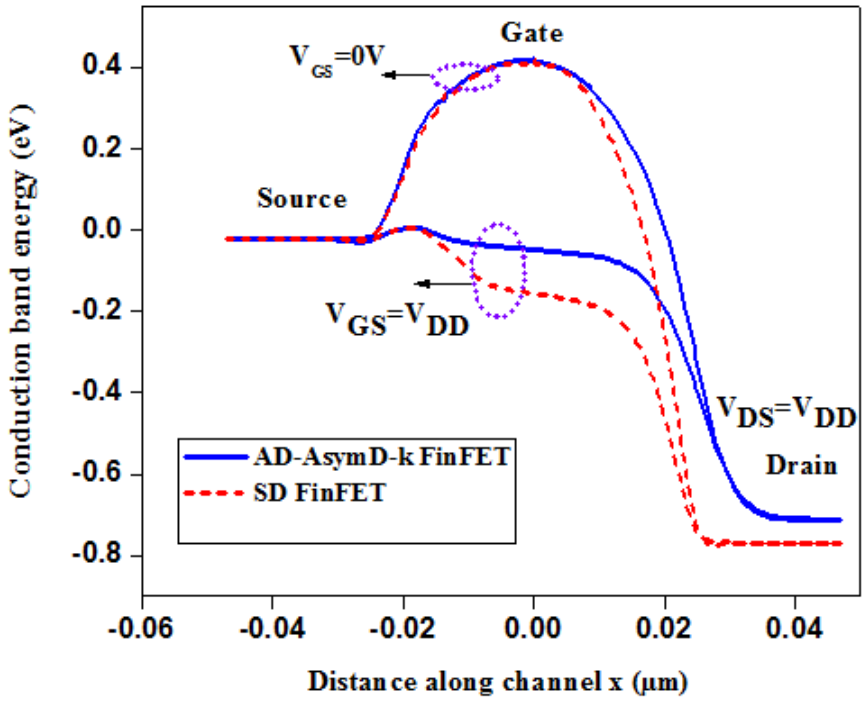


Figure 2.3: Conduction band profile of SD-FinFET and AD-AsymD-k FinFET at V_{DS}= V_{DD} for V_{GS}= 0V and V_{DD}.

wider depletion region at drain region. Because of this wider depletion region, the electric fields from drain do not reach the source underlapped barrier. It is also noticed that as increasing the drain bias, the drain underlapped barrier lowered but not much affecting the source underlapped barrier. This is because of Gate-Fringe-Induced-Barrier Lowering (GFIBL) [61].

From Figure 2.3, it is clear that the SD-FinFET exhibits lower conduction band profile than AD-AsymD-k FinFET at V_{GS}=0V and V_{DD}. It is one more evident that I_{OFF} is reduced greatly. From Figures 2.2 and 2.3, we conclude that gate control over the channel improved by performing asymmetric doping in Asym Dual-k FinFET. Figure 2.4 shows the transfer characteristics of AD-AsymD-k and SD-FinFETs. Improvement in subthreshold characteristics due to lower doping concentration of drain terminal and introduction of high-k spacer at source side.

2.4 Effect of Parameter Variations on Device Characteristics

This section presents current characteristics and SCEs of SD-FinFET, SD-AsymD-k FinFET and AD-AsymD-k FinFET.

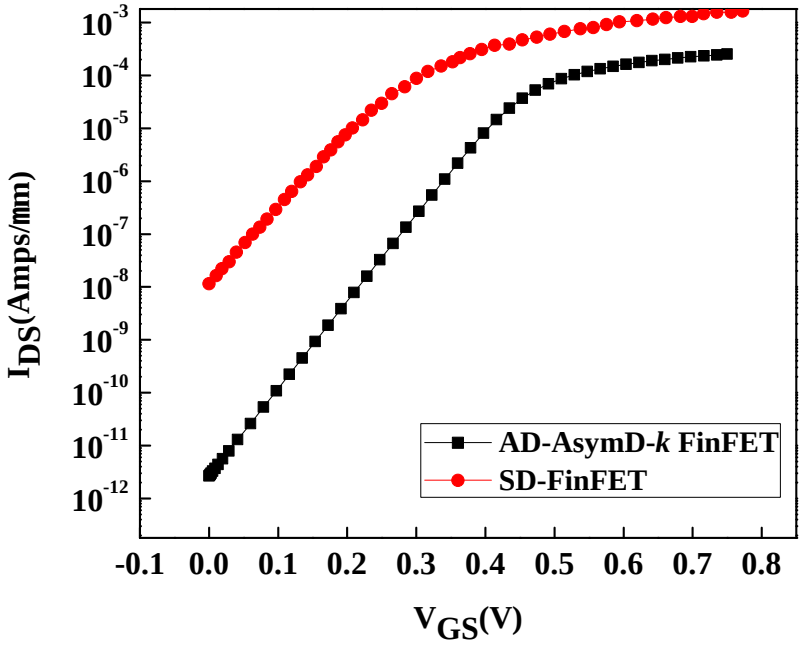


Figure 2.4: Transfer characteristics of SD-FinFET and AD-AsymD-k FinFET.

2.4.1 Comparision between SD and AD-ASymD-*k* FinFETs

In this section, we vary the device parameters about its projected value and evaluate the degradation of I_{ON}/I_{OFF}. It has been noticed that AD-AsymD-k FinFET exhibits consistently higher I_{ON}/I_{OFF} compared to SD FinFETs.

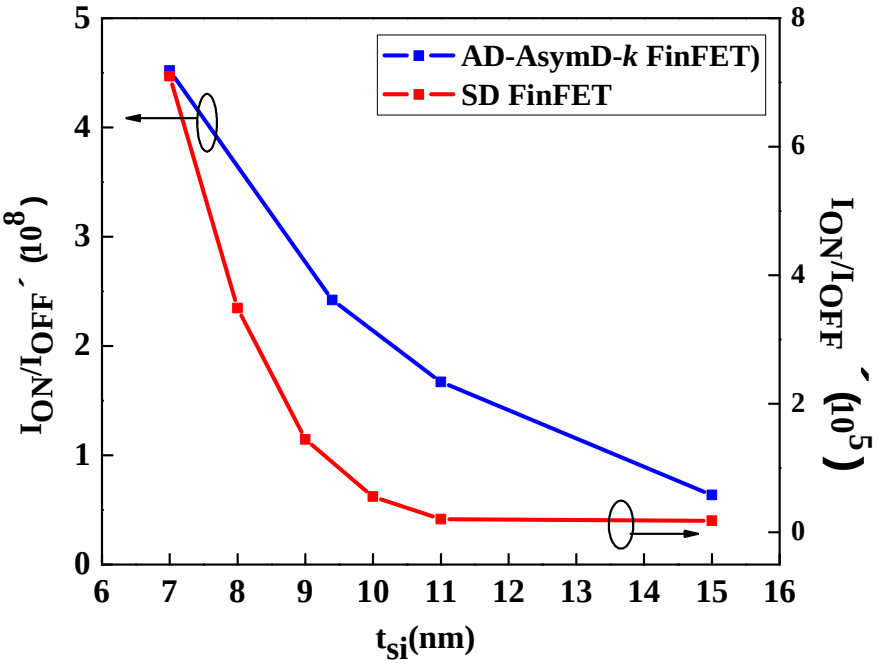


Figure 2.5: Variation of I_{ON}/I_{OFF} with t_{si} for SD-FinFET and AD-AsymD-k FinFET.

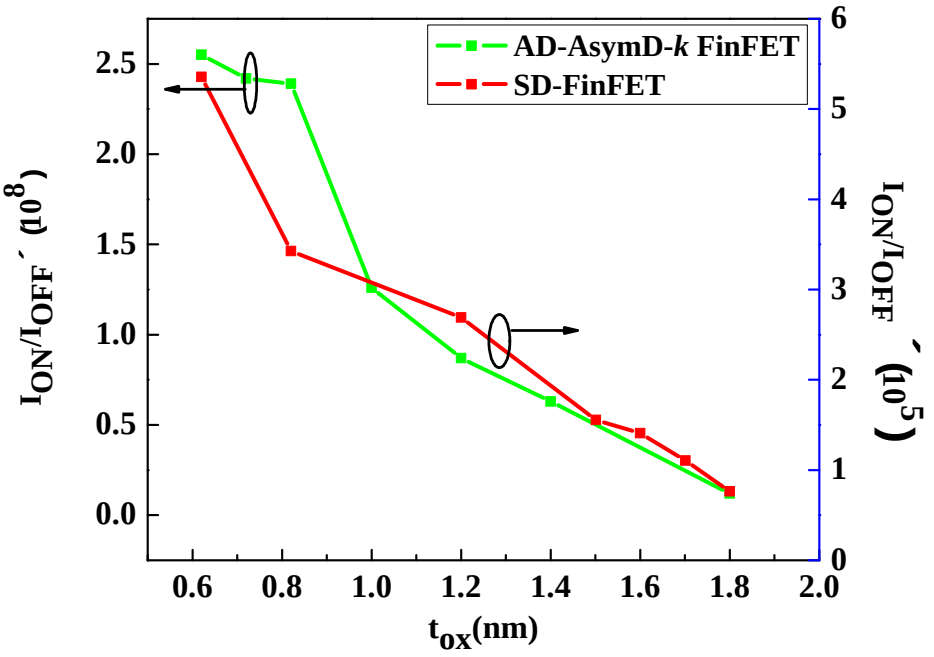


Figure 2.6: Variation of I_{ON}/I_{OFF} with t_{ox} for SD-FinFET and AD-AsymD-k FinFET.

Figures 2.5 and 2.6, show the degradation of I_{ON}/I_{OFF} of SD and AD-AsymD-k FinFETs with increasing silicon thickness (t_{si}) & oxide thickness (t_{ox}) due to degradation of SCEs. As t_{si} increases, influence of gate over the channel reduces as a result I_{OFF} increases. Hence, I_{ON}/I_{OFF} degrades. Thinner gate oxide helps to improve the SCEs but it leads to higher gate leakage. As t_{ox} increases drain electric fields increases that results in reduction in I_{ON}/I_{OFF}.

2.4.2 Comparision between SD and AD-ASymD-*k* FinFETs

Figure 2.7 shows the numerical comparison of SD-AsymD-k and AD-AsymD-k FinFET structures. AD-AsymD-k FinFET structure shows 9.11% improvement in I_{ON}/I_{OFF}, with improved SS and DIBL than SD-AsymD-k FinFET. From Figures 2.8 and 2.9, it is observed that AD-AsymD-k FinFET exhibits superior SCEs than SD-AsymD-k FinFET. At its nominal value, it achieved 64.4mV/decade (near to ideal SS) and 8mV/V in SS and DIBL respectively. This is due to the wider depletion region at drain region as drain is lightly doped than the source.

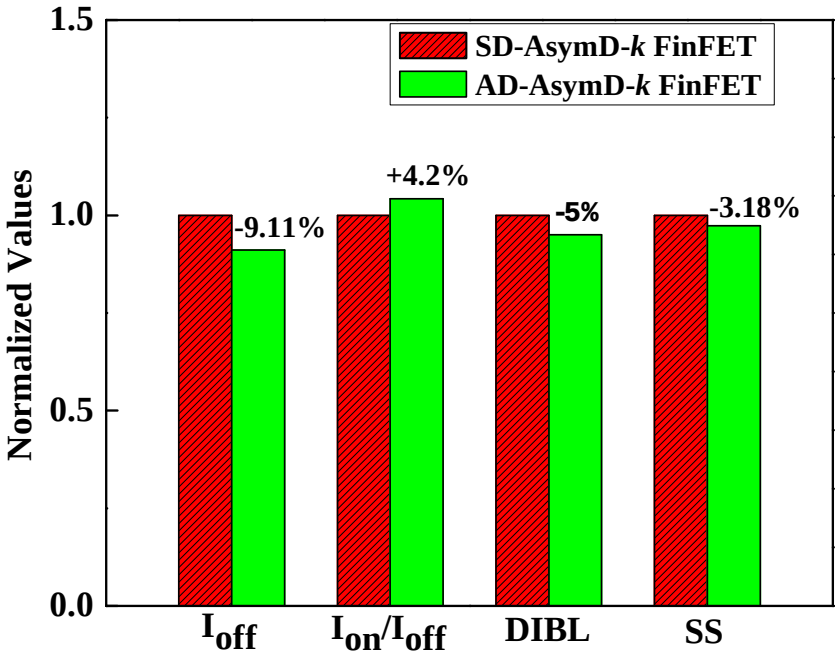


Figure 2.7: Comparison of device characteristics of SD-AsymD-k and AD-AsymD-k FinFETs.

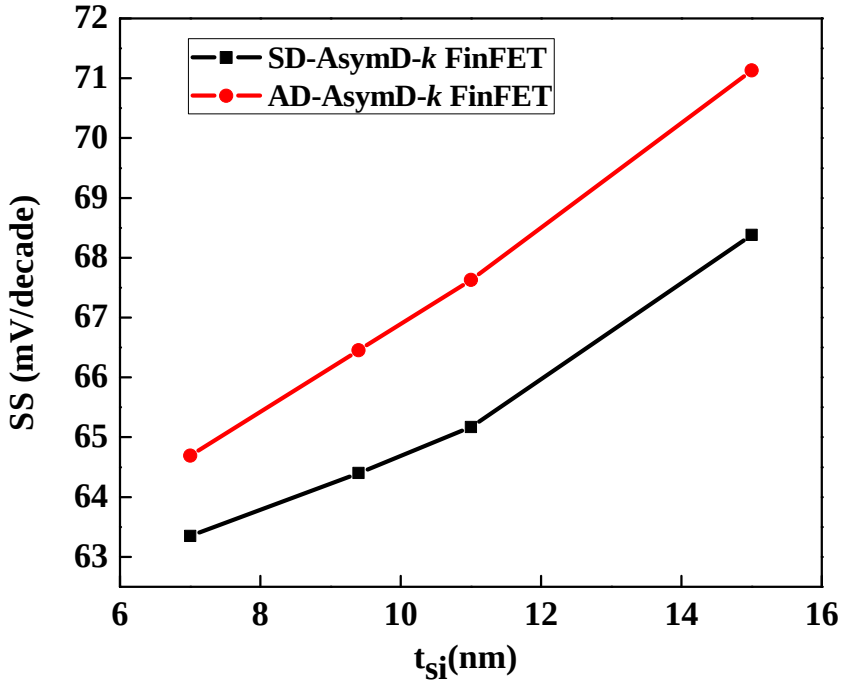


Figure 2.8: Variation of SS with t_{si} for SD-AsymD-k and AD-AsymD-k FinFETs.

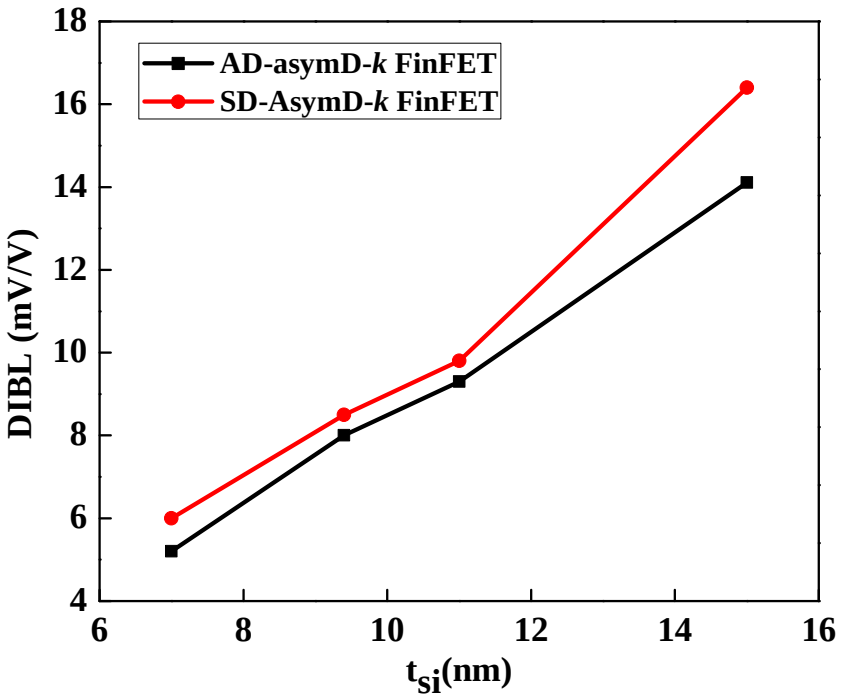


Figure 2.9: Variation of DIBL with t_{si} for SD-AsymD-k and AD-AsymD-k FinFETs.

2.5 Summary

In this chapter, we have performed asymmetric doping on AsymD-k FinFET. Lower doping concentration of drain region and introducing dual-k spacers at source side results in superior short channel characteristics viz., reduced DIBL, improved SS, lower I_{OFF} and improved I_{ON}/I_{OFF}. The proposed AsymD-k FinFET achieved near to ideal SS value (64.4mV/V) and lower I_{OFF}. It has an excellent electrostatic control over the channel because the drain electric fields do not reach the channel. Hence, designing of digital circuits with these devices is a beneficial approach.

Chapter 3

Impact of Varying Carbon Concentration in SiC S/D Asymmetric Dual-k Spacer for High Performance and Reliable FinFET

3.1 Introduction

As technology scaling, conventional scaling approach does not fulfill the CMOS technology to follow the road map requirements. To improve the device characteristics, novel materials has to be integrated in the device architecture. In this chapter, we propose a reliable asymmetric dual-k spacer with SiC source/drain (S/D) pocket as a stressor for a Si channel. This enhances the device performance in terms of electron mobility (eMobility), current driving capabilities, transconductance (G_m) and SS.

As discussed in the chapter 1, FinFET showed the intensity of VLSI research that it can be scaled up to the shortest channel length for the given gate oxide thickness [35]. The undoped underlap region facilitates to reduce SCEs and leakage current. It also reduces random dopant effects, which improves process variation effects [36]. These facilities are granted at the cost of increased S/D series resistance

($R_{S/D}$) that degrades the current driving capabilities and reliability [37] of the device. Henceforth, the need of improving the performance along with the reliability of the device are fulfilled by the use of high-k spacers, because it has the high coupling capability of the fringe field between the gate and underlap region, which reduces series resistance. On the other hand, as the value of 'k'increases, the fringe capacitance also increases that deteriorates the circuit delay. The device characteristics and circuit performance are together enhanced by using dual-k architecture in terms of symmetric and asymmetric design [38]. This creates a trade-off between fringe capacitance and $R_{S/D}$, consequently to take advantage of the high-k spacer and underlap length optimized from Yang *et al.* [39]. Many novel device architectures have been investigated in the past to improve the subthreshold characteristics. But, the improvements in subthreshold characteristics of those structures come at the cost of reduced I_{ON} [40] -[41].

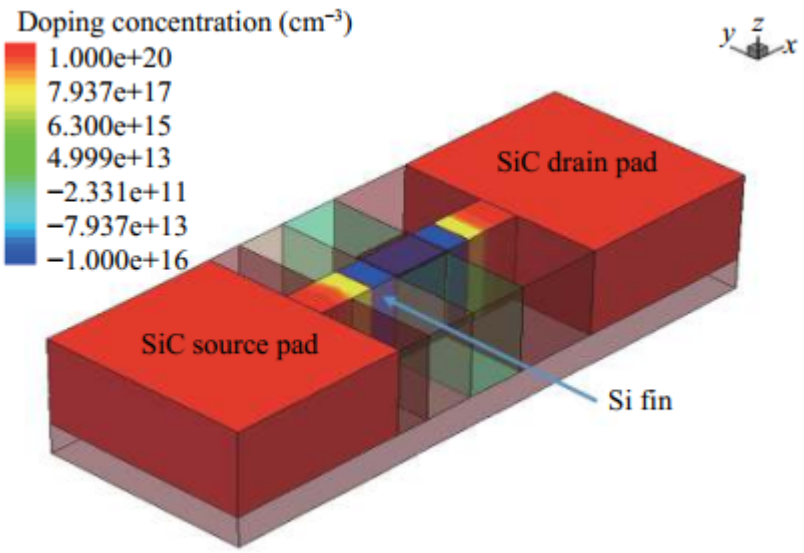
For further improvement in the on-current (I_{ON}) on the same technology node (without reducing the gate length), strain engineering in FinFET also proved itself by introducing stressors in the form of SiC and SiGe in S/D regions for n-type and p-type respectively [42]-[43]. Due to a lattice constant mismatch between Si and SiC, the tendency of SiC alloy stressor to expand causes tensile stress. Such tensile strain in the channel increases the mobility of charge carrier in SiC S/D devices. The possible increment in the drive current is due to improvement in the carrier mobility because of longitudinal uniaxial (processed induced) strain developed on the Fin due to SiC stressors [43]. The advantage of the uniaxial strain approach is that it can be engineered during the CMOS manufacturing. It has been shown that the introduction of a process induced stress in the Si channel can improve the mobility of both carrier types (n-FinFET and p-FinFET) [44]. The amount of stress introduced into the channel depends on the amount of SiC elevation, SiC lateral compression and the exact shape. The stabilised amount of stress and major challenges based on the epitaxial SiC S/D of FinFET are cautiously deliberated [45]. Among the various reliability issues, positive bias temperature instability (PBTI) is the major issue with the N-type device which was described by the many authors for various alloy based devices such as $In_xGa_{1-x}As$ FinFET [46]. But it has not been analysed for SiC FinFET, so we introduce reliability issues and their solutions for $Si_{1-y}C_y$

FinFET for the first time. In this work, we also thought-out and capture the assets of asymmetrical dual-k spacers and SiC S/D pockets to enhance the performance and reliability of N-type FinFET at the 14nm node. Variations in SCEs are also studied and explained in relation to gate lengths (L_g) at 10, 14, 18, and 22nm. We analyse the performance of SiC S/D asymmetric dual-k spacer for different mole fraction (y) in $Si_{1-y}C_y$ like the analysis done by varying the Ge mole fraction for SiGe alloy [47].

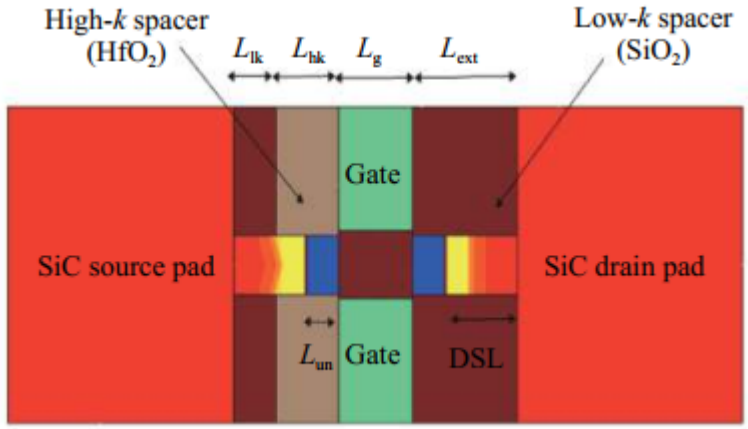
3.2 Proposed Device Structure and Simulation Method

The 3-D simulation of the device is done using the Sentaurus TCAD tool [48]. The proposed asymmetric dual-k spacer with SiC S/D FinFET 2-D and 3-D structures are shown in Figure 3.1. It consists of an inner high-k (HfO_2, $k = 25$) spacer having length L_{hk} as 12nm and an outer low-k (SiO_2, $k = 3.9$) spacer having length L_{lk} as 8nm, introduced only at the source side. At the drain side, we use a low-k spacer of length L_{ext} maintained at 20nm. The doping segregation length is 12nm. The conventional FinFET has a Si S/D and single low-k spacer throughout the extension length (L_{ext}) region from the gate edge to S/D edges. The optimized width of dual-k spacers to optimize the underlap length is considered from Pal *et al.* [49], and the key process steps are considered by Anderson *et al.*[50]. The fabrication methods of the asymmetric dual-k spacer are discussed by Cheng *et al.*[51]. Therefore, the fabrication of the proposed device is possible. Dimensions of the proposed structure are taken and calibrated according to ITRS projection 14nm physical gate length for I_{ON} and device leakage current presented in Table 3.1.

In the proposed structure we also used SiC in place of Si at the source and drain region to produce uniaxial tensile strain at the Si channel oriented at <110>orientation as the plane of conductance. For moderate stress levels, an average channel stress can be used to estimate the performance of the transistor with a non-uniform stress distribution across the channel. In order to ignore random dopant fluctuations and to increase mobility in the channel, the underlap and channel regions are considered with a lightly doped boron concentration of $10^{16}/cm^3$ [52].



(a)



(b)

Figure 3.1: (a)3-D and (b) 2-D view of the proposed asymmetric dual-k SiC S/D FinFET.

Table 3.1: Device parameters of the proposed device [1]

Device parameters	**ITRS projection value**
Physical gate length (L_g)	$14nm$
Body thickness (t_{si})	$9.4nm$
Physical oxide thickness (t_{ox})	$0.72nm$
Supply voltage (V_{DD})	$0.75\,V$
Channel doping (N_A)	$10^{16}/cm^3$
Source doping (N_{DOPS})	$10^{20}/cm^3$
Drain doping (N_{DOPD})	$10^{20}/cm^3$
Dopant straggle	$3nm$/decade

In this work, all the simulations are performed using a density gradient model for carrier transport. The quantum potential model is enabled to include the quantum confinement effect of inversion carriers in the the thin body and also the direct tunnelling model is used to consider the gate leakages. The enhanced high-k Lombardi mobility model has been enabled to account for high-k mobility degradation at the semiconductor-insulator interface. A hydrodynamic transport model and the Hobler model was used to simulate the damage profiles [48].

3.3 Simulation Results and Discussion

A well-designed device has to be optimized in the domain of performance, reliability and process variation effects, so that the device will work efficiently with a long working lifetime along with the easy and reasonable fabrication cost. Hence we present the simulation study of these areas for the proposed device in the below subsections through the medium of this chapter. The device calibration is done for the experimental data available for Si S/D FinFET, whereas we are analyzing for the first time the reliability and process variation issue for SiC S/D based FinFET under following subsections.

3.3.1 Performance Analysis of the Proposed Device

The capability of the Sentaurus Process (Synopsys TCAD) to recalculate the stresses in the structure due to carbon redistribution allows the simulation of the stress formation due to the silicon-carbon pockets. The longitudinal tension generated in the Si channel region breaks the symmetry of the band structure resulting in a decrease of electron effective mass along the channel. Moreover, a redistribution of the carrier to low effective mass subband valleys reduces interband scattering of electrons in the channel caused by the stress along x and z directions. Consequently, the electron mobility increases, so does the I_{ON}. The piezo resistive coefficients can have dependencies with respect to the normal electric field or the mole fraction or both. Hence the stress along the channel increased by increasing mole fraction of C(y) and the mobility of electron also increases, which results in the enhancement of the drive current. At the 14nm gate length (L_g) the variation in drive current

due to variation in C mole fraction (y) in $Si_{1-y}C_y$ shown by the I_{DS} versus V_{GS} curve at $V_{DS} = V_{DD} = 0.75$ V in Figure 3.2. Also, it is checked by the I_{DS} versus

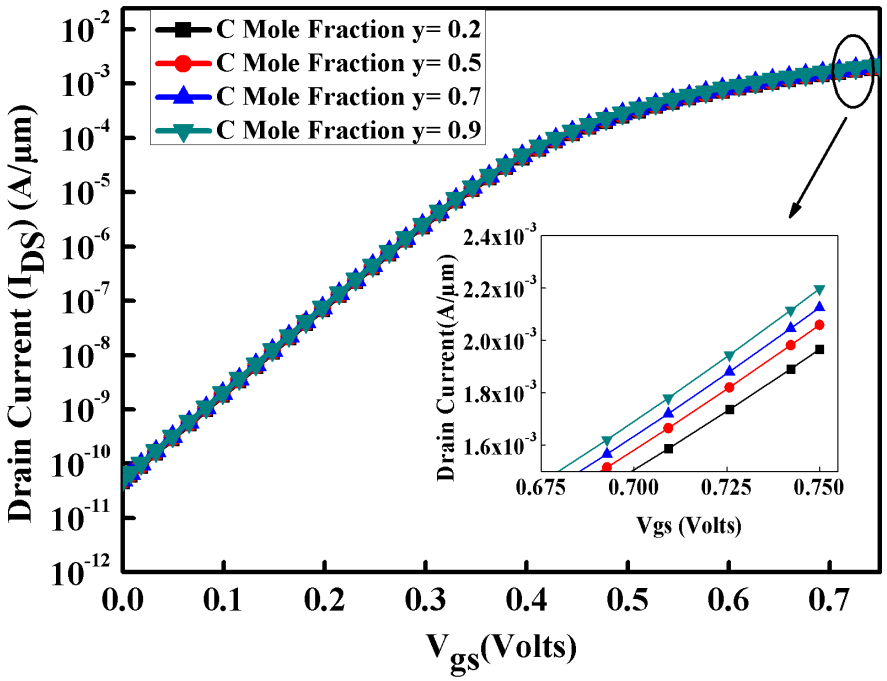


Figure 3.2: Variation in I_{DS} with respect to V_{GS} at $V_{DS} = 0.75$ V for different values of y in $Si_{1-y}C_y$.

V_{DS} curve at 0.75 V as V_{GS} in Figure 3.3. By taking $V_{DS} = V_{GS} = 0.75$ V and the value of C mole fraction y in $Si_{1-y}C_y$ is 0.7 in our proposed device structure. The $Si_{0.3}C_{0.7}$ S/D stressor considered here is approximately the largest C content such that the material is still like Si and also this amount of content is feasible from the device design context because the higher value of C can distort the lattice structure. In addition to the stressors effect, a high-k spacer at the source side helps to increase the I_{ON}/I_{OFF} and reduces the SCEs. The high-k spacers are used to increase the electric field coupling between the gate and the underlap regions, this further increases the I_{ON}/I_{OFF}; therefore, the performance of the proposed device increases. By studying the I_{DS}–V_{DS} curve for different values of V_{GS} shown in Figure 3.4, the results demonstrate the linear region and saturation region of the proposed device. The saturation behaviour of the device degrades with scaling of the device due to different mechanisms such as SCEs and source-drain resistance. In the proposed device, we noticed less saturation degradation because of reduction in source-drain series resistance [53].

The performance of the device depends on the current driving capability of the

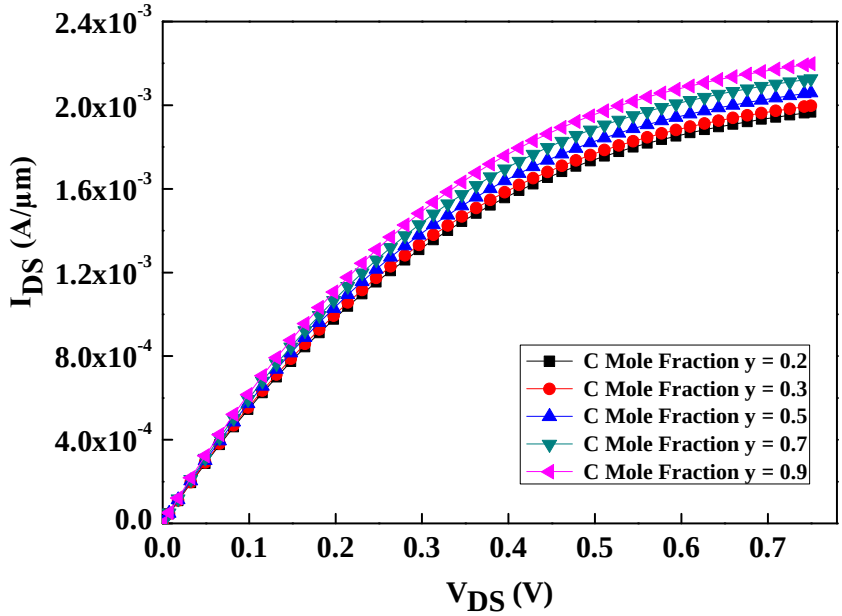


Figure 3.3: I_{DS}–V_{DS} curve of the proposed device at $V_{GS} = 0.75$ V for various values of y in $Si_{1-y}C_y$.

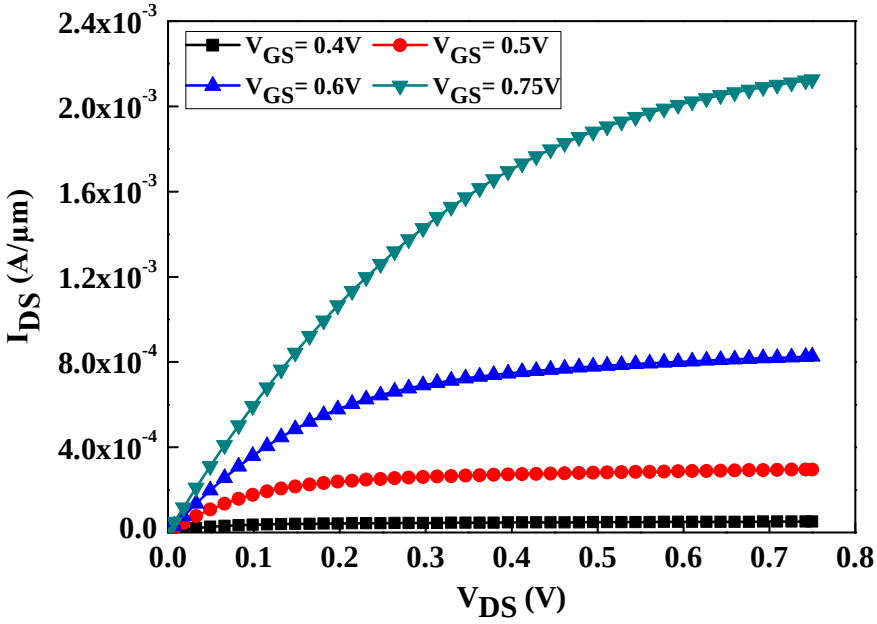


Figure 3.4: I_{DS} –V_{DS} curve of proposed device structure considering $Si_{0.3}C_{0.7}$

device and current driving capability depends on the mobility of charge carrier. Hence we study the variation of electron mobility along the channel for different gate length considering constant Fin thickness (t_{si}) of 9.4nm shown in Figure 3.5. The increase in mobility with the scaling of the device is because of the increase in the undoped or less doped region towards the S/D region; the stress effect becomes more useful for small-scale L_g. The increase in electron mobility also increases the

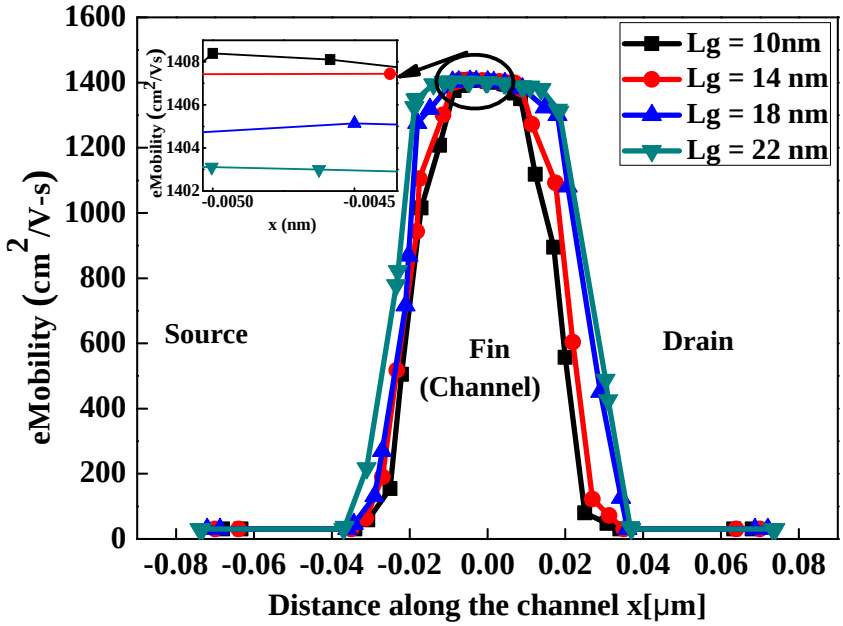


Figure 3.5: eMobility at the centre of the channel for gate lengths (L_g) 10, 14, 18, and 22nm at constant fin width.

I_{ON}, which is presented by comparing the $\log(I_{ON}/I_{OFF})$ curve of the reference *Si* FinFET with the proposed asymmetric dual-k spacer SiC FinFET sample in Figure 3.6. This also shows that the S/D stressors become adequate in introducing tensile stress when the L_g scale down. The electron transportation near the strained

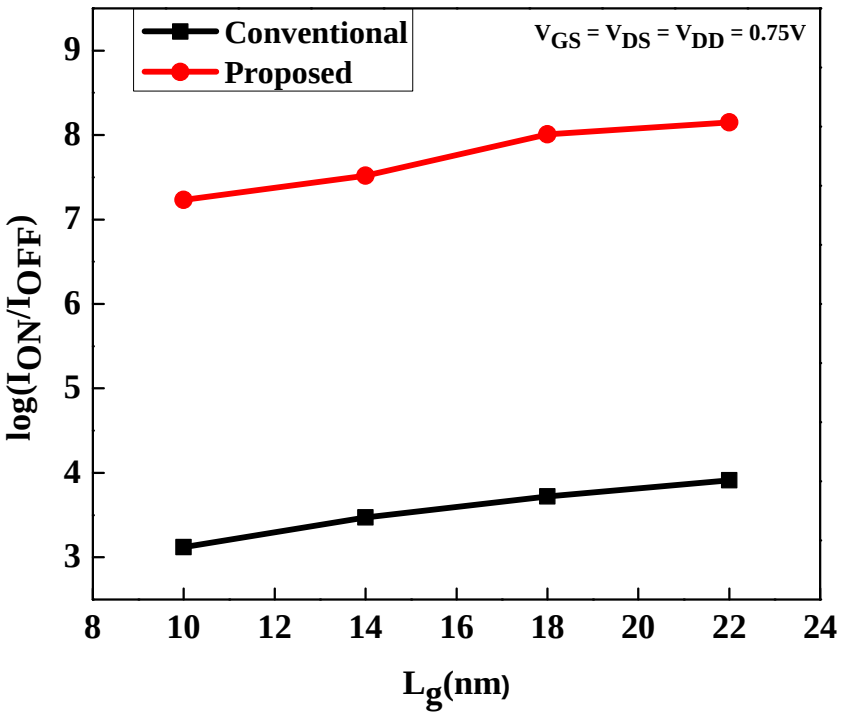


Figure 3.6: Variation of $\log(I_{ON}/I_{OFF})$ with respect to gate length (L_g).

Si/oxide interface for the strained Si device at the subthreshold bias provides a better gate control, and thus a smaller SS of the proposed device is obtained as compared to the conventional device. The potential of the drain decays as the length increases, hence the SS of both the devices decreases with the increase in L_g. It is observed that the amount of SS of Si S/D conventional structure at L_g = 14nm is larger even than the SS of proposed device structure at L_g = 10nm. The reduction in SS by introducing of this novel structure of FinFET can be clearly observed from the SS versus L_g curve Figure 3.7. The trans-conductance against the V_{GS} for

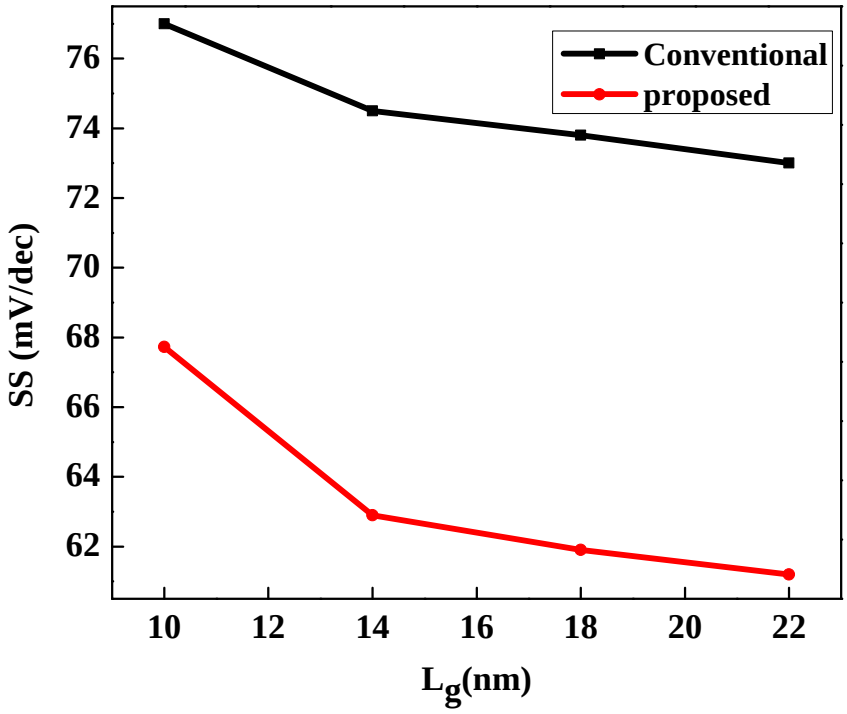


Figure 3.7: Change in subthreshold swing (SS) at different gate lengths (Lg).

both types of devices is shown in Figure 3.8. The peak linear transconductance for the FinFET with SiC S/D is much higher compared to that of the FinFET with Si as an S/D material, indicate a higher electron mobility enhancement due to induced stress. As we show above, the variation in eMobility with the change in L_g and the transconductance is directly proportional to the eMobilty. Hence, the transconductance also increases accordingly. This is mainly because of reduction in series resistance due to strain in the Si channel and the dual-k spacers at the source side. Hence an improved transconductance is obtained which helps to improve device performance. The proposed device improves the performance, but it reduces the reliability that will affect the device yield in terms of chip lifetime. Further

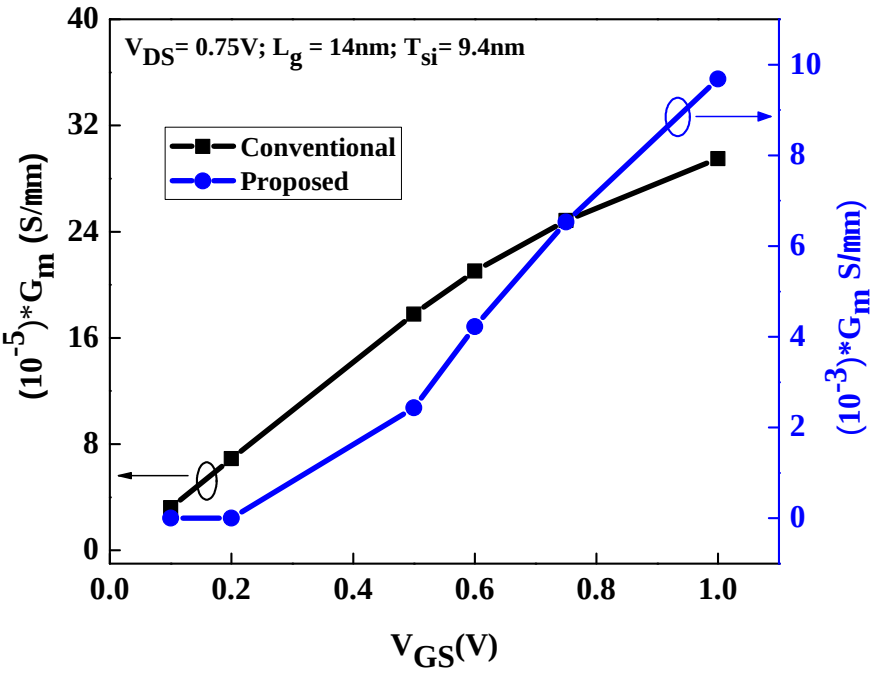


Figure 3.8: Variation of G_m with V_{GS} for the proposed and Si S/D conventional FinFETs.

reliability is analysed and gives possible solutions.

3.3.2 Reliability Analysis

The improvement in device performance is imperative, but the reliability of the device is also a crucial point that shows the device lifetime. Reliability of the device is analysed by the relaxation method, scaling of device degrades the electrical properties because hot carriers break the bond at the Si/Oxide interface and some of them are also trapped in the former bulk defects. Along with hot carrier injection (HCI), positive bias temperature instability (PBTI) is also a serious issue in n-type device, it breaks the SiH dangling bond at the Si/Oxide interface and allows the incorporation of the charge carriers in the gate oxide. To compensate these trapped charges more potential is required, this increases the threshold voltage which is shown in Figure 3.9 by means of different carbon mole fraction (y) for 14nm gate length. The effective mole fraction helps to improve the reliability shown in Figure 3.9. Because it has a direct impact on strain in the Si channel, which contributes to improving the reliability and in the proposed device maximum reliability is obtained at the maximum considerable mole fraction, which is 0.7. In Figure 3.10, we study

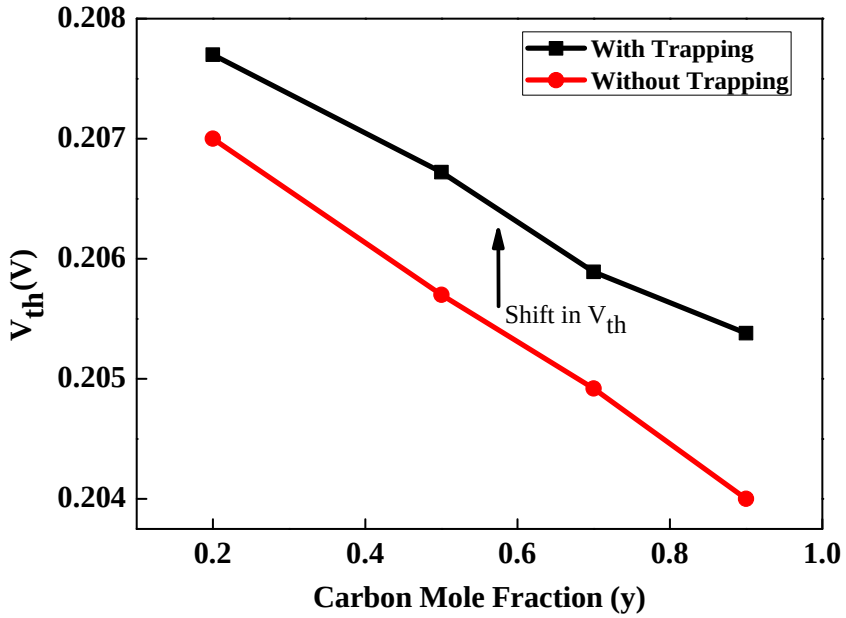


Figure 3.9: Variation in V_{th} with C mole fraction and trapped charge.

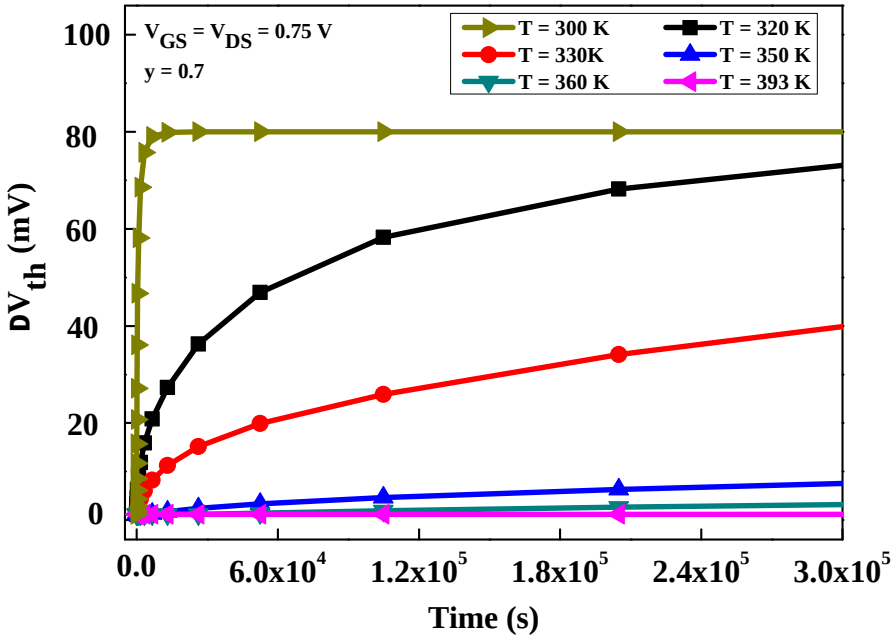


Figure 3.10: Shift in ΔV_{th} at different temperature levels with time.

the ΔV_{th} variation with the stress time from 0 to 3×10^5s at different temperature points to check the recovery of trap charges, and we analyse that the traps at room temperature do not recover and hence the change in V_{th} is large at room temperature. In the process of temperature increment from room temperature to 393K, the detrapping rate becomes approximately equal to the trapping rate, hence the overall trapping rate becomes low and the V_{th} decline towards a negligible amount. The varying mole faction of carbon helps to increase the reliability of the device, it

can also take the advantage to reduce the practical process variation effect on the performance and the total yield of the device.

3.4 Process Variation Effect

To examine the effect of process variation in the proposed device we analysed that the addition of carbon mole fraction in the $Si_{1-y}C_y$ enhances the effect of process variation expressed in terms of change in eMobilty with respect to change in doping concentration at the S/D region of arsenic from 10^{18} to $10^{22}cm^3$. It is clearly observed that the variation in eMobility is very much less for $Si_{0.5}C_{0.5}$ than the $Si_{0.3}C_{0.7}$ and $Si_{0.25}C_{0.75}$ up to N_D at $10^{21}cm^3$. It is because of sufficient carbon atoms present in the substrate and reduces the RDF in the source/drain of the device. The sequence of variation in the eMobilty is $Si_{0.25}C_{0.75} > Si_{0.3}C_{0.7} > Si_{0.5}C_{0.5}$ which is reflected in Figure 3.11. This study shows that the proposed device structure has improved its

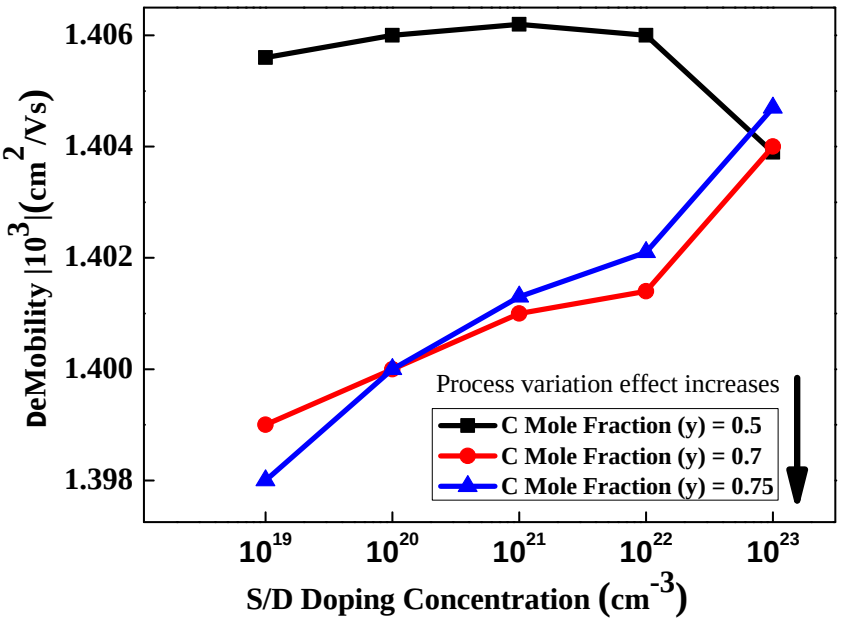


Figure 3.11: Analysing the process variation effect by change in eMobility with S/D doping concentration for different mole fraction of C in SiC.

performance and reliability along with a reduced process variation effect, hence it is suitable for future high yield IC fabrication.

3.5 Conclusion

In this chapter, we have proposed a novel asymmetric dual-k spacer based reliable and high-performance SiC FinFET device for future IC fabrication. We also studied the performance, reliability and process variation effect of the proposed SiC S/D Asymmetrical Dual-k spacer n-type FinFET. The SiC stressor provides a longitudinal uniaxial stress in the channel region to increase the charge carrier mobility, I_{ON}, SS. Hence, the large drive current is obtained at optimized SCEs at different gate lengths of 10, 14, 18, and 22nm. In addition to this, the improved reliability is demonstrated by the PBTI analysis and the process variation effect is highlighted by the eMobility variation with the S/D doping concentration.

Chapter 4

Strain Engineering for Performance Enhancement of AsymD-k FinFETs for Digital Circuit Applications

4.1 Introduction

As discussed in the previous chapter, the relentless down scaling of bulk MOSFET causes increased SCEs, degraded current driving capabilities and higher leakage current. Thus, it limits the scaling of Complementary MOS (CMOS) devices beyond 32nm node. The controllability of the gate over the channel can be ameliorated by alternative technologies such as ultrathin body SOI MOSFETs [54] and multi-gate devices [55][56]. Among all the Double Gate (DG) devices quasi-planar DG structure has attracted considerable interest of todays semiconductor industry owing to their lower SCEs and scalability than the conventional planar transistors.

However, the conventional FinFET exhibits poor subthreshold characteristics at lower technology nodes due to high longitudinal electric field from the drain. These subthreshold characteristics can be improved by introducing the underlap between gate-to-Source/Drain (S/D) of the device, but it increases the effective channel length of the device than physical gate length (L_g) that causes increase in channel resistance. However, such increase in effective channel length lowers the

SCEs at the cost of degraded I_{ON} [57, 58]. Recently, high permittivity (k) spacer materials have been extensively used below 20nm technology node to improve the gate controllability over the channel [59, 60]. This is due to the gate-induced fringe field lines [61]. However, as k value increased the mobility will be degraded due to enhanced trap charges and it worsens the circuit delay [55]. The high-k spacer materials inordinately increases the fringe capacitance (C_{fr}) that degrades circuit performance. Hence, it is paramount important to use optimum high-k spacer materials that simultaneously improves the device and circuit performance. The use of channel-strain engineering has been an enabling technology to limit the down scaling of semiconductor devices. The introduction of strain in the channel improves the device performance through higher carrier mobility[44]. Employing recessed strained SiGe/SiC in the source and drain regions of planar Si PMOS/NMOS devices improve the current driving capabilities[42]. This is due to the combined effect of mobility improvement due to strain and reduction in contact resistance. Because of nonplanar structure of FinFET, parasitic effects in FinFET are being more prominent[62]. The coupling capacitance between the Fin-shaped channel extension and other parts of the circuit is much larger than that in the planar MOSFET, which worsens the circuit delay.

As technology advances, the important constraint of Static Random Access Memory (SRAM) cell is conflict between Read Static Noise Margins (RSNMs) and write margins (WMs) which are an unavoidable design constraint. Hence, the auspicious ways to enhance the performance metrics of SRAM at lower V_{DD} is the introduction of SiGe/SiC material in the source and drain regions. Here, we prove that the combined effect of channel mobility enhancement and asymmetric dual-k placed at source offers better improvement in performance metrics of SRAM cell. Many novel device architectures have been investigated in the past to explore the technology-circuit co-design approach [33, 63, 34, 40, 41]. Although these devices have the ability to improve the subthreshold characteristics at the cost of poor current driving capabilities. This chapter discusses a new approach that combining strain induced effects with asymmetric dual-k spacers to improve the device/circuit performance.

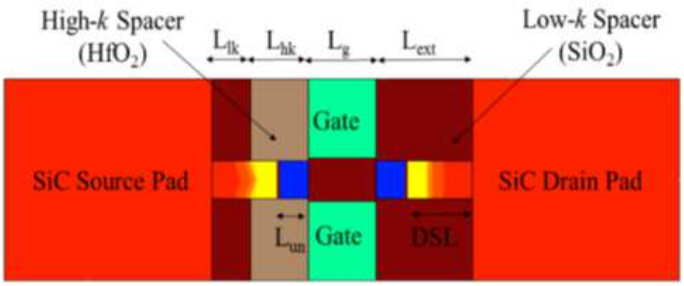


Figure 4.1: 2-D Cross sectional view of SiC AsymD-k underlap FinFET.

4.2 Device Architecture and Simulation Setup

Figure 4.1 describes the two-dimensional (2D) cross-sectional view of proposed SiC-AsymD-k underlap FinFET. The proposed device used SiGe/SiC material in the source and drain regions for PMOS/NMOS. The device structure considered with L_g of 14nm, Si body thickness (t_{si}) of 9.4nm and effective oxide thickness of 0.72nm in fulfilment of ITRS projections for high performance device in year 2017 [1]. The gate electrode thickness maintained approximately double the L_g value [39]. To gain high mobility and to avoid random dopant fluctuations, the channel is lightly doped with boron concentration of $10^{16}/cm^3$ [55]. Dopant segregation length maintained 12nm. Underlap length (L_{un}) is 8nm, work function of metal gate are tuned to 4.45 eV for n-type and 4.77 eV for p-type to achieve the required threshold voltage. The proposed device has dual-k spacers at source side unlike conventional FinFET. In conventional FinFET, single spacer material is used on both sides, whereas the proposed device has different spacer materials at source side [inner high-$k(HfO_2)$ and outer low-k (SiO_2)]. The lengths of inner high-k (L_{hk}) and outer low-k (L_{lk}) are 12 and 8nm, respectively.

Sentaurus Technology Computer Aided Design (TCAD) and mixed device/circuit tool has been used to analyse SRAM performancemetrics [48]. Density gradient model for carrier transport with Arora mobility model that accounts for ionised impurity scattering and temperature dependency. The quantum potential model is enabled to include the quantum confinement effect of inversion carriers in the thin body also the direct tunneling model is used to consider the gate leakages. The enhanced high-k Lombardi mobility model has been enabled to account for high-k mobility degradation at semiconductorinsulator interface. Some other transportation

models used for the simulation are Philips unified mobility model, hydrodynamic transport model.

4.3 Results and Discussion

4.3.1 Current-Voltage Characteristics of SiC/SiGe AsymD-*k* Underlap FinFET

The introduced SiC in the S/D regions act as stressors to induce lateral tension and vertical compression in the *Si* channel results in enhancement of electron mobility. Figure 4.2 shows the I_{DS} versus V_{GS} characteristics for different C content in the $Si_{1-y}C_y$ for V_{DS} = 0.75 V. Owing to generated longitudinal tension in the channel region, the effective mass of the electron decreases and it also reduces inter-band scattering of electrons in the channel caused by stress along x and z directions. As a result, the stress along the channel increased by increasing mole fraction of C(y). The $Si_{0.3}C_{0.7}$ S/D stressor considered here is approximately the higher amount of C content which is feasible from the device fabrication point of view because the higher amount of C can distort the lattice structure. The high-k inner spacer is used to enhance the GFIBL[61] [64] that reduces the S/D series resistance $R_{S/D}$. The

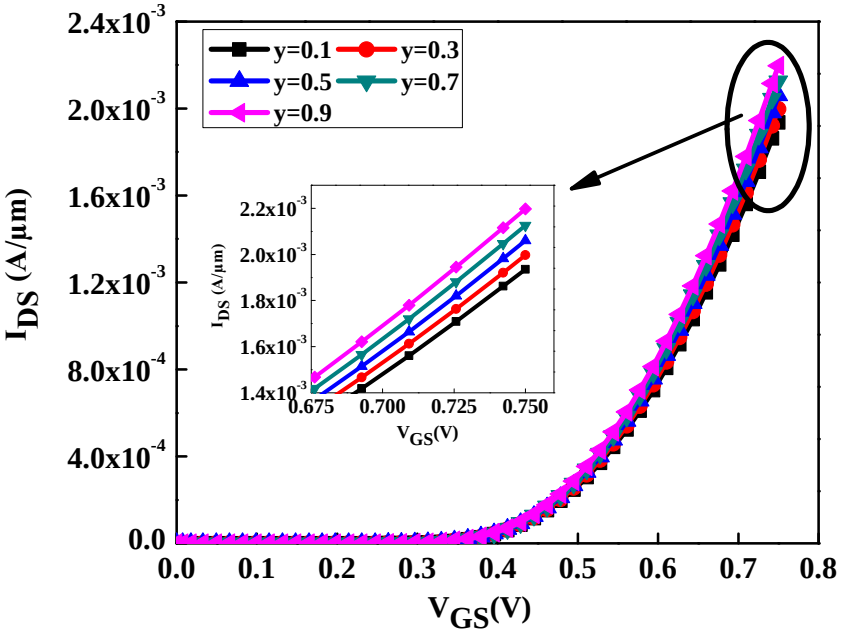


Figure 4.2: Variation in I_{DS} for different values of y in $Si_{1-y}C_y$ at V_{DS}=0.75V.

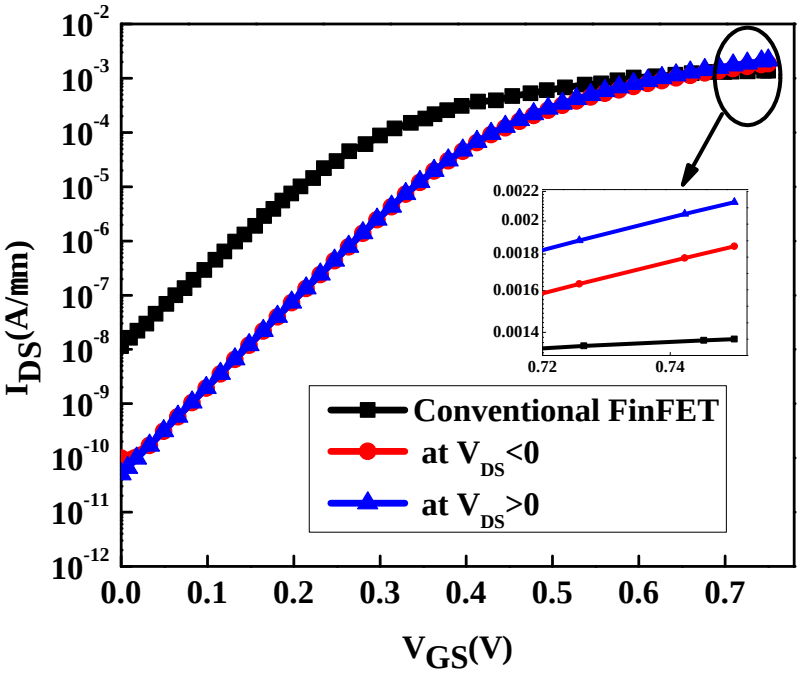


Figure 4.3: Transfer characteristics of conventional FinFET and SiC AsymD-k FinFET.

proposed device exhibits higher I_{ON} for higher amount of C mole fraction because the combined effect of strain-induced effects and asymmetric dual-k.

Introduced dual-k at source terminal causes the difference in magnitudes of currents for positive and negative drain-to-source voltages V_{DS}. From Figure 4.3, it is perceived that the proposed device has the higher-current driving capabilities for V_{DS} >0 than V_{DS} <0. This asymmetry in the current driving capabilities offers to achieve improvement in both read and write stability of 6T SRAM cell. As proposed, device shows consistently high I_{ON} for V_{DS} >0, the rest of the analysis has done among the proposed device for V_{DS} >0 and conventional FinFET. The output characteristics of the proposed device as shown in Figure 4.4 for V_{GS} value ranging from 0 to 0.75 V. In saturation region, the drain current is almost constant for a given V_{GS} value which shows lower-output conductance. The digital performance metrics of the proposed SiC-AsymD-k underlap FinFET and conventional FinFET structure are shown in Figure 4.5. The proposed structure exhibits 54.098% improvement in I_{ON}/I_{OFF} with improved subthreshold characteristics than conventional FinFET.

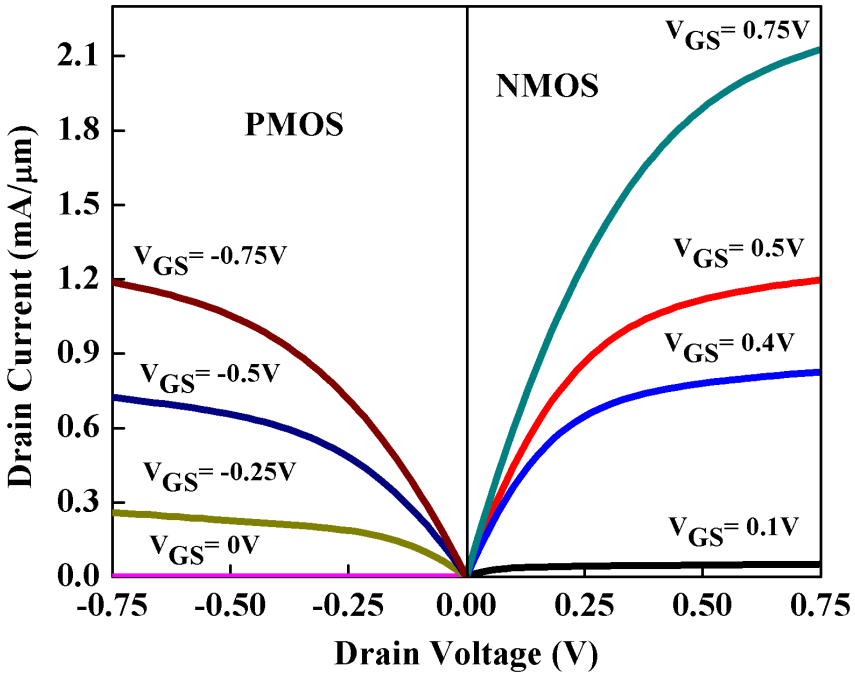


Figure 4.4: Output characteristics of proposed NMOS and PMOS devices.

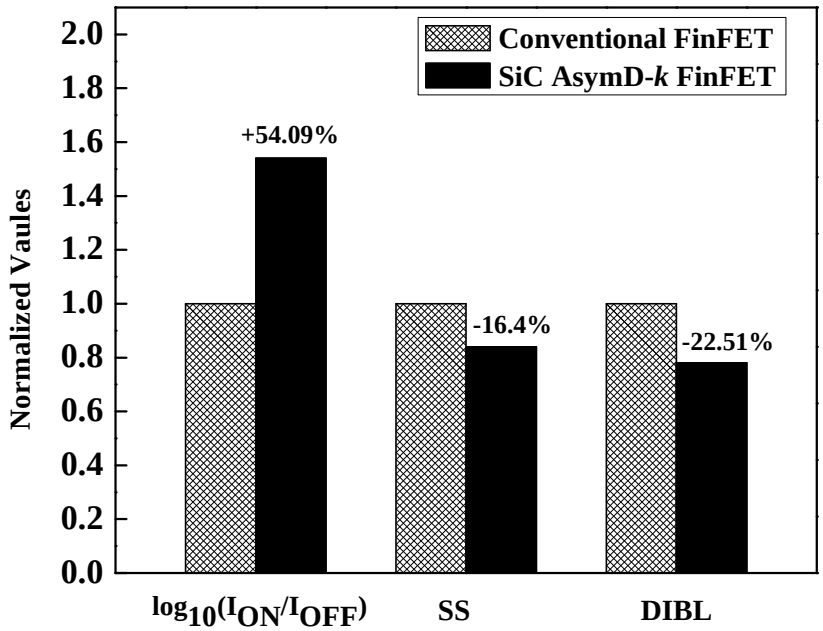


Figure 4.5: Comparison of device characteristics of conventional and SiC-AsymD-k FinFETs.

4.3.2 Effect of Variation of C/Ge Content in SiC/SiGe on Charge Carrier Mobility and $R_{S/D}$

The performance enhancement of the proposed device achieved through higher carrier mobility and reduced source/drain resistance is shown in Figures 4.6 and 4.7. Because the lattice mismatch between SiGe and *Si*, the channel region is placed

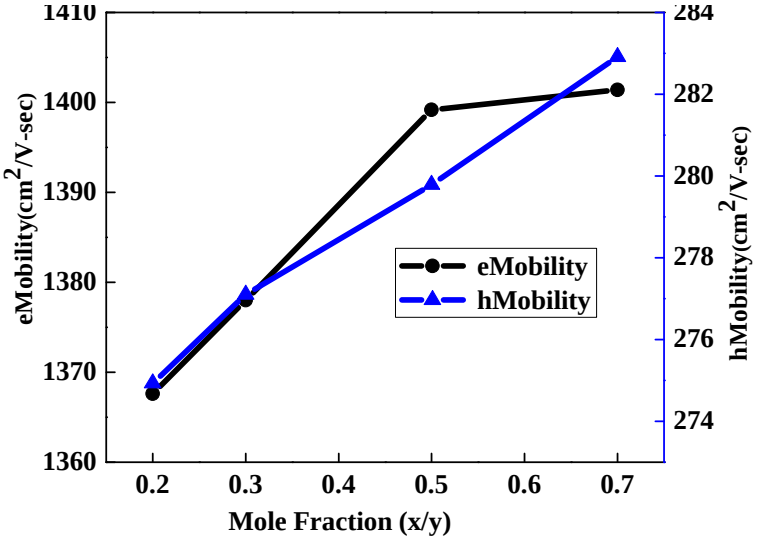


Figure 4.6: Charge carrier mobility versus mole fraction of SiGe/SiC AsymD-k FinFETs.

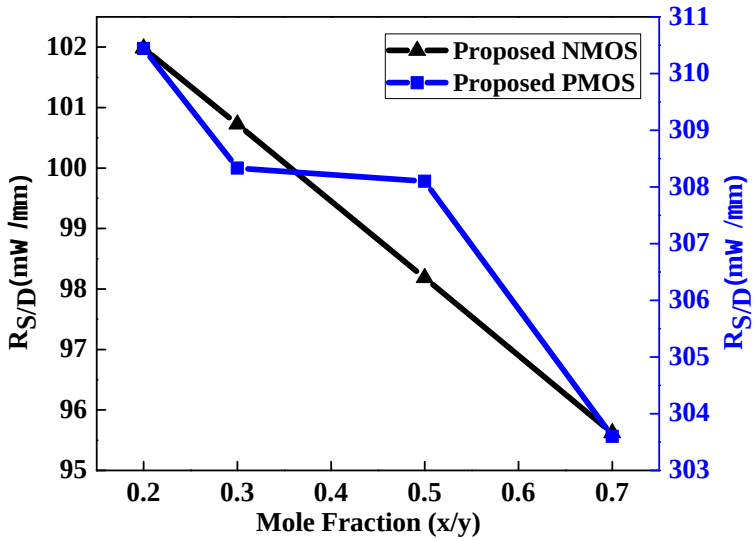


Figure 4.7: Change in $R_{S/D}$ for different mole fractions(x/y).

under uniaxial compressive stress, this type of stress enhances the hole mobility and thus PMOS performance. Since PMOS is a worst circuit component due to its intrinsic lower hole mobility compared to the electron mobility. Therefore, the behavior of these devices in circuits need to be investigated for sub-14nm gate length devices.

4.3.3 Effect of Variation of Carbon Content in $Si_{1-y}C_y$ on Short Channel Effects

The dependence of significant parameters like DIBL, SS, and threshold voltage (V_{th}) on gate length for different values of y in $Si_{1-y}C_y$ has been summarized in this section. Figures 4.8 to 4.10 plot the variation of DIBL, SS and V_{th} with gate length (7.5 to 20nm) for different carbon mole fraction C(y). It is noticed from Figures 4.8 to 4.10 that for a given carbon content C(y) in SiC, SS and DIBL of the device decreases with increase in gate lengths. The short channel effects become prevalent for varying carbon content in SiC due to improved gate control over the channel region. The threshold voltage decreases with increasing carbon content because of decrease in source-channel/drain-channel built-in potential barrier.

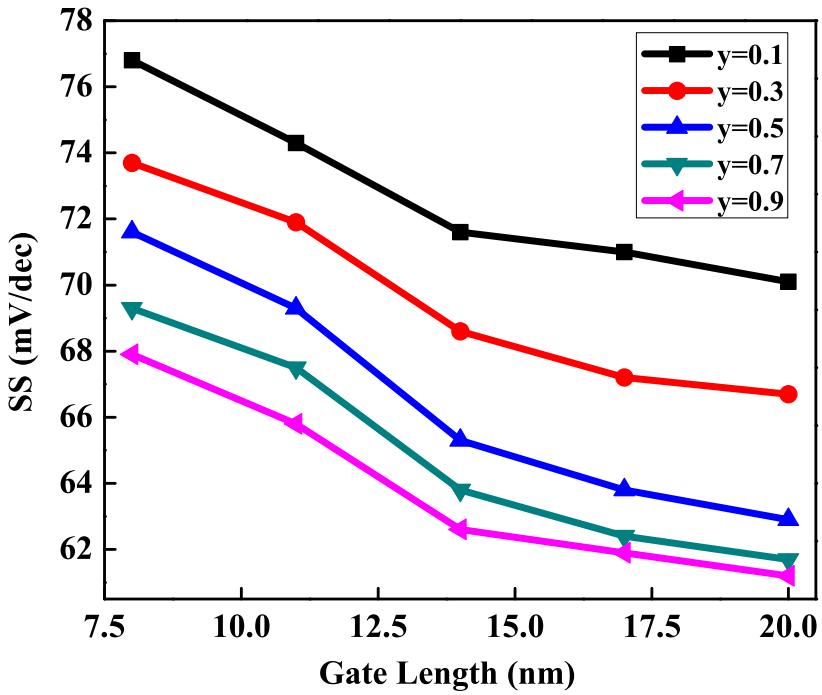


Figure 4.8: Variation in SS with varying gate length for different values of y in $Si_{1-y}C_y$.

4.3.4 Effect of Variation of Carbon Content in $Si_{1-y}C_y$ on C_{GS} and C_{GD} of SiC AsymD-k Underlap FinFET

Although, FinFET offers several challenges at device level, it also propounds new challenges at circuit level due to higher magnitude of parasitics. Higher magnitudes

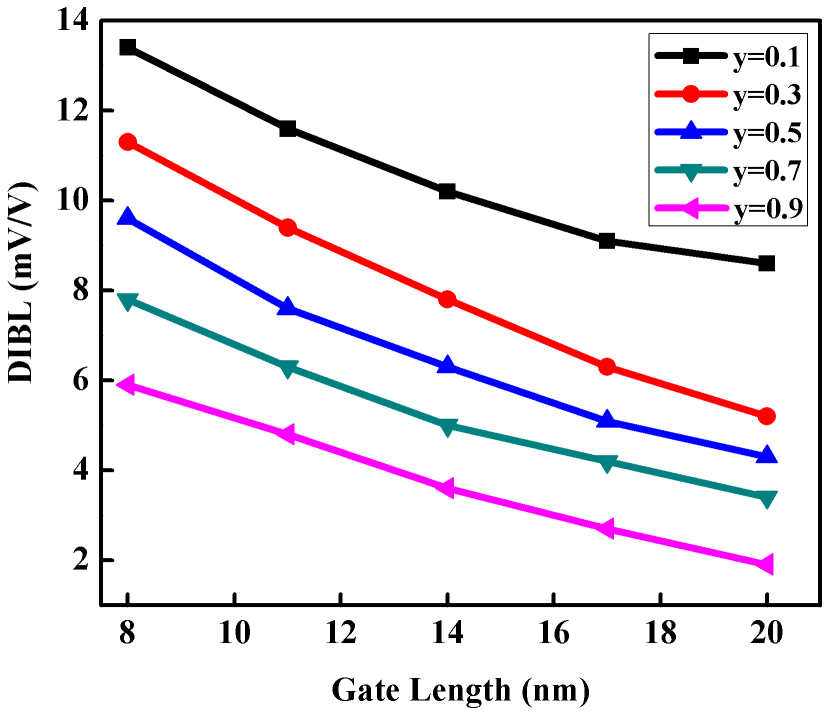


Figure 4.9: Variation in DIBL with varying gate length for different values of y in $Si_{1-y}C_y$.

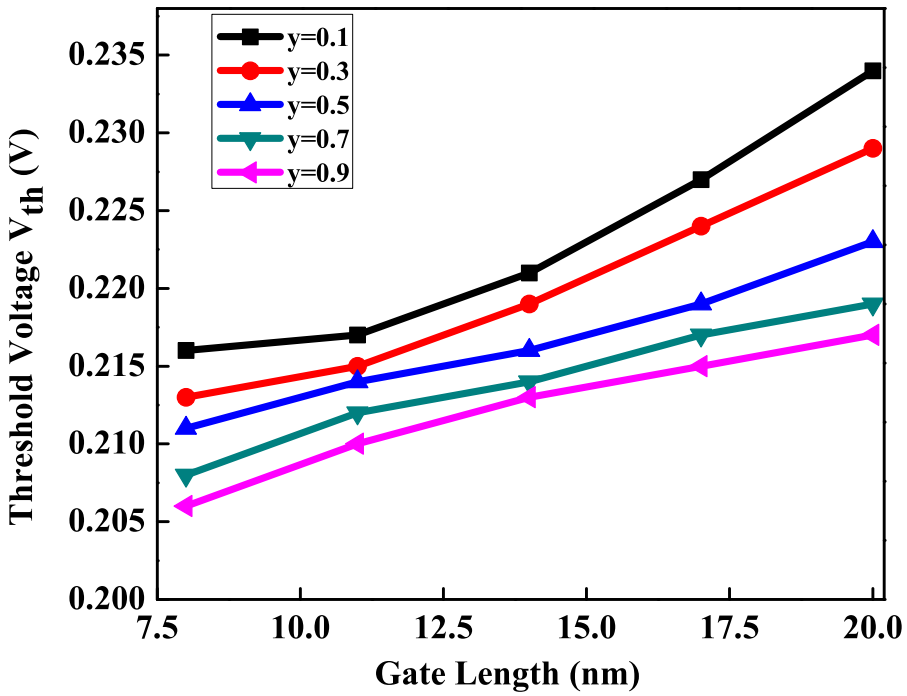


Figure 4.10: Variation in V_{th} with varying gate length for different values of y in $Si_{1-y}C_y$.

of parasitic capacitance causes degradation in dynamic circuit performance of high-k spacer device. In an underlap devices, total gate capacitance (C_{GG}) is a sum of gate-to-channel (C_{GC}) and fringe capacitance (C_{fr}) components. C_{GG} is further divided

into gate-to-source (C_{GS}) and gate-to-drain capacitance (C_{GD}). So, Figure 4.11 depicts the contribution of C_{GS} and C_{GD} in overall C_{GG} with varying carbon content C(y). One can notice that the contribution of C_{GD} component much lesser than the

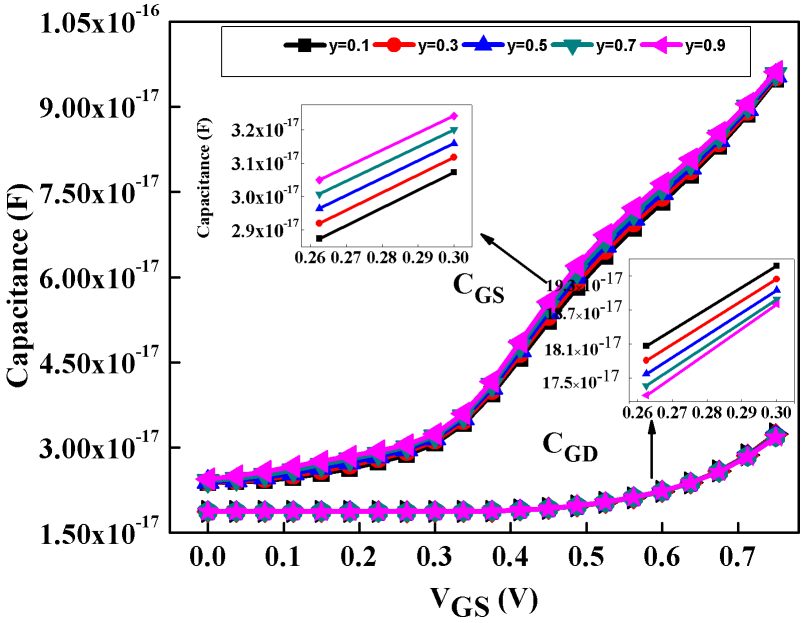


Figure 4.11: Variation in C_{GS} & C_{GD} for different values of y in $Si_{1-y}C_y$ at V_{DS}=0.75V.

C_{GS} component in the overall C_{GG}. C_{GS} component increases rapidly as increasing the C content that shows the higher current driving capabilities of the proposed device. The C_{GD} component plays an important role from the circuit perspective (delay and switching performance). For a logic circuit, the delay performance is directly dependent on the miller effect associated with C_{GD}. For the proposed device, as C content increases the C_{GD} component lowered which is evident that using proposed device in digital circuits greatly reduces the delay of the circuit. A higher value of C_{GD} in the high-k device worsens the circuit delay and switching performance.

4.3.5 SiGe/SiC-AsymD-k FinFET-based 6T SRAM Cell

The proposed device architecture governed by the performance metrics of a 6T SRAM cell. The immunity of SRAM cell to static noise is expressed in terms of SNM. Figure 4.12 shows the schematic representation of SiGe/SiC-AsymD-k based 6T SRAM bit cell. At the nanoscale regime, an avoidable design constraint of 6T

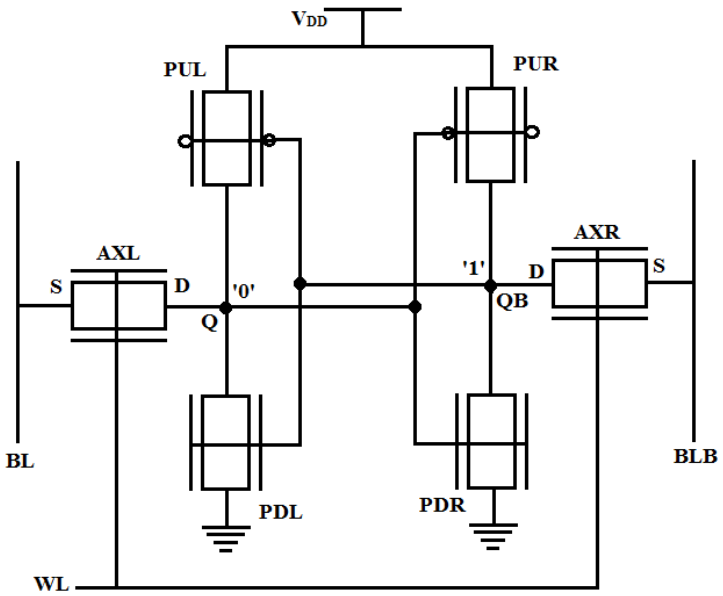


Figure 4.12: Schematic of SiGe/SiC AsymD-k based 6T SRAM cell.

SRAM cell is the conflict between read and write. During the read operation, both the bit lines (BLs) [BL and BL bar (BLB)] are precharged to supply voltage (V_{DD}) and word line (WL) is asserted to turn on the access transistors (access transistor left (AXL) and access transistor right (AXR)).

Since access pass transistor AXL and the pull-down PDL form a voltage divider, and the cell 0 storage node Q voltage rises V_Q, which is called read disturb voltage. If V_Q is higher than the trip voltage of the other inverter, it leads to read failure. Hence, for higher read stability, it is desirable to have a small ratio (strength ratio of access pass transistor AXL to pull-down PDL). During write operation, BL and BLB are maintained at V_{DD} and ground (GND), respectively. On asserting the WL the voltage at storage node QB (V_{QB}) is discharged. Successful write operation achieved if V_{QB} is less than the trip point of other inverter. Hence, for higher write ability strong access transistor is desired.

The proposed device exhibits improved subthreshold characteristics that improve the SRAM cell performance metrics. As the proposed device offers different current driving capabilities for V_{DS} >0 and <0 which is already demonstrated in Section 3.3.1. This asymmetricity helps to mitigate the read–write conflict. As the proposed device has lower drain induced barrier lowering (DIBL) that improves the stability of the SRAM cell. SNM has the negative correlation with DIBL. Designing of

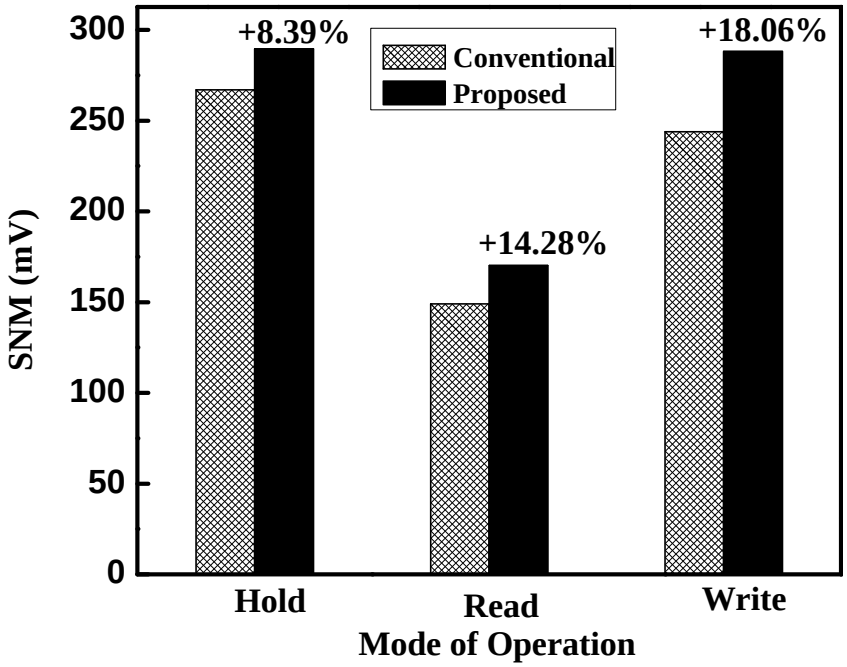


Figure 4.13: SNM comparison in all possible modes for conventional FinFET SRAM and proposed SRAM.

SRAM cell using the proposed device improves the SNM consistently with compared with conventional FinFET SRAM cell as shown in Figure 4.13. SiGe/SiC-AsymD-k FinFET based SRAM cell achieved SNM improvement 8.39% in hold, 14.28% in read and 18.06% in write mode.

4.3.6 Effect of Scaling of Supply Voltage and Temperature on SNM of SiGe/SiC-based 6T SRAM Cell

SRAM contributes majority of the leakage on the chip, which has the serious impact on the battery life of the portable devices. The supply voltage reduction is an effective way of reducing the leakage. Scaling of supply voltage limited by a tolerable noise immunity [65]. Figures 4.14 to 4.16 show the effect of the scaling of supply voltage on hold, read and write SNMs, respectively. Compared to conventional, SiGe/ SiC-AsymD-k underlap FinFET-based SRAM shows 9.77-24.160% improvement in read SNM and 4.26-8.26% improvement in WM. The proposed configuration is not a suitable candidate in the subthreshold region because it shows significant improvement for higher V_{DD} only. This is due to scaling of supply voltage increases source-side resistance. In Figures 4.14 to 4.16, as supply voltage scaled down, show

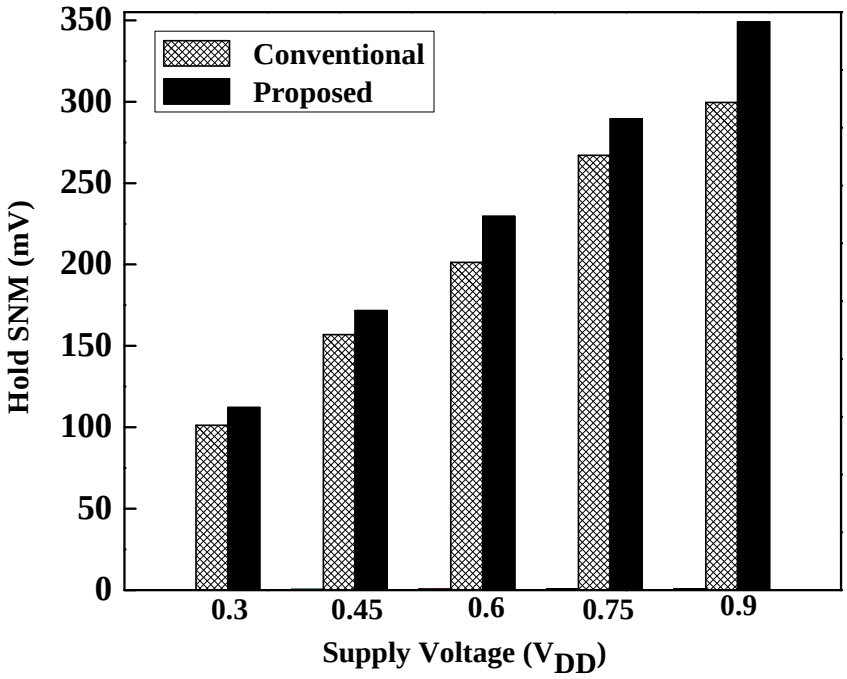


Figure 4.14: Comparison of hold SNM with supply voltage scaling.

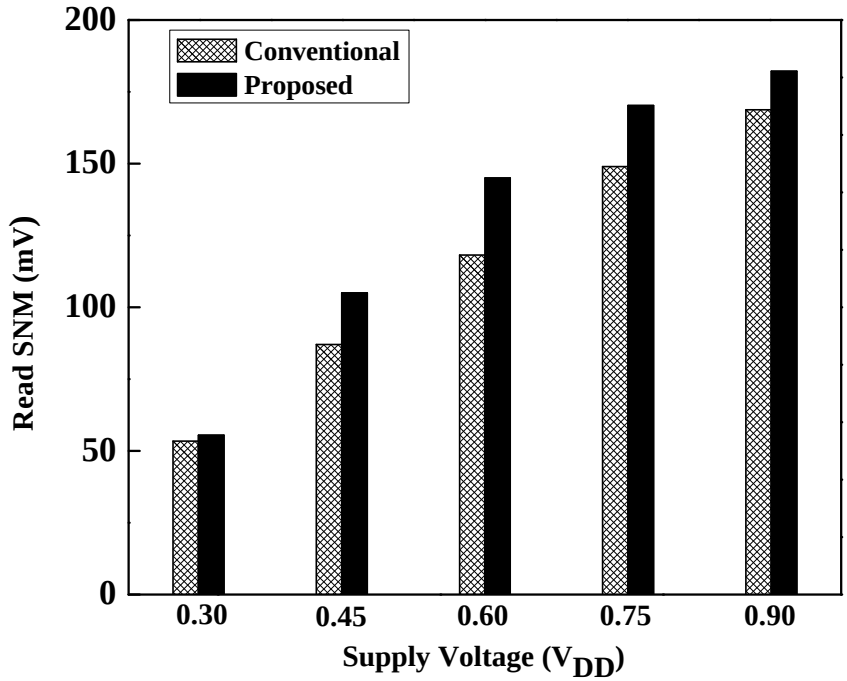


Figure 4.15: Comparison of read SNM with supply voltage scaling.

SNM is lowered in all three possible modes (hold, read and write).

Figure 4.17 shows the SNM of SiGe/SiC-AsymD-k FinFET-based 6T SRAM in all possible modes at $V_{DS} = 0.75$ V versus temperature. As temperature increases, SNM is lowered in all the modes of SRAM because drain current decreases with

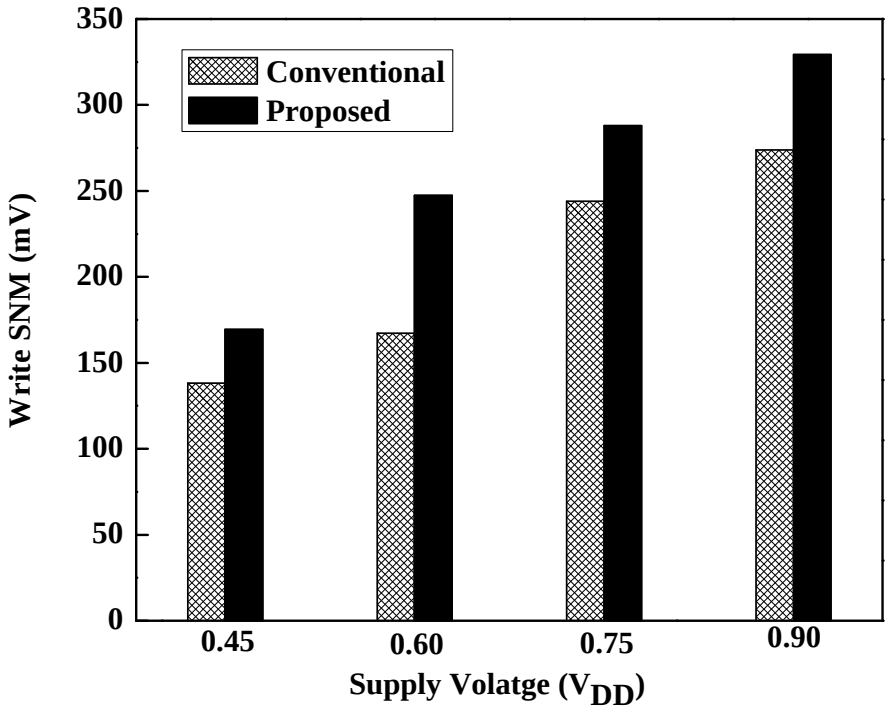


Figure 4.16: Comparison of write SNM with supply voltage scaling.

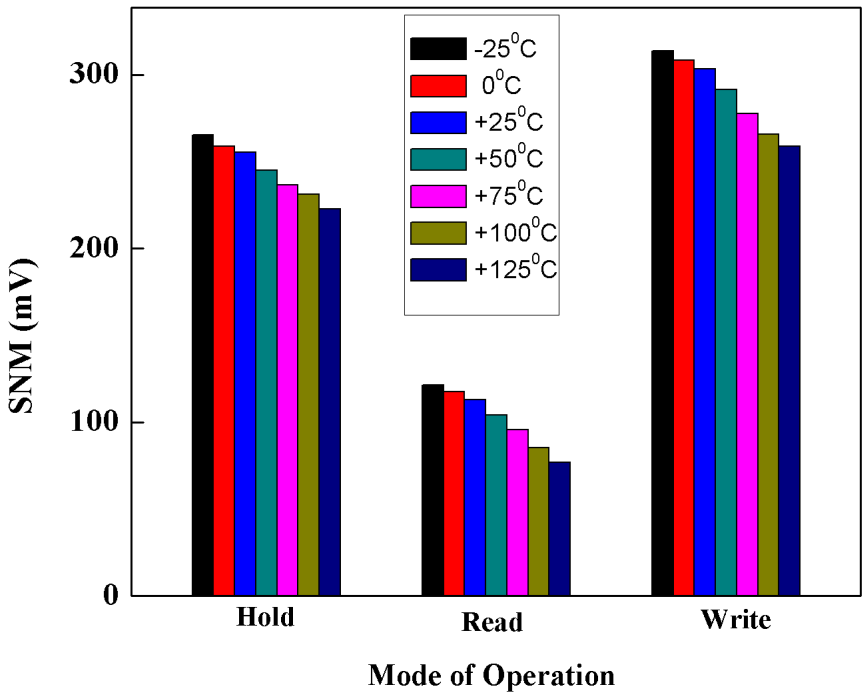


Figure 4.17: Impact of temperature on hold, read and write SNMs for the proposed SRAM bit cell.

increasing temperature. Thus, the proposed SRAM cell offers superior variation immunity and lesser temperature sensitivity.

4.3.7 Effect of Variation of Ge/C Content (in $Si_{1-x}Ge_x/Si_{1-y}C_y$) on SiGe/SiC AsymD-*k* Spacer FinFETs based Inverter

The foremost concern of any digital circuit designer is to enhance the stability and switching speed Although SiC AsymD-k FinFET achieves excellent electrostatics, it worsens the circuit delay as k value increases. To improve the circuit performance, we used SiC/SiGe source and drain (S/D) regions as discussed in the section 4.3.4, the proposed device exhibits lower C_{GD} component that results reduced delay of the circuit. For digital circuit applications, the device performance is studied as a function of carbon content for a inverter. AsymD-k FinFETs based inverter has been demonstrated using mixed mode circuit simulations. To obtain the maximum noise margin (NM) and symmetrical voltage transfer characteristics (VTC), we maintained , the P-type to N-type fin width ratio of a FinFET inverter is 2:1. This section demonstrates the VTCs of the AsymD-k FinFETs based inverter with an increase in carbon content C(y). Figure 4.18 depicts that the slope in the transition region increases with decreasing the carbon content C(y). A sharp transition region obtained when carbon content increases that results in enhanced stability. SiC AsymD-k FinFET exhibits higher I_{ON} with lower DIBL. However, the slope in transition region is not directly dependent on the value of I_{ON}[66]. Ostensibly, the noise margin has a negative correlation with DIBL [67]. By using the proposed device architecture the noise margin improved significantly.

The timing characteristics of the input and output signals are shown in Figure 4.19 along with low-to-high delay time (τ_{LH}) values indicated. τ_{LH} is defined as the time interval between 50% of the input voltage and output voltage of the transient response. As input signal changes its value from high-to-low voltage, the driver device starts to turn off. The circuit delay τ_{LH} primarily depends on drive current. As discussed in the previous sections, drive current increases and C_{GD} component lowered with increase in carbon content in $Si_{1-y}C_y$. Hence, as carbon content in $Si_{1-y}C_y$ increases, circuit delay reduces.

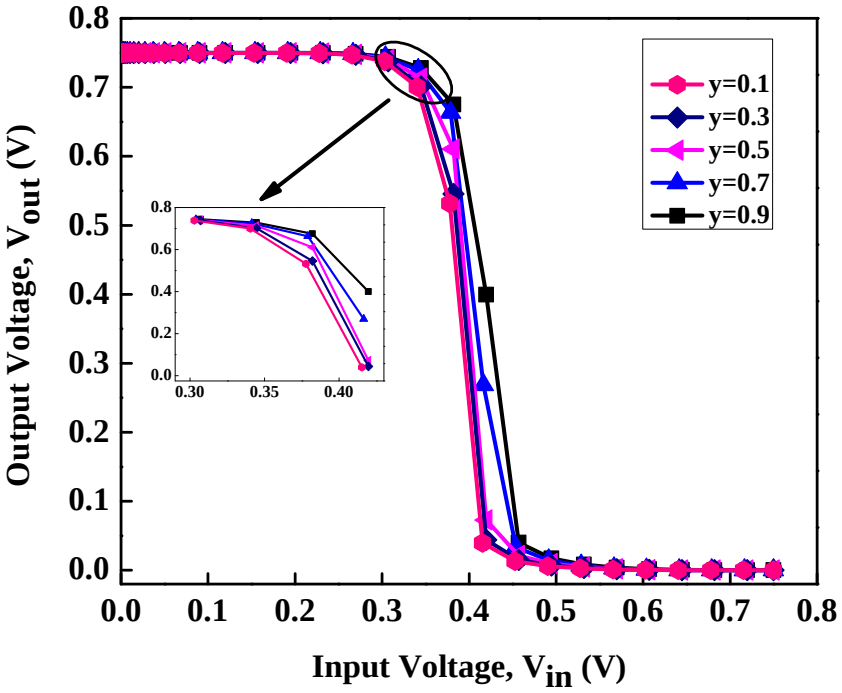


Figure 4.18: Variation in VTC of proposed inverter for different values of y in $Si_{1-y}C_y$.

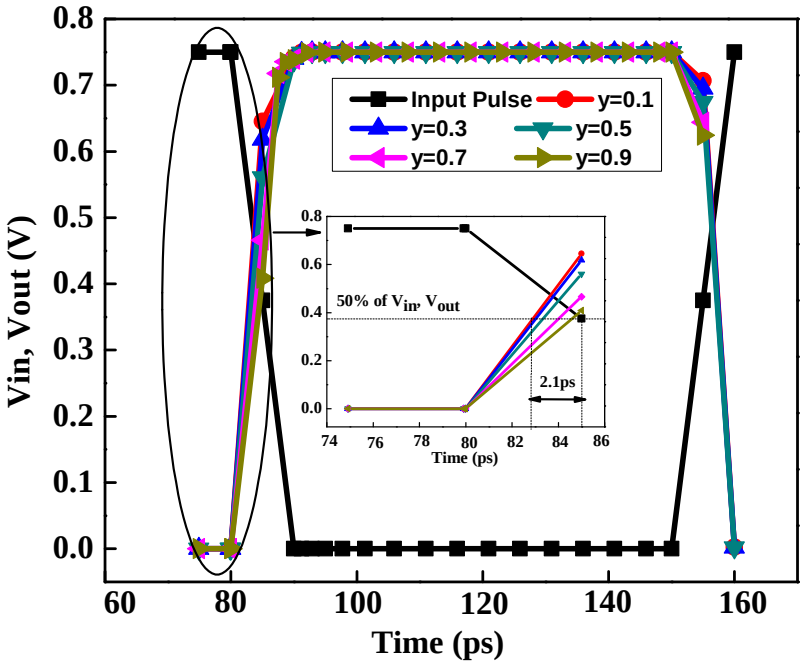


Figure 4.19: Variation in timing characteristics of proposed inverter for different values of y in $Si_{1-y}C_y$.

4.3.8 Effect of Variation of Ge/C Content (in $Si_{1-x}Ge_x/Si_{1-y}C_y$) on SiGe/SiC AsymD-*k* Spacer FinFETs based 6T SRAM Cell

As technology scaling the main challenging design constraint of SRAM cell is conflict between read and write SNMs. Many SRAM cells [68][69] have been reported to reduce the read-write conflict at the cost of cell delays. As the proposed device exhibits different current driving capabilities for $V_{DS}>0$ and $V_{DS}<0$ which is already demonstrated in Section 4.3.1. This asymmetricity helps to mitigate the readwrite conflict [63]. Figures 4.20 to 4.22 show the effect of variation of carbon content on hold, read and write SNMs. RSNM is a parameter to measure the read stability of the SRAM cell , which is the side length of the largest square that can be inscribed into the smaller lobe of the butterfly [32].

Write ability of the SRAM cell can be measured in terms of write static noise margin (WSNM). WSNM value is determined with the help of write butterfly curve [32] and defined as the side length of the smallest square inscribed in butterfly curve for the write operation. As the proposed device has lower drain induced barrier lowering (DIBL) that improves the stability of the SRAM cell. Due to

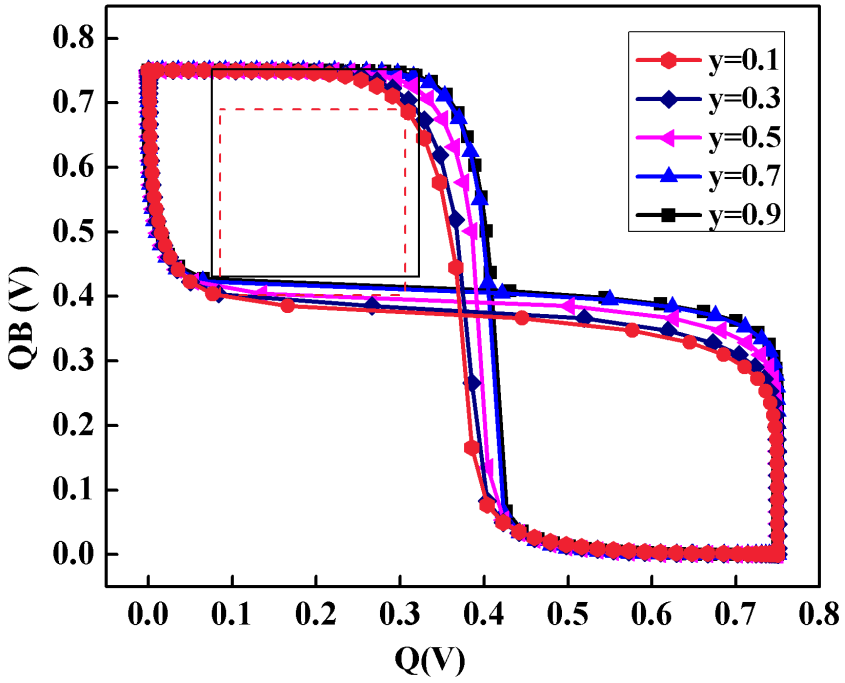


Figure 4.20: Variation in hold SNM of proposed 6T SRAM cell for different values of y in $Si_{1-y}C_y$.

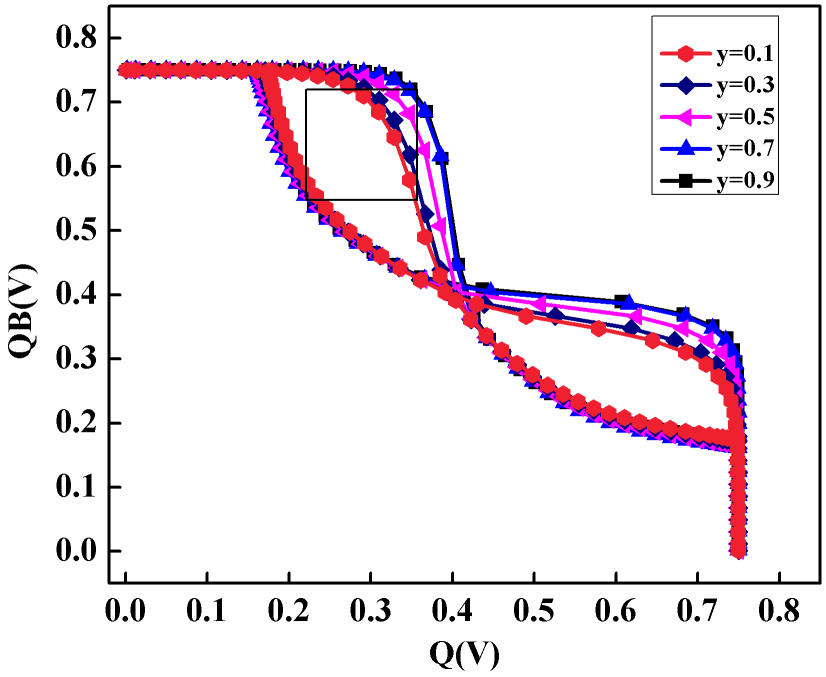


Figure 4.21: Variation in read SNM of proposed 6T SRAM cell for different values of y in $Si_{1-y}C_y$.

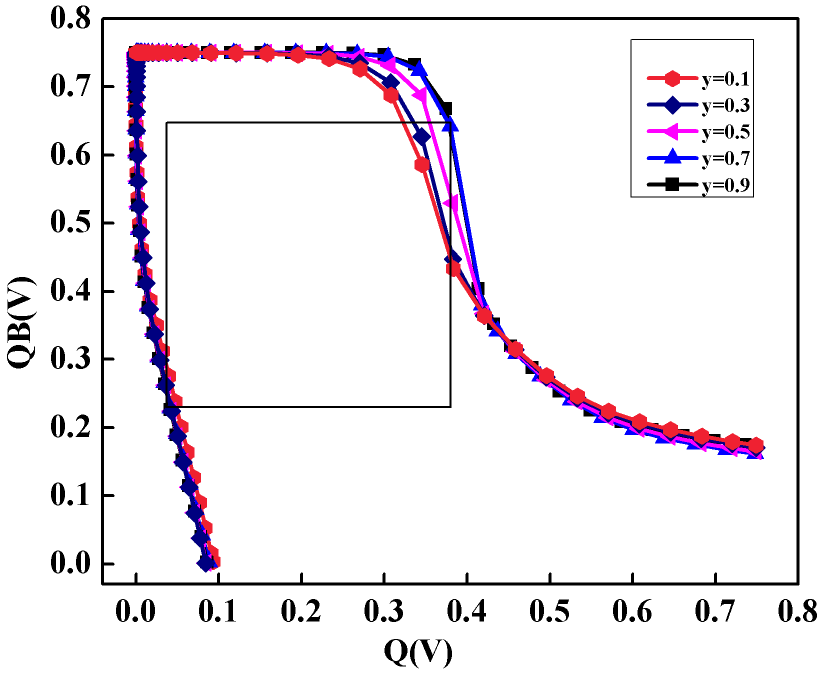


Figure 4.22: Variation in write SNM of proposed 6T SRAM cell for different values of y in $Si_{1-y}C_y$.

the combined effect of strain-induced effects and Asymmetric dual-k, SiC AsymD-k FinFET exhibits higher I_{ON} for higher amount of C mole fraction. As discussed SiC AsymDk FinFET exhibits higher I_{ON} for higher amount of C mole fraction which helps to enhance static noise margin of the 6T SRAM cell.

4.4 Summary

In this chapter, we proposed SiGe/SiC-AsymD-k underlap FinFETs and the applications of these devices in 6T SRAM cell has been analysed using 3D TCAD and mixed mode simulations. The introduced stressors (SiGe/SiC) in S/D regions provide lateral tension and vertical compression in the channel results in boosting of charge carriers (electron/hole) mobility. The introduced dual-k spacer at source side helps to control the SCEs and improves the electrostatic integrity, thus it exhibits the lower off state current. Hence, the combination of enhanced mobility and asymmetric dual-k offers high-current driving capabilities in the proposed device than conventional FinFET. As the proposed device has asymmetric nature with respect to spacers, for positive and negative drain biases, there are unequal currents in the device. This asymmetry results in mitigation of readwrite conflict. SiGe/SiC-AsymD-k 6T SRAM cell exhibits higher read SNM and WM at lower V_{DD} values show its potential.

Chapter 5

SiGe Channel based Asymmetric Dual-k Spacer FinFETs-based 6T SRAM Cell to Mitigate Read-Write Conflict

5.1 Introduction

In the chapter 4, we investigated the device performance of SiGe/SiC-AsymD-k FinFET with Si channel for high performance and robust SRAM cell. The introduced SiC/SiGe in the S/D regions act as stressors to induce lateral tension and vertical compression in the Si channel results in enhancement of electron/hole mobility. In this chapter, we study silicon-germanium (SiGe) channel based asymmetric underlap dual-k spacer Fin-Field Effect Transistor (AsymD-k FinFET) for high performance SRAM cell.

As technology is scaling beyond the 32nm node, silicon channel devices revealed its scaling limit due to severe SCEs, degraded drive current capability and higher leakage current [18, 70, 71, 72]. Application of these devices in memory cell degrades the performance metrics of static random access memory (SRAM). Because of lower SCEs, FinFET[30] has become a promising candidate at lower technology nodes; but beyond sub-30nm nodes SCEs are still exist. Furthermore, the undoped underlap region of FinFET structure helps to achieve lower SCEs with the cost of degraded drive

current (I_{ON})[73]. The propitious route to enhance the drive current is introducing a high permittivity (k) spacer material. This enhancement of drive current is due to the gate-induced fringe field lines [61]. But as k value increases the mobility will be degraded due to enhanced trap charges and it worsens the circuit performance[55]. Strain engineering has attracted much attention of todays industry as it boosts the channel mobility according to the modulation of subband structures[44]. Hence, the auspicious way to improve the performance metrics of SRAM at lower V_{DD} is the introduction of silicon-germanium (SiGe) channel material[74] that ameliorates the channel mobility than the silicon (Si) channel device. As technology advances the important constraint of SRAM cell is conflict between read and write SNMs. This conflict between read and write requirement is an unavoidable design constraint. Here, we prove that the amalgamation of channel mobility enhancement and asymmetric dual-k, offers good improvement in performance metrics of SRAM cell.

Many studies have explored the technology-circuit codesign approach by innovating the novel architectures in the past to improve the performance metrics of the memory cell. But, the improvements in subthreshold characteristics of those structures come at the cost of reduced I_{ON}, which degrades the robustness of the SRAM cell. Goel *et al.*[33] proposed Asymmetric Drain Spacer Extension (ADSE) FinFET that has a gate underlap only on the drain side. Because of its lower SCEs, the application of ADSE FinFETs in 6T SRAM shows possible improvement in read and write stabilities at the cost of increased access time. Moradi *et al.*[63] proposed asymmetrically doped FinFET. This asymmetrical doping introduces unequal currents for positive and negative drain biases, which will be helpful to improve read and write stabilities at the cost of higher access time in 6T SRAM cell. Furthermore, Pal *et al.*[34] have devoted their efforts to improve the performance metrics of the memory cell by incorporating the asymmetrical dual-k (low-k and high-k spacers) at source side. The application of these devices in the memory cell improves the performance metrics. However, this asymmetry helps to mitigate read-write conflict with higher access time. Recently, Pradhan *et al.*[40, 41, 75] proposed dual-k (Symmetric and Asymmetric dual-k hybrid FinFETs, these structures have improved subthreshold characteristics but their current driving capabilities are poor. Therefore, it is necessary to introduce the new channel material to improve the device performance.

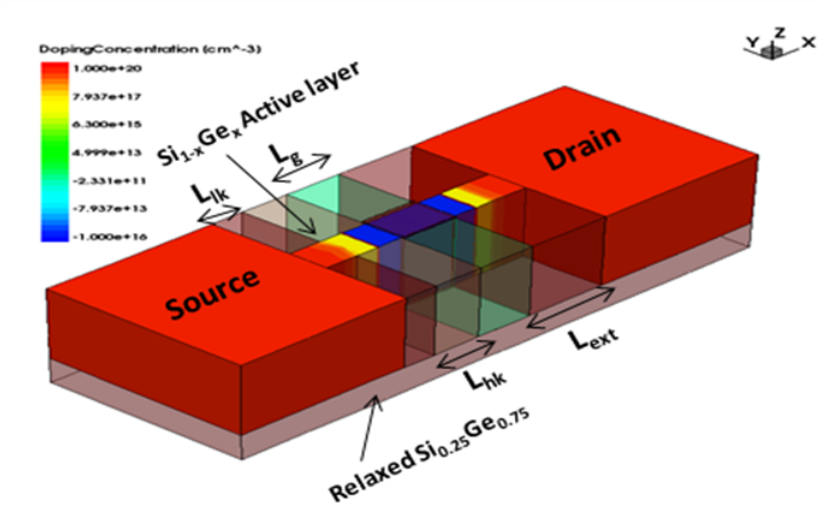


Figure 5.1: 3-D device structure of SiGe AsymD-k underlap FinFET.

For the first time, we investigate the performance metrics of 6T SRAM, based on the proposed FinFETs.

5.2 Device Structure and Simulation Setup

The 3-D structure of the proposed device is shown in Figure 5.1. It is unlike conventional FinFET. In conventional FinFET silicon is used as a channel material, single silicon dioxide is used as a spacer material on both sides where as AsymD-k underlap FinFET has different spacer materials at source side (inner high-k (HfO_2) and outer low-k (SiO_2)) and SiGe is used as a channel material to enhance the mobility. The channel is oriented at <110> as the plane of conductance. Table 3.1 shows the device parameters and electrical properties to satisfy the international technology road map for semiconductors (ITRS) projections. The channel and underlap regions are lightly doped with boron concentration of $10^{16}/cm^3$ and dopant segregation length (DSL) maintained 12nm. Underlap length (L_{un}) is 8nm, work functions of metal gate are tuned to 4.45 eV for n-type and 4.77 eV for p-type to achieve the required threshold voltage. The lengths of inner high-k (L_{hk}) and outer low-k (L_{lk}) are 12 and 8nm, respectively. For design of the device perspective, we considered the $Si_{0.25}Ge_{0.75}$ substrate[76]. The material is like germanium because it has the largest Ge content. As the Ge content becomes larger, it induces a tensile stress in the active layer of $Si_{1-x}Ge_x$ for large range of x values. Device simulations are carried

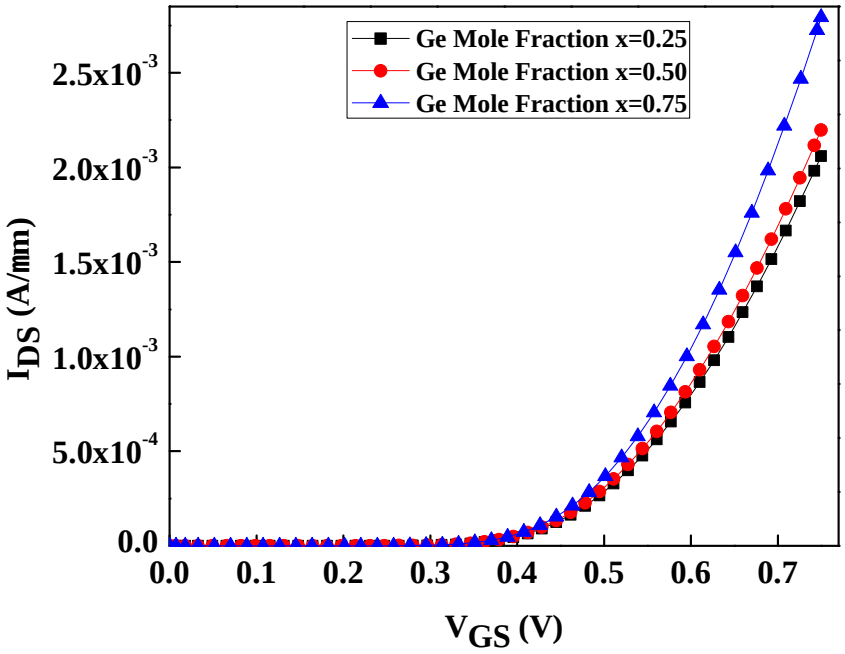


Figure 5.2: Variation in I_{DS} for different values of 'x' in $Si_{1-x}Ge_x$ at V_{DS}=0.75V.

out using 3-D Sentaurus TCAD tool. Sentaurus TCAD mixed device/circuit tool has been used to analyse SRAM performance metrics [48]. The quantum potential, Lombardi mobility, direct tunnelling and the set of transport models were activated.

5.3 Results and Discussion

5.3.1 Electrostatics of SiGe AsymD-*k* Underlap FinFET

The I_{DS} versus V_{GS} characteristics reported in Figure 5.2 for different Ge content in the $Si_{1-x}Ge_x$ for $V_{DS} = 0.75$ V. The effective mass of the electron decreases because of generated longitudinal tension in SiGe channel region, that breaks the symmetry of band structure. Moreover, a redistribution of carrier to low effective mass sub-band valley and reduces inter-band scattering of electrons in the channel caused by the stress along x and z directions. As a result, the electron mobility increases and hence the stress along the channel increased by increasing mole fraction of Ge(x).

In addition to the stressor effect, the introduced high-k spacer at source side increases the electric field coupling between gate and the under lapped regions that reduces source/drain (S/D) series resistance ($R_{S/D}$). So, the combination of channel mobility enhancement and asymmetric dual-k, offers high current drive capabilities

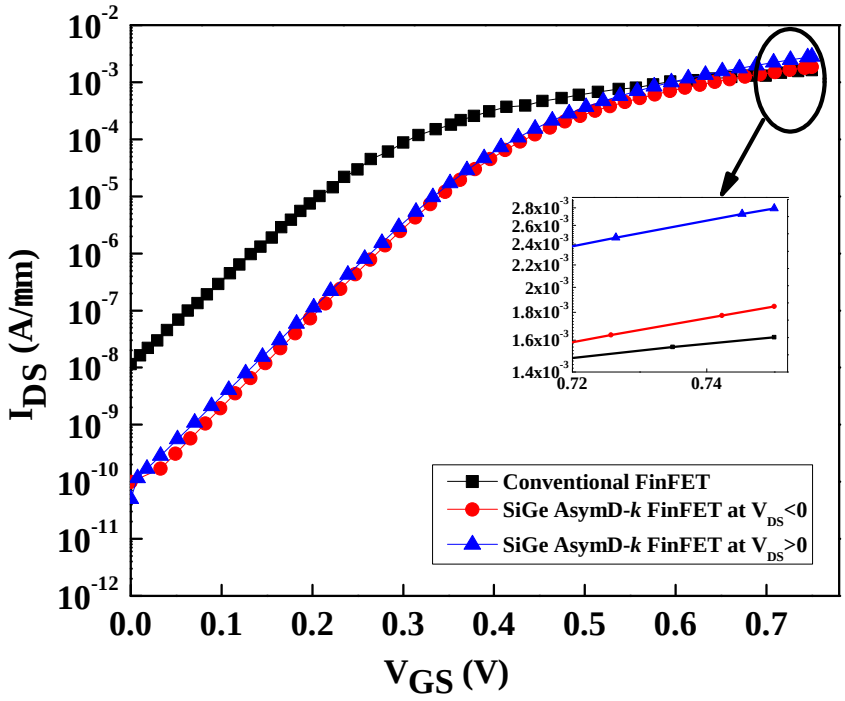


Figure 5.3: Transfer characteristics for conventional FinFET and SiGe AsymD-k FinFET

for the proposed device. For high content of Ge mole fraction the proposed device exhibits higher I_{ON}.

Figure 5.3 shows the transfer characteristics of conventional FinFET and SiGe AsymD-k FinFET. Introducing the dual-k spacer at source side and single spacer at drain side results in asymmetry of the device characteristics by applying the bias on both the terminals. It is perceived that the proposed device with V_{DS}>0 exhibits consistently higher I_{ON} and lower I_{OFF} than V_{DS}<0, which could be more beneficial to enhance the stability of a SRAM cell. Rest of the analysis done among the proposed device structure with V_{DS}>0 and conventional FinFET. The enhancement in I_{ON} due to amalgamation of SiGe channel and asymmetric dual-k. Figure 5.4 shows the numerical comparison of conventional FinFET and SiGe AsymD-k FinFET structures. The proposed structure exhibits 97% improvement in drive current, 50.25% in I_{ON}/ I_{OFF}, with improved SS and DIBL than conventional FinFET.

5.3.2 SiGe AsymD-*k* FinFET Based 6T SRAM Cell

This section explores the simultaneous improvement in read and write SNMs of SiGe AsymD-k based 6T SRAM cell. Figure 5.5 shows the schematic of SiGe AsymD-k

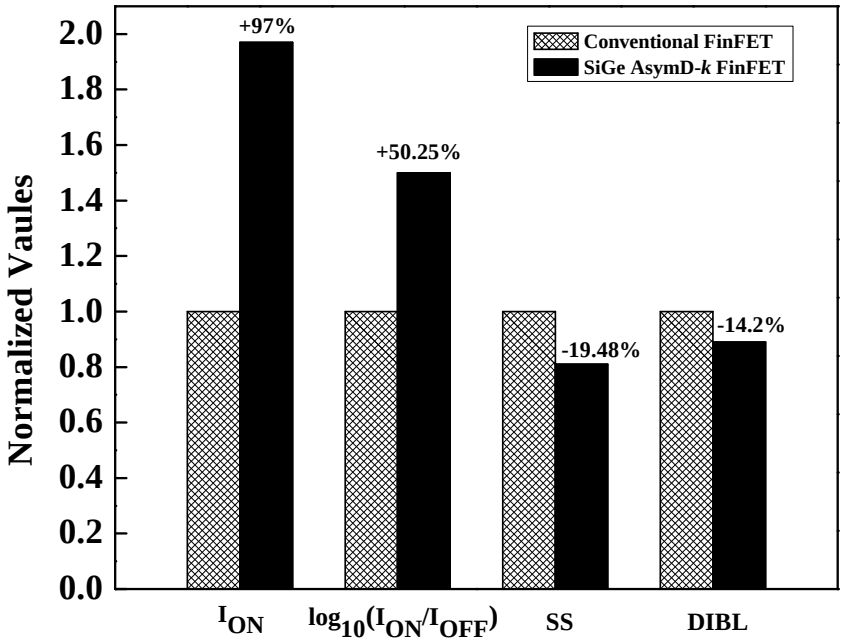


Figure 5.4: Comparison of device characteristics of conventional and SiGe AsymD-k FinFETs.

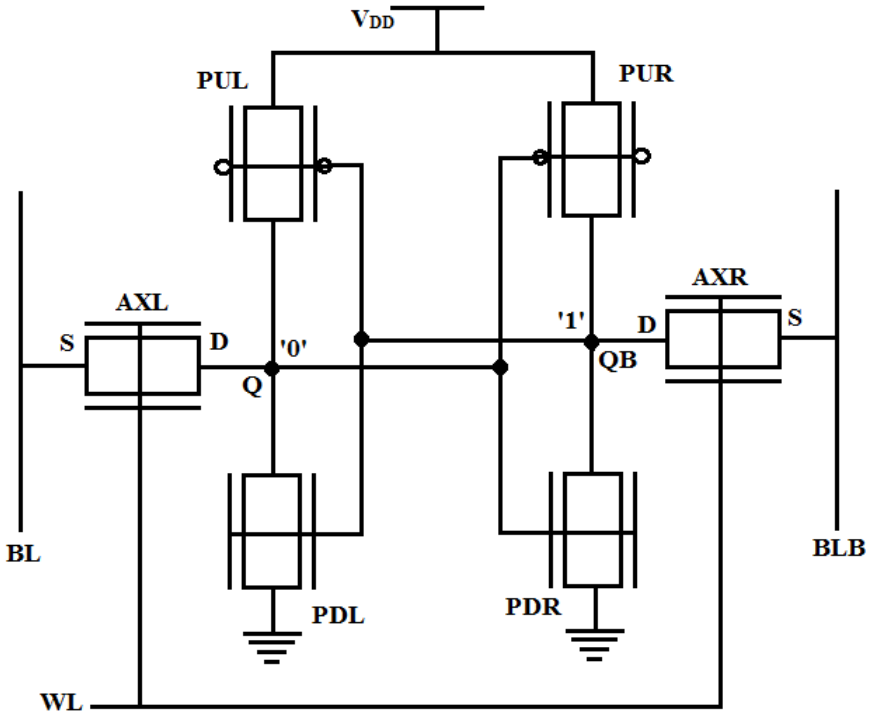


Figure 5.5: Schematic of SiGe AsymD-k based 6T SRAM cell.

based 6T SRAM cell. The device design is governed by the stability of the SRAM cell. The immunity of SRAM cell to static noise is expressed in terms of static noise margin (SNM). During hold mode, word line (WL) is maintained at ground, node Q stores logic '0' and node QB stores complement value of node Q. During the read

operation, both the bit-lines (bit line (BL) and bit line bar (BLB)) are precharged to supply voltage (V_{DD}) and word line is asserted to turn on the access transistors (AXL and AXR). On asserting the WL, the voltage at node Q (V_Q) rises. If V_Q is greater than the trip point of other inverter, it leads to read failure. Hence, for higher read stability weak access transistor is desired. During the write operation BL and BLB are maintained at V_{DD} and GND respectively. The voltage at QB (V_{QB}) is discharged on asserting the WL. If V_{QB} is less than the trip point of other inverter, successful write operation achieved. For higher write ability strong access transistor is desired. This read/write conflict occurs due to the antithetical sizing necessity of access transistors.

To mitigate the read/write conflict, there is prerequisite to use novel device architecture which exhibits the different device characteristics based on the biasing conditions. The proposed device has the different current driving capabilities for $V_{DS}>0$ and $V_{DS}<0$ as shown in Figure 5.3 that helps to mitigate the read/write conflict. SiGe AsymD-k exhibits higher I_{ON} with lower DIBL. However, the stability (read/write) is not directly dependent on the value of I_{ON}[66]. Ostensibly, SNM has a negative correlation with DIBL. As DIBLs of pull up and pull down become larger SNM degrades. By using the proposed device architecture the stability of the

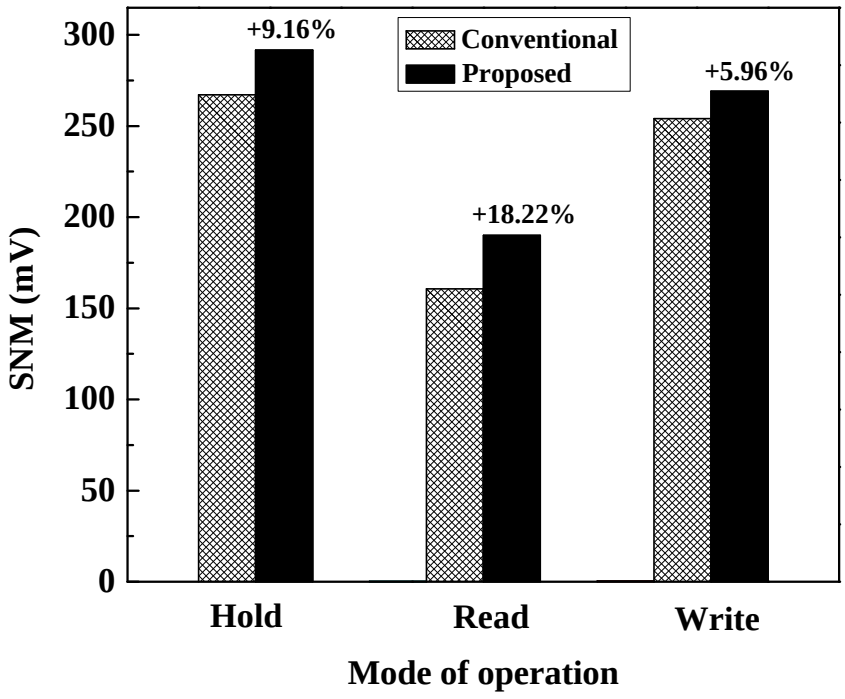


Figure 5.6: Comparison of hold, read and write SNMs.

SRAM is improved significantly. Figure 5.6 shows the SNMs comparisons of proposed SiGe AsymD-k SRAM and conventional FinFET SRAM in all three possible modes. Compared with conventional FinFET SRAM, the proposed SiGe AsymD-k FinFET based SRAM achieved the hold, read and write margin improvement by 9.16%, 18.22% and 5.96% respectively.

5.3.3 Effect of Range of V_{DD}'s on SiGe AsymD-k SRAM

One of the effective ways to reduce the leakage is lowering the supply voltage. Lowering the supply voltage reduces the noise immunity. Figures 5.7 to 5.9 shows the effect of lowering the supply voltage on hold, read and write SNMs respectively. The

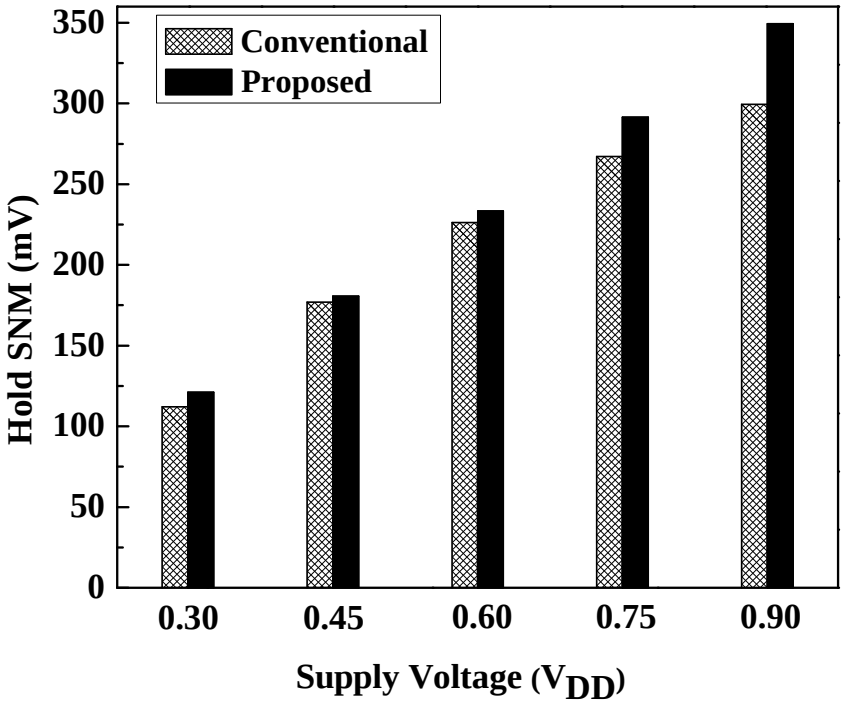


Figure 5.7: Comparison of hold SNM with supply voltage scaling.

proposed SiGe AsymD-k SRAM exhibits good improvement in hold, read and write SNMs over a range of supply voltage. From Figures 5.7 to 5.9 as supply voltage scaled down, SNM is reduced in all three possible modes (hold, read and write) due to increased resistance at source side.

Figure 5.10 shows the simultaneous improvement in read and write SNMs of proposed SiGe AsymD-k FinFET SRAM. The access time in read and write mode is another important performance metric of SRAM cell, which depends on the relative

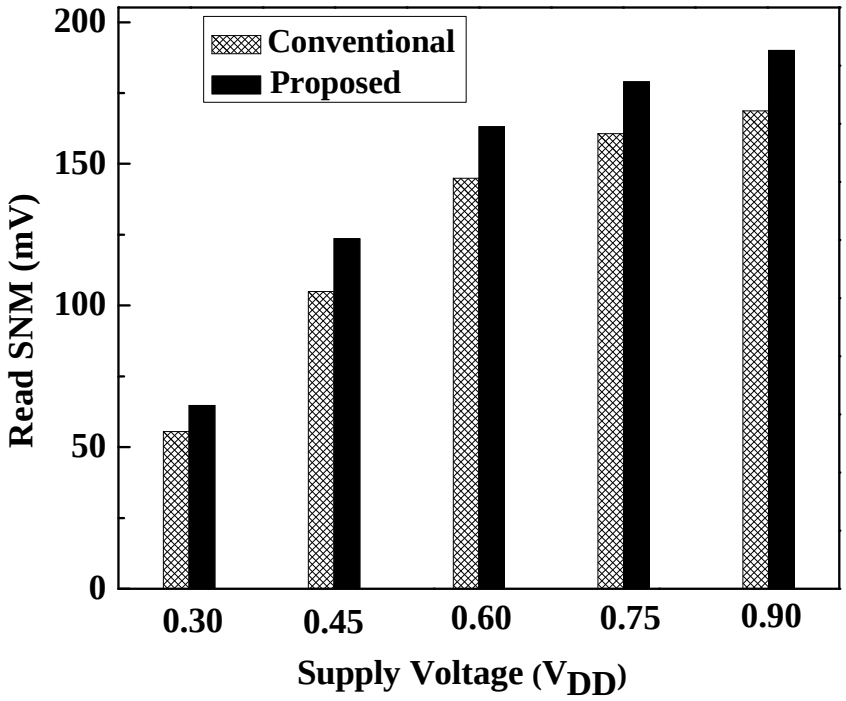


Figure 5.8: Comparison of read SNM with supply voltage scaling.

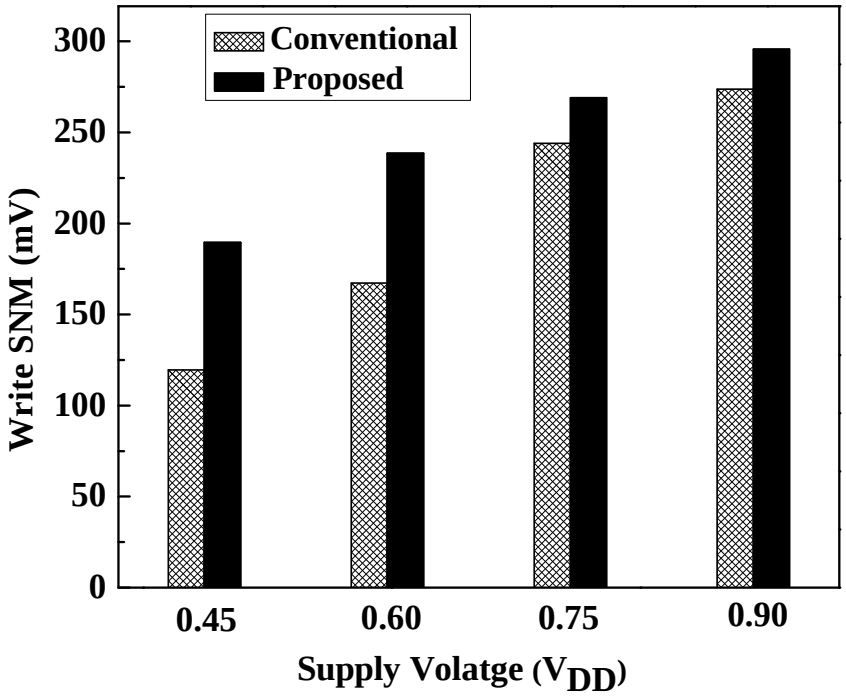


Figure 5.9: Comparison of write SNM with supply voltage scaling.

strengths of the access transistors. Figure 5.11 shows the numerical comparison of conventional and SiGe AsymD-k FinFET SRAM in terms of read and write access time. Compared with the conventional FinFET SRAM, proposed SiGe AsymD-k FinFET SRAM achieved 48.6% and 32.4% reductions in read and write access

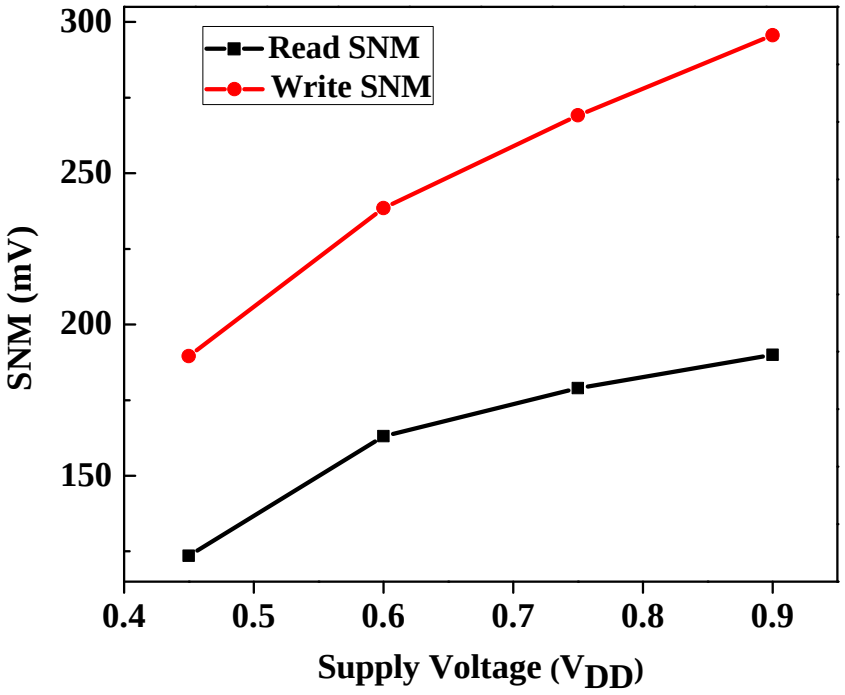


Figure 5.10: Simultaneous improvement in read and write SMNs of proposed SiGe AsymD-k FinFET SRAM.

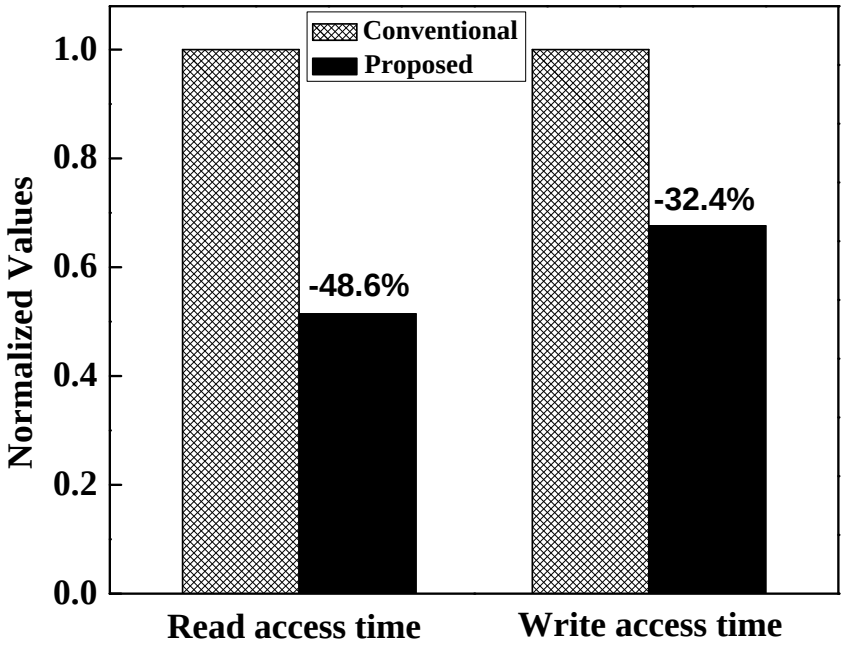


Figure 5.11: Comparison of read/write access time among conventional and SiGe AsymD-k FinFET based SRAM cell.

times respectively due to weak access transistor during read mode and stronger access transistor during write mode.

5.4 Summary

In this chapter, we studied the impact of SiGe channel material on asymmetric dual-k spacer FinFET device and 6T SRAM circuit performance using 3-D TCAD and mixed mode simulations. The combination of improved channel mobility and asymmetric dual-k offers high current driving capabilities in the proposed device than conventional FinFET. We shown that SiGe AsymD-k FinFET has lower short channel characteristics viz., reduced DIBL, improved SS and lower I_{OFF}. For positive and negative drain biases, there are unequal currents in the device because of its asymmetric dual-k spacers at the source. This asymmetry results in mitigation of read-write conflict, as a result the proposed SiGe AsymD-k FinFET SRAM yields simultaneous improvement in read stability, write ability and access time.

Chapter 6

Conclusions and Future Works

6.1 Conclusions

In this thesis, all the proposed device architectures are designed using 14nm FinFET technology. All the simulations has been carried out using 3D TCAD and mixed mode simulations.

The effect of asymmetric doping on AsymD-k FinFET has been analyzed. The SCEs are occurring because of influence of drain electric fields on the channel region. To reduce the influence of drain electric fields, drain is lightly doped than source terminal that results in wider depletion region and it also reduces the I_{OFF}. Introduced high-k at source side enhances the gate-fringe-induced-barrier lowering that reduces the S/D resistance. As a result the proposed device exhibits high I_{ON}/I_{OFF}. However, as 'k'value increases the mobility will be degraded due to enhanced trap charges and it worsens the circuit performance. Further, to improve the channel mobility strain engineering has been introduced.

Additionally, this thesis also investigate the device performance of SiGe/SiC source/drain AsymD-k spacer FinFET with Si channel. The introduced stressors (SiGe/SiC) in S/D regions provide lateral tension and vertical compression in the channel results in boosting of charge carriers (electron/hole) mobility. The introduced dual-k spacer at source side helps to control the SCEs and improves the electrostatic integrity, thus it exhibits the I_{OFF}. Hence, the combination of enhanced mobility and asymmetric dual-k offers high-current driving capabilities in the proposed device than conventional FinFET. As the proposed device has asym-

metric nature with respect to spacers, for positive and negative drain biases, there are unequal currents in the device. This asymmetry results in mitigation of read-write conflict. SiGe/SiC-AsymD-k 6T SRAM cell exhibits higher read SNM and WM at lower V_{DD} values show its potential.

Furthermore, this thesis reports the impact of SiGe channel material on asymmetric dual-k spacer FinFET device. The combination of improved channel mobility and asymmetric dual-k offers high current driving capabilities in the proposed device than conventional FinFET. The utilization of proposed device in 6T SRAM cell yields simultaneous improvement in read stability, write ability and access time.

6.2 Future Works

The research vision of this thesis is to design robust 6T SRAM cell. To reduce the read-write conflict, a novel device architecture has been investigated. As the proposed device uses SiGe/SiC in the S/D regions, it is essential to examine the effect of heavy ion irradiation in the proposed device from reliability prospective for inclusion in digital circuit applications. A detailed reliability analysis can be done for the proposed device. Further, due to relentless down scaling of transistor, process variation effects will be tediously increased. As a result to operate the digital circuits with required small voltage in presence of huge process variations i.e. random dopant fluctuation is an interesting challenge. The analytical model can be developed for the proposed device to validate the simulation results. This thesis deals with only one 6T SRAM cell, extending this research work to memory array level is a part of the research plan for future.

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Appendix

A Simulation Tool

Simulations are required to optimize the device performance when hands on calculation and fabrication methods become too complicated or impose unacceptable assumptions. Sentaurus TCAD tool from Synopsys is an advanced commercial computational environment with a collection of tools which is used for performing simulations of electronic devices and to understand advanced-device physics. It also helps to investigate scaling analyses of device and may provide different design rules. In addition, it also allows us to interact with the fabrication methodology using process manufacturing. Importantly, with a Sentaurus TCAD, the device behavior is obtained from the solution of the appropriate differential equations describing the device physics on a given geometrical domain. Here, the physics of the considered device is obtained from different models already available with the tool. After including the appropriate models, the considered device can be ramped with necessary electrical stimulation to get the final results.

Furthermore, Synopsys Sentaurus TCAD provides two methods for the device design :

- **Device TCAD** : It deals with the modeling of electrical, thermal, optical and mechanical behavior of semiconductor devices.

- **Process TCAD** : It aims to the modeling of semiconductor-chip process-manufacturing steps like lithography, deposition, etching, ion implantation, diffusion, oxidation, silicidation, mechanical stress, etc..

In this thesis, simulations are carried out using 3-D Sentaurus TCAD mixed device/circuit tool. Further, different steps for Sentaurus simulations with device TCAD are given in Figure A.

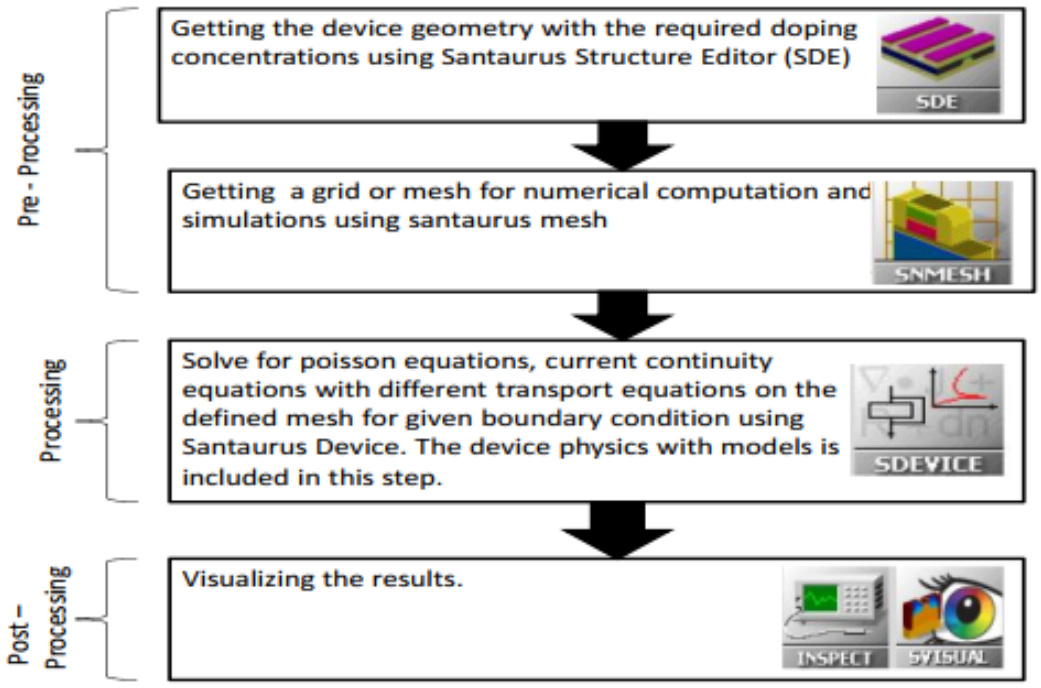

Figure A: Device simulation steps with Synopsys Sentaurus Device TCAD [48].

A.1 Sentaurus Device

The description of different tools used for simulation with device TCAD can be given as follows:

Sentaurus Structure Editor (SSE) : Sentaurus Structure Editor can be used as a two-dimensional (2D) or three-dimensional (3D) structure editor. Here, the required structures are generated or edited interactively using the graphical user interface (GUI). Doping profiles strategies for different regions of the considered device can also be defined with structure editor tool. In addition, Sentaurus Structure Editor provides an interface to call the Synopsys meshing tool i.e. Sentaurus Mesh to generate required grid points. Importantly, it provides the necessary input files (the .tdr boundary file and mesh command file) for the meshing tool and provide the way for the device simulation using Sentaurus Device.

Sentarus Mesh (SNMESH) : Sentaurus Mesh is a mesh generator that produces rectangular or hexahedral elements for use in applications such as semiconductor device simulation, process simulation and electromagnetic simulation. The points

where these elements intersects each other are known as the grid points. The physical equations of the considered device are solved corresponding to these grid points only. The mesh generation tools is composed of two mesh generators:

1. Sentarus Mesh: Sentaurus Mesh is a robust mesh generator capable of producing axis-aligned meshes or grid points in 2D and 3D. In the 2D MOS type of devices, Sentaurus Mesh works is recommended. Importantly, the simulated devices where the most important surfaces are the axis aligned surfaces, sentaurus mesh is used. Although Sentaurus Mesh works very well with MOS type devices, the effective and optimized numerical meshes in which the problem can be solved assuring convergence, and at the same time, with the reasonable simulation times, is a difficult to obtain. However, some general rules can be applied:

A. The grid spacing must be sufficiently dense so that all the relevant features of the geometry are accurately represented. However, it will increase the grid points and consequently the simulation time. Therefore, it is recommended that to create the most suitable mesh, the mesh must be densest in those regions of the device where High current density, High electric fields and High charge generation event occurs.

B. Points must be allocated to accurately approximate the physical quantities of interest.

2. Noffset3D: Noffset3D is an advancing front mesh generator, capable of producing triangular meshes in 2D and tetrahedral meshes in 3D. For devices where the main surfaces are nonaxis-aligned or curved, the recommendation is to use Noffset3D. The meshes produced by Noffset3D can contain layers of elements that are nearly parallel to given surfaces of a semiconductor device structure. The Noffset3D uses a series of algorithms to generate the final meshing. The main algorithm contains of layer generation, surface refinement and doping interpolation. Importantly, the overall computation time depends on the total number of grid points during meshing, therefore grid point number must be minimized for computational efficiency.

Sentarus Device (SDEVICE) : Sentaurus Device simulates numerically the electrical behavior of a semiconductor device in isolation or several physical devices combined in a circuit. The terminal currents, voltages, and charges are computed based on a set of physical device equations that describes the carrier distribution and conduction mechanisms. A real semiconductor device, such as a transistor, is represented in the simulator as a virtual device whose physical properties are discretized onto a nonuniform grid points. Therefore, a virtual device is an approximation of a real device in Sentarus TCAD. For this purpose, the poisson equation with electron and hole continuity equation are solved using newton iteration method for the whole range of electric stimulation with different physical models.

The SDEVICE has extensive set of models of physics for semiconductor devices, general support for different device geometries and mixed-mode support of electrothermal net lists with mesh-based device models and SPICE circuit models. Importantly, in SDEVICE, continuous properties such as doping profiles are represented on the mesh and therefore, are only defined at a finite number of points. The doping at any point between these grid points (or any physical quantity calculated by SDEVICE) can be obtained by interpolation.

The Sentaurus Device command file can be organized in commands or sections that can be in any order. Also, Sentaurus Device keywords are not case sensitive. A Sentaurus Device command file has following sections :

1. File Section: File section consists "input files" that define the device structure i.e. .tdr file along with parameter .par file. In addition, the "output files "such as .plt, .log file are also defined in the file section for the simulation.

2. Electrode Section: With Sentaurus Device, it is necessary to specify which of the contacts are to be treated as electrodes. Electrodes in Sentaurus Device are defined by electrical boundary conditions and contain no mesh. Any contacts that are not defined as electrodes are ignored by Sentaurus Device.

3. Physics Section: The physics section of sentaurus command file allows a selection of the physical models to be applied in the considered device simulation.

The selection of physical model strongly influences the accuracy of the simulation result. The physical models used are explained in detail later in this thesis.

4. Plot Section: The Plot section specifies all of the solution variables that are to be saved in the output plot files (.tdr). Only data that Sentaurus Device is able to compute, based on the selected physics models, is saved to a plot file.

5. Math Section: Sentaurus Device solves the device equations (which are essentially a set of partial differential equations) self-consistently, on the discrete mesh, in an iterative fashion. For each iteration, an error is calculated and Sentaurus Device attempts to converge on a solution that has an acceptably small error. For this purpose, one need to define a few settings for the numeric solver in Math section.

6. Solve Section: The Solve section defines a sequence of solutions to be obtained by the solver. The Quasistationary command is used to ramp a device from one solution to another through the modification of its boundary conditions or parameter values in the solve section.

Sentaurus Visual (SVISUAL) :

It is a plotting software for visualizing data output from simulations. Sentaurus Visual enables users to work interactively with data using both a graphical user interface and a scripting language for automated tasks.

A.2 Simulation Methods

In device TCAD, following methods are available for electrical simulations of the device.

Steady State Simulations: In steady-state conditions, for each property of the systems, its partial derivative with respect to time is zero, i.e. , nothing is changing with time. To perform steady-state simulations, the Sentaurus TCAD keyword is Quasistationary. The Quasistationary command is used to ramp a device from a

solution to another through the modification of the boundary conditions that can be Voltage, Current, or Temperature.

Transient Simulation: A transient response or natural response is the time-varying response of a system to a change from equilibrium. In Sentaurus, the keyword that must be used to perform transient simulation is "Transient". The command must start with a device that has already been solved under stationary conditions. The simulation then proceeds by iterating between incrementing time and re-solving the device.

AC simulations: Performing a small signal or AC analysis means simulate the behavior of system when a relatively small harmonic signal is superimposed to a steady-state condition or DC bias point. The keyword for AC analysis in Sentaurus SDEVICE is AC coupled

A.3 Physical Models

Synopsys Sentaurus TCAD tool offers an extensive set of models to represent the virtual device as an approximation of the actual device. These models are included in the SDEVICE script for the considered device simulation. Some of the important models are listed as follows :

Carrier Transport Model: All the carrier transport model supported by Sentaurus TCAD follows the charge conservation law in active region of the considered device. Here, carrier concentrations in any region of the device must never be negative during the newton iteration. If during a Newton iteration a concentration erroneously becomes negative, the tool provides the message that the newton is not able to converge. After this, SDEVICE applies damping procedures (i.e. using the smaller step size) to make it positive. If the newton iteration converges for the whole range of electrical stimulation, simulation gets complete. Here, following model for carrier transport is used in Sentaurus TCAD:

1. Drift Diffusion: The drift diffusion model is very important for the semiconductor device simulation with Sentaurus Device. This model is used for isothermal simulation and is suitable for low-power density devices with long active regions. Also, the drift-diffusion model is the default carrier transport model in Sentaurus Device. The drift diffusion equation mainly consist the poissons equation, the electron and hole current equation and the electron and hole current continuity equation. Therefore, with drift-diffusion model, current densities of electron and holes can be as follows:

$$J_n = \mu_n(n\nabla\ E_c\text{-}1.5nk\text{T}\ln(m_n))+D_n(\nabla n\text{-}n\nabla\ \ln(\gamma_n))$$

$$J_p = \mu_p(p\nabla\ E_v\text{-}1.5pk\text{T}\ln(m_p))+D_p(\nabla p\text{-}p\nabla\ \ln(\gamma_p))$$

Here, the first term of the above two equations comes the spatial variations of the electrostatic potential, the electron affinity, and the band gap. The remaining terms take into account the contribution due to the gradient of concentration, and the spatial variation of the effective masses m_n and mp. Also, the diffusion constants i.e D_n and D_p are calculated using Einstein relation.

To activate drift diffusion model, keywords Electron and Hole is used in the solve section of Sentarus Device command file with poisson equation. Further, in this thesis, only drift diffusion model is used for the carrier transport of the charge carrier because the simulation of the considered have been obtained for room temperature.

2. Thermodynamics : This model accounts for self-heating of the active area. It is suitable for devices with low thermal exchange, particularly, high-power density devices with long active regions. The model differs from drift-diffusion when the lattice temperature equation is solved. However, It is possible to use the drift-diffusion model together with a lattice temperature equation, but it is not mandatory. To activate the thermodynamic model, specify the Thermodynamic keyword in the physics section of the Sentarus Device command file.

3. Hydrodynamic : It accounts for energy transport of the carriers and is suitable for devices with small active regions. Simlar to the drift-diffusion model, the hole and electron current densities in hydrodynamic model takes into account the contribution due to the spatial variations of electrostatic potential, electron affinity, the band gap, the contribution due to the gradient of concentration, the carrier

temperature gradients, and the spatial variation of the effective masses. Along with this, the thermal diffusion constants are used with electron and hole to encounter the carrier temperature. To activate the hydrodynamic model, the keyword *Hydrodynamic* must be specified in the physics section. If only one carrier temperature equation is to be solved, *Hydrodynamic* must be specified with an option, either *Hydrodynamic(eTemperature) or Hydrodynamic(hTemperature).*

Generation Recombination Model: The drift diffusion model is used to calculate the electrostatic potential and electron/hole concentration. Apart from that the generation recombination processes are the methods that exchange carriers between the conduction band and the valence band. For each individual generation or recombination process, the electrons and holes involved appear or vanish at the same location. Following generation recombination models are used in this thesis:

1. Shockley Read Hall (SRH): In general, recombination of charge carrier through deep defect levels in the gap is depicted as ShockleyReadHall recombination. Net recombination with SRH is dependent on the energy difference between defect level and intrinsic level, the carrier lifetime for electrons and holes, intrinsic concentration and electron/hole charge carrier density in the considered device. Hence, SRH model takes many important features of the simulated device into consideration. In addition, the electron and hole concentration with SRH is doping dependent, field dependent, and temperature dependent.Therefore, the SRH can be made to handle variability accounted from doping, electric field and temperature variation also.

The generationrecombination model can be selected in the physics section of Sentaurus Device command file as an argument to the *Recombination* keyword i.e. Physics f(Recombination(SRH (dopingdependence..)...)).

2. Poole Frenkel: The PooleFrenkel model used for the interpretation of transport effects in dielectrics and amorphous films. The model predicts an enhanced emission probability for trap where the potential barrier is decreased because of the high external electric field. The model is selected by the *PooleFrenkel* keyword in the command file.

Mobility Model: Sentaurus Device uses a very modular approach for the explanation of the carrier mobilities in the Sentarus Device command file. For the simplest case, a constant mobility model is used with the undoped materials. For doped materials, the carriers scatter with the impurities and this leads to the degradation of the mobility. To justify this effect, following mobility model can be used with doped materials:

1. Doping Dependent Mobility Degradation: In doped semiconductors, the scattering of charge carriers by impurity ions leads to the degradation of the carrier mobility. The model to justify this mobility degradation due to impurity scattering are activated by specifying the *DopingDependence* flag to Mobility in the physics section of Sentarus Device command file i.e. *Physics(Mobility(DopingDependence ...)).*

If DopingDependence is specified without options, Sentaurus Device uses a material dependent default model. In silicon material, the default doping dependent mobility model is the Masetti model where the mobility is given by the following equation:

$$\mu_{dop} = \mu_{min1} exp\left(\frac{-P_C}{N_{A,0}+N_{D,0}}\right) + \frac{\mu_{min2}\mu_{const}}{1+((N_{A,0}+N_{D,0})/C_r)^{\alpha}} - \frac{\mu_1}{1+\left(\frac{C_s}{N_{A,0}+N_{D,0}}\right)^{\beta}}$$

Here, the mobilities μ_{min1}, μ_{min2}, and μ_1 are the reference mobilities which along with doping concentrations P_C, C_r, and C_s, and the exponents α , β are accessible in the parameter set *DopingDependence* in parameter file.

2. Enhanced Lombardi Model with High-*k* Degradation: High-k gate dielectrics are being considered as an alternative to SiO_2 to reduce unacceptable leakage currents as transistor dimensions become smaller. One obstacle when using high-k gate dielectrics is that a degraded carrier mobility is often observed for such devices. Although the causes of high-k mobility degradation are not completely understood, two possible contributors are remote Coulomb scattering (RCS) and remote phonon scattering (RPS). The enhanced Lombardi model with high-k degradation can be selected by specifying the parameter *Lombardi-highk* in the command file.

3. Philips Unified Mobility Model: The Philips unified mobility model considers mobility degradation due to both impurity scattering and carriercarrier

scattering mechanisms.

The Philips unified mobility model is activated by specifying the *PhuMob* option to Mobility:

Physics Mobility(PhuMob ...) ...

The keyword *PhuMob* must not be combined with the keyword *DopingDependence* or *CarrierCarrierScattering*. If a combination of these keywords is specified, Sentaurus Device uses only the Philips unified mobility model by default.

A.4 Mixed-Mode Sentaurus Device

Sentaurus device helps to simulate a single-device, also performs mixed-mode and circuit simulations. The command file of multiple device simulation composed of

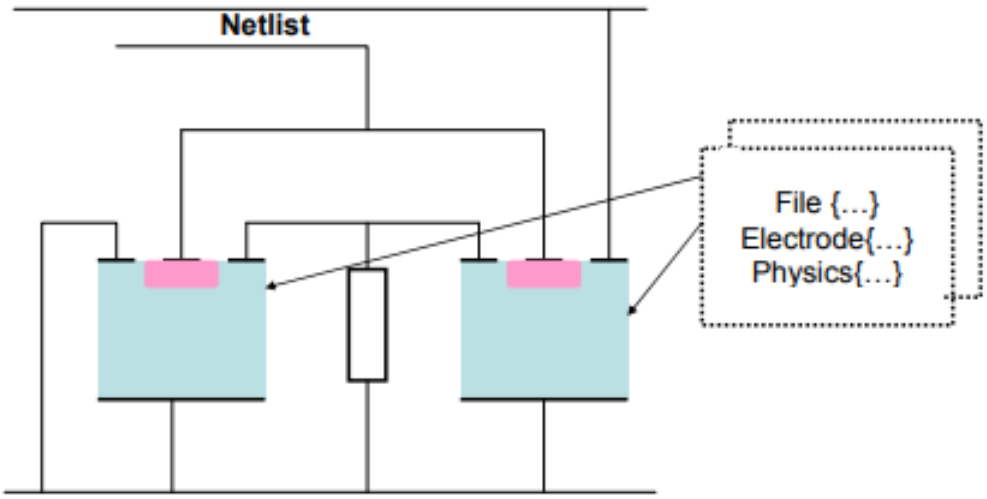

Figure B: Multidevice simulation: Each device is connected with a circuit netlist.

the mesh (File section), contacts (Electrode and Thermal sections), and physical models (Physics section) for each device. Device section consists of all the devices present in the circuit. As shown in Figure B, under command file, the circuit netlist must be defined to connect each device. To create and connect devices, the system section is needed. The solve commands must be specified to solve the whole system of the devices. System section uses SPICE syntax. It defines the netlists of physical devices and circuit elements to be solved. The netlist is connected through circuit nodes.

List of Publications

List of publications included in the thesis

Journal papers:

1. **Maisagalla Gopal**, Vishal Sharma and Santosh Kumar Vishvakarma, "Evaluation of Static Noise Margin (SNM) of 6T SRAM Cell using SiGe/SiC Asymmetric Dual-k Spacer FinFETs," *IET Micro & Nano Letters*, vol. 12, Issue 12, pp. 1028–1032, Dec 2017.

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