FEASIBILITY ASSESSMENT OF STEEP SWITCHING IN SILICON AND GERMANIUM JUNCTIONLESS TRANSISTORS

Synopsis of the thesis
submitted in partial fulfilment of the
requirements for the award of the degree

of

DOCTOR OF PHILOSOPHY

by

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NOVEMBER 2018

1. INTRODUCTION

Moore's law in conjunction with Dennard's scaling theory has enabled the semiconductor industry to significantly improve the performance of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) by enhancing the functionality per unit area [1]. In general, the logic operation of a transistor is characterized by switching from off-to-on state, with the transition from one logic state to another is characterized by a parameter known as Subthrehold swing (*S*-swing), which describes the rate of change of drain current with respect to gate bias and is equal to the thermal limit ~$(kT/q)\ln(10)$, where k is the Boltzmann constant, T is the temperature, and q is the electronic charge [2]. The conventional minimum value of *S*-swing is limited to 60 mV/decade at room temperature, thereby implying a minimum of 60 mV should be applied at the gate to increase the drain current by a decade. Since downscaling of transistor is aimed to densely arrange more number of devices per unit area, the consequential increase in the static power dissipation due to non-scalability of the supply voltage and *S*-swing below 60 mV/decade [2] limits the performance of MOSFETs. Hence, transistors which exhibit *S*-swing lower than 60 mV/decade are highly desirable.

Transistors capable of demonstrating steep switching i.e. achieving *S*-swing lower than 60 mV/decade can operate on different mechanisms such as negative capacitance due to a ferroelectric dielectric [3], and also due to feedback [4], tunneling [2] and Impact Ionization (II) [5] phenomenon. Although, MOSFETs with ferroelectric gate dielectric have shown the potential to achieve low *S*-swing (~ 1 mV/decade), material optimization and its integration with the present technology are critical issues that impede a viable solution [6]. While feedback Field Effect Transistors (FETs) have also shown the potential to achieve steep current transition, a reduction in supply voltage significantly degrades the on-state current and *S*-swing [7]. Tunneling based FETs have been optimized to achieve *S*-swing < 60 mV/decade [2]. However, the main limitations are the precise control of the doping profile at the tunneling junction [2], presence of traps which degrades the switching at lower current values [8] and gate-to-source overlap capacitance. Impact Ionization based devices usually need higher voltages to generate electron-hole pairs that result in Floating Body Effects (FBEs) to initiate a positive feedback loop to achieve ideal *S*-swing values [5]. The requirement of higher applied bias (~ 3 V) in conventional inversion mode devices does not make II conducive for downscaling [5].

With the advent of Junctionless (JL) transistors [9], the need for fabricating an ultra-sharp *pn* junction in the nanoscale regime can be eliminated while ensuring low off-current. JL devices also exhibit enhanced immunity towards short channel effects and are considered to be promising candidates for downscaling into the nanometer regime [9]. An important attribute of JL transistor is the occurrence of an enhanced degree of II induced FBEs to achieve a steep *S*-swing ~1 mV/decade at a relatively lower supply voltage than that required for a conventional inversion mode MOSFET [10]. The reason for the same is the higher current density and the wider area over which II occurs [11]. While previously reported results [10-11] for JL devices are promising and have paved a path forward to achieve *S*-swing ~1 mV/decade, the voltages needed to trigger II are not practical for logic applications in emerging technologies. Therefore, the research has been carried out in the thesis to provide physical insights for better understanding and optimization to facilitate steep switching in Si and Ge JL devices through the means of comprehensive physical device simulations [12], which are well calibrated with published results. The research is aimed to highlight transistor architectures that facilitate downscaling of applied voltages while preserving the effectiveness of II to trigger steep switching in JL transistors.

2. SUMMARY OF RESEARCH WORK

The key contribution of the research work is to provide insights into the understanding of physical phenomenon occurring in the transistor to enhance the steep current transition from off-state (low current) to on-state (high current) for a smaller gate bias interval. In order to achieve steep current transition, the basic mechanism triggering II in a MOSFET is re-examined with particular emphasis on unique attribute of JL transistor. The research has shown that II is governed by the product of current density (J) and ionization coefficients for electrons (α_n) and holes (α_p), which in turn depend on the lateral electric field (E). Hence, the product of current density and electric field i.e. $J.E$, estimating the total power generated per unit volume, acts as a pragmatic parameter to assess the effectiveness of II of an architecture to yield *S*-swing values lower than 60 mV/decade at room temperature. In order to improve the performance of JL devices, an understanding of various factors contributing to enhance the current density, and thus, impact ionization is indispensable, and the same has been extensively investigated in the work.

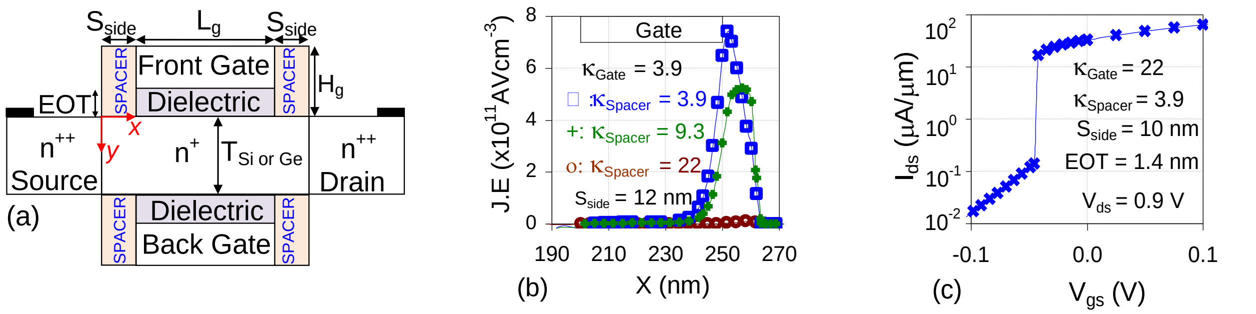

Figure 1: (a) Schematic diagram of a Double Gate (DG) JL transistor, (b) Drain current (I_{ds}) – gate voltage (V_{gs}) characteristics of JL transistor with varying spacer dielectric from 3.9 (SiO_2) to 22 (HfO_2), and (c) $I_{ds} - V_{gs}$ characteristics of an optimized JL transistor at a drain bias (V_{ds}) of 0.9 V. Parameters: Film thickness (T_{si}) = 10 nm, doping (N_d) = 10^{19} cm^{-3}, Equivalent Oxide Thickness (EOT) = 1.4 nm, sidewall spacer width (S_{side}) = 10 nm and gate length (L_g) = 50 nm.

I. Steep Switching Si and Ge Junctionless Transistor

*(a) **Significance of sidewall spacer***

As the relevance of sidewall spacer and high-κ gate dielectric has become significant in nanoscale MOSFETs, the same can be utilized to modulate current density (J) and electric field (E) to affect II, and hence, steep switching. In a Double Gate (DG) JL transistor, shown in Fig. 1*a*, the sidewall spacer significantly influences lateral extension of depletion region beyond the gate edge and governs the effective channel length (L_{eff}) in subthreshold region. A high-κ (HfO_2) spacer allows for a greater penetration of fringing fields into the semiconductor film and supports the extension of depletion beyond the gate edge as compared to that achieved in a spacer designed with SiO_2 leading to a shorter L_{eff} for SiO_2 spacer as compared to that achieved for HfO_2 spacer. The longer L_{eff} indicates a lower electron concentration and a reduced current density which further diminishes the magnitude of II due to the lowering of $J.E$ (Fig. 1*b*). Fig. 1*c* shows that an optimized JL device designed with a combination of low-κ spacer (S_{side} = 10 nm) and high-κ gate dielectric can achieve a steep rise in drain current.

*(b) **Intentional back gate misalignment***

While the optimization of sidewall spacer and gate dielectric does provide an opportunity to achieve II induced sharp rise in drain current, the number of decades of steep current transition at gate bias corresponding to the threshold voltage (V_{th}) is limited to a maximum of two. To increase the number of decades of current transition at threshold, back gate is engineered towards the drain by misaligning it with respect to front gate towards the region uncovered by the front gate as shown in Fig. 2*a*. The misalignment between the front and back gate can be implemented in practical devices through intentional shifting the electrical vernier [13]. The electric field redistribution in proposed JL topology facilitates movement of carriers in lateral as well as vertical direction, and thus, leads to an inclined conduction channel, as shown in the contour plot (Fig. 2*b*), to further augment II through an increase in current density. Misalignment governed conduction channel location is unique to a misaligned topology as the channel usually exists at centre of the semiconductor film in JL transistors [9-10]. The resulting increase in current density due to reduced depletion contributes towards aiding II, and is reflected in a very sharp transition in drain current with a nearly ideal *S*-swing ~1 mV/decade. The work showcases new viewpoints of transforming gate misalignment, traditionally considered detrimental feature into a unique opportunity, to lower the supply voltage to bandgap equivalent i.e. 0.9 V for Silicon and ~ 0.6 V - 0.7 V for Germanium JL transistors.

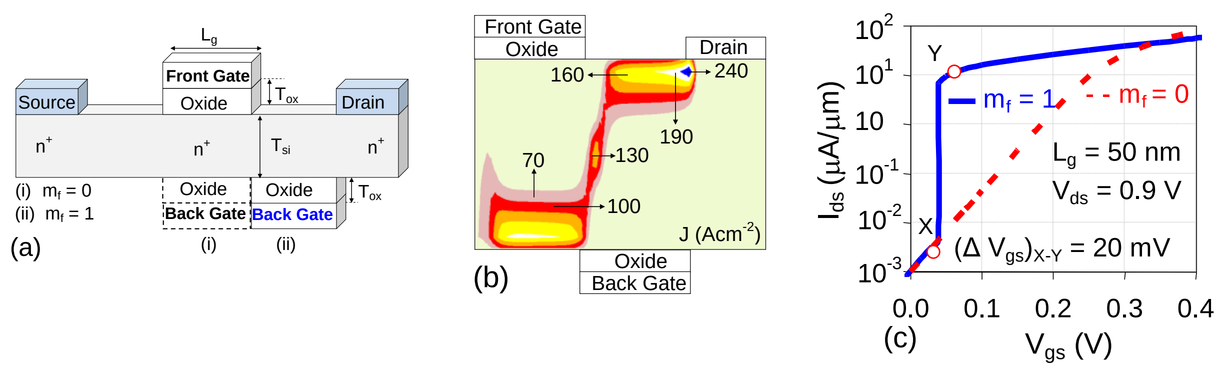

Figure 2: (a) Schematic diagram of DG JL transistor with a misaligned back gate. The misalignment factor (m_f) equals to 0 and 1 for fully aligned and completely misaligned cases, respectively. (b) Contour plot showing total current density in completely misaligned JL device before the onset of steep current transition. (c) Comparison of I_{ds} –V_{gs} characteristics of JL device with m_f = 0 and m_f = 1 at V_{ds} = 0.9 V. Parameters: T_{si} = 7 nm, Oxide thickness (T_{ox}) = 1 nm, L_g = 50 nm and doping (N_d) = 10^{19} cm^{-3}.

(c) ***Raised Source/Drain (RSD) JL architecture***

At the level of device architecture, II can be considerably improved by adopting a Raised Source/Drain topology [14] in a JL transistor (Fig. 3*a*) with Ge as channel material. Results shown in Fig. 3*b* depict that drain current in RSD JL device exhibits steep transition from off-to-on state with S-swing ~1 mV/decade, whereas a conventional DG JL device shows a more of a gradual off-to-on transition with a standard S-swing of 60 mV/decade. The enhanced performance of RSD JL transistor is due to a wider area over which II can be triggered in the semiconductor film. Also, due to single gate controllability, the lateral electric field in RSD architecture is expected to be higher that in a DG MOSFET. Thus, the higher value of electric field coupled with an enhanced current density supports II, and a sub-60 mV/decade S-swing is achieved. Band-to-Band Tunneling (BTBT) of the electrons from channel to drain at lower gate voltages can result in an undesirable increase in drain current, which deteriorates the on-to-off ratio of RSD Ge JL device as shown in Fig. 3*c* [14-15]. Designing RSD JL transistor with thicker side oxide ~1.4 nm can help in considerably suppress the undesirable increase of current at lower V_{gs} without affecting the II at the same supply voltage.

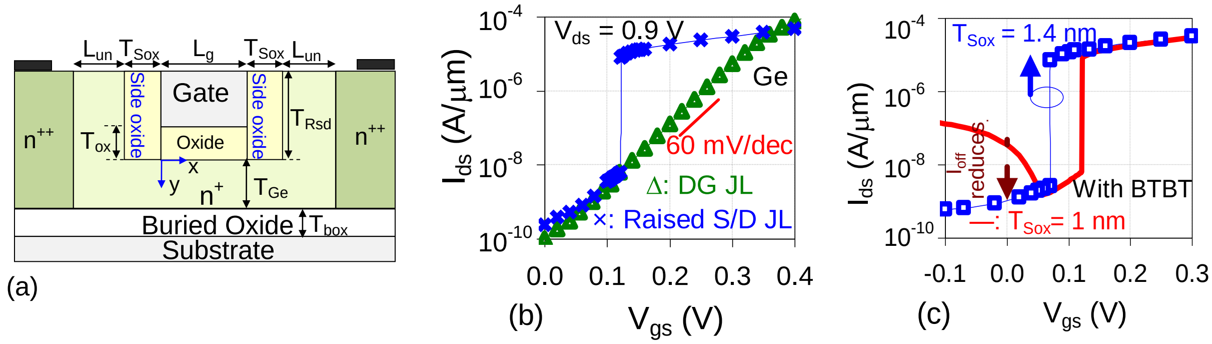

Figure 3: (a) Schematic diagram of a Raised Source/Drain (RSD) JL transistor, (b) Comparison of I_{ds} –V_{gs} characteristics of DG and RSD JL MOSFET, and (c) Impact of off-state Band-to-Band Tunneling (BTBT) and its suppression in a RSD JL MOSFET. Parameters: T_{ox} = 1.7 nm, L_g = 50 nm, N_{ch} = 10^{19} cm^{-3}, Thickness of Germanium film (T_{Ge}) = 7 nm, Side oxide thickness (T_{Sox}) = 1 nm, , height of raised portion (T_{RSD}) = 7 nm, buried oxide thickness (T_{box}) = 10 nm and underlap length (L_{un}) = 10 nm.

II. Anomalous Behaviour of Steep Switching JL Transistor

The research work also demonstrates the following two unique features in JL transistor resulting from FBEs.

(i) ***Positive and negative temperature coefficients of threshold voltage***

Inversion mode and JL transistors operated at relatively lower drain bias of 50 mV exhibit a negative temperature coefficient of threshold voltage i.e. V_{th} reduces with an increase in temperature due to excess generation of carriers with temperature [16]. However, result shown in

Fig. 4*a* depicts an anomalous behaviour due to the dominance of impact ionization induced bipolar effects. When a JL transistor is operated at high drain bias, threshold voltage increases with temperature up till a certain value instead of the usual trend of a continuous reduction in V_{th} with an increase in temperature. This occurs due to the occurrence of strong FBEs at lower temperatures, and V_{th} increases with temperature with a rate dV_{th}/dT = 1.76 mV/K (Region R1) up till T = 360 K. The reduction in V_{th} with dV_{th}/dT = -0.38 mV/K (Region R2) is only observed beyond 360 K. The contrasting behaviour of V_{th} in steep switching JL transistor is due to the two conflicting physical phenomena, having different dependencies on temperature. At lower temperatures (corresponding to R1), the degree of II is enhanced and carrier generation through II dominates over thermal generation. Thus, a significant increase in electron-hole pairs generated through II shifts V_{th} to lower values and yields a positive temperature coefficient of V_{th}. At higher temperatures (R2), thermal generation of carriers dominates over II, and a more conventional trend of negative dV_{th}/dT is observed.

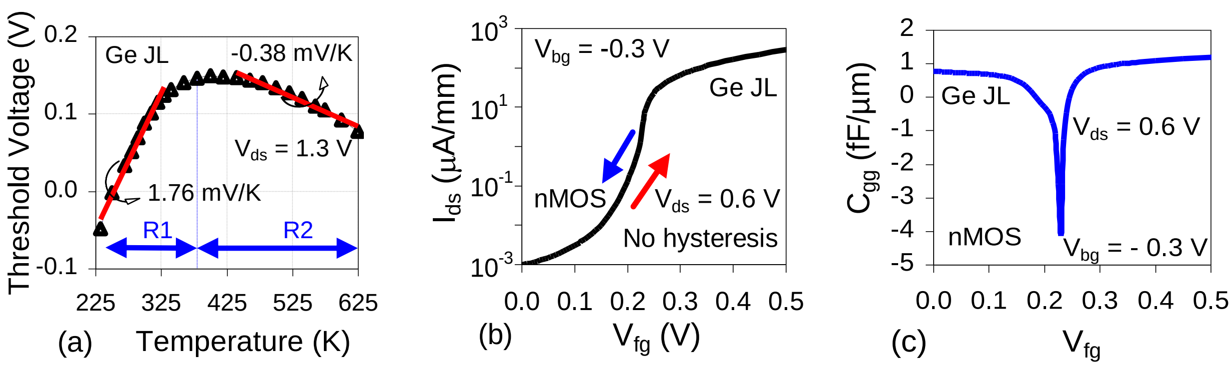

Figure 4: (a) Variation in V_{th} as a function of temperature in symmetric gate operation ($V_{fg} = V_{bg} = V_{gs}$) of Ge JL transistor operated at V_{ds} = 1.3 V, (b) I_{ds}-V_{fg} characteristics of JL transistor operating in asymmetric mode ($V_{fg} \neq V_{bg}$) indicating absence of hysteresis, and (c) Variation in total gate-to-gate capacitance (C_{gg}) in an asymmetrically biased Ge JL device with V_{ds} = 0.6 V and V_{bg} = -0.3 V. Parameters: T_{ox} = 1.7 nm, L_g = 50 nm, $N_d = 10^{19}$ cm^{-3}, T_{Ge} = 7 nm.

(ii) Negative values of total gate capacitance

In JL devices, impact ionization induced bipolar effects result in the occurrence of hysteresis i.e. drain current traverses different paths during Forward Sweep (FS) and Reverse Sweep (RS) of gate voltage [11]. While hysteresis in the transfer characteristics has shown application as memory, the two different values of V_{th} associated with forward and reverse sweeps of V_{gs} makes it unsuitable for logic applications. Moreover, hysteresis leads to an undesirable condition such as racing, variations in drain current and propagation delays depending on device switching history, and can cause instabilities like bit reversal [17]. The primary reason for the hysteresis is the generation of excess electrons due to II in reverse sweep of gate voltage which require more negative bias to be depleted. Therefore, independent gate ($V_{fg} \neq V_{bg}$) operation of JL transistor as shown in Fig. 4*b* has been investigated to suppress the hysteresis while preserving *S*-swing ~15 mV/decade at lower applied V_{ds} of 0.6 V and back gate (V_{bg}) bias of -0.3 V. In addition, the work also shows negative values of total gate capacitance (C_{gg}) at gate bias corresponding to threshold voltage as shown in Fig. 4*c*. The physical mechanism responsible for negative values of C_{gg} at V_{fg} = V_{th} is the significant increase in impact generated hole concentration underneath the front and back gates before the onset of steep transition which changes the *n*-type film into a pseudo '*p*-type' region, and results in negative value of C_{gg}.

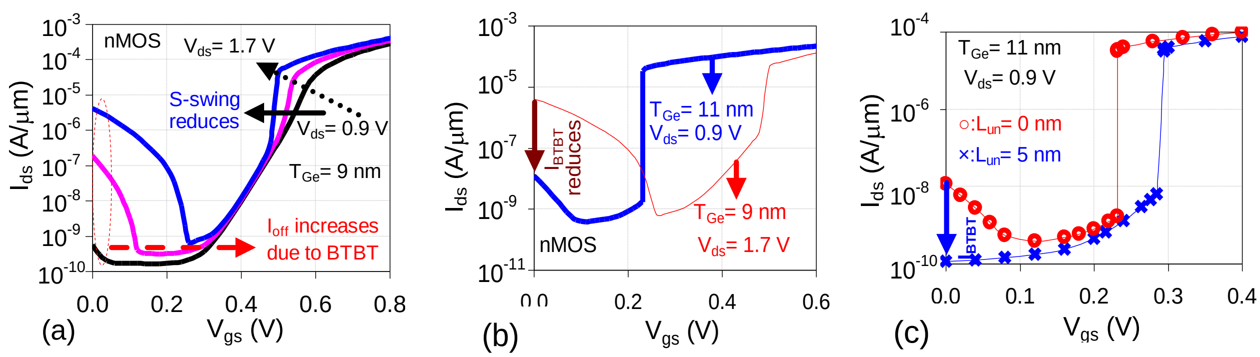

Figure 5: (a) I_{ds}-V_{gs} characteristics of DG Ge JL transistor designed with T_{Ge} = 9 nm for varying V_{ds}, (b) Comparison of I_{ds}-V_{gs} characteristics for Ge JL device designed with T_{Ge} = 11 nm and operated at V_{ds} = 0.9 V with a JL transistor designed with T_{Ge} = 9 nm and operated at V_{ds} = 1.7 V. (c) I_{ds}-V_{gs} characteristics of an optimized Ge JL device with an underlap (L_{un}) of 5 nm.

III. Design perspective using *J.E*

While Ge based JL devices have shown the potential to achieve steep current transition at relatively lower drain bias in comparison to their Si counterparts, the requirement of higher V_{ds} to trigger II results in an increased Band-to-Band Tunneling (BTBT) of electrons (for *n*MOS devices) from channel to drain which is accompanied by an undesirable increase in off-current (I_{off}) [20]. Therefore, a systematic methodology, based on the optimization of product *J.E*, is proposed to sustain II in the semiconductor film at a lower V_{ds} while limiting the off-state BTBT current to benefit from sub-kT/q switching in Ge JL MOSFET. Fig. 5*a*-*b* shows the usefulness of physical insights, through the optimization of *J.E*, into device design with the use of a thicker film (which can be depleted in the off-state) while operating the device at lower V_{ds} to augment *J.E* values along with a suppressed BTBT. The proposed approach is beneficial as the projected increase in the tunneling current at higher V_{ds} can be curtailed by operating at lower drain bias, while II is enhanced due to the higher current density associated with a thicker semiconductor film. An additional reduction in BTBT current (I_{BTBT}) can be achieved with a nominal underlap of 5 nm which limits I_{off} to ~0.1 nA, while maintaining steep switching with *S*-swing of ~5 mV/decade at V_{ds} of 0.9 V.

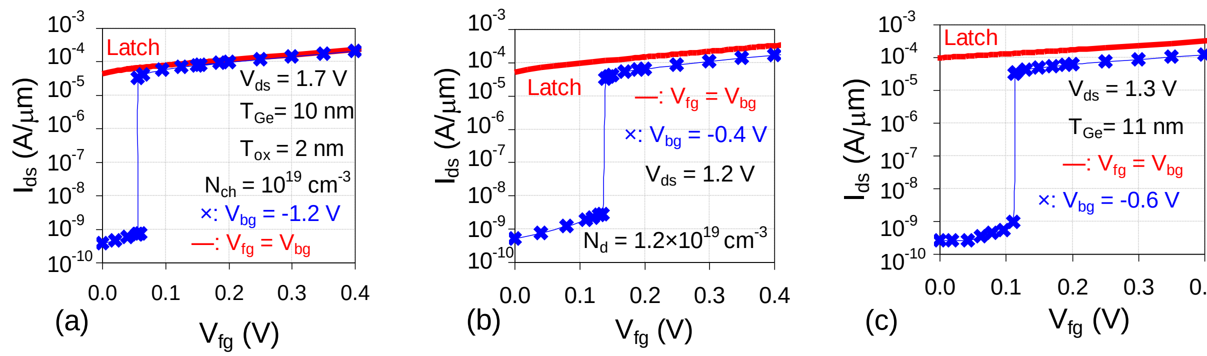

Figure 5: (a) I_{ds}-V_{fg} characteristics of symmetric (V_{fg} = V_{bg}) and independent (V_{bg} = -0.4 V) gate operation of DG Ge JL transistor at (a) V_{ds} = 1.7 V, (b) N_d =1.2 ×10^{19} cm^{-3} and (c) T_{Ge} = 11 nm. The single transistor latch effect is analysed by varying one parameter at any given instance.

IV. Suppression of single transistor latch effect

The work has also investigated the upper limit on II characterized by single transistor latch for *n*MOS and *p*MOS Ge JL devices. While turning-off a JL device can be critical due to heavy doping [11, 18], the problem is aggravated if FBEs are not properly controlled and device is driven into the latch condition. The previous investigations [19] have shown that latching phenomenon in inversion mode devices is solely due to increase drain bias. However, the heavy doping in JL devices facilitates an enhanced degree of II, and thus, latching to the on-state can be triggered due to an increase in doping, film thickness and gate oxide thickness as they all contribute to an increase in current density. Latch is detrimental to the operation as the device cannot be turned-off, and results in an increased power dissipation. The effect becomes more prominent in Ge JL devices due to the higher degree of II which lead to stronger FBEs.

Therefore, latch effect is analysed in DG Ge JL devices and a systematic approach is adopted to suppress the same while preserving the steep switching action with S-swing $\leq$ 10 mV/decade. Fig. 5*a*-*c* illustrates the latch effect in symmetrically biased ($V_{fg} = V_{bg}$) DG Ge JL transistor at V_{ds} = 1.7 V (Fig. 5*a*), $N_d = 1.2 \times 10^{19}$ cm^{-3} (Fig. 5*b*) and T_{Ge} = 11 nm (Fig. 5*c*). The independent gate operation with an appropriate back bias i.e. negative (positive) for *n*MOS (*p*MOS) allows the device to overcome latch condition, and regaining switching action from off-to-on state as shown in Fig. 5. It can also be observed that the use of a negative (*n*MOS) reduces the current density, and restores the transistor functionality while preserving S-swing < 10 mV/decade .

3. CONCLUSION

The prime objective of the thesis work is to provide insights into the operation of JL transistor to achieve a sharp rise in drain current from off-to-on state. The physical understanding of device functionality reveals that the generation of carriers due to II in a MOSFET is governed by the product of current density and electric field i.e. *J.E.* The work carried out in the thesis has primarily focused on enhancing the product *J.E* to augment II at drain bias $\leq$ 1 V for logic applications. Also, an attempt has been made to understand the challenges critical to II induced steep current transition in Germanium JL devices, and a systematic approach has been presented to extend the functionality of junctionless transistor for sub-Boltzmann switching applications. The key contributions of the work presented in thesis are summarized as follows:

(1) An optimized DG JL transistor with the utilization of low-κ sidewall spacer and high-κ gate dielectric can achieve a steep transition in drain current with S-swing ~1 mV/decade. As II is triggered at gate-drain edge, a comprehensive study in DG JL transistor has shown that misaligning the back gate with respect to front gate towards the drain aids to enhance II triggered floating body effects to achieve a sharp increase in current with higher number of decades of current transition at the threshold voltage. The work has also shown an alternative way to increase the impact generated power per unit volume (*J.E*) by increasing the area offered to the carriers to facilitate II through the use raised source/drain JL topology.

(2) The unique features of impact ionization triggered bipolar effects in an essentially unipolar Ge JL transistor have been analysed in the thesis. The research has demonstrated a positive temperature coefficient of threshold voltage in steep switching JL devices resulting from the dominant bipolar conduction mode at temperatures lower than 360 K, whereas unipolar conduction mode is prevalent at higher temperatures which results in the usual negative temperature coefficient of threshold voltage i.e. threshold voltage reduces with an increase in temperature. Also, the independent gate operation has been shown to preserve low *S*-swing ~15 mV/decade, along with negative values of total gate capacitance and a suppression of hysteresis.

(3) Since tunneling induced degradation is significant in Ge based devices, a methodology has been proposed to improve the performance of DG Ge JL transistor through the optimization of *J.E*. It is demonstrated that off-state tunneling current at lower gate voltages can be suppressed by incorporating an optimal underlap after carefully optimizing the film thickness and drain bias. The systematic design methodology has been presented in the work preserves the effectiveness of II to achieve sharp rise in drain current with *S*-swing < 5 mV/decade.

(4) The presence of single transistor latch effect is shown as a limitation, resulting from the enhanced degree of II, where the transistor cannot be turned-off even by reducing the gate voltage to negative values. Therefore, a systematic methodology of independent gate operation has been discussed to regain the steep switching action by overcoming latch effect while preserving the *S*-swing < 10 mV/decade in JL devices.

The work presented in the thesis presents new viewpoints for JL transistors specifically engineered for sub-Boltzmann switching. Physical insights and systematic analysis through innovative approaches leads to enhanced performance of Si and Ge JL devices, which can make them competitive for logic and memory applications.

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LIST OF PUBLICATIONS BASED ON RESEARCH WORK

A. Patent:

1. Abhinav Kranti, and **Manish Gupta**, "Multiple Gate Steep Switching Junctionless Transistor," **Indian Patent Filed** (2594/MUM/2015), Status: Pending India, (2015).

B. Peer-reviewed Journals:

1. **Manish Gupta** and Abhinav Kranti, "Regaining Switching by Overcoming Single Transistor Latch Effect in Ge Junctionless MOSFETs," **IEEE Transactions on Electron Devices**, vol. 65, no. 9, pp. 3600-07, 2018. (Journal Impact Factor: 2.62)
2. **Manish Gupta** and Abhinav Kranti, "Raised Source/Drain Germanium Junctionless MOSFET for Subthermal OFF-to-ON Transition," **IEEE Transactions on Electron Devices**, vol. 65, no. 6, pp. 2406-12, 2018. (Journal Impact Factor: 2.62)
3. **Manish Gupta** and Abhinav Kranti, "Steep-switching Germanium Junctionless MOSFET with Reduced Off-state Tunneling," **IEEE Transactions on Electron Devices**, vol. 64, no. 9, pp. 3582-87, 2017. (Journal Impact Factor: 2.62)
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C. Proceedings in International Conferences:

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2. **Manish Gupta** and Abhinav Kranti, "Hysteresis Free sub-60 mV/dec Subthreshold Swing in Junctionless MOSFETs," 31^{st} International Conference on VLSI Design and 17^{th} International Conference on Embedded System, Pune, India, pp. 133-38, 2018.
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