FEASIBILITY ASSESSMENT OF STEEP SWITCHING IN SILICON AND GERMANIUM JUNCTIONLESS TRANSISTORS

A THESIS

Submitted in partial fulfillment of the requirements for the award of the degree of

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MANISH GUPTA

DISCIPLINE OF ELECTRICAL ENGINEERING

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **Feasibility Assessment of Steep Switching in Silicon and Germanium Junctionless Transistor** in the partial fulfillment of the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY** and submitted in the **DISCIPLINE OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from January 2014 to December 2018 under the supervision of Dr. Abhinav Kranti, Professor, Discipline of Electrical Engineering, Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Signature of the student with date
(MANISH GUPTA)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Signature of Thesis Supervisor
(Prof. ABHINAV KRANTI)

Manish Gupta has successfully given his Ph.D. Oral Examination held on **June 20, 2019**.

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Signature of PSPC Member Date:	Signature of PSPC Member Date:	Signature of Convener, DPGC Date:

Signature of Head of Discipline
Date:

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Manish Gupta

Dedicated to my parents

ABSTRACT OF THE DISSERTATION

Feasibility Assessment of Steep Switching in Silicon and Germanium Junctionless Transistor

The strong demand for Internet of Things (IoT) applications and portable low power electronics has driven the semiconductor industry to design energy efficient transistors. While the circuit and system level optimization can be employed to improve the performance, the fundamental limit is rooted in the switching action of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). In general, the logic functionality of a transistor is characterized by switching from off-to-on state, and the transition from one logic state to another is characterized by a parameter known as Subthrehold swing (*S*-swing), which describes the rate of change of drain current with respect to gate bias in the subthreshold regime and is equal to the thermal limit ~$(kT/q)\ln(10)$, where k is the Boltzmann constant, T is the temperature, and q is the electronic charge. The conventional minimum value of *S*-swing is limited to 60 mV/decade at room temperature, thereby implying that a minimum of 60 mV should be applied at the gate to increase the drain current by a decade. This fundamental limit on the *S*-swing is immutable due to the operation principle i.e. injection of thermally distributed carriers over the barrier in a conventional field effect transistor, and thus, results in increase in an static power dissipation in scaled devices due to non-scalability of *S*-swing below 60 mV/decade. Hence, transistors exhibiting *S*-swing < 60 mV/decade are highly desirable.

With the advent of Junctionless (JL) transistors, the need for fabricating an ultra-sharp *pn* junction in the nanoscale regime can be eliminated while preserving full CMOS functionality. An important attribute of JL transistor is the occurrence of an enhanced degree of Impact Ionization (II) induced Floating Body Effects (FBEs) to achieve a steep rise in drain current with *S*-swing ~1 mV/decade at a relatively lower supply voltage than that required for a conventional inversion mode MOSFET. The reason for the same is the higher value of product of current density (*J*) and electric field (*E*) i.e. (*J.E*), a crucial parameter that governs the power generated per unit volume due to physical phenomena, along with the wider area over which II occurs. The previously reported results for JL devices have shown the potential to achieve *S*-swing ~1 mV/decade.

However, the supply voltage (~2 V) needed to trigger II is not practical for logic applications in emerging technologies. Therefore, the key contribution of research work is to provide physical insights for the better understanding and optimization of Si and Ge JL transistor to facilitate steep switching at relatively lower drain bias. In addition, the work carried out in the thesis is aimed to highlight transistor architectures that facilitate downscaling of applied voltages while preserving the effectiveness of II to trigger steep switching in nanoscale JL transistors.

The relevance of sidewall spacer and high-κ gate dielectrics has been investigated in the nanoscale JL MOSFETs which can be utilized to modulate current density and electric field to affect II, and hence, steep switching. In a Double Gate (DG) JL transistor, the sidewall spacer material and thickness significantly influences lateral extension of depletion region beyond the gate edge and governs the effective channel length (L_{eff}) in subthreshold region. A high-κ (HfO_2) spacer allows for a greater penetration of fringing fields into the semiconductor film and supports the extension of depletion beyond the gate edge as compared to that achieved in a spacer designed with SiO_2 material, and thus, results in a shorter L_{eff} for SiO_2 spacer as compared to that achieved for HfO_2 spacer. The longer L_{eff} indicates a lower electron concentration and a reduced current density which diminishes the magnitude of II due to the lowering of *J.E*. Results show that an optimized JL device designed with a combination of low-κ spacer with optimal thickness and high-κ gate dielectric can achieve a steep rise in drain current at drain bias of 0.9 V. In addition, the thesis reports on the transformation of gate misalignment, traditionally considered detrimental feature, into a unique opportunity to further enhance the II induced FBEs at drain bias equivalent to bandgap of the semiconductor. The misalignment between the front and back gate in DG JL topology facilitates movement of carriers in lateral as well as vertical directions, and thus, leads to an inclined conduction channel, to further augment II through an increase in current density. The advantage of higher current density in misaligned topology is reflected in a nearly ideal *S*-swing ~1 mV/decade along with increased number of decades at threshold.

Apart from presenting the methodologies to achieve steep *S*-swing at lower applied voltages in JL transistor, a detailed analysis on the behavior of electrical parameters of steep switching JL transistor forms an integral part of the thesis. Here, the characteristic feature of threshold voltage (V_{th}) in JL transistor with varying temperature is analyzed. Previously reported results show that inversion mode and JL transistors operated at relatively lower drain bias of 50 mV exhibit a

negative temperature coefficient of threshold voltage i.e. V_{th} reduces with an increase in temperature due to excess generation of carriers. As II induced bipolar effects are significant at relatively higher drain biases, threshold voltage in steep switching JL device increases with temperature up till a certain value instead of the usual trend of a continuous reduction in V_{th} with an increase in temperature. At higher temperatures, thermal generation results in essentially unipolar characteristics and V_{th} reduce with increase in temperature.

Another important attribute of II induced bipolar effect in JL device is the occurrence hysteresis in the transfer characteristics i.e. drain current traverses different paths during Forward Sweep (FS) and Reverse Sweep (RS) of gate voltage. While hysteresis in the transfer characteristics has shown application as memory, the two different values of V_{th} associated with FS and RS of V_{gs} makes it unsuitable for logic applications. In addition to hysteresis, bipolar effects are also responsible for the negative values of total gate capacitance (C_{gg}) at gate bias corresponding to threshold voltage. The negative value of total gate capacitance is the characteristic feature associated with II trigger positive feedback mechanism which results in sub-60 mV/decade *S*-swing. The work contributes to developing the understanding towards the unique behavior of C_{gg} in steep switching JL transistor and explores the independent gate operation as an option to suppress the hysteresis while preserving *S*-swing ~15 mV/decade along with negative C_{gg} at lower applied voltages.

The dissertation also investigates the feasibility and discusses various attributed of Ge based steep switching JL transistor. While Ge as channel material is best suited to design transistor with II as dominant conduction mechanism, the Band-to-Band Tunneling (BTBT) phenomena due to its lower bandgap is inherent to the Ge based devices. Despite uniformly doped channel, the performance of JL devices is deteriorated due to a significant increase in off-current (I_{off}) because of BTBT. Therefore, a systematic methodology, based on the optimization of product of current density and electric field i.e. *J.E*, is proposed to sustain II in the semiconductor film at a lower V_{ds} while limiting the tunneling induced I_{off} to benefit from sub-60 mV/decade switching in Ge JL MOSFET. The developed approach is beneficial as the projected increase in the tunneling current at higher V_{ds} can be curtailed by operating at lower drain bias, while II is enhanced due to the higher current density associated with a thicker semiconductor film. In addition, an optimal

source/drain underlap in JL device is beneficial after optimizing the film thickness and drain bias to further suppress the off-state tunneling while sustaining the *S*-swing < 5 mV/decade.

At the device architectural level, II generated power per unit volume can be considerably improved by adopting a Raised Source/Drain (RSD) topology in a JL transistor. On comparing the performance of RSD JL device with DG JL transistor it is observed that drain current in RSD JL device exhibits *S*-swing ~1 mV/decade, whereas a conventional DG JL device shows a more of a gradual off-to-on transition with a standard *S*-swing of 60 mV/decade. The enhanced performance of RSD JL transistor is due to a wider area over which II can be triggered in the semiconductor film. Also, due to single gate controllability, the lateral electric field in RSD architecture is expected to be higher than that in a DG MOSFET. Thus, the higher values of electric field coupled with an enhanced current density supports II, and a sub-60 mV/decade *S*-swing is achieved. The performance of RSD JL devices can also degrade due to increase in I_{off} because of BTBT. Designing RSD JL transistor with thicker side oxide can considerably suppress the undesirable increase in I_{off} without affecting II at the same supply voltage.

The work has also investigated the upper limit on II characterized by single transistor latch for *n*MOS and *p*MOS Ge JL devices. The latch effect in JL transistor can be triggered due to an increase in doping, film thickness and gate oxide thickness as they all contribute to an increase in current density. Latch is detrimental to the operation as the device cannot be turned-off, and results in an increased power dissipation. The effect becomes more prominent in Ge JL devices due to the higher degree of II which lead to stronger FBEs. Therefore, latch effect is analyzed in DG Ge JL devices and a systematic approach, based on independent gate operation, is adopted to suppress the same while preserving the steep switching action with *S*-swing ≤ 10 mV/decade. The use of a negative (positive) back gate bias in *n*MOS (*p*MOS) JL device reduces the current density, and restores the transistor functionality.

The research work carried out in this dissertation offers a comprehensive study on junctionless transistor and has provided new viewpoints by highlighting the significance of Si and Ge JL transistor architectures for steep switching applications through an understanding of physical phenomenon, and subsequent design and optimization.

LIST OF PUBLICATIONS

A. Patent:

1. Abhinav Kranti, and **Manish Gupta**, "Multiple Gate Steep Switching Junctionless Transistor," **Indian Patent Filed** (2594/MUM/2015), Status: Pending India, (2015).

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C. Proceedings in International Conferences:

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7. **Manish Gupta** and Abhinav Kranti, "Impact of Sidewall Spacer on Steep Subthreshold Swing in Junctionless MOSFETs," **In Abstracts of 18th International Workshop on the Physics of Semiconductor Devices (IWPSD 2015),** Bengaluru, India, pp. 401, 2015.
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ACRONYMS

BOX	*Buried Oxide*
BTBT	*Band-to-Band Tunneling*
BS	*Back Surface*
C	*Center*
CMOS	*Complementary Metal-Oxide-Semiconductor*
CB	*Conduction Band*
DG	*Double Gate*
DIMOS	*Depletion Impact ionization Metal Oxide Semiconductor*
DIBL	*Drain Induced Barrier Lowering*
DRAM	*Dynamic Random Access Memory*
eV	*Electron Volt*
E	*Electric Field*
EOT	*Equivalent Oxide Thickness*
ESD	*Electrostatic Discharge*
FB	*Feedback*
FBE	*Floating Body Effect*
FED	*Field Effect Diode*
FET	*Field Effect Transistor*
FS	*Front Surface*
G-rate	*Generation rate*
IGR	*Impact Generation Rate*
II	*Impact Ionization*
I-MOS	*Impact Ionization Metal Oxide Semiconductor*
INV-mode	*Inversion mode*
IoT	*Internet of Things*
J	*Current Density*
JL	*Junctionless*
MOS	*Metal-Oxide-Semiconductor*
MOSFET	*Metal-Oxide-Semiconductor Field Effect Transistor*
NCFET	*Negative Capacitance Field Effect Transistor*
NEMS	*Nanoelectromechanical Switch*
R-rate	*Recombination rate*
RS	*Reverse Sweep*
RSD	*Raised Source Drain*
SCE	*Short Channel Effect*
SGFET	*Suspended Gate Field Effect Transistor*

SILVACO	*Device Simulation Software*
SOI	*Silicon-on-Insulator*
SRH	*Shockley-Read-Hall*
S-swing	*Subthreshold swing*
STL	*Single Transistor Latch*
TCCT	*Thin Capacitive Coupled Thyristor*
TFET	*Tunnel Field Effect Transistor*
UL	*MOSFET with Source/Drain Underlap*
VB	*Valence Band*
Z^2FET	*Zero Impact Ionization Zero S-swing FET*
ZTC	*Zero Temperature Coefficient*

NOMENCLATURE

C	*Center*
CS	*Classical simulations*
C_d	*Depletion Capacitance*
C_{gg}	*Total Gate capacitance*
C_{ox}	*Oxide capacitance*
C_{para}	*Parasitic capacitance*
e	*Electrons*
E_g	*Band gap energy*
$F_{electrostatic}$	*Electrostatic force*
$F_{elastic}$	*Elastic force exerted by spring*
H_g	*Gate electrode height*
I	*Current*
I_{BTBT}	*Band-to-Band Tunneling current*
I_{ds}	*Drain current*
I_{off}	*Off-current*
I_{on}	*On-current*
$I_{\mathrm{on}}/I_{\mathrm{off}}$	*On-to-off current ratio*
k	*Boltzmann constant*
k_1	*Spring constant*
kT/q	*Thermal voltage*
L_{g}	*Gate length*
L_{eff}	*Effective channel Thickness*
L_{un}	*Underlap length*
m_{f}	*Misalignment factor*
N_{a}	*Doping concentration (Acceptor-type)*
$(N_{ch})_{\mathrm{min}}$	*Minimum channel doping*
N_{d}	*Doping concentration (Donor-type)*
N_{SD}	*Source/Drain doping*
n_e	*Electron concentration*
$n_{e,max}$	*Maximum electron concentration*
n_{h}	*Hole concentration*
$n_{h,min}$	*Minimum hole concentration*
q	*Electronic charge*
Q	*Electrode charge*
QS	*Quantum simulation*
$R1$	*Region 1*
$R2$	*Region 2*
S/D	*Source/Drain*

S_{side}	*Sidewall spacer width*
S-swing	*Subthreshold swing*
t_{gap}	*Distance between oxide and movable electrode*
T	*Temperature*
T_{box}	*Buried oxide thickness*
T_f	*Fin thickness*
T_{ox}	*Gate oxide thickness*
T_{RSD}	*Height of raised portion*
T_{si}	*Silicon film thickness*
T_{Ge}	*Germanium film thickness*
T_{Sox}	*Side oxide thickness*
V	*Voltage*
V_{bg}	*Back gate bias*
V_d	*Drain potential*
V_{dd}	*Supply Voltage*
V_{ds}	*Drain to source voltage*
V_{fg}	*Front gate voltage*
V_{go}	*Gate overdrive voltage*
V_{gs}	*Gate to source voltage*
V_s	*Source potential*
V_{th}	*Threshold voltage*
ΔV_{gs}	*Change in gate voltage*
ΔV_{th}	*Shift in threshold voltage*
W_{g}	*Gate width*
ΔW	*Hysteresis window*
x_1	*Disatance between the position of gate electrode and oxide*
X	*x-direction*
Y	*y-direction*
α_{n}	*Electron ionization coefficient*
α_{p}	*Hole ionization coefficient*
κ	*Permittivity*
κ_{Gate}	*Gate dielectric permittivity*
κ_{Spacer}	*Spacer dielectric permittivity*
φ_m	*Gate workfunction*
ΔV_{gs}	*Change in gate voltage*
$\Delta \Phi$	*Potential difference*
ψ_{s}	*Surface potential*
σ	*Constant of proportionality*

Chapter 1

Introduction

1.1 Motivation for Steep Switching Devices

Over the past six decades, considerable efforts have been carried out to scale down the dimensions of Metal Oxide Semiconductor (MOS) Field Effect Transistor (FET) to yield enhanced circuit functionality [1-18]. This has been made possible by the continuous improvement in the transistor performance through the concept of miniaturization proposed by Gordon E. Moore [3] along with scaling theory reported by Dennard *et al*. [18]. In 1965, Gordon Moore predicted that the number of transistors on a chip would double annually, which was subsequently revised to 18 months [4]. The vision of Moore continued to increase the transistor count [4], which on combining with Dennard's scaling [18] theory, revolutionized the semiconductor industry toward the development of faster and cheaper electronic equipment.

Table 1.1 Scaling theory proposed by Dennard *et al*. [18].

Device and Circuit Parameter	Scaling Factor
Device dimensions (W_g, L_g, T_{ox})	$1/\alpha$
Doping Concentration (N_a)	α
Voltage (V)	$1/\alpha$
Current (I)	$1/\alpha$
Capacitance ($\varepsilon A/t$)	$1/\alpha$
Delay time (Circuit) (CV/I)	$1/\alpha$
Power dissipation (Circuit) (VI)	$1/\alpha^2$

The key components of scaling theory are outlined in Table 1.1, in which, W_g, L_g, T_{ox} and t represent the gate width, length, oxide thickness and distance between the plates of the capacitor, respectively. α is the unitless scaling factor, ε is the dielectric permittivity and A is the area associated with the capacitances (including interconnections lines and devices). While the scaling of transistor, to pack more number of devices per unit area of the chip can be considered as a driving force to enhance the performance of integrated circuits, the resulting increase in static power dissipation of the transistor is a critical issue and limits the performance of circuit [19]. Therefore, to improve the overall system performance, the focus has been directed to an application specific design of the transistor to achieve high speed while maintaining the need for low power dissipation [20-21]. The logic chips, specifically designed to achieve low power operation, are mainly used in portable electronic gadgets such as mobile phones, notebook computers, where the optimization of both performance and power are of concern [22].

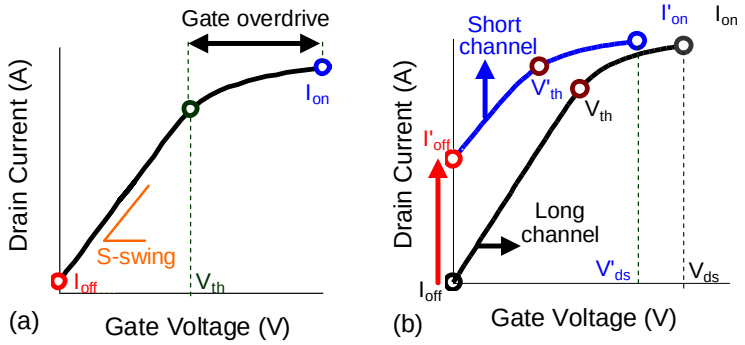

Fig. 1.1: (a) Drain current (I_{ds}) - gate voltage (V_{gs}) characteristics of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) showing switching action and (b) comparison of I_{ds}-V_{gs} characteristics of long channel and short channel MOSFET showing increase in on-current (I_{on}) and off-current (I_{off}) along with degradation in S-swing.

Fig. 1.1*a* illustrates the switching action of a transistor which in general, is outlined through drain current (I_{ds}) - gate voltage (V_{gs}) characteristics. The switching ability of the transistor is preserved by achieving lower value of off-

current (I_{off}) and higher value of on-current (I_{on}). The transition from off-to-on state is often described in terms of the rate of change of drain current with respect to applied gate. This parameter is usually known as Subthreshold swing (*S*-swing), and is given by [19-22]

$$S-swing = \frac{dV_g}{d\psi_s}\frac{d\Psi_s}{d\log_{10} I_d} \cong \left(1+\frac{C_d}{C_{ox}}\right)\ln 10\frac{kT}{q} \qquad (1.1)$$

where V_g is the applied gate voltage, Ψ_s is the surface potential, I_d is the drain current, k is Boltzmann constant, T is temperature, q is electronic charge, C_d and C_{ox} are depletion and oxide capacitance, respectively. The term $dV_g/d\Psi_s$ is known as transistor body factor, and is denoted by *m*, and $\frac{d\psi_s}{d\log_{10} I_d}$ is defined as *n*, a factor that characterizes the change in drain current with respect to surface potential, describing the conduction mechanism in the channel [22]. At room temperature, *S*-swing becomes equal to ~ (kT/q)ln(10) where (kT/q) is the thermal voltage. For classical transistors [22], *S*-swing turns out to be 60 mV implying that a minimum 60 mV of gate voltage is required to increase the drain current by one decade [22]. Moreover, lowering the drain bias (V_{ds}), in long channel device, adversely affects the transistor performance by reducing the I_{on} (or gate overdrive) [22]. Also, the reduction in on-current reduces the on-to-off current ratio, a crucial parameter for the transistor.

Fig. 1.1*b* compares the performance of long and short channel device. While the reduction in gate length is beneficial to maintain the gate overdrive at lower drain bias, the resulting degradation in *S*-swing due to Short Channel Effects (SCEs) such as Drain Induced Barrier Lowering (DIBL) deteriorate the performance of the transistor [11]. Moreover, the reduction in V_{th} contributes to an exponential increase in the off-current in short channel devices [19-20]. Thus, the non-scalability of the supply voltage and *S*-swing below 60 mV/decade while maintaining sufficiently low value of off-current [19-20] are critical issues which limit the switching action of the transistor and the associated circuit for logic applications. Therefore, to overcome the above

mentioned problems, focus has shifted towards energy efficient operation of a transistor which requires a value of *S*-swing to be as low as possible along with sufficiently low off-current at relatively lower applied V_{ds}. The device with considerably lower values of *S*-swing is designated as a steep switching device [19-20].

The devices that achieve *S*-swing < 60 mV/decade are used in various different applications [41-50]. For example, thyristor is widely used in power electronics due to its sharp switching and high current drive [23]. Other devices such as, Field Effect Diodes (FEDs) [24] and, thin capacitive coupled thyristor (TCCT) [25] can be used for electrostatic discharge (ESD) protection. Also, steep switching devices have shown wide applications in designing of Dynamic Random Access Memory (DRAM) applications [26-30]. Thus, it is necessary to review the advantages and challenges associated with the steep *S*-swing devices proposed in the literature.

1.2 Novel Steep Switching Devices

1.2.1 Negative Capacitance Field Effect Transistors

The *S*-swing in a MOSFET can be curtailed below 60 mV/decade by modifying the factor *m* or *n* (eq. 1.1). While the factor *m* depends on the gate electrostatics, *n* can be changed by adapting a different conduction mechanism. In 2008, Salahuddin *et al.*, [31] have experimentally demonstrated that integrating a standard gate insulator with ferroelectric material of appropriate thickness in conventional MOSFETs (Fig. 1.2) reduces the *m* value less than 1, and thereby results in *S*-swing value below 60 mV/decade. An important attribute that results in the enhanced performance of conventional FET with ferroelectric dielectric is the negative value of capacitance [31]. This negative value of the capacitance arises due to the negative slope of Polarization-Electric field (*P*-*E*) curve around the origin and can be used to step-up the surface potential, thereby reducing the *S*-swing. Therefore, in a conventional transistor, a ferroelectric layer in the gate-stack

can make the total capacitance looking into the gate larger than the classical MOS capacitance [31]. Thus, to induce the same amount of charge in the channel, the required applied gate voltage should be lower than what would be needed classically.

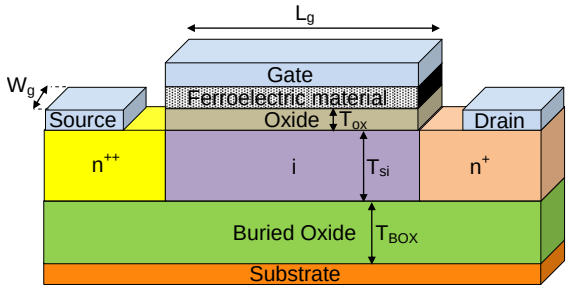

Fig. 1.2: Schematic diagram of Negative Capacitance (NC) Field Effect Transistor (FET) [31]. The substrate is lightly doped with *p*-type impurity, whereas source and drain regions are doped with *n*-type impurities. W_g, L_g, T_{ox}, T_{BOX} and T_{si} indicate gate width and length, gate oxide thickness, buried oxide thickness and silicon film thicknesses, respectively.

After the first successful demonstration of Negative Capacitance (NC) FETs, the operation principle of NCFETs has been investigated by various authors [32-34]. In addition, authors in [35] have reported the optimization technique to improve the performance of NCFET designed for analog applications. Also, considerable efforts have been made to model the performance of NCFET to analyze the impact of variation in structural parameters [36-37]. The operation of NCFETs significantly depends on polarization and optimization of ferroelectric layer thickness, thus integration of ferroelectric material with appropriate thickness is a critical issue [38]. In order to obtain the optimal performance of NCFET, the ferroelectric layer thickness should be thin enough to preserve the steep transition in drain current without contributing the gate leakage. Moreover, the voltage amplification in NCFETs depends on the viscosity coefficient of ferroelectric layer [39]. Therefore, a low viscosity coefficient is required for a steep switch, which makes it unsuitable for high speed applications [39]. Also, the

occurrence of hysteresis in NCFETs is not suitable for logic functionality [40-41]. Nevertheless, the applicability of NCFETs in hysteretic or non-hysteretic [41] applications are still under investigation.

1.2.2 Tunneling Based Field Effect Transistor

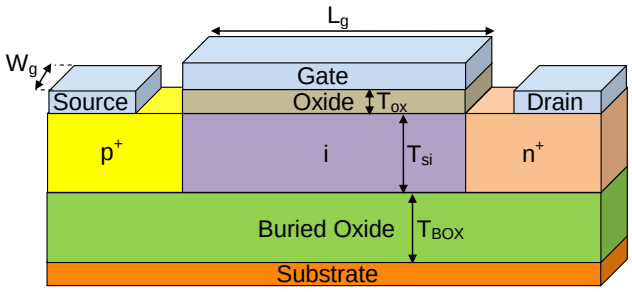

Fig. 1.3: Schematic diagram of *n*-type TFET [42]. The substrate is kept intrinsic or lightly doped with *p*-type impurity, whereas source and drain regions are doped with *p*-type and *n*-type impurities. W_g, L_g, T_{ox}, T_{BOX} and T_{si} indicate gate width and length, oxide thickness, buried oxide thickness and silicon film thicknesses, respectively.

In order to curtail the 60 mV/decade switching at room temperature in conventional MOSFETs, Tunnel Field Effect Transistor (TFETs), shown in Fig. 1.3, has been proposed [42-51]. The first three terminal Silicon TFET was studied by Banerjee *et al.*, [42] whereas the authors in [43] analyzed the various aspects related to scaling of TFETs. As shown in Fig. 1.3, TFETs are designed with asymmetric doping of source and drain region along with intrinsically or moderately doped channel [45]. In contrast to MOSFETs, in which carriers are thermally injected over a barrier, the conduction mechanism in TFETs is primarily governed by the interband tunneling of the electrons (for *n*-type operation) when positive gate voltage is applied [19]. While TFETs have been considered as promising candidates for *S*-swing < 60 mV/decade at lower applied supply voltages, their performance are mainly limited by the precisely controlled doping and abruptness of source-channel junction [45], increased value of parasitic capacitance [52], relatively lower values of on-current (I_{on}) [19], and occurrence of sub-60 mV/decade swing at

lower current levels. Also, the gate must be aligned to the tunneling junction for optimal performance of the device [19]. In addition, Qiu *et al*., [53] have reported that the performance of TFETs is mainly deteriorated due to presence of traps [53].

In an attempt to increase I_{on}, advance device architecture such as multiple gate TFETs to enhance the gate controllability over the tunneling junctions [45, 19], pocket doped [54-55] and bilayer TFETs [56] to increase the tunneling area [54-56], and heterostructure TFETs [57-59] to improve the carrier transport have been proposed. Although simulations predict that the above reported techniques can serve the purpose to improve the *S*-swing and I_{on} of TFETs, the experimental results on TFETs has shown *S*-swing value limited to ~ 30-50 mV/decade at room temperature in relatively complex structures [60-63].

1.2.3 Feedback Field Effect Transistors

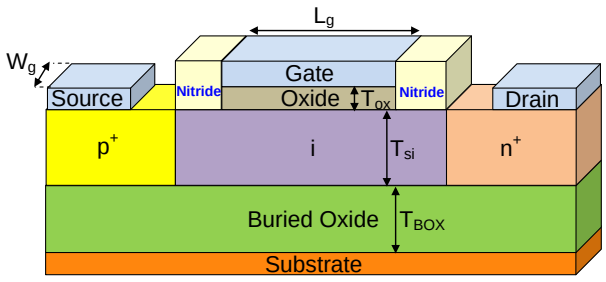

Fig. 1.4: Schematic representation of *n*-type Feedback (FB) FET [64]. The substrate is kept intrinsic, whereas source and drain regions are doped with *p*-type and *n*-type impurities. W_g, L_g, T_{ox}, T_{BOX} and T_{si} indicate gate width and length, oxide thickness, buried oxide thickness and silicon film thicknesses, respectively.

The schematic view of a Feedback (FB) FET, shown is Fig. 1.4, is similar to TFET, except that the doping of the source and drain regions are limited away from the gate edge with the help of nitride spacers. The first experimental demonstration of FBFET was demonstrated by Padilla *et al*., [64] in 2008, which shows the *S*-swing ~ 2 mV/decade at V_{ds} = 1.25 V [64]. A

one time programming event is necessary to achieve steep *S*-swing in FBFET [64]. With an appropriate programing condition (or applied voltages), electrons are trapped in the nitride spacer adjacent to n^+ region, whereas holes are injected into the spacer towards p^+ region. Once the device is programmed, the electrons stored in nitride spacer contributes to negative potential and creates an energy barrier for electrons towards n^+ region, whereas stored holes in spacer towards p^+ region restrict the flow of holes [64]. This results in the device to remain in off-state for lower values of gate voltages. In order to begin the operation of the transistor, a positive gate voltage is applied at the gate terminal which lowers the barriers for the electrons. The reduction in barrier allows electrons from source to flow towards the drain where they get trapped in the potential well. The trapped electrons lower the energy barrier and allow holes to diffuse from drain into the channel region. The diffusion of holes further reduces the barrier for electrons and allows more electrons to travel towards the drain and lowers the barrier for holes. The repeated reduction in the barrier height triggers positive feedback mechanism, and eventually, the energy barrier vanishes completely which results in sharp rise in drain current [64].

While FBFETs achieve steep *S*-swing, several issues limit their performance. The steep transition in FBFETs necessitates prior programming operation which requires a relatively higher voltage (~9 V) to trap the electrons and holes in nitride spacer [65]. The programming operation becomes critical when several transistors in a logic circuit need to be programmed simultaneously [65]. Moreover, the threshold voltage of the device can change over the time due to the detrapping of electrons and holes stored in the nitride layer [65]. Also, the scaling of drain bias set limitation on FBFET for energy efficient operation [65-67]. As the creation of potential well using spacers requires extra areas, the total area occupied by FBFET is relatively higher than MOSFET for the same feature size [66]. Therefore, steep switching mechanism achieved through the FBFET may not be reliable [65].

1.2.3.1 Zero Impact Ionization Zero S-swing Field Effect Transistor

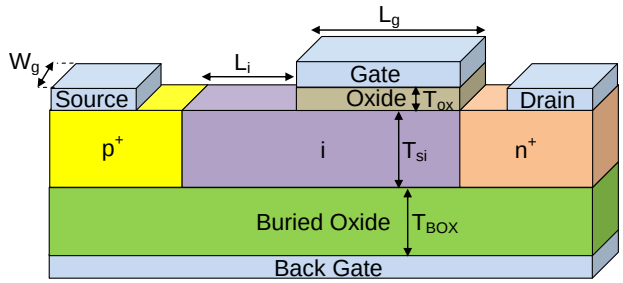

Fig. 1.5: Schematic diagram of *n*-type zero II and zero *S*-swing FET (Z^2FET) [68]. The substrate is kept intrinsic, whereas source and drain regions are doped with *p*-type and *n*-type impurities. W_g, L_g, L_{in}, T_{ox}, T_{BOX} and T_{si} indicate gate width and length, intrinsic region length, gate oxide thickness, buried oxide thickness and silicon film thicknesses, respectively.

Recently, zero impact ionization and zero *S*-swing FETs (Z^2FETs), shown in Fig. 1.5, have gained significant attention to overcome the problems associated with the feedback field effect transistors [68-70]. The fabrication of Z^2FET is relatively simple and it eliminates the need of pre-programing condition to achieve steep switching from off-state to on-state [68-70]. The doping in Si film in Z^2FET is similar to feedback field effect transistor except that the gate partially covers the intrinsic channel region. Additionally, the back gate in Z^2FETs is crucial to create the injection barriers. The portion of the channel left uncovered with the front gate is controlled by the back gate whereas the remaining part of the channel is controlled by both front and back gates [68]. While the charges stored in the spacer region govern the threshold voltage of the feedback FET, the threshold voltage in Z^2FETs varies linearly with the front gate voltage [68]. The working principle of Z^2FETs is similar to feedback FETs where the modulation in the energy band, via front and back gate, due to injection of the carriers in the channel region governs the off-state to on-state transition [68]. The experimentally reported results show that Z^2FETs can achieve *S*-swing $\leq$ 1 mV/decade for V_{ds} ~ 1V- 2 V [68].

Although Z^2FETs can be considered as potential contenders for sub-Boltzmann switching applications, the performance is mainly limited due to

the non-scalability of applied voltages below 1 V [68-70]. Also, a constant back gate bias of ~ 2V is essential to create the barrier for holes [68-70]. In addition, the number of decades of steep current transition at threshold voltage and on-current reduces significantly as supply voltage is scaled down to lower values. Results reported in [70] depict that the reduction in supply voltage from 1.5 V to 1 V in *n*-type Z^2FETs leads to 10^2 times reduction in the on-current i.e. from 10^{-3} A/μm at V_{ds} = 1.5 V to ~10^{-5} A/μm at V_{ds} = 1 V with applied back gate bias of 2 V. The recent results reported in [71] have further confirmed that the scaling of the applied drain bias is challenging in Z^2FET.

1.2.4 Nanoelectromechanical Switches

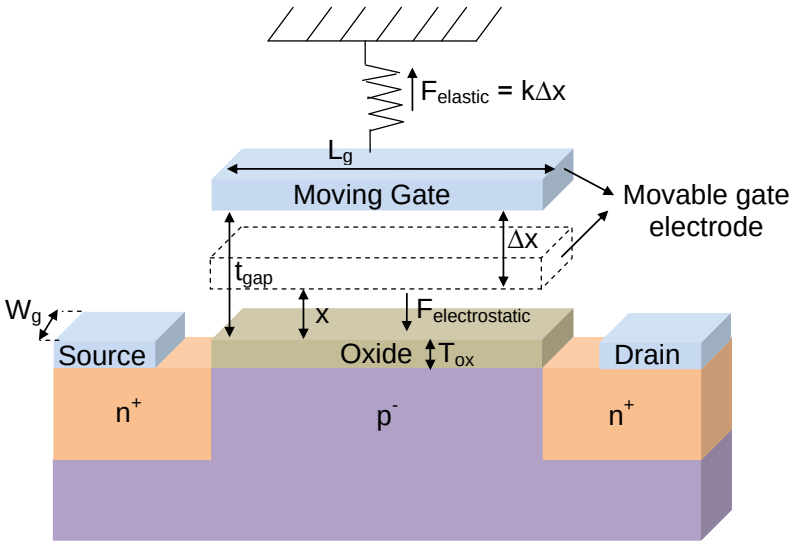

Fig. 1.6: Schematic diagram of *n*-types Suspended Gate (SG) FET [74]. The substrate is lightly doped with *p*-type impurity, whereas source and drain regions are heavily doped *n*-type impurities. W_g, L_g, T_{ox}, T_{BOX} and T_{si} indicate gate width and length, gate oxide thickness, buried oxide thickness and silicon film thicknesses, respectively. t_{gap} is the maximum distance between oxide and movable gate electrode, x_1 is the distance between the position of gate electrode and oxide and k_1 is spring constant [74].

A transistor architecture which uses an electromechanical gate, shown in Fig. 1.6, has been proposed in the literature to overcome the switching limit of

60 mV/decade in classical transistor [72-74]. The device structure is similar to conventional MOSFET except that the gate electrode, instead of being in direct electrical contact with the gate oxide, is mechanically suspended (Fig 1.6). Due to its suspended gate structure, such types of devices are also known as suspended gate FET (SGFET) [74]. This transistor topology introduces an air gap between the gate oxide and the gate electrode and part of the gate voltage is dropped over the capacitance associated with air gap [74]. At zero gate bias, the device is under flatband condition and the charge density on the gate electrode and inside the film is zero [74]. Also, the gap between the gate electrode and oxide remains equals to gap thickness (t_{gap}) i.e. $x_1 = t_{gap}$ [74]. When a positive gate bias is applied, the positive charge on the gate electrode induces the negative charge in the film and results in electrostatic force ($F_{electrostatic}$) pulling down the suspended gate i.e. $x_1 < t_{gap}$ [74]. At gate voltage less than the voltage require for balancing the counteracting elastic force ($F_{elastic}$), the device exhibits very low value of the current [74]. However, a further increase in gate voltage overcomes the elastic force and gate electrode collapses on the oxide [74]. The sudden reduction in air gap ($x_1 = 0$) leads to a significant increase in gate capacitance and results in considerable reduction in threshold, and consequently, a sharp rise in drain current with *S*-swing ~ 1 mV/decade is obtained [74].

Although NEMS shows the potential to achieve *S*-swing ~ 2 mV/decade, a crucial challenge while fabricating the suspended gate FETs featuring CMOS compatible threshold voltages is to realize the appropriate thickness of the gap between gate oxide and electrode [74]. Also, the switching speed is dependent on the mechanical delay which is of the order of nanoseconds in these devices [65]. In addition, the gate voltage needed to pull the gate electrode is always higher than the voltage required for pulling the electrode out which results in hysteresis effect (i.e. threshold voltages changes), and thus, limits the usability of SGFETs in logic applications [65]. Moreover, an increased air-gap in suspended gate enhances the SCEs which could deteriorate the performance of the transistor [20].

1.3 Evolution of Impact Ionization Induced Steep Switching MOSFETs

1.3.1 Impact Ionization in Inversion Mode MOSFETs

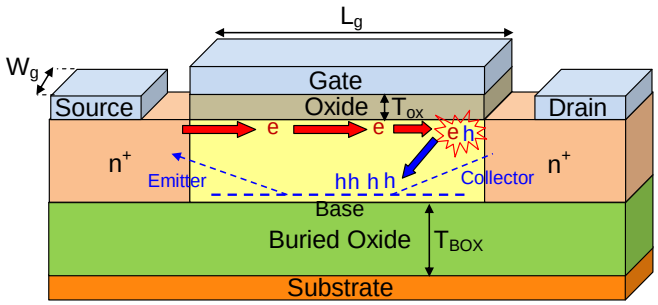

Fig. 1.7: Schematic of an *n*-type inversion mode MOSFET, with a gate length of L_g, gate oxide thickness of T_{ox}, silicon film thickness of T_{si}, buried oxide thickness of T_{BOX} and gate width of W_g. The substrate is lightly doped *p*-type (p^-) and source and drain are heavily doped with *n*-type of impurities [75].

Impact Ionization (II) is a high field phenomenon based on the avalanche breakdown, where electrons in the channel region, shown in Fig. 1.7, acquire sufficiently high energy from the applied drain bias and collide with the crystal atoms at the channel-drain edge to generate electron-hole pairs [75]. The same was reported by various research groups in partially depleted SOI MOSFETs operated at relatively higher drain bias [75-77]. The electrons generated because of impact ionization move towards the positively biased drain, whereas holes generated due to II are stored at lower potential region in the semiconductor film [75]. The successive accumulation of holes triggers strong Floating Body Effects (FBEs) and forward biases the source-channel junction by raising the film potential [75]. The increase in body potential further lowers the barrier between source and channel, and allows more electrons to facilitate II leading to an increase in drain current [75]. The higher value of drain current further enhances II and triggers positive feedback mechanism along with normal MOS operation [75]. Resulting from positive feedback, the drain current achieves very steep rise from off-to-on state for

few mV change in gate bias. The II facilitated steep *S*-swing has been observed experimentally in Silicon-on-Insulator (SOI) transistors [75].

While the inversion mode SOI MOSFETs are capable of achieving II triggered steep current transition from off-to-on state, the higher supply voltage (> 1V) makes II non-conducive for low power logic applications [75-77]. Since the conduction channel in inversion mode MOSFET is located at the oxide-semiconductor interface, the high electric field may give rise to hot electrons that can be injected into the gate oxide, thereby damaging the oxide-silicon interface [11]. Thus, while using II as a switching mechanism, device reliability has been a concern [11].

1.3.2 Impact Ionization MOS Transistor

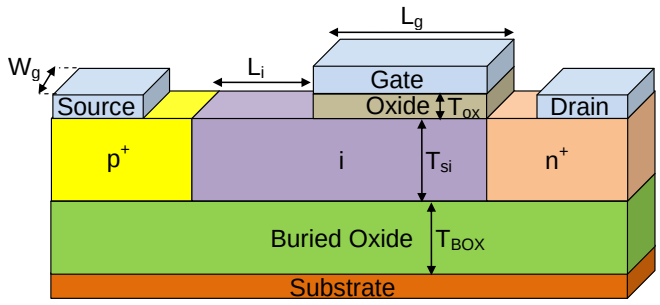

Fig. 1.8: Schematic view of Impact ionization MOS (IMOS) transistor [78]. The doping of substrate is lightly doped *p*-type (p^-) or kept intrinsic. Source and drain regions are doped with *n*-type and *p*-type impurities. W_g, L_g, L_i, T_{ox}, T_{BOX} and T_{si} indicate gate width and length, intrinsic region length, gate oxide thickness, buried oxide thickness and silicon film thicknesses, respectively.

Fig. 1.8 shows the schematic diagram of *n*-type Impact ionization MOS (IMOS) transistor [78]. The structural design of IMOS device is similar to conventional TFET except the gate partially covers the intrinsic channel region [78-82]. The IMOS transistor was first proposed and demonstrated in 2005 by Gopalakrishnan *et al*., [78-79]. The device is a gated *p-i-n* diode and works through the modulation of its channel length [78-79]. Initially at lower

V_{gs} i.e. V_{gs} = 0, the effective channel length is equal to the intrinsic region and current through the device is equal to reverse leakage current [78]. When a positive gate voltage is being applied, an inversion layer is formed underneath the gate which modulates the effective channel length and forces the drain voltage to fall across the uncovered region of the channel [78]. At sufficiently higher gate bias, the voltage drop across the un-gated region further increases to facilitate avalanche breakdown in the off-set region, and results in the sharp rise in drain current with *S*-swing ~ 5 mV/decade [78].

While the IMOS device due to its unique feature of achieving steep rise in drain current have gained a lot of attention, the scaling of the supply voltage is critical to low power operation [80]. For designing Si based IMOS transistor, Choi *et al*. [81–82] have investigated the integration processes by means of a two-spacer process with lengths ranging from 120 to 160 nm and operated at supply voltages ~ 5.5 V. Toh *et al*. [83-84] have proposed L-shaped IMOS with SiGe source and drain, with lengths between 120 and 160 nm and operated with the lowest measured supply voltage of 7.8 V. Mayer *et al*., [85-86] fabricated a 1.4 μm long *p*-channel IMOS device on SOI substrate and reported a sharp drain current transition at 18 V [85-86]. While the applied voltage in the devices with gate lengths as low as 17 nm have remained at higher level [87].

Although IMOS transistors are capable to achieve sub-60 mV/decade current switching from off-to-on state, their performance is limited by the non-scalability of the supply voltage to 1 V. Authors in [78] have reported that designing IMOS transistor with Ge can possibly reduce the supply voltage to 1 V [78]. However, the reliability issues associated with the IMOS transistor significantly deteriorates its performance [65], [79]. On multiple measurements, the hot carrier induced damage in IMOS devices causes considerably degradation in *S*-swing values along with large shift in threshold voltage [65]. Thus, steep switching action in IMOS transistor cannot be sustained after multiple measurements. Also, authors in [88] have shown that

the reliability concern of IMOS transistor can be improved with a delta-p^+ doped vertical structure [88]. However, the reported structure utilized FBEs as in partially depleted SOI MOSFET, which is fundamentally different from IMOS principle to achieve sharp increase in drain current.

1.3.3 Depleted Impact Ionization MOSFET

In order to improve the reliability of IMOS transistor and to reduce the supply voltage required for avalanche breakdown to trigger the steep rise in drain current, authors in [89] have proposed Depleted Impact Ionization MOS transistor (DIMOS) as shown in Fig. 1.9. In a DIMOS transistor, impact ionization occurs uniformly in the bulk, instead of the surface, and the carriers are physically distanced from the surface [89]. Thus, the degradation due to the trapping of energetic electrons into the oxide is no more present in DIMOS transistors. The schematic diagram of *p*-channel DIMOS transistor [89] shown in Fig. 1.9 is similar to IMOS device except that the region underneath the gate is moderately doped with *p*-type of impurity.

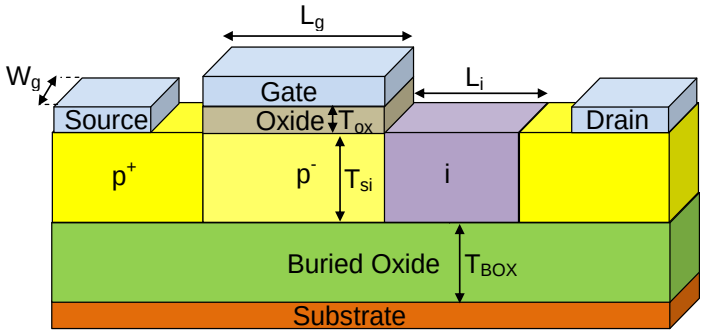

Fig. 1.9: Schematic view of Depleted Impact ionization MOS (DIMOS) transistor [89]. W_g, L_g, L_i, T_{ox}, T_{BOX} and T_{si} indicate gate width and length, intrinsic region length, gate oxide thickness, buried oxide thickness and silicon film thicknesses, respectively.

The basic principle of operation of DIMOS transistor is identical to conventional IMOS device provided the gate is used to deplete the carriers from the underlying moderately doped region [89]. For *p*-type operation,

applying $V_{gs} \leq 0$ V creates sufficiently high electric field to trigger impact ionization induced avalanche breakdown which results in higher value of drain current [89]. The increase in gate voltage to positive values depletes the carriers from the moderately doped region which lowers the field, and thus, turns off the device with steep value of *S*-swing [89]. Moreover, authors have experimentally demonstrated and confirmed that DIMOS transistor overcomes the reliability issues associated with conventional IMOS transistor [89]. While the result reported for DIMOS transistor are promising, requirement of higher supply voltage (> 3 V) limits its use for low power operation [89]. Therefore, to use II as a switching mechanism for achieving steep rise in drain current at relatively lower applied voltages, a transistor topology, which can trigger II and achieve sub-Boltzmann switching from off-to-on state at relatively lower applied voltages, is required.

1.4 Junctionless Transistors

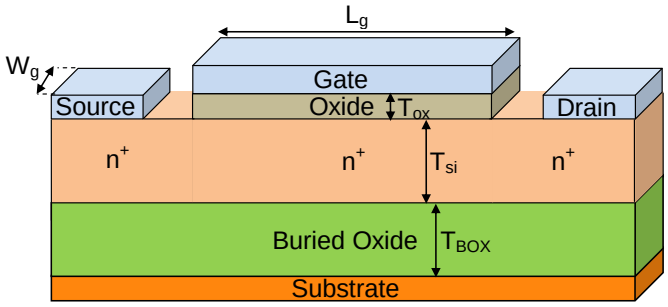

Fig. 1.10: Schematic view of *n*-type Junctionless (JL) transistor realized with uniformly doped Si film [90]. W_g, L_g, T_{ox}, T_{BOX} and T_{si} indicate gate width and length, gate oxide thickness, buried oxide thickness and silicon film thicknesses, respectively.

All the previously proposed transistors architectures were based on the fabrication of junctions between source/drain and channel regions. These junctions in the transistors are useful as they facilitate the flow and cut-off the charge carriers in the transistor, depending on the applied biases. However, with the miniaturization in gate length, it becomes extremely

difficult to design ultra-sharp junctions due to the presence of high doping concentration gradient that are difficult to control at small dimensions. In 2010, Colinge *et al*. [90] fabricated a transistor which eliminates the need of fabricating any junction, and hence, named it as Junctionless (JL) transistor. The schematic of the same is shown in Fig. 1.10. Also, due to the absence of gradient in the doping concentration between source/drain and channel, JL devices do not require the need for costly ultrafast annealing techniques, and thus, allow to fabricate devices with shorter gate length [90]. Despite being free from junctions, these transistors have shown full CMOS functionality [90]. The two constraints while fabricating JL transistor are the formation of a semiconductor region should be thin and narrow enough to allow for full depletion of carriers when the device is turned off, and the semiconductor film needs to be heavily doped to allow for a reasonable amount of current flow when the device is turned on [90]. Thus, the aforementioned two constraints suggest the use of nanoscale dimensions along with heavily doped channel while designing JL devices. In addition, JL transistors are normally on devices, a *p*-type (*n*-type) gate electrode workfunction for *n*-type (*p*-type) JL is needed to deplete the heavily doped channel at lower gate voltages (off-state) [90].

A unique feature of JL transistor is the location of subthreshold conduction channel. While the carriers are confined at the Si-oxide interface in conventional FETs, the subthreshold conduction is located in the bulk of the film in JL devices [90]. Thus, the carriers in JL devices are relatively immune towards the surface roughness scattering [91-92] and degradation in the device performance due to presence of traps at the oxide-semiconductor interface [91-92]. As conduction channel is located in the bulk of the film, corner effects due to higher electric field at the apex of Si channel is relatively lower in JL transistor in comparison to inversion mode counterparts [93]. In addition, while analyzing the performance of short channel JL devices, Lee *et al*., [94] have shown that these heavily doped transistors exhibit higher effective channel length in comparison to inversion

mode device and are relatively immune to SCEs [94]. Park *et al*., [95] have demonstrated that JL devices have showcased less mobility degradation due to transverse electric field in comparison with their inversion mode counterparts [95].

As JL devices are designed with heavily doped channel (~ 10^{19} cm^{-3}), transistor characteristics, threshold voltage, off-current, and DIBL can vary for a slight change in device parameters, and increases the variability in the device [96]. In order to overcome the variability issues in JL devices, core-shell doped JL devices have been have been investigated [97-99]. While the Random Dopant Fluctuation (RDF) is a critical issue [100] in JL devices, authors in [101] have showed that Ge due to its high permittivity can reduce the influence of RDF in JL devices [101]. Also, various research groups attempted to model the behavior of JL devices [102-107]. Authors in [102] have proposed full drain current model for double gate long channel JL MOSFETs [102]. In addition, Sallese *et al*., have developed charge based bulk current model [103]. Few other research groups have proposed models for subthreshold region and threshold voltage in short channel junctionless transistors [104-105]. Furthermore, the gate underlap dependent short channel performance of DG JL devices has also been modeled in [106-107].

Considering the unique features associated with JL transistors, these devices have extensively evolved for various applications such as analog/RF [108-109], biosensing [110], ultra-low power [111-112], dynamic [113-117] and non-volatile memories [118-119]. An important attribute of JL transistor is the occurrence of impact ionization induced FBEs which actuates a positive feedback mechanism and results in sharp rise in drain current with *S*-swing ~ 1 mV/decade [120-127]. The steep switching mechanism was first demonstrated by Lee *et al*., [120] in tri-gate JL devices at a relatively lower drain bias (~ 2 V) in comparison to inversion mode devices [120]. As the performance of previously proposed IMOS device is deteriorated due to the change in threshold voltage and the subsequent degradation in *S*-swing as the

device is stressed by repeated measurements [122]. However, authors in [114] have experimentally shown that a JL device has good device reliability and does not show much change in off-current, threshold voltage and *S*-swing values due to multiple measurements of transfer characteristics [122]. Moreover, it was reported that the device degradation due to hot carrier effect in IMOS transistor can be reduced using DIMOS transistor [122]. However, the applied drain bias in IMOS and DIMOS cannot be reduced below 5 V to facilitate impact ionization induced steep current transition [79] [86] [89]. Also, extremely thin film (~ 0.65 nm) gate-all-around JL devices achieves *S*-swing ~ 43 mV/decade due to BTBT as the conduction mechanism [128]. Therefore, JL transistor can be considered as a possible candidate for achieving a steep increase in drain current at relatively lower drain biases.

1.5 Organization of Thesis

The research work in this thesis has focused on feasibility assessment of steep switching in silicon and germanium junctionless transistor for low power applications. A systematic study has been made to present insights into the understanding of physical mechanisms governing II and various attributes related with junctionless transistors. The primary objective of the thesis is to highlight device architectures that facilitate downscaling of applied voltages while preserving the effectiveness of II induced FBEs to trigger a sharp rise in current from off-state to on-state. The significance of device topology, channel material and various parameters has been evaluated. The optimal design has shown impact ionization induced sharp current transition with *S*-swing < 5 mV/decade along with an increased number of decades of drain current transition from off-to-on state can be achieved at relatively lower supply voltage of 0.9 V-1 V. The thesis presents an advancement in JL transistor designed specifically for logic applications while progressing from Si as channel material to Ge based JL devices. The concept, design and working of JL architecture provide valuable viewpoints for enhancing impact generation process, at relatively lower applied voltages, to achieve sub-60

mV/decade switching action. The thesis is organized into five chapters, and the organization of the same is described below in brief.

Chapter 1 describes the switching action of the transistor and highlights the challenges associated with the downscaling of inversion mode devices. The investigation lays emphasis on emerging transistor architectures to overcome the problems associated with inversion mode devices, and discusses the need of designing sharp switching transistors to achieve energy efficient operation for logic applications. An extensive literature review on the advantages and limitations of the various device architectures proposed to achieve subthreshold swing lower than 60 mV/decade is discussed. Among various steep switching devices, junctionless transistor has shown promising results and the potential to achieve steep switching at relatively low voltages, and therefore, the thesis explores junctionless transistors to achieve the sharp switching in drain current from off-to-on state.

Chapter 2 provides insights into the understanding of physical phenomenon occurring in the device which influences steep current transition from off-state (low current) to on-state (high current) for a smaller gate bias interval. As sidewall spacer and high-permittivity (high-κ) gate dielectric have become inevitable in nanoscale MOSFETs, the same can be utilized to modulate current density and electric field at the gate edge towards the drain as it affects the degree of II, and hence, the extent of steep switching. Therefore, the work describes that an appropriate selection of sidewall spacer material/thickness can significantly enhance the degree of II induced FBEs to achieve steep current transition with *S*-swing < 5 mV/decade at sub-bandgap drain bias. Also, chapter 2 reports on misaligned back gate JL structure, traditionally considered detrimental for device design, as an advantage for achieving *S*-swing ~ 1 mV/decade with an increased number of decades of drain current transition at threshold at supply voltage of 0.9 V .

Chapter 3 extends the discussion on sub-Boltzmann switching in Si and Ge JL transistor through the identification of anomalous behavior of (i) threshold

voltage with temperature and (ii) negative value of total gate capacitance at gate bias corresponding to steep drain current transition. The work shows the occurrence of positive and negative temperature coefficients of threshold voltage resulting from the two contrasting physical effects and their dependence on temperature. Another important attribute of impact ionization induced bipolar effects is the occurrence of hysteresis effect along with negative values of total gate capacitance. While hysteresis effect is beneficial for designing dynamic random access memories, the ambiguity lies in defining threshold voltage for forward and reverse sweep of gate voltages, for logic applications. Therefore, an independent gate operation of JL transistor is proposed to suppress hysteresis effect in Si and Ge JL devices while achieving negative value to total gate capacitance depicting drain current transition with *S*-swing ~ 15-20 mV/decade.

Chapter 4 provides an assessment of designing JL transistor with Ge as channel material focusing on the various physical effects that govern the performance of the transistor. Although previously reported results [83] have successfully demonstrated the advantages of designing Ge based steep switching devices, the supply voltage being greater than 1 V suggest II non-conducive for logic applications. Also, the higher V_{ds} needed to trigger II results in an increased Band-to-Band Tunneling (BTBT) of electrons (for *n*MOS devices) from channel to drain which is accompanied by an undesirable increase in off-current. Therefore, a methodology is proposed, based on the optimization of *J.E*, to sustain II in the semiconductor film at a lower V_{ds} while limiting the off-state BTBT.

In addition, chapter 4 highlights that at the level of device architecture, the degree of II can be improved by increasing the area using a Raised Source/Drain topology in JL transistor. The presence of single transistor latch effect is shown as a limitation, resulting from enhanced degree of II, where the transistor cannot be turned off even for reducing the gate voltage to negative values, and therefore, a systematic approach of independent gate

operation has been discussed to regain the transistor steep switching action by overcoming latch effect while preserving the *S*-swing < 10 mV/decade.

Chapter 5 summarizes the conclusion of the thesis and proposes scope for future work.

1.6 References

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Chapter 2

Steep Switching in Junctionless Transistors

2.1 Introduction

The push towards an energy efficient near-perfect switch, often characterized by very low current in the off-state and high current in the on-state, has resulted in the development of various transistor architectures [1-35]. This transition from off-state to on-state in a MOSFET is usually characterized by a value of *S*-swing < 60 mV/decade at *T* = 300 K [34-35]. However, at lower gate lengths, *S*-swing value further increases and hinders the operation of MOSFETs as a switch for logic applications [5]. Thus, to improve the switching characteristics, various transistor architectures such as TFETs [1-7], FBFET [8-9], Z^2FET [10-11], NCFET [12], NEMS [13], and II [14-32] based devices have been proposed in the literature.

Among all the previously proposed steep switching devices, II based transistors, achieving *S*-swing < 10 mV/decade, have considerably evolved over the past years [14-32]. However, the requirement of higher drain bias (> 1V) to trigger II limits its usage in emerging CMOS technology [14-32]. The conventional theory has suggested that a drain bias at least equivalent to the energy bandgap (E_g) of channel material should be applied to trigger II in field effect transistors [36-37]. Considering the same, a voltage of ~ 1.0 V and ~ 0.7 V for Si and Ge, respectively, should be sufficient to activate II. However, to preserve the effectiveness of II to achieve *S*-swing < 60 mV/decade, relatively higher drain bias is needed [36-37]. Lee *et al*. [27] have demonstrate that JL devices [27] facilitate II induced sharp rise in drain

current at relatively lower drain bias (~ 2.2 V) in comparison to inversion mode devices (~ 5 V). However, the requirement of supply voltage ~ 2.2 V [27] does not make II conducive for CMOS downscaling.

In order to gain advantage from II induced steep drain current transition, approaches that facilitate scaling down of applied voltages while preserving the effectiveness of II are required. Therefore, this chapter describes the different approaches to enhance II, and has been categorized into two sections:

i. The first section (Section 2.3) discusses the impact of sidewall spacer material/thickness, and gate dielectric material on the impact generation phenomena in symmetric Double Gate (DG) JL MOSFETs. Results presented show that the appropriate selection of sidewall spacer material/thickness and gate dielectric enhances the degree of II at relatively lower drain bias while preserving the planar transistor topology.

ii. The second section (Section 2.4) demonstrates the methodology to augment II through the transformation of conventionally unfavorable attribute i.e. back gate misalignment. A complete misalignment in the back gate with respect to front gate towards the drain side causes redistribution of electric field in the film and results in an inclined conduction channel. This enhances the degree of II at relatively lower drain bias and achieves increased number of decades of drain current (*S*-swing ~ 1 mV/decade) transition at threshold.

2.2 Simulation Methodology

Device analysis has been carried out using Atlas [38] simulation software. The work throughout the thesis is based on JL transistor with II being utilized for steep switching mechanism. Thus, it is necessary to analyze II model used by simulator [38]. The II model, assume that ionization at any particular point within the device is a function of the electric field (*E*) [38].

While ionization coefficients are dependent on the electric field (E), the Generation (G) rate of carriers is given by [38] as

$$G = \alpha_n J_n + \alpha_p J_p \tag{2.1}$$

where G is local generation rate, α_n and α_p are ionization coefficients for electrons and holes, respectively. J_n and J_p are the current densities associated with the electrons and holes, respectively.

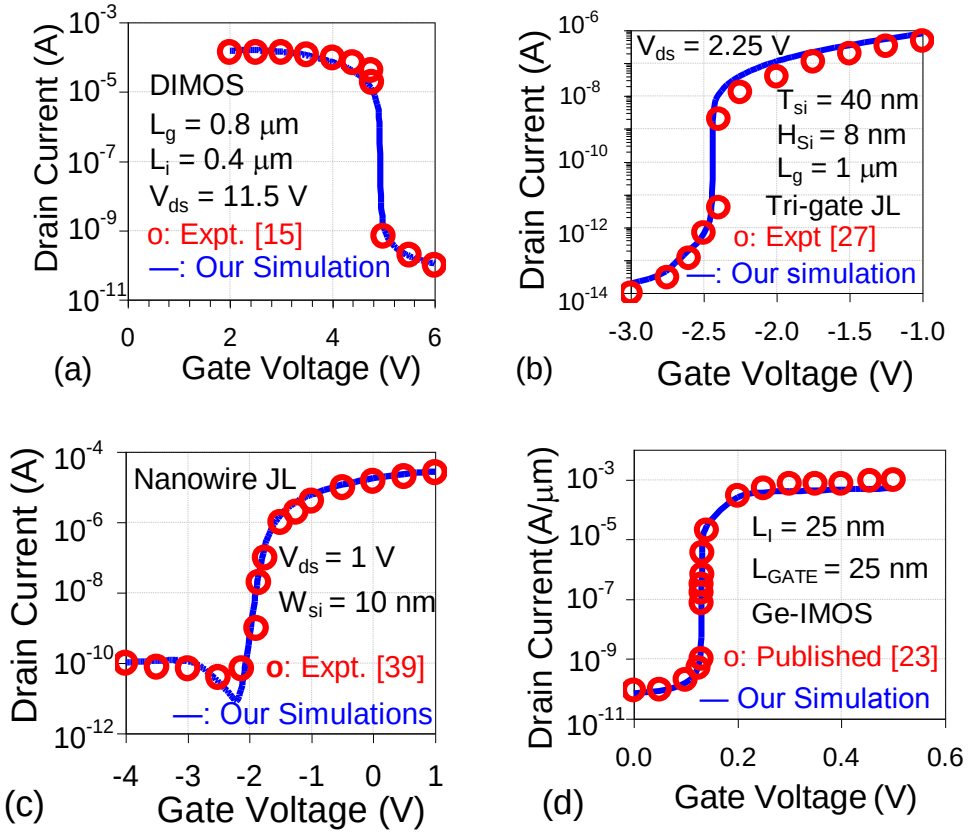

Fig. 2.1: Comparison of our simulated drain current - gate voltage characteristics for (a) DIMOS [15], (b) tri-gate JL [27], (c) nanowire JL [39] and (b) Ge IMOS at V_{ds} = 1 V [23] transistor with published data.

In order to model the impact generation phenomena, a local electric field model given by Selherberr's has been used in the analysis. The accuracy of this model has been previously reported by various research groups [15-16] [20-23] [27] [30]. The other models used while analyzing the performance of

JL transistors include Shockley Read Hall (SRH) and Auger recombination model [38], Lombardi mobility model [38] along with modules of bipolar and bandgap narrowing [38]. All models used in the simulations were calibrated to capture the essential physics of JL (tri-gate and nanowire) transistors [27], [39]. Moreover, to validate the models used to capture II, the calibration was carried out by comparing our simulation results with the published experimental data for transistor architectures such as DIMOS (Fig. 2.1*a*) [15], tri-gate JL (Fig. 2.1*b*) [27] work on the phenomena of II and show a steep rise in drain current [27]. In addition, the applicability of selected models is further confirmed on a non-II exhibiting JL topology i.e. nanowire JL (Fig. 2.1*c*) transistor [39]. As research work carried out in the thesis also explores the assessment of steep switching in Ge JL transistor, the ionization coefficient [40-41] and mobility parameters [42] were taken from the published data. The validity of the parameters chosen for analyzing Ge based JL transistor has been confirmed by comparing our simulations results obtained for IMOS (Fig. 2.1*d*) [23] transistor with published data. Incorporation of all the models discussed in this section lead to a systematic analysis, illustrating various and unique attributes of steep switching Si and Ge JL transistor, which will be discussed in the subsequent sections.

2.3 Sidewall Spacers and Gate Dielectric Optimization for Steep Switching in JL Transistors

As the transistor dimensions have aggressively scaled down to nanoscale regime, the optimization of sidewall spacer and high-κ gate dielectric in MOSFET architecture for superior transfer characteristics has become inevitable. As the prime location of II in the transistor is at the gate edge towards the drain side [27], the properties of sidewall spacer and gate dielectric will substantially affect the degree of II, and thereby, results in steep *S*-swing exhibited by the device. Therefore, it is imperative to revisit the functionality of sidewall spacers and gate dielectric for designing steep switching JL transistor for logic applications.

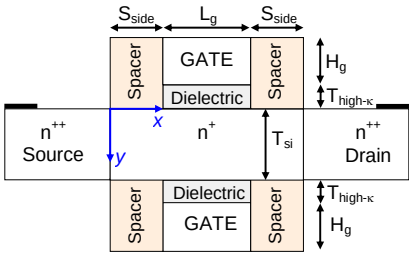

Fig. 2.2: Schematic view of a DG JL transistor. Parameters: L_g = 50 nm, T_{si} = 10 nm N_d = 10^{19} cm^{-3}, H_g = 50 nm, V_{ds} = 0.9 V and Source/Drain doping (N_{SD}) is fixed at 10^{20} cm^{-3}.

2.3.1 Device Structure and Analysis

In order to analyze the influence of sidewall spacer and gate dielectric thickness on *S*-swing, DG Si JL MOSFETs shown in Fig. 2.2 has been analyzed with channel doping 10^{19} cm^{-3}. In addition, the impact of spacer and gate dielectric material (permittivity, κ) on *S*-swing of the transistor has been investigated. Source/Drain regions were additionally doped (N_{SD}) with 10^{20} cm^{-3} to minimize series resistance effect. The width of sidewall spacer (S_{side}) was varied from 10 nm to 20 nm. The analysis has been performed with different dielectric materials, namely, silicon dioxide (SiO_2, $\kappa = 3.9$), silicon nitride (Si_3N_4, $\kappa = 7.5$), aluminum oxide (Al_2O_3, $\kappa = 9.3$), hafnium silicate ($HfSiO_4$, $\kappa = 12$) and hafnium dioxide (HfO_2, $\kappa = 22$). The oxide thickness of gate dielectric (κ_{Gate}) was taken as 1 nm for SiO_2, 1.92 nm for Si_3N_4, 2.38 nm for Al_2O_3, 3.08 nm for $HfSiO_4$ and 5.6 nm for HfO_2, all corresponding to an Equivalent Oxide Thickness (EOT) of 1 nm. Quantum effects will not be significant as considered film thickness > 7 nm [43-44].

2.3.2 Impact of Sidewall Spacer Material on S-swing

Achieving II induced steep *S*-swing values in JL devices requires the optimization of (i) S_{side} and κ_{Spacer} and (ii) κ_{Gate}. As shown in Fig. 2.3*a*, sidewall spacer influences the lateral extension of the depletion region beyond the gate edge and impacts the effective channel length (L_{eff}) in subthreshold region. A HfO_2 spacer allows for a greater penetration of

fringing field and extends the depletion beyond the gate edge to a wider region as compared to the spacer designed with SiO_2, thus leading to L_{eff2} (for HfO_2 spacer) > L_{eff1} (for SiO_2 spacer) [45]. The wider depletion width for a high-κ spacer material indicates a lower electron concentration (n_e) and reduced current density, an important parameter that governs the II in the film, is exhibited by the structure.

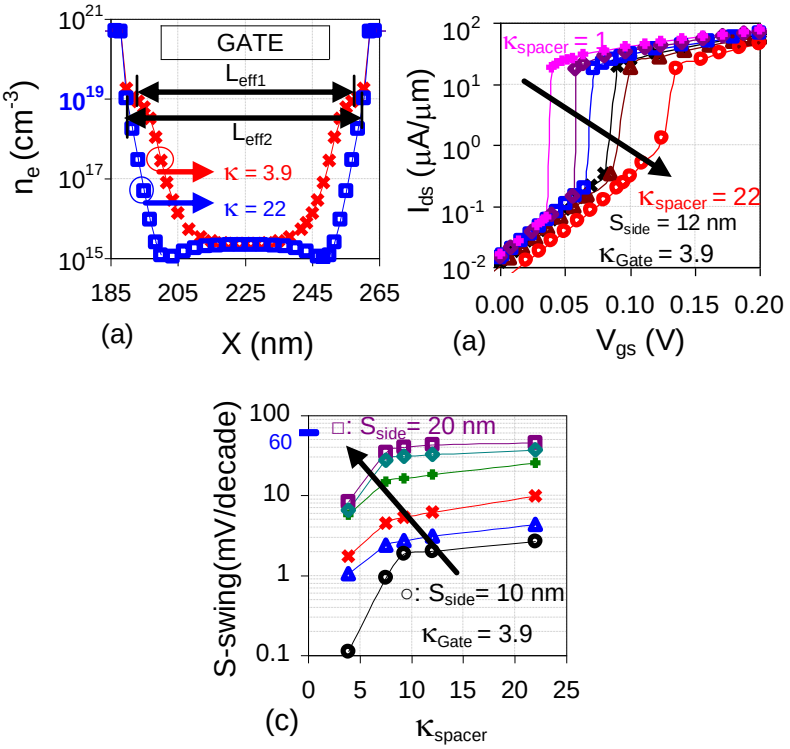

Fig. 2.3: (a) Variation in electron concentration (n_e) at the center ($y = T_{si}/2$) of the film along the channel direction (x-axis) at $V_{gs} = V_{ds} = 0$ V. (b) Drain current (I_{ds}) - gate voltage (V_{gs}) characteristics for different κ_{spacer}. (c) Variation in S-swing with κ_{spacer} and S_{side} for fixed $\kappa_{Gate} = 3.9$.

Fig. 2.3*b* shows the drain current (I_{ds}) – gate voltage (V_{gs}) characteristics as a function of κ_{spacer}. JL transistors designed with low permittivity (κ_{spacer} = 3.9) spacer achieve steep S-swing (~ 1 mV/decade) values in comparison to devices designed with high-κ material (κ_{Spacer} = 22) which yields nearly 4 times higher S-swing (4 mV/decade). Since S-swing ~ 1 mV/decade in JL device designed with κ_{spacer} = 3.9, further lowering the spacer dielectric will

result in a marginal change in *S*-swing values. However, the enhanced degree of impact ionization will manifest in the lower values of gate voltage at which steep transition can be observed along with in higher number of decades of I_{ds} transition at threshold voltage (V_{th}). Sidewall spacer with high-κ material allows the fringing component of the vertical electric field to influence the channel potential and reduces the lateral field associated with the drain, which lowers the degree of II and the steepness of the corresponding I_{ds}-V_{gs} characteristics. Moreover, the reduced degree of II can also be seen in the increase in V_{th} from 72 mV to 0.14 V with a change in κ_{Spacer} from 3.9 to 22, respectively. For steep switching devices, V_{th} is defined as the gate voltage at which I_{ds} increases sharply. As shown in Fig. 2.3*c*, the selection of SiO_2 as the sidewall spacer material is advantageous as *S*-swing is limited to ~10 mV/decade for a variation in S_{side} from 10 nm to 20 nm. However, *S*-swing degrades from ~2 mV/decade (S_{side} = 10 nm) to 45 mV/decade for S_{side} = 20 nm in JL transistor design HfO_2 spacer. As the penetration of the fringing component of gate field is dependent on the S_{side}, a wider high-κ spacer allows greater influence of the gate field into the channel resulting in relatively higher *S*-swing values albeit lower than 60 mV/decade.

2.3.3 Impact of Gate Dielectric Material on S-swing

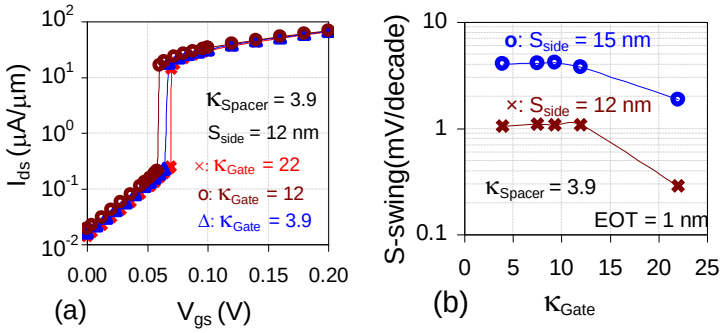

Fig. 2.4: (a) I_{ds}-V_{gs} characteristics for different κ_{Gate} materials at a fixed S_{side} = 12 nm and κ_{Gate} = 3.9, and (b) dependence of *S*-swing on κ_{Gate} for S_{side} = 12 nm and 15 nm.

As shown in Fig. 2.4*a*, I_{ds}-V_{gs} characteristics do not show an appreciable change in *S*-swing with κ_{Gate} for S_{side} = 12 nm and 15 nm as the use of

different materials for the same EOT maintains almost constant vertical gate field. The same is also reflected in Fig. 2.4*b* where *S*-swing marginally reduces from 4 mV/decade to 2 mV/decade with a change in gate dielectric material from SiO_2 (κ_{Gate} = 3.9) to HfO_2 (κ_{Gate} = 22). A high-κ gate dielectric corresponding to a thicker gate dielectric ($T_{High\text{-}\kappa}$) has a weaker control over the channel as the most of the fringing field lines terminate on the source/drain regions in comparison to a thinner gate dielectric (κ = 3.9) [46]. The weaker gate control allows for enhanced influence of the lateral electric field which assists II and results in relatively steeper *S*-swing. Results presented in Fig. 2.3 and Fig. 2.4 conclusively demonstrates that the choice of spacer width and material are important considerations to achieve steep current transition in JL devices.

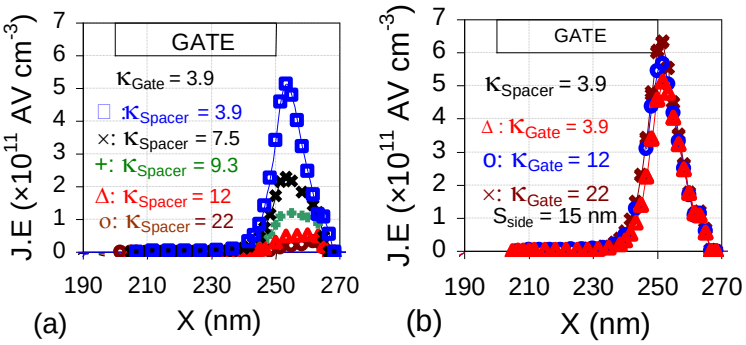

Fig. 2.5: Variation in product of current density (*J*) and electric field (*E*) i.e. *J.E* along the channel direction (*x*-axis) at the center of the film ($y = T_{si}/2$) for different (a) spacer with κ_{Gate} = 3.9 at V_{gs} = 0.12 V, and (b) gate dielectric material with κ_{spacer} = 3.9 at V_{gs} = 0.12 V. The results are obtained at V_{gs} = 0.12 V for S_{side} = 15 nm.

A major bottleneck, particularly for II, has been the unavailability of methodologies to enhance the degree of II in a transistor. Even the conventional theory suggests that an increase in lateral electric field via the increase of drain bias augments II. However, it is not just the electric field (*E*) but the product of current density (*J*) and electric field i.e. (*J.E*) that actually governs the impact generation phenomena [47]. As the ionization coefficients

for electrons (α_n) and holes (α_p) depend on the electric field [37], *J.E* provides a measure of II generated power per unit volume in the device [47]. Therefore, it will be worthwhile to investigate the product (*J.E*) to assess the feasibility of the sharp current transition through II at a drain bias near to bandgap of the semiconductor. Fig. 2.5*a* shows the variation of the *x*-component of (*J.E*) extracted at the center of the silicon film ($y = T_{si}/2$) along channel direction as a function of κ_{spacer}. The other parameters such as S_{Side} and κ_{Gate} are fixed at 15 nm and 3.9, respectively. A higher value of *J.E* signifies enhanced II, and hence, a steeper *S*-swing. An increase in κ_{Spacer} results in a lowering of *J.E* values which is responsible for a reduction in the degree of II and an associated degradation in *S*-swing as shown in Fig. 2.3*c*. The location of peak value of *J.E* i.e. $(J.E)_{max}$ also shifts away from the gate edge along with the reduction in magnitude with an increase in κ_{Spacer}. This is due to the increased contribution of fringing component of the vertical electric field via spacer region which shifts $(J.E)_{max}$ values away from the gate edge towards the drain.

The impact of gate dielectric on *J.E* product is shown in Fig. 2.5*b*. A gate dielectric with a high-κ material results in maximum *J.E* and minimum *S*-swing as shown in Fig. 2.4*b*. Results shown in Fig. 2.5 depicts that κ_{Spacer} is more critical as compared to κ_{Gate} as a greater reduction (~ an order) in the values of *J.E* is observed (5.1×10^{11} AVcm^{-3} to 0.4×10^{11} AVcm^{-3}) with κ_{Spacer} as compared to a much lesser variation in *J.E* (6.3×10^{11} AVcm^{-3} to 4.8×10^{11} AVcm^{-3}) with a change in κ_{Gate}. The lower variation in $(J.E)_{max}$ for different κ_{Gate} indicates a lesser impact on *S*-swing values, an observation consistent with the results in Fig. 2.4.

2.3.4 Optimized JL Transistor

Fig. 2.6*a* highlights the design constraints and guidelines associated with S_{side} and κ_{Spacer} for two different EOT values. The curve for each EOT reflects the maximum allowed value of S_{side} for a given κ_{Spacer} to achieve *S*-swing ~

10 mV/decade. If S_{side} is limited to 10 nm to 14 nm for EOT = 1 nm, then a larger range of κ_{Spacer} is useful for achieving the target *S*-swing. If sidewall spacer is to be designed with SiO_2, then the spacer width is not critical for achieving steep *S*-swing. However, considering a case with Si_3N_4 sidewall spacer, S_{side} should be lower than 14 nm for obtaining *S*-swing of 10 mV/decade. As a thicker EOT allows for a reduction in vertical electric field, a device with EOT = 1.4 nm facilitates a greater degree of freedom in the selection of parameters related to spacer for the desired *S*-swing value.

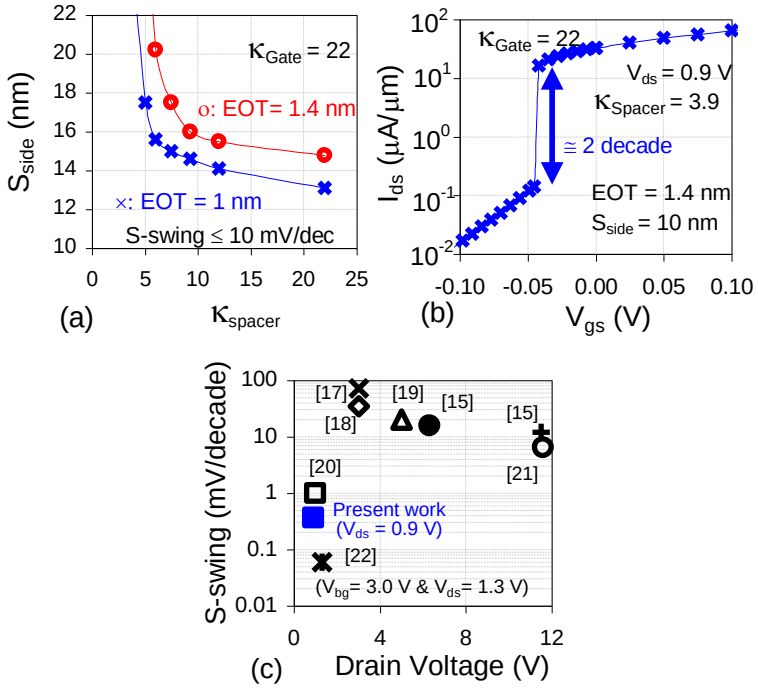

Fig. 2.6: (a) Design constraints associated with S_{side} and κ_{Spacer} required to achieve an *S*-swing ≤ 10 mV/decade. (b) I_{ds}-V_{gs} graph for an optimized sidewall spacer and gate dielectric in JL MOSFET at V_{ds} = 0.9 V at 300 K. (c) Comparison of *S*-swing and V_{ds} (absolute) values published in the literature [15, 17-22] with our result for optimized JL MOSFET. Reference numbers [15, 17-22] are marked against each data point in Fig. 2.6*c*.

Fig. 2.6*b* shows the I_{ds}-V_{gs} characteristics of the optimum device at a V_{ds} of 0.9 V for symmetric gate operation. A very steep *S*-swing ~ 0.12 mV/decade is exhibited by the optimum device designed with EOT of 1.4 nm

with κ_{Gate} = 22 nm and S_{side} =10 nm with κ_{Spacer} = 3.9. Fig. 2.6*c* compares *S*-swing and drain voltage (absolute) values reported in literature [15, 17-22] depicting sub-60 mV/decade off-to-on transition utilizing II in different MOSFETs. The result for JL transistor exhibiting *S*-swing of < 1 mV/decade at V_{ds} = 0.9 V through the optimization of sidewall spacer and gate dielectric represents the minimum *S*-swing value reported at relatively lower V_{ds}. Thus, results highlight that the greater consideration must be taken into account for spacer designing for accomplishing steep *S*-swing JL devices.

2.3.5 Effect of Temperature on S-swing

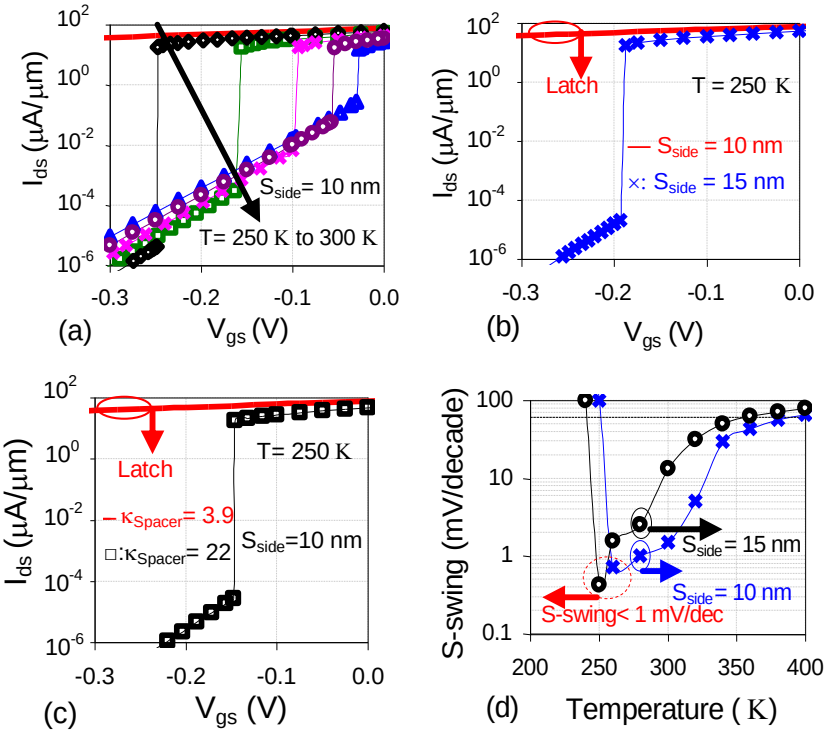

Fig 2.7: I_{ds}-V_{gs} characteristics as a function of (a) temperature (*T*), (b) S_{side} at *T* = 250 K with κ_{Spacer} = 3.9, and (c) sidewall spacer permittivity at *T* = 250 K. (d) Dependence of *S*-swing on temperature for of S_{side} = 10 nm and 15 nm with κ_{Spacer} = 3.9. All the results are shown for JL device with κ_{Gate} = 22.

As JL devices exhibits enhanced degree of II, the parameters for the sidewall spacer should be carefully selected for the intended temperature range of operation to avoid both extremes, i.e. latching effect at lower

temperatures and the reduction in the degree of impact ionization at higher temperatures. This section provides insights into the physical phenomena governing the functionality of steep switching JL transistor over the wider range of temperature. I_{ds}-V_{gs} characteristics for an optimized JL transistor (low-κ sidewall spacer and high-κ gate dielectric) as a function of temperature (T) are shown in Fig. 2.7*a*. At lower temperatures (T = 250 K), the device latches to the on-state and cannot be turned off, even for negative values of the applied gate voltage as the carriers generated due to II cannot be depleted. This condition is also known as the single transistor latch [47].

The impact ionization in a device is governed by the product current density and electric field ($J.E$). The current density through the semiconductor film is a function of mobility which depends on the different scattering mechanisms. At T = 250 K, due to lower thermal vibrations of lattice atoms, the degradation in carrier mobility owing to phonon scattering is less severe [48]. Hence, the improvement in mobility values at T = 250 K contributes to the increase in current density, and thus, the product ($J.E$) is enhanced. A higher value of $J.E$ significantly supports II and results in generation of more electron-hole pairs, which under extreme conditions cannot be depleted to turn-off the device. A possible solution to turn-off the device from the latched on-state is to utilize either a low-κ sidewall spacer with S_{side} = 15 nm (Fig. 2.7*b*) or a high-κ sidewall spacer with S_{side} = 10 nm (Fig. 2.7*c*). Fig. 2.7*b* compares I_{ds}-V_{gs} characteristics for a JL transistor with a low-κ sidewall spacer with thickness S_{side} = 10 nm and 15 nm, while Fig. 2.7*c* illustrates the impact of spacer permittivity at T = 250 K. The presence of a wider (S_{side} = 15 nm) or a high-κ sidewall spacer allows the penetration of fringing field lines from the gate which modulates the channel potential and diminishes the lateral electric field associated with drain, and reduces the strength of II, thereby facilitating the depletion of carriers and the turning off the device at lower gate voltages.

The dependence of *S*-swing for an optimized JL transistor on temperature is shown in Fig. 2.7*d* for S_{side} = 10 nm and S_{side} = 15 nm. The transistor latches to the on-state for sidewall spacer widths of 10 nm and 15 nm, and it cannot be turned off for the negative values of gate voltage for T < 250 K. An increase in temperature (> 300 K) reduces the impact generation rate and the number of decades of transition in the drain current. Any further increase in temperature beyond 300 K results in a degradation of *S*-swing with its value approaching the classical limit due to an increase in the phonon scattering of carriers with the crystal atoms [48]. The reduction in the mobility of carriers due to phonon scattering at higher temperature lowers the current density, and consequently *J.E*, which further degrades *S*-swing.

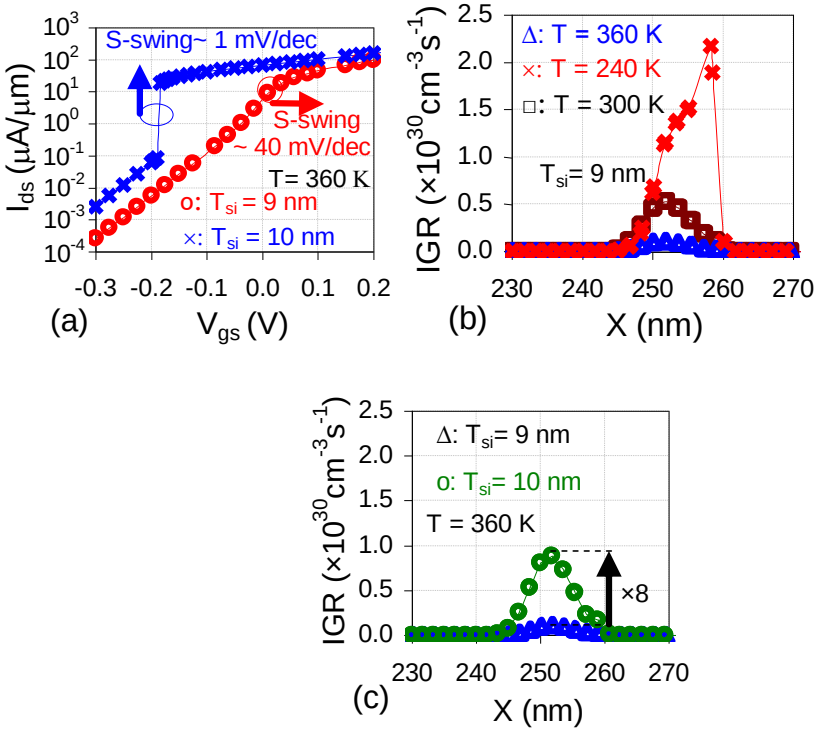

Fig 2.8: (a) I_{ds}-V_{gs} characteristics for different values of film thickness at T = 360 K. Variation in Impact Generation Rate (IGR) (b) with temperature varying from 240 K to 360 K with T_{Si} = 9 nm and (c) at T = 360 K with T_{Si} = 10 nm. IGR were extracted at the location of conduction channel.

A possible option to overcome the degradation of *S*-swing at a higher temperatures is to reduce the spacer width or to increase the silicon film thickness to facilitate an enhanced degree of II. The technological constraint for the width of the sidewall spacer limits any further reduction (<10 nm) in its value. The other option of increasing T_{si} is more pragmatic and can be utilized if the devices are operated at higher temperatures. It can be seen in Fig. 2.8*a* that a JL transistor with T_{si} = 9 nm exhibits an *S*-swing of 40 mV/decade due to the reduced value of II rates, while a device with T_{si} = 10 nm yields an *S*-swing of ~1 mV/decade. Thus, devices intended to be operated at higher temperatures should be designed with a thicker film thickness, which can be depleted at zero bias condition, to facilitate an enhanced degree of II. Fig. 2.8*b* shows the variation of Impact Generation Rate (IGR) along the center of the silicon film and confirms the reduction in II rates with an increase in temperature for a given T_{si}. At lower temperatures (T = 240 K), IGR is nearly four times higher in comparison to the rates observed at T = 300 K (Fig. 2.8*b*). The extracted IGR (Fig. 2.8*c*) at T = 360 K for T_{si} = 10 nm highlights the applicability of thicker film devices to exhibit an enhanced degree of II which helps in achieving steep *S*-swing values. The peak IGR value at T_{si} = 10 nm is nearly eight times higher than that achieved with T_{si} = 9 nm in JL devices designed with a high-κ gate dielectric and a low-κ narrow sidewall spacer at V_{ds} = 0.9 V. In addition, the results have implications for semiconductors material such as germanium with E_g ~ 0.7 eV along with higher ionization coefficients [23].

2.4 Misaligned Back Gate Junctionless Transistors

2.4.1 Device Structure and Operation

Although an appropriate selection of spacer material and width is beneficial to achieve steep transition in I_{ds} from off-to-on state at relatively lower V_{ds}, the number of decades at steep transition point is limited to 2 at T = 300 K. Therefore, to further enhance II at relatively lower V_{ds}, to achieve sharp transition in drain current along with increased number of decades, a

methodology allowing for the generation of significant number of electron-hole pairs is investigated. While it is desirable that device architecture at nanoscale dimensions should be perfect to yield device performance, some imperfections are bound to exist. An accomplished utilization of one of these traditional imperfections such as misalignment can serve as an opportunity to improve the performance. The misalignment between front and back gates can be used to provide additional degree of freedom in nanoscale regime to achieve steep *S*-swing at lower applied voltages for Si and Ge JL transistors.

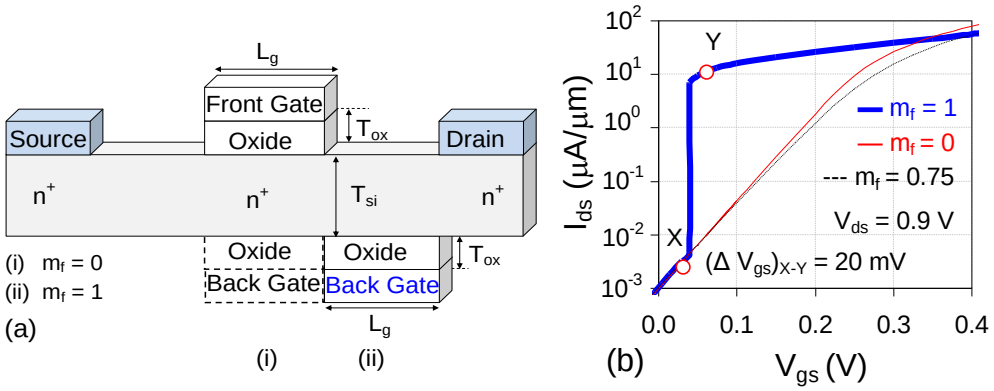

Fig 2.9: (a) Schematic diagram of JL transistor for two different back gate positions (i) aligned back gate (m_f = 0) and (ii) completely misaligned back gate (m_f = 1), (b) I_{ds}-V_{gs} characteristics for symmetric (m_f = 0) and asymmetric i.e. m_f = 1 and m_f = 0.75 JL MOSFET at V_{ds} = 0.9V. Parameters: T_{si} = 7 nm, L_g = 50 nm, T_{ox} = 1.5 nm and N_d = 10^{19} cm^{-3}.

Fig. 2.9*a* shows the schematic view of misaligned back gate JL transistor. The asymmetry exists in the relative position of back gate with respect to front gate i.e. back gate is misaligned by a misalignment factor (m_f) which varies from 0 to 1. A value of m_f = 0 signifies perfect alignment, whereas m_f = 1 signifies completely misaligned structure. A complete back gate misalignment towards the drain is considered as it serves as the principle region of interest for the occurrence of II in JL devices. As shown in Fig. 2.9*b*, I_{ds} - V_{gs} characteristics for JL device with m_f = 1 shows a sharp increase (*S*-swing ~1 mV/decade) of nearly 4 orders in drain current from off-to-on state for a 50 mV change in gate bias, whereas structure with a perfectly

aligned back gate (m_f = 0) and partially misaligned back gate (m_f = 0.75) exhibits a classical *S*-swing value of 60 mV/decade and confirms the non-existence of II in the structure. In order to take advantage of low power operation and steep *S*-swing, I_{on} should be defined at lower gate voltage i.e. just after the onset of transition from off-to-on state.

2.4.1.1 Electric Field Distribution

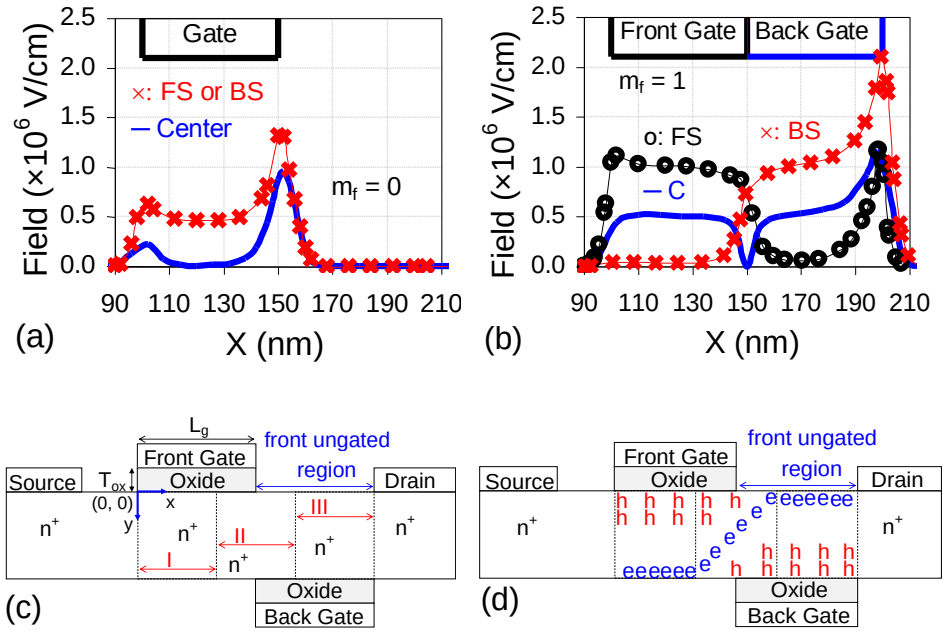

Fig 2.10: (a) Electric field distribution in JL transistor with (a) m_f = 0, (b) m_f = 1 extracted along *x*-axis at front surface (FS i.e. *x*, *y* = 0), center (C i.e. *x*, *y* = T_{si}/2) and at the back surface (BS i.e. *x*, *y* = T_{si}) before the onset of steep current transition i.e. V_{gs} = 30 mV, (c) 2D view of JL transistor with three regions: I, II and III, (d) schematic representation of inclined conduction channel in completely misaligned JL transistor.

In order to understand the conduction mechanism in JL transistor with m_f = 1, electric field is extracted and compared with symmetric gate JL device (m_f = 0). The electric field distribution along the channel direction (*x*) at front (*y* = 0) and back (*y* = T_{si}) surfaces along with at the center (*y* = T_{si}/2) of the film is shown in Fig. 2.10*a* for a JL transistor with m_f = 0. Since the off-current is same, field is extracted at V_{gs} = 30 mV for all devices. This value of

V_{gs} is just prior to the steep transition of drain current and is represented by point X in Fig. 2.9*b*. The region where electric field is minimum denotes the location of the conduction channel i.e. maximum concentration of electrons, which in perfectly aligned JL transistor, are present at the center of the silicon film. In order to initiate II to attain a low value of *S*-swing at lower V_{ds}, higher degree of collisions can be achieved by altering the electric field distribution in the semiconductor film.

It is suggested that instead of increasing the lateral field through an increase of V_{ds}, an electric field redistribution through the gate misalignment facilitates movement of carriers in lateral as well as vertical direction so as to enhance II through greater number of collisions. The misalignment between front and back gate in practical devices can be achieved by intentional shifting the electrical vernier as demonstrated by Widiez *et al*., [49]. The approach also permits the shifting of back gate in totality with the assistance of the electron beam position accuracy. While misalignment has been investigated for the loss of controllability over the conduction channel [50-51] and its effect on analog performance [52-53], it also acts as an effective approach to activate II at lower supply voltages.

As shown in Fig 2.10*b*, back gate misalignment results in a significant change in distribution of field within the semiconductor film. In order to understand the electric field in JL device with $m_f = 1$, the semiconductor film underneath the gates is divided into three regions (region I, II and III in Fig. 2.10*c*). Analyzing the region near to the front gate edge towards the source (region I), the high value of electric field at the front surface ($y = 0$) and at the center ($y = T_{si}/2$) of the semiconductor film indicates the absence of conducting channel (electrons). As the electric field is minimum at the back semiconductor surface ($y = T_{si}$) exactly below the front gate, the electrons are pushed away from the front surface and are located at the back surface. At the common edge of front and back gates in region II, the electric field is high at front and back surfaces while it is minimum at the center of the film ($y =$

$T_{si}/2$). This reflects on the location of conduction channel (electrons) at the center of the semiconductor film underneath the front gate edge towards the drain. Analyzing the electric field distribution in the semiconductor film (region III) above the back gate indicates that the electric field is minimum at the front surface while it is maximum at the back surface. Therefore, most of the electrons are likely to be at the front surface, exactly opposite to the back gate i.e. in the region between front gate and drain electrodes (region III).

The electric field distribution clearly implies that the conduction channel is not horizontal with respect to *x*-direction, rather, the improvised misaligned structure exhibits an inclined channel. It is important to note that at higher peak electric field at the back semiconductor surface adjacent to the back gate, pushes the electrons (or conduction channel) away from the back gate in the upward direction towards the front ungated surface (in region III). This is schematically represented in Fig. 2.10*d* where the notation 'e' signifies electrons and 'h' implies holes. As electrons move from source to drain, the relatively high electric field at the back surface adjacent to the back gate causes the carriers to shift towards the center and to the front surface i.e. movement along *y*-direction. This push towards the front surface further complements II process, and carriers are now not only driven towards the drain end (lateral direction) due to the applied drain bias, but are also simultaneously pushed towards the surface (vertical direction) which results in triggering of II through the misalignment induced field redistribution. The aforementioned distribution of electric field is unique to the misaligned architecture and not prevalent in any existing topology where either the channel is at the center of the semiconductor film in junctionless devices or spreads out across the volume of the film. As II occurs at the front surface near to the drain for misaligned structure ($m_f = 1$) while it is at the center of the film in symmetric structure ($m_f = 0$), parameters shown in subsequent section have been extracted at the respective locations i.e. front surface for misaligned structure and at center of the film for a self-aligned device.

2.4.2 Location of Conduction Channel in Misaligned JL Transistor

Another interesting consequence of electric field redistribution due to gate misalignment is the improvement in J as shown in Fig. 2.11*a*. Since the back gate is completely misaligned with respect to front gate, the effectiveness of gate to deplete the carriers in the semiconductor film is diminished leading to an associated increase in the electron concentration. This in turn results in a higher current density which is beneficial for II [42].

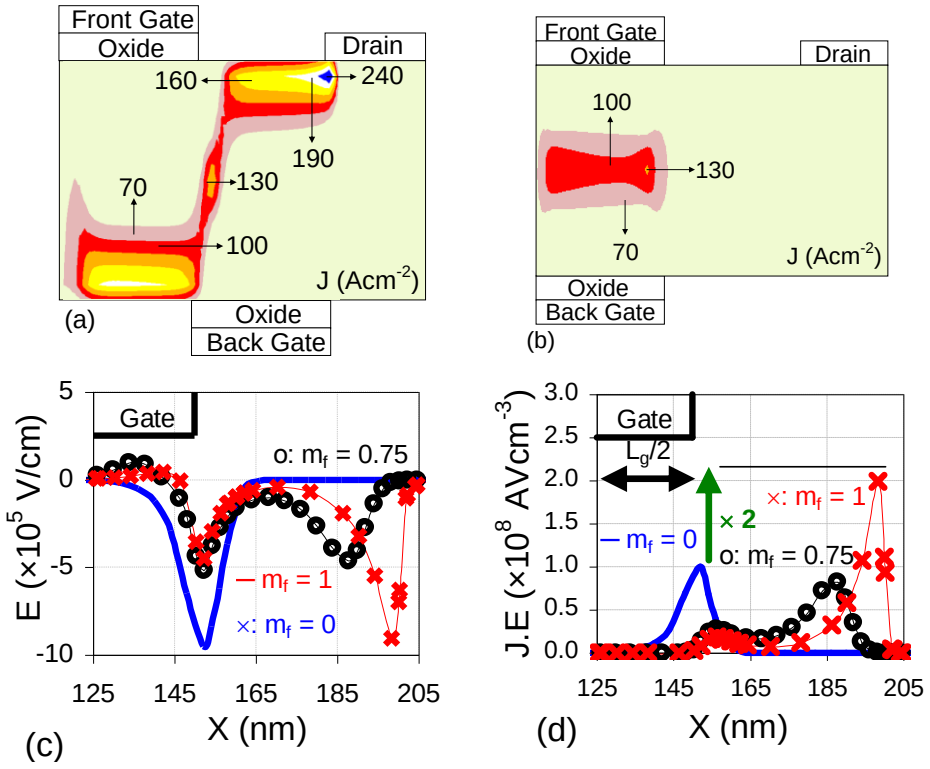

Figure 2.11: 2D contour plot showing current density in JL device with (a) $m_f = 1$ and (b) $m_f = 0$, (c) variation in electric field (E) in JL device for $m_f = 0$, 0.75 and 1, (d) variation of $J.E$ extracted at voltage corresponding to values represented by X and Y in Fig. 2.9*b*. Parameters were extracted along the cut-line (x, $y = T_{si}/2$) for self-aligned ($m_f = 0$) and (x, $y = 0$) for completely misaligned ($m_f = 1$) JL devices.

Fig. 2.11*a-b* shows the 2D contour plot of J just before the onset of steep transition at V_{gs} = 30 mV for completely misaligned (Fig. 2.11*a*) and self-

aligned (Fig. 2.10*b*) JL transistor. As shown in Fig. 2.11*a*, peak value of J for a misaligned structure increases nearly 2 times i.e. from 130 Acm^{-2} (m_f = 0) to 240 Acm^{-2} (m_f = 1). Even for a partially aligned device (m_f = 0.75), an increase in the peak J ~ 170 Acm^{-2} is observed. As shown in Fig. 2.11*c*, back gate misalignment causes a redistribution of the electric field along the x direction with higher values at gate edges. The peak value of electric field is nearly same for m_f = 0 and 1 structures, while it is reduced for a partially misaligned device (m_f = 0.75). The product of J and E shown in Fig. 2.11*d* indicates the effectiveness of completely misaligned structure (m_f = 1) to achieve nearly two times higher values of $J.E$ which is translated into an enhanced II generated power per unit volume and an associated steep S-swing as compared to other device topologies (m_f = 0 and 0.75).

2.4.3 Region of Impact Ionization

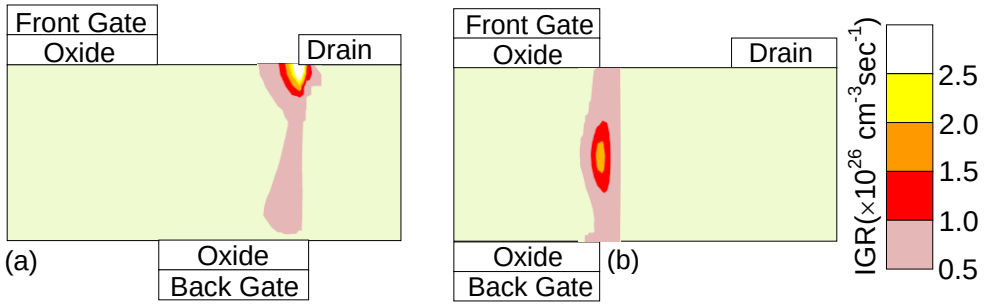

Figure 2.12: 2D contour plot of JL transistor showing IGR in (a) m_f = 1, and (b) m_f = 0 JL transistor at V_{gs} = 30 mV.

Fig. 2.12 shows the 2D contour plot of IGR at V_{gs} = 30 mV for completely misaligned (Figs. 2.12*a*) and self-aligned (Figs. 2.12*b*) JL transistor. The peak value of IGR is observed at front semiconductor surface at the back gate edge towards the drain in misaligned JL devices, whereas in self-aligned structures, II is facilitated at the center of the film at the front or back gate edge. The higher values of IGR exhibited by misaligned structure in comparison to self-aligned junctionless transistor confirm the enhanced degree of II resulting from the redistribution of electrons and holes in the semiconductor film. In addition, an oversized back gate will not be useful for

steep switching applications as it will deplete the back surface of semiconductor film due to high gate workfunction (p^+ poly). The depletion will lower the *J* and reduces product *J.E* which in turn will decrease the degree of II and will not be useful for achieving steep *S*-swing values.

2.4.4 Parasitic Capacitance and S-swing

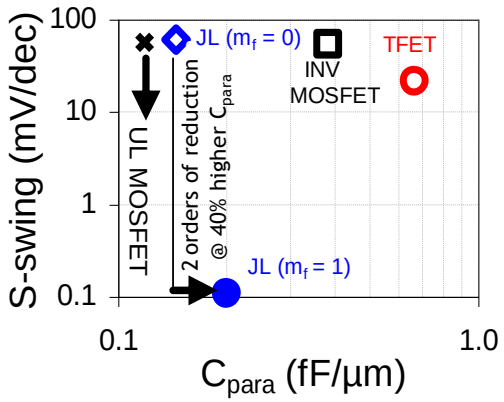

Figure 2.13: Comparison of *S*-swing and parasitic capacitance (C_{para}) values for self-aligned device. Notations: □: Inversion (INV) mode MOSFET, □: Underlap (UL) MOSFET, ◊: JL MOSFET (m_f = 0), o: TFET (with oxide thickness of 2.5 nm) and ●: JL MOSFET with m_f = 1.

A crucial consideration for a completely misaligned (m_f = 1) device is the increase in parasitic capacitance (C_{para}) which may eventually degrade the performance of the device. The data for C_{para} and *S*-swing values shown in Fig. 2.13 are obtained for different MOSFET topologies by simulating the devices with the same set of parameters except for Tunnel FETs (TFETs) where gate oxide thickness was 2.5 nm. A misaligned JL transistor achieves nearly two orders of reduction in *S*-swing but with an overhead of 40% higher C_{para}. Even though 40% high C_{para} is obtained, it is not very significant even for completely misaligned devices as JL topology with the same doping at source, channel and drain region results in the extension of depletion width beyond the gate edge towards source/drain regions, and limits the overall increase of the parasitic capacitance [45]. Tunnel FETs even with low *S*-swing of 10 mV/decade exhibit a high value of parasitic capacitance [54].

2.4.5 Misaligned Back Gate Ge Junctionless Transistor

An interesting application of the misaligned topology can be for Ge based devices which exhibit higher mobility and lower bandgap in comparison to silicon [40]. Using Ge as channel material in junctionless architecture can trigger II at lower supply voltages due to higher current density because of improved mobility [40]. Also, lower bandgap and higher ionization coefficient is beneficial as II can be triggered at lower supply voltages. While Si device can be designed with native oxide of silicon i.e. SiO_2, the native oxide of Ge i.e. GeO_2 is not appropriate for designing of Ge based MOS devices due to its poor intrinsic properties like thermal stability and water solubility [55]. Authors in [55] have highlighted that the problems associated with GeO_2 can be overcome by low temperature plasma nitridation of GeO_2 to form GeON with low (3×10^{11} cm^{-2} eV^{-1}) interface state density, higher dielectric constant (~ 6.5) and improved intrinsic properties [55]. Thus, Ge based JL devices are designed with GeON as gate dielectric.

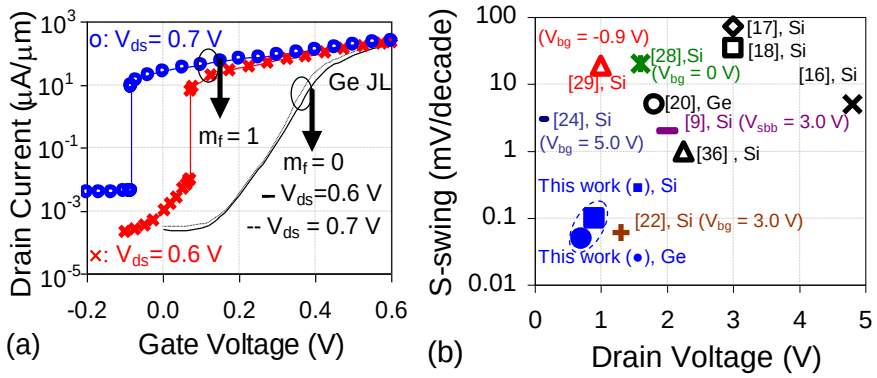

Figure 2.14: (a) I_{ds}- V_{gs} characteristics Ge JL MOSFET (m_f = 0 and 1) at V_{ds} = 0.6 V and 0.7 V. (b) Comparison of *S*-swing values for steep switching devices published in the literature [9], [16-18], [20], [22], [24], [28-29] with misaligned (m_f = 1) Si and Ge JL transistors. The dimensions used in the simulations for Ge JL device were T_{si} = 8 nm, EOT = 1.7 nm, L_g = 50 nm.

Results shown in Fig. 2.14*a*, demonstrate that the occurrence of steep switching at drain bias of 0.6 V ~ 0.7 V in Ge JL transistors with completely misaligned gates (m_f = 1), whereas the *S*-swing near to classical value is

observed in the self-aligned front and back gates (m_f = 0). As Band-to-Band Tunneling (BTBT) from channel to drain will be critical in low bandgap materials such as germanium, the same has been included using local tunneling model through the parameters reported by Kim *et al*. [56]. As seen in Fig. 2.14*a*, the impact of BTBT is more pronounced at higher drain voltages. Even then, the low *S*-swing (~ 1 mV/decade) with a sharp increase in the drain current by 2 to 3 orders at a drain bias of 0.6 V and 0.7 V shows the potential of back gate misalignment in Ge JL transistor for steep switching applications.

Fig. 2.14*b* shows the comparison of our results with published data available in the literature [9], [16-18], [20], [22], [24], [28-29] for steep switching devices. If any published data corresponding to asymmetric operation i.e. different voltages applied to front and back gates is shown, then the same is also mentioned by stating the values of required back bias for lower *S*-swing values. Results exhibiting much lower *S*-swing values due to the intention misalignment at sub-bandgap operating voltages are an improvement over the published data for Si and Ge junctionless transistors. While gate misalignment is traditionally considered as a disadvantage due to the loss of gate controllability over the channel, the double gate architecture with complete misalignment between front and back gates is indeed beneficial in achieving steep transition in drain current in nanoscale devices at sub-bandgap voltages due to the distinctive inclined conduction channel exhibited by the topology.

2.5 Conclusion

The chapter dealt with the detailed analysis for designing sharp switching double gate junctionless transistors at drain bias equivalent to bandgap of the semiconductor. The characteristics such as high current density and wider region over which II is observed in junctionless transistor give rise to enhanced degree of floating body effects at relatively lower drain bias to achieve *S*-swing ~ 1 mV/decade. An insightful evaluation depicts that

the gate dielectric and sidewall spacer material is critical for attaining II induced sub-60 mV/decade steep drain current transition from the off-state to the on-state at relatively lower V_{ds} ~ 0.9 V. Results have shown that the spacer region can be the most critical parameter governing the steep current transition as an optimized value can yield a subthreshold swing of 1 mV/decade (ideal), whereas a non-optimized spacer can result in a degraded *S*-swing of 50 mV/decade for the same set of device parameters. Results highlight that optimization of spacer width and permittivity facilitates an additional degree of freedom in selecting device parameters to achieve steep off-to-on current transition in JL transistors.

In addition, the systematic methodology based on gate misalignment induced electric field redistribution in the semiconductor film has been presented as a way forward to trigger II at relatively lower voltages. While the subthreshold conduction in conventional junctionless devices is located at the center of the film, the enhanced degree of II in asymmetric junctionless device is achieved through an inclined conduction channel facilitated by gate misalignment which improves the product *J.E*. Transforming a detrimental feature such as gate misalignment into a unique positive attribute without significantly degrading other performance metrics remains a crucial, and an innovative way forward to harness the energy efficient operation from Si and Ge JL devices at lower applied voltages in the nanoscale regime.

2.6 References

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Chapter 3

Anomalous Behavior of sub-Boltzmann Switching Si and Ge Junctionless Transistors

3.1 Introduction

Junctionless transistor, which is free from *pn* junction, can be useful in extending the scaling limits of MOS transistors in the nanoscale regime [1-8]. Unique attributes of JL transistors include the presence of conduction channel at the center of the semiconductor film [9-10], immunity from mobility degradation due to surface roughness scattering [11], lower degree of SCEs due to longer effective channel length in the subthreshold regime [12]. In addition to aforementioned advantages offered by JL devices, experimental results reported in the literature depict the occurrence of II induced steep *S*-swing at relatively lower V_{ds} [13].

JL transistors, being heavily doped with one type of impurity atoms, exhibit two types of conduction mechanisms i.e. unipolar and bipolar conduction mode [14]. At a relatively lower V_{ds} ranging from 50 mV to 700 mV (unipolar mode), the drain current in Si JL transistor is solely governed by electrons and exhibits a more gradual (conventional) transition from off-to-on state, whereas at higher V_{ds} ~ 2 V [14], II results in generation of electrons and holes in the film. The successive accumulation of holes triggers bipolar action along with normal MOS operation, and thus, results in very sharp rise in I_{ds} from off-to-on state [14-15]. Although detailed analysis has been carried out in previously reported work [1-8] on JL transistor operated at relatively lower V_{ds}, it is necessary to examine few distinctive features

associated with II induced bipolar mode in JL devices (at relatively higher V_{ds}). The analysis provides physical insights into II induced steep switching JL devices and can be useful for the development of an analytical model to accurately predict the device behavior. Therefore, this chapter presents a systematic study on the key attributes of sharp switching Si and Ge JL transistors, and has been categorized into two sections:

i. The first section (Section 3.2) investigates the variation of threshold voltage with temperature in Si and Ge JL devices. The dominating bipolar effects in JL devices results in positive and negative temperature coefficients of V_{th} which is contrary to the existence of an only negative temperature coefficient of V_{th} in inversion mode and JL devices. The analysis reveals that two contrasting physical mechanisms lead to the positive and negative coefficients of V_{th} as a function of temperature in JL devices.
ii. Another distinctive attribute of JL devices is the occurrence of II induced hysteresis and an associated negative value of the total gate capacitance (C_{gg}) at gate bias corresponding to V_{th}, which has been discussed in Section 3.3. While the hysteresis in the transfer characteristics has shown application in designing of DRAM, the two values of V_{th} associated with forward and reverse sweeps of V_{gs} makes it unsuitable for logic applications. Therefore, independent gate operation of JL transistor has been investigated to suppress the hysteresis while achieving negative value of C_{gg} with *S*-swing ~ 15 mV/decade.

3.2 Positive and Negative Temperature Coefficient of Threshold Voltage

In general, the conventional theory suggests the reduction in V_{th} of a MOSFET, operating at lower V_{ds}, due to an increase in temperature [16]. However, the same may not be applicable in II devices as two different sources of generation of carriers, namely thermal and II, exhibit contrasting

dependence on temperature [16]. While the II induced strong FBEs and variation of V_{th} have been studied for partially depleted (PD) Silicon-on-Insulator (SOI) [17-19] devices, the detailed investigation of the two distinct trends for V_{th} as a function of temperature have not been reported yet in inversion mode or JL devices. Moreover, previously reported work on the behavior of V_{th} with temperature at V_{ds} ~ 50 mV for inversion mode [20-21] and JL [22-27] devices also indicate towards a reduction in V_{th} with an increase in temperature [22-27]. Since JL MOSFETs exhibit an enhanced degree of II, a detailed investigation of the physical effects governing the behavior of V_{th} with temperature is required.

3.2.1 Device Structure

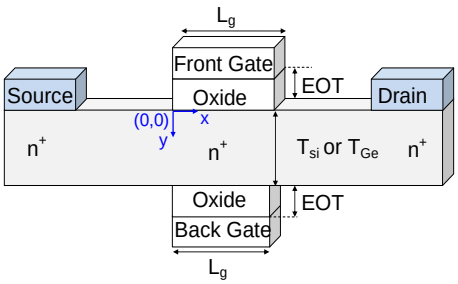

Fig. 3.1: Schematic diagram of a DG Si and Ge JL transistor. Parameters: L_g = 50 nm, T_{si} = 7 nm $N_d = 10^{19}$ cm^{-3}, T_{ox} = 1 nm.

JL MOSFETs are designed with L_g and T_{si} or T_{Ge} of 50 nm and 7 nm, respectively. The film is uniformly doped with dopant concentration of 10^{19} cm^{-3}. The drain bias in Si JL transistor is fixed at 2 V. While Si JL devices are designed with SiO_2 as gate dielectric, due to non-stability of GeO_2 [28], Ge JL devices are designed with GeON as gate dielectric material with higher dielectric constant (~ 6.5) and improved intrinsic properties [28]. The minimum reported thickness of fabricated gate dielectric, fabricated for Ge based MOS capacitor is 1.7 nm with sufficient reduction in the gate leakage current, and the same values for T_{ox} and dielectric constant were used in the analysis [28]. Since, Ge exhibits higher carrier mobility and ionization rates [29], V_{ds} = 1.3 V is used for Ge JL devices.

3.2.2 Variation in Threshold Voltage with Temperature at Lower V_{ds}

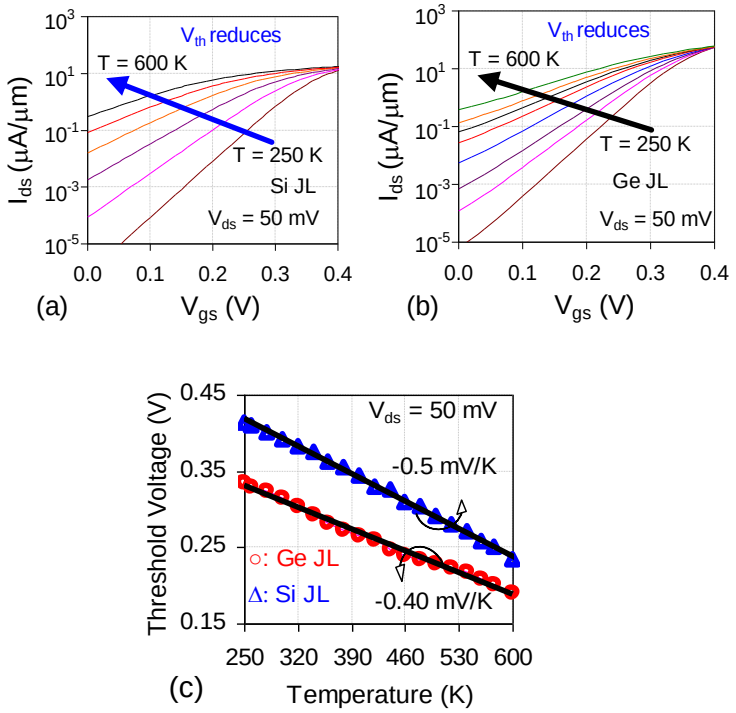

Fig. 3.2: I_{ds} - V_{gs} characteristics plotted as a function of T varied from T = 250 K to T = 600 K in (a) Si and (b) Ge JL devices, and (c) variation of V_{th} with temperature for Si and Ge JL transistors. The V_{ds} is fixed at 50 mV.

In Fig. 3.2*a-b*, I_{ds}-V_{gs} characteristics are plotted for Si and Ge JL transistor with temperature varying from T = 250 K to T = 600 K at V_{ds} = 50 mV. The variation in V_{th} with varying temperature for Si and Ge JL transistors can be seen from Fig. 3.2*c*. The second derivative method and linear extrapolation method reported to extract V_{th} in [30-32], although accurate, are applicable only at a lower V_{ds} of 50 mV (where II is non-existent), and thus, cannot be applied to extract V_{th} in II induced steep switching JL transistor which typically requires relatively higher V_{ds}. Therefore, V_{th} is extracted by transconductance-to-current ratio (g_m/I_{ds}) change method [33-34] as the gate voltage at which maximum of the (-$d(g_m/I_{ds})/dV_{gs}$) is obtained. This method is more stable and gives reliable value of V_{th} even at higher V_{ds} [33].

As temperature increases from 250 K to 600 K, V_{th} in Si JL devices shifts to lower values i.e. from 0.41 V to 0.23 V (Fig. 3.2*c*), whereas for Ge JL transistor it reduces from 0.34 V to 0.19 V (Fig. 3.2*c*). The thermally generated excess carriers contribute to I_{ds} and result in the lowering of V_{th} with increasing T. This behavior of V_{th} with T at V_{ds} = 50 mV is consistent with the work reported in the literature [20-25]. The rate of reduction of V_{th} with temperature (dV_{th}/dT) is nearly -0.42 mV/K (-0.40 mV/K) for Si (Ge) JL devices and quite close to the experimental value (dV_{th}/dT ~ -0.37 mV/K) reported by Trevisoli *et al.*, [24] for Si JL device. While the authors in [24] have used the gate all around nanowire structure to analyze the variation in V_{th} with varying temperature, the structure used in the thesis is a standard DG JL transistor. The small difference in published [24] and reported value of dV_{th}/dT in the thesis is due to the difference in device architecture. Also, authors in [24] have used g_m/I_d method for the extraction of V_{th} at V_{ds} = 50 mV [24]. Please note that the same method cannot be used at higher V_{ds} [30].

3.2.3 Variation in Threshold Voltage with Temperature at Higher V_{ds}

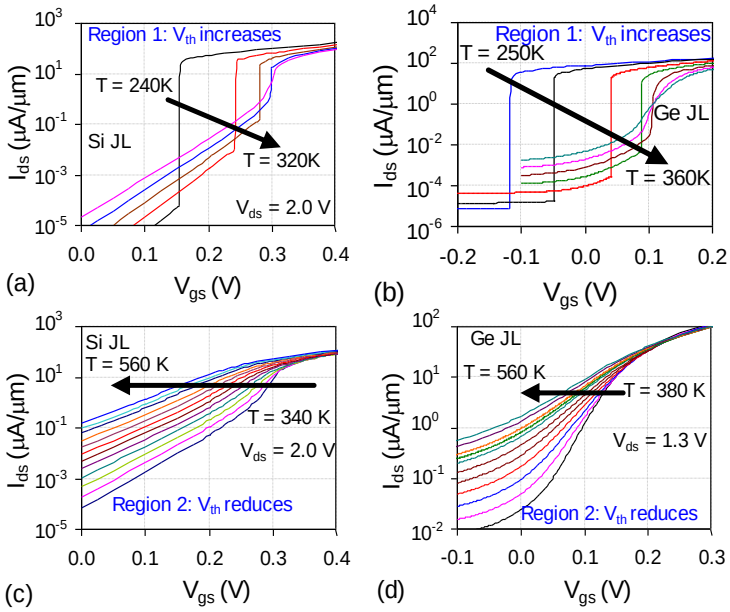

Fig. 3.3: I_{ds}-V_{gs} characteristics as a function of T varied from (a) T = 240 K to T = 320 K for Si, (b) T = 250 K to T = 360 K for Ge JL transistor, (c) T = 340 K to T = 560 K for Si, and (d) T = 380 K to 560 K for Ge JL devices.

In order to analyze the variation of V_{th} with respect to temperature at higher V_{ds} i.e. 2 V for Si and 1.7 for Ge JL devices, I_{ds}-V_{gs} characteristics are plotted as a function of temperature in Fig. 3.3*a-d*. The temperature is varied from 240 K to 560 K for Si and 250 K to 560 K for Ge JL transistor. Fig. 3.3*a-b* depicts that I_{ds}-V_{gs} characteristics exhibit a sharp increase in drain current along with a higher number of decades with a reduction in temperature. A V_{ds} of 1.3 V is considered for Ge JL transistors in comparison to Si JL transistor (V_{ds} = 2 V) as it is sufficient to trigger II in the semiconductor film. The sharp increase in I_{ds} along with the occurrence of subthreshold swing ~1mV/decade is a characteristic feature of II [14, 35]. However, as the temperature increases, the degradation in *S*-swing results in more gradual drain current transition from off-to-on state (Fig. 3.3*c-d*).

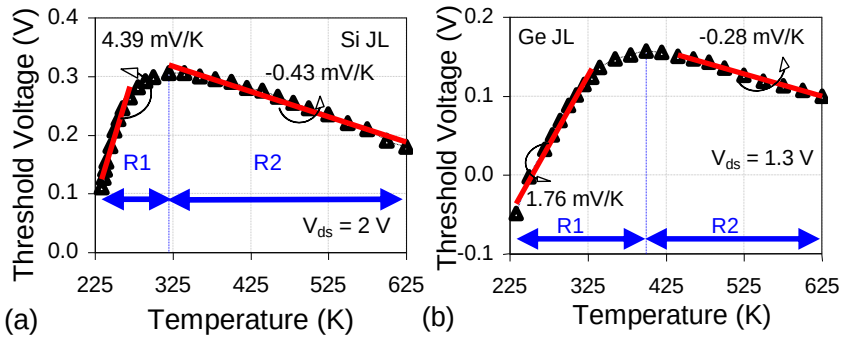

Fig. 3.4: Variation of V_{th} as a function of temperature for (a) Si (V_{ds} = 2 V), and (b) Ge (V_{ds} = 1.3 V) JL transistors.

In order to understand the V_{th} variation, Figs. 3.4*a-b* shows V_{th} as a function of temperature from 225 K to 625 K for Si and Ge JL devices. The graphs show two distinct behaviors of V_{th} with temperature i.e. an anomalous increase of V_{th} at lower temperatures, and a more conventional trend of reduction of V_{th} at higher temperatures. The distinct V_{th} behavior reflect on two different phenomena occurring in the device and leading to positive and negative values of dV_{th}/dT. The graph is divided into two regions denoted by Region 1 (R1) and Region 2 (R2). In R1 for Si JL device, a positive temperature coefficient of threshold voltage is observed as V_{th} increases with temperature (T = 225 K to 320 K) at a rate of ~4.39 mV/K. Any further

increase in temperature beyond T = 320 K results in an opposite trend of threshold voltage i.e. V_{th} reduces with increase in temperature and a negative temperature coefficient of V_{th} i.e. dV_{th}/dT = -0.43 mV/K within the range T = 340 K to 560 K is observed. As shown in Fig. 3.4*b*, the unique characteristics of two different values of dV_{th}/dT is also exhibited by Ge JL transistor at a relatively lower (in comparison to Si JL MOSFETs) V_{ds} = 1.3 V. The increase in V_{th} is observed over a wider range of temperature (T = 250 K to 360 K) with a positive value of dV_{th}/dT (= 1.76 mV/K). This is due to the enhanced degree of FBEs [36-37] in Ge JL transistor. For T > 380 K, a negative temperature coefficient of V_{th} is observed i.e. dV_{th}/dT = -0.28 mV/K in Ge JL devices. The graph clearly shows that the occurrence of II in the device can result in a deviation from the well-known reduction of V_{th} with temperature.

The strength of II in a device can be evaluated by the number of decades of I_{ds} which increases with lowering of temperature and results in a positive temperature coefficient of V_{th}. Two conflicting factors, namely thermal generation and II, govern the generation of excess carriers, and thus, positive and negative coefficients of temperature (Fig. 3.4*a*-*b*), respectively. At lower temperatures (corresponding to R1), carrier generation through II dominates over thermal generation. The degree of II in the semiconductor film enhances with a reduction in temperature [16, 38] which results in the generation of significant number of electron-hole pairs. The impact generated excess carriers trigger strong bipolar effects and shift V_{th} to lower values with a reduction in temperature as shown by region R1. The successive reduction in V_{th} with temperature results in a positive temperature coefficient of V_{th}. However, at higher temperatures (R2), thermal generation of carriers dominates over II. As a result, V_{th} reduces with an increase in temperature (corresponding to R2) and a more conventional trend i.e. negative dV_{th}/dT is observed in Fig. 3.3*c*-*d*.

Moreover, since the rate of generation of electron-hole pairs is more in II as compared to thermal process, the absolute values of dV_{th}/dT will be higher

in R1 than in R2. Results shown in Fig. 3.4 depict that region R1 with positive values of dV_{th}/dT signifies a dominant bipolar conduction mechanism, whereas Region 2 with negative values of dV_{th}/dT indicates a more unipolar behavior of the device. The different trends of dV_{th}/dT can be used to distinguish between the dominant conduction mechanisms i.e. bipolar or unipolar. Also, higher degree of II in Ge JL devices allows impact generated carriers to be sustained over a wider temperature range i.e. dominant bipolar conduction for a greater range of temperature in comparison to silicon. Thus, the rate of change of V_{th} is lower in R1 for Ge JL MOSFETs in comparison to Si JL devices. The unipolar conduction mechanism in Si and Ge JL transistor can also be confirmed from Fig. 3.3*c*-*d*. V_{th} exhibiting conventional trend, reduces as the temperature rises to higher values (T > 320 for Si and T > 380 for Ge JL devices) from 0.30 V to 0.14 V in Si JL transistors when temperature is varied from 320 K to 625 K, and from 0.15 V to 0.08 V for Ge JL devices for T ranges from 380 K to 625 K.

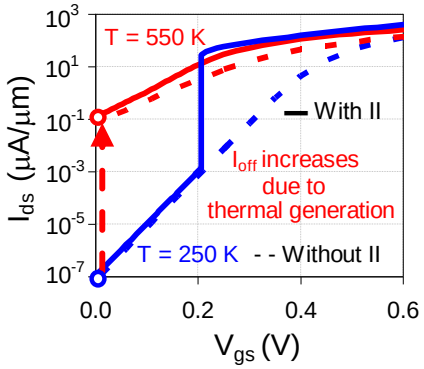

Fig. 3.5: I_{ds}–V_{gs} characteristics at T = 250 and T = 550 K with and without II model for Si JL transistor at V_{ds} = 2 V.

In order to obtain insights into the physical reasons for the occurrence of positive and negative temperature coefficient of V_{th}, I_{ds}–V_{gs} characteristics is shown in Fig. 3.5 at T = 250 K and T = 550 K with and without II model. At T = 250 K, the carrier generation is solely due to II which does not trigger the steep increase in I_{ds} until V_{gs} = 0.20 V, and accordingly off-current retains a lower value (10^{-7} μA/μm). A significant increase in the I_{off} from 10^{-7} μA/μm

at T = 250 K to 10^{-1} µA/µm at T = 550 K, and non-occurrence of sub-60 mV/decade transition from off-to-on state confirms that the dominant conduction mechanism at elevated temperature range is due to thermally generated carriers.

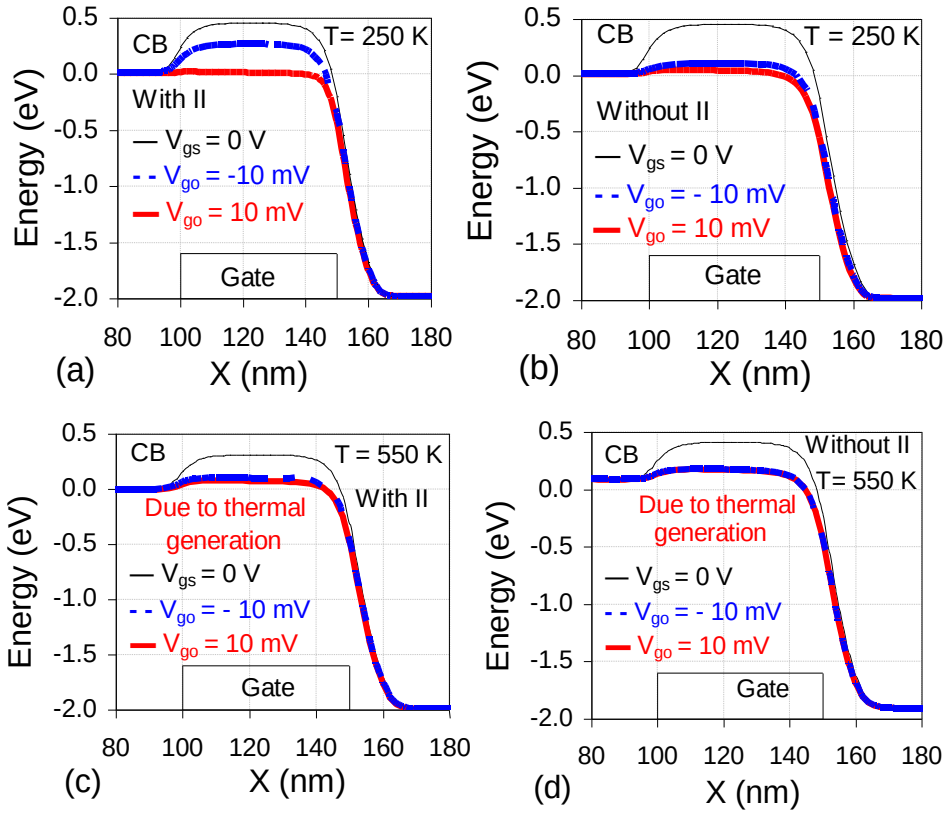

Fig. 3.6: Conduction Band (CB) energy extracted at T = 250 K (a) with II, (b) without II model, at T = 550 K (c) with II and (d) without II model. CB energy is extracted along the channel direction at (x, y = T_{si}/2) at V_{gs} = 0 V, V_{gs}- V_{th} = V_{go} = − 10 mV and V_{go} = 10 mV.

In order to confirm the above mentioned behavior, Conduction Band (CB) energy (Figs. 3.6*a–d*) is extracted with II (Fig. 3.6*a* and 3.6*c*) and without II (Fig. 3.6*b* and 3.6*d*) model for T = 250 K and T = 550 K along the channel direction at the center of the film. V_{th} values at T = 250 K with and without II (Fig. 3.5) are 0.20 V and 0.42 V, respectively, while at T = 550 K (Fig. 3.5), V_{th} is observed to be 0.20 V with II and 0.25 V without II (Fig. 3.5). The significant difference (220 mV) between V_{th} values for II and

without II cases at 250 K signifies the existence of dominant FBEs. Three different gate voltages: 1) V_{gs} = 0 V, 2) V_{gs}-V_{th} = V_{go} = -10 mV, and 3) V_{go} = 10 mV, are selected to capture the two effects, i.e. II and thermal generation of carriers, separately.

At V_{gs} = 0 V, JL transistor is in the off-state and the energy barrier can be clearly seen for the cases with II (Fig. 3.6*a*) and without II (Fig. 3.6*b*) model. However, for 20 mV change (i.e., from V_{go} = -10 mV to V_{go} = 10 mV) in V_{gs} around V_{th}, a sharp reduction in the energy barrier is observed (with II) which signifies a steep increase in I_{ds} at T = 250 K, whereas no change is observed in the CB energy in the device without II for 20 mV change in gate voltage. Considering a lower temperature of 250 K (with II), the probable way for such a significant lowering of energy barrier by ~0.25 eV (Fig. 3.6*a*) is through II. At T = 550 K, a very minor change in the energy barrier is observed for 20 mV change in V_{gs} around V_{th} with II (Fig. 3.6*c*) and without II (Fig. 3.6*d*) model. The absence of a significant change in the energy barrier for 20 mV change in V_{gs} signifies the dominant role of thermal generation at 550 K in both the cases.

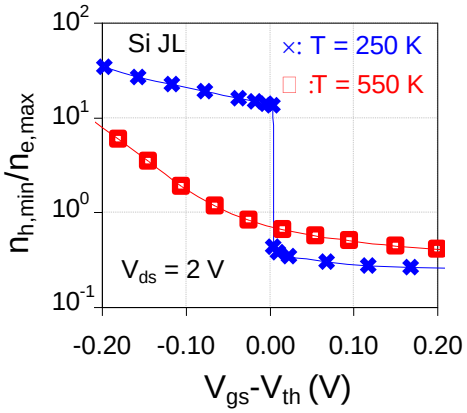

Fig. 3.7: Variation of the ratio of minimum hole concentration ($n_{h,min}$) to maximum electron concentration ($n_{e,max}$) with gate overdrive (V_{gs}-V_{th}) for T = 250 K and T = 550 K with II model at V_{ds} = 2 V in Si JL transistor.

Impact ionization can be understood by evaluating the ratio of minimum hole concentration ($n_{h,min}$) to maximum electron concentration ($n_{e,max}$) i.e.

$n_{h,min}/n_{e,max}$ at gate bias just before V_{th}. The essential condition for the device to operate in dominant bipolar mode is $n_{h,min}/n_{e,max} \sim 5$ [39]. The significant rise in hole concentration triggers a strong bipolar effect which raises the drain current sharply from off-to-on state as shown in Fig. 3.3*a*-*b*. Fig. 3.7 shows the variation of $n_{h,min}/n_{e,max}$ with $(V_{gs}-V_{th})$ for different values of temperature. At a gate bias before the V_{th} i.e. just before the onset of the steep current transition, $n_{h,min}$ is nearly 15 times higher than $n_{e,max}$ at T = 250 K, whereas the successive increase in the temperature deteriorates $n_{h,min}/n_{e,max}$ to 1.5 at T = 550 K. Hence, $n_{h,min}/n_{e,max}$ degrades at higher temperatures and shows the dominance of thermal generation over II at elevated temperature.

3.2.4 Impact Generation Rate with Varying Temperature

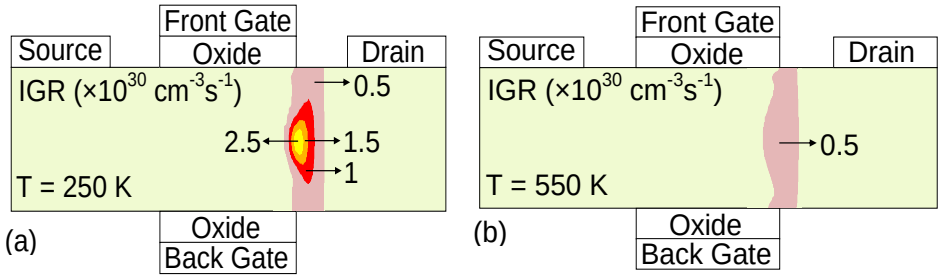

Fig. 3.8 2D contour plot of JL transistor showing IGR after the onset of transition at (a) T = 250 K and (b) T = 550 K.

The increase in temperature raises the thermally generated carrier concentration inside the semiconductor film, and also deteriorates the carrier mobility through the increased impurity scattering which results in the reduction in mobility of carriers [16, 40–42]. This reduction in mobility reduces the current density, which in turn lowers the product of current density and electric field, i.e. *J.E*, which is critical to sustain enhanced degree of II. The reduced *J.E* lowers the II generated power per unit volume, and reduces the ratio of carriers required to trigger dominant bipolar effects which result in positive value of dV_{th}/dT. The reduction in II rates with an increase in temperature has been previously reported by Reggiani *et al*. [40].

Fig. 3.8*a-b* shows the 2D contour plot of IGR at T = 250 K and 550 K immediately after V_{th} for Si JL MOSFET. The location of the peak value of IGR is observed at the center of the semiconductor film towards the drain. IGR values reduces by nearly five times i.e. from 1.5×10^{30} $cm^{-3}s^{-1}$ at 250 K to 0.5×10^{30} $cm^{-3}s^{-1}$ at T = 550 K. As reported in the literature [16, 40], carrier mobility is degraded at higher temperatures. The reduction in mobility lowers the values of current density which reduces the *J.E*, and thus reduces the IGR. Hence, higher values of IGR result in positive temperature coefficient of V_{th} and also the dominant conduction mode is bipolar corresponding to R1 (Fig. 3.4), whereas negative temperature coefficient of V_{th} indicates unipolar conduction shown by R2. It is important to highlight that the unipolar mode, at elevated temperature, does not imply absence of holes in the semiconductor film. Rather, it refers to the relatively lower concentration of holes which is not significant to trigger the steep increase in I_{ds} through II.

3.2.5 Zero Temperature Coefficient

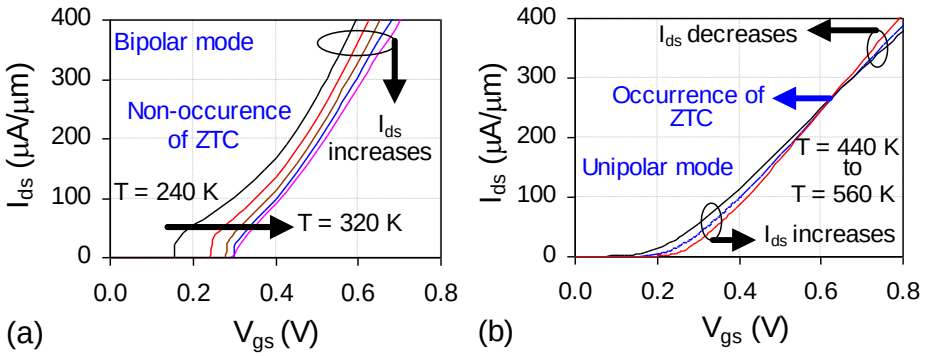

Fig. 3.9: I_{ds}-V_{gs} characteristics as a function of temperature varied from (a) T = 240 K to T = 320 K and (b) T = 440 K to T = 560 K showing non-occurrence of ZTC point and occurrence of ZTC point, respectively. The results are shown for Si JL transistor at V_{ds} = 2 V.

Various authors have reported the presence and absence of Zero Temperature Coefficient (ZTC) in JL transistors [22-27]. The ZTC condition is obtained from the cancellation of the dependencies of mobility and threshold voltage on temperature. The results obtained at relatively higher

drain bias demonstrate that ZTC is also linked with the dominant conduction mode in JL MOSFETs. For the temperature range of 240 K to 320 K, I_{ds}-V_{gs} characteristics (Fig. 3.9*a*) do not exhibit ZTC condition. This is because of the dominant bipolar conduction mode which leads to a significant reduction in V_{th} due to II and overcomes any increase in V_{th} owing to mobility degradation even at higher gate voltages. This results in absence of ZTC condition. As temperature exceeds beyond 320 K (Fig. 3.3*c* and Fig. 3.9*b*), the two conflicting effects i.e. reduction in carrier mobility due to phonon-phonon scattering reduces drain current, while the lowering of V_{th} due to the generation of carriers [16] increases I_{ds}, leading to the occurrence of ZTC condition at V_{gs} = 0.63 V. These results show that ZTC condition can be absent when dominant condition is bipolar instead of unipolar.

3.3 Hysteresis Free Negative Total Gate Capacitance

In JL devices, impact ionization induced FBEs result in hysteresis i.e. drain current traverses different paths during forward and reverse sweeps of gate voltage due to additional carrier generation inside the semiconductor film. The hysteresis associated with the steep drain current transition in II is not appropriate for logic applications as it can yield two threshold voltages corresponding to forward and reverse sweeps of gate voltage [43]. Although hysteresis in the transfer characteristics can be utilized for designing Dynamic Random Access Memories (DRAM) [44-45], it leads to undesirable conditions such as racing, variations in drain current and propagation delays depending on device switching history, and can cause instabilities like bit reversal for logic applications [43].

As hysteresis results in several undesirable effects for logic applications, its suppression while preserving *S*-swing < 60 mV/decade is extremely important for designing logic circuits. An effect consistent with sub-60 mV/decade *S*-swing switching in traditional MOS transistors (apart from tunnel FETs) is the negative value of total gate capacitance [46]. Such negative values of total gate capacitance due to steep switching is different

from the negative values of the gate oxide capacitance exhibited by ferroelectric dielectrics [47]. Design methodology and optimization of JL transistors is needed to achieve a hysteresis free negative total capacitance which can be beneficial for low power logic applications.

3.3.1 Hysteresis and Negative Value of Total Gate Capacitance

3.3.1.1 Hysteresis: Symmetric Mode Operation

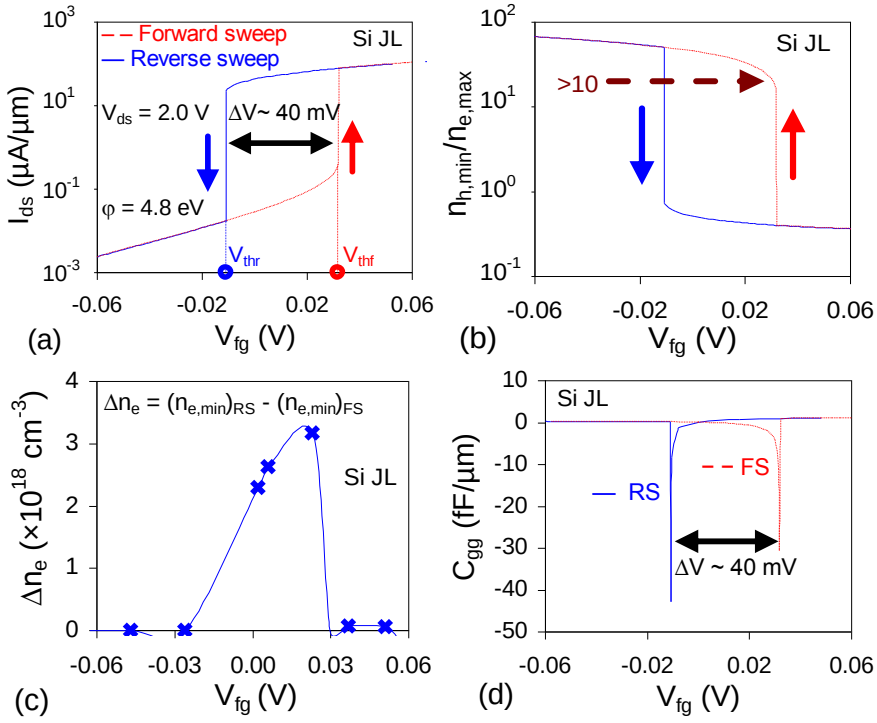

Fig. 3.10: (a) Drain current (I_{ds}) - front gate (V_{fg}) voltage characteristics of JL device biased in a symmetric (V_{fg} = V_{bg} = V_{gs}) mode for Forward Sweep (FS) and Reverse Sweep (RS) of gate voltage. (b) Variation of the ratio $n_{h,min}/n_{e,max}$, (c) extra electron concentration (Δn_e) generated during RS of gate voltages, and (d) variation of C_{gg} with respect to gate voltage.

Fig. 3.10*a* shows the drain current (I_{ds}) - front gate (V_{fg}) voltage characteristics of Si JL transistor for forward and reverse sweeps of gate bias when the device is operated in the symmetric mode i.e. V_{fg} = V_{bg} = V_{gs}. At a relatively higher drain bias (V_{ds} = 2 V), II is triggered at the gate edge near to drain which leads to electron-hole pair generation. While electrons contribute

to the channel at the center of the semiconductor film, holes accumulate at the region of minimum electrostatic potential i.e. semiconductor surface. The successive accumulation of holes actuates a positive feedback mechanism that leads to the sharp increase in I_{ds} with an *S*-swing of 1 mV/decade in both FS and RS of gate bias with nearly 3 orders of current transition at V_{th}. The hysteresis in I_{ds}-V_{fg} characteristics results in different values of threshold voltages corresponding to forward (V_{thf}) and reverse (V_{thr}) voltage sweeps of gate bias, and a difference of 40 mV is observed between V_{thr} and V_{thf}.

As shown in Fig. 3.10*b*, the ratio of minimum hole ($n_{h,min}$) to maximum electron ($n_{e,max}$) concentration i.e. ($n_{h,min}/n_{e,max}$) extracted at the center of the film ($x = L_g/2$, $y = T_{si}/2$) for symmetric gate operation (Fig. 3.10*b*) shows a sharp reduction at $V_{fg} = V_{thr}$ and $V_{fg} = V_{thf}$. The minimum hole concentration ($n_{h,min}$) in *n*-type Si film is 10 times greater than the maximum electron concentration ($n_{e,max}$) just before the onset of the steep current transition. The higher hole concentration in *n*-type JL transistor implies stronger floating body effects with the occurrence of hysteresis in I_{ds}-V_{fg} characteristics. To offset this positive feedback mechanism, a more negative gate bias is applied to deplete the extra electrons (~ 3×10^{18}) generated due to II (Fig. 3.10*c*). It is important to mention that in an inversion mode partially depleted devices, impact generated holes accumulate near the back surface of the buried oxide towards the source edge [48], whereas in JL transistors holes generated due to II accumulate at the front and back surfaces of the semiconductor film underneath the gate, and trigger strong floating body effects [49]. For $V_{gs} > V_{th}$, the conduction channel spread across the film and holes start recombining with electrons, and unipolar device operation is restored [49]. The sharp increase in I_{ds} and the occurrence of hysteresis window is also reflected in the variation of total gate capacitance with gate bias as shown in Fig. 3.10*d*. The sharp decrease in capacitance to negative values occur at the same gate voltages corresponding to steep increase in the drain current as shown in Fig. 3.10*a*.

3.3.1.2 Negative Value of Total Gate Capacitance

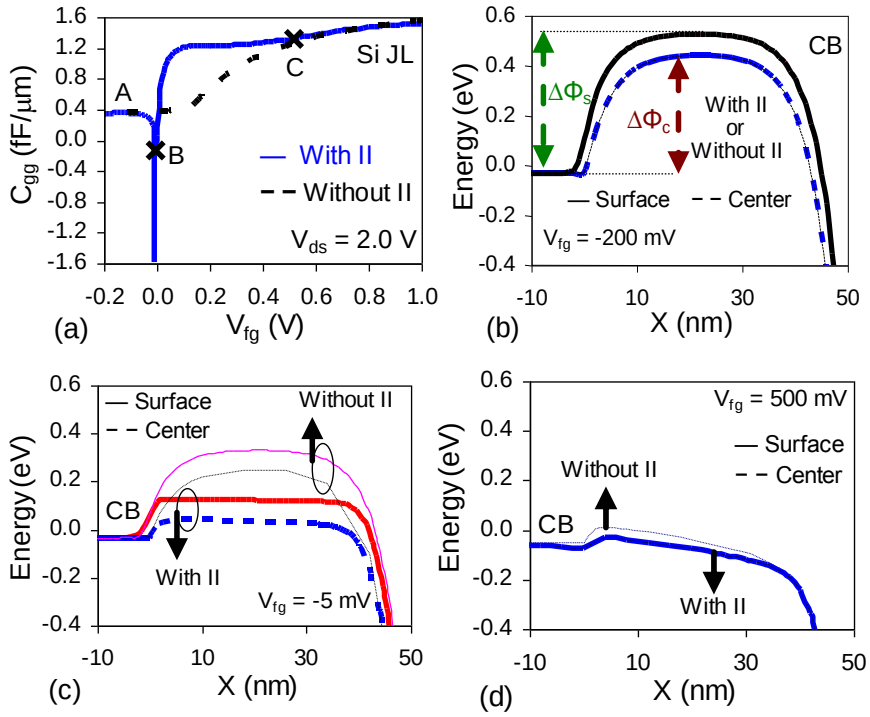

Fig. 3.11: (a) Variation of C_{gg} for RS of gate voltage at V_{ds} = 2 V with and without II model. Variation of CB energy for front gate voltages (b) V_{fg} = - 200 mV, (c) V_{fg} = - 5 mV and (d) V_{fg} = 500 mV along the channel direction. The CB energy is extracted at front (or back) surface and center of the film at x, y = T_{si}/2, and is compared for device with II and without II at V_{ds} = 2 V to highlight the reason for negative total gate capacitance.

The sharp decrease in C_{gg} is a characteristic feature of steep switching JL transistor and is confirmed through Fig. 3.11*a* as without II case does not indicate either a sharp change in current or negative values of total gate capacitance. For non-II case, capacitance exhibits a much anticipated conventional trend and C_{gg} increases with gate bias due to the increase in electron concentration in an *n*-type JL transistor. The constant value of C_{gg} ~ 0.35 fF/μm for V_{fg} < V_{thf} (V_{fg} < 0.2 V) reflects the device being off as the conduction channel at the center of the film is absent. As V_{fg} increases (> 0.2 V), gate capacitance increases due to an increase in electron concentration. For gate voltage greater than flatband (V_{fb}) i.e. V_{fg} > 0.78 V, the maximum

value of C_{gg} becomes equal to 1.5 fF/μm due to the widening of the conduction channel i.e. maximum number of carriers flow through the entire semiconductor film and device operates in the accumulation mode with the accumulation of carriers at front and back surfaces. An important point to be noted here is that the capacitance values (Fig. 3.11*a*) for the two extreme gate voltages are similar for JL device with II and without II cases, while the C_{gg} observed between these two extremes becomes negative due to II.

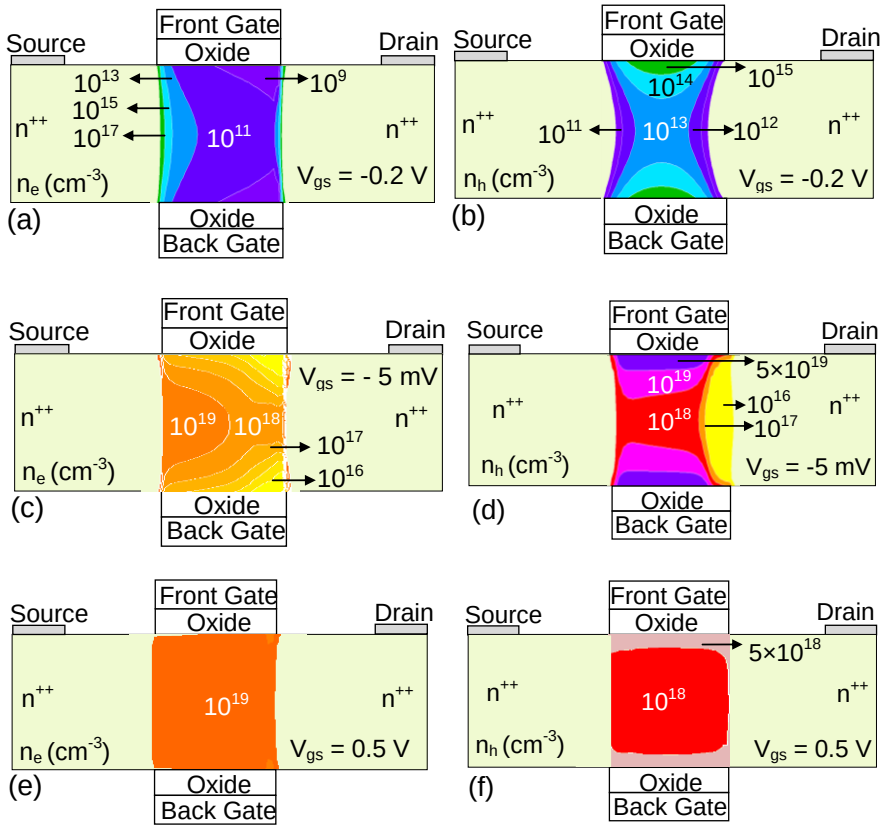

Fig. 3.12: 2D contour plot of JL transistor showing (a) electron (n_e) and (b) hole (n_h) concentration at V_{gs} = -0.2 V (gate bias corresponding to A in Fig 3.11*a*), (c) n_e and (d) n_h concentration at V_{gs} = -5 mV (gate bias corresponding to B in Fig 3.11*a*), (e) n_e and (f) n_h concentration at V_{gs} = 0.5 V (gate bias corresponding to C in Fig 3.11*a*).

To analyze the anomalous behavior of C_{gg}, CB energy is analyzed (Fig. 3.11*b-d*) along with the electron-hole distribution (Fig. 3.12) in the Si film for three different values of gate voltages as denoted by A, B and C in the graph.

(i) At V_{fg} = -0.2 V (denoted by A): When gate voltage is less than the reverse sweep threshold voltage (V_{thr} < -10 mV), similar values of C_{gg} for both impact and non-II cases indicate that II is not significant due to a lower current density as electrons are being depleted by the negative gate voltages. This can be confirmed by CB energy and 2D contour plot showing electron (n_e) and hole (n_h) concentration underneath the gate in Fig. 3.11*b* and Fig. 3.12*a*-*b*, respectively. The CB energy is extracted along the channel direction at 1 nm below the front surface (or 1 nm above the back surface) and at center (x, $y = T_{si}/2$) of the film at V_{fg} = -0.2 V in JL transistor with and without II model. The contour plots for electron-hole concentration shown in Fig. 3.12 are plotted for the device with II at gate voltages denoted by A, B and C in Fig. 3.11*a*. The identical energy band profiles and presence of high energy barrier for electrons at surface ($\Delta\Phi_s$ ~ 0.56 eV) and center ($\Delta\Phi_c$ ~ 0.46 eV) describe the non-conducting state of the device for both conditions i.e. with and without II. This can also be seen in the contour plot (Fig. 3.12*a*-*b*) which shows that the carrier concentration ($n_e < 10^{14}$ cm^{-3} and $n_h \sim 10^{13}$ cm^{-3}) is well below the doping concentration (~ 10^{19} cm^{-3}) at the center of the film. Since the semiconductor film is depleted of carriers, a lower value of total gate capacitance (~0.35 fF/μm) corresponding to off-state is obtained for both the cases.

(ii) At V_{fg} = -5 mV (denoted by B): As V_{fg} increases, the reduction in the barrier between source and channel facilitates more carriers to take part in II, and this increases electron-hole generation in the silicon film (Fig. 3.12*c*-*d*). It can be noted that before the steep transition point (V_{thr} = -10 mV), both electron and hole concentration increase with V_{fg}. However, the increase in hole concentration i.e. $n_h \sim 10^{17}$-10^{18} cm^{-3} at center and 5×10^{19} cm^{-3} at front and back surfaces is significant in comparison to electron concentration ($n_e \sim 10^{18}$-10^{19} cm^{-3} at center and 10^{16}-10^{17} cm^{-3} at front and back surfaces). The successive accumulation of generated holes underneath the front and back gate of the silicon film increases the effective potential in the film. This

results in the lowering of energy barrier at the surface ($\Delta\Phi_s$) from 0.56 eV to 0.15 eV, and at center ($\Delta\Phi_c$) from 0.46 eV to 0.067 eV for the JL device with II model. However, JL transistor without II model shows a relatively lower reduction in $\Delta\Phi_s$ from 0.56 eV to 0.36 eV and $\Delta\Phi_c$ from 0.46 eV to 0.29 eV (Fig. 3.11*c*). The significant increase in holes before the onset of steep transition changes the *n*-type film into a pseudo '*p*-type' region as the ($n_{h,min}$) > 10($n_{e,max}$) which results in the significant lowering of conduction band energy. The observed value of C_{gg} (Fig. 3.11*a*) corresponding to steep transition point is -40 fF/μm. Contrary to conventional case, instead of an increase in electron concentration, the hole concentration of the pseudo '*p*-type' region increases due to II with an increase in front gate voltage (Fig. 3.12*d*) giving rise to negative values of total gate capacitance. The concentration of impact generated holes underneath the gate will be higher than electron concentration at the steep transition voltage and reduces gradually with an increase in gate bias. It can be noted that negative values of C_{gg} with the conventional gate oxide (SiO_2) in JL transistors is the characteristic feature associated with steep switching from off-to-on state.

The II induced negative C_{gg} in JL transistor can also be understood with the conventional definition of intrinsic capacitance between two terminals *i* and *j* in MOSFETs given by $C_{ij} = (\sigma)\ (\partial Q_i/\partial V_j)$ where *i* and *j* corresponds to source, gate and drain terminals, σ = -1 if $i \neq j$ and 1 if $i = j$, Q_i is the terminal electrode charge and V_j is the terminal voltage [50]. The total gate capacitance is defined as $C_{gg} = (\sigma)(\partial Q_g/\partial V_g)$, to capture the effect of change in gate voltage on the gate electrode charge. As the gate voltage increases in JL transistor (without II model), the electron concentration increases in the film. The successive rise in electron concentration induces an equivalent positive charge at the gate terminal, forcing ∂Q_g to be positive, and hence, C_{gg} remains positive. However, in a device with II, a region of semiconductor film (underneath the gate) is dominated by the hole concentration for V_{fg} < -10 mV, and with an increase in ∂V_{fg}, the dominating hole concentration

further rises in the film. This forces ∂Q_g at the gate electrode to be equally negative, and hence, C_{gg} switches its polarity from positive to negative around steep transition point. A similar occurrence of a negative gate capacitance has been previously reported by Omura *et al.*, [51] for a power transistor.

(iii) At V_{fg} = 500 mV (denoted by C): For gate voltage significantly higher than reverse sweep threshold voltage (V_{thr} > 10 mV), the electron concentration (~ 10^{19} cm^{-3}) in JL transistor (with II model) at the center and surface of semiconductor film is higher in comparison to the hole concentration (~ 10^{18} cm^{-3}), and thus, restores the silicon film to *n*-type as electrons become the dominant carriers inside the film (Fig. 3.12*e-f*). This switches C_{gg} back to positive values and capacitance becomes equal to 1.3 fF/μm as electron concentration reaches a value nearly equal to the doping concentration (≈ N_d). The dominant conduction in the film due to a higher electron concentration can also be seen from the CB energy (Fig. 3.11*d*) which shows the absence of barrier between source and channel region at the surface and center of the film for both II and non-II cases.

While the conduction channel is confined at the center of the film for V_{fg} < V_{th} (V_{fg} < -10 mV), for V_{th} < V_{gs} ≤ V_{fb}, the conduction channel spreads across the semiconductor film, and at V_{gs} = V_{fb} (= 0.5 V), the electron concentration in the film becomes nearly equal to the doping. Further increasing gate bias (V_{gs} > V_{fb}) results in accumulation mode conduction with an increase in electron concentration at the front and back surfaces [52]. The increase in electron concentration in the accumulation regime, increases C_{gg} value to 1.5fF/μm. The rise in capacitance has also been previously reported in [53]. However, in JL device without II, the electron concentration increases gradually with V_{gs} and attains the same value of C_{gg} ≅ 1.5 fF/μm at higher gate voltages (V_{gs} ≥ 0.78 V). It should be noted that C_{gg} ≅ 1.5 fF/μm (at V_{ds} = 2 V) does not correspond to deep accumulation regime of the JL transistor where C_{gg} ~ $2C_{ox}$ is expected. JL transistor operating at relatively

higher drain bias (~ 2V) achieves the $C_{gg} \sim 2C_{ox}$ in deep accumulation regime at higher gate voltages ($V_{gs} >> V_{fb}$) which is not the region of interest for steep switching JL transistors.

3.3.2 Suppression of Hysteresis: Asymmetric Mode Operation

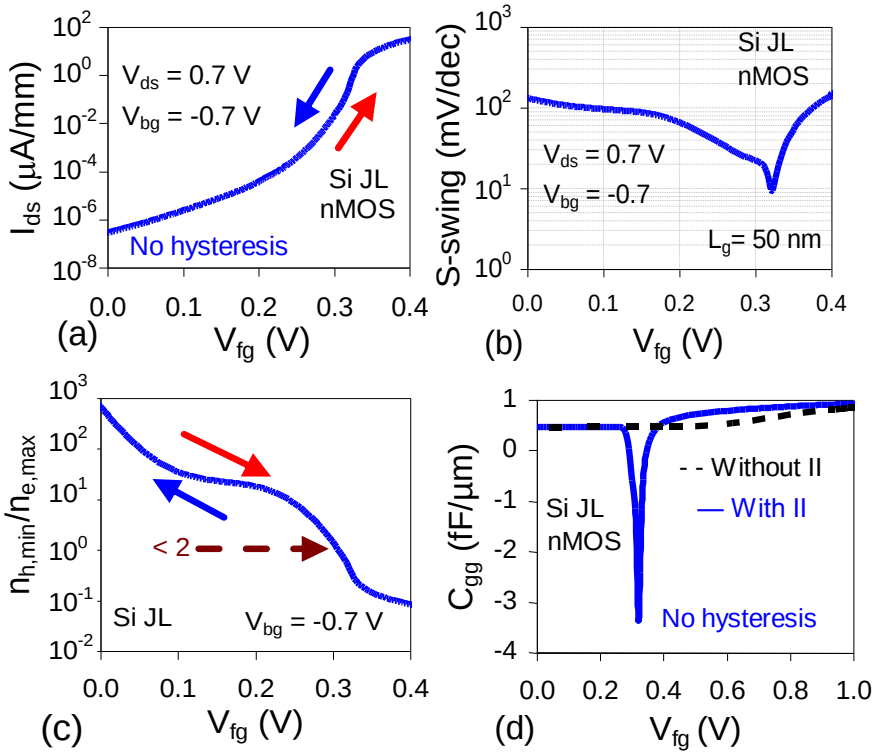

Fig 3.13: (a) I_{ds}-V_{fg} characteristics of JL transistor biased in a asymmetric ($V_{fg} \neq V_{bg}$). (b) Variation of *S*-swing with the front gate voltage, variation of (c) ratio $n_{h,min}/n_{e,max}$ and (d) total gate capacitance for forward sweep or reverse sweep of front gate voltage.

The possible options to reduce the hysteresis in JL transistor are to operate the device at lower V_{ds} in the symmetric mode or in asymmetric mode with a finite back bias (negative for *n*-type JL devices). Operating the device in symmetric mode at lower drain bias will indeed eliminate the hysteresis, but at the expense of an insignificant II, and thus, will results in classical *S*-swing value of 60 mV/decade [14-15]. Therefore, asymmetric mode operation has been explored as an option of suppressing hysteresis and

achieving sub-60 mV/decade *S*-swing. I_{ds}-V_{fg} characteristics at back gate bias (V_{bg}) of -0.7 V is shown in Fig. 3.13*a*. No hysteresis is observed in the characteristics with a sub-60 mV/decade transition in drain current. As shown in Fig. 3.13*b*, *S*-swing remains nearly constant at 100 mV/decade for V_{fg} < 0.2 V, and thereafter, reduces to 11 mV/decade at V_{fg} = 0.32 V.

To understand the physical reason behind the absence of hysteresis in the transfer characteristics, the ratio ($n_{h,min}/n_{e,max}$) with respect to V_{fg} is shown in Fig. 3.13*c*. The carrier concentration is extracted at location of the conduction channel. Although the ratio ($n_{h,min}/n_{e,max}$) is quite high at V_{fg} = 0 V due to lower electron concentration and higher hole concentration, it does not trigger II due to lower current density. As the electron concentration (current density increases) builds up in the channel with an increase in V_{fg}, II phenomenon is initiated. Hysteresis is obtained in the transfer characteristics if the ratio ($n_{h,min}/n_{e,max}$) ≥ 5 is obtained just before the onset of steep current transition in the semiconductor film. In asymmetric mode, $n_{h,min}/n_{e,max}$ ~ 1 just before the gate voltage corresponds to the minimum *S*-swing value. This implies that hole concentration in asymmetric gate operation although sufficient to trigger floating body effects due to II, but with a degree lower than that observed in the symmetric mode of operation at higher V_{ds} (2 V) as shown in Fig. 3.10*a-d*. This is also confirmed by the fact that I_{ds} increases gradually with V_{fg} in asymmetric case, whereas higher value of $n_{h,min}/n_{e,max}$ forces a sharp increase in I_{ds} in symmetric gate operation of JL transistor.

Fig. 3.13*d* shows the variation of C_{gg} in an asymmetric mode operation. The behavior is similar to C_{gg}-V_{fg} curve obtained in the symmetric mode operation (Fig. 3.10*d*). The only difference is that the negative value of gate capacitance is extended over the wider area, and the peak C_{gg} is smaller (absolute value) in comparison to that obtained in the symmetric mode operation. The wider negative area of gate capacitance is due to the variation in *S*-swing as shown in Fig. 3.13*a-b* before threshold voltage (V_{thr} = V_{thf} = 0.32 V).

3.3.3 Benefits of Asymmetric Mode Operation

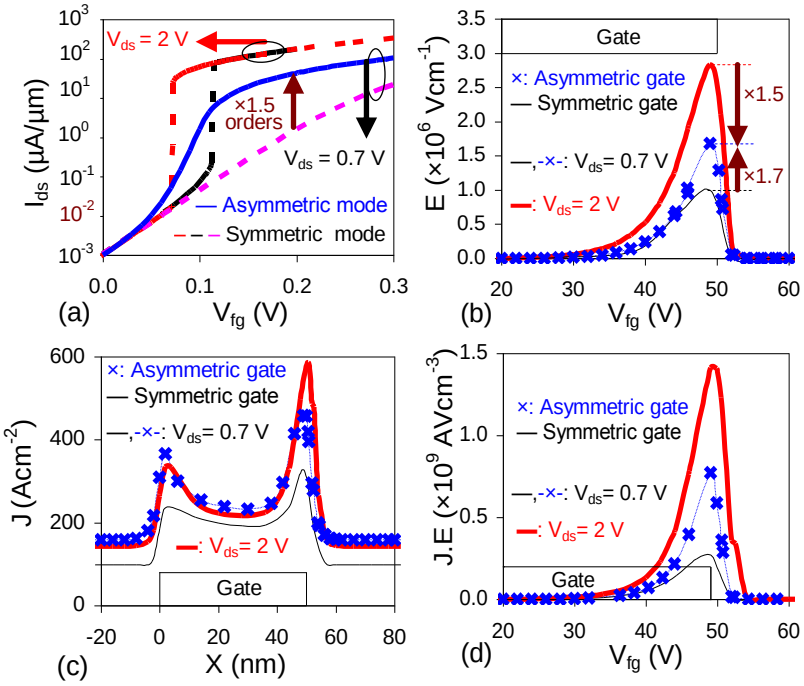

Fig. 3.14: (a) I_{ds}-V_{fg} characteristics of JL transistor for symmetric and asymmetric gate operation. Variation of (b) electric field, (c) current density and (d) product of current density and electric field i.e. *J.E* extracted at the channel location along the *x*-direction. Mode A and mode C denote symmetric gate operation at V_{ds} = 0.7 V and 2 V, respectively. Mode B corresponds to asymmetric gate operation at V_{ds} = 0.7 V and V_{bg} = -0.7 V.

In order to obtain a reasonable comparison between symmetric and asymmetric mode operation, transfer characteristics are shown for the same off-current (I_{off} = 10^{-3} μA/μm) in Fig. 3.14*a* for *n*-type JL transistor. The asymmetric mode operation with V_{bg} = -0.7 V is the best compromise between symmetric mode operation with lower and higher drain biases as hysteresis free sub-60 mV/decade off-to-on transition is achieved. Moreover, utilizing the same drain bias, asymmetric mode operation achieves nearly ~1.5 order higher I_{on}/I_{off} values as compared to symmetric mode operation. Steep switching devices are the best suited to be operated when the gate bias is near to V_{th}. While I_{on}/I_{off} values with V_{ds} = 0.7 V in asymmetric mode is

lower than that achieved in symmetric mode at V_{ds} = 2 V, the advantage in asymmetric mode operation is reflected in the absence of hysteresis and a sub-60 mV/decade *S*-swing with a V_{ds} that is ~3 times lower (V_{ds} = 0.7 V). Three different conditions i.e. symmetric gate operation at (i) V_{ds} = 0.7 V (mode A), (ii) asymmetric gate operation at V_{ds} = 0.7 V and V_{bg} = -0.7 V (mode B), and (iii) symmetric mode at V_{ds} = 2 V (mode C) are selected to evaluate the effectiveness of II under different operating conditions.

Fig. 3.14*b-d* shows the individual component of *J*, *E* and their product (*J.E*) extracted at the channel location before the onset of steep transition at a constant current of 10^{-2} μA/μm. For symmetric gate operation (Fig. 3.13*b*) at V_{ds} = 2 V, the peak magnitude of electric field (2.8×10^{6} Vcm^{-1}) is ~3 times higher in comparison to the device operated at V_{ds} = 0.7 V ($E = 10^{6}$ Vcm^{-1}) and ~1.7 times higher for asymmetric gate operation (~1.7×10^{6} Vcm^{-1}). The higher value of electric field in asymmetric mode is due to the applied negative back bias (V_{bg} = -0.7 V) which results in an increase in the potential difference between channel and drain. The higher potential difference increases the electric field and is sufficient to trigger II in the asymmetric mode operation. The lower degree of II in JL transistor operated in mode B in comparison to mode C can be understood through the current density shown in Fig. 3.14*c*. In an asymmetric gate operation, the negative back gate depletes the electrons from the back surface of the film and lowers the current density in the device. The peak magnitude of current density in asymmetric mode (J ~ 400 Acm^{-2}) at the gate edge is marginally higher (J ~ 330 Acm^{-2}) in comparison to the symmetric gate (mode A) device, while *J* for mode C is ~1.8 times higher (J ~ 600 Acm^{-2}). Relatively lower values of *J* in the asymmetric gate operation in comparison to symmetric gate operation at V_{ds} = 2 V is responsible for reducing the degree of II. Although JL device operated in asymmetric mode exhibits a marginally higher current density as compared to the JL device operated in symmetric mode with lower V_{ds}, but the effectiveness of asymmetric mode to achieve sub-60 mV/decade off-to-on transition is due to the 1.7 times higher field (Fig. 3.14*b*) which enhances *J.E*

(Fig. 3.14*d*). Also, the independent gate operation in JL transistor removes the constraint of selecting higher gate workfunction to fully deplete the device in the off-state as a negative bias at the back gate is applied. The gate workfunction for symmetric gate operation to achieve the same off-current is relatively high i.e. ~ 4.9 eV, whereas a midgap (~ 4.6 eV) workfunction is sufficient to turn-off the device for asymmetric mode operation.

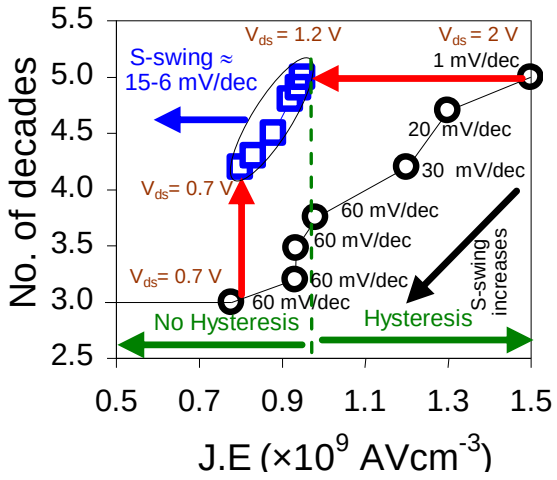

Fig. 3.15: Variation in peak magnitude of product *J.E* plotted as a function of V_{ds} for (○) symmetric gate and (□) asymmetric gate operation of JL transistors. All the results are extracted at the gate voltage corresponding to the I_{ds}= 10^{-2} μA/μm.

The criterion of sub-60 mV/decade *S*-swing and the occurrence of hysteresis for asymmetric and symmetric modes can be understood through a plot of the number of decades of I_{on}/I_{off} with respect to $(J.E)_{max}$ as shown in Fig. 3.15 for various values of V_{ds}. The degree of II can be quantified through the evaluation of *J.E*, where higher values of *J.E* indicate higher degree of II while the lower values deteriorate II phenomena. Higher *J.E* values also reflect on the occurrence of hysteresis along with a super steep (~ 1 mV/decade) off-to-on transition, whereas a lower (*J.E*) values imply sub-60 mV/decade gradual off-to-on transition without hysteresis. The product *J.E* is extracted at the gate voltage corresponding to I_{ds} = 10^{-2} μA/μm for symmetric and asymmetric gate operation of JL transistor. A higher drain bias enhances

J.E value which leads to higher II and I_{on}/I_{off} values along with lower *S*-swing values. The data for symmetric mode represents *S*-swing values from 60 mV/decade (V_{ds} = 0.7 V) to 1 mV/decade (V_{ds} = 2 V), whereas *S*-swing for asymmetric mode ranges from 15 mV/decade (V_{ds} = 0.7 V) to 6 mV/decade (V_{ds} = 1.2 V) in Fig. 3.15. For lower *J.E* values, the significant improvement in I_{on}/I_{off} in asymmetric mode operation is due to the reduction in *S*-swing due to the occurrence of II. If *J.E* values are limited to 10^9 AVcm^{-3}, the transfer characteristics are free from hysteresis. Results indicate that even though symmetric operation with V_{ds} = 2 V result in very high *J.E* values (1.5×10^9 AVcm^{-3}), the same I_{on}/I_{off} can be achieved with asymmetric operation without hysteresis by reducing the drain bias (V_{ds} = 1.2 V) by a factor of ~2. The graph highlights the typical range of *J.E* values ($\leq 10^9$ AVcm^{-3}) which results in the absence of hysteresis and sub-60 mV/decade *S*-swing with asymmetric mode of operation in JL transistors.

Also, the available range of various biases such as (i) drain bias and (ii) back bias for hysteresis free negative total gate capacitance can be analyzed from Fig. 3.15. The impact of drain bias on the asymmetric gate operation of JL transistor has been analyzed in terms of the product of current density and electric field plotted against number of decades of drain current transition (Fig. 3.15). The device can achieve hysteresis free total negative gate capacitance with *S*-swing lying between 6 and 15 mV/decade for V_{ds} varying from 1.2 V to 0.7 V. For V_{ds} > 1.2 V, hysteresis window appears for forward and reverse sweeps of V_{fg} due to an enhanced electron-hole generation. The back gate bias has been varied from -0.7 V to -1 V for *n*-type JL devices. Lowering (more negative) back gate bias will reduce the off-current by depleting the semiconductor film, and increases the threshold voltage while resulting in *S*-swing > 15 mV/decade. Hence, V_{ds} > 1.2 V and using a V_{bg} lower than -1 V (V_{bg} more negative than -1 V) is not a feasible option for hysteresis free negative total capacitance values.

3.3.4 Asymmetric Mode Operation of Ge JL Transistor

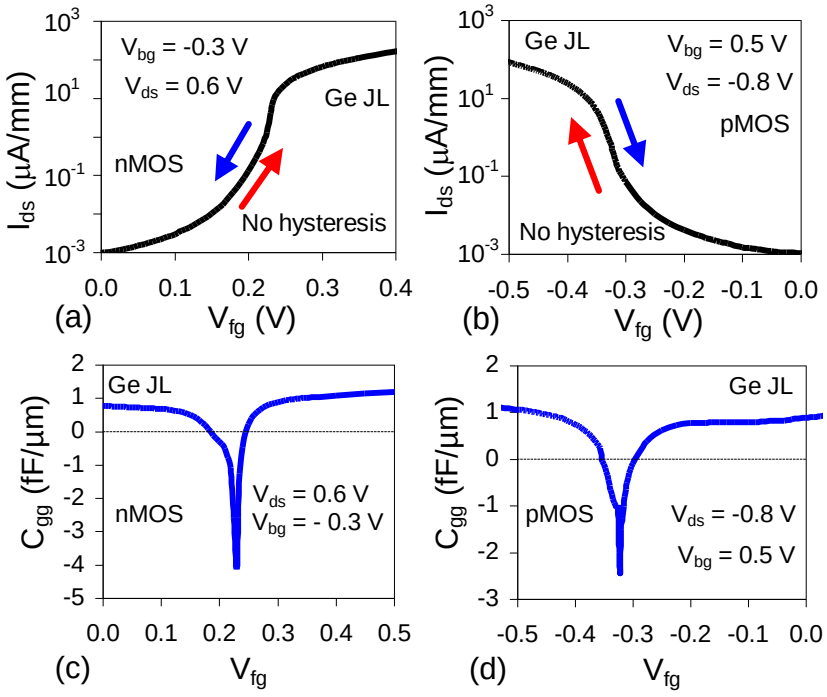

Fig. 3.16: I_{ds}-V_{fg} characteristics for (a) *n*MOS and (b) *p*MOS Ge JL transistor. Variation of C_{gg} with respect to front gate voltage for (c) *n*MOS and (d) *p*MOS Ge JL transistor.

Although, lower bandgap in Ge is beneficial to trigger II at lower voltages, it also results in increased band-to-band tunneling at lower gate voltages [54]. This tunneling has been considered through the incorporation of tunneling parameters reported by Kim *et al.*, [55]. Fig. 3.16*a-b* show I_{ds}-V_{fg} characteristics of *n*MOS (V_{ds} = 0.6 V and V_{bg} = -0.3 V) and *p*MOS (V_{ds} = -0.8 V and V_{bg} = 0.5 V) Ge JL transistor, respectively. A *S*-swing of ~8 mV/decade for *n*MOS and ~20 mV/decade for *p*MOS without any hysteresis in the characteristics is observed in Ge JL MOSFET. The C_{gg} corresponding to I_{ds}-V_{fg} characteristics is shown in Fig. 3.16*c-d*. *J.E* values for *n*MOS and *p*MOS Ge JL at the gate voltage corresponding to $I_{ds} = 10^{-2}$ μA/μm is 0.6×10^{9} AVcm^{-3} and 0.4×10^{9} AVcm^{-3}, respectively, which are consistent with the specified range for obtaining *S*-swing < 15 mV/decade with hysteresis free I_{ds}-V_{fg} curve.

3.4 Conclusion

The chapter described the anomalous behavior of sharp switching junctionless transistor. The unique features of impact ionization triggered bipolar effects in an essentially unipolar JL transistor have been analyzed. It has been demonstrated that a positive temperature coefficient of threshold voltage in steep switching JL devices results from the dominant bipolar conduction mode at lower temperatures, whereas unipolar conduction mode is prevalent at higher temperatures which results in the usual negative temperature coefficient of threshold voltage i.e. threshold voltage reduces with an increase in temperature. Also, the independent gate operation has been shown to suppress hysteresis while preserving low *S*-swing ~15 mV/decade along with the negative values of total gate capacitance.

3.5 References

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Chapter 4

Optimization of Ge Junctionless Transistors for sub-*kT*/*q* Switching Action

4.1 Introduction

As Silicon CMOS technology is facing challenges due to aggressive scaling, high mobility materials such as Ge have gained significant attention to improve the transistor performance [1-2]. Considerable attention has been paid to improve the quality of interface with low surface trap density [3-4], and contact formation [5-6]. Also, integration of high-κ gate dielectric [7-8] and scaling aspects [9-11] has been reported for *p*-type Ge based devices. While the inversion mode *p*-type Ge based transistors are the best suited for high performance applications [12], the functionality of conventional *n*-type Ge devices is limited due to the presence of surface states and degraded quality of oxide-semiconductor interface [13]. The aforementioned problems in an inversion mode transistor can have significant effect on II, and hence, on the performance of Ge devices. These surface states trap electrons from the inversion layer which significantly degrade the interface quality and mobility of the carriers due to Coulombic scattering in *n*-type Ge MOSFET [14-15].

The above reported problems associated with inversion mode *n*-type Ge based transistors due to traps are not expected to be significant in JL devices as subthreshold conduction starts from the bulk of the film [16-17], and gradually spreads across the film till gate voltage becomes equal to the V_{fb} [18]. Also, irrespective of the surface states and traps, II in JL transistor is always triggered at the bulk of the film near to the gate edge towards the drain

side. Hence, the degree of II induced floating body effects are expected to be less dependent on the surface non-idealities in JL devices for $V_{gs} < V_{fb}$ as compared to inversion mode devices. As steep switching devices are the best suited to operate around threshold voltage, operating the device at $V_{gs} > V_{fb}$ is not desirable.

Although the previously proposed Ge [19-20] and SiGe [21-22] based IMOS device achieves *S*-swing < 10 mV/decade at T = 300 K, the requirement of higher supply voltage is a critical issue for low power applications [19-22]. In previous chapters, it has been shown that Ge JL devices trigger II at lower drain bias as compared to their Si counterparts [19-22]. However the performance of Ge based devices, due to lower E_g, is significantly deteriorated due to BTBT. Therefore, it is necessary to obtain insights into various physical mechanisms governing the functionality of sharp switching Ge JL devices, and highlight the optimization technique to preserve the effectiveness of II to achieve *S*-swing < 5 mV/decade. The chapter describes the guidelines for designing steep switching Ge JL transistor for low power applications and has been categorized into following three sections:

i. The first section (Section 4.2) describes the design methodology to suppress off-state BTBT, a crucial phenomenon at lower gate lengths in Ge based device, while achieving steep *S*-swing < 5 mV/decade.

ii. The second section (Section 4.3) demonstrates a technique to enhance II through the use of Raised Source/Drain (RSD) Ge JL transistor at relatively lower drain bias of 0.9 V.

iii. The third section (Section 4.4) discusses the extreme condition of II i.e. Single Transistor Latch, and its suppression in DG JL transistors while preserving steep *S*-swing.

4.2 Multiple Physical Phenomena in Ge JL Transistors

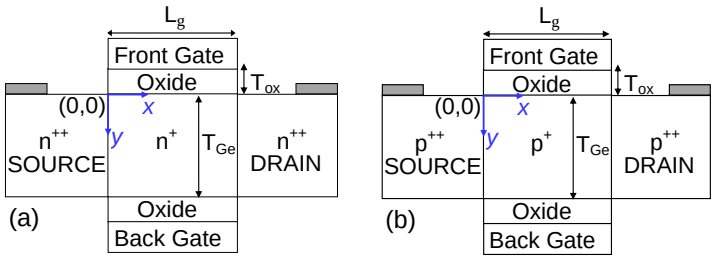

Fig. 4.1: Schematic diagram of (a) *n*-type and (b) *p*-type DG Ge JL transistor. Parameters: L_g = 50 nm, N_d = 10^{19} cm^{-3}, T_{Ge} = 9 nm, N_{SD} = 10^{20} cm^{-3}.

DG Ge JL device, shown in Fig. 4.1, was analyzed with L_g = 50 nm, T_{Ge} = 9 nm (*n*MOS) and T_{Ge} = 11 nm (*p*MOS), N_d = 10^{19} cm^{-3} and N_{SD} = 10^{20} cm^{-3}. In the nanoscale regime, multiple physical effects such as II and BTBT can occur in a MOS transistor. As these effects are related to physical phenomena in the device and affect the performance, a careful identification and optimization of the same is required to achieve an application specific (steep switching) optimal performance. Recent results have shown that the performance of JL devices are deteriorated due to BTBT [23-29] at lower gate bias, which results in an undesirable increase in the I_{off}. Additionally, BTBT becomes more prominent in Ge based JL devices due to lower bandgap, and thus, degrades any advantage offered by the sub-60 mV/decade *S*-swing.

Although II induced FBEs can be useful to achieve a sharp increase in drain current [2-4] at the threshold, BTBT at lower gate bias limits the performance due to an increase in off-current. Therefore, a pragmatic metric to understand the occurrence of multiple physical phenomena i.e. II and BTBT in MOS device is the product *J.E*, which denotes total power generated per unit volume in the device due to a physical phenomenon, and has been used previously to analyze II in JL devices [30] but not for optimizing multiple physical process occurring in the device. In general, *J.E* values are low (~10^{8} $AVcm^{-3}$) in the subthreshold region whereas higher *J.E* values (~10^{12} $AVcm^{-3}$) are expected above threshold due to a greater number of electrons in the channel [30]. Thus, any change in the carrier concentration

due to a physical process (or application of bias) is reflected in the values for *J.E*. Since BTBT and II, both involve generation of additional carriers, the use of *J.E* will be beneficial in understanding the device operation as well as optimizing its performance. A methodology is described, focusing on the optimization of drain bias and film thickness, to balance the conflicting requirements of *J.E* for tunneling and II, while maintaining higher values of *J.E* near to threshold for achieving sub-60 mV/decade *S*-swing values. In order to perform the analysis, II rates and mobility parameters were obtained from published data [31-33]. The tunneling of the carriers is captured through non-local BTBT model [34]. While using non-local BTBT model, it is ensured that the quantum meshes in the tunneling prone area are fine enough to capture the appropriate behavior of BTBT current.

4.2.1 Impact of Drain Bias on DG Ge JL Transistor

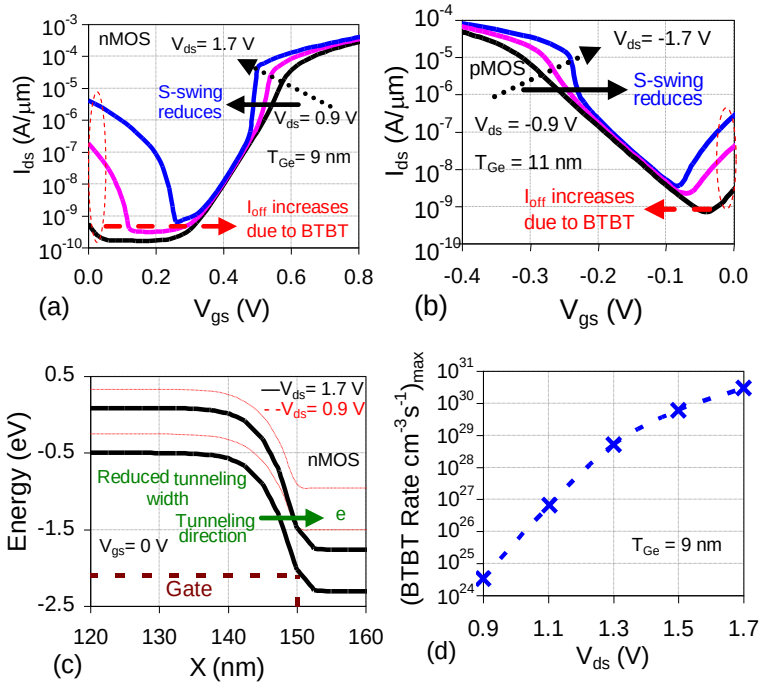

Fig. 4.2: I_{ds}-V_{gs} characteristics of (a) *n*MOS and (b) *p*MOS DG Ge JL device at V_{ds} = 1.7 V with II and BTBT model. Variation in (c) VB and CB energy showing off-state tunneling at V_{gs} = 0 V, and (d) BTBT rate extracted for V_{ds} varied from 0.9 V to 1.7 V. Results shown in Fig. 4.2*c*-*d* are extracted at the channel location *x*, *y* = T_{Ge}/2 at V_{gs} = 0 V.

Figs. 4.2*a*-*b* shows I_{ds}-V_{gs} characteristics for *n*MOS and *p*MOS Ge JL MOSFET. A reduction in *S*-swing from the classical value of 60 mV/decade is observed with an increase in $|V_{ds}|$ due to enhanced degree of II which actuates positive feedback loop due to successive accumulation of holes at lower potential region underneath front and back gates. The value of *S*-swing is close to the ideal 60 mV/decade at lower drain bias (~ 0.9 V), thus indicating that II is not likely to occur at drain biases lower than the threshold suggested by Anderson *et al.*, [35] and Lee *et al.*, [36]. Although *S*-swing < 10 mV/decade is obtained for both *n*MOS and *p*MOS JL devices with a corresponding increase in the number decades of I_{ds} transition from off-state to on-state, BTBT results in a degradation in off-current from ~ 10^{-10} A to ~ 10^{-6} A (for *n*MOS) and ~10^{-9} A to 10^{-7} A (for *p*MOS) at V_{ds} = 0.9 V and 1.7 V, respectively. The observed trend of tunneling current is similar to that published in the literature [23, 37-38].

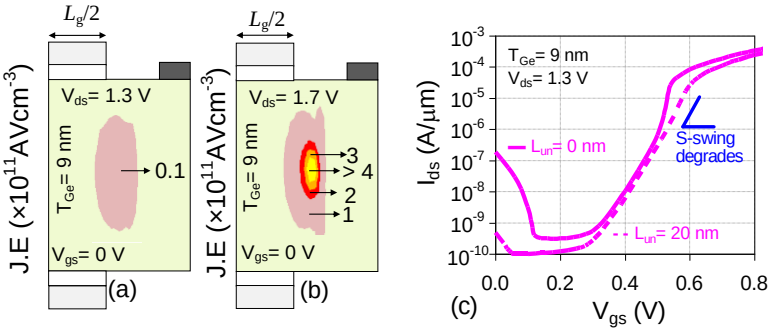

Fig. 4.3: 2D contour plot showing the product *J.E* in the off-state (V_{gs} = 0 V) in *n*MOS JL at (a) V_{ds} = 1.3 V and (b) V_{ds} = 1.7 V, and (c) I_{ds}-V_{gs} characteristics showing the effect of underlap i.e. with L_{un} = 0 nm and 20 nm.

The enhanced tunneling in Ge JL transistor at higher V_{ds} can be confirmed by analyzing CB and VB energy levels extracted along the channel direction at V_{gs} = 0 V and V_{ds} = 0.9 V and 1.7 V as shown in Fig. 4.2*c*. At higher V_{ds}, the reduced tunneling width along with the increased overlap between the available filled states in VB and empty states in CB results in higher value of BTBT generation rate as shown in Fig. 4.2*d*. The generation rate increases from ~5×10^{24} cm^{-3}s^{-1} to ~10^{30} cm^{-3}s^{-1} for change in V_{ds} from 0.9 V to 1.7 V,

respectively. The tunneling of electrons from VB to CB results in the generation of holes underneath the gate. The successive accumulation of holes at V_{gs} = 0 V with increasing V_{ds} in the valence band contributes to positive potential and raises the electrostatic potential from -0.032 V to 0.21 V, thereby lowering the barrier between source and channel region underneath the gate with a significant increase in the off-current.

The off-state BTBT in Ge JL transistor can also be explained through *J.E* product as shown by the 2D contour plot in Figs. 4.3*a*-*b* at V_{ds} = 1.3 V and 1.7 V in the off-state (V_{gs} = 0 V). The magnitude of *J.E* increases with V_{ds} and is an indicative of the enhanced tunneling component of current which degrades the off-current. The higher V_{ds} significantly increases the lateral electric field associated with the drain and increases the tunneling of electrons from channel to drain region which results in ~40 times higher value of *J.E* at higher V_{ds} i.e. *J.E* changes from 0.1×10^{11} AVcm^{-3} to 4×10^{11} AVcm^{-3} at V_{ds} = 1.3 V and 1.7 V, respectively at V_{gs} = 0 V. While the authors in [23] have shown the advantage of gate-to-drain underlap in suppressing tunneling, Fig. 4.3*c* shows that the underlap even though useful in suppressing tunneling, is not suited for JL device as it also degrades II with a loss of steep switching at around V_{gs} = 0.5 V. Therefore, an alternative approach of suppressing *J.E* at V_{gs} = 0 V while ensuring the enhancement of the same near to the threshold for II and sharp switching is needed.

4.2.2 Optimization of Product of Current Density and Electric Field

A possible option proposed in the literature [11] to reduce the off-state BTBT current in JL transistor is by reducing channel doping (N_d). Unlike inversion mode devices which exhibit lower current densities due to undoped (10^{15} cm^{-3}) semiconductor film, heavily doped (10^{19} cm^{-3}) JL devices achieve higher values of current density which is beneficial to enhance II [30]. Therefore, reducing the doping is not a useful option. Alternatively, the off-state BTBT can be suppressed by reducing V_{ds}. However, it will also degrade II and steep current switching. In order to enhance *J.E*, a possible option is to

increase T_{Ge} to its maximum possible value while ensuring depletion in off-state and minimizing V_{ds}. Minimizing drain bias reduces the extent of tunneling at lower V_{gs}, whereas improvement in J due to a thicker heavily doped film is significant, and thus, dominates the overall increase in $J.E$. The proposed concept allows for higher value of $J.E$, beneficial for steep drain current from off-to-on-state, at gate voltage after the steep current transition while simultaneously achieving lower $J.E$ values at V_{gs} = 0 V (off-state).

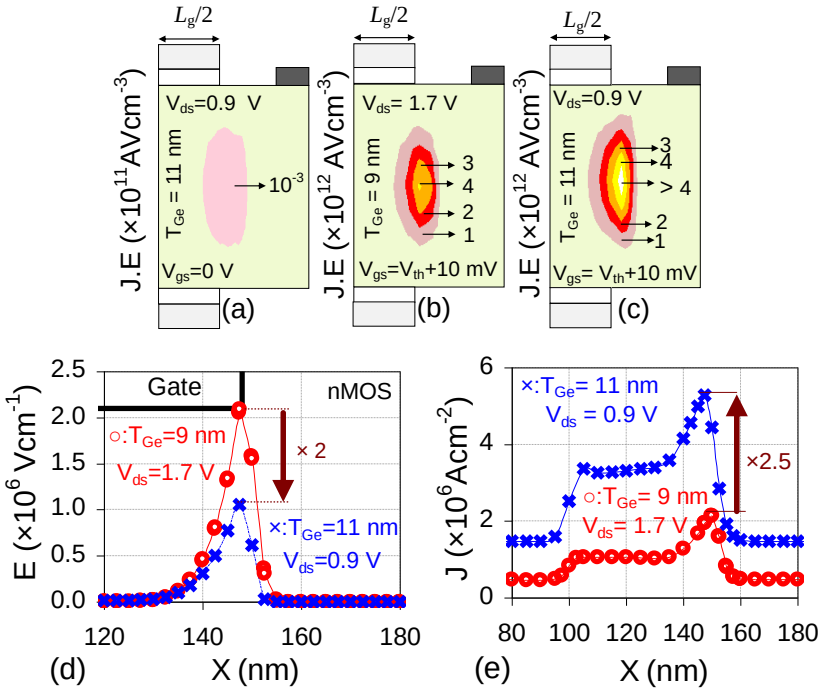

Fig. 4.4: 2D contour plot showing the product $J.E$ (a) for T_{Ge} = 11 nm at V_{gs} = 0 V and V_{ds} = 0.9 V, (b) for T_{Ge} = 9 nm at V_{ds} = 1.7 V, and (c) for T_{Ge} = 11 nm at V_{ds} = 0.9 V and V_{gs} = V_{th}+10 mV at the gate edge towards the drain. Variation of (d) lateral electric field and (e) current density extracted along the channel direction at the center of the film at x, y = L_g/2.

In order to confirm the advantage gained by utilizing a thicker film, Fig. 4.4*a* shows the product $J.E$ at V_{ds} = 0.9 V and V_{gs} = 0 V. A lower value (10^8 AVcm^{-3}) of product $J.E$, as compared to that shown in Figs. 4.3*a-b*, obtained at V_{gs} = 0 V, is due to reduction in V_{ds} which suppresses BTBT. This reduction in the BTBT by lowering V_{ds} reduces I_{off}, and more importantly,

simultaneously increasing the film thickness enhances II generated power at gate voltages near about the threshold. The benefits of using a thicker film can be observed from 2D contour plot of *J.E* shown in Figs. 4.4*b*-*c* after the onset of steep transition at V_{ds} = 1.7 V and 0.9 V, respectively. $(J.E)_{max}$ observed at the center of the film at the gate edge towards drain is ~2 times higher along with the enhanced degree in a JL MOSFET with T_{Ge} = 11 nm operated at V_{ds} = 0.9 V than a device with T_{Ge} = 9 nm at V_{ds} = 1.7 V. Figs. 4.4*d*-*e* show the variation of electric field and current density extracted along the channel direction at V_{ds} = 1.7 V (with T_{Ge} = 9 nm) and V_{ds} = 0.9 V (with T_{Ge} = 11 nm). Although peak electric field of 10^6 V/cm for V_{ds} = 0.9 V is lower in comparison to that at V_{ds} = 1.7 V (Fig. 4.4*d*), the 2.5 times higher current density (Fig. 4.4*e*) obtained by using a relatively thicker heavily doped film (T_{Ge} = 11 nm) eventually enhances *J.E* values.

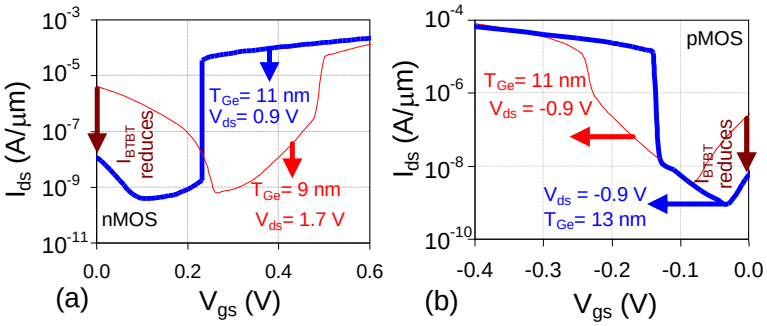

Fig. 4.5: Comparison of I_{ds}–V_{gs} characteristics for (a) *n*MOS and (b) *p*MOS showing reduced off-state BTBT.

The increase in *J.E* is also reflected in I_{ds}-V_{gs} curve shown in Figs. 4.5*a*-*b* which depicts a sharp rise in I_{ds} with *S*-swing ~2 mV/decade along with ~4.5 decades of current transition for *n*MOS (Fig. 4.5*a*) and ~3 decades with *S*-swing ~4 mV/decade for *p*MOS at V_{ds} = 0.9 V (Fig. 4.5*b*) along with a reduction in BTBT current by 2 orders in *n*MOS and 1.5 orders in *p*MOS devices. Hence, enhancing *J.E* through an appropriate selection of V_{ds} and T_{Ge} is clear with reference to Figs. 4.2*a*-*b* as steep *S*-swing occurs at lower operating voltage (Fig. 4.5*a*-*b*) along with much reduced BTBT.

4.2.3 Impact of Gate Workfunction and Underlap

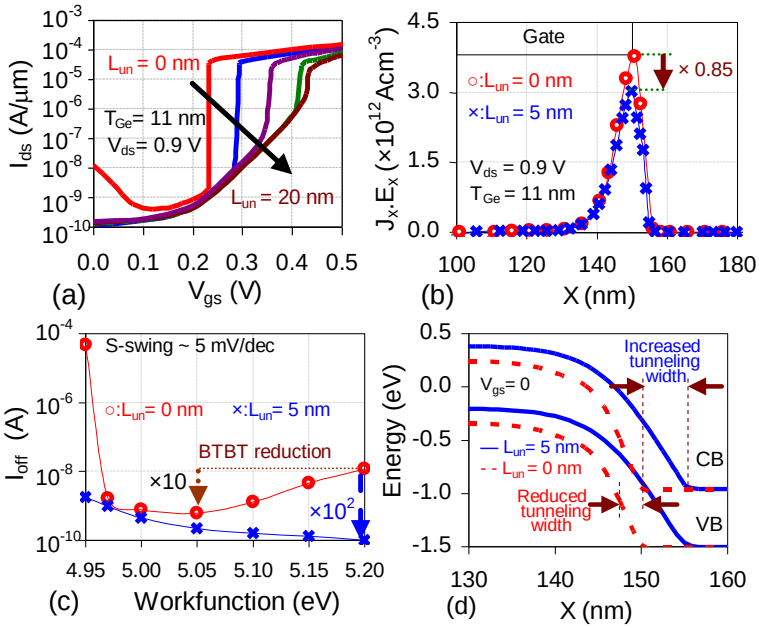

Fig. 4.6: (a) I_{ds}-V_{gs} characteristics for Ge JL device as a function of underlap length (L_{un}), (b) variation of ($J.E$) extracted at (x, y = T_{Ge}/2) at V_{gs} = V_{th} + 10 mV and L_{un} = 0 nm and 5 nm, (c) off-current as a function of gate workfunction (φ_m), and (d) comparison of CB and VB energy profile of Ge JL transistor designed with L_{un} = 0 nm and L_{un} = 5 nm. All the results are plotted for T_{Ge} = 11 nm and V_{ds} = 0.9 V.

The optimization of Ge JL transistor by increasing the film thickness (T_{Ge} = 11 nm) and reducing the drain bias (V_{ds} = 0.9 nm) may not completely suppress the off-state band-to-band tunneling for φ_m = 5.2 eV as shown in Fig. 4.6. Apart from V_{ds} and T_{Ge}, off-current can also be controlled by gate workfunction (φ_m) and adopting a nominal underlap length (L_{un}). Although, underlap is a useful option to suppress the tunneling, it should be incorporated after optimizing V_{ds} and T_{Ge} in order to maintain lower S-swing values. Thus, the technique can be useful to reduce static power dissipation without performance loss. The use of an underlap region between gate and drain can reduce the degree of II through a lower current density, and hence, the selection of optimal underlap length is essential and should be done after the optimization of $J.E$.

I_{ds}-V_{gs} characteristics of Ge JL device for L_{un} = 0 nm and 20 nm is shown in Fig. 4.6*a*. Results depict that L_{un} = 5 nm reduces the tunneling current by nearly 2 orders i.e. from 10^{-8} A to 10^{-10} A along with a marginal reduction in II as the number of decades of current transition is reduced for φ_m (~ 5.20 eV). This can also be confirmed from the graph of *J.E* which shows a minor decrease (Fig. 4.6*b*) in its value from 3.7×10^{12} AVcm^{-3} (L_{un} = 0 nm) to 2.9×10^{12} AVcm^{-3} (L_{un}= 5 nm). The reduction in *J.E* results in a higher threshold voltage while maintaining 4 orders of drain current transition from off-state to on-state. Further increase in L_{un} from 5 nm to 20 nm results in a significant reduction in *J.E* can be seen in reduction in the number of decades of I_{ds} transition at V_{th}. Also, the steep transition in I_{ds} can be seen at higher V_{gs} at L_{un} = 20 nm. As shown in Fig. 4.6*c*, an appropriate value of φ_m (~ 5.05 eV) is important as it further reduces the off-state tunneling current from 10^{-8} A to 10^{-9} A without an underlap while maintaining *S*-swing < 5 mV/decade for a fixed T_{Ge}. Moreover, it can be observed that the increase in tunneling limited off-current with an increase in workfunction (> 5.05 eV) is due to the excess depletion of the film near to the gate edge towards the drain side, which results in significant proximity of valence and conduction band (reduced tunneling width) in JL devices designed without underlap region (L_{un} = 0 nm). However, I_{off} reduces as gate workfunction increases in Ge JL transistor designed with a minimal underlap (L_{un} = 5 nm).

Fig. 4.6*d* shows CB and VB energy levels to compare the tunneling width at the channel-drain junction in JL designed with and without underlap. The energy band profile is extracted for Ge JL transistor with T_{Ge} = 11 nm operated at V_{ds} = 0.9 V along the channel direction at V_{gs} = 0 V and at x, y = $T_{Ge}/2$. The underlap region in JL transistor allows the lateral extension of depletion width and increases the effective channel length [23] in the subthreshold region which increases the tunneling width between VB and CB (Fig. 4.6*d*), and considerably reduces the off-state BTBT. Further reducing φ_m from 5.05 eV to 4.95 eV limits the depletion of the carries in the film and

negative V_{gs} values are required to turn off the device. Contrary to the trend of reduction in I_{off} with φ_m due to lower BTBT current at V_{gs} = 0 V, a reduction in φ_m in a JL MOSFET with L_{un} = 5 nm results in an expected increase in I_{off} which is limited to ~3 nA. Gate material such as $Ta_{0.58}Pt_{0.42}$ [39] would be the most suitable for achieving the desired φ_m values.

4.3 Raised Source/Drain (RSD) Ge JL Transistor

4.3.1 Device Structure

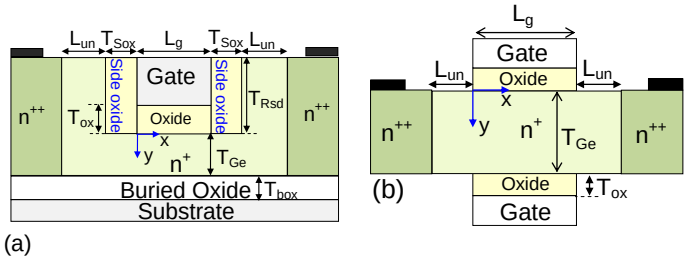

Fig. 4.7: Schematic diagram of (a) Raised Source/Drain and (b) DG Ge JL MOSFET.

The aggressive scaling in transistor dimensions has resulted in Raised Source/Drain (RSD) MOS devices to minimize the source/drain resistance [40-41]. Tang *et al*. [40] demonstrated the methodology by with elevated source/drain JL devices can be fabricated at low cost. Also, the experimental results reported by Wu *et al*. [41-42] on recessed channel accumulation mode Ge based device have shown the potential to achieve higher carrier mobility, low source/drain contact resistance on *n*-type Ge MOS devices, and stronger gate controllability, and hence, makes Ge as a potential candidate for device downscaling. While the results reported in [41-42] are promising and pave path forward to progress with Ge based devices, *S*-swing values $\geq$ 60 mV/decade due to lower current density exhibited by accumulation mode transistors. This section describes RSD Ge JL devices designed with channel doping $\geq 5 \times 10^{18}$ cm^{-3} to facilitate II induced *S*-swing < 60 mV/decade.

Fig. 4.7*a* shows the schematic representation of RSD Ge JL transistor. The performance of RSD Ge JL transistor has been compared with DG Ge JL

MOSFET (Fig. 4.7*b*). Both devices have L_g = 50 nm with GeON as the gate dielectric with a thickness of 1 nm [14], side oxide thickness (T_{Sox}) of 1 nm, T_{Ge} = 7 nm, underlap length (L_{un}) of 10 nm, channel doping (N_{ch}) of 10^{19} cm^{-3} and S/D doping of 10^{20} cm^{-3} with the height of raised S/D portion (T_{RSD}) of 7 nm. Since subthreshold conduction channel in JL transistor is located in the bulk of the film, corner effects are not expected to be significant in RSD JL devices [43]. In order to obtain fair assessment of both the structures, φ_m for RSD and DG JL devices was adjusted to attain nearly similar values of I_{off} at V_{ds} = 0.9 V. The back gate was grounded for RSD architecture, whereas symmetric gate operation is considered for DG device.

4.3.2 I_{ds}-V_{gs} Characteristics of DG and RSD JL Transistor

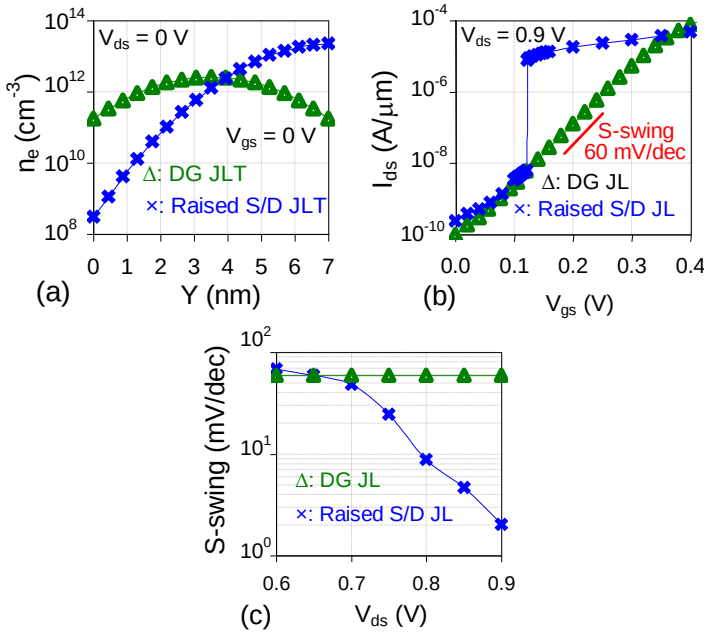

Fig. 4.8: Variation in (a) n_e extracted at mid gate position ($x = L_g/2$, y) for $V_{gs} = V_{ds}$ = 0 V and along y-direction at channel location. (b) I_{ds}-V_{gs} characteristics for RSD and DG Ge JL MOSFETs at V_{ds} = 0.9 V. (c) S-swing with varying V_{ds} for RSD and DG JL devices. The gate workfunction for DG and RSD JL devices are 4.75 eV and 5.05 eV, respectively.

Fig. 4.8*a* shows the n_e across the film at mid-gate position ($x = L_g/2$, y) for RSD and DG Ge JL transistor at V_{gs} = 0 V, respectively. The maximum

electron concentration ($n_{e,max}$) obtained at the back surface ($y = T_{Ge}$) is limited to lower than 10^{14} cm^{-3} in RSD architecture while $n_{e,max}$ in DG MOSFET, obtained at the center ($y = T_{Ge}/2$), is an order lower than that obtained in the RSD topology. Due to reduced $n_{e,max}$ both devices exhibit low I_{off} (~10^{-10} A/μm). Fig. 4.8*b* shows I_{ds}-V_{gs} characteristics of RSD and DG Ge JL device at V_{ds} = 0.9 V. DG JL device exhibits a classical *S*-swing of 60 mV/decade while RSD architecture displays a sharp rise in I_{ds} with *S*-swing ~ 2 mV/decade which yields higher values (~3 orders) of I_{ds} at low gate biases (~0.12 V). The graph shows potential benefits of using a RSD architecture vis-à-vis a DG MOSFET for steep switching applications. The enhanced performance of RSD JL device is due to the wider area over which II can be triggered.

4.3.3 Current Density and IGR in DG and RSD JL Transistor

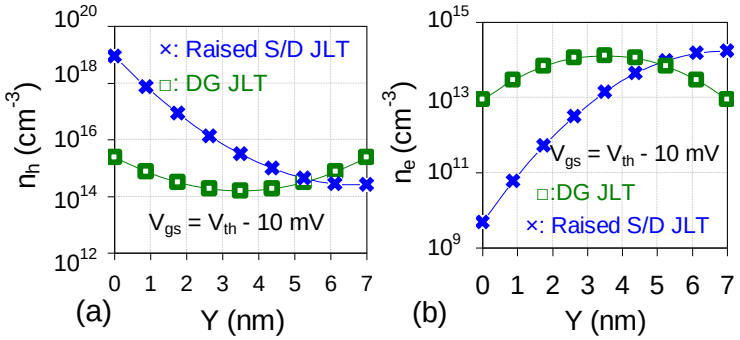

Fig. 4.9: Variation in (a) n_h and (b) n_e extracted across the film at $x = L_g/2$, y along the vertical direction at $V_{gs} = V_{th}$ –10 mV.

In general, II in MOSFET is strongly dependent on the lateral electric field associated with V_{ds}. Due to single gate controllability, lateral electric field in RSD architecture is expected to be higher than in DG MOSFET. The higher value of electric field coupled with an enhanced current density triggers II, which results in a sub-60 mV/decade *S*-swing as shown in Fig. 4.8*c*. Results indicate that for V_{ds} nearly equal to E_g/q, RSD devices do not exhibit dominant II and *S*-swing ~ 65 mV/decade can be observed. This is also consistent with the theory proposed in [35-36] regarding the bias requirement for II. The reduction in *S*-swing from 65 mV/decade (V_{ds} = 0.65 V) to 2

mV/decade (at V_{ds} = 0.9 V) in RSD Ge JL device is due to enhanced electron-hole pair generation which causes dominant FBEs and results in sharp increase in current.

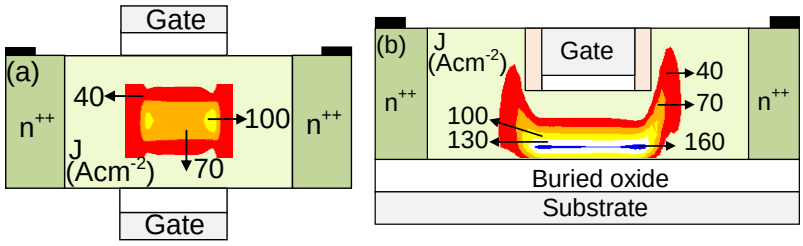

Fig. 4.10: 2D contour plot of the J at V_{gs} = 0.1 V for (a) DG and (b) RSD JL transistor at V_{ds} = 0.9 V.

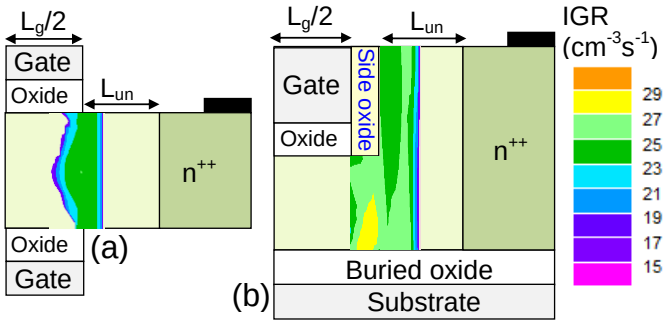

Fig. 4.11: 2D contour plot showing IGR at V_{gs} = 0.1 V for (a) DG and (b) RSD JL transistor at V_{ds} = 0.9 V.

In order to understand the triggering of II in RSD Ge JL device at relatively lower V_{ds} = 0.9 V, Fig. 4.9*a-b* shows the variation in hole and electron concentration at V_{gs} = 0.1 V. As both devices exhibit nearly same $n_{e,max}$ (Fig. 4.8*b*), the improved performance of RSD JL transistor is due to the significantly higher hole concentration underneath the gate. The maximum hole concentration ($n_{h,max}$) before the onset of steep transition is nearly equal to channel doping (~10^{19} cm^{-3}) in RSD devices, whereas DG JL transistor exhibits lower hole concentration of ~10^{15} cm^{-3}. The relatively higher value of $n_{h,max}$ actuates positive a feedback loop, and results in an increased value of J, as shown in Figs. 4.10*a-b*, in RSD architecture as compared to DG MOSFET. The absolute magnitude of J (~160 Acm^{-2}) in RSD JL transistor is ~ ×1.6

higher in comparison with DG JL (~100 Acm^{-2}) MOSFET. Another unique attribute of RSD JL topology is the spreading of *J* over a wider area and is clearly observed in Fig. 4.10*b*.

Fig. 4.11 shows the 2D contour plot of IGR in DG (Fig. 4.11*a*) and RSD (Fig. 4.11*b*) JL device. As the minimum field region in RSD JL device is located at the back surface, the maximum magnitude of IGR (~10^{29} $cm^{-3}s^{-1}$) in RSD JL device is obtained at back surface near to gate edge towards the drain (Fig. 4.11*a*). IGR value corresponding to raised source/drain part, although lower (~10^{27} $cm^{-3}s^{-1}$) than the maximum (~10^{29} $cm^{-3}s^{-1}$), is still higher than the maximum IGR value (~10^{25} $cm^{-3}s^{-1}$) exhibited by DG JL transistor as shown in Fig. 4.11*b*. The 4 orders (at back surface) and 2 orders (at raised part) higher magnitude of IGR in RSD JL device in comparison with DG JL device is beneficial to augment the degree of II leading to sharp rise in I_{ds} shown in Fig. 4.8*b*. Apart from *S*-swing, another important aspect in the design of RSD devices is the off-current that requires the consideration of BTBT. Due to the non-existence of steep *S*-swing in DG JL transistor (Fig. 4.9*b*), subsequent text is focused only on RSD architecture.

4.3.4 BTBT in RSD Ge *JL Transistor*

I_{ds}-V_{gs} characteristics of RSD JL transistor with the inclusion and exclusion of BTBT is shown in Fig. 4.12*a*. The observed tunneling component in I_{ds} at lower V_{gs} is similar to experimentally reported results in [23-24], [41]. Although RSD JL devices exhibit steep *S*-swing at V_{ds} = 0.9 V, I_{ds} obtained considering BTBT model at V_{gs} = 0 V is ~2 orders higher i.e. I_{ds} increases from 10^{-9} A (without BTBT) to 10^{-7} A (with BTBT). The on-to-off current ratio without considering BTBT in RSD Ge JL device is nearly equal to 4.5 orders, whereas the same degrades to ~3 orders with the inclusion of BTBT. This increase in I_{off} is due to the proximity between VB and CB in the raised portion of the film which facilitates tunneling of electrons from VB of the channel to CB of the drain.

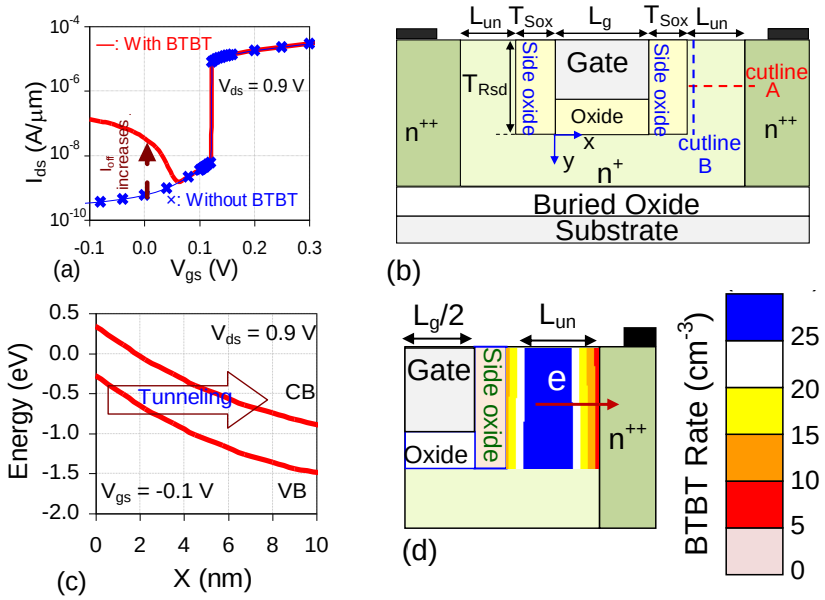

Fig. 4.12: (a) I_{ds}-V_{gs} characteristics of RSD Ge JL transistor with BTBT and without BTBT model, (b) schematic view showing the cutline A drawn from $x = L_g+T_{Sox}$ to $x = L_g+T_{Sox}+L_{un}$ at $y = -T_{RSD}/2$. (c) Variation in VB and CB energy extracted along the cutline A, and (d) 2D contour plot showing BTBT generation rate in RSD JL transistor.

In DG JL transistor, the depletion of electrons towards the gate edge near to the drain is responsible for tunneling current, whereas in RSD devices tunneling prone region is located in the raised part of source/drain regions. The reason for shift in the location of tunneling is due to maximum depletion of electrons adjacent to the vicinity of side oxide edge which triggers the tunneling of electrons. This can be confirmed through the variation in VB and CB energy levels, extracted along the cutline A in Fig. 4.12*b*, shown in Fig. 4.12*c* and 2D contour plot of BTBT generation rate in Fig. 4.12*d* at V_{gs} = -0.1 V. The energy band profiles are extracted in the *x*-direction along the cutline (A) drawn from $x = (L_g+T_{Sox})$ to $x = (L_g+T_{Sox}+L_{un})$ at $y = -T_{RSD}/2$ (Fig. 4.12*b*). The tunneling of electrons owing to the significant overlap between the filled VB states corresponding to empty CB states leaves holes in the channel region. Moreover, the peak magnitude (~10^{27} $cm^{-3}s^{-1}$) of the BTBT generation rate in Fig. 4.12*d* is observed in the raised portion of RSD JL device.

Successive accumulation of tunneling generated holes with the reduction in V_{gs} to negative values increases the channel potential, and thus, I_{off}.

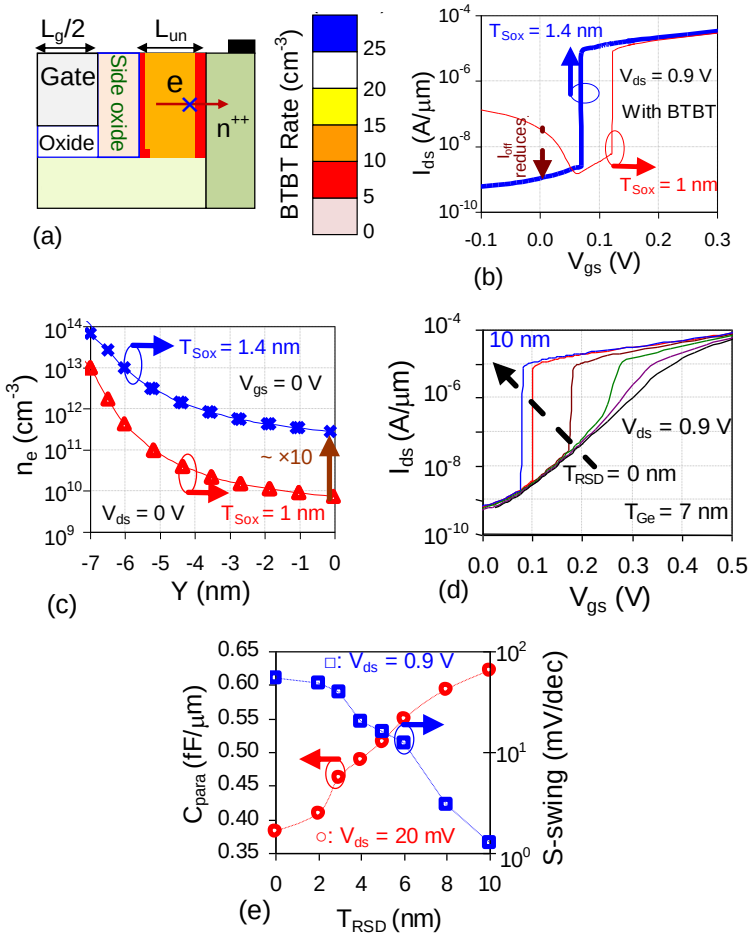

Fig. 4.13: (a) Contour plot showing BTBT generation rate for T_{Sox} = 1.4 nm at V_{gs} = -0.1 V, (b) I_{ds}-V_{gs} characteristics with T_{Sox} = 1 nm and T_{Sox} = 1.4 nm. (c) Variation in n_e at (x = L_g+T_{Sox}+0.5 nm, y) along the cutline B shown in Fig. 4.12*b* away from the side oxide at V_{ds} = 0 V. The value of -7 nm on the x-axis of Fig 4.13*c* indicates the top of the RSD region. (d) I_{ds}-V_{gs} characteristics as a function of L_{un} and (e) variation of parasitic capacitance (C_{para}) and S-swing with T_{RSD} at V_{ds} = 20 mV.

The magnitude of BTBT generation rate from raised portion near to drain side can be reduced by using a relatively thicker T_{sox} which can reduce the electric field in region adjacent to the side oxide, and also lowers the extent of depletion in raised portion. The reduction in degree of depletion of electrons

lowers BTBT generation rate (~ 10^{15} $cm^{-3}s^{-1}$) as shown in Fig. 4.13*a* and reduces I_{off} from 10^{-7} A to 10^{-9} A (Fig. 4.13*b*). In order to confirm the same, n_e in Fig. 4.13*c* is extracted 0.5 nm away from the side oxide along the *y*-direction (cutline B in Fig. 4.12*b*) in the raised portion at V_{gs} = V_{ds} = 0 V. Higher n_e (×10) for T_{Sox} = 1.4 nm in raised part of JL device is beneficial as it further assists to enhance the degree of II through a higher *J* while suppressing tunneling at lower V_{gs} by limiting the extent of depletion. The improved performance of the device with relatively thicker T_{Sox} can be seen in Fig. 4.13*b* where I_{ds} achieves steep transition of ~4 decades at V_{gs} = V_{th}.

Although the raised part of source/drain is beneficial in enhancing II, it also contributes to increased parasitics. Fig. 4.13*d* shows the dependence of parasitic capacitance (C_{para}) and *S*-swing on the height of RSD region (T_{RSD}). While JL device with T_{RSD} = 0 nm triggers the II, its extent is not significant enough to achieve sharp rise in I_{ds}. The *S*-swing obtained for planar device (T_{RSD} = 0 nm) is limited to ~48 mV/decade. An increase in T_{RSD} results in an increase in fringing component of C_{para}, but also provides greater area for II An increase in T_{RSD} from 2 nm to 8 nm increases C_{para} by 50% while reducing *S*-swing by ~10 times. A possible optimization can be adopted to limit the value of T_{RSD} such that C_{para} does not increase by more than 50% of the non-RSD architecture. In present case, this condition is satisfied for T_{RSD} = 7 nm.

4.3.5 Impact of Quantum Confinement Effects in RSD JL Transistor

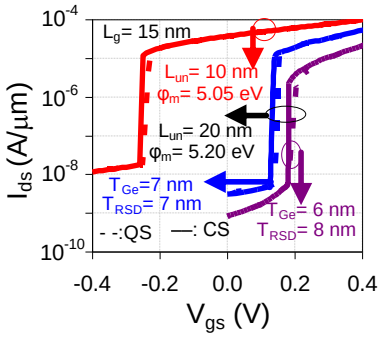

Fig. 4.14: I_{ds}-V_{gs} characteristics for 15 nm RSD Ge JL device with L_{un} = 10 nm and 20 nm obtained through Quantum (QS) and Classical (CS) simulations.

Fig. 4.14 shows steep switching in RSD JL devices with L_g = 15 nm and T_{Sox} = 1.4 nm by considering Quantum Confinement Effects (QCEs). Quantum simulations are performed by solving Schrödinger equation consistently with Poisson equation [34]. The methodology used to analyze the QCEs is consistent with the work reported by [44]. The marginal shift (Fig. 4.14) in V_{th} was observed because QCEs does not significantly affect II. Result highlights that the increase in off-current at lower gate length can be reduced by using a longer L_{un} ~ 20 nm and higher φ_m ~ 5.20 eV, or by reducing T_{Ge} (6 nm) and increasing T_{RSD} (8 nm) to compensate for the reduction in II.

4.3.6 Impact of Vertical Doping Gradient in RSD JL Transistor

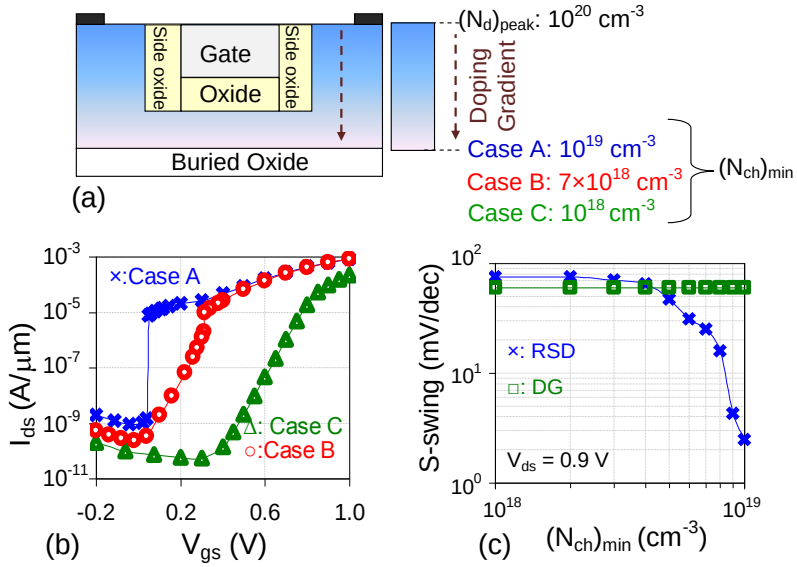

Fig. 4.15: (a) Schematic diagram of RSD Ge JL MOSFET with vertical doping profile. Three different cases (A, B and C) with minimum channel doping $(N_{ch})_{min}$ of 10^{19} cm^{-3}, 7×10^{18} cm^{-3} and 10^{18} cm^{-3} are considered in the analysis. (b) I_{ds}-V_{gs} characteristics for $(N_{ch})_{min} = 10^{19}$ cm^{-3} (Case A), $(N_{ch})_{min} = 7\times10^{18}$ cm^{-3} (Case B) and $(N_{ch})_{min} = 10^{18}$ cm^{-3} (Case C). (c) Variation in *S*-swing with $(N_{ch})_{min}$ for DG and RSD JL transistors.

While RSD JL device is useful for enhancing II, recent results reported by Wu *et al*. [11] on Ge recessed channel devices (with a doping gradient in the

vertical direction) have not shown sharp transition in I_{ds} at V_{ds} ~1 V. To understand the reasons for the same, devices with the vertical doping gradient in the Ge film is analyzed. The doping profile considered in the analysis (Fig. 4.15*a*) is of Gaussian type with maximum value of ~10^{20} cm^{-3} at the top of source/drain regions. Three separate cases with the minimum doping $(N_{ch})_{min}$, as shown by cases A, B and C, at $y = T_{Ge}$ have been considered. The presence of doping gradient in the *y*-direction reduces the number of electrons available for II, and thus, the extent of impact generated power per unit volume in the film is reduced. Fig. 4.15*b* shows the I_{ds}-V_{gs} characteristics of RSD JL transistor with vertical doping gradient. *S*-swing values determined from I_{ds}-V_{gs} (Fig. 4.15*b*) for $(N_{ch})_{min}$ = 10^{18} cm^{-3} is 68 mV/decade, whereas *S*-swing of ~3 mV/decade with nearly 4 decades of current transition is obtained for $(N_{ch})_{min}$ = 10^{19} cm^{-3}. The dependence of *S*-swing on $(N_{ch})_{min}$ is shown in Fig. 4.15*c*. Results indicate that a minimum doping of 5×10^{18} cm^{-3} should be maintained in the film to facilitate a reasonable degree of II and to achieve sub-60 mV/decade current transition.

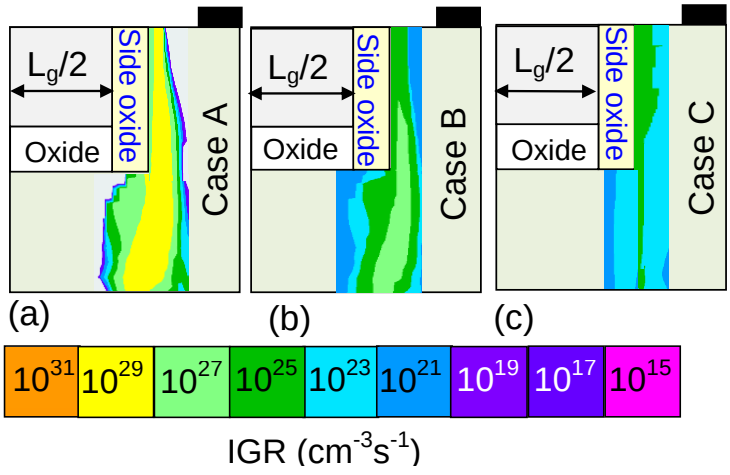

Fig. 4.16: Contour plot showing IGR for (a) Case A, (b) Case B and (c) Case C.

2D Contours for IGR shown in Fig. 4.16*a-c* for three different $(N_{ch})_{min}$ values also confirm the degradation in II with reduction in $(N_{ch})_{min}$. A significant reduction in IGR from 10^{29} $cm^{-3}s^{-1}$ (Fig. 4.16*a*) to 10^{24} $cm^{-3}s^{-1}$ (Fig.

4.16*c*) results in an increase in *S*-swing from 3 mV/decade to 68 mV/decade for $(N_{ch})_{min}$ varying from 10^{19} cm^{-3} to 10^{18} cm^{-3}, respectively. Although I_{off} obtained at relatively lower channel doping (10^{18} cm^{-3}) is ~10 times lower in comparison to a device designed with channel doping of 10^{19} cm^{-3}, the advantage of a higher $(N_{ch})_{min}$ is reflected in the 4 orders of current transition for a 100 mV change in V_{gs}. Thus, $(N_{ch})_{min}$ can be a critical parameter governing extent of impact ionization in RSD JL devices. For $(N_{ch})_{min}$ = 5×10^{18} cm^{-3}, *S*-swing of ~50 mV/decade is obtained, whereas for $(N_{ch})_{min}$ = 7×10^{18} cm^{-3}, a sub-thermal off-to-on transition with *S*-swing of 23 mV/decade is preserved. RSD Ge JL devices should be designed such that the vertical doping gradient can be suppressed and $(N_{ch})_{min}$ is limited to ~5×10^{18} cm^{-3}.

4.4 Overcoming Single Transistor Latch

While the enhanced degree of FBEs is beneficial to achieve a sharp increase in I_{ds} from off-to-on state with a sub-60 mV/decade transition [45] due to higher degree of II, the extreme case of the same can result in the device being latched to the on-state [30]. Such a scenario is undesirable as the transistor action and functioning are hindered. While turning-off JL device can be critical due to heavy doping (~10^{19} cm^{-3}) [46], the issue can be aggravated if FBEs are not properly controlled and device enters into the latch condition [30], [47]. Latching has been considered as detrimental effect [48-49] as device cannot be turned off, and results in an increase in power dissipation [50]. Previously reported techniques for suppressing latching in inversion mode [51-55] devices required additional fabrication steps such as silicidation of source/drain region [51], using SiGe as source material [52-53], altering the properties of the channel/buried oxide interface [54] and design optimization [55]. Although proposed techniques for conventional inversion mode MOSFETs are useful for suppressing latch, adopting the same would essentially affect the generation of electron-hole pairs, and thereby, counteract on the possibility to achieve sub-60 mV/decade current transition.

The lower energy bandgap along with higher carrier mobility and ionization rates facilitates stronger degree of II FBEs, and therefore, Ge JL devices are more prone to latch condition in comparison to Si counterparts. This can essentially limit the usability of steep switching Ge JL devices if FBEs are not adequately controlled. Therefore, this section investigates the occurrence of Single Transistor Latch (STL) effect due to variation in various device parameters in symmetrically biased (V_{fg} = V_{bg}) DG JL transistor, and its suppression by utilizing independent gate operation i.e. ($V_{fg} \neq V_{bg}$).

4.4.1 Device Structure and Analysis: Symmetric Gate Operation

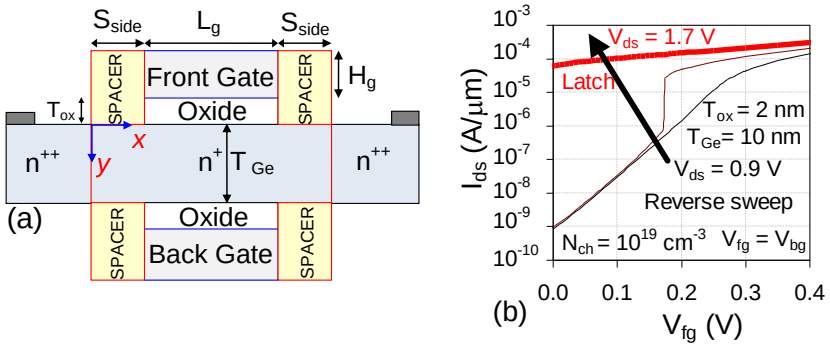

Fig. 4.17: (a) Schematic diagram of DG Ge JL MOSFET, and (b) I_{ds}-V_{fg} characteristics with varying V_{ds} from 0.9 V to 1.7 V. V_{ds} in Fig. 4.17*b* is varied in the interval of 0.4 V and both gates are tied together (V_{fg} = V_{bg}).

In order to investigate the latching phenomena and its suppression through independent gate operation, DG Ge JL MOSFETs shown in Fig. 4.17*a* is analyzed with GeON as the gate dielectric with a thickness (T_{ox}) of 2 nm, film thickness (T_{Ge}) of 10 nm, spacer thickness (S_{side}) of 15 nm, gate electrode height (H_{sp}) of 50 nm and gate length (L_g) of 50 nm. Fig. 4.17*b* shows drain current (I_{ds}) – front gate voltage (V_{fg}) characteristics with varying V_{ds} from 0.9 V to 1.7 V. At a lower V_{ds} of 0.9 V, gradual transition in I_{ds} with a classical *S*-swing of 60 mV/decade is observed which implies that II is not significant at 0.9 V in the device. This particular result at V_{ds} = 0.9 V is in agreement with the theory of II in Ge based transistor proposed in [35-36].

As the V_{ds} increases, *S*-swing reduces from 60 mV/decade to 2 mV/decade at V_{ds} = 1.3 V along with a shift in V_{th} from 0.25 V to 0.17 V. The reduction in V_{th}, increase in number of decades of I_{ds} transition, and reduction in *S*-swing with an increase in V_{ds} are in good qualitatively agreement with the results reported by Lee *et al*., [45] for Si JL transistor. A higher V_{ds} of 1.7 V further augments II with the generation of significant number of electrons which cannot be depleted even at negative gate biases, and the device is latched to the on-state indicating a complete loss of gate controllability.

4.4.2 Asymmetric Gate Operation to Suppress Latch

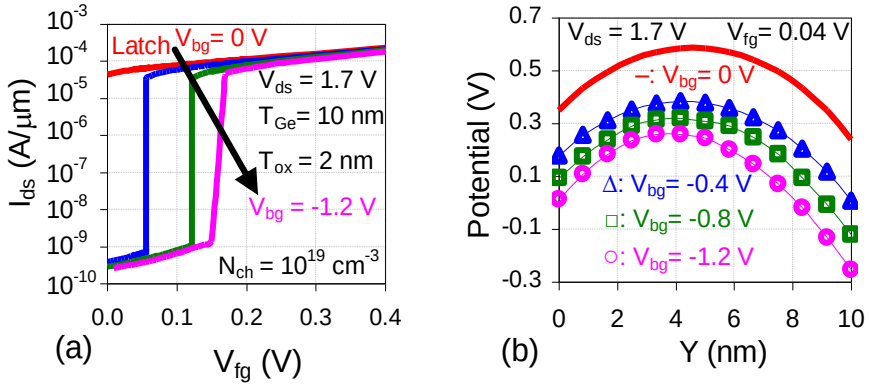

Fig. 4.18: (a) I_{ds}-V_{fg} characteristics of *n*-type Ge JL transistor, (b) variation of electrostatic potential extracted at V_{fg} = 40 mV across the film at ($x = L_g/2$, y) with varying V_{bg} from 0 V to -1.2 V.

In order to regain transistor functionality by overcoming the latch condition, the devices are operated in asymmetric mode i.e. different voltages are applied at front (V_{fg}) and back (V_{bg}) gates. Fig. 4.18*a* shows I_{ds}-V_{fg} characteristics of Ge JL transistor with varying V_{bg}. At V_{bg} = 0 V, transistor continues to be in the latched state. As V_{bg} is reduced to -0.4 V, the sharp current transition (*S*-swing ~ 1 mV/decade) is reclaimed. Further, a reduction in V_{bg} to -1.2 V shifts V_{th} to more positive values (~ 0.17 V) while maintaining the sharp increase in I_{ds} i.e. the device does not remain latched to on-state but can be turned-off. The V_{th} in steep switching devices is defined as the gate voltage corresponding to sharp rise in drain current [56]. Moreover, the

impact of higher V_{bg} can be observed through a slight increase in *S*-swing i.e. from ~1 mV/decade to ~4 mV/decade.

In order to understand the shift in V_{th} to higher V_{fg} and increase in *S*-swing, Fig. 4.18*b* shows the potential distribution underneath the gate extracted along the cutline ($x = L_g/2$, y) at V_{fg} = 40 mV for V_{bg} varying from 0 V to -1.2 V. The maximum value of the potential underneath the gates in channel region for fixed V_{fg} = 40 mV reduces from ~ 0.6 V (latched state @ V_{bg} = 0 V) to ~ 0.26 V (non-latched state @ V_{bg} = -1.2 V). The reduction in electrostatic potential is attributed due to the depletion of electrons because of the applied negative V_{bg}. The lower n_e at higher V_{bg} reduces the number of carriers available to facilitate II, and thus, results in higher V_{th} corresponding to steep transition point with a marginal increase in *S*-swing.

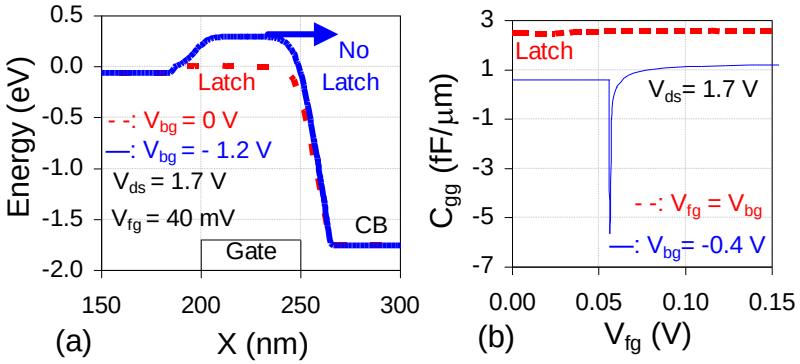

Fig. 4.19: Variation in (a) CB energy extracted along the *x*-direction at channel location at V_{bg} = 0 V and V_{bg} = -1.2 V, and (b) C_{gg} with respect to V_{fg} for V_{bg} = -0.4 V and $V_{fg} = V_{bg}$.

Fig. 4.19*a* shows the variation in CB energy extracted along the *x*-direction at the channel location before the onset of steep transition at V_{bg} = 0 V, V_{bg} = -1.2 V and V_{fg} = 40 mV. JL device with negative bias at the back gate i.e. V_{bg} = -1.2 V exhibits barrier (~ 0.3 eV) between source and channel regions whereas the barrier is absent at V_{bg} = 0 V. The presence of finite barrier indicates depletion of electrons due to negative V_{bg}. The barrier between source and channel regions restricts the flow of electrons and turns-off the device at lower V_{fg}. Fig. 4.19*b* shows the variation in C_{gg} with respect

to V_{fg} in JL device with symmetric (V_{bg} = V_{fg}) and independent gate operation (V_{bg} = -0.4 V). JL device operating in the latch state exhibits higher value of C_{gg} ~ 2.5fF/μm which cannot be reduced even at lower V_{fg}. The higher value of C_{gg} corresponds to higher n_e in the film. However, C_{gg} exhibits lower value (~ 0.63fF/μm @ V_{fg} = 0 V) owing to depletion of electrons when V_{bg} is fixed at -0.4 V. As V_{fg} increases, II becomes dominant and results in negative values of C_{gg} corresponding to *S*-swing < 10 mV/decade [57] at V_{fg} = V_{th} = 56 mV. Thereafter, C_{gg} increases as V_{fg} rises to higher values and attains positive values due to dominant conduction in the film being governed by electrons.

4.4.2.1 Generation and Recombination Rates

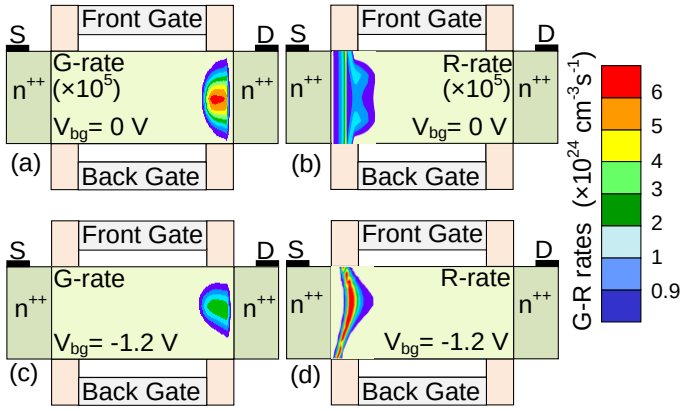

Fig. 4.20: 2D contour plot showing (a) Generation rate (G-rate) at V_{bg} = 0 V, (b) Recombination rate (R-rate) at V_{bg} = 0 V, (c) G-rate at V_{bg} = -1.2 V and (d) R-rate at V_{bg} = -1.2 V. All results are extracted at V_{fg} = 0.04 V and V_{ds} = 1.7 V.

Fig. 4.20 shows the 2D contour plot of Generation rate (G-rate) and Recombination rate (R-rate) with V_{bg} = 0 V (Figs. 4.20*a*-*b*) and with V_{bg} = -1.2 V (Figs. 4.20*c*-*d*). Figs. 4.20*a*-*b* depict that JL device operating in latch condition at V_{bg} = 0 V exhibits ×6 higher value of G-rate (~6×10^{29} cm^{-3} s^{-1}) in comparison with R-rate (~10^{29} $cm^{-3}s^{-1}$). While the higher value of G-rate is beneficial to augment II, it can also result in a loss of gate controllability. Although, the independent gate operation in JL device with V_{bg} = -1.2 V lowers G-R rates (~ 10^{24} $cm^{-3}s^{-1}$), the observed reduction is more profound in

G-rate. This is because the applied negative bias accumulates more number of holes at the back gated surface. Since source is maintained at relatively lower potential in comparison to drain (V_{ds} = 1.7 V), the accumulated holes start recombining towards the heavily doped source region. A ×2.5 times increase in R-rate (6×10^{24} $cm^{-3}s^{-1}$) in comparison with G-rate (2.2×10^{24} $cm^{-3}s^{-1}$) at source side reduces the electron concentration, and thus, reduces the degree of II in the film as shown in Fig. 4.18*a*.

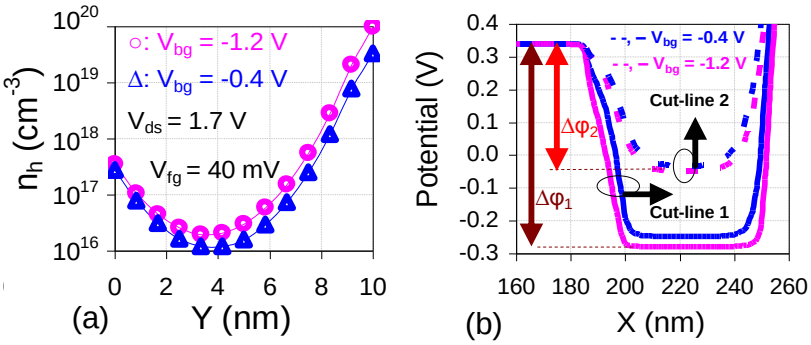

Fig. 4.21: Variation in (a) hole concentration extracted across the film at x = $L_g/2$, y and (b) potential distribution extracted in x-direction along the cut-line 1: at back surface and cut-line 2: at channel location in the film at V_{bg} = -0.4 V and -1.2 V. All results are extracted at V_{fg} = 0.04 V and V_{ds} = 1.7 V

R-rate can be understood by evaluating the variation in hole concentration and potential distribution in the film as shown in Figs. 4.21*a*-*b*. n_h is extracted across the film at midgate i.e. x = $L_g/2$, y (Fig. 4.21*a*), whereas potential distribution is shown along the cut-line 1, which is at back surface while cut-line 2 is at the channel for V_{bg} = -0.4 V and V_{bg} = -1.2 V, respectively (Fig. 4.21*b*). Fig. 4.21*a* depicts that n_h increases from 3×10^{19} cm^{-3} to 10^{20} cm^{-3} as V_{bg} reduces from -0.4 V to -1.2 V, respectively at the back surface of the film. This increase in n_h (at V_{bg} = -1.2 V) at back surface raises the potential barrier height between source-channel region (Fig. 4.21*b*), and thus, reduces the recombination of the carriers towards the source side at the back surface. Furthermore, to understand the location of peak magnitude of R-rate, the potential distribution in Fig. 4.21*b* is compared. A reduction in the potential barrier ($\Delta\varphi$) i.e. $\Delta\varphi_1 > \Delta\varphi_2$ from -0.28 V (at back surface) to -0.05 V (at

channel location) at V_{bg} = -1.2 V and from -0.25 V to -0.032 V at back gate bias of -0.4 V is observed. This reduction in barrier allows carriers to recombine towards the source at the back surface, and thus, results in a peak magnitude of R-rate at the center of the film.

4.4.2.2 Impact Back Gate Bias on *J.E*

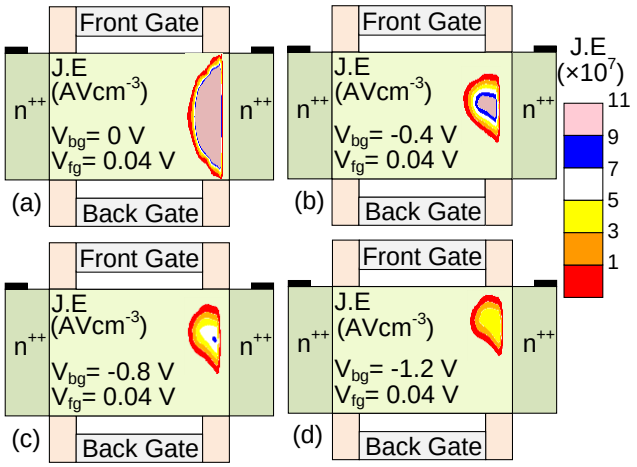

Fig. 4.22: 2D contour plot of *J.E* at (a) V_{bg} = 0 V, (b) V_{bg} = -0.4 V, (c) V_{bg} = -0.8 V and (d) V_{bg} = -1.2 V. All the results are extracted at V_{fg} = 0.04 V and V_{ds} = 1.7 V.

In order to confirm the influence of V_{bg} in reducing II, 2D contour plots of *J.E* is shown in Figs. 4.22*a-d*. *J.E* is extracted at V_{fg} = 40 mV with varying V_{bg} from 0 V to -1.2 V. The high value of *J.E* signifies enhanced power per unit volume. Applying a negative V_{bg} reduces the number of electrons available to facilitate II, and thus, *J* decreases which considerably lowers the product *J.E*, a critical parameter governing II. The peak magnitude of *J.E* successively reduces from 10^{11} AVcm^{-3} (Fig. 4.22*a*) to 3×10^{7} AVcm^{-3} (Fig. 4.22*d*) as V_{bg} reduces from 0 V to -1.2 V. The significant reduction of ~10^{3} times in *J.E* values is sufficient for gate to regain controllability over the channel, and consequently turn-off the transistor with a sub-60 mV/decade transition in I_{ds}. Another key attribute of JL transistor biased with fixed negative potential is the area over which II is significant. JL transistor with V_{bg} = 0 V (Fig. 4.22*a*) exhibits II over a wider area which is responsible for enhanced generation of

the carriers in the film. However, the area over which II occurs successively reduces, and becomes localized towards top half of the film (near to the gate edge towards drain) as V_{bg} reduces from 0 V to -1.2 V (Fig. 4.12*b*-*d*).

4.4.2.3 Occurrence of Latch due to Variation in N_d, T_{ox} and T_{Ge}

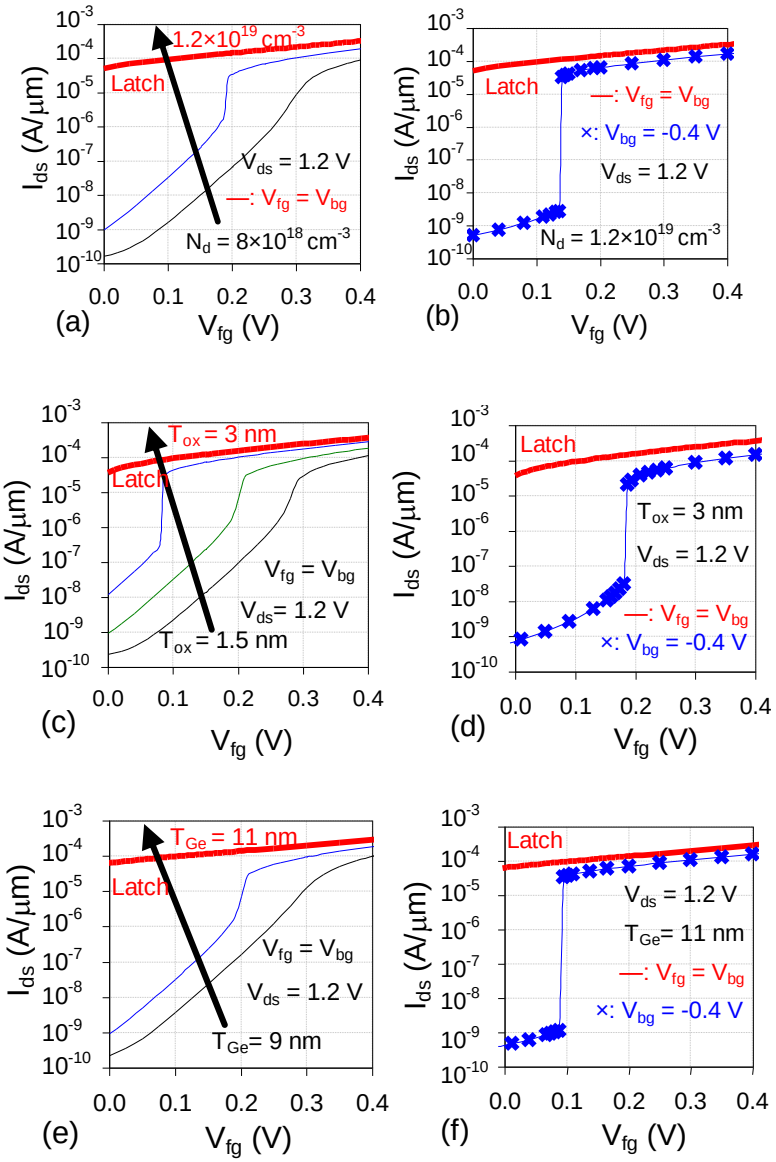

Fig. 4.23: I_{ds}-V_{fg} characteristics of *n*-type Ge JL device (a) V_{fg} = V_{bg} for N_d varying from 8×10^{18} cm^{-3} to 1.2×10^{19} cm^{-3}, (b) V_{bg} = -0.4 V at N_d = 1.2×10^{19} cm^{-3}, (c) V_{fg} = V_{bg} for T_{ox} varying from 1.5 nm to 3 nm, (d) V_{bg} = -0.4 V at T_{ox} = 3 nm, (e) V_{fg} = V_{bg} for T_{Ge} varying from 9 nm to 11 nm, and (f) V_{bg} = -0.4 V at T_{Ge} = 11 nm.

Unlike inversion mode devices, latching in JL devices not only occurs at higher V_{ds} values, but is also observed through an increase in N_d, T_{ox} and T_{Ge} as an increase in these tend to enhance *J.E*. In order to analyze the same in *n*-type Ge JL MOSFETs, V_{ds} is fixed at 1.2 V. Figs. 4.23*a-f* shows I_{ds}-V_{fg} characteristics of JL transistor with a variation in N_d from 8×10^{18} cm^{-3} to 1.2×10^{19} cm^{-3} (Fig. 4.23*a*), T_{ox} from 1.5 nm to 3 nm (Fig. 4.23*c*) and T_{Ge} from 9 nm to 11 nm (Fig. 4.23*e*). An increase in N_d, T_{ox}, and T_{Ge} primarily reduces the extent of depletion of carriers in semiconductor film, and thus, increases the number of carriers which strengthen II through an increase in *J.E*.

It is observed from Fig. 4.23*a* that in a symmetric (V_{fg} = V_{bg}) JL device at N_d = 8×10^{18} cm^{-3} or 10^{19} cm^{-3}, gate is able to deplete the excess carriers generated due to II and the device could be turned-off with a low I_{off} and *S*-swing < 60 mV/decade. Further, an increase in N_d to 1.2×10^{19} cm^{-3} leads to a greater number of carriers in the channel, and latch is triggered as the gate is unable to turn-off the device. Fig. 4.23*b* shows the suppression of latch in JL transistor with V_{bg} = -0.4 V. Fig. 4.23*c* shows the occurrence of latch effect due to an increase in T_{ox}. An increase in T_{ox} enhances the degree of II due to the reduction in the vertical field, and the same is evident from the increased number of decades of I_{ds} transition. At T_{ox} = 3 nm, the device is unable to overcome the positive feedback loop and is driven into the latched state. The transistor action can be reclaimed by applying a negative V_{bg} (Fig. 4.23*d*). Additionally, an increase in T_{Ge} can also trigger the device into latched state (Fig. 4.23*e*). It can be observed that the use of negative V_{bg} reduces *J* resulting from thicker film, and thus, restores the transistor functionality as shown in Fig. 4.23*f*.

4.4.3 Latch and its Suppression in p-type JL Transistor

Fig. 4.24 shows the occurrence of the latch effect, and its suppression in *p*-type Ge JL at V_{ds} = -2.2 V (Fig. 4.24*a*), T_{Ge} = 11 nm (Fig. 4.24*b*), T_{ox} = 3 nm (Fig. 4.24*c*) and N_d =1.2×10^{19} cm^{-3} (Fig. 4.24*d*). The latch effect in *p*-type Ge JL device is analyzed by varying one parameter while keeping all other

parameters fixed. The asymmetric gate operation of *p*-type JL device is realized at V_{bg} = 0.4 V. Since holes have lower mobility than electrons, II generated power per unit volume in *p*-type Ge JL device is relatively lower in comparison to *n*-type devices. Therefore, higher value of V_{ds} is required to trigger II in *p*-type JL device. In *p*-type JL transistor, impact generated electrons accumulate at higher potential region, whereas holes generated due to II contribute to I_{ds} in *p*-type JL devices. The successive accumulation of electrons in *p*-type JL devices triggers FBEs and results in a sharp I_{ds} transition.

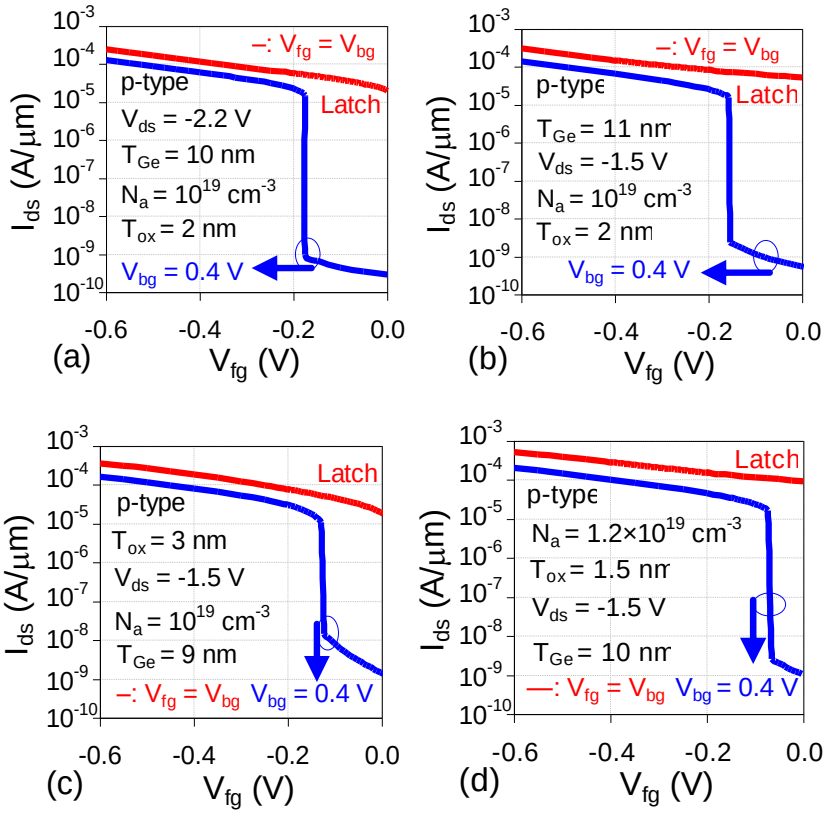

Fig. 4.24: I_{ds}-V_{fg} characteristics of symmetric (V_{fg} = V_{bg}) and independent (V_{bg} = 0.4 V) gate *p*-type Ge JL transistor at (a) V_{ds} = -2.2 V and T_{Ge} = 10 nm, (b) T_{Ge} = 11 nm and V_{ds} = -1.5 nm, at (c) T_{ox} = 3 nm and (d) N_d =1.2 ×10^{19} cm^{-3}.

The occurrence of latch phenomena due to excess generation of holes because of variation in V_{ds}, T_{Ge}, T_{ox} and N_d can be suppressed by applying

positive V_{bg} for *p*-type JL devices. It can be observed from Fig. 4.24 that the extent of II induced FBEs increases with an increase in V_{ds}, T_{Ge}, T_{ox} and N_d, and results in the latch condition. The occurrence of latch can be suppressed with V_{bg} of 0.4 V which results in depletion of excess holes generated due to II and turns off the transistor while preserving a *S*-swing < 10 mV/decade.

4.4.4 Impact of Back Gate Bias on off-state BTBT

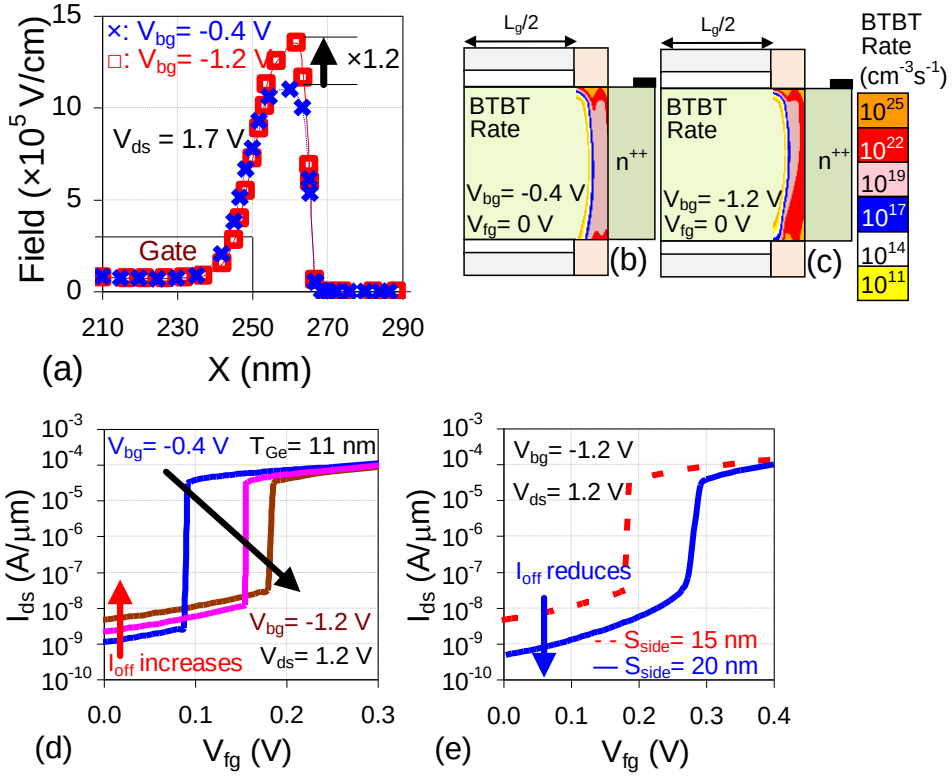

Fig. 4.25: (a) Variation in electric field extracted along the channel direction. 2D contour plot showing tunneling generation rate at (b) V_{bg} = -0.4 V and (c) V_{bg} = -1.2 V. I_{ds}-V_{fg} characteristics of DG JL transistor with varying (d) V_{bg} from -0.4 V to -1.2 V and (e) with spacer thickness of 15 nm and 20 nm biased at V_{bg} = -1.2 V. Results shown in Fig. 4.25*a*-*c* are extracted at V_{fg} = 0 V and V_{ds} = 1.2 V.

In order to estimate the variation in tunneling current at lower V_{fg} with varying V_{bg}, BTBT is considered in the analysis. Kao *et al*. [58] have reported that tunneling current in Ge based transistors is dominated by direct tunneling

of the carriers from valence band to conduction band [29]. Hence, the effective mass for electrons and holes corresponding to the direct bandgap in Ge is considered in the analysis. While the application of negative V_{bg} in Ge JL transistors is indeed beneficial to suppress latch, it increases the potential difference between channel and drain region. The higher potential difference results in an enhanced electric field at the gate edge near to drain side, and yields higher tunneling current at lower V_{fg}. Fig. 4.25*a* shows the electric field distribution in *n*-type Ge JL transistor obtained at the location of the conduction channel along the *x*-direction at V_{fg} = 0 V and V_{ds} = 1.2 V. The field distribution is compared at V_{bg} = -0.4 V and V_{bg} = -1.2 V. A ~×1.2 times increase in the electric field i.e. from ~8×10^5 V/cm (V_{bg} = -0.4 V) to ~10^6 V/cm (V_{bg} = -1.2 V) results in close proximity between valence and conduction band to facilitate the tunneling of electrons [29].

Fig. 4.25*b*-*c* shows the 2D contour plot of BTBT generation rate at V_{bg} = -0.4 V and -1.2 V for fixed V_{fg} = 0 V and V_{ds} = 1.2 V. The increase in V_{bg} significantly enhances the BTBT generation rate from 10^{19} $cm^{-3}s^{-1}$ at V_{bg} = -0.4 V (Fig. 4.25*b*) to 10^{22} $cm^{-3}s^{-1}$ at V_{bg} = -1.2 V (Fig. 4.25*c*). The tunneling of electrons results in greater number of holes in VB, and thus, successive accumulation of holes in the film at lower V_{fg} raises the channel potential and increases I_{off} as shown in Fig. 4.25*d*. An increase (~×5 times) in I_{off} i.e. I_{off} = 10^{-9} A/μm (@ V_{bg} = -0.4 V) to I_{off} = 5×10^{-9} A/μm (@ V_{bg} = -1.2 V) is observed which not only deteriorates on-to-off current ratio but also increases the static power dissipation.

The increase in I_{off} at V_{bg} = -1.2 V can be limited by designing DG Ge JL transistors with relatively thicker sidewall spacer which lowers the electric field associated with the drain, and thus, can be utilized to extend the depletion width beyond the gate edge. The reduction in lateral field at the gate edge towards drain increases the tunneling width between VB and CB and reduces BTBT. In order to confirm the behavior of JL transistor with relatively thicker sidewall spacer thickness (S_{side}), Fig. 4.25*e* shows I_{ds}-V_{fg}

characteristics for L_{sp} = 15 nm and 20 nm at V_{bg} = -1.2 V and V_{ds} = 1.7 V. The reduction in off-state tunneling is significant as ×10 times lower value of I_{off} i.e. I_{off} ~8×10^{9} A (@ L_{sp} = 15 nm) and I_{off} ~8×10^{10} A (@ L_{sp} = 20 nm) is achieved with a wider spacer.

4.4.5 Tunable Hysteresis in Asymmetrically Biased DG Ge JL Transistor

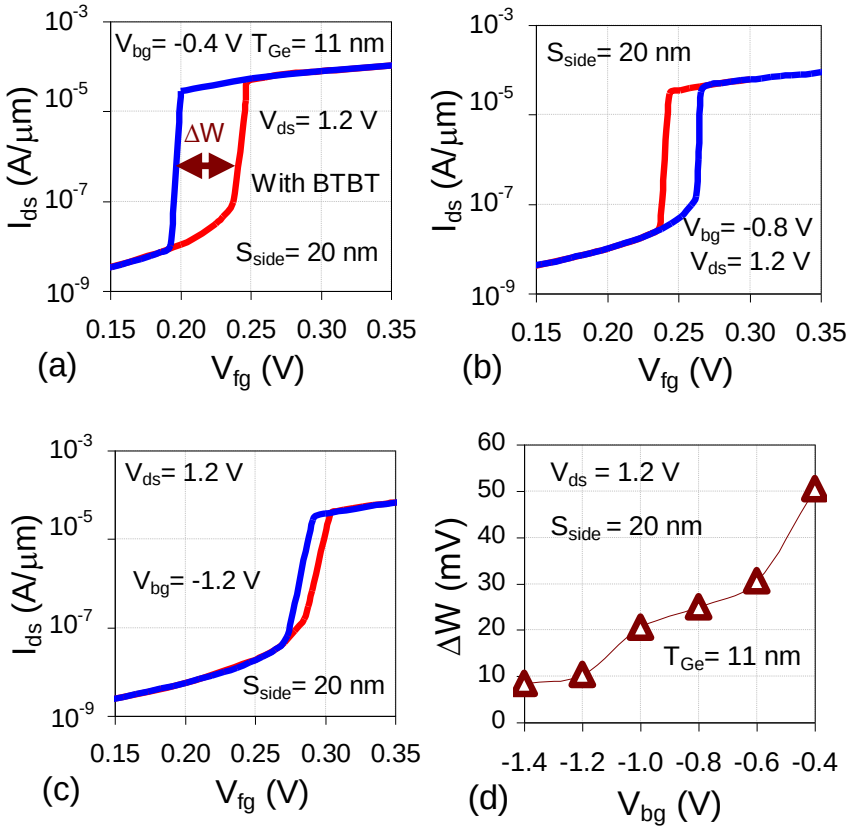

Fig. 4.26: I_{ds}-V_{fg} characteristics of Ge JL transistor showing hysteresis effect associated with forward and reverse sweeps of gate voltage at (a) V_{bg} = -0.4 V, (b) V_{bg} = -0.8 V and (c) V_{bg} = -1.2 V. (d) Variation in hysteresis window (ΔW) for different V_{bg} values. All the results are shown for T_{Ge} = 11 nm.

An important attribute of *n*-type DG Ge JL transistor biased with negative V_{bg} is the tunability of hysteresis associated with forward and reverse sweeps of gate bias. It is observed that read operation [59-60] associated with the hysteresis window (ΔW) for dynamic memory applications can also be tuned to desired range through back bias. Previously, tunable hysteresis was

observed by Han *et al.*, for fin-array structure [60] in which ΔW could be tuned by altering the device parameters and load resistance connected to the fin-array. In DG JL devices, the independent gate operation can be further utilized to obtain tunable hysteresis without changing device parameters. The device structure used for analyzing the back bias dependent tunable hysteresis in DG JL device has a film thickness of 11 nm and spacer thickness of 20 nm. The reason for designing JL devices with relatively thicker film is to trigger FBEs at lower V_{ds} (~ 1.2 V). Moreover, the thicker spacer i.e. L_{sp} = 20 nm is sufficient to suppress the off-state tunneling for V_{bg} varied from -0.4 V to -1.4 V. Fig. 4.26*a-c* shows I_{ds}-V_{fg} characteristics for the two sweeps of V_{fg} with varying back gate bias. It is observed that varying V_{bg} from -0.4 V to -1.2 V can tune hysteresis window from 50 mV to 10 mV as shown in Fig. 4.26*d* without altering the device dimensions. The tuning ability of ΔW in an independent gate operation of DG JL device is governed by the extent of depletion due to the applied negative V_{bg}, which reduces the degree of II.

4.5 Conclusion

This chapter showcases the usefulness of composite and pragmatic parameter in terms of the product of current density and electric field i.e. (*J.E*) to optimize the performance of steep switching Ge JL transistors. Insightful analysis for limiting the off-state BTBT while sustaining steep switching in DG Ge JL transistors has been presented. As JL transistors are heavily doped, II at lower V_{ds} can be enhanced by selecting a thicker semiconductor film, to yield higher value of *J.E* which can be depleted at zero bias condition. It is shown that the appropriate optimization of film thickness and drain bias can lower BTBT dominant I_{off}. This can further be reduced to either by workfunction engineering or by incorporating an underlap of 5 nm while sustaining *S*-swing $\leq$ 5 mV/decade with nearly four orders of drain current transition at the threshold voltage.

Also, the analysis presented in this chapter reveals that RSD architecture is beneficial to enhance the degree of II over a wide area which results in *S*-

swing of 2 mV/decade at V_{ds} = 0.9 V. The limitation of RSD architecture in terms of BTBT can be overcome by the use of a thicker side oxide which can suppress the off-state BTBT and result in low $I_{OFF} \sim 10^{-9}$ A, along with an enhancement in II. Despite higher degree of II, RSD devices have shown higher C_{para} associated with RSD geometry. Analysis shows that C_{para} can be curtailed without severely degrading *S*-swing by limiting its increase to 50% of the original (non-RSD) geometry. In addition, the presence of vertical doping gradient in RSD profile can limit the carriers available for II and affects *S*-swing. The analysis suggests that the minimum dopant concentration in the channel to facilitate steep *S*-swing should be greater than 5×10^{18} cm^{-3}.

Due to higher value of *J.E*, Ge JL devices are more prone to latch effect and hinder the transistor switching action. Therefore, a systematic methodology to suppress single transistor latch effect, which is an extreme case of II in DG Ge JL transistors, has been presented in this chapter. A unique feature of the proposed technique is to suppress latching phenomena without altering the device architecture while preserving *S*-swing <10 mV/decade. Results highlight that negative (positive) bias at the back gate for *n*-type (*p*-type) JL MOSFET can considerably reduce: (1) *J.E* product, and (2) the area over which II occurs. Also, the drawback of applying negative back gate bias (for *n*-type JL device) in terms of BTBT can be overcome by the use of a thicker sidewall spacer which can suppress possible increase in off-current.

4.6 References

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Chapter 5

Conclusion and Scope for Future Work

5.1 Conclusion

This chapter presents the summary of work carried out on different aspects of floating body effects and their applicability in Silicon and Germanium junctionless transistor. The impressive feature of JL transistor is the occurrence of II induced dominant floating body effects which resulted in a sharp rise in drain current with a near ideal *S*-swing ~ 1 mV/decade at relatively lower applied voltages when compared with classical inversion mode MOSFET [1]. Although previously published works [1-5] on steep switching JL transistors are promising, the requirement of drain bias > 1 V for triggering impact ionization is not feasible for low power applications. Thus, different methodologies have been presented to optimize the basic junctionless architecture for triggering II at relatively lower drain bias. Moreover, the research work carried out in the thesis discusses physical effects prominent at nanoscale regime which affect the performance of Ge JL devices. A possible solution to overcome the degradation in steep switching Ge JL transistor has been addressed in the thesis work to make Ge based JL devices more suited candidature for logic applications.

The research work presented in the thesis provides insights into the operation of JL devices through comprehensive device simulations and addresses various problems associated with the switching action of JL transistor at lower gate lengths. The conclusion related with different aspects of junctionless MOSFETs drawn from different chapters is summarized as follows:

I. Steep Switching in Junctionless Transistors

It is demonstrated that double gate junctionless MOSFETs with the utilization of low-κ sidewall spacer and high-κ gate dielectric can achieve II triggered steep rise in drain current with *S*-swing ~ 1 mV/decade at relatively lower drain bias. As the sidewall spacers can modulate the metric *J.E*, parameters (thickness and dielectric constant) associated with sidewall spacer should be carefully selected for the intended temperature range of operation to avoid both extremes, i.e. the latching effect at lower temperatures or reduction in the degree of II at higher temperatures. Results have shown that wider spacer with low-κ and a narrow spacer with high-κ permittivity will be useful to limit the latching effect that can occur at lower temperatures (250 K). For high temperature operation (360 K), the decrease in the II rate can be compensated by designing a JL transistor with a thicker silicon film.

A comprehensive study in double gate Si and Ge JL transistor topology has shown that completely misaligning the back gate with respect to front gate towards the drain resulted in an inclined conduction channel, unique to misaligned topology, which results in an enhanced degree of II. The misaligned topology in JL architecture, considerably improves the product (*J.E*) than its contemporary perfectly aligned topology, and has the potential to achieve a sharp increase in drain current with higher number of decades of current transition at the threshold voltage.

II. Anomalous Behavior of sub-Boltzmann Switching Si and Ge Junctionless Transistor

Other features of II triggered bipolar effects in an essentially unipolar Si and Ge JL transistor have also been analyzed in the thesis. The work has demonstrated a systematic study of threshold voltage in steep switching JL transistors over the wide range of temperature (T = 250 K - 625 K). At low temperatures the dominant conduction mode is bipolar, whereas thermal generation at higher temperatures governs a more traditional unipolar

conduction mode in JL devices. The bipolar conduction mode results in a positive temperature coefficient of threshold voltage (i.e. threshold voltage increases with an increase in temperature) while unipolar conduction leads to the negative temperature coefficient of threshold voltage. The influence of strong bipolar mode conduction mode is also reflected in the absence of zero temperature coefficient condition from the transfer characteristics for positive values of dV_{th}/dT, whereas negative dV_{th}/dT values signify the existence of zero temperature coefficient condition.

Other unique attributes of II triggered bipolar effects in JL transistors are the presence of hysteresis and negative values of total gate associated with sub-60 mV/decade *S*-swing. It is shown that the symmetric gate operation of JL transistor does lead to an ideal switching with *S*-swing of 1 mV/decade, but with hysteresis in the transfer characteristics. The independent gate operation has been demonstrated to preserve negative values of total gate capacitance corresponding to lower value of *S*-swing ~15 mV/decade along with suppression of hysteresis. Additionally, the benefit of utilization of an independent gate operation in double gate JL MOSFETs has been reflected in the lowering of drain voltage required to trigger II induced sub-60 mV/decade *S*-swing.

III. Optimization of Germanium Junctionless Transistor for sub-*kT/q* Switching Action

Since tunneling induced degradation is significant in Ge based devices [6], a systematic approach has been followed to improve the performance of double gate Ge JL transistor through the optimization of the product *J.E*. Insightful analysis showcases that off-state tunneling current at lower gate voltages can be suppressed by incorporating an optimal underlap or workfunction engineering after carefully optimizing the film thickness and drain bias. The systematic design methodology has been presented in the work that preserves the effectiveness of II to achieve a sharp rise in drain current with *S*-swing < 5 mV/decade at lower applied drain bias.

At architecture level, an enhanced degree of II in Ge JL device to facilitate sharp current switching from off-to-on state at relatively lower V_{ds} can be achieved using raised source/drain topology. It is shown that raised source/drain architecture is beneficial to augment II over a wider area which results in *S*-swing of 2 mV/decade at V_{ds} = 0.9 V. The limitation of raised source/drain architecture in terms of BTBT can be overcome by the use of a thicker side oxide which can suppress off-state tunneling along with an enhancement in impact ionization. An insightful analysis suggests that the minimum dopant concentration in the channel to facilitate steep *S*-swing should be greater than 5×10^{18} cm^{-3}.

While II is beneficial to achieve a sharp rise in drain current from off-to-on state, the upper limit on II has been the single transistor latch in both *n*MOS and *p*MOS Ge JL devices. The latching phenomenon in inversion mode devices was reported because of increase in drain bias [7]. However in JL transistor, due to the heavily doped channel, latch effect is shown to be triggered with an increase in the drain voltage, channel doping, film thickness, and gate oxide thickness due to a considerable enhancement in the product *J.E*. The presence of single transistor latch effect is shown as a limitation, where the transistor cannot be turned-off even by reducing the gate voltage to negative values. Therefore, a systematic methodology of independent gate operation has been discussed to regain the steep switching action by overcoming latch effect while preserving the *S*-swing < 10 mV/decade in JL devices.

5.2 Scope for Future Work

The aggressive scaling in the transistor gate length down to sub-50 nm regime has resulted in innovative 3D device architectures such as FinFETs [8] and nanowires [9]. Thus, it will be interesting to understand and evaluate the constraints for facilitating impact ionization induced FBEs to achieve steep switching from off-to-on state. As impact generation mechanism is governed by the product *J.E*, the distribution of current density and electric

field (vertical and lateral electric field) will be different in 3D transistor architectures. Therefore, the constraints for selecting the device architecture and optimization of structural parameters are expected to be different from that proposed in this work. Hence, the future scope of the thesis work can be to perform a systematic study of the dependence of height, width and aspect ratio of the silicon fin or diameter of the nanowire on the impact generation process as it is expected to provide insights to achieve steep *S*-swing at voltages corresponding to the energy bandgap.

The analytical model, describing the physical phenomenon associated with the impact ionization, to capture the behavior of threshold voltage and total gate capacitance in steep switching JL transistor is another possible extension of the present work. Physical models predicting the behavior of electrical quantities such as threshold voltage and capacitance will be useful for circuit designers and semiconductor industry to analyze the performance of the device and associated circuit over the wider range of temperature.

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