TRANSISTOR ARCHITECTURE EVALUATION FOR STANDALONE AND EMBEDDED 1T-DRAM

Ph.D. Thesis

By

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DISCIPLINE OF ELECTRICAL ENGINEERING

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TRANSISTOR ARCHITECTURE EVALUATION FOR STANDALONE AND EMBEDDED 1T-DRAM

A THESIS

Submitted in partial fulfillment of the
requirements for the award of the degree
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MD. HASAN RAZA ANSARI

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"TRANSISTOR ARCHITECTURE EVALUATION FOR STANDALONE AND EMBEDDED 1T-DRAM"** in the partial fulfillment of the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY** and submitted in the **Discipline of Electrical Engineering, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from **July 2016** to **February 2019** under the supervision of **Dr. Abhinav Kranti**, Professor, Electrical Engineering Discipline, IIT Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Signature of the student with date
(MD. HASAN RAZA ANSARI)

This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

Signature of Thesis Supervisor with date
(Dr. ABHINAV KRANTI)

MD. HASAN RAZA ANSARI has successfully given his/her Ph.D. Oral Examination held on **July 08, 2019**.

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Signature of Convener, DPGC Date:

Signature of Head of Discipline
Date:

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Dedicated to my Grandfather

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ABSTRACT OF THE DISSERTATION

Transistor Architecture Evaluation for Standalone and Embedded 1T-DRAM

For the past few decades, scaling of the transistor for higher speed and dense memory with lower cost per bit has been successfully achieved by semiconductor memory industries. The increase in demand for innovative applications has further stimulated the development of novel memory technologies. The Dynamic Random Access Memory (DRAM), which is the main memory for desktop and larger computers due to its high density, low latency and low cost, is facing physical limitations and process complexity in the nanoscale regime.

The reduction in size of the capacitor in a conventional DRAM (1T-1C DRAM) adversely affects the charge retention, requires more refresh cycles, and consequently, dissipates more power. The problem can be circumvented with the use floating body of Silicon-on-Insulator (SOI) of the single transistor (1T) as DRAM cell. However, the scaling of conventional SOI Metal-Oxide-Semiconductor FETs (MOSFETs) suffers from Short Channel Effects (SCEs), Band-to-Band Tunneling (BTBT) along with the formation of ultrsharp *pn* junction in nanoscale regime. Although conventional SOI MOSFET based 1T-DRAMs have shown promising results, the issue of formation of ultrsharp *pn* junction and SCEs in nanoscale regime are quite challenging. Thus, the focus has shifted towards use of devices with a without junction and operatation at lower drain bias as compared to Inversion Mode (IM) transistors. Junctionless (JL) transistors overcome the issue of formation of ultrasharp junction and SCEs in nanoscale transistor compared to other *pn* junction based transistor. Thus, the thesis work focuses on different JL architectures for standalone and embedded capacitorless DRAM (1T-DRAM) with improvement in its metrics such as Retention Time (*RT*), Sense Margin (*SM*), Current Ratio (*CR*), speed, and scalability at low lower bias.

JL transistor has shown the possibility as 1T-DRAM. However, it achieves much lower *RT* (*RT* < 64 ms, a target specified by International Technology Roadmap for Semiconductors (ITRS)). Therefore, a careful reinvestigation is required for JL architecture as DRAM with its operation and requirement to enhance the performance metrics with modification of device architecture for standalone and embedded DRAM (eDRAM). The work in the thesis provides physical insights into the understanding of the performance and behavior of JL devices for memory applications through device simulations.

The key contribution of this research is the evaluation of device architecture for standalone and embedded DRAM applications. The DRAM metrics decide the application, therefore, the thesis work demonstrates device perspective, where various metrics of DRAM are regulated by device architecture (double gate, stacked, and shell-doped), geometry (gate lengths, film thickness), parameters (oxide thickness, gate workfunction), biases and temperature. These DRAM metrics are governed through hole generation and recombination in the storage region that defines distinct operations (Write, Hold and Read) of DRAM.

The doping dependent analysis showcasing the carrier lifetime and potential depth modulates DRAM metrics of conventional Junctionless architecture for standalone and embedded DRAM applications. The independent gate operation of JL transistor utilizes the front gate (Gate1) for conduction and back gate (Gate2) for charge storage. The depletion of electrons from the silicon film forms a profound potential well, and therefore, enhances the retention characteristics. The moderate doping (N_d) in the channel, longer underlap length (L_{un}) and higher gate workfunction (φ_m) shows the applicability for standalone memory with higher *RT* while higher doping can be utilized for eDRAM with high speed. Results highlight a high retention of ~2.5 s at 85 °C and ~4.5 s at 27 °C for a gate length (L_g) of 400 nm and N_d of 10^{17} cm^{-3} with scalability down to 25 nm (*RT* > 64 ms, target specified by ITRS). The variation in channel doping shows a reduced retention with increased doping, but higher doping can be used for high speed and low power consumption in an embedded memory. Insights into doping dependent characteristics for AM and JL devices along with storage volume analysis presents new viewpoints for efficient memory operation.

The Stacked junctionless (SJL) architecture consists of an *n*-type and *p*-type regions separated by an oxide. The functionality of architecture as DRAM is based on physically decoupling the conduction region (top *n*-type JL transistor) and storage region (bottom *p*-type JL), while maintaining an electrostatic coupling between them. The use an of oxide layer (SOX), separating the conduction and storage regions, reduces the hole recombination as the stored holes are away from heavily doped n^{++} Source and Drain regions, and also, reduced generation of holes, and thus, can enhance *RT*. SJL transistor enhances *RT* of 1T-DRAM, with a significant improvement (~×10^3) as compared to a conventional JL transistor with a doping (N_d) of 10^{19} cm^{-3} and L_g of 200 nm at 85 °C. SJL based 1T-DRAM achieves maximum *RT* of ~2.5 s for $N_d = 5\times10^{18}$ cm^{-3} and ~1 s for 10^{19} cm^{-3} with L_g of 200 nm at 85 °C. Results demonstrate its functionality down to 20 nm. The work showcases the possibilities of achieving higher retention time through an appropriate optimization of the architecture.

While SJL topology achieves a higher *RT* it requires more time to perform write operation due to the separation of storage region from the conduction. Shell-Doped (SD) topology is an optimal choice to overcome the trade-off between DRAM metrics. Shell-Doped topology with a thin heavily doped shell and a thicker (intrinsic) core achieves a deeper potential well, and thus, enhances the performance of 1T-DRAM. The advantage in terms of high *RT* in SD topology is due to enhanced depletion of electrons that facilitates a deeper potential well for charge storage and reduces the diffusion and recombination of generated holes. The work also investigates the dependence of shell thickness (T_{Shell}) and doping (N_{d}) on physical mechanisms associated with *RT* and Sense Margin (*SM*), current ratio and speed. Additionally, the impact of gate length scalability and high temperature on *RT* is shown. Results highlight the possibility of achieving enhanced *RT* in SD JL devices at lower gate lengths through appropriate selection of device parameters and optimization.

The work presented in the thesis showcases new viewpoints for JL devices to function as dynamic memory. The physical insights and analysis of different attributes with optimal utilization of each can lead to improved metrics as well as suppressed trade-offs. Further, the feasibility assessment of the proposed DRAM for standalone and embedded applications is presented through the evaluation of key performance metrics.

LIST OF PUBLICATIONS

A. Publications from PhD thesis work:

A1. In Refereed Journals:

1. **Md. Hasan Raza Ansari**, Nupur Navlakha, Jyi-Tsong Lin, and Abhinav Kranti, "1T-DRAM with Shell Doped Architecture," **IEEE Transactions on Electron Devices**, vol. 66, no. 1, pp. 428-435, Jan. 2019. (Journal Impact Factor: 2.62)

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3. **Md. Hasan Raza Ansari**, Nupur Navlakha, Jyi-Tsong Lin, and Abhinav Kranti, "Doping Dependent Assessment of Accumulation Mode and Junctionless FET for 1T DRAM," **IEEE Transactions on Electron Devices**, vol. 65, no. 3, pp. 1205-1210, Mar. 2018. (Journal Impact Factor: 2.62)

A2. In Refereed Conferences:

1. **Md. Hasan Raza Ansari**, Nupur Navlakha, Jyi-Tsong Lin, and Abhinav Kranti, "Architecture Evaluation for Standalone and Embedded 1T-DRAM" **In IEEE International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA-2019)**, Hsinchu**,** Taiwan, Apr. 2019.

2. **Md. Hasan Raza Ansari**, and Abhinav Kranti, "Retention Enhancement through Architecture Optimization in Junctionless Capacitorless DRAM" **In IEEE International Conference on Emerging Electronics (ICEE-2018)**, Banglore, India, Dec. 2018.

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4. **Md. Hasan Raza Ansari**, Nupur Navlakha, Jyi-Tsong Lin, and Abhinav Kranti, "Influence of Material Parameters on the Performance of Accumulation Mode DRAM" **In International Conference on Solid State Devices and Materials (SSDM-2018)**, pp. 149-150, Tokyo, Japan, Sep. 2018.

5. **Md. Hasan Raza Ansari**, Nupur Navlakha, Jyi-Tsong Lin, and Abhinav Kranti, "Emerging FETs for Low Power and High Speed Embedded Dynamic Random Access Memory**," In Proc. of 31st International Conference on VLSI Design and 17th International Conference on Embeded System (VLSID-2017)**, pp. 422–427, Pune, India, Jan. 2018.

6. **Md. Hasan Raza Ansari**, Nupur Navlakha, Jyi-Tsong Lin, and Abhinav Kranti, "Junctionless Capacitorless Dynamic Random Access Memory**," In Abs. 6th International Symposium on Integrated Functionalities (ISIF-2017)**, pp. 11, Delhi, India, Dec. 2017.

7. **Md. Hasan Raza Ansari**, Nupur Navlakha, Jyi-Tsong Lin, and Abhinav Kranti, "Investigation of Junctionless Transistor based DRAM," **In 19th International Workshop on the Physics of Semiconductor Device (IWPSD-2017)**, pp. 1-3, Delhi, India, Dec. 2017.

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ACRONYMS

1C	*Single Capacitor*
1T	*Single Transistor*
2D	*Two-Dimensional*
AM	*Accumulation Mode*
ADAS	*Advanced Driver-Assistance Systems*
A-RAM	*Advanced-RAM*
BL	*Bitline*
BOX	*Buried Oxide*
BTBT	*Band-to-Band Tunneling*
CB	*Conduction Band Energy*
CMOS	*Complementary Metal Oxide Semiconductor*
COLSA	CO_2 Laser Spike Annealing
CR	*Current Ratio*
DEPL	*Depletion*
DG	*Double Gate*
DIFF	*Diffusion*
DRAM	*Dynamic Random Access Memory*
eDRAM	*embedded-DRAM*
EEPROM	*Electrically Erasable Programmable Read Only Memory*
EHPs	*Electron-Hole Pairs*
EOT	*Effective Oxide Thickness*
EPROM	*Erasable Programmable Read Only Memory*
eV	*Electron Volt*
FB	*Forward Bias*
FBCs	*Floating Body Cells*
FBEs	*Floating Body Effects*
FB-FET	*Feedback Field Effect Transistor*
FDSOI	*Fully Depleted Silicon on Insulator*

FED	*Field Effect Diode*
FET	*Field Effect Transistor*
G1	*Gate 1*
G2	*Gate 2*
GAA	*Gate-All-Around*
GEN	*Generation*
GIDL	*Gate Induced Drain Leakage*
AI	*Artificial Intelligence*
IM	*Inversion Mode*
IMOS	*Impact Ionization MOS*
IoT	*Internet of Things*
ITRS	*International Technology Roadmap for Semiconductors*
JL	*Junctionless*
MLD	*Monolayer Doping*
MOS	*Metal-Oxide-Semiconductor*
MOSFET	*Metal-Oxide-Semiconductor Field Effect Transistor*
MOX	*Middle Oxide*
MSD	*Meta-Stable Dip*
MWA	Microwave Annealing
NVRAM	*Non-volatile Random Access*
NVRAM	*Non-Volatile Random Access Memory*
PC	*Personal Computer*
PDSOI	*Partially Depleted Silicon on Insulator*
QCEs	Quantum Confinement Effects
REC	*Recombination*
RR_{RT}	*Reduction Ration in RT*
RT	*Retention Time*
SCEs	*Short Channel Effects*
SD	*Shell-Doped*
SILVACO	*Device Simulation Software*
SISOI	*Silicon-with-partially- Insulating-layer-on-SOI*

SJL	*Stacked Junctionless*
SM	*Sense Margin*
SOI	*Silicon on Insulator*
SOX	*Separation Oxide*
SRAM	*Static Random Access Memory*
SRH	*Shockley Read Hall*
TCCT	*Thin Capacitive Coupled Thyristor*
TFET	*Tunnel Field Effect Transistor*
TRAM	*Thin Capacitively-Coupled Thyristor based DRAM*
VB	*Valence Band Energy*
WL	*Wordline*
WT	*Write Time*
Z^2-FET	*Zero sub-threshold swing and Zero impact ionization FET*

NOMENCLATURE

ΔI_{ds}	Shift in current levels
ΔV	Potential depth
C_B	Bitline capacitance
C_s	Storage capacitance
E	Magnitude of the electric field
H0	Hold ‘0’
H1	Hold ‘1’
I	Current
I_d	Drain current
I_0	Read currents for state ‘0’
I_1	Read current for state ‘1’
I_{off}	Off-current
I_{on}/I_{off}	On-to-off current ratio, Switching speed
κ	Gate dielectric
L_g	Gate length
L_{g1}	Front gate length
L_{g2}	Back gate length
L_{gap}	Lateral spacing between the gates
L_{in}	Front ungated region
L_s	Storage region
L_{un}	Underlap between drain and gate
N_a	*p*-type doping concentration
N_d	*n*-type doping concentration
$N_{d(S/D)}$	*n*-type source and drain doping concentration
n_e	Electron concertation
n_h	Hole concentration
R0	Read ‘0’
R1	Read ‘1’

S/D	Source/Drain
T	Temperature
T_{box}	Buried oxide thickness
T_{Core}	Core thickness
τ_d	Doping dependent carrier lifetime
T_{ox}	Oxide thickness
T_{Shell}	Shell thickness
T_{si}	Silicon film thickness
T_{Si1}	Conduction region thickness
T_{Si2}	Storage region thickness
T_{SOX}	Separation oxide thickness
V	Voltage
V_D	Drain voltage
V_G	Gate voltage
V_{G1}	Front gate voltage
V_{G2}	Back gate voltage
V_{Th}	Threshold voltage of MOSFET
W0	Write ‘0’
W1	Write ‘1’
W_{Si}	Gate width
ε	Dielectric permittivity
τ_0	Electron and hole lifetime at 300 K
φ_{m1}	Front gate workfunction
φ_{m2}	Back gate workfunction

Chapter 1

Introduction

1.1 Memory

Over the last few decades, the usage and demand of semiconductor memories has increased tremendously, and there has been no looking back [1]–[10]. The applications requiring high speed and high density semiconductor memories have resulted in the development of various memory technologies [1]–[10]. The solid-state memory is categorised in terms of volatility such as volatile (Static Random Access Memory (SRAM) and Dynamic RAM (DRAM)) and non-volatile (Non-volatile Random Access Memory (NVRAM), NOR flash, Erasable Programmable Read Only Memory (EPROM), Electrically Erasable Programmable Read Only Memory (EEPROM), and NAND flash) [8]–[10]. A volatile memory is not able to retain the information when power is off, while a non-volatile memory retains data even after the power is off. Their utility in real-time applications is based on various parameters, a few of them are illustrated in Table 1.1.

Table 1.1 Comparison of different types of memories [1], [7], [8].

Memory	***Volatility***	***Density***	***Write Speed***	***Read Speed***	***Cost/bit***
Flash	No	High	Slow	Fast	Moderate
EPROM	No	High	Slow	Fast	Moderate
EEPROM	No	Moderate	Slow	Fast	Expensive
SRAM	Yes	Low	Fast	Very Fast	Expensive
DRAM	Yes	Very High	Moderate	Moderate	Moderate

1.2 Motivation of DRAM

The concept of DRAM was proposed in 1966 by Robert Dennard in which the information is stored in the form of charge in the capacitor along with a transistor to access the stored data [6]. The first patent was filed in 1967 on the single-transistor (1T) and capacitor (1C) based DRAM (1T-1C) [11], which was issued in

1968 [11]. The discovery of DRAM by Dennard has remarkably improved the performance of computers and led to development of Personal Computers (PC) [12], [13]. After this in 70's, the DRAM was commercialized by Intel with 1 kilobyte of storage with utilization of 3 transistors and a capacitor (3T-1C) [12]. However, in late 70's, 1T-1C based DRAM was commercially introduced, and till now, there have been various modifications in the design to improve the functionality of 1T-1C topology [14].

DRAM is a volatile, smaller in size, fast and robust memory with high density working at low power and cost [15]–[21], which is used for data management [22]–[26], but needs further innovations to compete with cheap and low power NAND memory [27]. In the last fifty years, volatile memories (SRAM and DRAM) have seen remarkable growth [6]. Both have been developed, improved, and used in large quantities. However, in terms of volume, DRAMs have remained on top as a main memory in large systems, apart from other widespread applications [6], due to higher density and low cost per bit of information stored. Conventional Dynamic Random Access Memory (1T-1C DRAM) cells are composed of a Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) (pass transistor (1T)) and a capacitor (charge storage (1C)) as shown in Fig. 1.1 [14]. The operation of conventional DRAM (Fig. 1.1) is based on charging and discharging of the storage capacitor (C_S) [12], [28], [29]. Write operation is performed when a sufficient voltage is applied to wordline (WL), which turns on the transistor thereby sending current to the storage capacitor (C_S). The fully charged capacitor indicates the state '1' while discharged capacitor shows the state '0' of the memory. During read operation, the transistor is again accessed and based on the data stored in the storage capacitor, the charge is distributed among storage capacitance (C_S) and bitline (BL) capacitance (C_B). The architecture requires a rewrite (refresh) after every read operation as the charge sharing destroys the information contained in the DRAM cell. Typically, this recharge happens every few milliseconds to compensate for the charge leakage from the capacitor [30].

The DRAM is smaller in size, fast and dynamic in nature (when computer is running) with the storage capacitor being constantly refreshed, typically every 64

milliseconds [30]. The application of memory cell is shown in Fig. 1.2. DRAM has been used as main memory for workstations, PCs, and recently in working memory of mobile phones and digital electrical home appliances [31].

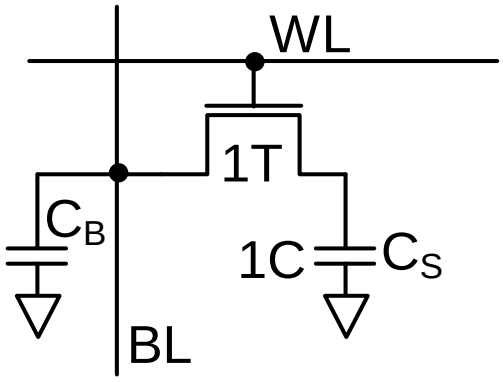

Fig. 1.1. Schematic diagram of conventional DRAM (1T-1C DRAM) [12].

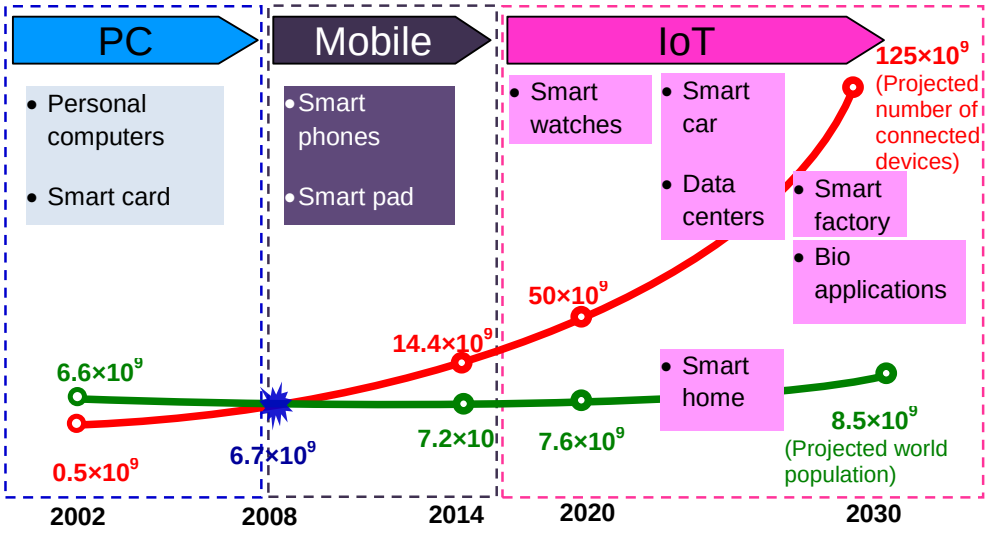

Fig. 1.2. Projected explosive growth of connected device in the 4th industrial revolution [31].

The 4th industrial revolution is expected to be defined by new technologies which are combining the conventional physical and cyber systems [31]. In such a projected scenario, the demand for memory is expected to be much greater than the previously used. The number of projected connected devices in cyber physical systems are expected to witness an exponential growth, which are projected to reach 125 billion in 2030 (Fig. 1.2) [32]. This is expected to achieved through smart adaptable applications requiring the development of advanced semiconductor memories at an unprecedented scale [31]–[35].

The ever increasing demand of memories in portable electronic gadgets [22] require continuous improvisation and downscaling. Moreover, the digital information and internet applications generate immense amount of data, which is stored in a cloud [22]–[24]. Hence, the focus of the memory development is shifting from computational to data intensive applications that further demands innovation [25], [26], [36], [37]. Another technology requirement is the shifting paradigm towards embedded applications, where the memory system is incorporated with logic devices on an integrated circuit [27], [38], [39]. Thus, the key contributors necessitating the need for innovative technology includes, Internet of Things (IoT), mobility, networking, cloud computing and big data application [5], [22]–[26], [40]–[43] that drives the need for ease of system integration, lower power consumption, enhanced storage in smaller volume, faster storage and retrieval, and real time analytics [39], [44]. The technology metrics of the memory are stability, reliability, data retention, on–off ratio, power and endurance [8]. The major barrier is trade-offs between these metrics, and hence, optimization is crucial to design application specific memory. The alternative memory architecture should reduce the process complexity and cell cost, and enhance scalability with enhanced functionality.

1.3 Capacitorless DRAM (1T-DRAM)

Conventional 1T-1C DRAM cell [16], [45], [46] has been investigated for several decades. The major issue associated with DRAM cell is the non-scalability of capacitor, which can be leaky, and thus, requires to be refreshed periodically [18], [30]. The problem can be resolved by using vertical array transistor and 3D cell storage capacitor [38], [47]–[49]. However, the fabrication of 3D cell storage capacitor is quite challenging. Utilizing the floating body of Silicon-on-Insulator (SOI) devices allows the single transistor (1T) to store charges and also overcome the non-scalability of the external capacitor in a conventional DRAM cell. The concept of capacitorless-DRAM (1T-DRAM) has been proposed more than 20 years ago [50] and evolved into architectures such as Partially-Depleted (PD) SOI MOSFET [51]–[65], Fully Depleted (FD) SOI [66]–[76], Meta-Stable Dip (MSD) [77]–[86], Advanced-RAM (A-RAM) [87]–[89], A2RAM [90]–[94], Thin Capacitively-Coupled Thyristor (TCCT) [95]–[100], Field Effect Diode (FED)

[101]–[106], Zero-Slope and Zero-Impact Ionization FET (Z^2-FET) [107]–[115], Tunnel Field Effect Transistor (TFET) [116]–[126], Impact Ionization (IMOS) [127], [128] and Junctionless (JL) [129], [130], as shown in Fig. 1.3 [51]-[130]. 1T-DRAM utilizes an undesirable phenomenon (floating-body effect of SOI transistor [131], [132]) to serve as storing capacitance for DRAM cell and distinguishes the states '1' and '0'. Also, 1T-DRAM offers several potential advantages with respect to conventional 1T-1C DRAM [13], [18], such as

(i) High density due to elimination of the external capacitor,
(ii) Non-destructive read,
(iii) Low cost of fabrication, since it is implemented on a standard SOI logic process without exotic process steps [133],
(iv) Excellent delay–power trade-off due to the use of SOI technology, and
(v) Possibility of taking advantage of multigate architectures, as demonstrated in [77], [134], [135].

While capacitorless DRAM has a simple architecture and easy fabrication, it needs to be explored and optimized for standalone memory and embedded applications. The requirements of Retention Time (*RT*) are different for standalone and embedded DRAMs (eDRAM) [136], [137]. *RT* of the memory is defined as the time until which states can be distinguished [136], [137]. One of the issues associated with conventional IT-1C DRAMs as embedded memory due to the many processes that are required for fabricating the charge storage capacitors, which are not needed for logic devices [136], [137]. Floating body cells (FBCs) are dense, reliable, low power and high speed DRAM cells, being a competitive candidate as embedded DRAM [138]. eDRAMs are being developed to replace static RAM to achieve cheaper and lower voltage embedded chips [45], [46].

In PD-SOI MOSFET shown in Fig. 1.4(a), at relatively higher drain voltages, Impact Ionization (II) phenomenon generates Electron-Holes Pairs (EHPs) in the semiconductor film. Holes start to accumulate at the back surface and source end (due to lower potential region) and electrons flow towards the drain end.

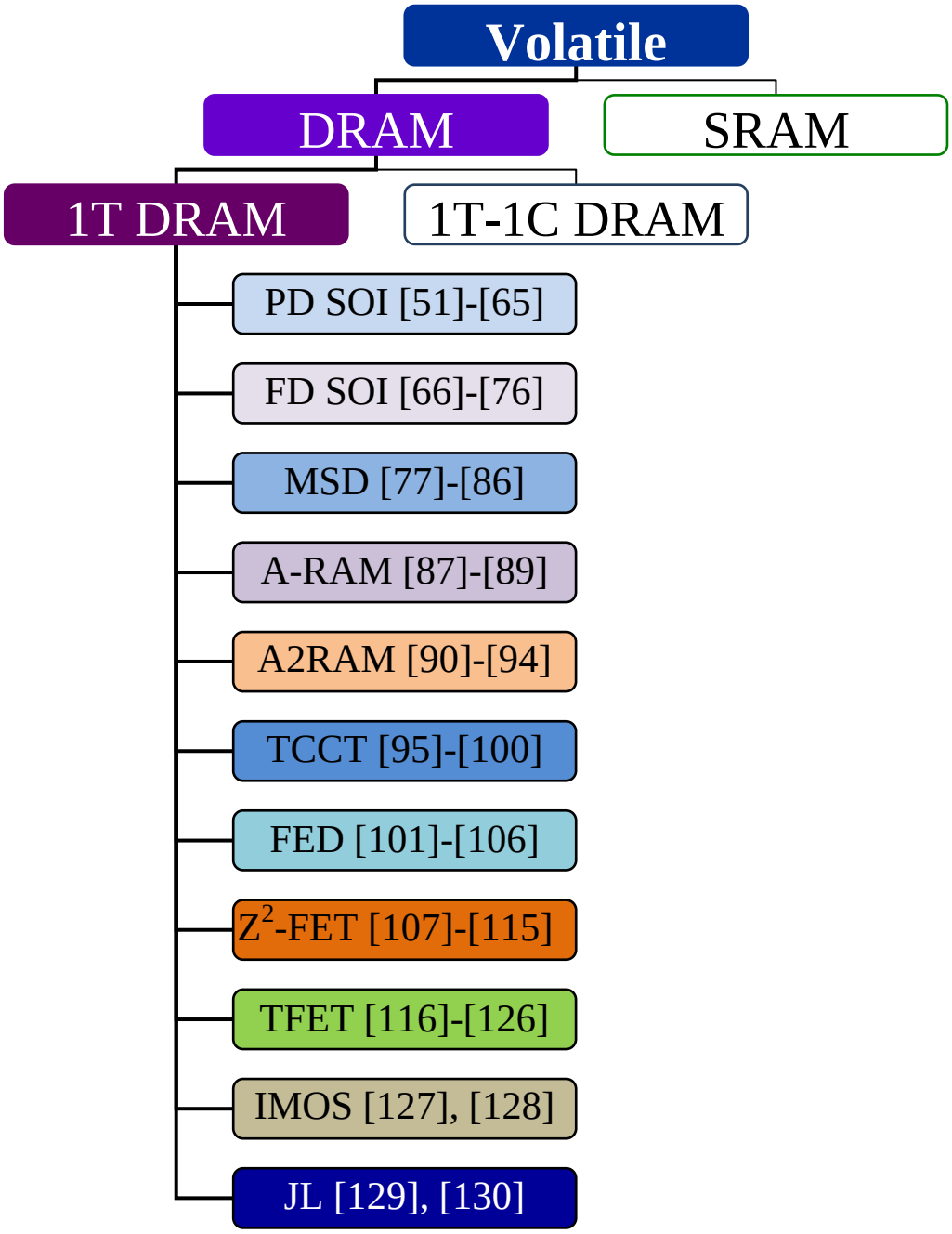

Fig. 1.3. Schematic illustration of the various 1T-DRAM architectures.

The undesirable kink effect in PD SOI devices introduces a sharp increase in the drain current due to presence of holes at the back surface of the silicon film as shown in Fig. 1.4(b). This indicates a change in the threshold voltage of the transistor. Thus, the operation shows the memory states, where more number of holes are stored in the body is defined as the state '1' (higher potential), while the state with fewer holes stored is defined as state '0' (lower potential). The

threshold voltage of the device as 1T-DRAM cell is lower for state '1' than that of the state '0' due to the body effect in SOI MOSFET.

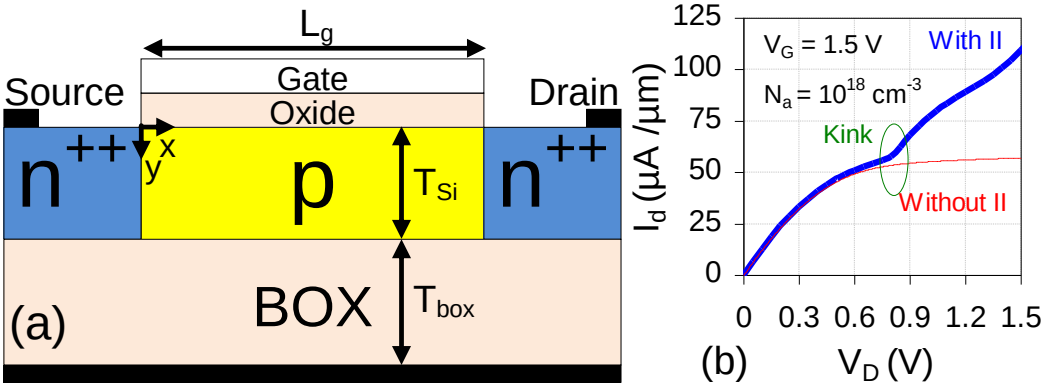

Fig. 1.4. (a) Schematic diagram of PD-SOI [58]. (b) Comparison of output characteristic (I_d-V_D) of PD-SOI with and without Impact Ionization (II).

1.4 1T-DRAM operation

1.4.1 Write operation

The capacitorless DRAM operation is based on storing the holes for state '1' and evacuating the holes for state '0'. There are different methods to generate holes during Write '1' operation for state '1' while Write '0' operation is performed with the forward bias mechanism.

1.4.1.1 Write '1' operation

1) **Impact Ionization** [55], [60], [74], [75], [134], [139]–[142]: The operation is based on the avalanche breakdown, where a high electric field at the channel-drain region creates EHPs on collision with electrons [143]. The generated electrons drift towards positively biased drain while holes are stored at lower potential region. Write '1' operation based on impact ionization is demonstrated in Fig. 1.5. In this method, a sufficient gate voltage is required to invert the channel and accumulate the electrons. If a high enough drain voltage is also applied then electrons can accelerate towards the drain, and generate the electron-hole pairs. This mechanism is fast and consumes less time to perform write '1' operation. However, the main concern is reliability due to the applied high drain bias [144].

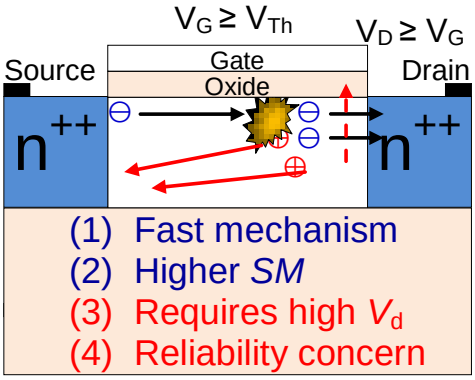

Fig. 1.5 Schematic representation of Write '1' operation through impact ionization [139]-[142]. The electrons accelerated towards drain strike the bonded electrons to generate EHPs. Dashed arrow indicates reliability concern. ⊖ and ⊕ indicates electron and hole, respectively. V_D, V_G, and V_{Th} indicate the drain, gate and threshold voltage, respectively.

2) **Bipolar Action** [145]–[147]**:** In this mechanism, the generation of electro-hole pair is based on the impact ionization along with a feedback loop that generates more electron-hole pairs as shown in Fig. 1.6(a).

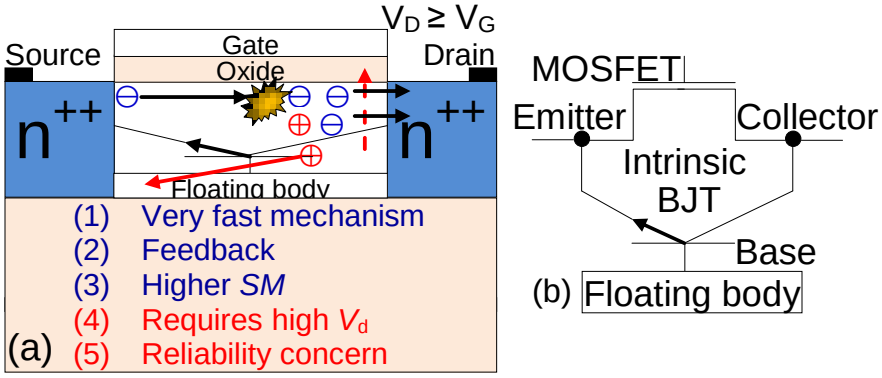

Fig. 1.6 Schematic representation of (a) Write '1' operation through bipolar action, and (b) bipolar action in SOI MOSFET due to impact ionization [145]–[147]**.** Dashed arrow indicates reliability concern.

In this method, the collector refers to the drain, the emitter to the source and the base to the body. The accumulated holes at the back surface makes a forward biases the source and channel junction, which reduces the source-channel barrier, allows more number of electrons to drift towards drain, and further triggers the impact ionization. The parasitic bipolar transistor in the

SOI MOSFET is used for second generation (Gen-2) based 1T-DRAM application to speed up the write operation [76]. Impact ionization enhanced by parasitic bipolar transistor is a very fast write mechanism. However, the use of high drain bias and reliability can be a concern [144].

3) **Band-to-Band Tunneling (BTBT)** [119]–[121]**:** Tunneling in the device is achieved through a negative bias at the gate and a positive bias at drain which operates the transistor in the reverse bias mode [12] as shown in Fig. 1.7(a). The negative bias at the gate with a positive bias at drain creates a high electric field region and reduces the tunneling width between gate and drain junction [148], and hence, allows the electrons to tunnel from valence band (VB) of the channel to conduction band (CB) of the drain, thereby, accumulating holes into the potential well [121].

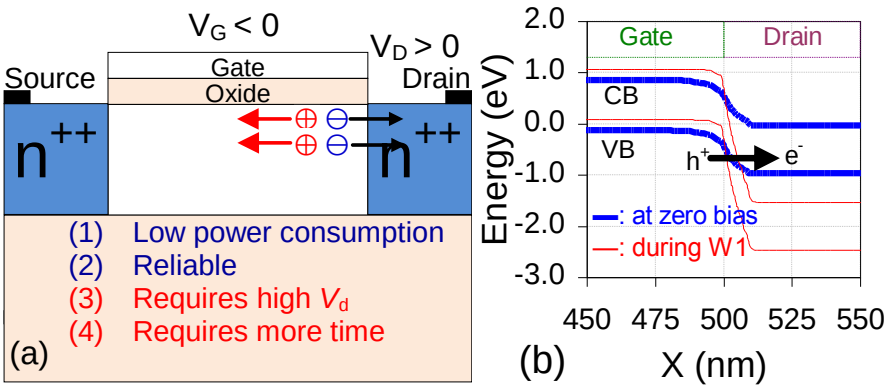

Fig. 1.7 (a) Schematic representation of Write '1' operation through BTBT mechanism [119]-[121]. (b) Energy band at zero bias (V_S = V_D = V_G = 0 V) and during Write '1' operation (V_D > 0 and V_G <0). CB and VB indicate the conduction and valence band, respectively.

Fig. 1.7(b) shows the energy band diagram of SOI transistor at zero bias condition (V_S = V_D = V_G = 0 V) and during Write '1' operation (V_{D_W1} > 0 V and V_{G_W1} < 0 V). The energy band diagram is extracted at 1 nm above of the back gate oxide. BTBT occurs by applying a negative bias at back gate and positive at drain, which reduces the tunneling width at gate and drain junction to enable electrons to tunnel from valence band of the channel to conduction band of the drain. This tunneling is usually categorized as Gate Induced Drain

Leakage (GIDL) [65]. Although this write mechanism requires high drain bias, the write current is smaller as compared to previous methods (write through impact ionization and bipolar action), and thus, BTBT is a power efficient mechanism with minimized reliability concerns [12]. Due to the low power consumption mechanism being reliable, BTBT has been used as the programming mechanism throughout the rest of this thesis. In this technique, a potential well is always formed during Write '1' operation that helps to store the charges for state '1' for longer duration, and thus, enhances the retention characteristics.

1.4.1.2 Write '0' operation

During Write '1' operation, cell reaches from state '0' to state '1' with excess holes, which can be generated through different mechanism as discussed in 1.4.1.1. To bring the cell back to state '0', excess holes need to be removed, which is called "erasing of the cell" i.e. Write '0'. The same is performed with the simplest and most effective way through the Forward Bias (FB) mechanism (Fig. 1.8(a-b)) [12]. In this mechanism, a positive bias is applied to gate and source/drain is biased with negative voltage, which constitutes two forward biased *pn* junctions in the transistor such that holes can be evacuated from the storage region. The forward biased body and source/drain junction results in the recombination (REC) of holes at the heavily doped n^{++} region, and thus, holes are removed from the storage region, and the memory shows the state '0' with a reduction in drain current [12].

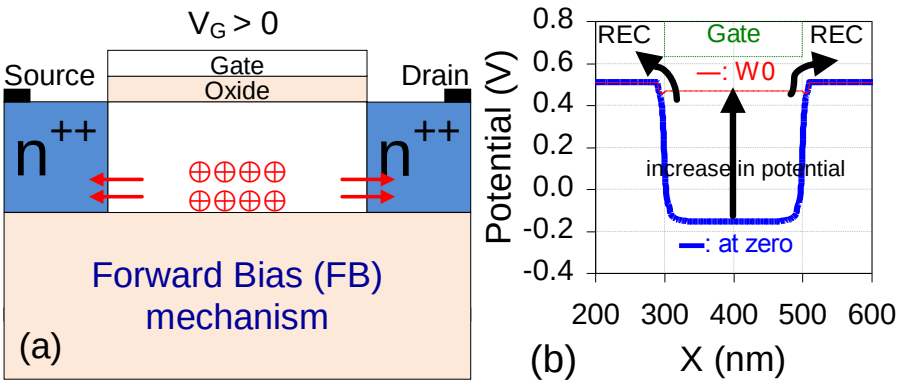

Fig. 1.8 (a) Schematic representation of Write '0' operation through Forward Bias (FB) mechanism [12]. (b) Potential at zero bias (V_S = V_D = V_G = 0 V) and during Write '0' operation (V_G > 0). REC indicates recombination.

1.4.2 Read operation

Read operation is performed to sense the presence and absence of holes in the memory by applying a drain voltage and measuring the current. Excess holes stored (removed) in the body of transistor reduces (increases) the threshold voltage for state '1' (state '0') and the same is shown in Fig. 1.9. This change in threshold voltage depends on the amount of holes stored in the floating body. The bias at drain during read has to be low enough not to trigger impact ionization as it will disturb the state '0'. It is evident from figure 1.9 that more (less) number holes present in the silicon film allows (restricts) more number of electrons to diffuse to the channel and drift to the drain and result into higher (lower) read current (Fig. 1.9(a)-(d)). The difference between state '1' and '0' current is defined as Sense Margin (*SM*) [75], [116]–[118].

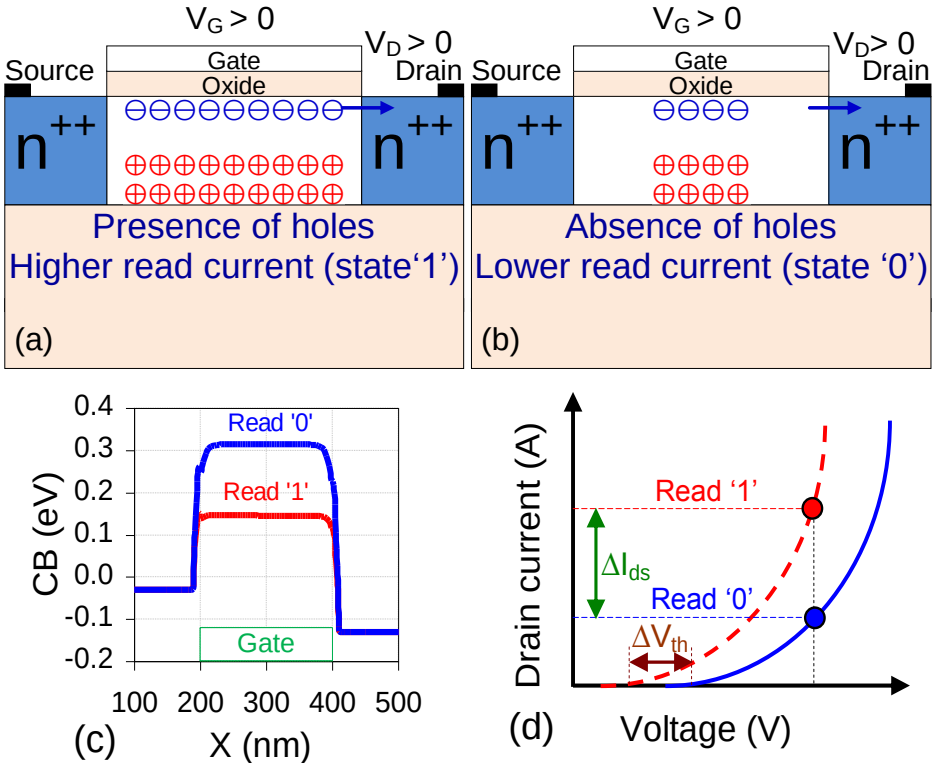

Fig. 1.9. Schematic diagram of a SOI device [51] illustrating the read mechanism, the presence of excess holes in the neutral body region leads to higher current for (a) state '1' as compared to (b) state '0', and the variation is observable in drain current – gate voltage characteristics through. (c) Conduction Band (CB) energy during Read '1' and '0'. (d) shift in threshold voltage (ΔV_{th}) and difference in the current levels (ΔI_{ds}) [12].

Read operation of a 1T-DRAM cell is different from the conventional 1T-1C DRAM. In the conventional 1T-1C DRAM, the charge is stored in the capacitor for state '1'. To read the cell, the transistor is turned on by applying a positive gate voltage. If the capacitor is charged, then it transfers part of its charge to the bitline capacitance [12], [28], [29]. The transferred charge increases the bitline voltage slightly which is read by the sense amplifier. Thus, after one successful reading, the cell (which was in state '1') loses a part of its charge. The read operation destroys the state of the cell. For proper operation, the cell needs to be written again according to the data read from the cell. This writing operation consumes extra energy which increases the overall power dissipation for the DRAM cell.

In 1T-DRAM, read current depends on (i) the hole concentration stored in the previous operation, (ii) the bias applied in previous and performed current operation, and (iii) device architecture and parameters. Thus, the cell need not to be programmed each time it is read. Also, the cell can be read multiple times once it is programmed. This multiple-read capability saves power for the 1T-DRAM cell.

1.4.3 Hold operation

Hold operation is performed between write and read operations that determines the retention of states [75], [116], [122]. The charge retention is regulated through hole generation and recombination that is controlled through device architecture, geometry, bias and temperature [75], [116], [122]. State '0' is perturbed through thermal generation and BTBT of electrons towards drain/source that generates holes in the potential well during Hold '0' operation [75], [116], [122]. State '1' is disturbed due to the decrement in hole concentration in the storage region due to thermal recombination and hole diffusion during Hold '1' operation [75], [116], [122]. Thus, to attain high retention time, which is one of the key metrics defining DRAM performance, the regulation of process governing hole recombination and generation is essential.

1.4.4 1T-DRAM operation through hole distribution

The working operation of a capacitorless DRAM is explained through hole

distribution in the storage region. Fig. 1.10 shows the variation of hole concentration (n_h) in the storage region, which shows the state '1' (presence of holes) and state '0' (absence of holes) along with the contours for each operation. At time, t = 0 ns, 1T-DRAM is at zero bias condition ($V_S = V_D = V_{G1} = V_{G2}$ = 0 V). In this condition, due to a higher back gate workfunction, the storage region will be in accumulation condition with the hole concentration of ~1.5×10^{18} cm^{-3}. The Write '1' is performed with write time of 100 ns through BTBT mechanism [75], [119], [122] by applying a negative back gate bias (V_{G2_W1} = -1.5 V and V_{D_W1} = 1.5 V), which increases the hole concentration in the storage region (around 10^{20} cm^{-3}). The applied bias triggers BTBT due to an increase in the electric field, which reduces the tunneling width (Fig. 1.7(b)). The reduction in tunneling width allows the electrons to tunnel from semiconductor region under the gate to drain, which generates holes for state '1'. The additional holes in storage region lowers the threshold of the device and results in a higher read current.

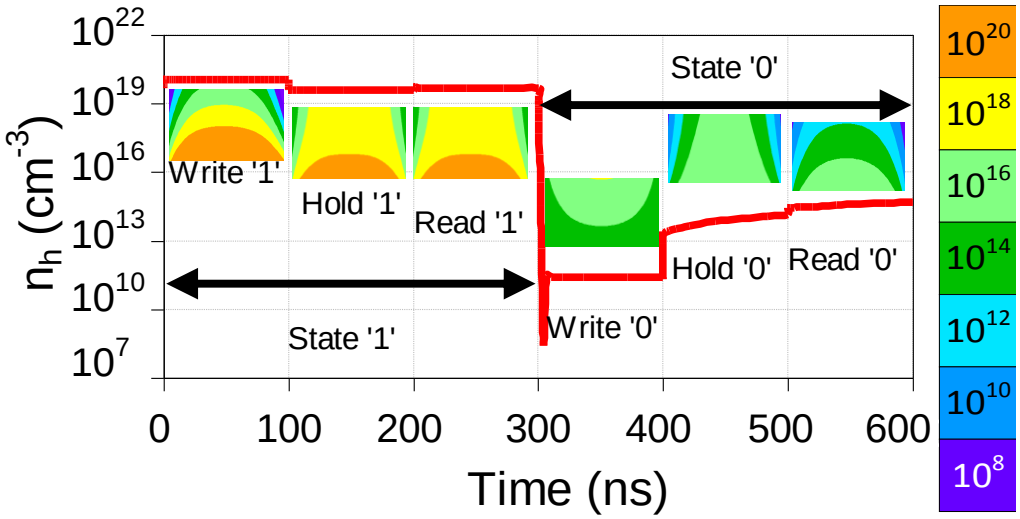

Fig. 1.10. Variation in hole concentration (n_h) with time in storage region for a typical sequence of memory operation for state '1' (Write '1', Hold '1' and Read '1') and state '0' (Write '0', Hold '0' and Read '0'). Contour plots are taken at the end time of operations.

At t = 100 ns, in Fig. 1.10, Write '1' bias is removed, and Hold (H) bias is applied (V_{G2_H} = -0.2 V). The hole concentration reduces by an order due to recombination of holes with virtual n-region, and the remaining charge is accumulated in storage region. After the hold operation, Read (R) bias (V_{D_R} = 0.1

V and V_{G1_R} = 0.9 V) with 100 ns is applied in which hole concentration is maintained, which results in a high read current for state '1'. After this, state '0' is stored through Write '0' (W0) operation. The removal of holes is performed with a forward bias mechanism by applying a positive bias at the back gate of (V_{G2_W0} = 1.0). At t = 400 ns, hold bias is applied. The hole concentration in the storage region increases due to thermal generation and BTBT in the device. The removal of holes from storage region lowers the read current for state '0' due to an increase in barrier for electrons (Fig. 1.9(c)). The difference between state '1' and '0' current is defined as Sense Margin (*SM*) [75]. Retention Time (*RT*) is estimated as the time when *SM* of memory reaches to 50% of its maximum value [75]. It is primarily governed through generation and recombination of holes during hold operation in storage region.

SOI MOSFETs have proven to be a promising architectures for 1T dynamic memory [51]-[130], achieving retention time that satisfies the 64 ms specification for standalone DRAM [136] with acceptable read sensitivity. However, the rapidly evolving semiconductor industry demands innovative methodologies to enhance performance with improvement in speed, power and density [18]. Thus, the focus has shifted towards different SOI devices for various applications to facilitate a high speed operation, while maintaining the need for low power and high density.

The proposed SOI devices (Fig. 1.3) for capacitorless DRAM have its own advantages and limitations. These are outlined in the next section.

1.5 SOI devices as 1T-DRAM

1.5.1 Partially Depleted (PD) 1T-DRAM

In SOI transistor, if the semiconductor film has an undepleted body (neutral region $n_h = N_a$) at zero bias due to use of thicker film and higher doping, the transistor is termed as PD SOI MOSFET (Fig 1.11(a)) [51]-[65]. Fig. 1.11(b) shows the variation of hole concentration along the film thickness (T_{Si}) of 100 nm and channel doping (N_a) of 10^{18} cm^{-3} at zero bias condition. Cutline is taken along the *y*-direction. It is evident from the figure that hole concentration is depleted

upto a certain limit of T_{Si}, after that it is undepleted i.e. $n_h = N_a$. In 2010, Okhonin et al. [51] utilized the PD SOI as a capacitorless DRAM with smaller feature size compared to conventional 1T 1C DRAM cell.

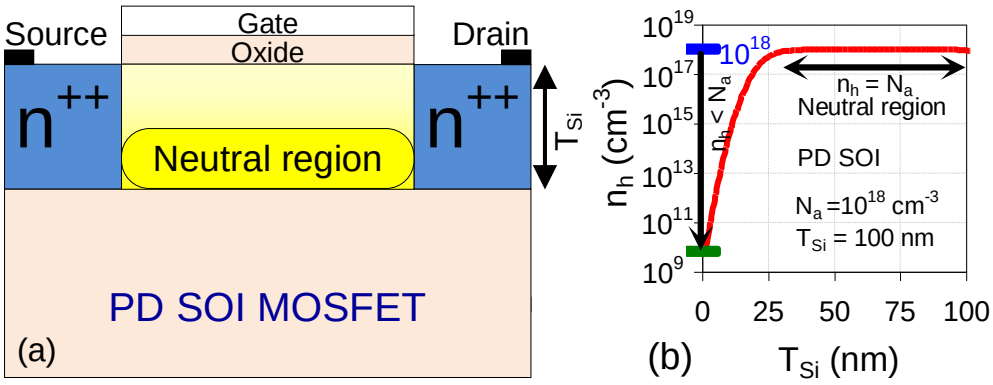

Fig. 1.11. (a) Schematic diagram of Partially Depleted (PD) SOI MOSFET [51]-[65]. (b) Variation of hole concentration along the film thickness with channel doping (N_a) of 10^{18} cm^{-3} and film thickness (T_{Si}) of 100 nm at zero bias condition.

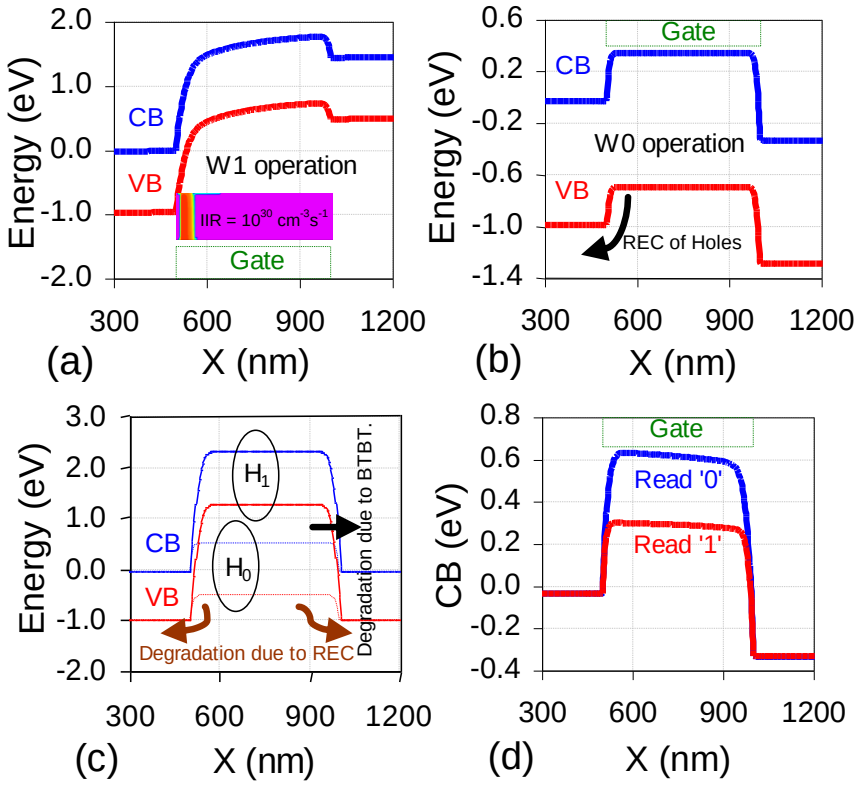

Fig. 1.12. Schematic representation of energy band diagrams of PD SOI based 1T-DRAM during (a) Write '1' operation, (b) Write '0' operation and (c) Hold '1' (H1) and Hold '0' (H0) operation, and (d) conduction band energy during Read operation.

Fig. 1.12 shows the operation of partially depleted SOI MOSFET as1T-DRAM through energy band diagram. The device dimension and biasing parameters are obtained from [51]. The generation of holes (Write '1') is performed with Impact Ionization and BTBT phenomenon as shown in Fig. 1.12(a). By applying negative bias at the gate and drain increases the electric field at the source end, which allows the electrons to collide with crystal atom, generate the electron-hole pairs and store the holes at the drain end. The Write '0' operation is performed with forward bias mechanism, which allows the stored holes to recombine with source electrons as shown in Fig. 1.12(b). In order to sustain the hole in the storage region, the same bias is applied during hold '1' and '0' [51]. Fig. 1.12(c) indicates that state '1' can be degraded due to BTBT during hold '1' operation and state '0' due to recombination holes during hold '0'. Read operation is performed through drift-diffusion mechanism. State '1' shows the lower barrier compared to state '0', and thus, results into higher read current. The major issue with PD SOI based DRAM is the scalability while maintaining the retention of 64 ms at 85 °C.

1.5.2 Fully Depleted (FD) 1T-DRAM

In SOI transistor, if the semiconductor film is fully depleted at zero bias due to use of thinner film thickness and moderate doping or undoped in the channel then transistor is termed as FD SOI MOSFET (Fig. 1.13(a)) [66]-[76]. Fig. 1.13(b) shows the variation of hole concentration along the film thickness with T_{Si} of 20 nm and N_a of 10^{18} cm^{-3} at zero bias condition. Cutline is taken along *y*-direction. It is evident from figure that hole concentration is less than the doping of the channel through the film.

The operation of a FD SOI MOSFET as 1T-DRAM is illustrated using as double gate MOSFET with the two gate contacts connected to the word lines and the source and drain electrodes connected to the bit lines. The front gate is utilized for the conduction, whereas back gate is used for storage of holes and modulates the DRAM metrics [76]. The Write '1' (Fig. 1.13(c)) operation is performed through BJT effect with same bias is applied to two gates and the source electrode, which is negative with respect to the drain bias. The applied bias creates the high electric field region at the drain side and generates the electron-hole pairs through BTBT and Impact Ionization phenomenon. Excess electrons are pushed toward the drain

due to the favourable field, whereas excess holes are pushed toward the source and may trap in the bulk if appropriate bias is applied to the electrodes. Further, electrons are injected from source–gate barrier and are collected by the relatively high potential at the drain contact in a manner reminiscent of typical bipolar junction transistors (BJTs) (Fig. 1.13(c)).

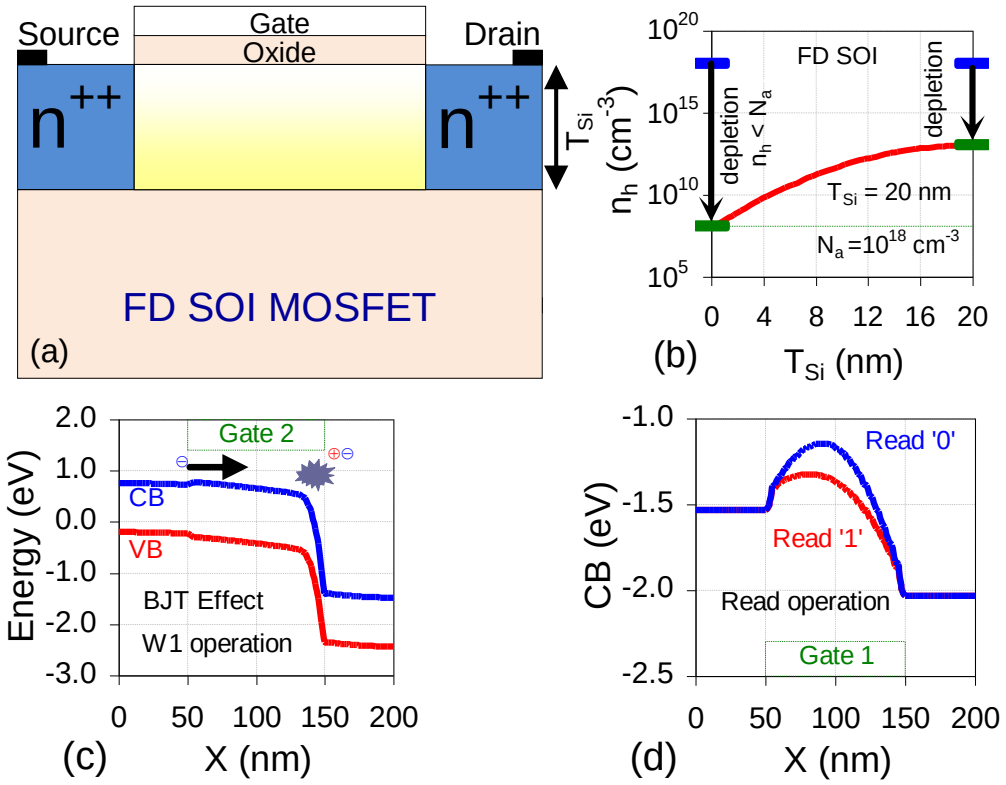

Fig. 1.13. (a) Schematic diagram of Fully Depleted (FD) SOI MOSFET [66]-[76]. (b) Variation of hole concentration along the film thickness with channel doping (N_a) of 10^{18} cm^{-3} and film thickness (T_{Si}) of 20 nm at zero bias condition. (c) Energy band diagram of a double gate FD SOI as 1T-DRAM during Write '1' operation. (d) Conduction band energy during Read operation.

Write '0' operation is performed through the forward bias mechanism with negative bias at the source and drain electrode and positive at the gate electrode. The applied bias allows the stored holes to recombine with source and drain electrons. The majority (minority) of holes at the back surface increases (reduces) the potential locally, and if the two gates are close to each other, the potential at the top interface is increased (reduced) (Fig. 1.13(d)). The higher (lower) potential at the top interface reduces (increases) energy barrier, and more electrons are

injected, which in turn increases (reduce) the drain current. FD SOI based DRAMs resolve the downscaling issue of PD SOI based DRAM [66]-[76]. Thus, all topologies for capacitorless i.e. standalone as well as embedded DRAM are based on FD SOI.

1.5.3 Meta-Stable Dip (MSD) 1T-DRAM

Meta-Stable DRAM (MSDRAM) (Fig. 1.14(a)) [77]–[86] operation is based on the Meta-Stable Dip (MSD) effect or hysteresis in drain current (Fig.1.14(b)). The MSDRAM memory cell uses the double gate action in FD SOI MOSFETs, namely the dynamic coupling between front and back interfaces, which gives rise to a hysteresis in transfer characteristic as shown in Fig.1.14(b). MSDRAM structures prevent the supercoupling effect with use of thicker film thickness. State '1' is defined by the presence of charges stored in the silicon body and programming is performed through charge generation by BTBT. Reading the cell is achieved by using a back gate voltage to activate the back channel ($V_{GB} \geq V_{TH}$) for state '1', current flows through this inversion layer. The very wide hysteresis ($-4 < V_{GF} < -2$, in Fig.1.14(b)) is used as a memory window. The operation of MSDRAM is same as FD SOI MOSFET. The only difference is write '1' operation is performed with BTBT and write '0' operation is performed with capacitive coupling.

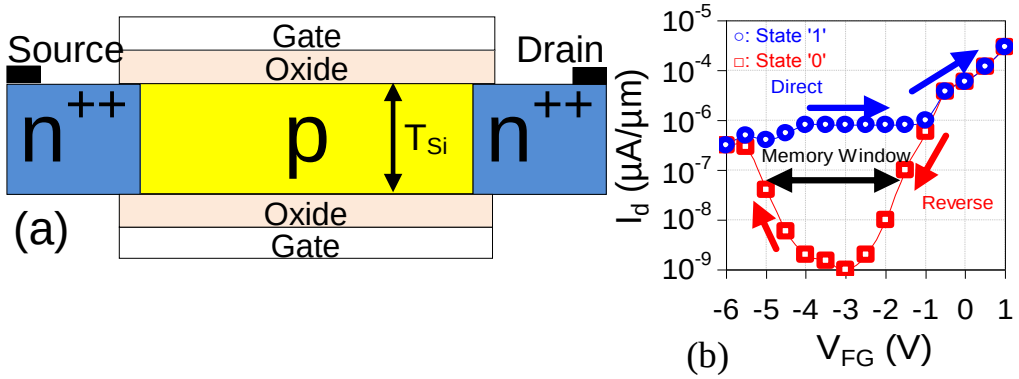

Fig.1.14. (a) Schematic diagram of Meta-Stable Dip (MSD) as 1T-DRAM [77]–[86]. (b) A typical MSD hysteresis [77]–[86] of FD DG MSDRAM cell with direct (circle) and reverse (square) scan of the top-gate voltage (V_{FG}).

The advantages of the MSDRAM memory cell are wide memory window, high sense margin, high Current Ratio (*CR*), and low power consumption. However,

the issue with MSDRAM is that state '0' is unstable, and thereby, degrades during a continuous reading. Although MSDRAM shows a better opportunity to achieve high current ratio, but it does not achieve a sufficient read current and retention time as compared to other device architecture [80]. Also, MSDRAM requires relatively higher voltages to perform DRAM operations. Another issue with MSDRAM is Short Channel Effects (SCEs), which enhance the injection of holes through BTBT. This injection is much faster than the thermal generation, which leads to a decrease in the retention time for shorter devices.

1.5.4 Advanced-RAM (ARAM)

The Advanced-RAM (ARAM) [87]–[89] is a FD SOI transistor in which conduction (*n*-type doped silicon film) and storage (*p*-type doped silicon film) region are physically isolated through a Middle Oxide (MOX) but the source and drain regions are shared (Fig. 1.15(a)).

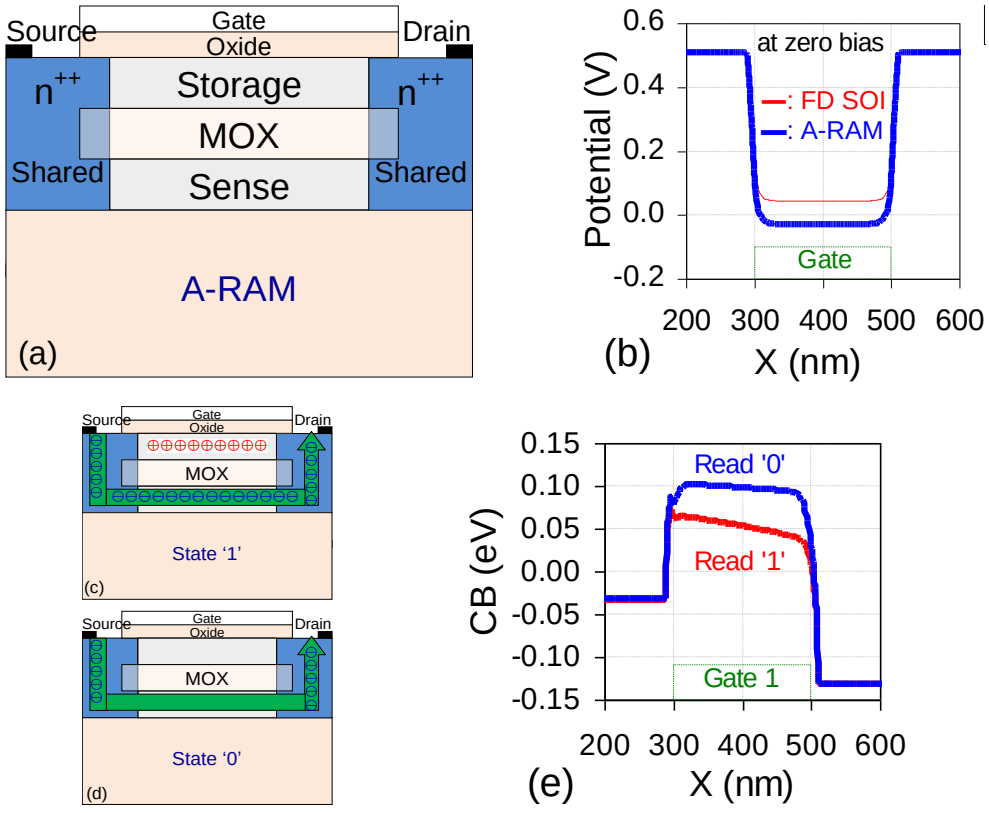

Fig. 1.15. (a) Schematic representation of A-RAM architecture for capacitorless DRAM [87]–[89]. (b) Potential profile at zero bias condition for FD SOI and A-RAM cell. (c) State '1': charged semi-body. (d) State '0': discharged semi-body. (e) Conduction band energy of A-RAM during Read '1' and '0' operation.

In A-RAM topology, the top semiconductor is utilized for charge storage while back semiconductor is used for conduction and serves to sense the memory states through an electron current. The key advantage of the A-RAM cell as a DRAM is utilizing a MOX, which reduces the coupling effect, and electron and hole concentrations can be brought very close to each other without triggering their recombination which would have occurred in an ultrathin single body. However, sharing of storage region with heavily doped n^{++} source and drain enhances the recombination during Hold '1' and generation of holes through BTBT during Hold '0', which degrades the retention of the memory. The advantage of A-RAM cell is shown in Fig. 1.15(b) with deeper potential well for A-RAM cell at zero bias condition compared to FD SOI MOSFET.

State '1' is defined when the top semi-body is charged with holes as shown in Fig. 1.15(c). The state '1' is programmed with high positive pulses on both the gate and the drain. Impact ionization phenomenon generates more number of holes in the top semi-body. The holes are maintained in the upper semi-body when the gate returns to a negative value, used for holding and reading state '1'. State '0' is defined as the absence of hole when the gate voltage is high and the drain voltage is zero, hence no positive charge can be generated in the upper semi-body. When A-RAM cell is in state '0' (Fig. 1.15(d)), the top semi-body is discharged. The A-RAM cell state is read by slightly increasing the drain voltage, typically to V_D = 0.1 V. Fig. 1.15(e) shows the conduction band energy of A-RAM cell during Read '1' and '0' operation. The state '0' current is low compared to state '1' current.

1.5.5 A2RAM

The fabrication of MOX issue with A-RAM [87]–[89] is resolved through A2RAM [90]–[94] structure by physically separating the conduction and storage regions. A2RAM architecture was proposed in 2011 as a new device with potential application as 1T-DRAM. The novelty of the device is the juxtaposition of two silicon films with different doping polarities i.e, a vertical *pn* junction, which defines a body partitioning for hole storage and current sense (Fig. 1.16(a)). The charge accumulated in the top body controls the current flowing through the bottom body. However, the issue with this architecture is that it requires precise doping and sharing of storage region with heavily doped n^{++} source and drain,

which enhances the recombination during Hold ‘1’, and generation of holes through Band-to-Band Tunneling during Hold ‘0’, which degrades the retention of the memory. In this topology, the holes are stored in the top *p*-type semiconductor while electrons flow through bottom *n*-type semiconductor. The majority of holes stored in the *p*-type semiconductor allows more number of electrons to flow from source to drain, which shows the state ‘1’ of the memory (Fig. 1.16(b)). When the top body is discharged of holes (state ‘0’), the gate field is no longer screened, therefore, *n*-type semiconductor becomes FD. The lack of majority carriers in the *n*-type semiconductor causes a very low current (State ‘0’) in Fig. 1.16(c). The same is also reflected in Fig. 1.16(d) through conduction band of A2RAM cell during Read ‘1’ and ‘0’ operation.

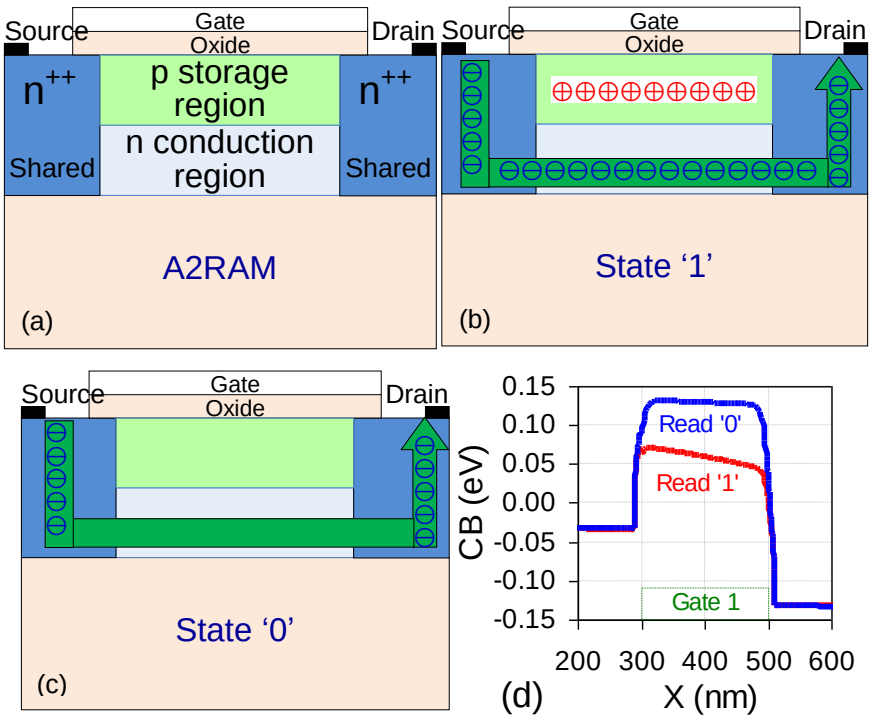

Fig. 1.16. (a) Schematic representation of A2RAM architecture for capacitorless DRAM [90]–[94]. (b) State ‘1’: charged top body. (c) State ‘0’: discharged top body. (d) Conduction band energy of A2RAM during Read ‘1’ and ‘0’ operation.

1.5.6 Thin Capacitively-Coupled Thyristor (TCCT) 1T-DRAM

Thin Capacitively-Coupled Thyristor based DRAM (TRAM) [95]–[100] cell structure is simply a SOI *p*-*n*-*p*-*n* thyristor with regular MOS gate over the *p*-base (Fig. 1.17(a))), which exploits the bistable nature of the thyristor characteristics to

store data. Fig. 1.17(b) shows the energy band diagram of TCCT FD SOI device at zero bias condition. The device utilizes the *p*-type doped region in the channel for charge storage.

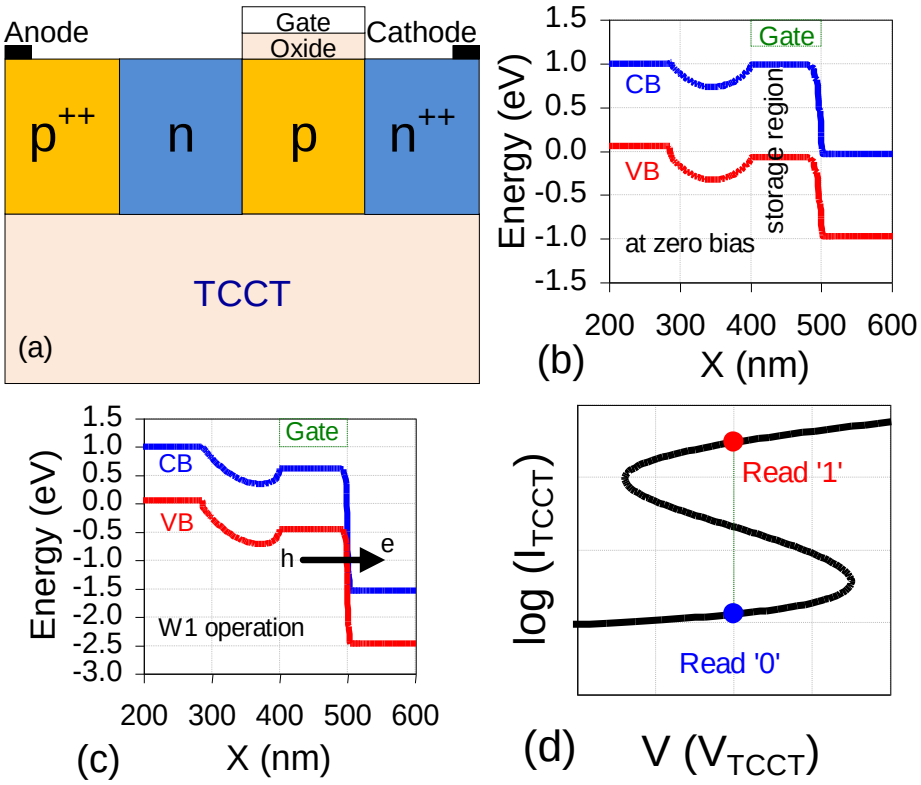

Fig. 1.17. (a) Schematic representation of TCCT architecture for capacitorless DRAM [95]-[100] (b) Energy band diagram of TCCT device as capacitorless DRAM at zero bias direction and gate region is utilized to store the charges. (c) Schematic illustration of energy band diagram of TCCT device during Write '1' operation by applying positive bias at the drain and negative bias at the gate. (d) Typical *I-V* characteristic of TCCT based transistor.

The generation of holes (Write '1') in the device is performed with BTBT mechanism by applying a positive bias at the drain and negative bias at the gate. By applying these biases, the tunnelling width reduces (Fig. 1.17(c)), which allows the electrons to tunnel from gate region to the drain region and generates the holes for state '1'. State '0' operation is performed either with forward bias mechanism or capacitive coupling mechanism. TCCT operation is based on Feedback Field Effect Transistor (FB-FET) that exhibits a snapback in the current voltage (*I-V*) characteristic (Fig. 1.17(d)). The anode current characteristics goes

through a negative resistance region, and finally, snap back to distinguish between the states of memory. TRAM shows the advantages in terms of high speed (~1 ns) and *CR* (~10^9), which is beneficial for eDRAM. However, the TRAM requires precise control of doping profiles of the *pn* junctions to achieve optimized breakdown characteristics.

1.5.7 Field Effect Diode (FED) 1T-DRAM

Field Effect Diode (FED) [101]–[106] is similar to TCCT cell, which shows unique advantages over TCCT and does not require precise doping. Fig. 1.18(a) shows the FED architecture, which is similar to a lateral *p*-*i*-*n* SOI diode without gate (Fig. 1.18(a)). The *n*-type and *p*-type semiconductor region underneath the gate is induced through utilization of different metal gate workfunction of *n*-poly (Gate 1) and *p*-poly (Gate 2), respectively (Fig. 1.18(b)), which form the barrier for holes underneath the high metal gate workfunction (*p*-poly) and serve as a storage region as shown in Fig. 1.18(c).

In order to operate the device as a memory cell, it must be possible to write '1' and read '1', write '0' and read '0', and hold '1' and '0' with a sufficient sense margin, speed, and retention time. Write '1' operation is performed by inducing holes and electrons into the channel. As the memory cell switches back to the hold state (hold '1'), holes and electrons are collected in a potential well. The bias and time are crucial during hold operation. Fig. 1.18(d) shows the conduction band energy during Write '1' and Hold '1' with different hold time. During hold '1' operation, the device is trying to reach at the equilibrium condition, and thus, reduce the holes from the storage region due to recombination with electrons. The removal of stored holes from the device is performed during write '0'. Write '0' operation is performed with positive bias at the Gate 2 by discharging the stored holes from the device. Fig. 1.18(e) shows the conduction band energy during Write '0' and Hold '0' with different hold voltage. Higher negative bias is beneficial for state '1', which can sustain the holes for longer duration and shows longer retention time. However, at the same time, state '0' will degrade with higher negative bias due to BTBT mechanism. Fig. 1.18(f) shows the variation of state current (I_1 and I_0) with hold time to estimate the retention time. Retention Time (*RT*) is estimated as the time when *SM* of memory reaches to 50% of its

maximum value [75]. The utilization of two metal workfunction implies it requires two front gates over the intrinsic region, and thus, the downscaling of gate is challenging for this architecture.

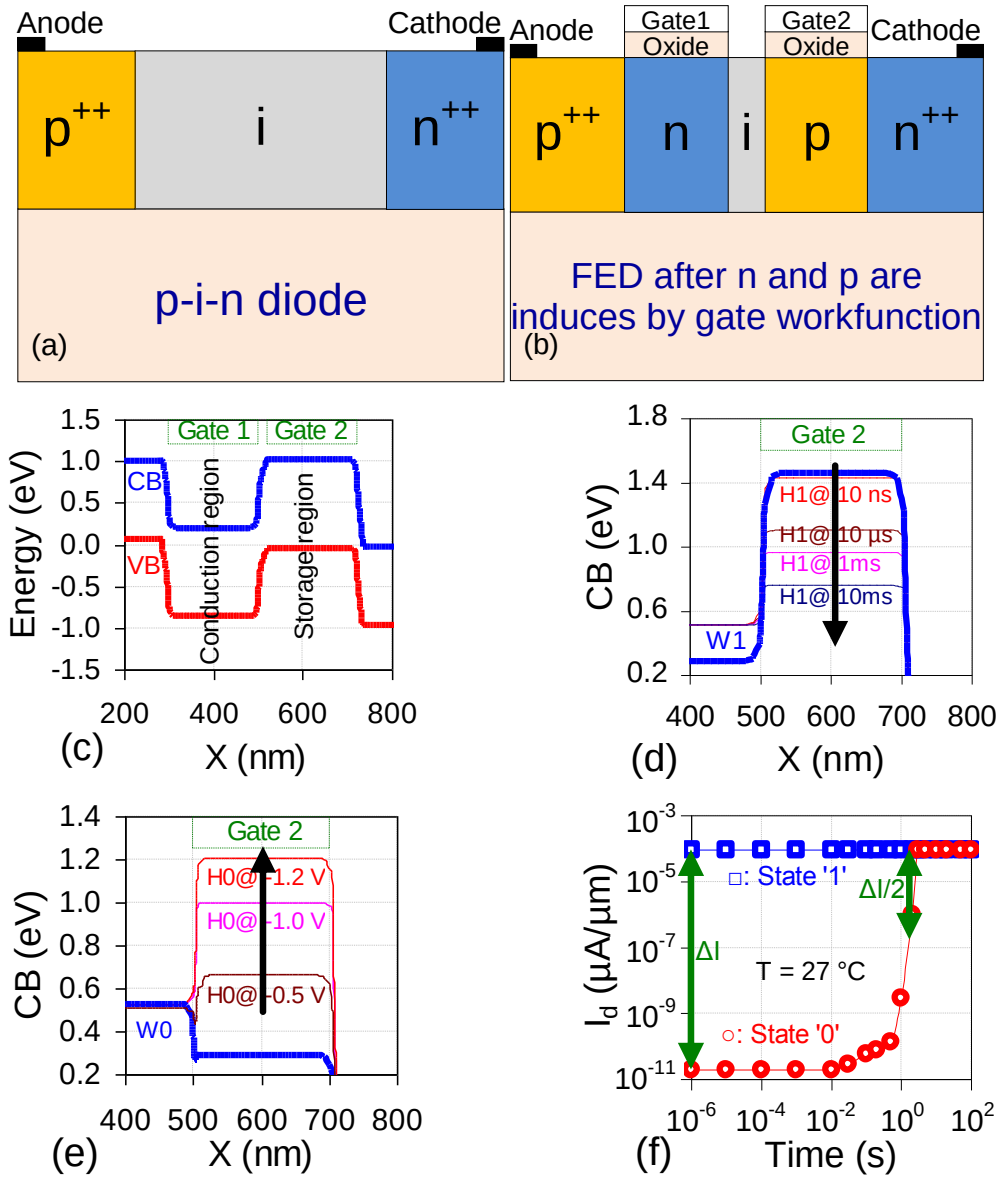

Fig. 1.18. Schematic representation of (a) *p-i-n* diode without gate and (b) FED for capacitorless DRAM [101]–[106] after *n* and *p* are induced underneath the gate by utilizing different metal gate workfunctions of *n*-poly (Gate 1) and *p*-poly (Gate 2), respectively. (c) Variation in energy band diagram for FED device as 1T-DRAM at zero bias condition. Conduction band during (d) Write '1' and Hold '1' for different hold time and (e) Write '0' and Hold '0' for different gate1 and gate 2 hold voltage. (f) Variation of states current (I_1 and I_0) with hold time to estimate retention time.

1.5.8 Zero-Slope and Zero-Impact Ionization FET (Z^2-FET) 1T-DRAM

While floating body based architectures are promising candidates for capacitorless DRAM, the retention time of the memory degrades due to the occurrence of Impact Ionization and/or BTBT in the device. A recently proposed zero impact ionization and zero subthreshold swing device named Z^2-FET [107]–[115] is shown in Fig. 1.19(a). Z^2-FET structure is formed by *p-i-n* structure on SOI substrate, with partial front gate (Gate), and holes are stored for the memory operation in the ungated region (L_{in}). Fig. 1.19(b) shows the variation of electron and hole concentration in the device at zero bias condition. The cutline is taken at 1 nm below of the front gate oxide.

The generation and recombination of holes in the device is controlled through the front and back gate by modulating the barrier for electrons and holes. The holes accumulated under the gate are depleted as drain voltage increases close to front gate voltage, reducing the electron injection barrier. This enables the injection of electrons from the n^+ drain into the channel, which flow to the p^+ source and induces a potential drop at source–channel junction, thereby reducing the injection barrier for holes and initiating positive feedback. The advantage of this architecture is for low voltage operation and longer charge retention. However, the Z^2-FET memory operation is limited due to the scaling of L_{in} (ungated region). In comparison to A2RAM and MSDRAM, Z²-FET requires a longer device length.

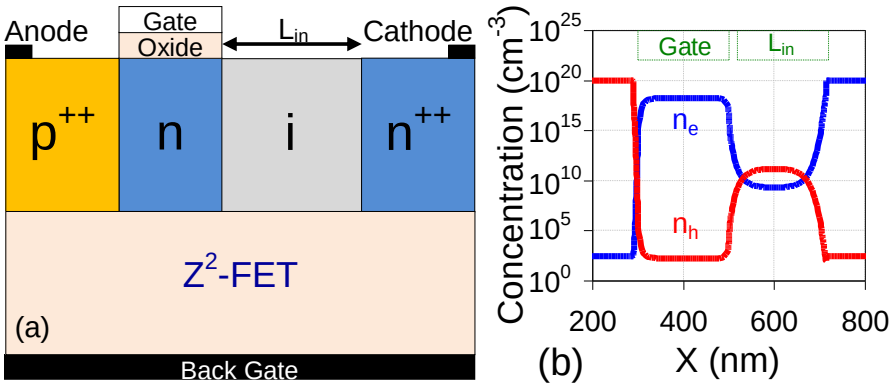

Fig. 1.19. (a) Schematics representation of Zero-Slope and Zero-Impact Ionization FET (Z^2-FET) for capacitorless DRAM [107]-[115]. (b) Variation in electron (n_e) and hole (n_h) concentration in Z^2-FET at zero bias condition.

1.5.9 Tunnel Field Effect Transistor (TFET) 1T-DRAMs

Single gate Tunnel Field Effect Transistor (TFET) [116]–[126] is unable to store the charges due to *p-i-n* architecture. The first concept for TFET based DRAM utilized an oversized back gate where the storage region is located at front ungated portion of the semiconductor film. The result showed a lower *SM* of 10–20 nA with a *RT* of a few milliseconds at room temperature. The *SM* was improved to 500 nA with the use of a *p*-doped pocket as the storage region. Further, Navlakha et al. [120] reported a planar tri-gate TFET (Fig. 1.20(a)), in which dual gates near the source increase the tunneling current, and also reduce SCEs, which enhance *SM*, and improve scalability, thereby overcoming the critical bottleneck faced by TFET based dynamic memories.

The storage of excess holes defines Write '1', which is based on the generation of holes in the region under Gate 2. Fig. 1.20(b) shows the lower potential region induced through p^+ polysilicon Gate 2 with a hole concentration of ~10^{18} cm^{-3} at zero bias condition [119]. The potential is further lowered (Fig. 1.20(c)) due to a negative gate bias that results in the tunneling of electrons towards the drain as shown in Fig. 1.20(c), thereby accumulating holes ~10^{20} cm^{-3}. The Write mechanism with BTBT is a power efficient methodology and reliable compared to that based on impact ionization [75]. Write '0' presented as discharging of the capacitor and is based on the recombination of holes with drain electrons that removes the holes from the potential well. The holes are evacuated through a positive gate bias that raises the potential at the storage region (Fig. 1.20(d)). This forward biases Gate 2 and drain region, and thus, holes recombine at the drain. The presence and absence of excess charge carriers, contributed by generation and recombination of holes, respectively, distinguish the two states, and are quantified by the read currents as represented in Fig. 1.20(e) through conduction band energy during read operation. A higher effective potential at Gate 2 results into lower barrier for electrons at Gate 2 region (Fig. 1.20(e)) and thus, distinguishes the two currents (I_1 and I_0). Fig. 1.20(f) shows the transient analysis of TFET based 1T-DRAM. The difference between the read currents for state '1' and '0' is Sense Margin (*SM*) and the time required to reduce the maximum *SM* by 50% is estimated as Retention Time (*RT*). TFET based DRAM shows the better performance as compared to *p-i-n* based SOI based DRAM. However, the

limitation related to downscaling of the tri-gate and speed is the main concern due to use of dual gates and gap between two gates.

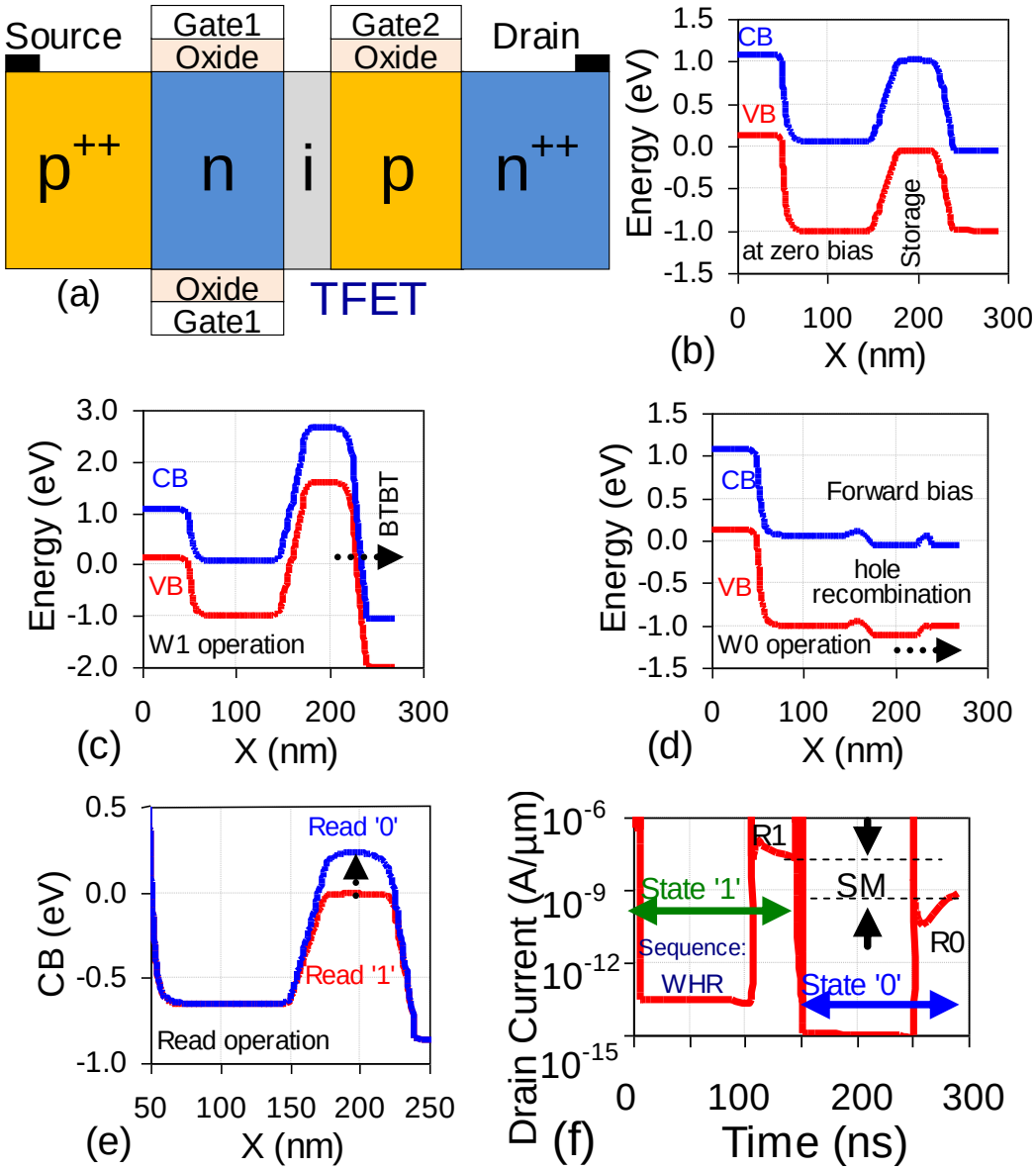

Fig. 1.20. Schematic representation of Tunnel Field Effect Transistor (TFET) for capacitorless DRAM [116]–[126]. Variation in energy band diagram of TFET as 1T-DRAM at (b) zero bias condition, (c) W1 operation and (d) W0 along the *x*-direction at 1 nm below the front oxide. (e) Conduction band energy for Read operation, showing an increased barrier for electrons for Read '0' compared to '1'. (f) Transient currents in the sequence of operation (Write: W, Hold: H, Read: R). CB and VB indicate the conduction and valance band energy, respectively.

1.5.10 Junctionless (JL) Transistor 1T-DRAM

A Junctionless (JL) architecture [129], [130] (Fig. 1.21) with same type of dopant throughout the semiconductor overcomes the issue related (formation of ultrasharp *pn* junction and SCEs) to Inversion Mode transistor in nanoscale regime [149], [150]. Unlike the conventional SOI MOSFET, JL transistors have heavy doping throughout the source to drain, and function as a normally on device. In order to turn-off the device, a high (low) gate workfunction for *n*-type (*p*-type), and thinner film to deplete the carriers and to form the barrier for source electron (hole) is required [149], [150]. The transistor architectures facilitating floating body effects at relatively lower drain biases compared to IM device, which can be a good option for capacitorless DRAM.

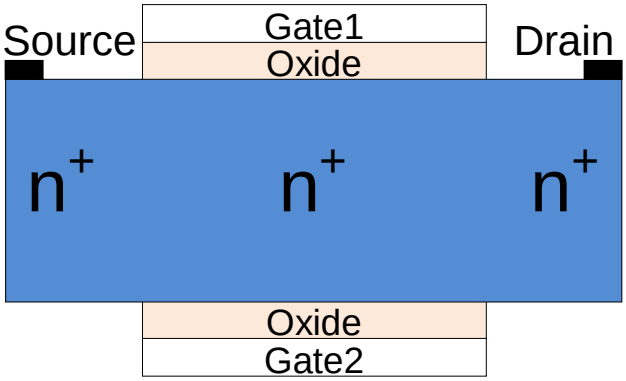

Fig. 1.21. Schematic representation of a Junctionless (JL) transistor [129], [130] for capacitorless DRAM.

Previous studies on JL has focused on performance evaluation, design optimization and scaling [149], [151]–[154], steep switching [155]–[159], fabrication [160], [161], analog/RF applications [162], [163], low power logic applications [164], bipolar effects [165]–[170], mobility behavior [171]–[174], temperature analysis [175]–[178], variability assessment [179]–[182], circuits [183], implementation in bulk technology [184]–[186], and potential use as sensors [187]–[189]. The application of JL as volatile memory is still at a very early stage. Guisi et al. [129] demonstrated the possibility of JL as DRAM with a gate length of 10 nm and film thickness of 3 nm with *RT* of few ms at 27 °C. However, its exploitation while showcasing insights into device physics with all the operations (Write, Hold and Read) requires further investigation.

1.6 Organisation of thesis

The research work presented in this thesis focuses on evaluating and optimizing different physical processes that govern the performance as a capacitorless dynamic memory while improving retention, read sensitivity, scalability, write time, and the limiting associated trade-offs in a junctionless capacitorless DRAM. The simulation of junctionless, devices in this thesis as 1T-DRAM was performed through Silvaco ATLAS simulation tool [190]. The thesis presents an advancement in JL based DRAM while progressing from a conventional double gate junctionless transistor to a vertically stacked JL and shell doped architecture. The concept, design, and operation of various architectures proposed in the work provide valuable viewpoints for JL based 1T-DRAM. The thesis presents systematic retention characteristics, which allows further optimization of scalability, speed, power, and read sensitivity.

Following is the chapter wise organization of the thesis:

Chapter 1 introduces the dynamic memory as an essential component for semiconductor industry. The investigation with emphasis on its requirement in the past as well as future prospects, reflects the need for replacing conventional DRAM (1T-1C) with different capacitorless DRAM transistor architectures. Further, the scaling issues (SCEs and BTBT) with formation of ultrasharp *pn* in nanoscale regime lead to the quest for a novel SOI device to function as 1T-DRAM in nanoscale regime. Junctionless transistor with same type of dopant throughout the film provides an alternate solution for low power dynamic memory. Therefore, this thesis work explores the potential of Junctionless transistor for capacitorless dynamic memory applications.

Chapter 2 highlights the advantages and challenges of a conventional Junctionless transistor as 1T-DRAM with an in-depth understanding of channel doping and different device parameters governing the memory operation. The previous work on Junctionless as a capacitorless DRAM [129], [130] achieves a lower retention (< 64 ms target specified by ITRS [30]) due to shallower potential depth and lower carrier lifetime. Therefore, JL devices with various channel

doping are analyzed, as the doping is critical to potential depth as well as carrier lifetime at higher temperature. The work shows the benefits of a deeper potential well and higher carrier lifetime through the use of moderate doping for standalone applications while shallower potential well at higher doping for embedded applications. Chapter 2 analyses a conventional DG JL architecture for standalone and embedded DRAM application by analysing metrics such as sense margin, retention time, current ratio, and speed.

Chapter 3 overcomes the relatively low retention of a junctionless transistor with the physical separation of conduction (top *n*-type JL layer) and storage (bottom *p*-type JL layer) regions through an oxide layer. The requirement of potential well for charge storage in this topology is based through a Metal-Oxide-Semiconductor (MOS) concept. The separation oxide between two regions allows the storage of holes away from the heavily doped (n^{++}) source and drain regions, which reduces the recombination and generation rate, and subsequently enhances the retention of state '1' and state '0', and thus, improves the retention time. The architecture achieves high retention even with a heavily doped junctionless film, and can be utilized as standalone memory for emerging technologies.

Chapter 4 presents a Shell-Doped (SD) architecture for capacitorless DRAM and utilizes the same for standalone and embedded DRAM applications. In SD topology, a heavily doped region (Shell) from source to drain region is partitioned through an intrinsic silicon film (Core), creating vertical layers of n^{++}-n^{+}-n^{++}, n^{+}-*i*-n^{+} and n^{++}-n^{+}-n^{++} regions. This topology shows advantage over double gate junctionless transistor with deeper potential well, and also overcomes the issue of stacked junctionless transistor with lower write time. SD junctionless transistor achieves better performance in terms of DRAM metrics and overcomes the trade-offs between metrics as compared to other junctionless architecture.

Chapter 5 summarizes the key results and contributions of this dissertation and proposes the scope for future work.

Appendix shows a typical Silvaco ATLAS program for creation of device architecture and DC I-V characteristic.

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Chapter 2

Assessment of Channel Doping in Junctionless Transistors for Capacitorless DRAM

2.1 Introduction

Conventional DRAM (1T-1C DRAM) cell consists of one transistor, utilized as a switch (pass transistor), and one capacitor for charge storage. However, the electrical charge can leak over time from the physical capacitor [1]–[5]. Also, downscaling of the capacitor is a challenging issue in DRAM as it reduces the charge storage, and hence, the capacitance. Therefore, DRAM must be refreshed periodically to preserve the data stored in capacitor and improve the retention characteristics [6]–[8]. Shorter period of refresh cycle negatively affects DRAM performance and power dissipation [1]–[5]. The downscaling issue associated with the physical capacitor in 1T-1C DRAM topology can be overcome with the use of a single SOI transistor [9]–[17].

A single transistor (1T) DRAM cell utilizes FBEs of SOI transistor for charge storage [9]–[17]. However, SOI MOSFETs have been aggressively scaled down to improve integration, speed, and functionality [18]–[20]. A MOS transistor with n^+-p-n^+ architecture can result in a higher off-current due to the *pn* junction, which is amplified at shorter channel lengths [18]–[20]. Also, the formation of ultrasharp abrupt *pn* junctions is difficult in the nanoscale regime [21], [22]. Therefore, the use of an Accumulation Mode (AM) or JL device has been encouraged as their channel body has the same polarity as that of S/D regions. AM MOSFETs offer better immunity to SCEs, higher current drivability, and easier fabrication process as compared to Inversion Mode (IM) devices [23]–[25]. The advantages offered by AM devices improve as the concentration increases beyond 10^{18} cm^{-3}, due to

the shifting of the conduction channel to the centre of the film for operation below flatband voltage. These devices are referred to as Junctionless transistors [24].

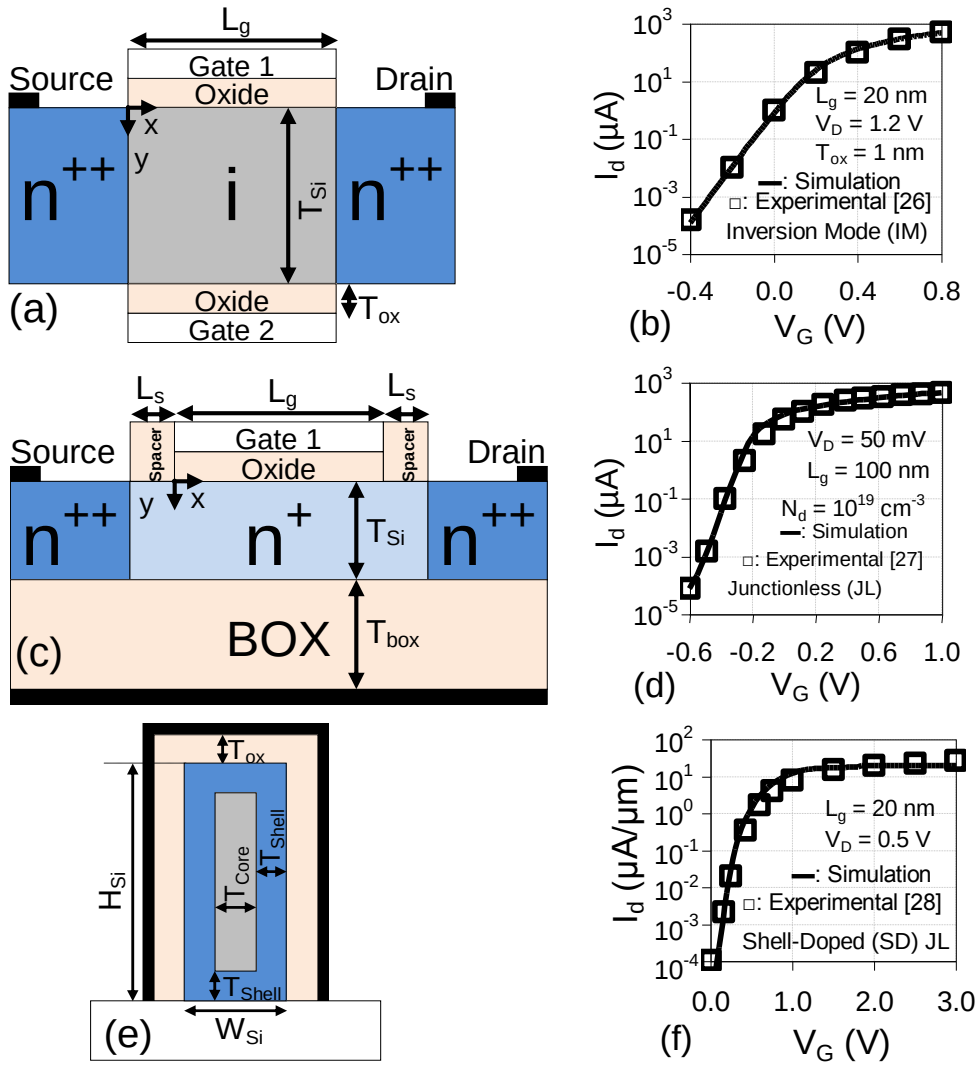

Fig. 2.1 Schematic diagram and comparison of simulation results (transfer characteristics (I_d-V_G)) with experimental data of (a-b) Inversion Mode with gate length of 20 nm at a drain bias of 1.2 V [26], (c-d) single gate Junctionless transistor with gate length of 100 nm at a drain bias of 50 mV [27] and (e-f) Shell-Doped (SD) JL architecture with gate length of 20 nm at a drain bias of 0.5 V [28].

This chapter presents a doping dependent analysis of AM and JL devices for functionality as 1T-DRAM with an independent gate operation. The chapter focuses on achieving high retention and improvement in DRAM metrics through the optimization of channel doping (N_d), silicon film thickness (T_{Si}), workfunction

of front and back gates (φ_{m1} and φ_{m2}), storage volume, and bias. Investigating the impact of total storage volume is essential for real time applications, and the contributing components of the same should be optimized to maximize the *RT* within smaller volume. The doping of the channel influences carrier lifetime and potential depth. However, decoupling their effect will be useful to ascertain the dominant factors for different doping values. The variation in channel doping shows reduced retention with increased doping, but higher doping can be exploited for the design of a high speed embedded memory. Insights into doping dependent characteristics for AM and JL devices along with storage volume analysis presents new viewpoints for efficient memory operation.

2.2 Calibration of physical models

In order to validate our simulation models, the results are compared with published experimental data (transfer characteristics (I_d-V_G)) of Double Gate (DG) IM (Figs. 2.1(a) and (b)) with gate length of 20 nm at drain bias of 1.2 V [26], single gate JL transistor (Figs. 2.1(c) and (d)) with gate length of 100 nm at drain bias of 50 mV [27] and SD JL devices (Figs. 2.1(e) and (f)) with gate length of 20 nm at drain bias 0.5 V [28], respectively.

2.3 Device description and simulation

The structures used in this chapter for 1T-DRAM are conventional *n*-type Double Gate (DG) JL (n^+ doping in the channel) and AM (*n* doping in the channel) device, with a n^{++} Source/Drain (S/D) doping of 10^{20} cm^{-3}, gate length (L_g) of 400 nm, oxide thickness (T_{ox}) of 1 nm with SiO_2 as the dielectric layer, and width (W_{Si}) as 1 μm as shown in Figs. 2.2(a) and (b) with the device specifications as in Table 2.1.

The design incorporates an underlap (L_{un}) and silicon film thickness (T_{Si}) of 10 nm, which are varied to study their impact on the performance metrics. DRAM functionality requires independent gate operation, where the front gate (G1) is utilized to regulate the conduction during Read operation, while the back gate (G2) is associated with charge storage and retention. Device analysis has been carried out using Atlas simulation software [29] using concentration dependent

model, bandgap narrowing, Lombardi mobility, Shockley-Read-Hall recombination model and Auger recombination model. The analysis for DRAM includes Impact Ionization (SELB) and standard Band-to-Band Tunneling (BTBT) models. The doping and temperature-dependent carrier lifetime [30] is also considered with default carrier lifetime (τ_0) of 100 ns. Fig. 2.2(c) shows the drain current (I_d) - front gate voltage (V_{G1}) characteristics for *n*-type channel doping (N_d = 10^{18} cm^{-3} to 10^{19} cm^{-3}) at 85 °C and a low drain (V_D) and back gate (V_{G2}) bias of 0.1 V. A lower off-current in transfer characteristics is observed at lower channel doping and higher workfunction due to depletion of more electrons from the silicon film and with at lower temperature due to lower thermal generation.

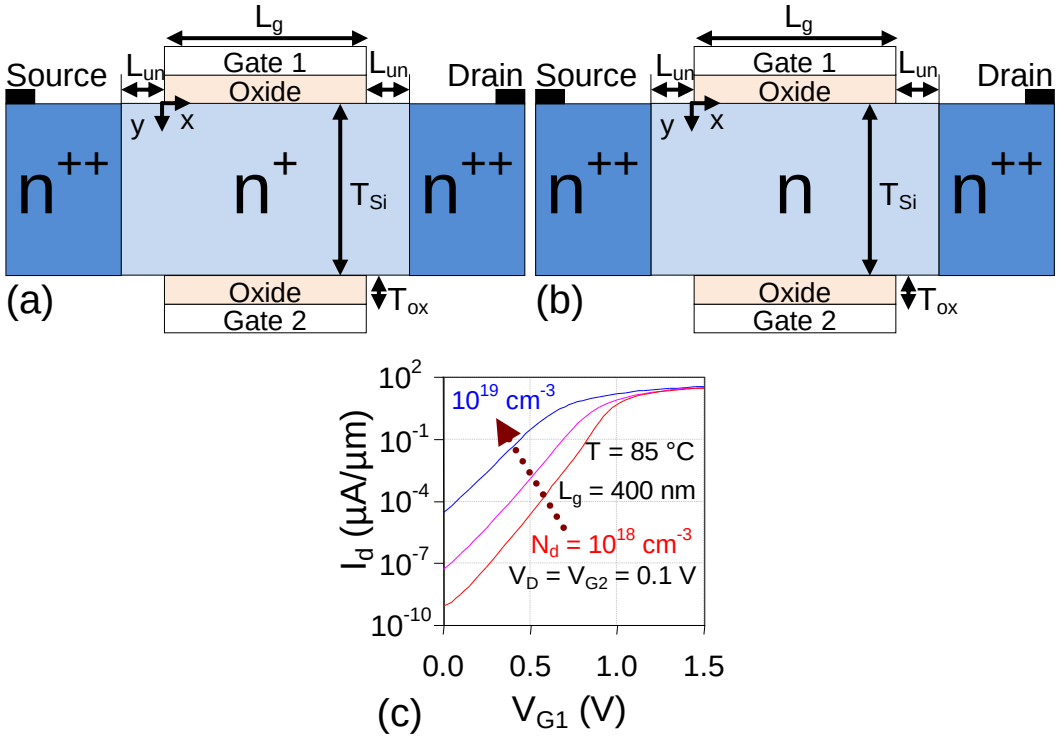

Fig. 2.2. Schematic diagram of conventional Double Gate (DG) (a) JL (n^+ doping in the channel) and (b) AM (*n* doping in the channel) MOSFET for 1T-DRAM. (c) Drain current (I_d) with front gate voltage (V_{G1}) for AM and JL with different channel doping (N_d) for gate length of 400 nm at 85 °C and drain bias (V_D) = back gate bias (V_{G2}) of 0.1 V.

This chapter showcases a systematic analysis with focus on achieving high retention time through the selection of optimal values of channel doping (N_d),

silicon film thickness (T_{Si}), workfunctions (φ_{m1} and φ_{m2}), architecture and bias for AM and JL devices. The key metric for DRAM performance is retention time, which evaluates the time for which a state can sustain and is governed through the generation and recombination of holes.

Table 2.1 Device specifications of AM and JL transistors for 1T-DRAM

Parameters	***Values***
Gate length (L_g)	400 nm - 25 nm
Width (W_{Si})	1 μm
Underlap length (L_{un})	10 nm - 16 nm
Silicon film thickness (T_{Si})	10 nm - 20 nm
Oxide thickness (T_{ox})	1 nm (SiO_2)
Front gate workfunction (φ_{m1})	5.0 eV
Back gate workfunction (φ_{m2})	5.2 eV
Source/Drain doping ($N_{d(S/D)}$)	10^{20} cm^{-3}
Channel doping (N_d) (*n*-type)	10^{17} cm^{-3} - 10^{19} cm^{-3}

2.4 Memory operation

DRAM memory operation is based on hole distribution in the storage region and is regulated through generation and recombination [14]. The methodology to balance generation and recombination of holes, described in [14], [31]–[34], is essential to operate DRAM and requires optimal biases. Fig. 2.3 shows the DRAM operation of state '1' (Write '1' (Fig. 2.3(a)), Hold '1' (Fig. 2.3(b)) and Read '1' (Fig. 2.3(c)) and state '0' (Write '0' (Fig. 2.3(d)), Hold '0' (Fig. 2.3(e)) and Read '0' (Fig. 2.3(f)) with hole distribution in the silicon film.

Write '1' (Fig. 2.3(a)) operation is performed with BTBT mechanism with a write time of 50 ns, which is a reliable and power-efficient mechanism as compared to Impact Ionization [34], [35]. In order to generate the holes in the semiconductor film, a negative voltage at the back (V_{G2_W1} = -1.6 V) and a positive bias at the drain (V_{D_W1} = 1.5 V) are applied. Under this condition, electrons in the valance band of the channel tunnel to the conduction band of the drain, which results in an increase of hole concentration in the storage region. The presence of excess holes

in the storage region shows the state '1' and results into higher read current (state '1'). The generated holes are evacuated from the storage region through Forward Bias (FB) mechanism (Fig. 2.3(d)). By applying a positive bias at front and back gate ($V_{G1\_W0} = V_{G2\_W0} = 1.5$ V) of the transistor, the potential increases and allows the holes in the storage region to recombine with electrons in the heavily doped source and drain [32], [36]. The absence of holes in the storage region results in a lower drain current (state '0').

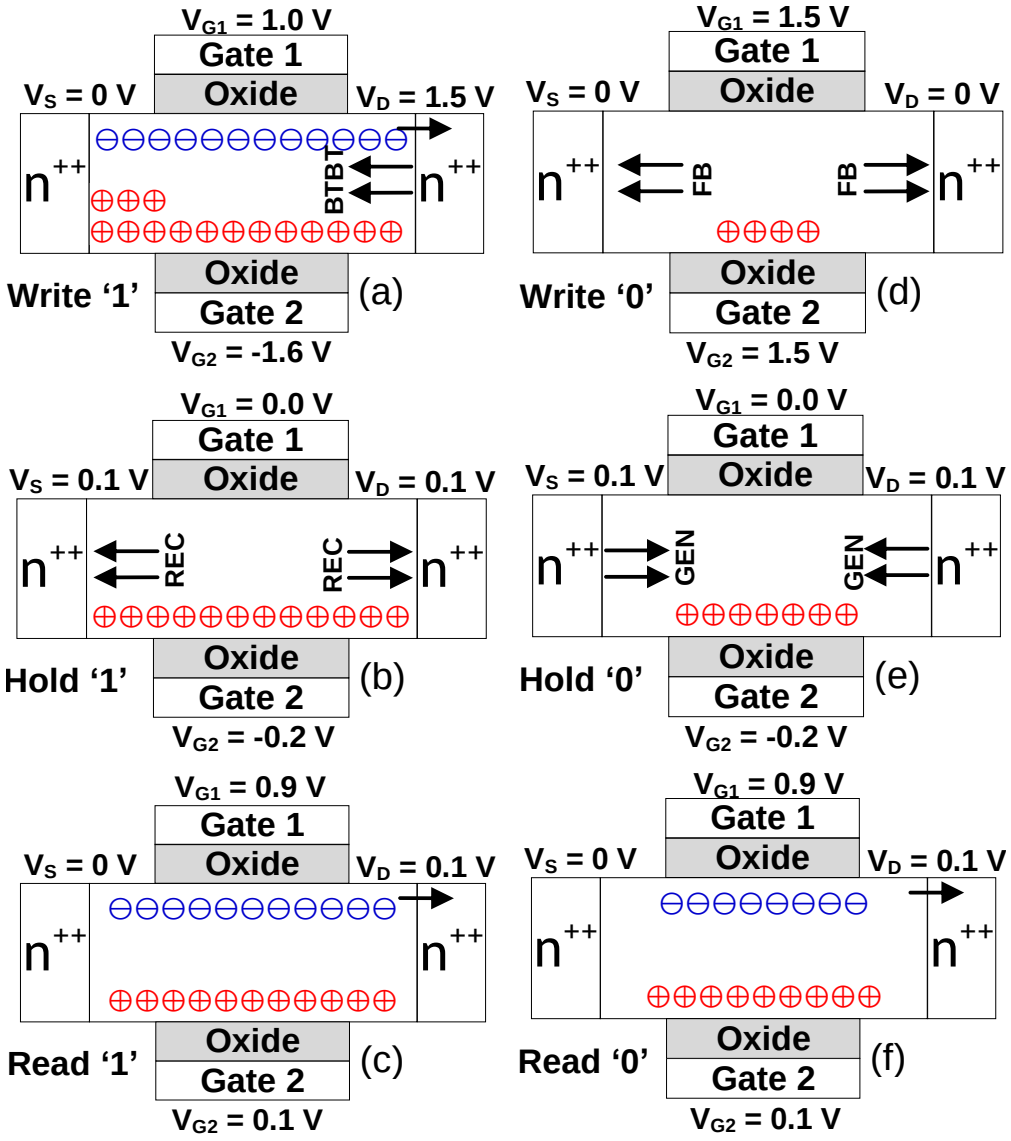

Fig. 2.3 Operation of JL and AM as a 1T DRAM with (a) Write '1', (b) Hold '1', (c) Read '1', (d) Write '0', (e) Hold '0' and (f) Read '0'. Various mechanisms in the devices are Band-To-Band-Tunneling (BTBT), Recombination (REC), Forward Bias (FB), and Generation (GEN). Arrow indicates direction of holes movement.

Read operation (Figs. 2.3(c) and 2.3 (f)) is performed to sense the presence (state '1') and absence (state '0') of holes from the storage region. During read operation, it is clearly observed that more (less) number holes at the back surface of the silicon film allows more (less) number electrons to diffuse to channel and drift towards the drain, thereby resulting in higher (lower) read current due to floating body effect in the device. The difference in the magnitude of current for state '1' and state '0' is termed as Sense Margin (*SM*). Also, the read '1' current and maximum *SM* depend on the generation of holes during Write '1' and holes during Hold '1'. Thus, an optimized bias and time during Write '1' is needed [35] and read operation is based on drift-diffusion mechanism. In order to sense these holes from the silicon film with an optimal *SM* and maximum *RT*, a front gate (V_{G1_R}) = 0.9 V with a low voltage of 0.1 V at drain (V_{D_R}) and back gate (V_{G2_R}) for 100 ns is utilized.

The Hold operation is performed between Write and Read operation. It is used to evaluate the Retention Time (*RT*). *RT* of the memory is defined as the time when maximum *SM* reaches to its 50% [34]–[41]. In some published text [42], the *RT* is estimated at 0% of maximum *SM*. The *RT* of the memory depends on the thermal recombination and diffusion of carriers during Hold '1', and thermal generation and BTBT during Hold '0'. The biasing is a factor to control the generation and recombination of carriers in the device. If a negative bias is applied at the back gate which forms a deeper potential well that helps to sustain the holes for a longer duration. On the other hand, higher negative bias increases the generation of carriers through BTBT and degrades the *RT* of state '0'. A positive bias during hold operation reduces the barrier, resulting in the recombination of carriers and degrades *RT* of the state '1'. Figs 2.3(b) shows that state '1' is disturbed by thermal recombination (REC) and diffusion of holes from the potential well while state '0' is perturbed by accumulation of holes in the potential well due to thermal generation (GEN) and BTBT of electrons as shown in Fig. 2.3(e). Therefore, the charge sustenance in the device is controlled during Hold operation with an optimized bias of V_{G2_H} = -0.2 V, V_{D_H} = 0.1 V and V_{S_H} = 0.1 V.

2.5 Impact of device parameters

AM and JL, being doped with same type of dopants throughout the semiconductor film, require careful understanding and optimization of crucial device parameters such as T_{Si}, T_{ox}, φ_{m1}, φ_{m2} and N_d for optimum DRAM performance.

2.5.1 Potential depth (ΔV) and Carrier lifetime (τ_0)

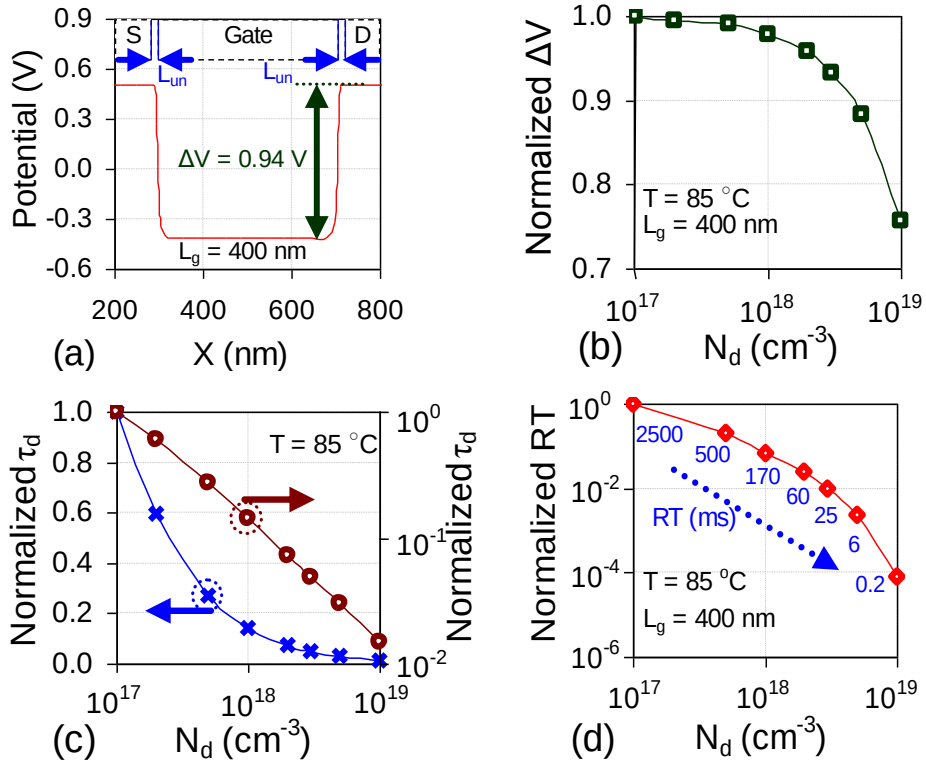

Fig. 2.4. (a) Variation in potential profile along the channel direction at zero bias for $N_d = 10^{18}$ cm^{-3}. Dependence of normalized (b) potential depth (ΔV), (c) doping dependent carrier lifetime (τ_d), and (d) *RT* on N_d for L_g of 400 nm at 85 °C. The cutlines for (a) and (b) are taken at a cross-section of 1 nm above the back surface. The normalization is carried out with respect to N_d of 10^{17} cm^{-3}.

The extent of depletion in vertical direction, expressed as potential depth (ΔV), and shown in Fig. 2.4(a), is one of the most critical parameters to determine the DRAM metrics (*SM* and *RT*) [14], [31]–[34]. As shown in Fig. 2.4(a), the depth of the potential well along with L_g defines the storage region, which must be maximized to enhance *RT*. A profound well sustains charges for longer duration that reduces hole recombination, and thus, maintains state '1'. The wider well suppresses leakage currents that enhances the retention [14], [34]. The doping of

the channel governs both carrier lifetime (τ_d) and depth of the potential well (ΔV). The default value of carrier lifetime (τ_0) for a doping of 10^{15} cm^{-3} at room temperature is 100 ns. The temperature dependent carrier lifetime, estimated through Schenk model [30], reduces to 76 ns at 85 °C for the same doping.

Figs. 2.4(b)-(d) show the variation of normalized (with respect to $N_d = 10^{17}$ cm^{-3}) potential depth (ΔV), doping dependent carrier lifetime (τ_d) at 85 °C, and *RT* for L_g = 400 nm, respectively, for a fixed set of device parameters. Fig. 2.4(b) shows that an increase in the doping reduces ΔV due to lesser extent of depletion in the semiconductor. The depletion of electrons from the film, and hence, the change in ΔV is minimal for $N_d = 10^{18}$ cm^{-3}. As shown in Fig. 2.4(c), carrier lifetime (τ_d) shows an exponential degradation with an increase in N_d as it reduces (from 76 ns for 10^{15} cm^{-3}) to 25 ns, 3.7 ns and 0.37 ns at 85 °C for channel doping of, 10^{17} cm^{-3}, 10^{18} cm^{-3}, and 10^{19} cm^{-3}, respectively. The reduction in ΔV and τ_d degrades *RT* from ~2.5 s ($N_d = 10^{17}$ cm^{-3}) to 200 µs ($N_d = 10^{19}$ cm^{-3}). ΔV and τ_d, both depend on N_d that governs *RT*, and therefore, understanding their individual effects is crucial. The impact of τ_d for a fixed ΔV (through constant φ_m, T_{Si}, and N_d) on the retention characteristics is shown. Such an approach allows the decoupling of two main parameters, namely, τ_d and ΔV, while evaluating their effect on retention. As observed in Figs. 2.4(b) and (c), for N_d lying between 10^{17} cm^{-3} to 10^{18} cm^{-3}, the variation in τ_d is significant rather than the reduction in ΔV, while for N_d beyond 10^{18} cm^{-3}, the reduction in ΔV is crucial.

Figs. 2.5(a) and (b) indicate that if there was no degradation in τ_d from 10^{17} cm^{-3} to 10^{18} cm^{-3} i.e. τ_d = 25 ns for both doping values, *RT* would have been 800 ms, whereas the degradation in lifetime results in a much reduced *RT* of 170 ms i.e. ~4.7 times lower. Similarly, if there was no reduction in τ_d from 10^{17} cm^{-3} to 10^{19} cm^{-3} i.e. τ_d = 25 ns for both, the *RT* would have been 400 µs, whereas the reduction in τ_d results in a value (200 µs) which is nearly half of that obtained for 10^{17} cm^{-3}. The results indicate a significnt impact of τ_d for $N_d \leq 10^{18}$ cm^{-3} while for higher doping, ΔV is critical. The potential depth signifies the barrier for electrons [14], and thus, influences read currents (I_1 and I_0) and *SM* as shown in Fig. 2.5(c). The increase in N_d enhances the magnitude of I_1 and I_0, with a

prominent impact on I_0 at $N_d \geq 5\times10^{18}$ cm^{-3}. This is evident from Fig. 2.5(c) that shows a significant change in current for state '0' for $N_d = 10^{19}$ cm^{-3}, and thus, a lower *SM* is observed. Higher N_d leads to a decrease in *SM* as well as *RT*.

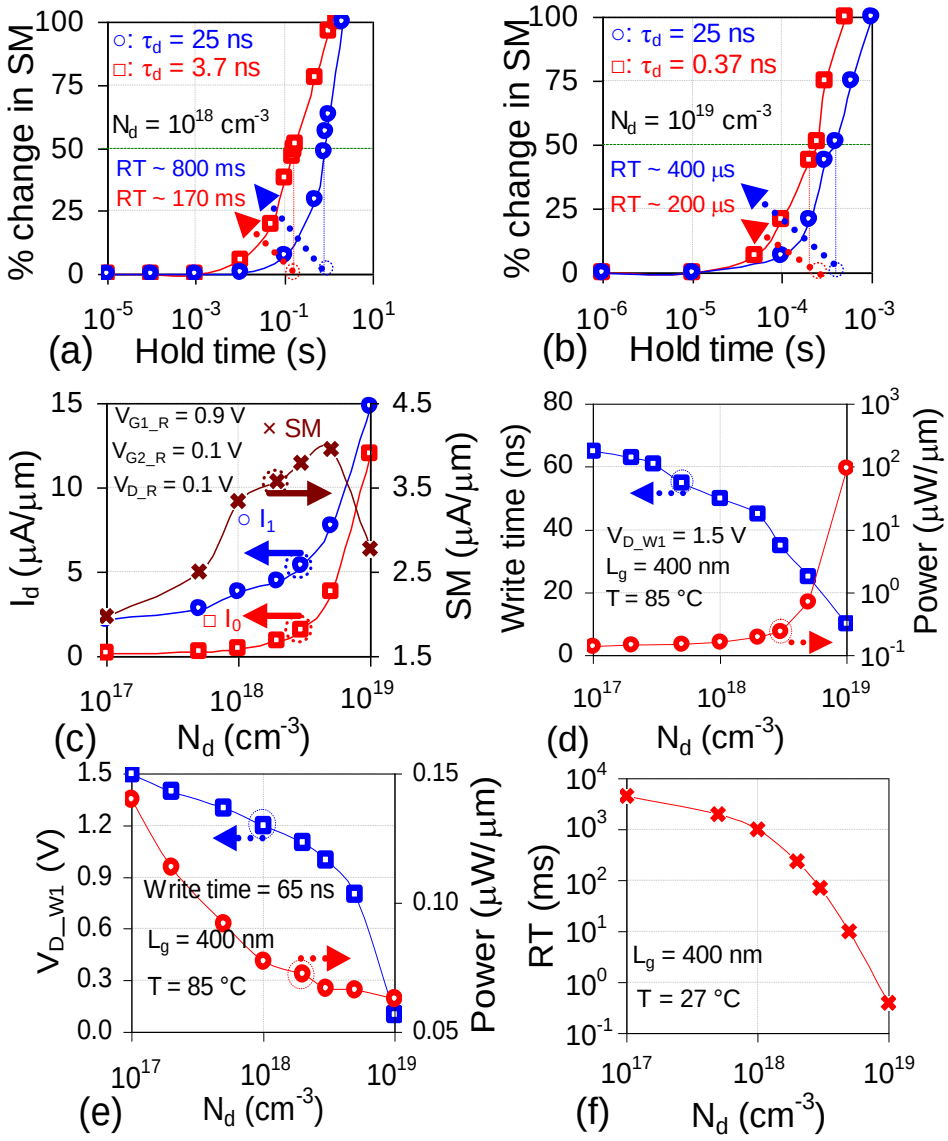

Fig. 2.5. Variation of *SM* with Hold time to estimate *RT* when *SM* is changed by 50% for N_d of (a) 10^{18} cm^{-3} with τ_d = 3.7 ns and 25 ns and (b) 10^{19} cm^{-3} with τ_d = 0.37 ns and τ_d = 25 ns. Dependence of (c) I_1, I_0, *SM*, (d) write time and power consumed during Write '1' for fixed V_{D_W1} = 1.5 V, (e) V_{D_W1} and power consumed during Write '1' for fixed write time = 65 ns and (f) *RT* on N_d.

A DRAM with higher N_d is benefited in terms of lower programming time and bias (Figs. 2.5(d) and (e)). This is due to the increase in carrier density in the silicon film [24]. The maximum time required to perform Write '1' operation for

channel doping of 10^{19} cm^{-3} is 10 ns for fixed drain bias of 1.5 V. The power consumption during Write '1' is estimated in terms of drain current for a fixed drain bias (Fig. 2.5(d) and (e)). The higher current during write operation results into an increased power consumption for higher N_d, reflecting a trade-off between speed and power. The operation can also be performed by increasing the write time and reducing the bias required. Therefore, for a fixed write time of 65 ns, JL devices consume less power due to requirement of lower drain bias. Thus, JL devices can be beneficial for embedded dynamic memory due to the low write time and power consumption with proper optimization. Further, evaluating doping dependent performance at 300 K, *RT* observed for 10^{17} cm^{-3} is ~4.5 s which decreases to ~1 s for $N_d = 10^{18}$ cm^{-3} and to 400 μs for 10^{19} cm^{-3} (Fig. 2.5(f)). The decreases in temperature reduces hole generation and recombination, and thus, improves *RT* [32], [34]. To further understand the impact of ΔV, N_d is fixed at 10^{17} cm^{-3} and 10^{18} cm^{-3}, and φ_m is varied.

Figs. 2.6(a) and (b) demonstrates a linear variation in ΔV, at both, front and back surfaces, with variation in front gate (φ_{m1}) and back gate workfunction (φ_{m2}), respectively. A higher φ_m depletes more electrons, thereby creating a profound potential well [14], [24]. Although φ_{m1} predominantly influences the region under G1, the variation at the back surface (Fig. 2.6(a)) reflects the coupling between the two gates. Thus, G1 and G2, both affect DRAM metrics. I_1 and I_0, both increase with decrease in φ_{m1}, due to barrier lowering for electrons. The linear increase in both currents shows an almost constant *SM* for $\varphi_{m1} < 4.9$ eV. A further increase in φ_{m1} results in an increased hole generation for state '0', and thus, increases I_0 increases and degrades *SM* for N_d of 10^{17} cm^{-3} and 10^{18} cm^{-3}. Although, $\varphi_{m2} = 5.0$ eV shows higher read current, compared to 5.2 eV due to lower barrier for electrons, it influences read '0' significantly, and hence, *SM* achieved for $\varphi_{m2} = 5.0$ eV is lower than that achieved for $\varphi_{m2} = 5.2$ eV (Fig. 2.6(c)). While a deeper well, attributed to higher φ_m can lead to higher *SM*, it also reflects an improved retention for N_d of 10^{17} cm^{-3}. A similar trend with lower value is observed for $N_d = 10^{18}$ cm^{-3} (Fig. 2.6(d)). The analysis confirms that a higher *RT* for AM device depends on the sustenance of state '1' due to the deeper ΔV. State '0' is

maintained for a longer duration due to the underlap region that decreases hole generation.

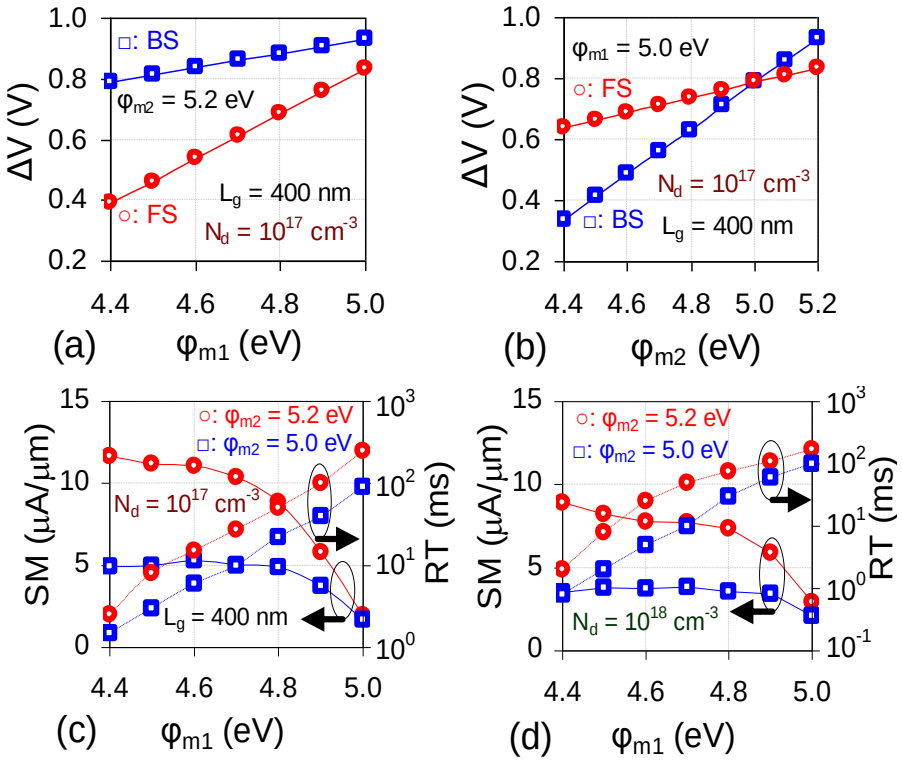

Fig. 2.6. Variation in ΔV with (a) front gate workfunction (φ_{m1}) for a fixed back gate workfunction (φ_{m2}) = 5.2 eV, (b) φ_{m2} for a fixed φ_{m1} = 5.0 eV with N_d of 10^{17} cm^{-3}. The cutlines are taken at a cross-section of 1 nm above the back surface of silicon film. Dependence of *SM* and *RT* on φ_{m1} and φ_{m2} with N_d of (c) 10^{17} cm^{-3}, and (d) 10^{18} cm^{-3}.

2.5.2 Gate length (L_g) scaling

The depth and width of the potential well varies with L_g, L_{un} and T_{Si} for 1T-DRAM [33], [35]. The width of ΔV is a direct consequence of L_g variation. However, ΔV is variable due to SCEs as observable in Fig. 2.7(a) for N_d = 10^{17} cm^{-3}. The device shows reduced SCEs due to use of a 10 nm underlap on both sides of the gate, which increases the effective channel length (L_{eff}) [43]. The effect of L_g on the read currents is observed with two different N_d values in Fig. 2.7(b). The read currents for both the states increase with a reduction in L_g. SCEs are observed for L_g being scaled down below 25 nm, which is evident through Fig. 2.7(c) that shows a reduction in *SM* for $L_g \leq$ 25 nm, and also, higher for a channel

doping of 10^{18} cm^{-3} as compared to that for 10^{17} cm^{-3}. This confirms that AM device with a higher N_d show more SCEs due to the decrease in L_{eff} for the same gate workfunction [43]. The effect of L_g on *RT* is shown in Fig. 2.7(d), where the decrease in *RT* is due to reduction in the storage area. For L_g = 25 nm with N_d = 10^{17} cm^{-3}, *RT* attained is ~90 ms at 85 °C. This shows a significant improvement in scalability achieved through optimized bias, workfunction, channel doping, and also, underlap length.

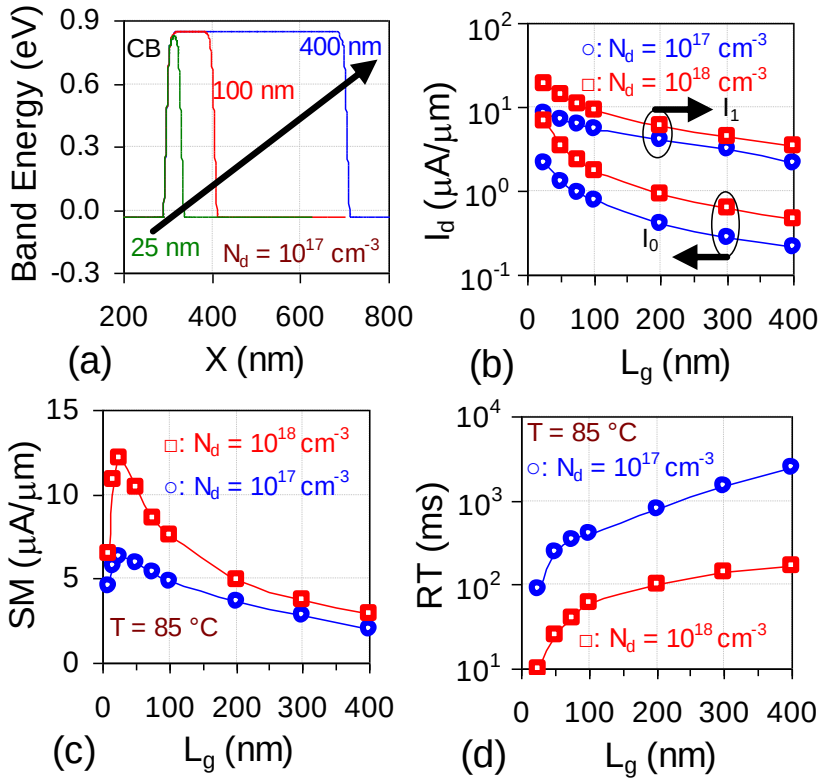

Fig. 2.7. (a) Variation in Conduction Band (CB) energy at Y = 0.5 nm along x (channel direction) for N_d of 10^{17} cm^{-3} with L_g = 25 nm, 100 nm and 400 nm. Variation in (b) I_1 and I_0, (c) *SM* and (d) *RT* as a function of gate length (L_g) for N_d of 10^{17} cm^{-3} and 10^{18} cm^{-3}.

2.5.3 Underlap length (L_{un})

The incorporation of an underlap (L_{un}) reduces the electric field as shown in Fig. 2.8(a). The generation of holes during Hold '0' in the silicon film is mainly governed by the lateral electric field that results in tunneling of electrons into drain/source, and hence, generation of holes in the semiconductor [33], [35]. The effect of L_{un} on read currents and *SM* is shown in Fig. 2.8(b). By increasing L_{un},

L_{eff} increases [43] that decrease I_1 and I_0, and thus, the *SM* reduces. The increase in effective storage region enhances *RT*. However, the significant impact is due to the decrease in the electric field at the junction that decreases BTBT, and hence, improves state '0' retention.

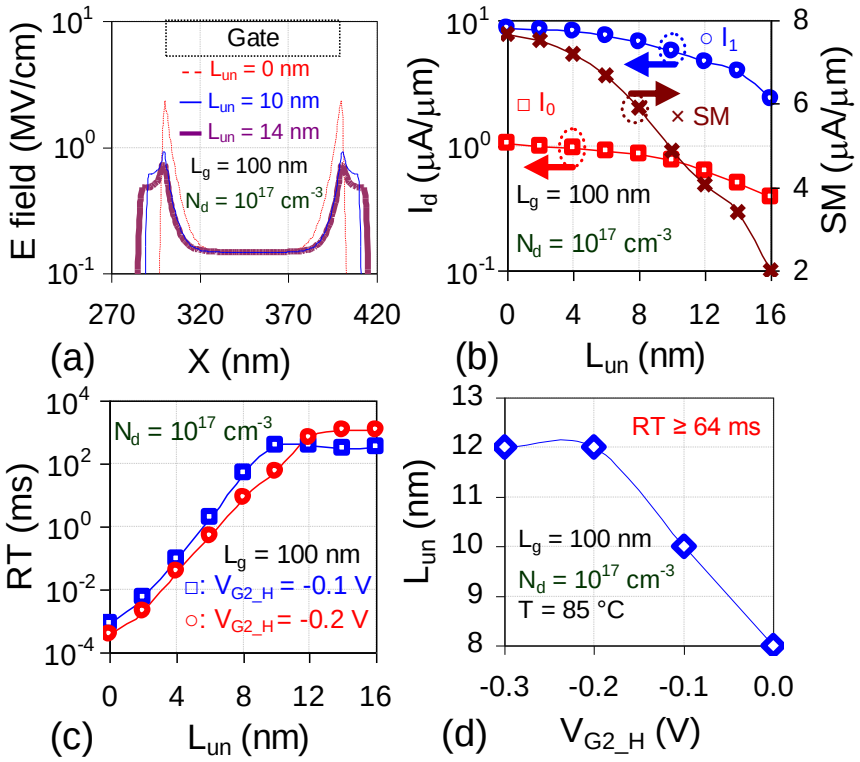

Fig. 2.8. Variation in (a) Electric field (E field) for different L_{un} (0 nm, 10 nm, and 14 nm) at zero bias extracted along *X*, 1 nm above back interface. Variation in (b) I_1, I_0 and *SM*, and (c) *RT* as a function of L_{un} and hold voltage (V_{G2_H}) with N_d of 10^{17} cm^{-3}. (d) Minimum L_{un} required to achieve $RT \geq 64$ ms for L_g = 100 nm as a function of hold voltage (V_{G2_H}) at 85 °C.

The application of a more negative bias results in enhanced hole generation [14], [31]–[33], and thus, requires a wider underlap, as illustrated in Figs. 2.8(c)-(d). With V_{G2_H} = -0.1 V, the maximum *RT* of 400 ms and 60 ms for L_g = 100 nm is achieved with L_{un} = 10 nm for N_d of 10^{17} cm^{-3} and 10^{18} cm^{-3}, respectively. The maximum *RT* = 1.2 s and 100 ms for N_d of 10^{17} cm^{-3} and 10^{18} cm^{-3}, respectively, is achieved for V_{G2_H} = -0.2 V which is attained at L_{un} = 14 nm. The work demonstrates the necessity of optimizing L_{un} with different hold voltages. Fig. 2.8(d) shows the same, highlighting the minimum underlap required to attain $RT \geq$ 64 ms at 85 °C, which decreases for more positive bias at N_d = 10^{17} cm^{-3}. Further

investigation shows that the use of a more negative bias (-0.2 V) at back gate with longer underlap (L_{un} = 14 nm) results in a threefold improvement in *RT* i.e. from 400 ms to 1.2 s, as compared to that achieved with a back bias of -0.1 V.

2.5.4 Silicon film thickness (T_{Si})

The scalability of 1T-DRAM is critical due to an increase in the leakage current and reduction in storage region, both of which limit the retention time [14], [32], [33], [35], [44]. A thinner silicon film and oxide are required for better gate controllability. IM transistors show super coupling effect for thinner film (< 20 nm), where the coexistence of electrons and holes in the film is difficult [45]. Contrary to AM devices, thin film of IM devices show enhanced tunneling current [32] that degrades the *RT*. On the contrary, AM or JL device is benefited with the use of thinner silicon film, which is helpful to deplete the carriers to turn-off the transistor [46]. Enhanced depletion in the vertical direction leads to the creation of a profound well that stores the charges for longer duration.

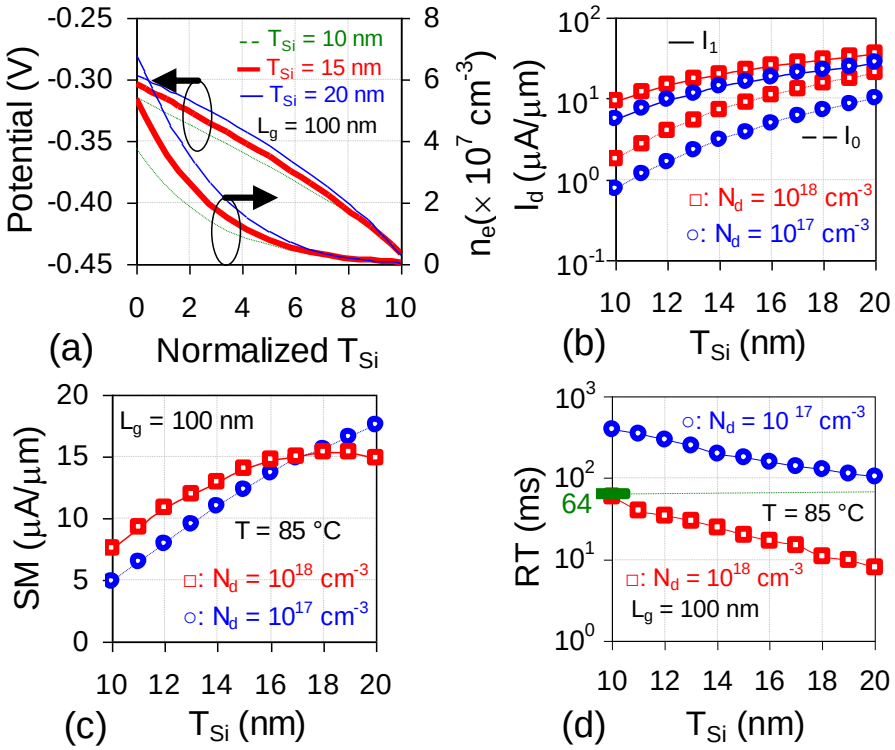

Fig. 2.9. Variation in (a) electron concentration (n_e) and potential in the silicon film along *Y*-direction at $X = L_g/2$ with normalized T_{Si} (10 nm) for the channel doping of 10^{17} cm^{-3}. Dependence of (b) read currents (I_1 and I_0), (c) *SM*, and (d) *RT* with T_{Si} for L_g of 100 nm with two different N_d = 10^{17} cm^{-3} and 10^{18} cm^{-3}.

The effect of film thickness (T_{Si}) on *RT* and *SM* for accumulation mode 1T-DRAM is investigated for L_g = 100 nm with channel doping 10^{17} cm^{-3} and 10^{18} cm^{-3}. Variation of potential and electron concentration is normalized with T_{Si} = 10 nm along the vertical direction at ($y = L_g/2$) for silicon film thickness (T_{Si} = 10 nm, 15 nm, and 20 nm) at zero bias with $N_d = 10^{17}$ cm^{-3} is shown in Fig. 2.9(a). The thinner film with moderate doping ($N_d = 10^{17}$ cm^{-3}) depletes more electrons and thus, shows a lower potential, and hence, lower read currents (I_1 and I_0) for both the states (Fig. 2.9 (b)). A thicker film with higher doping shows more SCEs [43] as evident from Fig. 2.9(c). *SM* and *RT* are shown in Figs. 2.9(c) and (d) which increases with T_{Si} while *RT* decreases. The *SM* with a channel doping of 10^{18} cm^{-3} starts decreasing for thicker T_{Si} ($\geq$ 17 nm) due to SCE that shows higher influence on the state "0" current for 10^{18} cm^{-3} as compared to 10^{17} cm^{-3}. The increase in film thickness enhances generation/recombination of carriers in AM and JL devices, and thus, degrades *RT*. Higher retention for thinner film thickness with moderate doping can be advantageous and consistent with downscaling of device, and could be beneficial when realized in vertical topology.

2.5.5 Volumetric analysis

Although the impact of individual device dimensions (L_g, T_{Si}) has been presented, the evaluation of composite volume metric can be beneficial for real-time applications. This is possible through the estimation of least volume of storage region that suggests the use of an optimal geometry. Thus, different combinations of $L_g \times T_{Si} \times W_{Si}$ (= 1 μm) are evaluated for a fixed volume with two different channel doping of 10^{17} cm^{-3} and 10^{18} cm^{-3}, as shown in Figs. 2.10(a) and (b), respectively. T_{Si} scaling reduces SCEs as well as depletes more electrons from the channel that enhances the retention of state '1', while downscaling of L_g reduces ΔV, and also, increase SCEs that degrades *RT*. It is shown that as T_{Si} is scaled down to 10 nm, the minimum allowed L_g is 25 nm for $N_d = 10^{17}$ cm^{-3}, whereas for $N_d = 10^{18}$ cm^{-3}, L_g greater than 100 nm is required for $RT \geq 64$ ms. Also, for a thicker T_{Si}, a longer L_g is needed to achieve $RT \geq 64$ ms at 85 °C. For a thinner film (T_{Si} = 10 nm), a change in L_g reduces *RT*, but *SM* largely remains unaffected. For a thicker film (T_{Si} = 20 nm), both *RT* and *SM* reduces with a decrease in L_g. The investigation of storage volume, ranging from 25×10^4 nm^3 to 10^6 nm^3

suggests that RT > 64 ms is possible for N_d = 10^{17} cm^{-3}. However, an optimal value of each dimension (L_g, T_{Si}) is essential.

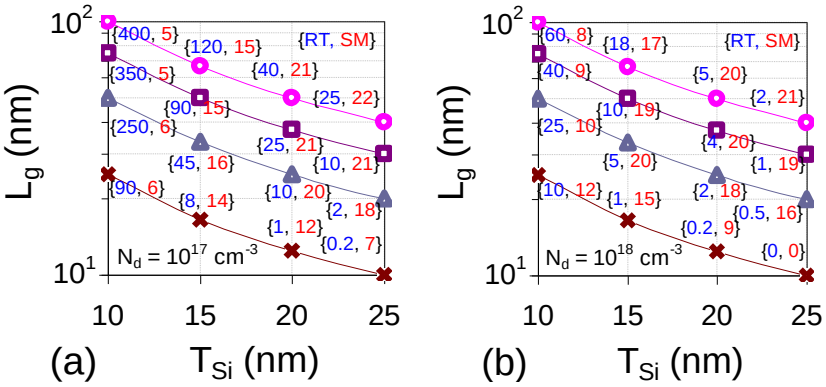

Fig. 2.10. Scaling of gate length (L_g) and silicon film thickness (T_{Si}) for different volume of the device for AM 1T-DRAM with (a) N_d = 10^{17} cm^{-3} and (b) N_d = 10^{18} cm^{-3}. Symbols (×), (Δ), (□) and (○) indicate for 2.5×10^5 nm^3, 5×10^5 nm^3, 7.5×10^5 nm^3 and 10×10^5 nm^3, respectively. RT in ms, and SM in μA/μm are expressed as {RT, SM} for each data point.

A comparison with other devices presents an improved retention characteristic with a thinner film thickness (Table 2.2), which also highlights better scaling capability. The investigation shows a better immunity to SCEs in thin film devices, and RT > 64 ms for L_g = 25 nm with N_d = 10^{17} cm^{-3}. DRAM metrics (SM, RT, and storage volume) for AM and JL devices are compared with similar architectures in Table I. Present work with N_d = 10^{17} cm^{-3} shows a higher RT as compared to previous work [37] with same storage volume of 40×10^5 nm^{-3}. When compared with a topology having twice the storage volume [47], our work with L_g = 100 nm shows a tenfold improvement in RT, but with sense margin as a compromise. Although RT is low for a heavily doped JL transistor (10^{19} cm^{-3}), results highlight a comparable retention [33] with a doping of 10^{15} cm^{-3}. The achieved retention paves a way forward towards further exploring JL transistor as DRAM with possible architecture changes. Also, RT > 64 ms is attained the minimum storage volume of 2.5×10^5 nm^{-3}, which is much higher than IM device [32] with almost same storage volume. Thus, the systematic analysis highlights enhancement in retention time at reduced storage volume through assessment of device as a function of doping and optimal device design.

Table 2.2 Comparison of present work with JL FETs [31], [48], IM transistors [32], [33], [44], [47], [49]–[52], Tunnel FET [37], IMOS [53].

Ref.	L_S *(nm)*	T_{Si} *(nm)*	V *($\times 10^5$ nm^3)*	*RT (ms)*	*T (°C)*	*SM (μA/μm)*	N_a, N_d *(cm^{-3})*
[31]	10	3	0.3	Few ms	27	2	10^{19}
[32]	100	100	100	1000	27	9	10^{17}
[33]	100	20	20	0.6	85	230	10^{15}
[37]	200	20	40	1500	85	0.14	10^{15}
[49]	70	20	14	150	85	165	10^{15}
[50]	170	20	34	3	85	210	10^{15}
[47]	105	20	21	167	85	170	10^{15}
[51]	75	16	120	10	85	40	10^{15}
[52]	75	9.5	----	10	85	44	10^{15}
[44]	50	10	5	40	27	----	10^{15}
[53]	75	16	37.5	320	85	3	5×10^{17}
[48]	100	10	10	30	27	60	5×10^{18}
This Work	25	10	2.5	90	85	6.32	10^{17}
	100	10	10	1200	85	3.4	10^{17}
	400	10	40	2500	85	2	10^{17}
	400	10	40	0.2	85	2.7	10^{19}

L_s indicates storage region.

2.6 Conclusion

The work presents an in-depth study of DRAM characteristics in terms of retention time and sense margin as a function of channel doping (10^{17} cm^{-3} to 10^{19} cm^{-3}) for an *n*-type independent gate DG AM and JL transistor at 85 °C. The analysis highlights two crucial parameters regulated by doping for dynamic memory applications, namely carrier lifetime and potential depth. While carrier lifetime for a fixed temperature is regulated by channel doping, the potential depth is also governed by device dimensions and gate workfunction. The impact of individual device dimensions along with their combined effect through storage volume analysis for different doping levels is presented. The results indicate the following:

(i) An increase in N_d reduces carrier lifetime with dominant impact limited up to a doping of 10^{18} cm^{-3}, which reduces *RT*. The reduction in the potential depth is more significant for $N_d > 10^{18}$ cm^{-3} that also leads to a decrease in *RT*,

(ii) Storage volume analysis with different combinations of ($L_g \times T_{Si} \times W_{Si}$) is useful being out the optimal device geometry to attain higher retention. The longer gate length and thinner film thickness in AM devices are benefited for longer charge sustenance. Thinner silicon film can result in reduced hole recombination and generation, thereby enhancing the charge retention,

(iii) As T_{Si} is scaled down to 10 nm, the minimum allowed L_g is 25 nm for N_d = 10^{17} cm^{-3} whereas, for $N_d = 10^{18}$ cm^{-3}, $L_g > 100$ nm is required to attain $RT \geq$ 64 ms,

(iv) Optimal gate workfunction aids in maintaining the potential depth that improves retention characteristics, and

(v) Although reduction in L_g reduces the capability of charge retention, optimal bias and underlap can yield a high retention time of ~1.2 seconds for L_g = 100 nm with $N_d = 10^{17}$ cm^{-3} at 85 °C

Further, the analysis highlights the possibility of JL transistors for high speed embedded memory with a low write time of ~10 ns for $N_d = 10^{19}$ cm^{-3} but with degraded retention time. The work showcases the usefulness of optimizing workfunction, silicon film thickness, gate length, underlap and bias with channel doping for optimum performance as dynamic memory.

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Chapter 3

Enhancement of Charge Retention through Separation of Conduction and Storage Regions

3.1 Introduction

Scaling of the capacitor in 1T-1C DRAM technology has become increasingly challenging [1]–[5]. The fabrication of this capacitor itself costs about 25% of the total cell cost, and also decreases yield and reliability, while limiting the retention as each memory cell requires a certain minimum storage capacitance to distinguish the states [5], [6]. SOI based 1T-DRAM have been proposed to overcome the problems associated with downscaling of the storage capacitor in 1T-1C DRAM [7], [8], [17]–[21], [9]–[16]. SOI transistor stores the charge in the floating body instead of a capacitor as in 1T-1C DRAM. However, downscaling of SOI transistors increases the leakage current due to SCEs and BTBT, which adversely impacts the charge retention [7], [8], [17]–[21], [9]–[16]. The most crucial aspect of 1T-DRAM is to analyse the scaling capability while maintaining a *RT* of 64 ms at higher temperatures [22]. JL shows better gate length scalability, although functionality as capacitorless dynamic memory is limited due to heavily doped channel, which increases recombination rate due to shallower potential well and lowers the carrier lifetime [23]–[25].

This chapter addresses the issue of low retention time in heavily doped JL 1T-DRAM through a *n*-Oxide-*p* JL architecture. The conventional JL architecture [23]–[25] is modified to isolate the conduction (top *n*-type JL) and storage regions (bottom *p*-type JL) through a separation oxide. The proposed topology requires simpler fabrication steps than the previously reported architectures for 1T-DRAM [26]–[29] as the device can be fabricated through steps outlined in [26]–[28], [30]–[33]. One of the advantages of utilizing the proposed Stacked JL (SJL)

transistor is the reduction in the etching step of separation oxide as compared to Silicon-with-partially- Insulating-layer-on-Silicon-on-Insulator (SISOI) structure [27]. Requirement of the separation oxide in the mid of the silicon film, as in A-RAM increases the fabrication complexity in the cell architecture [26], while A2RAM needs precise control on doping [28], [29]. The proposed structure is also beneficial, as it does not require the heavily doped S/D regions to be shared between conduction and storage regions. This reduces the hole generation during Hold '0' and recombination during Hold '1', and thus, can enhance the retention characteristics. The use of oxide layer (SOX), separating the conduction and storage regions reduces hole recombination, and also, generation of holes due to BTBT, and thus, can enhance Retention Time (*RT*). The regulation of hole recombination and generation is made feasible through the optimal use of each region for efficient functionality as standalone DRAM.

3.2 Design and operating principle

3.2.1 Device description

The analysis of SJL transistor as 1T-DRAM has been performed with ATLAS simulation software [34] using impact ionization, BTBT, and concentration dependent models. The other modules used are bandgap narrowing, Lombardi mobility, Shockley Read Hall (SRH) recombination model, and Auger recombination model. The structure of SJL transistor is shown in Fig. 3.1(a) with the device specifications as in Table I. The functionality as capacitorless DRAM needs independent gate operation, where the front gate (G1) is utilized to regulate the conduction through top region, while the back gate (G2) is associated with charge storage and retention. The creation of potential well in the *n*-Oxide-*p* SJL DRAM is crucial and is based on the Metal-Oxide-Semiconductor (MOS) concept i.e. heavily doped n^{++} S/D region behaves analogous to a metal (M), separation oxide as an Oxide (O) and *p*-doped storage region as a semiconductor (S) [35]. The impact of top (conduction) region on bottom (storage) region regulates the formation of potential well, which is governed through (a) MOS effect, and (b) front gate workfunction (φ_{m1}), which influences the storage region underneath S/D and channel regions, respectively. The impact of bottom region (*p*-type) on front region (*n*-type) controls read currents that determine *SM* as well as *RT*. The

difference between state '1' and '0' is termed as *SM* [14], [21], [36], [37], while *RT* is evaluated as time, when *SM* reaches 50 % of its maximum value [14], [21], [36], [37].

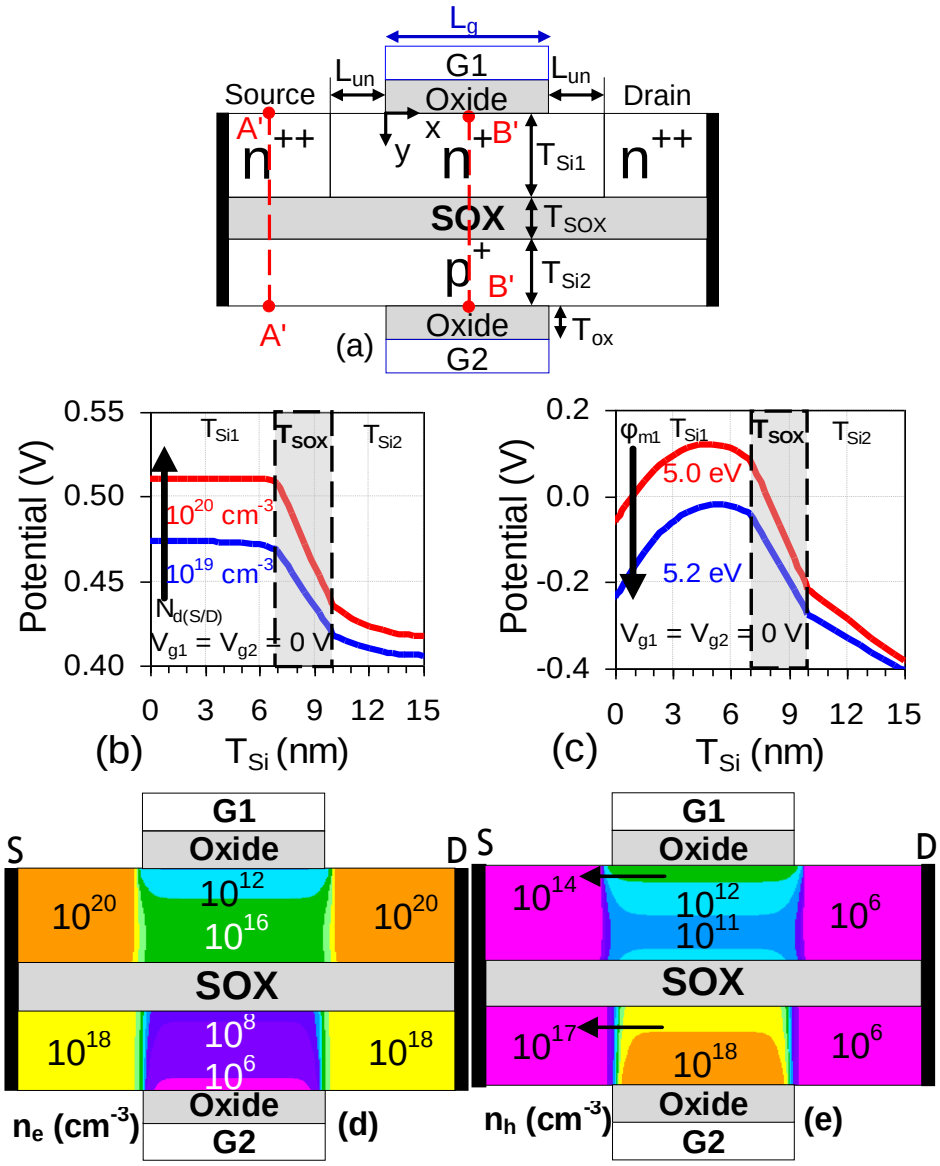

Fig. 3.1. (a) Schematic diagram of SJL transistor. Variation in the potential profile in the vertical direction with (b) S/D doping, $N_{d(S/D)}$ (A to A′) and (c) front gate workfunction, φ_{m1} (B to B′). V_{g1} and V_{g2} indicate front and back gate voltages, respectively. Contour plot of (d) electron concentration (n_e) and (e) hole concentration (n_h) at zero bias condition.

In order to understand the impact of heavily doped S/D (MOS effect) and gate workfunction on the potential profile in the silicon film, vertical cutlines are taken at source (A to A′) and channel region (B to B′), respectively, at zero bias (V_{g1} =

V_{g2} = 0 V). Fig. 3.1(b) demonstrates the variation in electrostatic potential in the storage region with S/D doping ($N_{d(S/D)}$) for a fixed N_a of 10^{17} cm^{-3}. S/D of the conduction region behaves as an equipotential region and depletes the holes from the storage region underneath S/D that creates a virtual *n*-type region. The MOS effect is confirmed through an increase in the potential underneath S/D region in T_{Si2} with increment in $N_{d(S/D)}$ (Fig. 3.1(b)). Further, the impact of φ_{m1} with a fixed φ_{m2} = 5.2 eV for N_a = 10^{17} cm^{-3} and N_d of 10^{19} cm^{-3} is shown in Fig. 3.1(c). The maximum potential in T_{Si1} is observed for lower φ_{m1} due to a lesser depletion of electrons. This also influences the potential of T_{Si2} underneath the gate. Higher φ_{m1} exhibits lower potential in the T_{Si2} due to accumulation of more holes, which along with *p*-type doping creates a deeper potential well that could sustain holes for a longer duration. The same can also be observed from contours of electron (n_e) and hole (n_h) concentration as shown in Figs. 3.1(d) and (e), respectively. The depletion of holes underneath the S/D regions (Fig. 3.1(d)) and accumulation of holes (Fig. 3.1(e)) at the back surface of T_{Si2} creates a virtual *n-p-n* region that is responsible for formation of a deeper potential well for charge storage and further functionality as DRAM with various physical phenomena as shown in Fig. 3.2.

Table 3.1 Device specifications of SJL transistor for 1T-DRAM

Parameters	***Values***
Gate length (L_g)	200 nm - 20 nm
Width (W_{Si})	1 μm
Underlap length (L_{un})	10 nm
Conduction region thickness (T_{Si1})	7 nm
Storage region thickness (T_{Si2})	4 nm - 12 nm
Oxide thickness (T_{ox})	1 nm (SiO_2)
Separation oxide thickness (T_{SOX}/EOT_{SOX})	0.5 nm - 6 nm
Front gate workfunction (φ_{m1})	5.0 eV
Film thickness (T_{Si})	T_{Si1} + T_{SOX} + T_{Si2}
Back gate workfunction (φ_{m2})	5.2 eV
Source/Drain doping ($N_{d(S/D)}$)	10^{20} cm^{-3}
Conduction region doping (N_d) (*n*-type)	5×10^{18} cm^{-3} and 10^{19} cm^{-3}
Storage region doping (N_a) (*p*-type)	10^{17} cm^{-3} - 10^{19} cm^{-3}

3.2.2 Operation

The working of SJL as a 1T-DRAM (with optimized biasing and timing schemes) is illustrated in Figs. 3.2(a)-(e), with different operations: (a) Write '1', (b) Hold '1', (c) Read '1', (d) Write '0', (e) Hold '0' and (f) Read '0'. The generation of holes during Write '1' (W_1) in T_{Si2} is performed through BTBT mechanism [14], [21], [36]. The presence of holes in the storage region indicates state '1' (high current) of the memory.

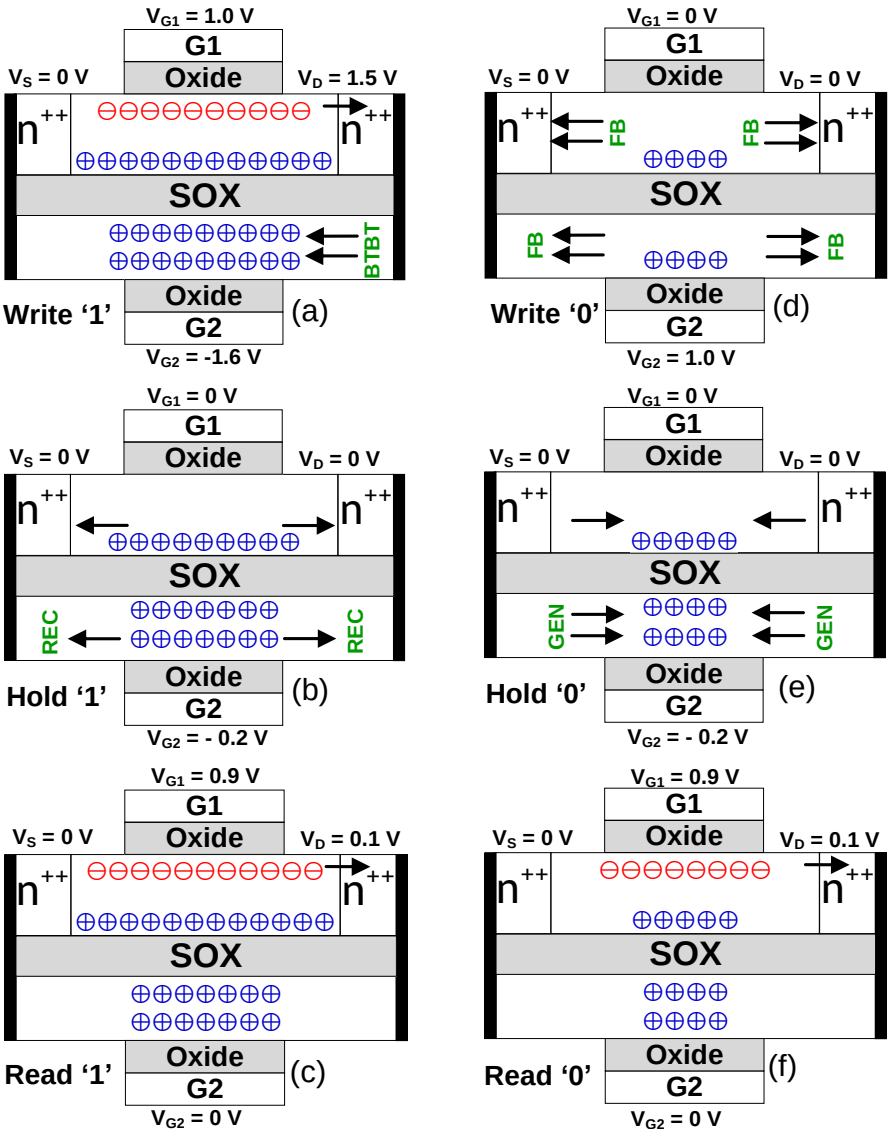

Fig. 3.2. Schematic representation of SJL as 1T-DRAM with bias scheme to perform various operations, (a) Write '1', (b) Hold '1', (c) Read '1', (d) Write '0', (e) Hold '0' and (f) Read '0'. BTBT, REC, FB, GEN indicate Band-To-Band-Tunneling, Recombination, Forward Bias, and Generation, respectively. Arrow indicates holes movement.

Write ‘0’ (W_0) is characterized by the removal of holes from the storage region. The operation is performed with Forward Bias (FB) mechanism by applying a positive bias at the back gate. This forward bias allows holes to recombine with virtual *n* region (underneath S/D regions) [14], [21], [36]. The reduction in barrier permits holes to recombine with electrons. This reduction in hole concentration from storage region repersents the state ‘0’ (low current) of the memory. In order to read these states, a front gate (V_{G1_R} = 0.9 V) with a drain voltage (V_{D_R}) = 0.1 V is applied. *RT* of memory depends on the thermal recombination (REC) and diffusion of carriers during Hold ‘1’ and generation (GEN) of holes due to thermal generation and BTBT during Hold ‘0’ [14], [21], [36]. The controlling of generation and recombination during hold and read operation through bias is also crucial [21], [36], [38]–[40]. Therefore, appropriate hold bias is applied to achieve high retention, which is integrated with optimal doping and device dimensions.

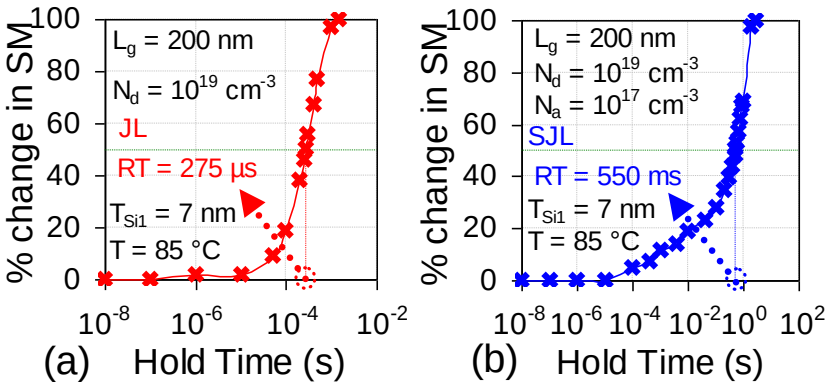

Fig. 3.3. Variation in *SM* with hold time with *RT* estimated when *SM* is 50 % of its maximum value for (a) JL and (b) SJL with N_d of 10^{19} cm^{-3} for L_g of 200 nm. N_a for SJL transistor is 10^{17} cm^{-3}.

Fig. 3.3(a) and (b) show the variation in *SM* with hold time for JL and SJL transistors, respectively. Results show an improvement in *RT* by a factor of ~10^3, for same device parameters (N_d, L_g, T_{Si1}, φ_{m1}, φ_{m2}) and programming scheme, which reflects on the significance of device architecture for DRAM perspective. The use of a thinner silicon film in JL (T_{Si} = T_{Si1}) than in SJL (T_{Si} = T_{Si1}+ T_{SOX} + T_{Si2}) is beneficial as it reduces BTBT [25] and improves the retention characteristics, but the values attained are still lower than that observed in SJL device. This chapter outlines a systematic analysis of devices dimension along

with the utility of such a topology for improved retention. Other than device architecture, bias and gate workfunction, the formation and maintenance of potential well in SJL transistor is regulated by Separation Oxide (SOX) thickness (T_{SOX}), storage region doping (N_a), conduction region doping (N_d), gate length (L_g), and storage thickness (T_{Si2}).

3.3 Effect of device parameters

3.3.1 Effect of separation oxide thickness (T_{SOX}) and materials

The main focus of this chapter is to enhance *RT* of JL based 1T-DRAM achieved through separation of conduction and storage regions. The separation oxide (SOX) between two regions allows the storage of holes away from the heavily doped (n^{++}) S/D regions. It increases hole sustenance in state '1', and also, reduces BTBT that enhances state '0' retention.

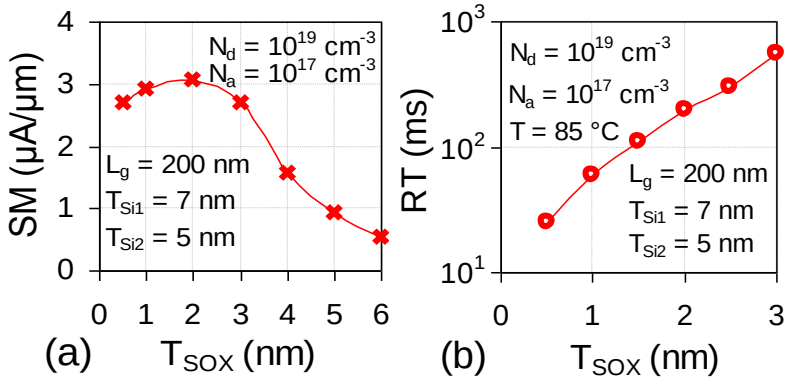

Fig. 3.4. Variation in (a) *SM* and (b) *RT* with T_{SOX} for N_d of 10^{19} cm^{-3}, N_a of 10^{17} cm^{-3} and L_g = 200 nm at 85 °C.

The reduced influence of back gate workfunction decreases electron depletion from conduction region, which results into higher read currents, and thus, improves *SM* (Fig. 3.4(a)). The difference between state '1' and '0' increases and attains maximum at T_{SOX} = 2 nm (*SM* = ~3 µA/µm). However, further increase in T_{SOX} reduces *SM*. The reduction in *SM* is attributed to the higher degree of change in state '0' current compared to that in state '1'. The state '1' current is influenced by the holes accumulated in the storage region that increases the effective potential during read, and thus, state '1' current is higher than state '0'. However, a thicker separation oxide lowers the impact of stored holes, and thus, effectively

reduces state '1' current. The combined effect of holes in the storage region and back gate workfunction reduces *SM* for T_{SOX} > 2 nm. Fig. 3.4(b) shows the increase in *RT* with T_{SOX}. A thinner T_{SOX} results in an enhancement depletion of holes underneath heavily doped S/D regions, which increases the lateral electric field. Higher electric field increases hole generation during Hold '0' due to BTBT, and thus, degrades *RT*. Although thicker T_{SOX} increases *RT*, the *SM* reduces (Fig. 3.4(a)). Moreover, a thicker T_{SOX} reduces generation of holes during Write '1' due to a decrease in electric field that necessitates the use of either higher bias or higher write time. Thus, optimal T_{SOX} of 3 nm is used to achieve maximum *RT* (~550 ms), an acceptable *SM* (~2.7 μA/μm) with write time of 100 ns for N_d of 10^{19} cm^{-3} and N_a of 10^{17} cm^{-3} with gate length of 200 nm at 85 ℃.

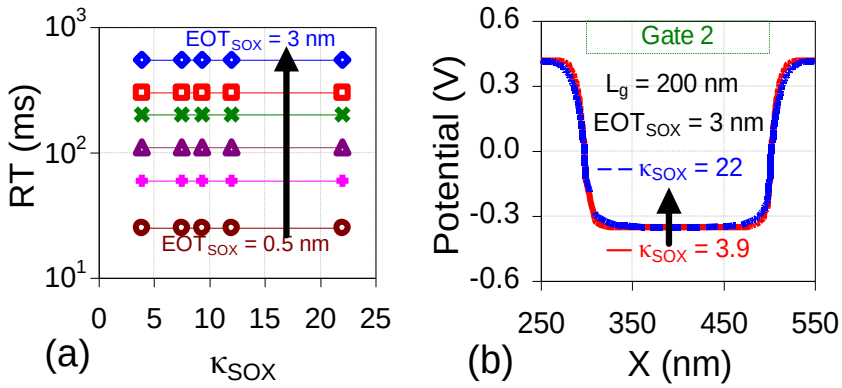

Fig. 3.5. Variation in (a) *RT* with dielectric constant (κ_{SOX}) when EOT_{SOX} is varied from 0.5 nm to 3 nm, and (b) potential profile along the *x*-direction (channel direction) for different κ_{SOX}.

The most critical aspect of the architecture is SOX, which separates holes from the conduction region (*n*-type) and aids in achieving a higher *RT*. Impact of different dielectric materials for SOX along with Equivalent Oxide Thickness (EOT_{SOX}) is analyzed in Fig. 3.5(a). For the same EOT_{SOX}, the depletion of holes underneath S/D regions results into the same potential depth (Fig. 3.5(b)). Therefore, *RT* is constant for different SOX materials (SiO_2, Si_3N_4, Al_2O_3, $HfSiO_4$ and HfO_2) with same EOT_{SOX}. In order to understand the degradation of *RT* with variation in EOT_{SOX}, Fig. 3.6 shows contour plots of hole concentration (n_h) during Hold '1' (Figs. 3.6(a)-(c)) and Hold '0' (Figs. 3.6(d)-(f)) operations. During Hold '1', the hole concentration decreases with an increase in EOT_{SOX} due

to recombination (shallower potential depth due to electrostatic doping) which degrades I_1 [14]. Thinner EOT_{SOX} increases the electric field in T_{Si2}, which results in higher BTBT that degrades I_0.

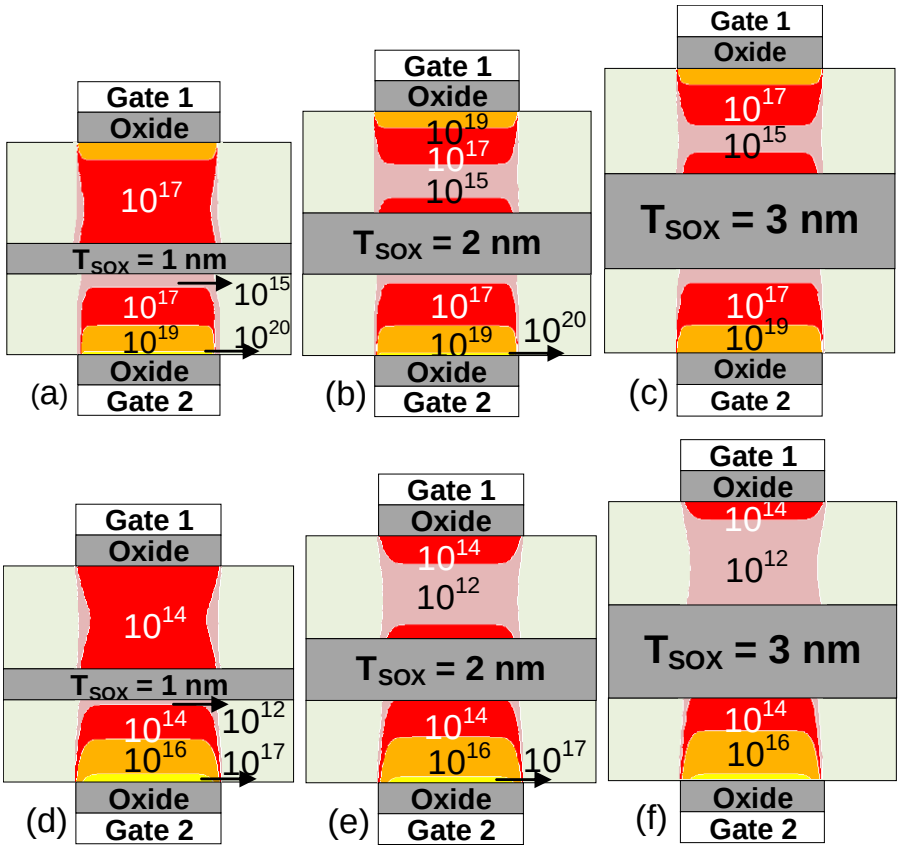

Fig. 3.6. Contour plots showing the n_h for different T_{SOX} values ranging from 1 nm to 3 nm during ((a)-(c)) for Hold '1' and ((d)-(f)) for Hold '0' at V_{G2_H} = -0.2 V.

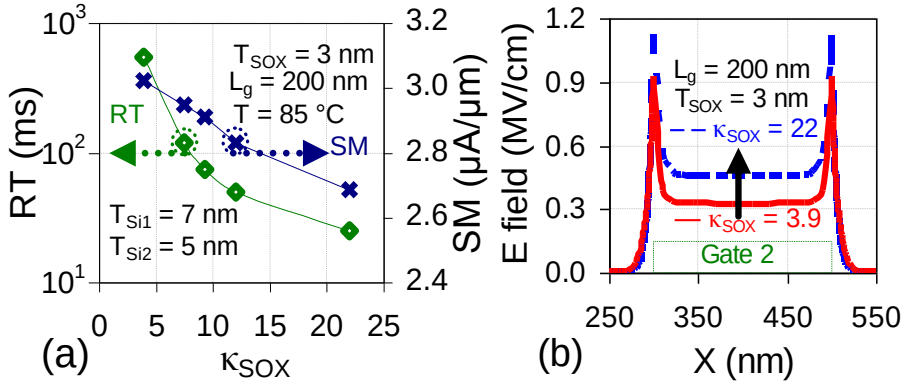

Fig. 3.7. Variation in (a) *RT* and *SM* with κ_{SOX} for T_{SOX} = 3 nm, and (b) Electric field (E field) along the *x*-direction for different κ_{SOX}.

Fig. 3.7(a) shows the reduction in *RT* and *SM* with dielectric constant for T_{SOX} = 3 nm. A reduction in T_{SOX} increases (i) depletion of holes underneath S/D regions, and (ii) accumulation of holes underneath the gate that results in a higher electric field (Fig. 3.7(b)). *RT* of ~550 ms and ~30 ms were achieved with lower κ_{SOX} (SiO_2) and higher κ_{SOX} (HfO_2) materials, respectively. The reduction in *SM* (3.9 µA/µm to 2.7 µA/µm) with κ_{SOX} is due to the increased impact of back gate workfunction on the conduction region (T_{Si1}), which depletes electrons and lowers I_1 and I_0, and thus, a reduction in *SM*. With use of $\kappa_{SOX} < \kappa_{Si}$ as dielectric material for SOX, SJL based 1T-DRAM exhibits enhanced performance [26].

3.3.2 Effect of doping (N_a and N_d)

The doping dependent factors, which modulate the *RT* of memory, are potential depth and carrier lifetime [14], [25], [36], [39]. Fig. 3.8(a) shows the potential profile along *x*-direction for different N_a. The reduction in the depth of potential well due to higher doping of the storage region is governed by the MOS concept [35]. The higher doping of the storage region along with the high workfunction at the back gate lowers the potential to store holes for longer duration. However, with higher doping of the storage region, the extent of hole depletion in the storage region underneath the heavily doped (n^{++}) S/D regions also reduces. This result into a greater change in potential for regions under S/D, as compared to channel in the storage region, which leads to shallower potential depth.

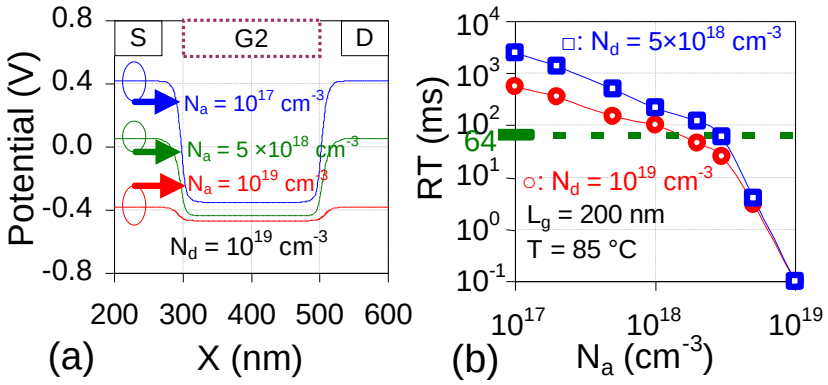

Fig. 3.8. Variation in (a) potential profile along *x*-direction for different storage region doping (N_a = 10^{17} cm^{-3}, 5×10^{18} cm^{-3} and 10^{19} cm^{-3}). Cutlines are taken at 1 nm above the back surface of storage region. (b) Dependence of *RT* on N_a for two different N_d of 5×10^{18} and 10^{19} cm^{-3} with L_g of 200 nm at 85 °C.

Fig. 3.8(a) confirms that the potential depth for doping N_a < 5×10^{18} cm^{-3} can create a n^+-p-n^+ that results into deeper potential well, while for $N_a \geq 5\times10^{18}$ cm^{-3}, a shallower potential depth is observed. The shallower potential depth decreases *RT*, which further reduces with an increase in doping of the storage region (Fig. 3.8(b)). The variation in *RT* with N_a for two different N_d (5×10^{18} cm^{-3} and 10^{19} cm^{-3}) at L_g of 200 nm is shown in Fig. 3.8(b). The maximum *RT* = ~2.5 s is achieved for $N_d = 5\times10^{18}$ cm^{-3} with storage region doping of 10^{17} cm^{-3} at L_g of 200 nm and 85 °C.

3.3.3 Gate length (L_g) scaling

The reduction of the storage region of the memory with gate length downscaling affects DRAM metrics due to SCEs and BTBT in the device [11], [13], [36], [41]. The variation in *SM* with gate length (L_g) for N_d of 5×10^{18} cm^{-3} and 10^{19} cm^{-3} with fixed N_a of 10^{17} cm^{-3}, and fixed T_{Si2} of 5 nm is shown in Fig. 3.9(a). A lower doping in JL transistor suppresses SCEs [42]. *SM* of SJL DRAM increases with gate length scaling, but decreases beyond 75 nm and 50 nm for N_d of 10^{19} cm^{-3} and 5×10^{18} cm^{-3}, respectively, due to SCEs.

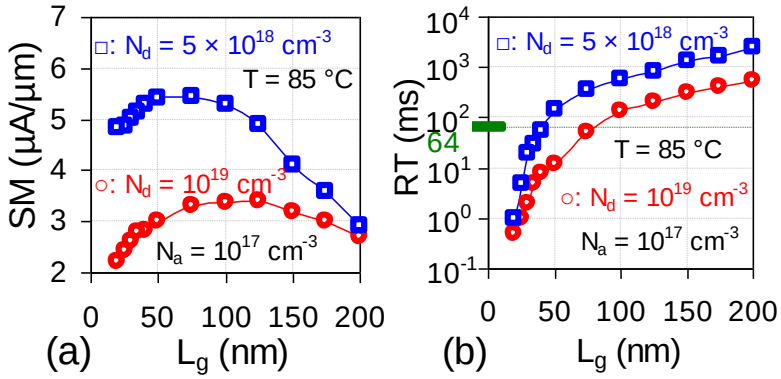

Fig. 3.9. Dependence of (a) *SM* and (b) *RT* with gate length ($L_g = L_{g1} = L_{g2}$) for N_d of 5×10^{18} cm^{-3} and 10^{19} cm^{-3} for fixed N_a of 10^{17} cm^{-3} at 85 °C.

Secondly, the issue related to BTBT is overcome through the use of an underlap, which reduces the lateral electric field [36], [43]. The inclusion of underlap also increases the effective channel length (L_{eff}), but its impact is significant at shorter gate lengths [43], [44]. Fig. 3.9(b) shows the dependence of *RT* with gate length for N_d of 5×10^{18} cm^{-3} and 10^{19} cm^{-3} with N_a of 10^{17} cm^{-3}. The maximum *RT* ~2.5 s

and ~550 ms for N_d as 5×10^{18} cm^{-3} and 10^{19} cm^{-3}, respectively, is achieved for L_g = 200 nm. Gate length of SJL based 1T-DRAM can be scaled down to 20 nm with *RT* of 1 ms for N_d of 5×10^{18} cm^{-3}.

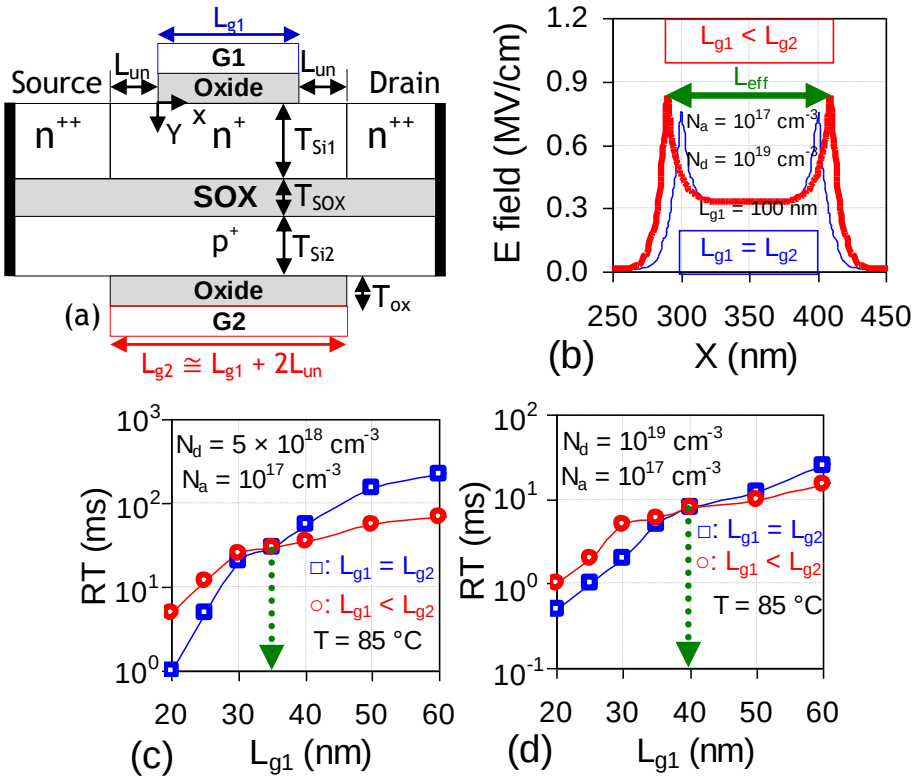

Fig. 3.10. (a) Schematic of SJL transistor with an oversized back gate ($L_{g2} \cong L_{g1} + 2L_{un}$). (b) Variation in electric field (E field) for architecture with $L_{g2} = L_{g1}$ and $L_{g2} > L_{g1}$ for L_{g1} = 100 nm. Dependence of *RT* on L_{g1} for (c) $N_d = 5\times10^{18}$ cm^{-3} and (d) $N_d = 10^{19}$ cm^{-3} with $N_a = 10^{17}$ cm^{-3} at 85 °C.

RT can be further improved for shorter gate lengths (L_{g1}) through use of an oversized back gate ($L_{g2} \cong L_{g1} + 2L_{un}$), which aids in enhancing the storage region for holes. Fig. 3.10(a) shows the schematic diagram of SJL transistor with oversized back gate. Fig. 3.10(b) shows the higher electric field (E field) for a structure with an oversized back gate as compared to self-aligned ($L_{g1} = L_{g2}$) device (Fig. 1(a)) for L_{g1} of 100 nm due to the reduced influence of front gate [5]. Figs. 3.10(c) and (d) show the variation of *RT* with self-aligned and oversized back gate structures for N_d of 5×10^{18} cm^{-3} and 10^{19} cm^{-3} respectively, with fixed N_a of 10^{17} cm^{-3}. For L_{g1} > 35 nm, N_d of 5×10^{18} cm^{-3} and L_{g1} > 40 nm with N_d of 10^{19} cm^{-3}, *RT* is less than the case with $L_{g1} = L_{g2}$ due to high electric field, which

increases BTBT and generates more holes for state '0' while for $L_{g1} \leq 35$ nm with N_d of 5×10^{18} cm^{-3} and $L_{g1} \leq 40$ nm for $N_d = 10^{19}$ cm^{-3}, retention time is higher than the case with $L_{g1} = L_{g2}$ due to an increase in the effective storage region. Thus, the use of an oversized back gate in SJL transistor can results in a *RT* of 1 ms for N_d of 10^{19} cm^{-3} and 5 ms for 5×10^{18} cm^{-3} with L_g of 20 nm at 85 °C.

3.3.4 Effect of thickness of storage region (T_{Si2})

The scaling of storage region (T_{Si2}) is analyzed for a gate length of 200 nm and 75 nm with T_{Si1} = 7 nm, T_{SOX} = 3 nm, $N_d = 10^{19}$ cm^{-3} and N_a of 10^{17} cm^{-3}. Thinner T_{Si2} increases the influence of back gate, which depletes more electrons from T_{Si1}, and thus, reduces read currents (I_1 and I_0). Focusing on *RT*, a thinner T_{Si2} increases BTBT due to an increase in the electric field that degrades *RT*. A thicker T_{Si2} reduces the potential depth due to a lesser depletion of holes underneath the S/D regions that results into an increase in the diffusion of holes from the storage region during state '1', and thus, reduces *RT*.

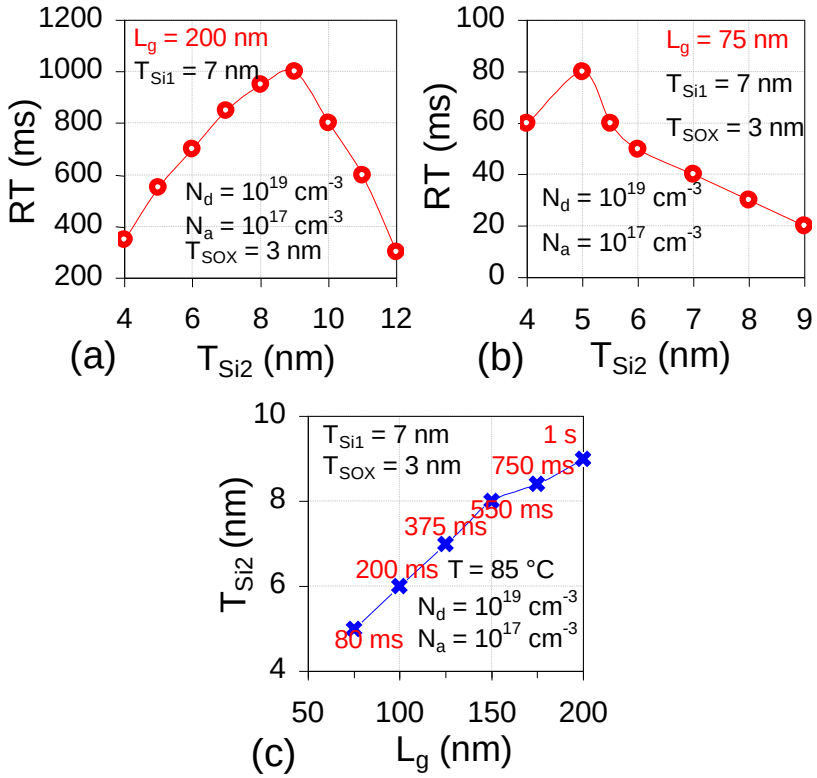

Fig. 3.11. Variation in *RT* with thickness of storage region (T_{Si2}) with L_g of (a) 200 nm and (b) 75 nm for $N_d = 10^{19}$ cm^{-3} and $N_a = 10^{17}$ cm^{-3} at 85 °C. (c) Optimal T_{Si2} for maximum *RT* with variation in L_g at 85 °C.

This is evident from that Figs. 3.11(a) and (b) which show the variation in *RT* with T_{Si2} for a longer gate length of 200 nm and 75 nm, respectively. Shorter gate length (75 nm) shows more SCEs (Fig. 3.9(a)), and thus, requires thinner storage region (T_{Si2} = 5 nm) as compared to a longer gate length that shows maximum retention at T_{Si2} = 9 nm. The gate length scaling necessitates the use of thinner film, corresponding to the storage region that suppresses SCEs, and thus, could improve retention. Fig. 3.11(c) showcases the optimal thickness of storage region with respect to each L_g to achieve maximum *RT* (> 64 ms) [22]. *RT* achieved for L_g of 200 nm is ~1 s with T_{Si2} of 9 nm while for shorter L_g of 75 nm, *RT* is ~80 ms with T_{Si2} of 5 nm at 85 °C. Figs. 3.12(a)-(c) shows the 2-D contour plot of hole concentration (n_h) during Hold '0' and Figs. 3.12(d)-(f) show hole concentration for Hold '1' for different storage thickness (7 nm, 9 nm, and 11 nm). The figures confirm higher generation of holes for thinner silicon film and more hole recombination for thicker T_{Si2}.

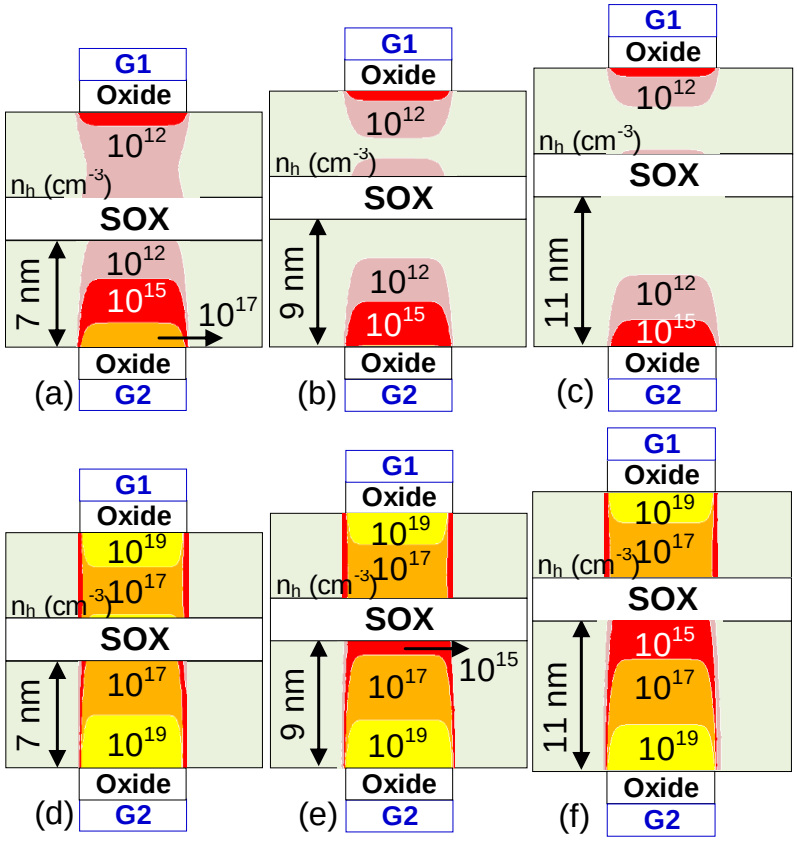

Fig. 3.12. Contour plot showing the hole concentration (n_h) for different T_{Si2} of 7 nm, 9 nm, and 11 nm during ((a)-(c)) for Hold '0' and ((d)-(f)) for Hold '1' with T_{Si1} = 7 nm, T_{SOX} = 3 nm and gate length of 200 nm at V_{G2_H} = -0.2 V.

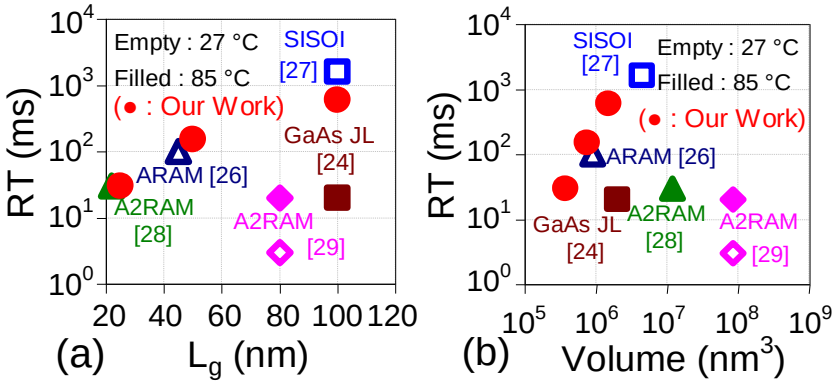

Fig. 3.13. Comparison of *RT* with published experimental and simulation results with (a) gate length and (b) volume ($L_g \times T_{Si} \times W_{Si}$). In our work, $T_{Si} = T_{Si1} + T_{Si2} + T_{SOX}$, where $T_{Si1} = 7$ nm, $T_{Si2} = 5$ nm, and $T_{SOX} = 3$ nm.

Fig. 3.13 compares the results of the proposed SJL based 1T-DRAM with published results of JL transistor [24], and other topologies having separate conduction and storage regions [26]–[28]. Filled and empty symbols show the results at 85 °C and 27 °C, respectively. Fig. 3.13(a) shows SJL attains a *RT* ~30 times higher compared to GaAs JL based 1T-DRAM [24] with same gate length and doping (N_d) of 5×10^{18} cm^{-3} at 85 °C. The enhanced *RT* is due to the separation of conduction and storage regions through the oxide layer. Comparing with A-RAM structure [26] in sub-50 nm regime (at 27 °C), SJL based 1T-DRAM attains improved *RT* of 150 ms at 85 °C due to the segregation of holes from the heavily doped S/D regions.

The proposed SJL architecture shows a better performance with an oversized back gate as it attains *RT* of ~30 ms for gate length of 25 nm at 85 °C, which is comparable with that achieved through A2RAM for a gate length of 22 nm [28]. The work demonstrates the impact of each dimension individually. However, practical approach requires a composite metric to evaluate the *RT* with respect to the total volume occupied by the device that defines the memory density. Therefore, for real-time application volumetric analysis ($L_g \times T_{Si} \times W_{Si}$) is beneficial, and thus, the retention characteristics have been evaluated in similar architectures [26]–[28] as a function of volume in Fig. 3.13(b), SJL based 1T-DRAM exhibits better performance compared with similar topologies due to thinner total film thickness ($T_{Si} = T_{Si1} + T_{SOX} + T_{Si2}$). In terms of volumetric analysis, SJL attains higher *RT* at the same volume as compared to previous works [24], [26]–[28],

which highlights the usefulness of the proposed concept to work at reduced volume.

3.4 Conclusion

The work shows an enhanced *RT* for 1T-DRAM with vertically stacked *n*-Oxide-*p* JL transistor. In comparison to conventional JL1T-DRAM, *n*-Oxide-*p* SJL based 1T-DRAM achieves ~10^3 times higher *RT* at 85 °C for a gate length of 200 nm. Results demonstrate the advantage achieved by physically decoupling the conduction and storage regions through an oxide, while maintaining the electrostatic coupling between them, which regulates the potential depth and retention. Analysis demonstrates the feasibility of the proposed topology as DRAM through the optimization of device parameters. A maximum *RT* of ~2.5 s is achieved for N_d of 5×10^{18} cm^{-3} and ~1 s for N_d of 10^{19} cm^{-3} with L_g = 200 nm and N_a of 10^{17} cm^{-3} at 85 °C. The individual effect of the thickness of separation oxide and storage region demonstrates the utility of an optimal T_{SOX} = 3 nm, T_{Si2} = 9 nm for L_g = 200 nm and T_{Si2} = 5 nm for L_g = 75 nm for higher *RT*. Further, evaluation at shorter gate length demonstrates the potential of an oversized back gate to enhance retention characteristics. The work showcases opportunities to achieve high retention in heavily doped structure through device engineering.

3.5 References

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Chapter 4

Shell-Doped Architecture for Capacitorless DRAM

4.1 Introduction

Over the past 50 years, the semiconductor industry has been the key enabler in the advancement of electronics [1]–[4]. Continuously shrinking the size of the 1T-1C DRAM faces the problem associated with charge retention and integration of external capacitor [5]–[10]. Floating Body Effects (FBEs) in SOI MOSFETs highlight a possible solution to remove the capacitor and retain the charges in the floating body [5]–[10]. JL devices have shown to exhibit dynamic FBEs at lower drain bias as compared to conventional IM transistors [11]. However, the higher doping in JL architecture results in lower carrier lifetime and a shallower potential well, which limits the retention [8]–[10].

In the previous chapter, body partitioning through a separation oxide shows a possible solution to achieve high *RT* in heavily doped JL DRAM [12], However, the separation of storage region from the conduction region through an oxide material, also reduces the probability of tunneling during Write '1' operation and requires more time to perform Write '1' operation. Another issue with SJL based 1T-DRAM is that it requires an oversized back gate to maximize storage area for charge retention at shorter gate lengths. These problems can be overcome with Shell-Doped (SD) architecture, which was originally proposed to limit SCEs [13]–[20]. In SD topology, heavily doped region (Shell) from source to drain region is partitioned through an intrinsic silicon film (Core), creating vertical layers of n^{++}-n^{+}-n^{++}, n^{+}-i-n^{+} and n^{++}-n^{+}-n^{++} regions in the silicon film [13]–[18]. Limiting the heavily doped (top and bottom) regions to few nanometers of the silicon surface [13]–[15], [21] is practically feasible through monolayer doping (MLD), and combination of microwave annealing (MWA) and CO_2 laser spike annealing (COLSA) as demonstrated in [13]–[15], [21].

In this chapter, we explore the utility of SD JL architecture as 1T-DRAM. The advantage in terms of high *RT* in SD topology is due to enhanced depletion of electrons that facilitates a deeper potential well for charge storage and reduces the diffusion and recombination of generated holes [9], [22]. The work also investigates the dependence of shell thickness (T_{Shell}) and doping (N_d) on physical mechanisms associated with *RT* and *SM*. Additionally, the impact of gate length scalability and high temperature on *RT* is shown. Results highlight the possibility of achieving enhanced *RT* in SD JL devices at lower gate lengths through appropriate selection of device parameters and optimization.

4.2 Device description and simulation

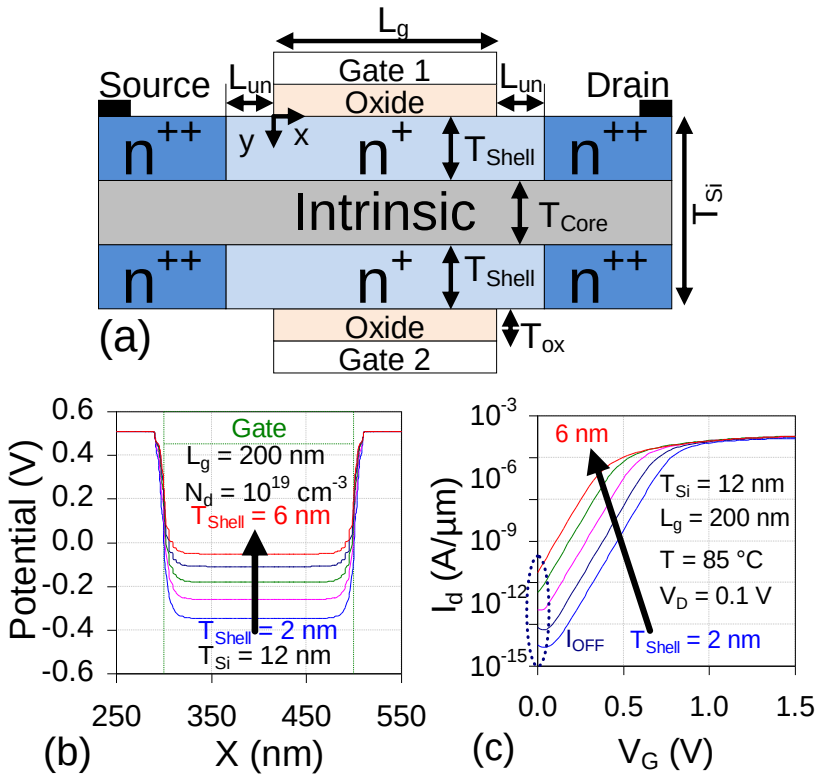

Fig. 4.1. (a) Schematic diagram of SD JL MOSFET. (b) Variation in electrostatic potential profile with different shell thickness for SD JL at zero bias with L_g of 200 nm. (c) I_d-V_G with different T_{Shell} for T_{Si} of 12 nm and L_g of 200 nm at drain voltage (V_D) of 0.1 V and 85 °C. Cutlines are taken 1 nm above the back gate oxide at zero bias condition along the *x*-direction in Fig. 4.1(c).

In order to validate the models in ATLAS simulation tool [23] that captures essential aspects of SD JL architecture, I_d –V_G characteristics of a tri-gate SD JL

transistor have been compared with experimental data [13], as shown in Figs. 2.1(e) and (f). The physical models used for DRAM operation are BTBT and Impact Ionization model along with doping and temperature dependent SRH models, Lombardi mobility model and bandgap narrowing. The usefulness of SD architecture for 1T-DRAM is analyzed through DG SD JL transistor. Fig. 4.1(a) shows the schematic diagram SD JL architectures. The device parameters used for SD as 1T DRAM are shown in Table 4.1.

Table 4.1 Device parameters of SD JL for 1T-DRAM

Parameters	***Values***
Gate length (L_g)	200 nm - 10 nm
Width (W_{Si})	1 μm
Underlap length (L_{un})	10 nm
Shell thickness (T_{Shell})	2 nm – 6 nm
Core thickness (T_{Core})	0 nm – 8 nm
Film thickness ($T_{Si} = T_{Core} + 2T_{Shell}$)	12 nm
Oxide thickness (T_{ox})	1 nm (SiO_2)
Front gate workfunction (φ_{m1})	4.8 eV - 5.2 eV
Back gate workfunction (φ_{m2})	4.8 eV - 5.2 eV
Source/Drain doping ($N_{d(S/D)}$)	10^{20} cm^{-3}
Shell doping (n-type)	10^{18} cm^{-3} - 10^{19} cm^{-3}
Core doping (p-type)	10^{15} cm^{-3}

Figs. 4.1(b) and (c) show the advantage of using SD architecture with a deeper potential well formation over the conventional DG JL transistor for the same film thickness (T_{si}) and gate workfunction (φ_m). The advantage of SD JL over the conventional JL is shown in Fig. 4.1(b) with a variation in potential profile of SD JL (T_{Shell} = 2 to 5 nm) and conventional DG JL (T_{Shell} = 6 nm) for the same device dimensions along the x-direction at zero bias condition. SD JL topology achieves a profound potential well due to the depletion of greater number of electrons from the silicon film. Fig. 4.1(c) shows the I_d-V_G of SD transistor with T_{Shell} varying from 2 nm to 6 nm for L_g = 200 nm at drain voltage (V_D) of 0.1 V. It is evident from Fig. 4.1(c) that off-current ($I_{OFF} = I_d$ @ V_G = 0 V) decreases with a reduction

in T_{Shell} due to a deeper potential well (higher barrier for electrons). The decrease in I_{OFF} can be associated with enhanced *RT* due to an increase in the hole barrier that decreases the recombination rate [9], [22]. Thus, SD JL topology, benefited with a deeper potential, is helpful in improving the DRAM for standalone as well as embedded DRAM compared to a conventional JL (T_{Shell} = 6 nm (T_{Si} = 12 nm)) and SJL device.

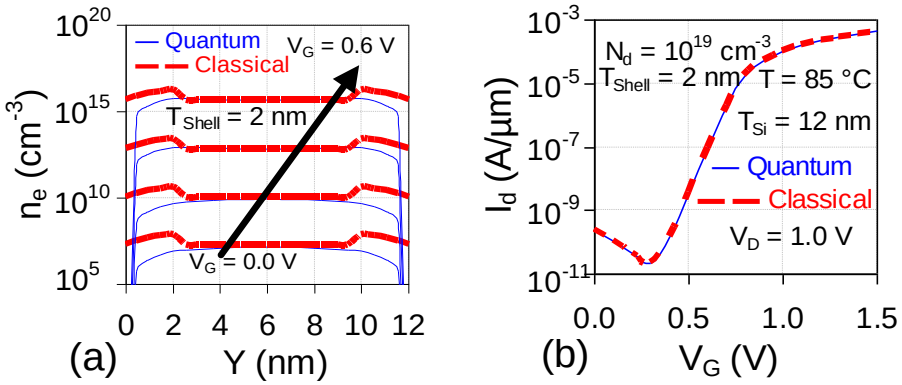

Fig. 4.2. Comparison of quantum (density gradient) and classical models in terms of (a) electron concentration (n_e) along the *y*-direction at different gate voltages, and (b) I_d-V_G characteristics obtained through classical and quantum simulations for L_g of 200 nm SD JL architecture at 85 °C.

The downscaling of device dimensions can lead to quantum confinement effects (QCEs) [17], [24]. Therefore, in analysis for thinner T_{Shell} and at shorter L_g, Schrödinger equation was consistently solved with the Poisson's equation with density gradient model as in [17], [24]. Fig. 4.2 shows the comparison of results obtained by quantum (density gradient model [17], [24]) and classical models. Fig. 4.2(a) shows the variation of electron concentration (n_e) along the silicon film (*y*-direction) for N_d = 10^{19} cm^{-3} as a function of gate bias (V_G). n_e (for both approaches) is nearly same at the center of the film, while it approaches very to low values at the surface in quantum model due to effective potential [24]–[27]. I_d from classical and quantum simulations is nearly same (Fig. 4.2(b)), thereby confirming that energy quantization is not significant [24], and the same is not likely to affect DRAM performance [28]. Also, T_{Si} used in the work is higher than the minimum acceptable limit (~3 nm) for memory applications [28].

4.3 Shell-Doped as 1T-DRAM

Working operation of SD JL architecture as 1T-DRAM with optimized biasing and timing schemes is shown in Table 4.2. The barrier between source and channel at the front gate is modulated through holes stored at the back surface. The storage of holes at the back surface of the film estimates the DRAM metrics, namely, sense margin and retention time, which can be evaluated through the state currents (I_1 and I_0) [29], [30].

Table 4.2 Biasing and timing for operation of SD JL based 1T-DRAM

Operation	***V_{G1} (V)***	***V_{G2} (V)***	***V_S (V)***	***V_D (V)***	***Time (ns)***
Write ‘1’	1.0	-1.6	0.0	1.5	50
Hold	0.0	-0.1	0.1	0.1	--
Read	1.0	0.1	0.0	0.1	100
Write ‘0’	1.5	1.5	0.0	0.0	50

Fig. 4.3(a) shows the transient analysis, which outlines different operations. DRAM consists of two states, state ‘1’ (characterized by Write ‘1’, Hold ‘1’ and Read ‘1’) and state ‘0’ (represented through Write ‘0’, Hold ‘0’ and Read ‘0’) as shown in Fig. 4.3(a). Fig. 4.3(b) shows the energy band diagram of SD JL at zero bias condition (V_S = V_D = V_{G1} = V_{G2} = 0.0 V) and during Write ‘1’ operation (V_{G1_W1} = 1.0, V_{D_W1} = 1.5 and V_{G2_W1} = -1.6 V). The energy band diagram is extracted at 1 nm above of the back gate oxide. As demonstrated in [31], [32], in a JL transistor, BTBT occurs by applying a negative bias at back gate and positive at drain. This reduces the tunneling width at Gate2 and drain junction, and electrons can easily tunnel from valence band (VB) of the channel to conduction band (CB) of the drain. Fig. 4.3(c) shows the contour plot of BTBT rate which confirms Write ‘1’ operation is performed through BTBT at the gate and drain junction. The maximum BTBT rate occurs at Gate2 and drain junction due to high electric field at the drain region. This results in an increase in excess hole concentration at the back surface of the silicon film, which shows a higher current (state ‘1’). The dominant degradation in DRAM happens due to the interface state generation by impact ionization for Write ‘1’ [33]. In this work, BTBT has been primarily utilized to perform the Write operation, which is more reliable and low

power consumption as compared to impact ionization [34], [35]. The Write operation is performed with lower drain bias 1.5 V and back gate bias of -1.6 V, and read operation is performed at drain bias of 0.1 V. Hence, endurance is not expected to be an issue in a SD JL.

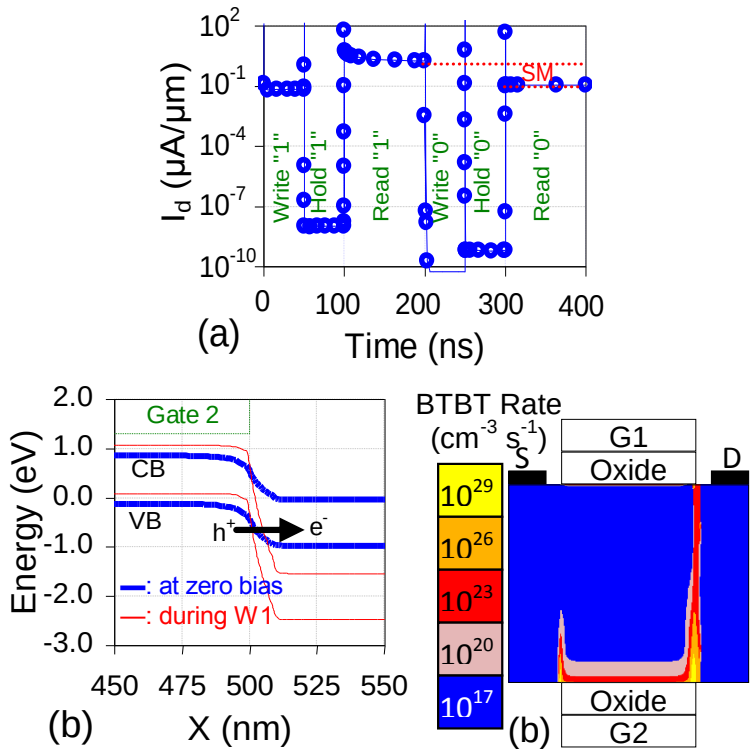

Fig. 4.3. (a) Transient analysis of SD architecture for T_{Shell} of 2 nm with L_g of 200 nm at 85 °C. (b) Variation in energy band diagram of SD JL during initial condition (V_S = V_D = V_{G1} = V_{G2} = 0.0 V) and Write '1' operation (V_{G1_W1} = 1.0, V_{D_W1} = 1.5 and V_{G2_W1} = -1.6 V) for shell doping of 10^{19} cm^{-3} with gate length of 200 nm and T_{Shell} of 2 nm. (c) Contour plot of BTBT rate during Write '1' operation. The maximum tunneling rate is observed at Gate2 and drain junction due to high electric field. CB and VB indicate conduction and valence band energy, respectively.

Removal of holes (Write '0' operation) from the back surface is performed through a forward bias mechanism by applying a positive bias at back and front gates (V_{G1_W0} = V_{G2_W0} = 1.5 V). A applying a positive bias at the gate terminal increase the potential during Write '0' and allows the stored hole to recombine with heavily doped source and drain electrons. Absence of holes from the film increases the barrier for electrons during read operation, and results into a lower

current (state '0'). In order to estimate the *SM*, read operation is performed with front gate (V_{G1_R}) of 1 V, back gate (V_{G2_R}) and low drain bias (V_{D_R}) of 0.1 V. The generation and recombination of holes during Hold '0' and Hold '1' operation, respectively, in the device is controlled through with optimized Source/Drain (S/D) voltage (V_{S/D_H}) of 0.1 V and back gate bias (V_{G2_H}) of -0.1 V.

4.4 Effect of device parameters on DRAM metrics

4.4.1 Impact of shell thickness (T_{Shell})

Fig. 4.4 shows the 2D contour plots of electron concentration (n_e) at zero bias condition for different combinations of T_{Shell} and T_{Core}. The depletion of electrons from the film is significant in a thinner shell due to the increased impact of φ_{m1} = φ_{m2} = φ_m. Fig. 4.4(a) shows that a T_{Shell} of 2 nm has minimum n_e in the silicon film compared to others (Fig. 4.4(b)-(d)).

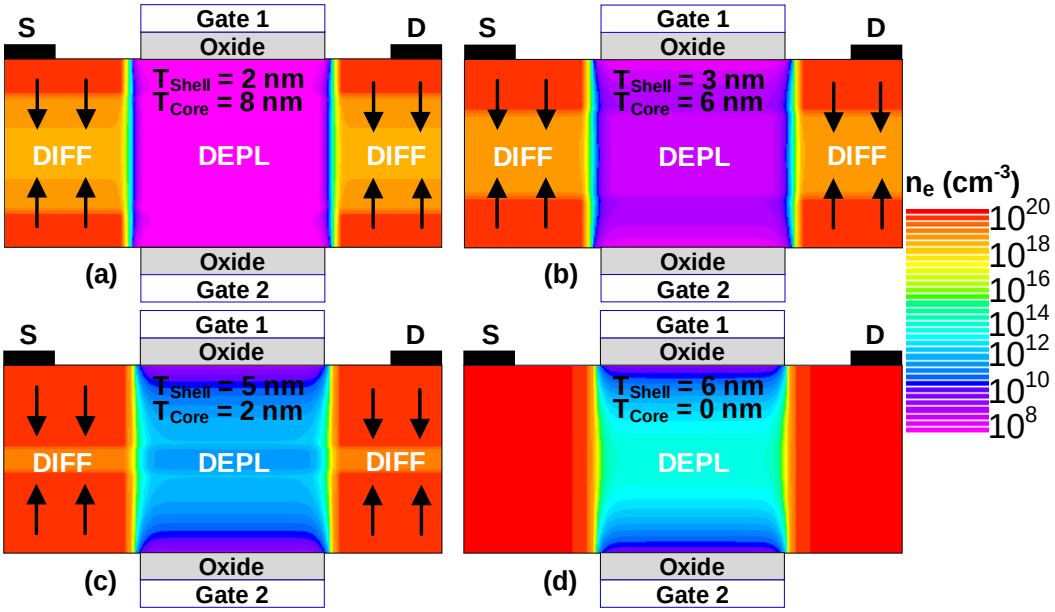

Fig. 4.4. 2D contour plots of electron concentration (n_e) for T_{Si} of 12 and L_g of 200 nm with (a) T_{Shell} = 2 nm, (b) T_{Shell} = 3 nm, (c) T_{Shell} = 5 nm, and (d) T_{Shell} = 6 nm at zero bias condition. DEPL and DIFF indicate depletion and diffusion of electrons, respectively.

An increase in T_{Shell} (for a constant T_{Si}) transforms a SD design into a conventional JL transistor as shown in Fig. 4.5(d) (T_{Shell} = 6 nm). The depletion of

electrons from a thinner T_{Shell} results in a deeper potential well underneath the gate. The presence of an undoped core between heavily doped n^{++} S/D regions results in the diffusion of electron towards the core. A higher diffusion area indicates a thicker core (T_{Core} = 8 nm (Fig. 4.5(a)), and thus, a region with lower potential as compared to a conventional JL transistor (no diffusion area in Fig. 4.4(d)). As observed in Figs. 4.4(a)-(d), a greater variation in n_e between S/D and core regions indicates enhanced tunneling, and thus, more hole generation during Hold '0'. Also, the potential depth (Fig. 4.1(b)) at the back surface decreases, showing a lower barrier for hole recombination, and thus, degrading state '1'. Therefore, the combined effects of electron depletion and their diffusion determine the DRAM performance.

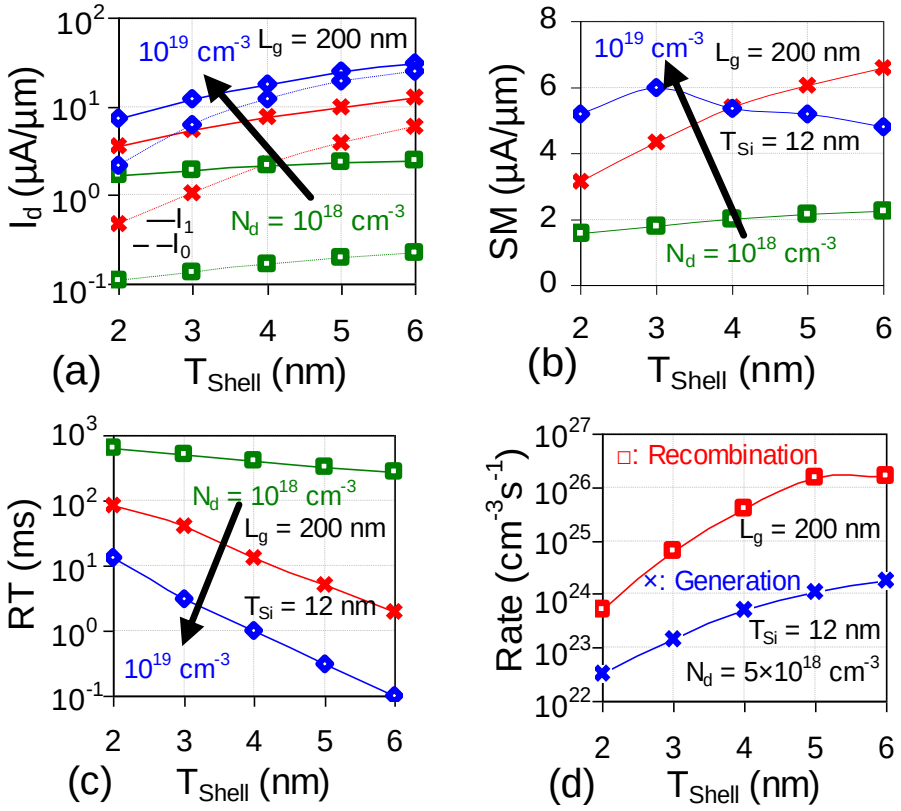

Fig. 4.5. Variation in (a) state currents (I_1 and I_0), (b) *SM* and (c) *RT* with T_{Shell} for N_d of 10^{18} cm^{-3} to 10^{19} cm^{-3}. (d) Dependence of generation and recombination rates with T_{Shell} for N_d of 5×10^{18} cm^{-3} and L_g of 200 nm at 85 °C. Cutlines are taken 1 nm above the back gate oxide for Fig. 4.5(d).

Fig. 4.5(a) shows the variation of state currents (I_1 and I_0) with T_{Shell} at L_g of 200 nm. I_1 and I_0 increase with T_{Shell} and N_d due to lesser extent of diffusion of

electrons from heavily doped S/D to undoped core and the reduction in depletion of electrons from the film underneath the gate, respectively. This improves *SM* of DRAM (Fig. 4.5(b)). However, for $N_d = 10^{19}$ cm^{-3}, *SM* decreases from ~6 μA/μm for T_{Shell} = 3 nm to ~4.5 μA/μm for T_{Shell} = 6 nm. The lesser depletion of electrons increases the state '0' current due to the higher potential in the film during Read '0'. The increase in state '0' current with T_{Shell} and N_d reduces *SM* as well as the current ratio (I_1/I_0). To facilitate an even deeper potential well, and enhance the carrier lifetime, a lower doping of the shell can be utilized. Fig. 4.5(c) shows the variation of *RT* with T_{Shell} for N_d with L_g = 200 nm. An increase in N_d and T_{Shell} results in the reduction of *RT* due to a shallower potential and lower carrier lifetime. The maximum *RT* achieved at $N_d = 10^{19}$ cm^{-3} is ~13 ms at 85 °C with L_g = 200 nm. The degradation of *RT* with T_{Shell} can be explained through the variation in generation and recombination rates during Hold (Fig. 4.5(d)) for N_d of 5×10^{18} cm^{-3}. The recombination rate is higher as compared to generation rate due to a lower carrier lifetime [9]. An increase in T_{Shell} increases the sharing of gated region (reduction in diffusion area underneath S/D) with heavily doped S/D regions (Fig. 4.4), which enhances hole generation during Hold '0' and recombination/diffusion of holes during Hold '1' due to barrier lowering (higher I_{OFF} in Fig. 4.1(c)). Therefore, maximum *RT* is achieved with thinner T_{Shell}.

Other than *SM* and *RT*, speed and power consumption during Write '1' is also dependent on T_{Shell}. The hole generation during Write '1' is influenced by Write Time and voltage. Write Time (or speed) is estimated when *SM* attains a constant value for a fixed drain bias (Fig. 4.6(a)) [7], [9]. An increase in Write Time or voltage increases the generation of holes during Write '1' operation but the accumulation of holes in the potential well during read is constant for fixed read bias, hence, state '1' and *SM* is constant [7], [9]. The minimum time required for performing Write '1' operation for shell doping of 10^{19} cm^{-3} with T_{Shell} of 2 nm and L_g of 200 nm at 85 °C is 20 ns. Fig. 4.6(b) shows the impact of T_{Shell} on Write Time to perform Write '1' operation for a fixed write drain voltage (V_{D_W1}) of 1.5 V with L_g of 200 nm at 85 °C. An increase in T_{Shell} results in the architecture becoming a conventional JL transistor (without any undoped core), which reduces *RT* but enhances the speed [8], [9].

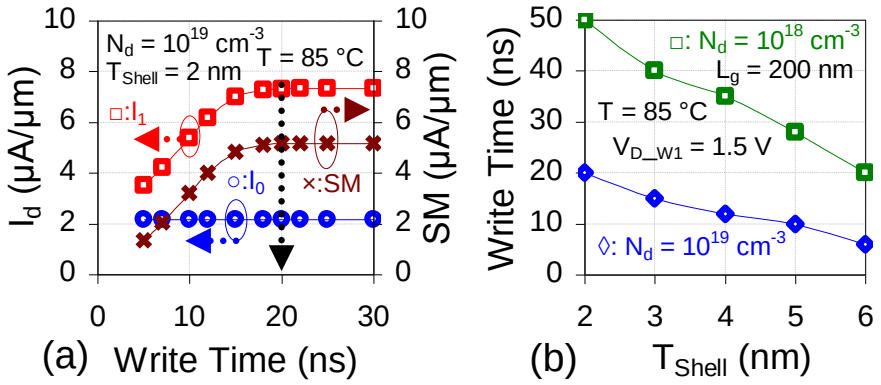

Fig. 4.6. (a) Variation in state currents and *SM* with Write Time for a fixed write drain bias of 1.5 V for N_d of 10^{19} cm^{-3} with L_g = 200 nm and T_{Shell} = 2 nm at 85 °C. (b) Variation in Write Time with T_{Shell} for N_d of 10^{18} cm^{-3} and 10^{19} cm^{-3} with L_g of 200 nm at 85 °C.

4.4.2 Impact of gate workfunction (φ_m)

The depth of potential well and carrier lifetime are the two main factors, which control the generation and recombination of holes in the silicon film, and thereby modulate DRAM metrics [9], [22], [30], [36], [37]. In JL 1T-DRAM, the potential depth is mainly governed through device parameters (gate workfunction, channel doping, film thickness, and oxide thickness). Selecting a higher gate workfunction, for a fixed set of device parameters, depletes more number of electrons that results in to a deeper potential well for charge storage. Fig. 4.7(a) shows the impact of gate workfunction (φ_m) on potential profile of SD JL along the *x*-direction for shell doping of 10^{18} cm^{-3} with gate length (L_g) of 200 nm and shell thickness (T_{Shell}) of 2 nm. An increase in the potential depth corresponds to an increase in barrier at source, which reduces the state currents (I_1 and I_0) with gate workfunction (Fig. 4.7(b)). *SM* of memory increases with reduction in gate workfunction up to 5.0 eV, and *SM* starts to decrease for φ_m > 5.0 eV due to prominent change in state '0' (higher potential during Read '0'). Fig. 4.7(c) shows that an increase in gate workfunction leads to a deeper potential well that sustains charges for a longer duration and enhance *RT*. A maximum *RT* of ~630 ms is achieved for φ_m = 5.2 eV and decreases to ~5 ms for φ_m = 4.8 eV with gate length of 200 nm and shell thickness of 2 nm at 85 °C. Thus, the analysis shows that workfunction is most important parameters to achieve high retention time.

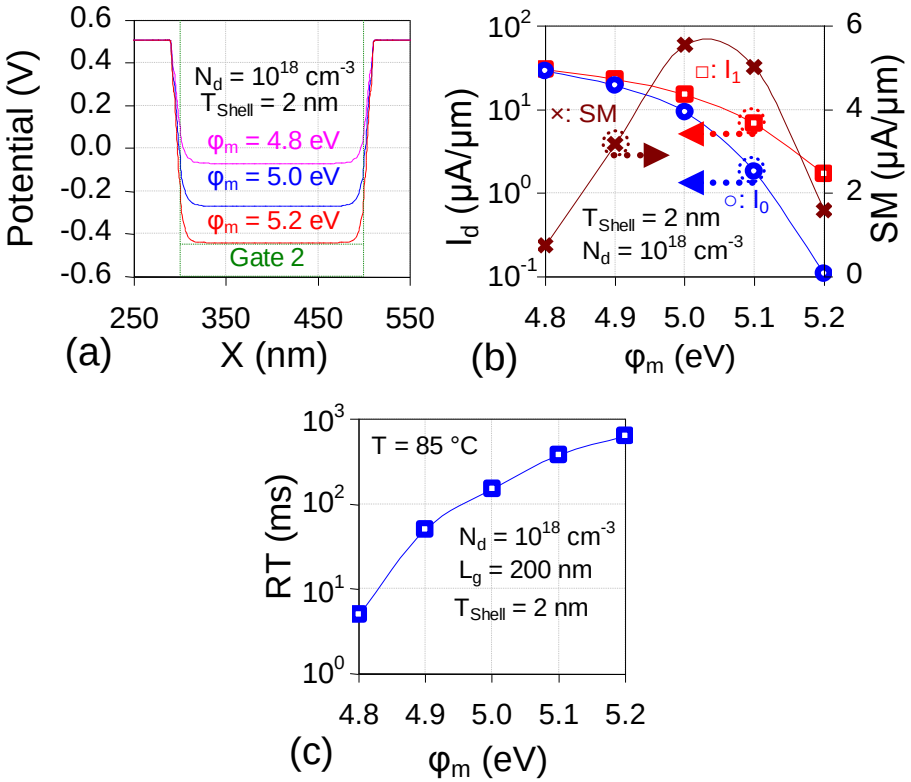

Fig. 4.7. (a) Variation in potential profile for different gate workfunctions (φ_m) along *x*-direction for shell doping (N_d) of 10^{18} cm^{-3} with gate length (L_g) of 200 nm and shell thickness (T_{shell}) of 2 nm. Variation in (b) state currents (I_1 and I_0), and *SM*, and (c) *RT* with gate workfunction for N_d = 10^{18} cm^{-3} with L_g of 200 nm and T_{shell} of 2 nm at 85 °C. Parameters are extracted at 1 nm above of the back gate oxide for extraction of potential profile.

4.4.3 Gate length (L_g) scaling

Downscaling the transistor degrades the performance of DRAM cells due to an increase in BTBT and SCEs [5], [28]. An underlap region is used to control BTBT as it increases the tunneling width as well as the storage region, which enhances *RT* of 1T-DRAM, and also shows improved scalability [7], [9]. Fig. 4.8(a) shows the variation in Conduction Band (CB) energy for different gate lengths at a constant underlap (10 nm) and N_d of 10^{18} cm^{-3}. Cutlines are taken at 1 nm above the back gate oxide along the *x*-direction at zero bias condition. The reduction in barrier height due to SCEs is observed for L_g < 15 nm suggesting an enhanced immunity of SD JL devices to SCEs [38].

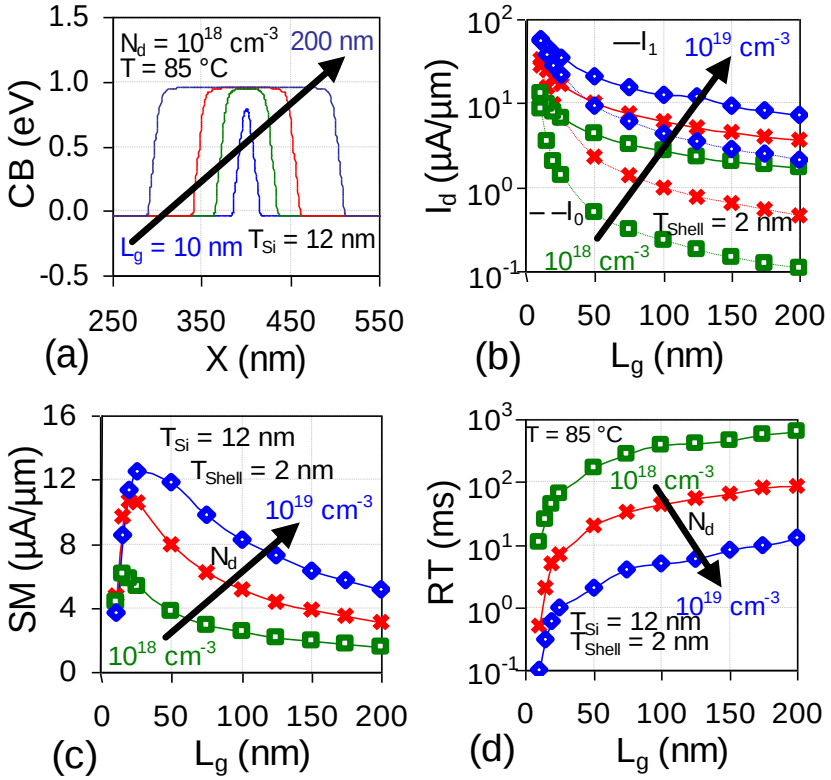

Fig. 4.8. (a) Variation in Conduction Band (CB) energy at y = 1 nm along x for N_d of 10^{18} cm^{-3}. Variation in (b) I_1 and I_0, (c) *SM* and (d) *RT* with L_g for N_d varying from 10^{18} cm^{-3} to 10^{19} cm^{-3} at 85 °C.

Fig. 4.8(b) shows the variation of I_1 and I_0 with L_g at T_{Shell} = 2 nm and 85 °C. The barrier between source and channel is lowered with an increasing N_d due to lesser depletion of electrons from the shell. Therefore, I_1 and I_0 increase with reduction in L_g and an increase in N_d. SD architecture with relatively lower shell doping (10^{18} cm^{-3}) shows less SCEs due to longer effective channel length (L_{eff}) [13], [38], which is evident from Fig. 4.8(c). *SM* of the memory decreases with L_g lowering from 25 nm, 20 nm and 15 nm for N_d of 10^{19} cm^{-3}, 5×10^{18} cm^{-3} and 10^{18} cm^{-3}, respectively, at 85 °C. The prominent change at shorter L_g is observed in state '0' current due to SCEs, (Fig. 4.8(b)), and thus, *SM* decreases. The dependence of *RT* on L_g and N_d is shown in Fig. 4.8(d). The maximum *RT* achieved at L_g of 200 nm are ~630 ms, ~85 ms and ~13 ms for a shell doping of 10^{18} cm^{-3}, 5×10^{18} cm^{-3} and 10^{19} cm^{-3} at 85 °C, respectively. The SD JL shows better scalability with *RT* of ~11 ms at a shorter L_g (= 10 nm) for N_d of 10^{18} cm^{-3}, and ~5 ms at L_g = 20 nm for N_d of 5×10^{18} cm^{-3}, both at 85 °C.

4.4.4 Temperature dependence

The use of DRAM at high temperatures [39] is limited by the reduction in *RT* of the memory due to thermal generation and recombination of carriers [7], [9], [40]. Fig. 4.9 shows the variation of state currents (Fig. 4.9(a)-(c)) and percentage change in *RT* (Fig. 4.9(d)) with temperature. Fig. 9(a) shows that state '1' has a longer retention at 27 °C, and is maintained with hold time at all values of N_d due to deeper potential well, facilitated by the SD architecture. However, state '0' reduces due to thermal generation and BTBT with hold time. The maximum *RT* attained is ~5.5 s, ~275 ms and ~16 ms for N_d of 10^{18} cm^{-3}, 5×10^{18} cm^{-3} and 10^{19} cm^{-3}, respectively, with L_g of 200 nm at 27 °C.

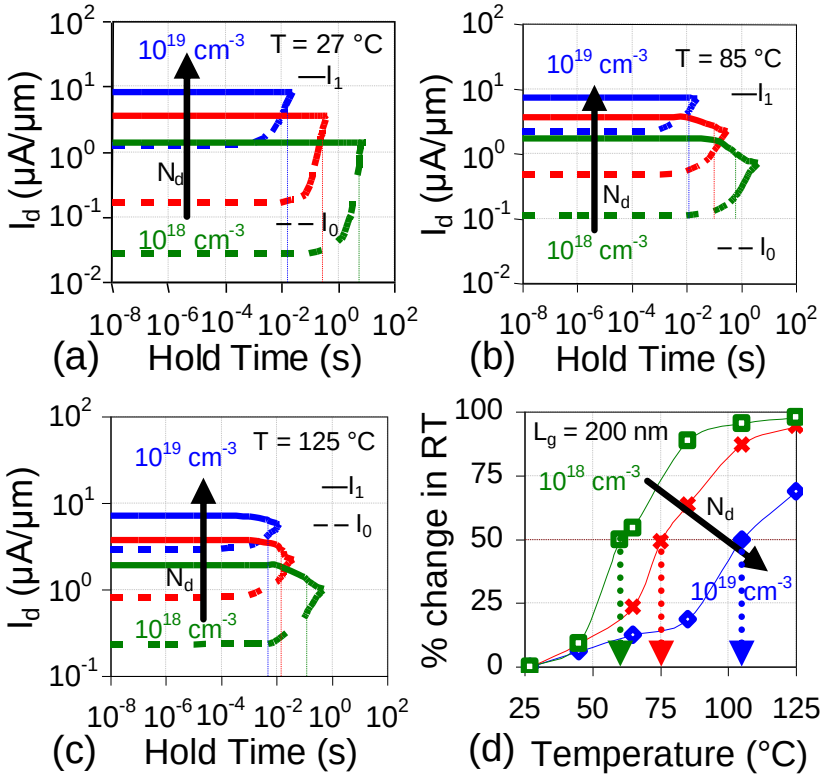

Fig. 4.9. Variation of state currents (I_1 and I_0) with hold time for different N_d at (a) 27 °C, (b) 85 °C and (c) 125 °C with T_{Shell} of 2 nm. (d) Percentage change in *RT* with temperature for different N_d with *RT* at 27 °C as the reference. The maximum *RT* for N_d of 10^{18} cm^{-3}, 5×10^{18} cm^{-3} and 10^{19} cm^{-3} is ~5.5 s, ~630 ms and ~16 ms at 27 °C, respectively.

Table 4.3 Retention Time and Reduction Ration in *RT* (RR_{RT}) with temperature. RR_{RT} is estimated with reference to *RT* at 27 °C.

N_d (cm^{-3})		45 °C	65 °C	85 °C	105 °C	125°C
10^{18}	*RT* (ms)	5000	2500	630	250	120
	RR_{RT}	9.1%	54.5%	88.5%	95.4%	97.8%
5×10^{18}	*RT* (ms)	250	210	85	35	15
	RR_{RT}	9.1%	23.6%	69.1%	87.3%	94.5%
10^{19}	*RT* (ms)	15	14	13	8	5
	RR_{RT}	6.2%	12.5%	18.7%	50%	68.7%

The advantage of a higher N_d in SD JL is reflected through the evaluation of Reduction Ratio of *RT* (RR_{RT}). Table 4.3 shows the reduced degree of change in *RT* with temperature for 10^{19} cm^{-3} as compared to a lower shell doping (10^{18} cm^{-3}). RR_{RT} is estimated using the reference value at 27 °C for each N_d. The degradation of RR_{RT} with temperature can be understood through Fig. 4.9(a)-(c). Fig. 4.9(b) shows the degradation in *RT* for N_d of 10^{19} cm^{-3} is due to the generation of holes (state '0' is increasing) while state '1' remains constant. However, for N_d of 10^{18} cm^{-3} and 5×10^{18} cm^{-3}, both generation of holes (state '0') and recombination of holes (state '1') contribute towards the reduction in *RT*. Fig. 4.9(d) shows percentage change in *RT* reaches to ~50% at 65 °C for 10^{18} cm^{-3}, at ~75 °C for 5×10^{18} cm^{-3}, and at 105 °C for 10^{19} cm^{-3} with L_g of 200 nm and T_{Shell} of 2 nm. Therefore, the degradation of RR_{RT} is higher for lower N_d. The advantage of higher N_d in JL in terms of RR_{RT} is due to less variation in carrier lifetime with temperature [41], and thus, the dominance of doping over temperature reduces RR_{RT} with increase in doping. The maximum doping dependent carrier lifetime values for 5×10^{18} cm^{-3} and 10^{19} cm^{-3} are 1 ns and 0.5 ns, respectively, at 27 °C, and which reduces to 0.64 ns and 0.32 ns at 125 °C, respectively, [41]. *RT* is severely degraded as a high value of 95% is achieved for RR_{RT} at 105 °C for N_d = 10^{18} cm^{-3}. At the same temperature, a relatively lower value of RR_{RT} (50%) reflects less degradation in *RT*. At 125 °C, only ~69% degradation in *RT* is observed for N_d = 10^{19} cm^{-3} due to the relatively lower variation in carrier lifetime with temperature. A *RT* of ~120 ms (> 64 ms at 85 °C as specified by ITRS [42]) is achieved for L_g of 200 nm at 125 °C.

4.4.5 Sensitivity assessment

Fig. 4.10(a) shows the sensitivity analysis through percentage change in *RT* with the corresponding change in T_{Shell} for two different N_d values in SD JL transistor. The reference device is chosen to be with T_{Shell} = 2 nm. It is evident from Fig. 4.10(a) that the percentage change in *RT* with a change in T_{Shell} is lesser for $N_d \leq 5\times10^{18}$ cm^{-3} due to a negligible change in potential depth (Fig. 4.10(b) for N_d = 10^{18} cm^{-3}). However, for $N_d > 5\times10^{18}$ cm^{-3}, the percentage change in *RT* is significant due to a prominent change in potential depth (Fig. 4.10(c) for $N_d = 10^{19}$ cm^{-3}). An increase in T_{Shell} (1.8 nm to 2.2 nm) shows a greater influence on *RT* rather than in its reduction due to an increase in the relative separation between the two adjacent potential levels. *RT* does not change much (< 10%) if N_d is limited to 5×10^{18} cm^{-3}.

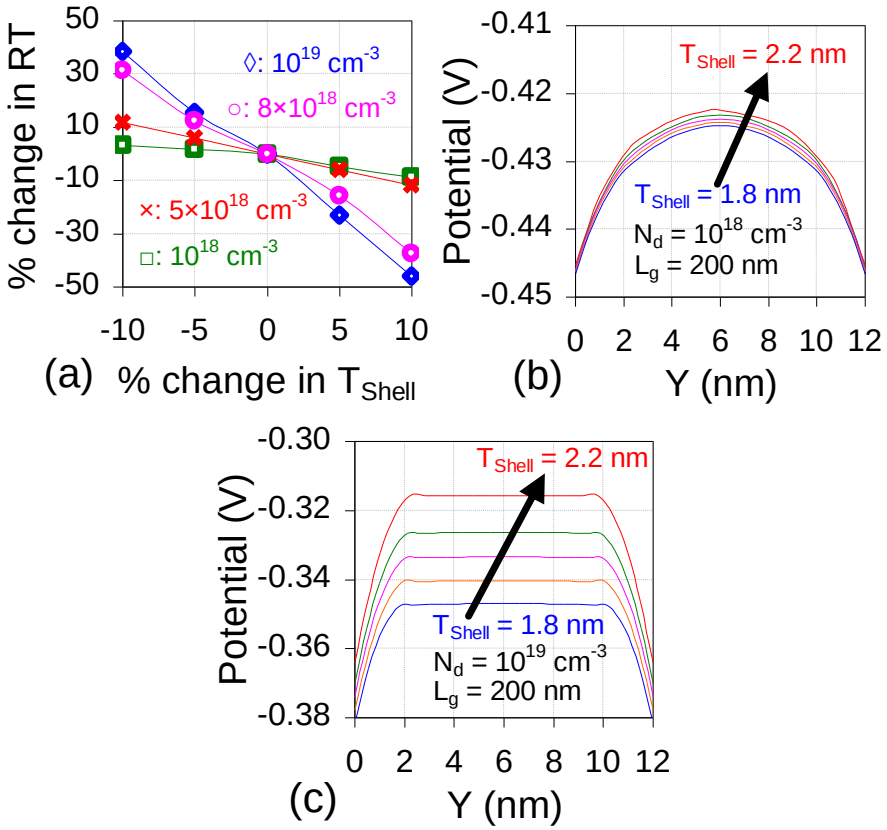

Fig. 4.10. (a) Variation in percentage change in *RT* with percentage change in T_{Shell} for different N_d with L_g of 200 nm at 85 °C. Variation in potential profile along the *y*-direction for N_d of (b) 10^{18} cm^{-3} and (c) 10^{19} cm^{-3}. Reference point is taken to be *RT* at T_{Shell} = 2 nm.

Experimental results [14] on SD JL transistor have shown the possibility of achieving a steepness of ~0.8 nm/dec. In order to understand the impact of the gradient of N_d, a Gaussian shell doping, as shown in Fig. 4.11(a), was considered in the analysis. An increase in the gradient increases the dopant concentration in the core, which results in a lesser depletion of electrons, and lower lifetime. As shown in Fig. 4.11(b), an idealized abrupt doping profile maintains an undoped core and exhibits a maximum *RT* as compared to a Gaussian profile with a realistic gradient. The maximum *RT* of ~630 ms and ~13 ms achieved for an abrupt doping profile with N_d = 10^{18} cm^{-3} and 10^{19} cm^{-3}, respectively, reduces to ~280 ms (56% reduction) and ~0.7 ms (95% reduction) with Gaussian doping profile of 2 nm/decade for same N_d values.

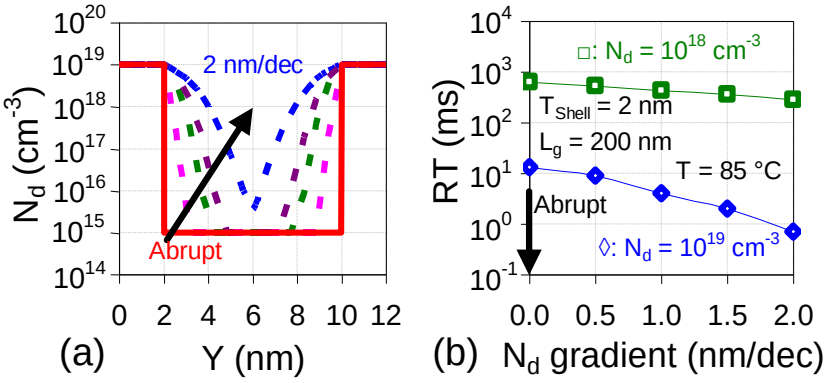

Fig. 4.11 (a) Variation in abrupt and Gaussian doping profile in SD JL. (b) Variation in *RT* with abrupt and with different doping gradient (0.5 nm/ decade to 2 nm/decade) in SD JL. Cutlines are taken at the center of gate along the *y*-direction for Fig. 4.11(a).

4.4.6 Assessment performance comparison of 1T-DRAM architectures

Fig. 4.12(a) compares *RT* of a SD JL DRAM with published results of other JL DRAM topologies [10], [12] at shorter gate lengths ($L_g \leq 50$ nm) and N_d = 5×10^{18} cm^{-3}. SD JL architecture achieves higher *RT* compared to vertically stacked *n*-oxide-*p* transistor [12] at $L_g \leq 25$ nm with same doping. However, for $L_g \geq 30$ nm vertically stacked *n*-oxide-*p* transistor with thicker T_{Si} achieves higher *RT* as compared to SD JL device due to separation of conduction and storage region through a separation oxide. On the other hand, for thicker film thickness at L_g of 25 nm, SD architecture achieves ~6.5 times higher *RT* compared to [9] with N_d =

10^{18} cm^{-3} at 85 °C due to the formation of a deeper potential well in SD architecture. GaAs based DRAM [10] with vertical structure attains lower *RT* due to lower carrier lifetime, but higher *SM* due to higher mobility and thicker film thickness compared to SD JL DRAM at 27 °C.

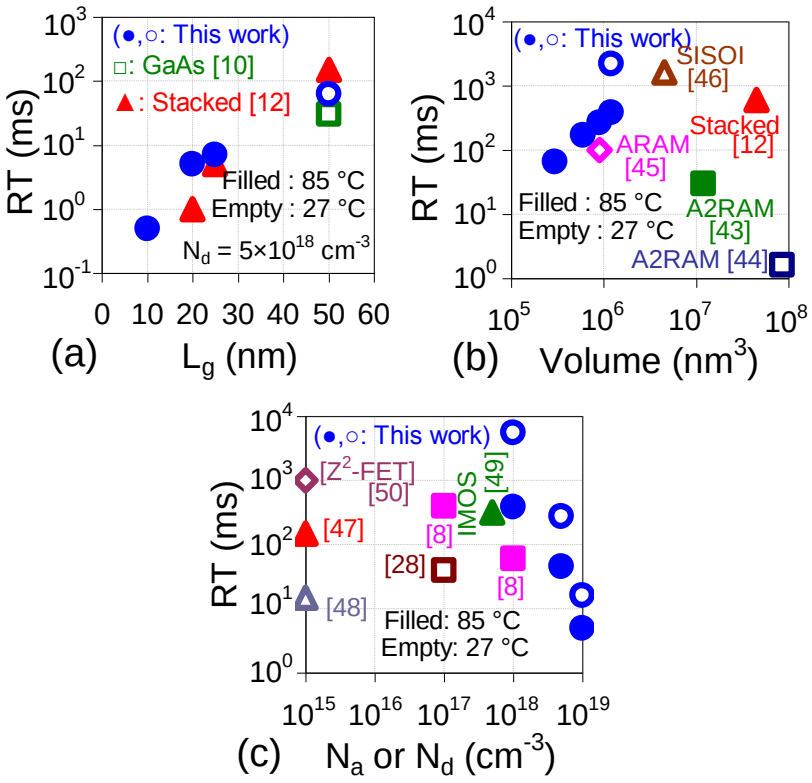

Fig. 4.12. Comparison of *RT* with published results of (a) Junctionless based DRAM for N_d of 5×10^{18} cm^{-3} with gate length, (b) devices with body partitioned for charge storage with volume and (c) Inversion Mode, Accumulation Mode, IMOS and Z^2-FET based DRAM with doping. Empty symbols indicate 27 °C while filled symbols reflect 85 °C.

Fig. 4.12(b) compares *RT* with devices where the conduction and storage are separated electrically [43], [44] and physically [12], [45], [46] at sub-100 nm gate lengths in terms of volumetric analysis. Volume of the device is calculated as in [9], [12] (*Volume* = L_g×T_{Si}×W_{Si}). In SD JL DRAM, the total film thickness is considered is 12 nm including 2 nm of shell thickness. In comparison to electrically separated (vertically *pn* junction underneath the gate) architectures (A2RAM [43], [44]), SD JL DRAM attains high *RT* with smaller volume. In A2RAM, the use of two heavily doped regions in the vertical direction (T_{Si} = 36

nm) and sharing of these regions with heavily doped S/D increases the generation and recombination rates compared to SD architecture, thus, lowering *RT*. Similarly, in comparison to SISOI (*RT* = ~1.6 s) [46], SD JL DRAM achieves a high *RT* (~2.2 s) at 27 °C with same gate length of 100 nm and smaller volume. The partial separation in SISOI increases the recombination of generated holes, which degrades *RT*. In terms of L_g, SD JL DRAM shows comparable results with architectures, where conduction and storage region are physically separated through an oxide (ARAM at 27 °C with L_g of 45 nm [45], SISOI at 27 °C with L_g of 100 nm [46] and vertically stacked at 85 °C with L_g of 100 nm [12]). SD JL DRAM showcases a remarkable improvement compared to devices with body partitioning in sub-100 nm regime.

Fig. 4.12(c) shows the comparison of *RT* with published Inversion Mode (IM) transistors [28], [47], [48], Accumulation Mode (AM) [9], IMOS [49] and Z^2-FET [50] based DRAM results at 27 °C and 85 °C. SD JL devices with a higher N_d (5×10^{18} cm^{-3} and 10^{19} cm^{-3}, and L_g of 100 nm) achieves a comparable retention with respect to IM devices [28], [47], [48] (with lower N_d and at shorter $L_g \leq 75$ nm) due to thinner film and suppressed SCEs. In comparison to AM MOSFET (*RT* ~400 ms and 60 ms at $N_d = 10^{17}$ cm^{-3} and 10^{18} cm^{-3}, respectively, at L_g = 100 nm) [9], SD JL transistor achieves nearly comparable *RT* ~380 ms at L_g = 100 nm) despite a higher shell doping of 10^{18} cm^{-3}. However, if we compare AM device with the same doping of 10^{18} cm^{-3}, SD JL MOSFET achieves ~6 times higher retention due to deeper potential in SD JL. In comparison to an IMOS (*RT* = ~320 ms at L_g = 150 nm) [49], SD JL DRAM achieves marginally higher *RT* (~380 ms) at 85 °C with smaller L_g of 100 nm and higher N_d (10^{18} cm^{-3}). Similarly, in comparison to Z^2-FET (*RT* ~1 s at L_g = 400 nm at 27 °C) [50], SD JL DRAM achieves high *RT* (~5.5 s) at 27 °C with smaller L_g of 200 nm and higher N_d of 10^{18} cm^{-3}.

4.5 Conclusion

The chapter demonstrates the advantage of shell doped architecture that facilitates enhanced depletion, thereby forming a deeper potential well that aids in higher *RT* at high temperatures. The maximum *RT* of ~5.5 s, ~275 ms, and ~16 ms is

achieved for shell doping of 10^{18}, 5×10^{18} and 10^{19} cm^{-3} with L_g of 200 nm at 27 °C, respectively. SD architecture with a thinner shell thickness shows better scalability with ~11 ms of *RT* for L_g of 10 nm and N_d of 10^{18} cm^{-3} at 85 °C. Further, the advantage of higher doping in SD JL transistor is presented in terms of variation in *RT* and RR_{RT} with temperature. The heavily doped region shows less reduction in retention time with temperature due to dominance of carrier lifetime on doping rather than on temperature. The maximum *RT* of ~120 ms is achieved at 125 °C with gate length of 200 nm and shell thickness of 2 nm. Results highlight the possibility of SD JL transistors for high speed embedded memory with a low write time of ~10 ns for T_{Shell} = 5 nm and $N_d = 10^{19}$ cm^{-3} at 85 °C. Volumetric analysis shows the competence of SD JL DRAM with other similar architectures. New viewpoints on SD architecture reflects better scalability, enhanced retention and less variation of *RT* with temperature, thus highlighting the opportunity to utilize heavily doped devices for 1T-DRAM for high temperature applications.

4.6 References

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Chapter 5

Conclusion and Scope for Future Work

5.1 Conclusion

This thesis presents physical insights and design considerations of junctionless transistors for 1T-DRAM applications. JL devices were originally introduced to replace the conventional *pn* junction based IM devices [1]. Although, previously published work on JL [2] shows the possibility as 1T-DRAM, the *RT*, which is the most essential metric for DRAM, is much lower than the target of 64 ms, specified by ITRS [3]. The lower depth of potential well as well as degraded carrier lifetime due to heavy doping limits the applicability of JL as 1T-DRAM. However, the higher doping can be advantage for reducing the write time of DRAM. Therefore, a careful reinvestigation is required to enhance the charge retention of JL based 1T-DRAM. The research work presented in the thesis focuses on evaluating and optimizing different physical processes that govern the performance as a capacitorless dynamic memory while improving retention, read sensitivity, scalability, write time, and the limiting associated trade-offs in a junctionless capacitorless DRAM. The simulation of junctionless devices in this thesis as 1T-DRAM was performed through Silvaco ATLAS simulation tool [4].

The main contribution of this research work is to utilize the different architectures of JL transistors to control the physical phenomenon occurring in the device, which influences the operation of dynamic memory, with a focus on improving retention and scaling capability. The thesis work demonstrates device perspective, where various DRAM metrics are regulated by device architectures (conventional DG JL, Stacked JL, and Shell-Doped JL), geometry (L_g, T_{si}, L_{un}), parameters (T_{ox}, φ_m) biases and temperature. The charge retention is regulated through hole generation and recombination [5], [6]. State ‘0’ is perturbed through thermal generation and BTBT of electrons towards drain/source that generates holes in the

potential well during Hold '0' operation [5], [6]. State '1' is disturbed due to the decrement in the hole concentration in the storage region due to thermal recombination and hole diffusion during Hold '1' operation [5], [6]. Thus, to attain a high retention time, which is one of the key metrics defining DRAM performance, the regulation of process governing hole recombination and generation is essential. The key conclusions of the work are as follows:

I. Design perspective of SOI based DRAM

The functionality of SOI architectures as DRAM is based on hole distribution in the storage region by using independent gate operation. The flow chart shown in Fig. 5.1 outlines the approach adopted for analysing and optimizing the operation as DRAM. The front gate (Gate 1) is utilized for conduction while back gate (Gate 2) is utilized to create an electrically induced potential well for charge storage. The optimized DRAM architectures can be classified for standalone and eDRAM according to the requirements of *RT* for both the cases [7].

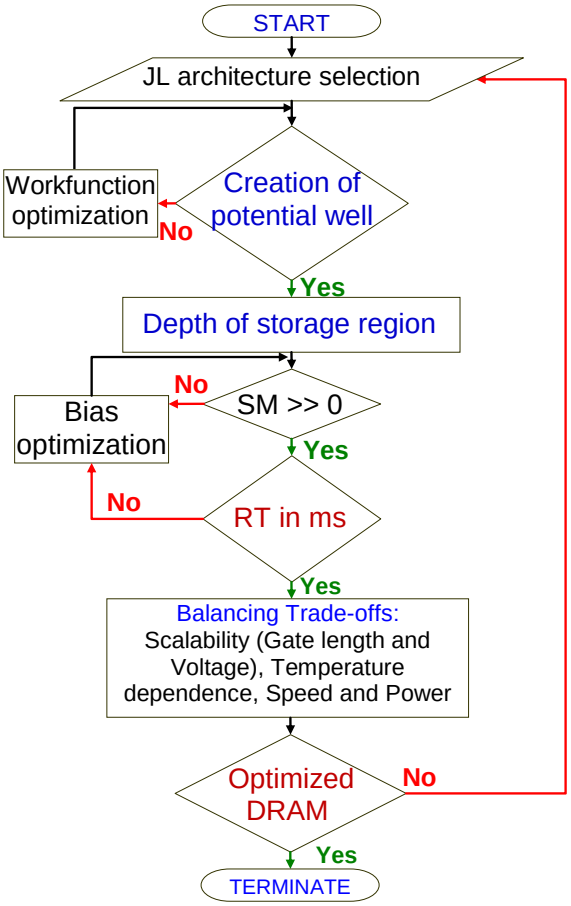

Fig. 5.1 Flow chart for assessing DRAM functionality.

II. Assessment of channel doping in JL for 1T-DRAM

DRAM metrics are governed through the generation and recombination of holes in the device, which are primarily controlled by potential well and carrier lifetime [5]. The doping dependent analysis in DG JL is carried out with a longer gate length of 400 nm, T_{Si} of 10 nm and T_{ox} of 1 nm. As BTBT can be significant in JL devices [8], an underlap length (L_{un}) of 10 nm is utilized to reduce the tunneling at source/drain and gate junctions. The assessment of channel doping in a JL device shows the dominant impact of carrier lifetime for channel doping (N_d) $\leq 10^{18}$ cm^{-3}, while the depth of potential well is more critical at higher doping levels ($> 10^{18}$ cm^{-3}). The carrier lifetime reduces exponentially from 76 ns (for 10^{15} cm^{-3}) to 25 ns, 3.7 ns, and 0.37 ns for a channel doping of 10^{17} cm^{-3}, 10^{18} cm^{-3}, and 10^{19} cm^{-3}, respectively, at 85 °C. An increase in channel doping reduces the *WT* (increases the speed of the memory) due to an increase in tunneling in device [8]. However, the main concern for the memory is to obtain higher retention time, which can lower the refresh rates and signify low power operation. Results indicate that higher doping in JL transistor can be beneficial for embedded DRAM (eDRAM) (as write operation is performed in ~10 ns at $N_d = 10^{19}$ cm^{-3}) while a lower doping is more appropriate for standalone applications as *RT* of ~4.5 s and ~2.5 s is obtained at $N_d = 10^{17}$ cm^{-3} at 27 °C and 85 °C, respectively. The work also shows the concept of volumetric analysis with different combinations of ($L_g \times T_{Si} \times W_{Si}$) to demonstrate the optimal device geometry to attain higher retention. The longer gate length and thinner film thickness in AM devices are beneficial for longer charge sustenance. Thinner silicon film can result in reduced hole recombination and generation, thereby enhancing the charge retention.

III. Separation of Conduction and Storage Regions

The applicability of JL based DRAM is further extended with separation of conduction and storage regions through an oxide material, which shows a considerable improvement (~ $\times 10^3$) in *RT* as compared with a conventional DG JL transistor with a doping (N_d) of 10^{19} cm^{-3} and gate length of 200 nm at 85 °C. The proposed topology consists of a conduction (top *n*-type JL layer) and storage (bottom *p*-type JL layer) regions that are physically isolated through an oxide layer. The work showcases that the creation of potential well is based on Metal-Oxide-Semiconductor (MOS) concept and electrostatic doping (underneath the

gate) effect [9]. The MOS concept can be implemented as the heavily doped Source/Drain (S/D) can act as metal (M), the separation oxide functions as an oxide (O), and the moderate *p*-type doping of storage region as semiconductor (S) region. The use of oxide layer (SOX), separating the conduction and storage regions reduces hole recombination as holes are maintained away from heavily doped n^{++} Source/Drain regions, and also, limit the generation of holes due to BTBT, and thus, can enhance *RT*. The maximum *RT* ~2.5 s and 600 ms for N_d as 5×10^{18} cm^{-3} and 10^{19} cm^{-3}, respectively, is achieved for L_g = 200 nm. Results indicate that the gate length of SJL based 1T-DRAM can be scaled down to 20 nm with *RT* of 1 ms at N_d of 5×10^{18} cm^{-3}. *RT* can be further improved for a shorter front gate length (L_{g1}) through use of an oversized back gate ($L_{g2} \cong L_{g1} + 2L_{un}$), which increases the storage region for holes. The higher *RT* in a heavily doped silicon film shows usefulness of SJL DRAM for standalone applications.

IV. Shell-Doped architecture as 1T-DRAM

Although the separation of conduction and storage regions through an oxide shows a possible solution to enhance *RT*, but the architecture requires more time to perform the Write '1' operation, and oversized back gate to enhance the retention at shorter gate lengths. These problems can be overcome with a Shell Doped (SD) JL architecture [10] in which heavily doped region (shell) is partitioned through an intrinsic silicon film (core). The work shows the advantage of shell doped architecture that facilitates enhanced depletion, thereby forms a deeper potential well that aids in higher *RT* at high temperatures. The maximum *RT* of ~5.5 s, ~275 ms, and ~16 ms is achieved for a shell doping of 10^{18}, 5×10^{18} and 10^{19} cm^{-3} with L_g of 200 nm at 27 °C, respectively. SD architecture with thinner shell thickness shows better scalability with ~11 ms of *RT* for L_g of 10 nm and N_d of 10^{18} cm^{-3} at 85 °C. Also, SD JL transistors with higher doping show the advantage in terms of less variation in *RT* and RR_{RT} with temperature. SD JL transistor showcases the possibility for high speed embedded memory with a low write time of ~10 ns for T_{Shell} = 5 nm and $N_d = 10^{19}$ cm^{-3} at 85 °C. Volumetric analysis shows the competence of SD JL DRAM with other similar architectures. The new viewpoints on SD architecture reflects better scalability, enhanced retention and less variation of *RT* with temperature, thus highlighting the

opportunity to utilize heavily doped devices with proper optimization for standalone as well as eDRAM at high temperature.

The physical insights and analysis of different attributes with optimal utilization lead to improved performance metrics as well as suppressed trade-offs. The systematic analysis through innovative approache has resulted in high retention, operation at lower drain bias at reduced volume. The use of optimized JL architectures for 1T-DRAM memory with *RT* > 64 ms is well-suited for standalone applications, and as well as, embedded DRAM.

5.2 Scope for future work

5.2.1 Balancing the trade-offs between DRAM metrics

Downscaling of SOI transistor limits *RT* due to BTBT and SCEs [11]. In addition, the formation of an ultrasharp *pn* junction in nanoscale regime is very difficult [1], [12]. Junctionless device with same type of carriers throughout the film overcomes challenge associated with the formation of an ultrasharp *pn* junction and SCEs [1], [12]. However, heavy doping in JL lowers the carrier lifetime and exhibits shallower potential depth (lesser depletion of carriers), and thus, degrades the retention time of 1T-DRAM cell [2], [13], [14]. The advantage of higher doping in junctionless device is that it requires less time (high speed) to perform Write '1' operation [14]. In order to achieve a high *RT* in junctionless based DRAM, vertical *n*-oxide-*p* junctionless transistor shows a better solution due to the separation of conduction and storage regions [15]. The issue with vertical *n*-oxide-*p* junctionless transistor, segregation of storage region from heavily doped n^{++} S/D regions, which requires more time to perform Write '1' operation [15].

In order to overcome this trade-off between speed and retention time, a double gate junctionless transistor with physical barrier (oxide underneath the S/D region) for 1T-DRAM application can be explored as an alternate solution. Holes can be stored in between two oxides underneath the S/D regions rather than in the potential well. The proposed architecture can achieve high *RT* due to a reduction in BTBT (during hold "0") and recombination (during hold "1") of holes in the storage region, while heavy doping in the transistor perform the write operation

very fast. Thus, a device with a physical barrier can be helpful to overcome the trade-off between speed (with WT < 10 ns) and RT (with RT > 64 ms) and can be utilized as a standalone as well as embedded DRAM.

5.2.2 JL with different materials for standalone and eDRAM

As DRAM metrics are governed through the generation and recombination of the carriers, and hence, can also be controlled through different semiconductor materials (Si, Ge, $Si_{1-x}Ge_x$, and GaAs) which can modulate the potential depth as well carrier lifetime. JL based 1T-DRAM with different semiconductor materials can improve the DRAM metrics at lower gate length and high temperature. Previously, results for Si JL based 1T-DRAM in SJL and SD topologies showed degradation in the retention characteristics in the nanoscale regime [15], [16]. The impact of material parameters such as carrier lifetime and energy bandgap can be analysed on DRAM metrics for standalone and eDRAM.

A higher bandgap (GaAs) material has lower carrier lifetime [17] but it can also exhibit a deeper potential as well as lower BTBT rate, which can enhance RT of the memory at higher temperatures. In comparison to GaAs based 1T-DRAM, lower bandgap material (Ge) is beneficial for high speed embedded memory application due to fast writing speed and requirement of a low drain bias. However, higher BTBT rate in lower bandgap material can consume more power even at a low drain bias as compared to GaAs based DRAM. Therefore, need for appropriate innovations at material and device (biasing) aspects to overcome the trade-off between retention time and speed of the memory can be useful to extend DRAM functionality.

5.2.3 1T-DRAM with Gate-All-Around Architecture

Over the past few decade, the scaling of MOSFETs increasing the transistor density and performance of memory chip. However, continuing this trend in the nanometer regime is very challenging due to the drastic increase in the subthreshold leakage current (I_{off}) [18], [19]. The increase in leakage current degrades the performance of the transistor and thus, the charge retention of the memory. Junctionless transistor with Gate-All-Around (GAA) architecture are potential candidates for next generation high speed and low power electron

devices due to their electrostatic integrity and simple fabrication steps [1]. The better gate controllability of GAA architecture compared to planer MOSFET achieves deeper potential well and reduces the BTBT, which can improve the performance of 1T-DRAM cell in nanoscale regime.

5.3 References

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Appendix

A typical program (syntax) for device structure generation and current-voltage simulation in ATLAS tool [1] is shown below. The parameters used in the simulation should be carefully evaluated considering doping and temperature dependence.

1. Structure generation and current-voltage characteristics of inversion mode transistor

#Start the program
#Structure Creation
go atlas
mesh space.mult=1.0

 # Syntax for defining Mesh in x-direction
x.mesh loc=0 spac=0.05
x.mesh loc=0 spac=0.05
x.mesh loc=0.1 spac=0.05
x.mesh loc=0.29 spac=0.05
x.mesh loc=0.29 spac=0.05
x.mesh loc=0.29 spac=0.001
x.mesh loc=0.3 spac=0.001
x.mesh loc=0.305 spac=0.008
x.mesh loc=0.5 spac=0.008
x.mesh loc=0.695 spac=0.008
x.mesh loc=0.7 spac=0.001
x.mesh loc=0.71 spac=0.001
x.mesh loc=0.71 spac=0.05
x.mesh loc=0.9 spac=0.05
x.mesh loc=1 spac=0.05

#Syntax for defining Mesh in y-direction
y.mesh loc=0 spac=0.0005
y.mesh loc=0.001 spac=0.0005
y.mesh loc=0.001 spac=0.0008
y.mesh loc=0.006 spac=0.0008
y.mesh loc=0.011 spac=0.0008
y.mesh loc=0.011 spac=0.0005
y.mesh loc=0.012 spac=0.0005

#Syntax for Region and Area specification
region num=1 material=Air
region num=2 x.min=0.3 x.max=0.7 y.min=0 y.max=0.012 material=SiO2
region num=3 x.min=0 x.max=1 y.min=0.001 y.max=0.011 material=Silicon

#Syntax for Electrode specification
electrode name=source x.min=0 x.max=0.1 y.min=0.001 y.max=0.001
electrode name=drain x.min=0.9 x.max=1 y.min=0.001 y.max=0.001
electrode name=gate1 x.min=0.3 x.max=0.7 top
electrode name=gate2 x.min=0.3 x.max=0.7 bottom

#Syntax for Doping specification
doping uniform x.left=0 x.right=1 y.top=0.001 y.bottom=0.011 conc=1e15 p.type reg=3
doping uniform x.left=0 x.right=0.29 y.top=0.001 y.bottom=0.011 conc=1e20 n.type reg=3
doping uniform x.left=0.71 x.right=1 y.top=0.001 y.bottom=0.011 conc=1e20 n.type reg=3

 # Syntax for Contact specification
contact name=source
contact name=drain
contact name=gate1 workfunction=4.7
contact name=gate2 workfunction=4.7

#Syntax for models used in the analysis
models fldmob consrh bbt.std cvt bgn auger bipolar conmob temperature=300 print

#Defining iteration method
method newton

#Syntax for visualizing energy band diagram, potential, and electric field distribution
output con.band val.band e.field recomb u.auger u.bbt u.srh

#Syntax to save structure at zero bias condition
solve init
solve vsource=0
solve vgate1=0
solve vdrain=0
solve vgate2=0
save outf=MOSFET.str

#Syntax to visualize the DC characteristics of the transistor
solve vdrain=0.0 vstep=0.1 vfinal=1.0 name=drain

log DC_IV.log
solve vgate1=0.0 vstep=0.1 vfinal=1.0 name=gate1

#Syntax for analysing the time dependent behaviour of the transistor
solve vgate1=1.0 vgate2=-1.6 vdrain=1.5 vsource=0.0 ramptime=1e-12 tstep=2e-12 tstop=50e-9

exit

2. Structure generation and current-voltage characteristics of Accumulation Mode/Junctionless transistor

#Start the program
#Structure Creation
go atlas
mesh space.mult=1.0

 # Syntax for defining Mesh in x-direction
x.mesh loc=0 spac=0.05
x.mesh loc=0 spac=0.05
x.mesh loc=0.1 spac=0.05
x.mesh loc=0.29 spac=0.05
x.mesh loc=0.29 spac=0.05
x.mesh loc=0.29 spac=0.001
x.mesh loc=0.3 spac=0.001
x.mesh loc=0.305 spac=0.008
x.mesh loc=0.5 spac=0.008
x.mesh loc=0.695 spac=0.008
x.mesh loc=0.7 spac=0.001
x.mesh loc=0.71 spac=0.001
x.mesh loc=0.71 spac=0.05
x.mesh loc=0.9 spac=0.05
x.mesh loc=1 spac=0.05

#Syntax for defining Mesh in y-direction
y.mesh loc=0 spac=0.0005
y.mesh loc=0.001 spac=0.0005
y.mesh loc=0.001 spac=0.0008
y.mesh loc=0.006 spac=0.0008
y.mesh loc=0.011 spac=0.0008
y.mesh loc=0.011 spac=0.0005
y.mesh loc=0.012 spac=0.0005

#Syntax for Region and Area specification
region num=1 material=Air
region num=2 x.min=0.3 x.max=0.7 y.min=0 y.max=0.012 material=SiO2
region num=3 x.min=0 x.max=1 y.min=0.001 y.max=0.011 material=Silicon

#Syntax for Electrode specification
electrode name=source x.min=0 x.max=0.1 y.min=0.001 y.max=0.001
electrode name=drain x.min=0.9 x.max=1 y.min=0.001 y.max=0.001
electrode name=gate1 x.min=0.3 x.max=0.7 top
electrode name=gate2 x.min=0.3 x.max=0.7 bottom

#Syntax for Doping specification
doping uniform x.left=0 x.right=1 y.top=0.001 y.bottom=0.011 conc=1e18 n.type reg=3

```
doping uniform x.left=0 x.right=0.29 y.top=0.001 y.bottom=0.011 conc=1e20
n.type reg=3
doping uniform x.left=0.71 x.right=1 y.top=0.001 y.bottom=0.011 conc=1e20
n.type reg=3

# Syntax for Contact specification
contact name=source
contact name=drain
contact name=gate1 workfunction=5.0
contact name=gate2 workfunction=5.2

#Syntax for models used in the analysis
models fldmob consrh bbt.std cvt bgn auger bipolar conmob temperature=300
print
impact selb

#Defining iteration method
method newton

#Syntax for visualizing energy band diagram, potential, and electric field
distribution
output con.band val.band e.field recomb u.auger u.bbt u.srh

#Syntax to save structure at zero bias condition
solve init
solve vsource=0
solve vgate1=0
solve vdrain=0
solve vgate2=0
save outf=MOSFET.str

#Syntax to visualize the DC characteristics of the transistor
solve vdrain=0.0 vstep=0.1 vfinal=1.0 name=drain

log DC_IV.log
solve vgate1=0.0 vstep=0.1 vfinal=1.0 name=gate1

#Syntax for analysing the time dependent behaviour of the transistor
solve vgate1=1.0 vgate2=-1.6 vdrain=1.5 vsource=0.0 ramptime=1e-12 tstep=2e-
12 tstop=50e-9

exit
```

A1. References

[1] Atlas User's Manual, Silvaco Int., Santa Clara, CA, Jan. 18, 2015.