Design and Simulation of Low Power Operational Transconductance Amplifier

M.Tech. Thesis

By
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DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

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DESIGN AND SIMULATION OF LOW POWER OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

A THESIS

Submitted in partial fulfillment of the

requirements for the award of the degree

of

M.Tech. Thesis

by

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **Design and Simulation of Low Power Operational Transconductance Amplifier** in the partial fulfillment of the requirements for the award of the degree of **Master of Technology - VLSI Design And Nanoelectronics** and submitted in the **Department of Electrical Engineering, Indian Institute of Technology Indore,** is an authentic record of my own work carried out during the time period from July 2023 to June 2025 under the supervision of Dr. Vipul Singh, Professor, Indian Institute of Technology Indore, Indore, India.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

21/05/2025

Signature of the Student with Date

(Atharv Alok Limaye)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

23/05/2025

Signature of the Supervisor of M.Tech. Thesis with Date

(Prof. Vipul Singh)

Atharv ALok Limaye has successfully given his M.Tech. Oral Examination held on **05/05/2025**

23/05/2025

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Date:

Saptarshi Ghosh

Signature of Convener, DPGC

Date: 23-05-2025

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This Thesis is Dedicated

to

my family and friends

Abstract

In the era of portable and battery-operated devices, the need for power-efficient analog circuits has grown significantly. Operational Transconductance Amplifiers (OTAs), being integral components in analog signal processing, data conversion, and sensing applications, must be optimized to balance power consumption with performance. This work presents the design and implementation of a low-power Class-AB OTA using standard 180nm CMOS technology, targeting low-voltage, energy-constrained systems such as biomedical devices, wearable electronics, and sensor interfaces.

A two-stage as well as three-stage amplifier architecture have been worked upon, enhanced by Class-AB output operation to improve drive capability and dynamic range without significantly increasing quiescent power consumption. The design incorporates Miller compensation to ensure adequate phase margin and stability across a wide range of capacitive loads. Low power operation is achieved through optimized transistor sizing and bias current selection, focusing on minimizing static power dissipation while retaining high gain and sufficient bandwidth.

Simulations performed using Cadence tools confirm that the proposed OTA achieves a favorable trade-off between power, gain, and stability. By leveraging conventional design techniques such as Class-AB operation and Miller compensation, this work demonstrates a practical approach to developing low-power OTAs within mature 180nm CMOS technology. The design is compatible with standard analog design flows, making it ideal for integration into energy-efficient analog and mixed-signal systems where use of biomedical devices is prominent.

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List of Abbreviations

OTA	Operational Transconductance Amplifier
CMOS	Complementary Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Feild Effect Transistor
CLM	Channel Length Modulation
EDA	Electronic Design Automation
PDK	Process Design Kit
gm	Transconductance
CS	Common Source
IC	Integrated Circuits
ADC	Analog to Digital Converter
PVT	Process Voltage Temperature
CG	Common Gate
FET	Feild Effect Transistor
CMRR	Common Mode Rejection Ratio
SCMOS	Self Cascode MOS
RNMC	Reverse Nested Miller Compensation
PPF	Partial Positive Feedback
RHP	Right Half Plane
BDOTA	Bulk-Driven OTA
LPOTA	Low Power OTA
ICMR	Input Common Mode Range

Chapter 1

Introduction to Amplifiers

1.1 Motivation of the Project:

Low Power Operational Transconductance Amplifiers (OTAs) are extensively used in biomedical applications due to their ability to function efficiently at low power levels. Biomedical devices, such as wearable monitors and implantable sensors, demand extremely low power consumption to prolong battery life and prevent overheating. OTAs are ideal for this as they operate at low quiescent currents, making them suitable for compact, battery-powered systems. Because they're compatible with CMOS technology, these chips can be designed to be incredibly compact.

In addition to low power, OTAs offer a high degree of flexibility in analog signal processing, particularly in filter design. Biomedical signals like ECG, EEG, and EMG are typically low-frequency and analog, requiring precise filtering to isolate useful information and suppress noise. OTA-based filters, especially OTA-C filters (using only OTAs and capacitors), are widely used for this purpose. The filter circuitry can be configured into low-pass, band-pass, or notch filter topologies.

Another big plus of OTAs in biomedical applications is that they’re electronically tunable. By adjusting the bias current, we can easily change the gain and cutoff frequencies of OTA-based filters. This tunability makes OTAs highly versatile in environments where signal properties may vary significantly or need to be customized for individual users.

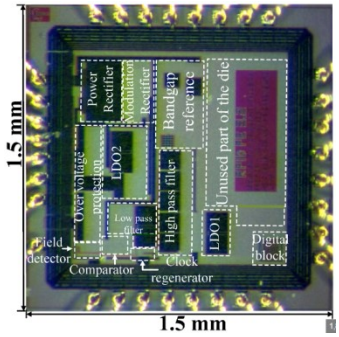


Fig 1.1: Use of OTA in all Components

Lastly, OTAs provide high input and low output impedance, enabling precise signal sensing with minimal source loading for accurate measurements. This is particularly critical when dealing with weak biosignals from the human body, where any distortion or signal loss can compromise the quality of diagnosis or monitoring. Overall, the combination of low power, tunability, compactness, and effective signal conditioning makes OTAs a foundational component in modern biomedical electronics and analog filter design.

1.2 Simulations of Cadence:

Cadence is a leading Electronic Design Automation (EDA) tool widely used for the design, simulation, and verification of analog and digital integrated circuits. For simulating a Low Power OTA, Cadence Virtuoso, combined with the Spectre simulator, offers a comprehensive environment. Using SCL 180nm CMOS technology, designers can analyze the performance of the OTA across multiple operating conditions and optimize it for power, gain, bandwidth, and other key metrics.

1. Setting Up the Environment
    a) Technology File: Begin by installing and configuring the 180nm CMOS Process Design Kit (PDK), such as from UMC or TSMC, in Cadence Virtuoso. The PDK contains all necessary design rules, models, and components for simulation and layout.

b) Library Creation: Create a new design library and attach it to the installed 180nm technology.

c) Schematic Entry: Use the Composer tool to draw the OTA schematic using the provided MOSFETs and other passive components (e.g., capacitors, resistors) from the PDK.

2. DC Analysis

   a) Biasing Setup: Perform DC analysis to verify that all transistors are operating in the desired regions (typically saturation for amplifying stages).

   b) Current Consumption: Measure the total current from the supply to evaluate power consumption.

   c) Node Voltages: Check DC operating points to ensure correct biasing for low power operation (especially in subthreshold designs).

3. AC Analysis

   a) Gain and Bandwidth: Perform AC analysis using a small-signal input to measure the open-loop voltage gain and -3dB bandwidth of the amplifier.

   b) Determine the transconductance (g_m) and output resistance (r_o) through gain analysis and examination of the circuit topology.

4. Transient Analysis

   a) Step Response: Apply a pulse or step input and observe the output voltage over time to examine settling time, slew rate, and dynamic behavior.

   b) Linearity: A sinusoidal input can be used to assess signal integrity and check for distortion under transient conditions.

5. Power Analysis

   a) Measure total power consumption by observing supply current and multiplying with supply voltage.

   b) Validate that the design meets the low-power specifications.

1.3 Amplifier:

An amplifier is a fundamental electronic device or circuit designed to increase the magnitude of a signal - whether voltage, current, or power. The amplification process involves using an external power source to supply the energy required to boost the signal. The device accepts a weak input signal and outputs a stronger output signal that resembles the input in waveform but is larger in amplitude.

The gain of an amplifier, a fundamental performance parameter, represents the ratio of output to input signal magnitude. Depending on the amplifier type and application, gain may be specified as voltage gain (Vout/Vin), current gain (Iout/Iin), or power gain (Pout/Pin). This classification leads to distinct amplifier categories including voltage amplifiers, current amplifiers, power amplifiers, and operational amplifiers (op-amps), each optimized for specific circuit requirements.

Amplifiers serve as fundamental components across diverse domains, including audio systems, telecommunications, medical instrumentation, and sensor interfaces. Their performance is characterized by essential parameters that minimize loading effects, ensure effective power delivery, linear response, operational stability, and minimal distortion.

Some of the widely used chipsets are:
Neural Amplifier: Neural Prosthetics
Integrator Circuits: Low Noise Amplifiers
Low Pass filters: ECG, EEG, Pulse Oximeters
Instrumentation Amplifier: EMG, ECG, BP Monitors

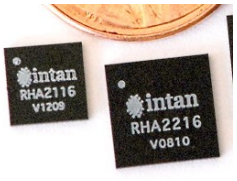


Fig1.2: Neural Amplifier, Integrator Circuits, LP Filter and Instrumentation Amplifier

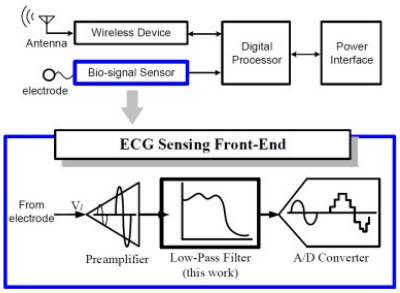


Fig1.3: OTA in Bio-Medical Device Usage

1.4 MOS Amplifier and Current Mirrors:

We use the term "deep triode region" for $V_{DS} << 2(V_{GS} - V_{TH})$, where the transistor operates as a resistor.In reality, the drain current reaches "saturation," that is, becomes constant for $V_{DS} > V_{GS} - V_{TH}$. The channel experiences pinch-off if $V_{DS} = V_{GS} - V_{TH}$.

Further increase in V_{DS} simply shifts the pinch-off point slightly toward the drain and the current equation becomes independent of V_{DS}. This is called the "overdrive voltage," the quantity $V_{GS}-V_{TH}$ plays a key role in MOS circuits. MOSFETs are sometimes called "square law" devices to emphasize the relationship between I_D and the Overdrive.

In Saturation region, the MOSFET behaves like a voltage-controlled current source. For amplification, a DC bias is applied to the gate to set V_{GS} such that the transistor remains in saturation throughout the signal swing.

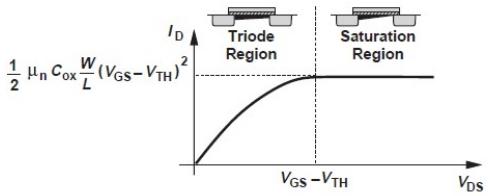


Fig.1.4: Amplifier behaviour for different Regions

A small AC signal is then superimposed on this DC bias. These current changes, flowing through a load resistor (R_D) connected at the drain, create voltage variations at the output. Since the output voltage depends on the current through R_D, small input voltage changes result in large output voltage swings, thus achieving amplification (Fig.1.5). The voltage gain is approximately:

$$A_v = -g_m R_D$$

Where g_m is the transconductance, indicating how sensitive the drain current is to changes in V_{GS}.

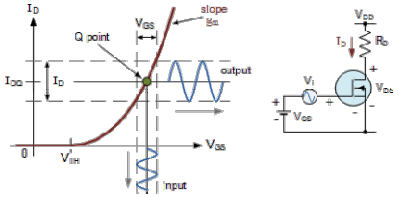


Fig1.5: For small V_{GS}, large change in Current

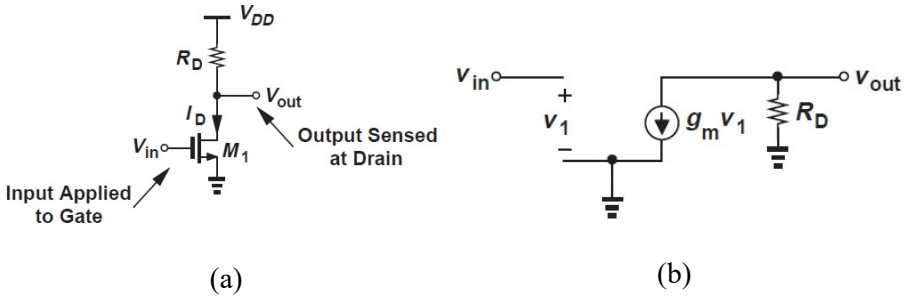
The transistor amplifies because in saturation, small variations in gate voltage lead to proportional changes in current, which through a resistor or load, result in amplified voltage swings.

1.4.1 Common Source amplifier:

The input signal at the gate modulates the MOSFET's channel, converting voltage variations to drain current via its g_m. This current flows through the load resistance (R_D), generating an output voltage at the drain ($V_{out} = i_ə \times R_l$). Both nMOS and pMOS operate similarly but with opposite polarity.

$$\frac{v_{out}}{v_{in}} = -\, g_m R_D$$

1.4.1.1 Resistance R_D:



(a) (b)

Fig.1.6: (a) CS Amplifier, (b) Small Signal Model of CS amplifier

Effect of CLM
$A_v = -g_m(R_D||r_o)$
$R_{in} = \infty$
$R_{out} = R_D||r_o$

The amplifier works by using the transconductance property of the MOSFET: it converts a small input voltage at the gate into a modulated current through the drain, which then develops a voltage across a load resistor (or active load).

- The gate of the nMOS is insulated.
- A small input voltage (Vin) applied at the gate terminal modulates the current flowing from drain to source (I_D).
- This current travels through the R_D, causing a voltage drop.
- The output voltage is taken at the drain, and it changes inversely with the input voltage: as Vin increases, Vout decreases, and vice versa. This gives it inverting gain.
- A bias voltage (V_{GS}) must be applied to the gate to ensure $V_{GS} > V_{th}$.
- This can be done by a voltage divider or current source.

Advantages of CS amplifier:

- Simple design
- High Input Impedance
- Can achieve significant Voltage Gain

Limitations of CS Amplifier:

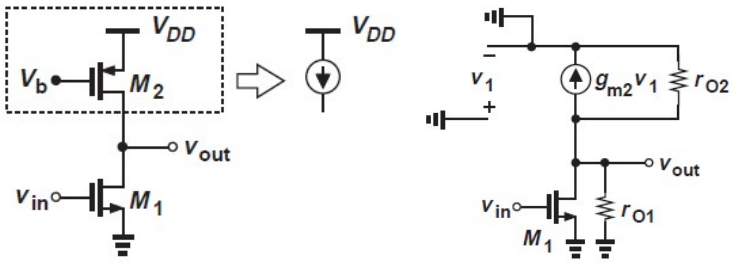
- Requires precise biasing

- Gain can vary with temperature and device parameters
- Output resistance may limit the drive capability

1.4.1.2 Current Source Load:

The gain-headroom trade-off in amplifier design can be mitigated by substituting resistive loads with current sources. This approach offers significant performance benefits, as evidenced by CS amplifiers: This configurations demonstrate superior voltage gain, enhanced output swing, and improved power efficiency compared to their resistor-loaded counterparts.

In a conventional CS amplifier using a resistor R_D as the load, Voltage Gain here $A_v=-g_mR_D$. But, physical resistor R_D, which occupies significant chip area in ICs and is limited in value due to voltage headroom and power consumption. Larger R_D gives higher gain but reduces the available output swing and increases power dissipation.



(a) (b)

Fig.1.7: (a) CS with current Source Load, (b) Small Signal model

By contrast, replacing R_D with an active load, such as a current source implemented with a MOSFET, overcomes these limitations. A current source has a very high output resistance r_o, often in the range of tens or hundreds of kilo-ohms, which effectively boosts the voltage gain to $A_v = -g_m r_o$. This allows higher gain without increasing the physical size or power consumption.

Using a current source load has some real advantages—it improves biasing stability and output swing, which is especially helpful in differential amplifiers and analog ICs where headroom is tight. Plus, since you can adjust it electronically by tweaking the bias current, it gives designers more flexibility.

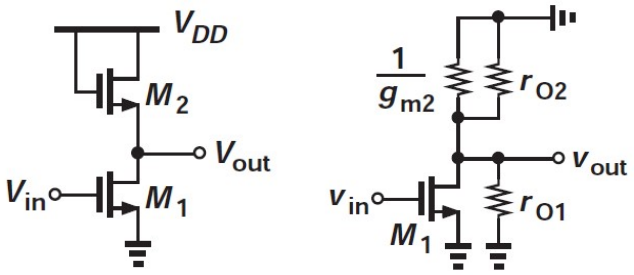
On top of that, resistors in IC design eat up a lot of space and can hurt performance. It's way more compact and helps keep amplifier stages efficient, making it a great fit for analog and mixed-signal systems.

Thus, this configuration is preferred in modern analog design for higher gain, better linearity, efficient use of power supply voltage, and better scalability in ICs.

1.4.1.3 Diode Connected:

A CS amplifier with a diode-connected load is a popular configuration in analog integrated circuits due to its simplicity, compactness, and reliable performance. In this setup, the load is a MOSFET with its gate and drain connected together, forming a diode-like behavior. This forces the MOSFET to operate in the saturation region, acting as a nonlinear resistor with moderately high resistance, suitable for signal amplification.

This configuration is favored for its area efficiency and ease of implementation. Unlike resistive or current-source loads, a diode-connected load uses a single MOSFET, making it ideal for space-constrained ICs. It also simplifies the biasing of the amplifier by ensuring that the load device remains in saturation, which stabilizes the operating point and improves circuit reliability.



(a) (b)

Fig.1.8: (a) Diode Connected CS, (b) Small Signal Model

$$\mathrm{Av} = -\mathrm{gm1}\left(\frac{1}{\mathrm{gm2}} \,||\, \mathrm{ro2} \,||\, \mathrm{ro1}\right)$$

$$\mathrm{Rout} = \left(\frac{1}{\mathrm{gm2}} || \mathrm{ro2} || \mathrm{ro1}\right)$$

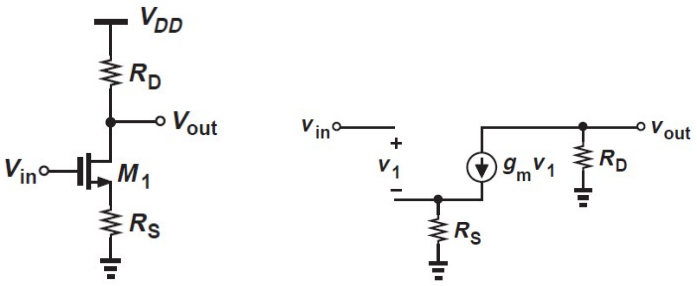
Another advantage is device matching, particularly when both the transistors are fabricated identically. This matching leads to predictable behavior and improved linearity in signal amplification. However, the gain here that is determined by the ratio of the g_m of the two transistors, the overall voltage gain is moderate. Specifically, the voltage gain is approximately $A_v = -\frac{g_{m1}}{g_{m2}}$, often close to -1 if the transistors are identical.

While the gain is lower compared to amplifiers with current-source loads, the diode-connected load offers better frequency response and bandwidth, thanks to its lower output resistance. Therefore, this configuration is commonly used in the initial stages of analog circuits, such as differential amplifiers and biasing networks, where compactness, linearity, and consistent performance are more important than achieving high gain.

1.4.1.4 Source Degenerated:

A source-degenerated CS amplifier adds a resistor at the MOSFET's source terminal. This negative feedback improves linearity, gain stability, and input impedance.

One of the primary uses of the source-degenerated CS amplifier is in high-linearity analog circuits, such as those found in communication systems and ADCs. The negative feedback introduced by the source resistor linearizes the amplifier's response by making the output less sensitive to changes in the transistor's g_m. This is especially useful in environments where signal distortion must be minimized.



(a) (b)

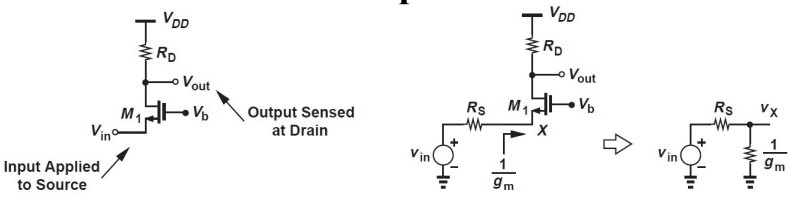
Fig.1.9: (a) CS degenerated, (b) Small Signal Model

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_D}{1 + g_m R_S}$$

Another important application is in bias-stable amplifier stages. Because the gain becomes less dependent on the variations in PVT, the amplifier's performance remains consistent. This predictable gain behavior makes it useful in designing analog circuits that require reliable performance over varying conditions.

Additionally, source degeneration is widely used in differential amplifier designs, where matching and balance are critical. It also helps in increasing the input resistance of the amplifier, making it suitable for applications where the signal source has a relatively high impedance. Due to these advantages, source-degenerated CS amplifiers are commonly found in operational amplifier stages, analog front ends, and RF circuit blocks where both linearity and robustness are essential.

1.4.2 Common Gate Amplifier:



(a) (b)

Fig.1.10: (a) CG Amplifier, (b) Small Signal Model

$$R_{in} = 1/\mathrm{g_m}$$

$$R_{out} = R_D$$

$$\frac{vout}{vin} = \frac{g_m R_D}{1 + g_m R_S}$$

The CG amplifier's voltage gain mirrors the degenerated CS stage's magnitude but with opposite polarity. Unlike CS topologies, the CG configuration provides unity current gain, with the input current directly propagating from source to drain. This analysis holds for the general case, accounting for both channel-length modulation and finite source impedance.

The common-gate (CG) configuration features a DC-biased gate terminal with signal input at the source and output at the drain. Contrasting with common-source amplifiers that ground the source, the CG topology AC-grounds the gate while actively driving the source. This unique arrangement provides inherently low input impedance and excellent high-frequency response, making it ideal for radio-frequency applications and impedance transformation circuits where broadband performance is critical.

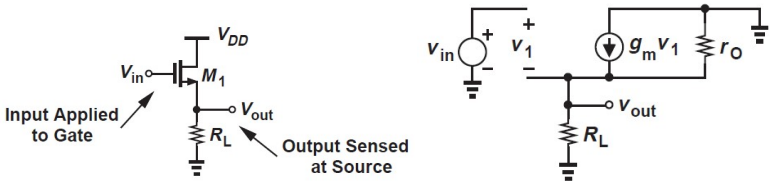
In a CG amplifier, the input signal at the source modulates the current through the transistor, and the output is developed at the drain across a load resistor or current source. The voltage gain is positive and typically high, and the configuration does not invert the signal, unlike the CS amplifier.

One of the defining characteristics of the CG amplifier is its low input impedance, approximately $\frac{1}{g_m}$, which makes it suitable for interfacing with low-impedance sources. The output impedance is relatively high, similar to the CS amplifier, making the CG amplifier well-suited for voltage amplification in cascaded stages.

The CG amplifier shares similarities with the source-degenerated CS amplifier, particularly in how it responds to the input signal and the role of negative feedback.

In a source-degenerated CS amplifier, a resistor is added in series with the source terminal to introduce local negative feedback, improving linearity and stabilizing the gain. Interestingly, this resistor impedes the signal flow in a way that partially mimics the behavior of the CG configuration. From a small-signal perspective, both configurations can achieve similar voltage gain expressions under certain conditions, and both can offer wide bandwidth and good linearity. The main distinction lies in their input impedance: the CG amplifier inherently has low input impedance, whereas the source-degenerated CS amplifier increases the input impedance compared to a basic CS stage. CG and source-degenerated CS amplifiers manage feedback and signal control, making them suitable for overlapping applications in analog and RF design where gain stability, bandwidth, and impedance matching are critical.

1.4.3 Source Follower Amplifier:



(a) (b)

Fig.1.11: (a) Source Follower, (b) Small Signal Model

$$\frac{v_{out}}{v_{in}} = \frac{r_o||R_L}{\frac{1}{g_m} + (r_o||R_L)}$$

$$R_{out} \approx \frac{1}{g_m}||R_L$$

The amplifier operates as a source follower, sensing inputs at the gate and delivering outputs at the source (with drain at VDD). A small increase in M1's gate voltage (Vin) elevates V_{GS}, increasing the source current and consequently Vout. This voltage-following action, offset by a V_{GS} level shift, enables DC level translation while preserving signal integrity.

The common source follower amplifier, more commonly known as the source follower or common drain amplifier, is a fundamental MOSFET-based amplifier configuration used primarily for voltage buffering.

This arrangement results in a configuration where the source terminal "follows" the gate voltage. One of the defining features of the source follower is that it provides unity gain (or slightly less than one) with a high input resistance and low output resistance, making it ideal for impedance matching and signal buffering between stages.

Unlike the common source amplifier which inverts and amplifies the input signal, the source follower does not invert the signal and offers minimal voltage gain—typically slightly less than one due to the voltage drop across the MOSFET's gate-source threshold. However, its real strength lies in impedance transformation.

Because of the MOSFET’s insulated gate, the input impedance is very high, which means it draws almost no current from the preceding stage. Simultaneously, the low output resistance allows the amplifier to drive low-impedance loads without significant signal loss. This makes the source follower highly useful in analog signal chains where loading effects must be minimized.

Additionally, the source follower provides excellent buffering capability, making it a common choice in the output stages of operational amplifiers, voltage followers, and analog front ends. It is also widely used in analog integrated circuits for level shifting and driving large capacitive loads. Although the voltage gain is close to unity, the combination of high input impedance, low output impedance, and signal fidelity makes the source follower an essential building block in analog circuit design.

1.4.4 Current Mirrors:

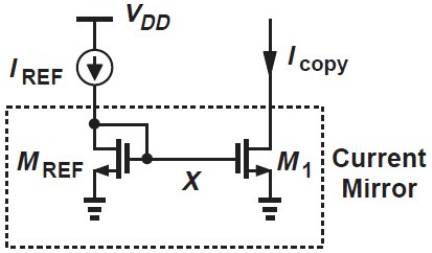


Fig.1.12: Current Mirror Circuit

$$I_{copy} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} I_{REF}$$

A current mirror is a fundamental analog building block used in MOSFET circuits to copy or replicate a reference current in one branch of a circuit into another branch. It operates based on the principle that two or more transistors with the same characteristics and operating conditions will conduct the same drain current if their gate-source voltages are equal. In MOSFET-based current mirrors, this is achieved by connecting the gate and drain of one transistor (the reference transistor) to form a diode-connected MOSFET, and then mirroring its gate voltage to one or more identical transistors (the output transistors), ensuring they conduct the same current.

Current mirrors are widely used in analog circuits such as biasing networks, active loads, differential amplifiers, operational amplifiers, and current-mode signal processing systems due to their ability to provide constant, stable currents and compact current replication across a chip. The basic current mirror consists of two matched nMOS or pMOS transistors. The reference transistor has its drain and gate connected together, forming a diode-like structure that sets a fixed gate-source voltage based on a reference current I_{REF}.

This gate voltage is then applied to the gate of the second transistor, ensuring that it operates under the same V_{GS} and ideally mirrors the same current $I_{OUT} \approx I_{REF}$. However, this basic design assumes perfect matching and infinite output resistance, which is rarely achievable in practice. To improve performance, more advanced current mirror types are used.

The Wilson current mirror is a three-transistor configuration that offers higher output resistance and better current matching compared to the basic current mirror. By introducing negative feedback through an additional transistor, it reduces the sensitivity of the output current to changes in output voltage, thereby improving accuracy in real-world applications.

The cascode current mirror is another widely used variant that further improves output impedance and accuracy by stacking a cascode transistor on top of the output transistor. This cascode structure keeps the drain-source voltage of the output transistor constant, enhancing current stability over varying output voltages. It is essential in high-precision analog circuits.

Other types include the regulated cascode current mirror, which adds an amplifier to regulate the gate of the cascode device, achieving even higher output resistance and improved current copying. Low-voltage current mirrors and wide-swing mirrors are designed for modern low-power designs where headroom is limited, allowing better performance under tight voltage constraints.

1.4.5 Cadence Results for CS Amplifiers:

V_{DD} = 1.8V, SCL 180nm Technology

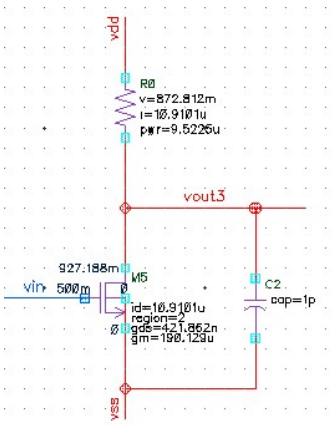


Fig1.13: CS Amplifier with Resistance R_D

R_D = 85 kΩ

W/L_{nM} = 6.2 µm/0.5 µm

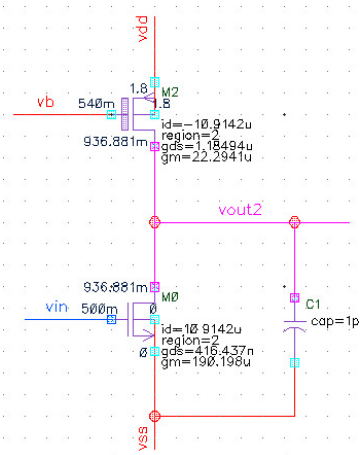


Fig1.14: CS Amplifier with Current Source Load
W/L_{M2} = 0.3 µm/ 0.5 µm
W/L_{M0} = 6.2 µm/0.5 µm

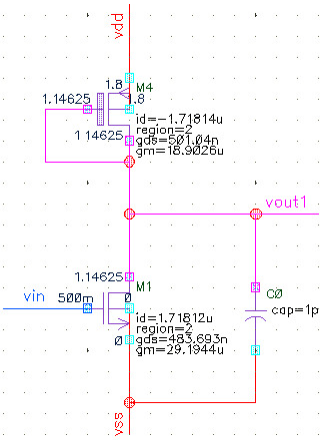


Fig1.15: CS Amplifier with Diode Connected Load
W/L_{M4} = 0.42 µm/ 0.18 µm
W/L_{M1} = 0.42 µm/0.18 µm

1.5 OTA and Configurations:

Operational Transconductance Amplifiers (OTAs) are analog building blocks that function as voltage-controlled current sources. Unlike traditional operational amplifiers (op-amps), which provide voltage output, OTAs convert an input voltage difference into an output current. The key relationship for an ideal OTA is:

$$I_o = G_m(V_+ - V_-)$$

where I_o is the output current, V+ and V− are the non-inverting and inverting input voltages respectively, and gm is the transconductance, typically controlled by a bias current I_{bias}.

This makes OTAs particularly useful in systems where current-mode signal processing or electronically tunable behavior is desired.

OTAs can be configured in various ways to realize different analog functions. A common application is the OTA-C filter, where the OTA is used with capacitors (and no resistors) to create low-pass, high-pass, band-pass, and notch filters. For example, a first-order low-pass filter using an OTA and capacitor C has a transfer function:

$$H(s) = \frac{I_{out}}{V_{in}} = \frac{g_m}{sC+g_m}$$

This allows the cutoff frequency fc = $\frac{g_m}{2\pi C}$ to be tuned by adjusting g_m, which in turn is controlled by I_{bias}. In addition to filters, OTAs can be configured for variable gain amplifiers, oscillators, integrators, and mixers. In a linear integrator configuration, for instance, the OTA feeds a capacitor and the output voltage is the time integral of the input signal:

These configurations benefit from the OTA's high input impedance and controllable output characteristics, making them highly adaptable for analog signal processing tasks where conventional op-amps may be less efficient or too rigid.

Feature	Operational Transconductance Amplifier	Voltage Amplifier
Output Type	Current	Voltage
Transfer Function	$I_{out} = g_m(V_{in})$	$V_{out} = A_v(V_{in})$
Gain Control	Tuned by bias current I_{bias}	Fixed or externally set (resistors)
Typical Use	Filters, modulators, integrators	Amplifiers, buffers, comparators
Output Impedance	High	Low
Common Configuration	OTA-C filters	Op-amp circuits (inverting/non-inv.)

Table1: Difference between OTA and Voltage Amplifier

1.6 Organization of Thesis:

- In **Chapter 1,** we started our discussion on different types of amplifiers and based on different device configuration and discussed their working principle.
- In **Chapter 2**, we have discussed on differential Amplifiers and their importance to modern CMOS Amplifiers and Biomedical Devices. Along with this we will also focus on different configurations that have been used in OTAs for reduction of instability with the help of introduction of poles and zeroes using passive components.
- In **Chapter 3,** a Bulk-Driven MOS configuration has been discussed with the usage of Class-AB Configuration to add stability to the system in Low Power application.
- In **Chapter 4**, Cadence Simulation Results focusing on the Bulk-Driven Inputs and Class-AB Amplifiers with Different configuration discussed in Chapter 2.
- In **Chapter 5,** presents the conclusion of the work done and the future scope of the presented word.

Chapter 2

Differential Amplifier and Amplifier Configurations

This chapter focuses on the development Differential Amplifier and its transition from Conventional to Amplifier with Active Load Amplifier. This chapter also explain how bulk driven amplifier are used to furthur increase the gain and decrease the power consumption by a large factor.

2.1 Introduction:

The differential amplifier is a critical analog circuit that selectively amplifies the voltage difference between two input signals while effectively suppressing common-mode voltages. As a foundational component, it serves as the core building block for key analog systems including operational amplifiers, precision instrumentation amplifiers, and high-performance data converters. The basic configuration consists of two transistors (or op-amps) sharing a common emitter (or source), with each receiving one of the input signals. The circuit then outputs a voltage proportional to the difference between the two inputs. The amplifier's suppression of common-mode signals (identical in-phase inputs) is measured by its Common-Mode Rejection Ratio (CMRR), a critical specification for differential amplification performance. High CMRR is desirable, as it indicates the amplifier's ability to suppress noise and interference common to both inputs.

Differential amplifiers are widely used in applications where accuracy and noise immunity are crucial. One of their primary uses is in sensor signal processing, where they extract small differential signals from noisy environments.

For example, in biomedical instruments like ECG or EEG machines, they amplify microvolt-level signals from the body while rejecting ambient electrical noise. Another significant use is in communication systems, where differential signaling minimizes electromagnetic interference and crosstalk, improving data integrity. They also play a critical role in analog computing, audio electronics, and control systems, and are embedded in the input stages of op-amps for balanced signal handling.

They offer high noise immunity due to their common-mode rejection, making them ideal for use in environments with significant electrical interference. Their ability to amplify small differential signals while ignoring large common signals ensures high accuracy and signal fidelity. In addition, they are compatible with balanced transmission lines, which are standard in professional audio and data transmission, allowing for longer cable runs without signal degradation. Moreover, the symmetrical design of differential amplifiers contributes to temperature stability and drift minimization. In summary, differential amplifiers are crucial components in modern electronics, valued for their precision, reliability, and robustness in handling small signals in noisy environments.

2.2 Traditional CS Differential Amplifier:

The differential common-source amplifier serves as a foundational analog circuit, extensively employed in operational amplifiers, data conversion systems, and RF front-end designs. It consists of two identical MOSFET transistors configured in a differential pair, with their sources connected together and biased by a constant current source. The drains of each transistor are connected to load resistors (or active loads like current mirrors), and the gates receive the differential input signals.

One gate gets the input signal V_{in+} while the other receives V_{in-}. Amplification of differential of these 2 voltages - two input signals, outputting the result as a differential signal at the drains. The term "common-source" refers to the fact that the sources of the two transistors are tied together, creating a shared node that connects to the tail current source, which provides a constant current regardless of the differential input.

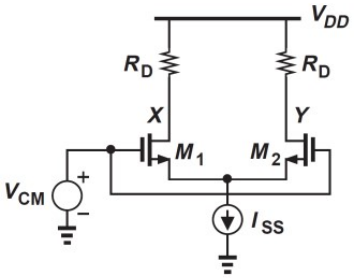


Fig.2.1: Differential Amplifier

$$V_X = V_Y = V_{DD} - \frac{R_D I_{SS}}{2}$$

$$(Vgs - Vth)_{equil.} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

To keep both transistors M_1 and M_2 in the saturation region, requirement,

$$V_{DD} - R_D \frac{I_{SS}}{2} > V_{CM} - V_{th}$$

It can be seen that when a change is given in V_{CM}, both current in node X and Y are same, i.e. $ID_1 = ID_2 = I_{SS}/2$, putting Voltages at node X and Y untouched. The circuit thus rejects Common Mode changes in Input.

Now circuit's behavior for a small input difference

$$\Delta ID1 = gm\Delta V$$

$$\Delta ID2 = -gm\Delta V$$

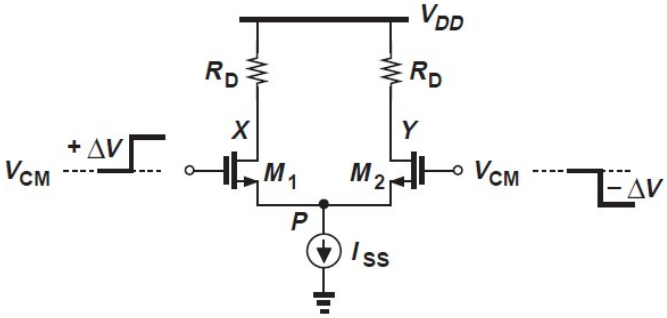


Fig.2.2: Differential Small Variation in both inputs

$VX - \Delta VY = -2gmRD\Delta V$

Differential voltage gain is given by,

similar to Normal Voltage Gain, $Av = -g_m R_D$, i.e.,

$$\frac{\mathrm{v}_{out1} - \mathrm{v}_{out2}}{v_{in1} - v_{in2}} = - g_m R_D$$

One of the most important advantages of this configuration is its ability to reject common-mode noise — signals or interference that are present equally on both inputs. This noise rejection is called as the CMRR, which is ideally infinite. The differential amplifier's inherent rejection mechanism cancels any noise appearing equally at both inputs, responding exclusively to the inter-terminal voltage difference. For instance, power supply fluctuations or EMI that affect both inputs similarly will not impact the output, assuming perfect symmetry and matching in the circuit. The constant current source at the source node further stabilizes the operation by ensuring that any increase in current in one transistor results in an equal decrease in the other, maintaining balance and preventing distortion.

Additionally, differential CS amplifiers benefit from improved linearity and increased gain compared to single-ended configurations. The symmetry of the differential pair contributes to a more linear transfer function, and the differential nature allows for doubling of gain because the output is taken across both drains. Furthermore, they are less susceptible to threshold voltage variations and temperature drift, which often appear as common-mode effects. In real-world circuits, careful layout and design techniques such as common-centroid placement and device sizing can mitigate mismatches. In summary, the traditional differential CS amplifier is a noise-resistant, high-gain, and versatile circuit that forms the core of many precision analog systems, primarily because of its superior common-mode noise rejection.

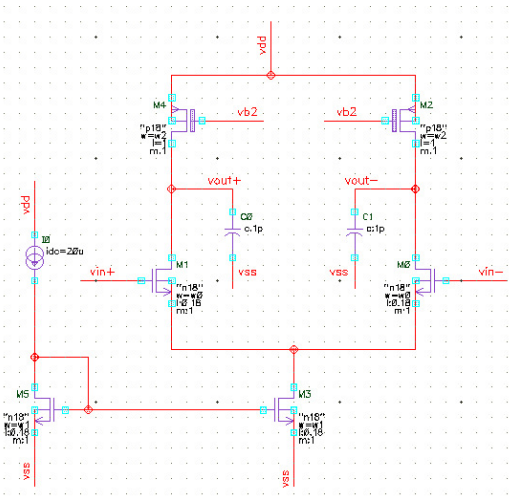


Fig.2.3: Traditional Differential CS Amplifier Cadence Simulation

VDD = 1.8 V

V_{CM} (Both Inputs) = 650 mV

Vb2 = 1.25 V

$(W/L)_{M2,\ M4}$ = 14 µm/1 µm

$(W/L)_{M0,\ M1}$ = 3 µm/0.18 µm

$(W/L)_{M3,\ M6}$ = 6 µm/0.18 µm

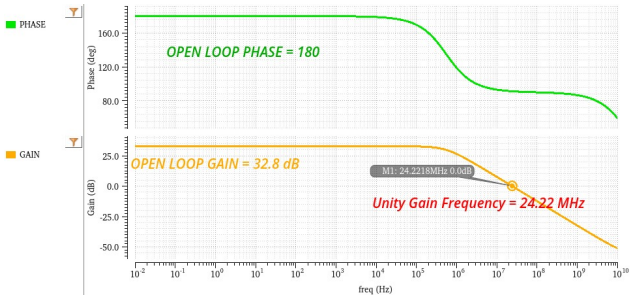


Fig.2.4: Gain and Phase Plot of Differential CS Amplifier

$$|A_v| = -\frac{g_{m0,1}}{g_{ds0,1} + g_{ds2,4}}$$

2.3 Differential Amplifier with Active Load:

A differential amplifier with an active load is a refined version of the conventional differential amplifier that significantly enhances performance by replacing the resistive load with an active device, typically a current mirror or a MOSFET configured as a high-impedance load. In the basic differential amplifier, two transistors receive input signals and share a common emitter or source terminal, with load resistors on each collector or drain. However, the use of resistive loads limits the gain and consumes more voltage headroom.

By contrast, an active load provides a much higher output resistance, which in turn increases the voltage gain substantially. The active load, often implemented using a current mirror, not only allows for more efficient use of voltage swing (especially in low-voltage operations) but also improves CMRR, a critical parameter in analog systems.

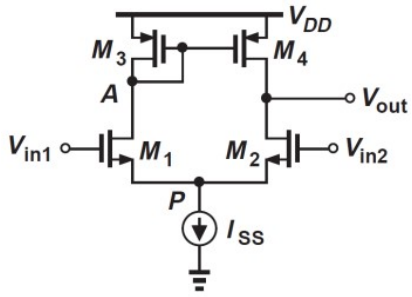


Fig.2.5: Differential Amplifier with Active Load

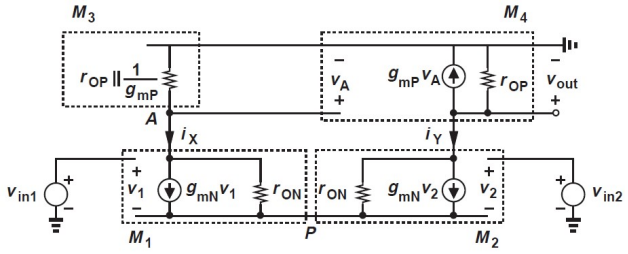


Fig.2.6: Small Signal Model of Amplifier

$$\frac{v_{out}}{v_{in1} - v_{in2}} = - g_{mN}(r_{oN} || r_{oP})$$

The use of active loads in differential amplifiers is common in modern CMOS integrated circuits because it allows designers to achieve higher gain within smaller silicon area and with lower power consumption. In this configuration, the current mirror not only acts as a load but also replicates and balances the current flowing through the differential pair, enhancing the circuit's symmetry. This directly converts to a better rejection of common-mode signals, which is crucial in noise-sensitive applications such as sensor interfaces, analog front ends, and operational amplifier input stages.

One of the primary advantages of active load differential amplifiers over conventional ones is the significantly higher gain. Differential amplifiers achieve significantly higher gain through active loads, as their superior output resistance amplifies the transconductance-dependent gain relationship compared to resistive loads. Additionally, active loads consume less voltage headroom than resistors, making them suitable for low-voltage operations—a critical factor in today's low-power, battery-operated devices. They also enhance CMRR and power efficiency, making the amplifier more robust against interference and ideal for use in precision analog circuits. Furthermore, active loads contribute to better linearity and greater integration flexibility, as they can be fine-tuned with biasing circuits and adapt to varying operating conditions.

2.4 Cascode Amplifiers:

Cascode stages are introduced in MOS amplifier design to overcome several limitations of single-stage amplifiers, particularly in terms of gain, bandwidth, and output resistance. The conventional common-source MOSFET amplifier faces inherent gain-bandwidth and output resistance limitations. The cascode topology overcomes these constraints by stacking a CG stage atop the CS configuration, significantly improving both gain and output impedance. This arrangement significantly increases the output resistance, which in turn leads to higher voltage gain. As a result, cascode amplifiers offer a much wider bandwidth compared to single-stage amplifiers.

Cascode structure improves the frequency response of the amplifier by maintaining a relatively constant drain voltage on the input transistor, reducing distortion and improving linearity. This constant drain voltage helps maintain a steady transconductance and minimizes variations due to channel-length modulation.

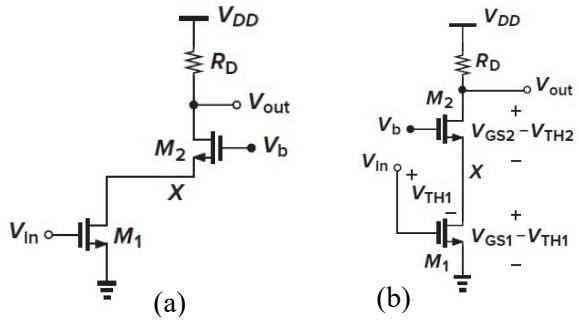


Fig. 2.7: Cascode Stage and voltage levels

$$Vout \geq Vin - V_{TH1} + V_{GS2} - V_{TH2} = (V_{GS1} - V_{TH1}) + (V_{GS2} - V_{TH2})$$

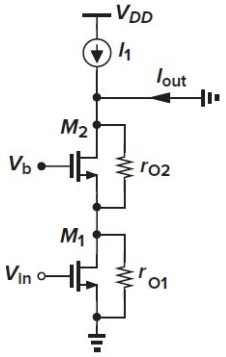


Fig.2.8: Cascode Stage with Channel Length Modulation

$$|A_v| = G_m R_{out} = g_{m1} r_{o1} [(g_{m2} + g_{mb2}) r_{o2} + 1]$$

Another important advantage of cascode amplifiers is their improved isolation between the input and output, which enhances stability and prevents unwanted feedback. In IC design, where layout area is at a premium and high-performance analog blocks are needed, the cascode configuration becomes even more attractive due to its ability to deliver high gain without resorting to large passive components.

2.4.1 Self Cascode Amplifiers:

Compared to conventional MOSFETs with identical geometries, SCMOS devices demonstrate superior transconductance and output resistance. This eliminates the traditional MOSFET trade-off requiring long channels for high gain and short channels for high-speed operation. With the same channel length as that of regular MOSFET, an SCMOS will give a higher gain without compromising the speed.

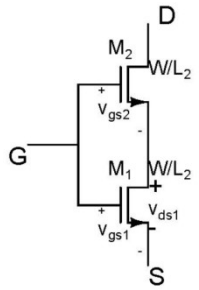


Fig.2.9: Self Cascode Structure

A self-cascode MOS [23], also known as a regulated cascode, is a transistor configuration where a single MOSFET is effectively split into two series-connected transistors (typically of the same type, either nMOS or pMOS) with their gates connected in a self-biasing manner. This structure mimics a cascode configuration but eliminates the need for an external bias voltage, making it more efficient in certain applications. The self-cascode arrangement enhances key performance parameters such as output resistance, voltage gain, and power supply rejection while maintaining simplicity in design.

The bottom transistor (M1) of self Cascode configuration is biased at a fixed gate voltage (Vb), while the top transistor (M2) has its gate connected to its own drain, creating a diode-like connection with local feedback. This feedback mechanism regulates the drain voltage of M1, ensuring stable operation and improved output characteristics. The self-cascode structure inherently increases the output impedance compared to a single transistor, similar to a traditional cascode, but with a more compact biasing scheme. Operational Transconductance Amplifiers (OTAs) require high gain, high output impedance, and good linearity for effective signal processing.

2.5 Partial Postive Feedback:

Partial positive feedback is a circuit technique where a fraction of the output signal is fed back in phase with the input, intentionally increasing gain and signal amplification. In MOS devices, this is implemented by carefully coupling the output of a transistor stage back to its input or a related node in a way that reinforces the signal without causing full oscillation. [2]

Partial positive feedback is controlled to enhance performance metrics such as gain, bandwidth, or impedance without pushing the circuit into saturation. In a MOSFET-based amplifier, partial positive feedback can be introduced through a resistive or capacitive network that feeds a portion of the drain signal back to the gate or source terminal. For example, in a common-source amplifier, a small resistor between the drain and gate can create a controlled regenerative effect, boosting the effective g_m and output resistance (Fig.2.10).

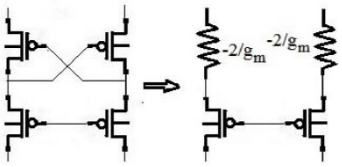


Fig.2.10: Partial Poitive Feedback Cicuit

One key application of partial positive feedback is in improving the gain and linearity of OTA. By carefully tuning the feedback factor, designers can enhance the open-loop gain without significantly compromising stability. Partial positive feedback have a trade-off between performance enhancement and risk of instability. Despite its limitations, partial positive feedback remains a valuable, especially in high-speed and low-power applications. When properly implemented, it allows MOS-based circuits to achieve higher gain-bandwidth products and better noise performance compared to conventional negative feedback topologies. However, designers must carefully balance the feedback ratio to avoid undesirable effects such as ringing or signal distortion.

2.6 Miller Compensation Circuit:

Miller compensation is a widely used technique in op-amps and other feedback circuits to improve stability by controlling frequency response and preventing unwanted oscillations.

It involves placing a capacitor between the input and output of an inverting gain stage, exploiting the Miller effect [2, 18] to effectively increase the capacitance seen at the input node.

This method is particularly useful in multi-stage amplifiers, where high gain and bandwidth can lead to phase margin degradation. The Miller effect states that a capacitor (C) connected between the input and output of an inverting amplifier with gain (-A) appears as a much larger effective capacitance at the input. The effective input capacitance becomes: $C_{eff} = C(1 + A)$. This artificially increases the time constant at the dominant pole, pushing it to a lower frequency while keeping the physical capacitor small. As a result, the amplifier's phase margin improves, reducing the risk of instability.

A typical Miller compensation setup in a two-stage op-amp consists of:

1. Differential Input: A differential pair with high gain.
2. Common-Source/Gain Stage: Provides additional amplification.
3. Compensation Capacitor (Cc): Connected between the output of the second stage and the high-impedance node (first-stage output).

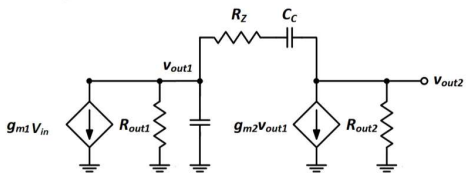


Fig.2.11: Small Signal Model - Miller Compensation

The main goal is to move the dominant pole (the frequency at which gain starts to drop) by introducing Cc to a lower frequency where $f_{dominant} = \frac{1}{2\pi R_{out1} C_{eff}}$, where $C_{eff} = C_c(1 + A_2)$, and A_2 is the gain of the second stage, ensuring the system becomes a single-pole system over the frequency range of interest. This prevents excessive phase shift at the unity-gain frequency, which could otherwise cause positive feedback and instability.

The Miller effect significantly increases the effective capacitance seen at the input of the second stage, thus lowering the pole frequency. The Miller capacitor also pushes the non-dominant pole (originally from the second stage) to a higher frequency, improving phase margin.

This helps create a large separation between the dominant pole and the higher-frequency poles, improving phase margin and stability.

Advantages of Miller Compensation

- Area Efficiency: A small physical capacitor provides a large effective capacitance.
- Improved Phase Margin: Reduces peaking and ringing in transient response.
- Widely Applicable: Works well in multi-stage amplifiers like op-amps.

Disadvantages & Mitigations

- Reduced Bandwidth: The dominant pole lowers the amplifier's bandwidth.
- Right-Half-Plane (RHP) Zero: The compensation capacitor can introduce a zero that degrades phase margin. To mitigate this, use of a nulling resistor (Rz) in series with Cc.

2.7 Reverse Nested Miller Compensation Circuit:

In three-stage amplifier configurations where solely the intermediate stage provides signal inversion, RNMC establishes itself as the most effective frequency stabilization method. This sophisticated compensation topology specifically addresses the bandwidth constraints and right-half-plane zero complications inherent to conventional Miller approaches. By enabling more deliberate pole-zero positioning, RNMC maintains exceptional phase margin while delivering wide frequency response characteristics - critical advantages for modern high-performance OTA requiring both substantial gain and rapid signal processing capabilities.

The RNMC scheme typically employs three gain stages:

- First Stage (Input Stage): A transconductance stage (gm1)
- Second Stage (Intermediate Stage): A second transconductance stage (gm2)

- Third Stage (Output Stage): A buffer or additional gain stage (gm3)

The compensation network consists of:

- Primary Compensation Capacitor (Cm1): Connected between output and first stage
- Secondary Compensation Capacitor (Cm2): Connected between output and second stage

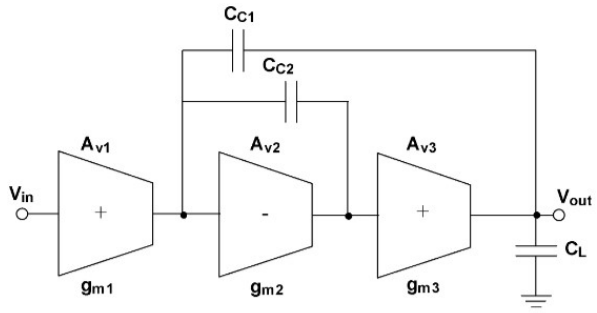


Fig.2.12: Block Diagram of RNMC

The RNMC technique strategically modifies the amplifier's frequency response:

Dominant Pole (ωp1): Created at the output node by Cm1 through Miller effect

ωp1 ≈ 1/(gm2·gm3·Ro1·Ro2·Ro3·Cm1)

Pushed to very low frequency for stability

Non-Dominant Poles:

ωp2 ≈ gm2/Cm2

ωp3 ≈ gm3/CL (where CL is load capacitance)

These are pushed to higher frequencies compared to simple Miller compensation

Zeroes:

The structure naturally creates left-half-plane (LHP) zeroes

ωz1 ≈ gm2/Cm2 (beneficial for phase margin)

Avoids problematic RHP zeroes found in standard Miller compensation

Advantages Over Conventional Compensation

1) Better Stability: Provides more than 60° phase margin even with large load capacitors. Maintains stability across wider range of operating conditions

2) Improved Bandwidth: The nested structure allows higher unity-gain frequency. Achieves GBW up to 70-80% of the non-compensated amplifier

3) Power Efficiency: Doesn't require large compensation capacitors. Minimizes the need for additional power-hungry buffer stages

4) Load Insensitivity: Performance remains stable with varying load conditions. Particularly useful for driving large capacitive loads

Parameter	RNMC	NMC	Simple Miller
Phase Margin	$> 60^0$	$\sim 50^0$	$< 45^0$
GBW	High	Medium	Low
Power	Medium	High	Low
Complexity	High	Medium	Low
Load Drive	Excellent	Good	Poor

Table 2: Difference Table for Different Miller Configurations over the years

RNMC represents a polished solution for stabilizing multi-stage OTAs without sacrificing bandwidth or power efficiency. By intelligently arranging compensation capacitors and leveraging multiple gain stages, RNMC provides superior control over pole-zero positions compared to conventional techniques. While more complex to design, its benefits make it the preferred choice for high-performance amplifier applications where stability, speed, and load-driving capability are crucial requirements.

Chapter 3

Bulk Driven and Class-AB

4.1 Bulk-Driven Amplifier:

Bulk-driven amplifiers [7-10, 17] represent an innovative MOSFET configuration where the input signal couples to the transistor's bulk terminal instead of the conventional gate input. This architecture enables unprecedented low-voltage operation, functioning reliably below the device threshold voltage - a critical advantage for ultra-low-power analog designs. In operation, the gate maintains a fixed bias voltage to preserve channel formation while the bulk terminal modulates the threshold voltage to control drain current. This unique threshold voltage modulation mechanism permits practical implementation of analog circuits at supply voltages ≤0.5V, overcoming fundamental limitations of traditional gate-driven approaches. The technique proves particularly valuable in energy-constrained applications requiring sub-threshold operation without compromising signal integrity.

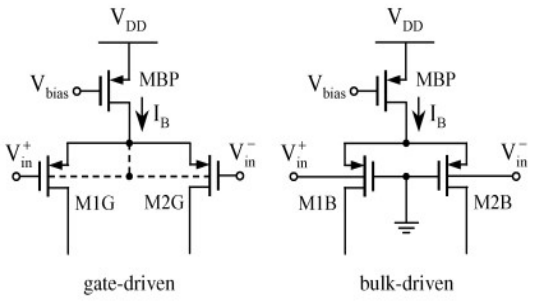


Fig.3.1: Difference between Gate-Driven and Bulk-Driven Amplifier Configuration

$$I_{ds} = I_s * \ W/L * \ \exp(qV_{gs} - V_{th}/nkT) * \ [1 - \exp(-qV_{ds}/kT)]$$

$$V_{th} = V_{th0} - \lambda_{DS}V_{DS} - \lambda_{BS}V_{BS}$$

The advantages of bulk-driven amplifiers are particularly evident in low-power and low-voltage environments. First and foremost, they eliminate the threshold voltage limitation, allowing the circuit to operate with a wider input signal range even when the supply voltage is close to or below the transistor's threshold. This enables enhanced functionality in low-power systems, such as implantable medical devices, wearable electronics, and energy-harvesting systems. Additionally, bulk-driven transistors are compatible with standard CMOS processes, requiring no additional fabrication steps, which is economically and technically advantageous. They also exhibit good common-mode rejection and are suitable for fully differential architectures, making them ideal for sensor front-ends.

The main drawback for bulk-driven amplifiers is their lower transconductance compared to gate-driven devices. This results in reduced gain and bandwidth, limiting their performance in high-speed or high-precision applications. Moreover, the body effect, which causes variations in threshold voltage due to changes in source-bulk voltage, can lead to nonlinearity and reduced predictability.

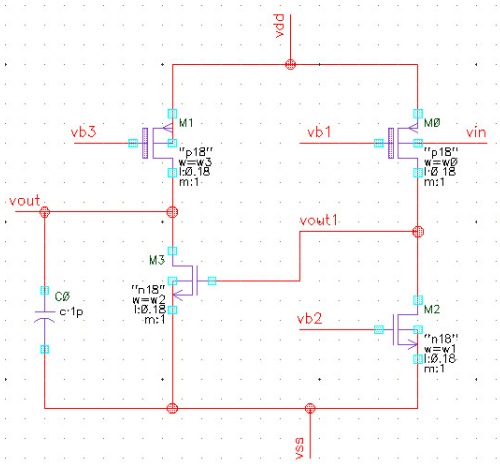


Fig.3.2: Cadence Simulation result for Bulk-driven with 2nd stage as CS amplifier with Current Source Load

V_{DD} = 1 V
W/L_{M0} = 11 µm/ 0.18 µm

$$A_v = \frac{g_{mb0}g_{m3}}{(g_{ds0} + g_{ds2})(g_{ds1} + g_{ds3})}$$

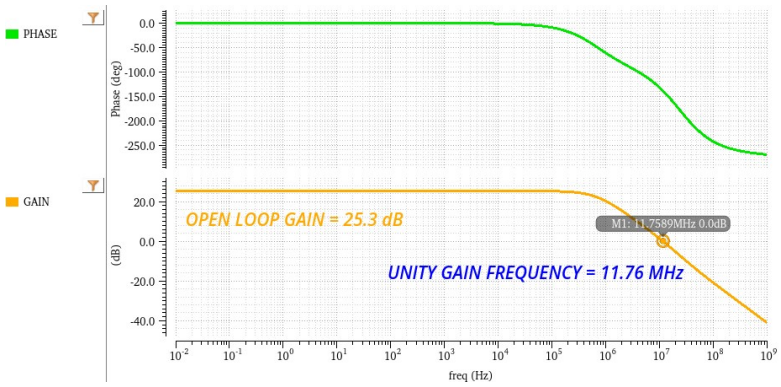


Fig.3.3: Gain and Phase Plot of Bulk-Driven Amplifier

Applications of bulk-driven amplifiers include ultra-low-power analog front ends in biomedical instrumentation, such as ECG and EEG monitors, sensor interface circuits, portable electronics, and Internet of Things (IoT) devices. They are also used in low-voltage operational amplifiers, signal conditioning circuits, and energy-efficient analog computation systems. Their ability to function reliably under minimal power makes them invaluable in designing the next generation of power-sensitive electronics.

4.2 Class-AB Amplifier:

Class AB amplifiers combine the advantages of Class A and Class B topologies, achieving an optimal trade-off between linearity, efficiency, and distortion. Unlike Class A amplifiers that conduct continuously (360° operation) for superior linearity but poor efficiency, or Class B designs that operate for half-cycles (180°) with improved efficiency but crossover distortion, the Class AB configuration maintains partial conduction during zero-crossing transitions. This hybrid approach minimizes crossover artifacts while preserving reasonable power efficiency, making it particularly suitable for applications demanding both signal fidelity and energy conservation. Class AB resolves this by ensuring that both output transistors conduct slightly more than 180°, typically around 200°–220°, allowing for smoother transitions and significantly reduced distortion while still maintaining better efficiency than Class A.

In modern LPOTA, the Class AB configuration [3, 18, 20] is widely adopted due to its ability to provide high output swing, moderate to high slew rates, and improved power efficiency, which are critical in battery-operated and portable devices. LPOTAs are frequently used in sensor front-ends, biomedical instruments, and analog signal processing blocks within integrated systems. The Class AB architecture allows for adaptive current sourcing: the amplifier operates in a low-power idle state during low-signal conditions and automatically increases its output current capability when larger signals are present, without needing continuous high bias currents.

In low-voltage CMOS technologies, implementing Class AB OTAs poses challenges, as the available headroom is limited. To counter this, techniques such as bulk-driven input stages, floating-gate techniques, and transistor stacking with level shifters are used. A common Class AB OTA structure involves a differential input stage with transconductance enhancement, followed by push-pull output stages that provide rail-to-rail output swing and improved current driving capabilities. There are various types of Class AB amplifier designs, each tailored for specific application constraints and performance targets given in below table:

Type of Class-AB	Key Features	Use Cases
Traditional	Push-pull, moderate power	General-purpose OTAs
Floating	Ultra-low power	Low-voltage biomedical designs
Adaptive Biasing	Dynamic current control	Power-efficient amplifiers
Rail-to-Rail	Full swing, constant transconductance	Low-voltage analog front ends
Current Mode	Current domain operation	High-speed filters and converters
Level Shifters	Cross-voltage stage compatibility	Deep submicron CMOS OTAs

Table3: Features and Use cases of Class-AB Amplifiers

Chapter 4

Results from Cadence Simulation

This section includes the cadence Simulation performed on SCL 180 nm Technology and results were genereted with the listed Yearwise Research Papers to show the trend of different OTA configurations over the years and verified the results with the same.

4.1 Source Degenerated BD-OTA [24]

Using the Miller compensated Amplifier to ensure stability at output stage.

Application: Designing of an anti-aliasing Gm-C filter for band limiting.

$$Av = \frac{Gm}{gm\,(N7)} * \frac{kGm}{gds1 + gds0}$$

where $k = \frac{(W/L)\,N8}{(W/L)\,N7}$, $Gm = \frac{gm1(2n-1)}{1 + Rs * gm1(2n-1)}$

Specification as per the requirement of OTA:

Supply, V_{DD} = 0.5V
DC Gain, A_v = 43 dB
Power Consumption = 146 nW
Gain-Bandwidth = 90 kHz

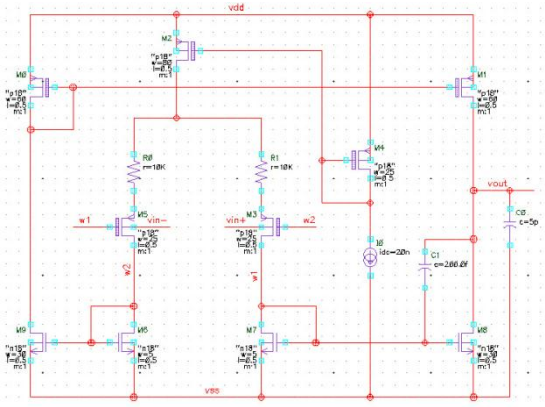


Fig.4.1: Circuit Schematic of OTA [24]

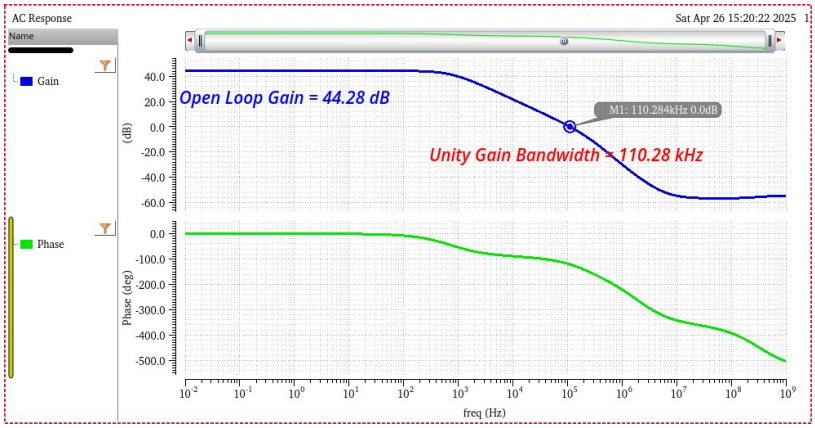


Fig.4.2: Gain and Phase Plot of OTA [24]

4.2 Gain Amplification of 3-Stage CMOS OTA [20]

High performance bulk-driven 3-stage OTA working at 0.7 V_{DD}, and providing adequate DC gain for a subthreshold OTA. This circuit has used lastly a Class-AB amplifier topology that works on less than 1-V Supply. This Amplifier is a 3-Stage Nested Miller Compensated OTA where C_{C1} = 550 fF and C_{C2} = 30 fF. Dominant Pole is achieved by the use of capacitor-C_{C1}.

The use of resistors R (Fig.4.3) in the active load of the input stage enables fully differential operation of an pseudodifferential pair. This resistor Pair also works for increasing CMRR. We can see the working of Class AB Part. The output stage provides unconstrained maximum signal current capability, free from DC biasing limitations. The nMOS transistor (M6) operates in common-source configuration, while the pMOS device (M5) exhibits current enhancement with rising Vin+ due to corresponding increases in Vgs(M10).

Specification as per the requirement of OTA:

Supply, V_{DD} = 0.7V

DC Gain, A_v = 57 dB

DC Current Supply = 4 µA

Gain-Bandwidth = 3 MHz

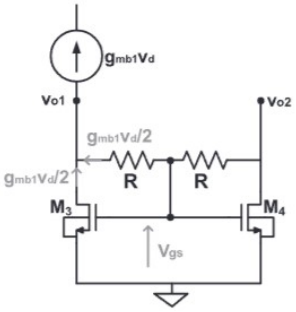


Fig.4.3: Differential Input Stage of pseudodifferential pair.

$$A(s) \approx A_0 \frac{1+\frac{s}{z_1}}{\left(1+\frac{s}{p_1}\right)(as^2+bs+1)}$$

$$A_0 = \frac{g_{mb1,2} g_{m5} g_{m7} (R//r_{o1}) r_{o2} r_{o3}}{2}$$

$$p_1 = \frac{2}{g_{m5} g_{m7} (R//r_{o1}) r_{o2} r_{o3} C_{C1}}$$

$$z_1 = \frac{g_{m5} g_{m3}}{2C_{C1} g_{m5} - C_{C2} g_{m3}}.$$

$$a = \frac{C_{C2} C_L (2g_{m5} + g_{m3})}{g_{m3} g_{m5} g_{m7}}$$

$$b = \frac{C_{C1} C_L + C_{C2} C_L g_{m5} r_{o2}}{C_{C1} g_{m5} g_{m7} r_{o2}}.$$

Fig.4.4: Voltage Gain and its poles and zeroes

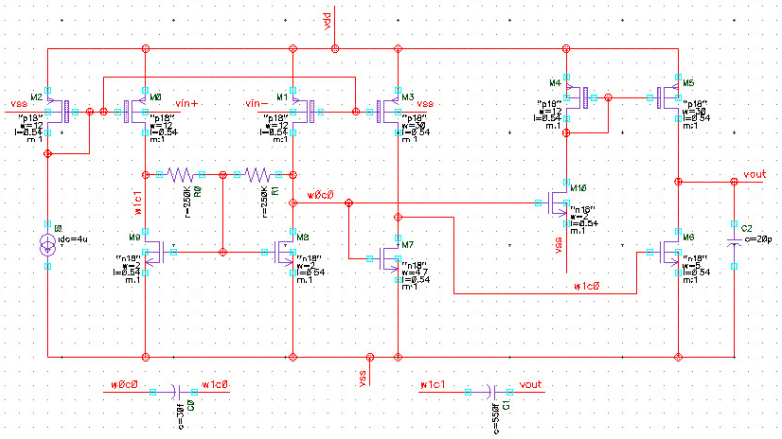


Fig4.5: Circuit Schematic of OTA [20]

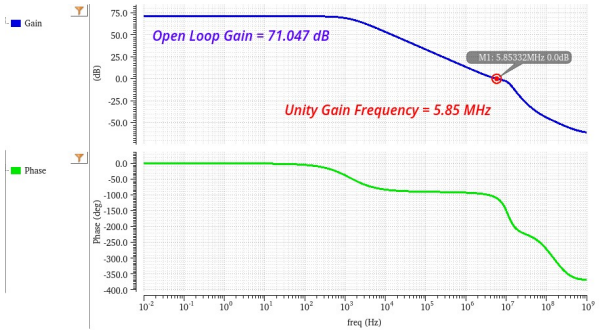


Fig4.6: Gain and Phase Plots of OTA [20]

4.3 Further OTA working in 0.3-V Supply [6]

Class AB power-efficient ULV structure where M5–M7 form a class-AB output stage with M8. Use of Feed-Forward Path by the OTA through the path of M3, M5, M6 and M7 which Removes the Zero of the system and introduces Stability. Rail-to-Rail ICMR achieved for the system and Larger CMRR. Power Simulation results in ~10nW.

Specification as per the requirement of OTA:

Supply, V_{DD} = 0.3V

DC Gain, A_v = 64.7 dB

Power Consumption = 12.6 nW

DC Current Supply = 5 nA

Gain-Bandwidth = 2.96 kHz

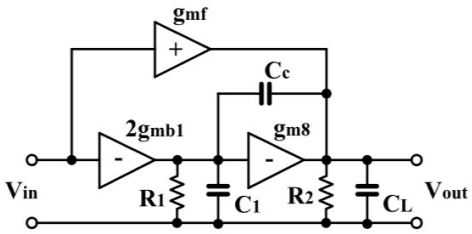


Fig.4.7: Block Diagram of the OTA

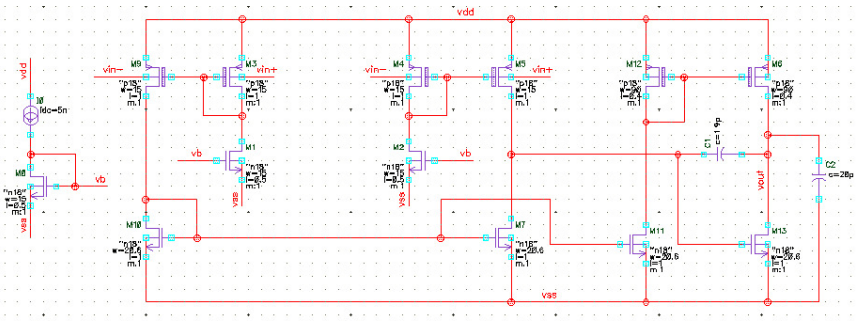


Fig.4.8: Circuit Schematic of OTA [6]

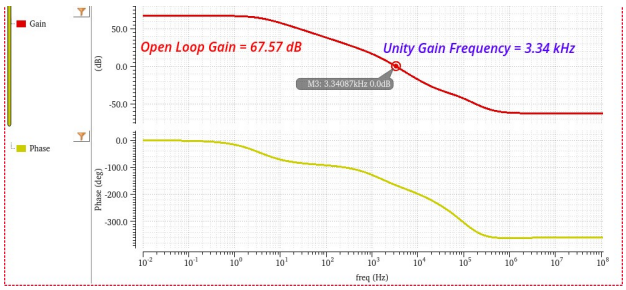


Fig.4.9: Gain and Phase Plots of the OTA [6]

4.4 3 Gain Stages of Class-AB Amplifiers [22]

The design implements a three-stage topology employing Reverse Nested Miller Compensation (RNMC) without nulling resistors. The input stage features a novel bulk-driven differential pair operating without tail current sources, while subsequent stages maintain the RNMC compensation network to ensure stability across the full operational bandwidth. This configuration achieves optimal frequency response while preserving the ultra-low-voltage advantages inherent to bulk-driven input stages.

Specification as per the requirement of OTA:
Supply = 0.3 V
DC Gain = 98 dB
Power Consumption = 13 nW
Gain-Bandwidth = 3.1 kHz

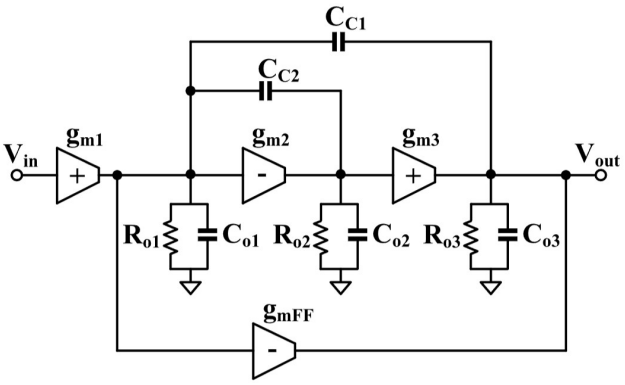


Fig.4.10: Block Diagram of OTA

DC Voltage Gain :

$$A_{v0} \approx - g_{m1}R_{o1}g_{m2}R_{o2}g_{m3}R_{o3}$$

$$p1 \approx - \frac{1}{R_{o1}g_{m2}R_{o2}g_{m3}R_{o3}C_{C1}}$$

$$\omega_{GBW} = \frac{g_{m1}}{C_{C1}}$$

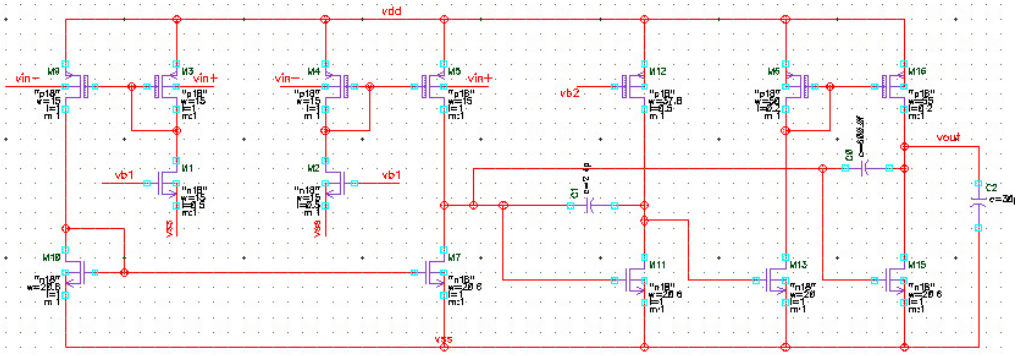


Fig.4.11: Circuit Schematic of OTA [22]

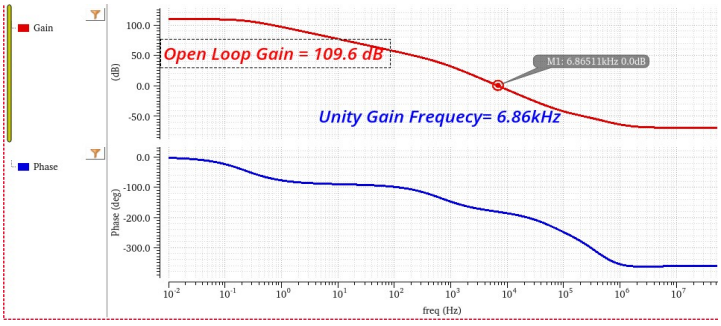


Fig.4.12: Gain and Phase Plots of OTA [22]

4.5 BD-OTA using Self-Cascode Structure [23]

This design operates at VDD = VTH = 0.5V using Partial Positive Feedback (PPF) to enhance stability. By introducing negative conductances at M2A/M2B's drain-gate nodes, PPF boosts nodal resistance and differential gain without affecting common-mode gain or VDD sensitivity. The self-cascode output stage increases output resistance beyond single-transistor limits, maintaining performance at minimal supply voltages.

Specification as per the requirement of OTA:

Supply = 0.5 V

DC Gain = 54.7 dB

Power Consumption = 31.3 nW

Gain-Bandwidth = 6.18 kHz

$$A_{v0} = \frac{g_m}{g_{ds1}+g_{ds6}}$$

Where $g_m = 2g_{mb1}\frac{1+p/2}{1-m+p}$

Where $m = g_{m7,8}/g_{m2}$

And $p = (g_{ds2} + g_{ds7,8} + g_{ds3,4})/g_{m2}$

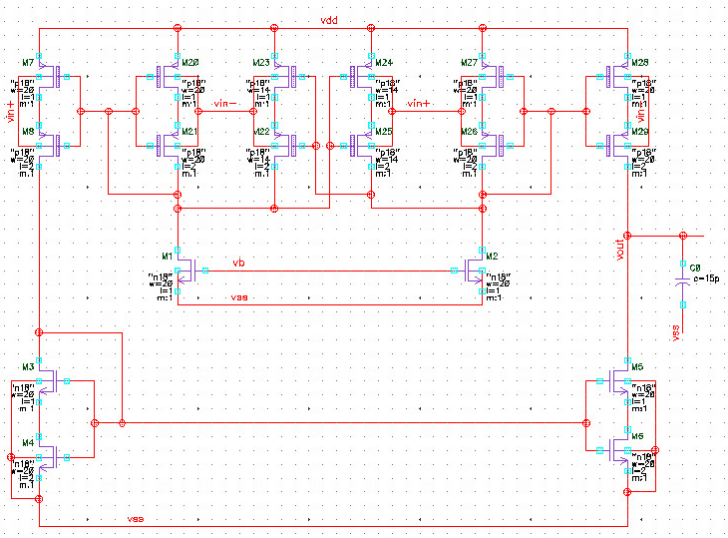


Fig.4.13: Circuit Schematic of OTA [23]

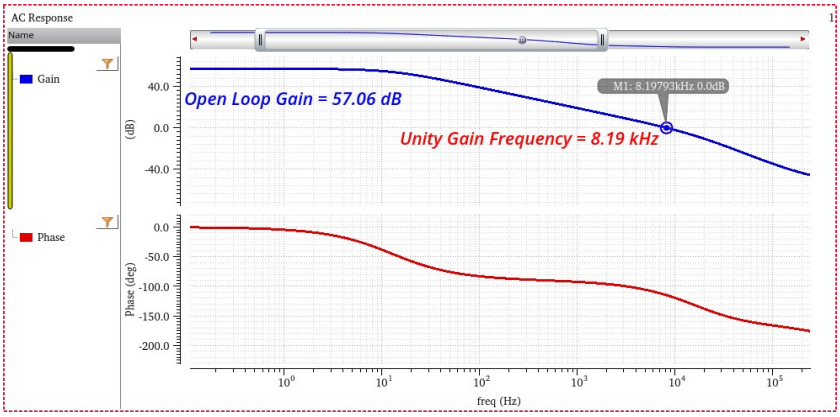


Fig.4.13: Gain and Phase Plots of OTA [23]

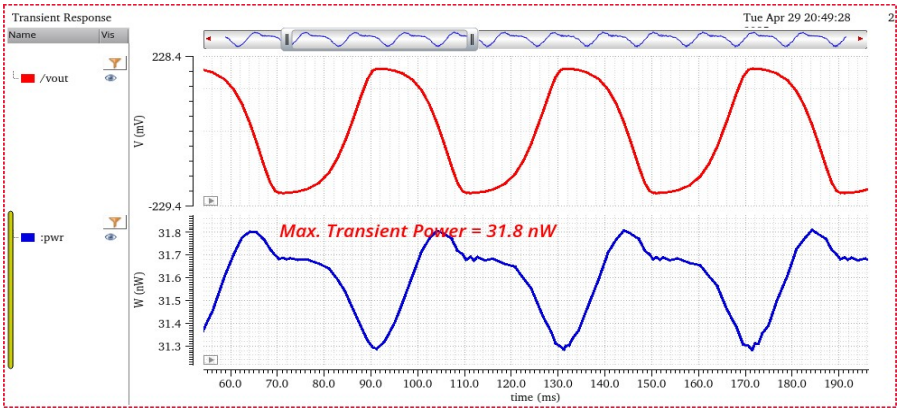


Fig.4.13: Power Consumption of OTA [23]

Chapter 5

Conclusion and Future Scope

5.1 Conclusion:

The goal of this project was to design and test a low-power OTA using proven analog techniques—something that could work well in today's energy-sensitive applications. We focused on a classic Class-AB amplifier design but gave it a few key upgrades: Miller compensation to boost frequency stability and bandwidth, plus a nulling resistor in the compensation network to sharpen the phase margin. These tweaks made the amplifier more reliable, even when driving heavy capacitive loads.

We also looked into adding an active feedforward network to boost the dynamic response—without burning extra power. This hybrid approach gave us the best of both worlds: better speed and linearity, all while keeping idle power draw low. And since we built the whole thing in standard 180nm CMOS, it stays cost-effective and easy to manufacture.

Beyond just running simulations, we also dug into the math—using small-signal modeling to break down the circuit's behavior. By deriving the gain and frequency response theoretically, we could double-check our simulation results and really understand how the OTA was behaving. This combo of hands-on simulation and pencil-and-paper analysis gave us a complete picture of performance, from gain and bandwidth to power efficiency. By carefully applying classic techniques like Class-AB biasing, Miller compensation, and feedforward tricks, we hit solid performance without burning power. It all works in standard 180nm CMOS, showing older processes still have plenty to offer for energy-efficient analog design.

5.2 Future Scope:

We've successfully designed and tested a low-power OTA using Class-AB architecture with Miller compensation and active feedforward techniques in 180nm CMOS. The results show a good balance between power efficiency, gain, and stability - but there's still room to push the boundaries even further in future work.

Adaptive biasing. Unlike traditional static biasing, this approach lets the circuit automatically adjust its bias currents based on the input signal or load - works as a smart throttle for power consumption. When things are quiet, it dials back to save energy. When activity picks up, it ramps up for full performance. Perfect for battery-powered applications like medical devices and IoT sensors, where power is useful and signals come in unpredictable bursts.

We could also take this design to more advanced nodes - think 130nm, 65nm, or even FinFET processes. That jump could give us some serious benefits: tighter layouts, less parasitic drag, wider bandwidth, and a smaller footprint. But it's not all smooth sailing - we'd be trading those gains for process variability, lower intrinsic gain, and razor-thin voltage margins. To make it work, we'd need to get clever with our design strategies and bulletproof our layout approach.

Tweaking the threshold voltages. We've got options like body biasing (forward or reverse) or mixing low-Vt and high-Vt devices - basically giving us a tuning knob to optimize for either power or speed. Further design exploration could evaluate resistive isolation techniques for differential stages and gain blocks.

This approach offers distinct advantages: enhanced linearity, reduced parasitic coupling, and stabilized bias points—all achieved through relatively simple implementation. For more demanding performance requirements, alternative architectures such as regulated cascode topologies or floating-gate OTA implementations merit investigation. These advanced configurations can deliver superior output impedance and gain characteristics while maintaining strict power efficiency constraints.

In summary, future research directions for low-power OTAs span multiple dimensions: innovative circuit techniques, advanced biasing schemes, process technology scaling, and system-level integration. These developments will be crucial for creating next-generation analog front-ends that combine power efficiency with robustness and scalability across diverse applications

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