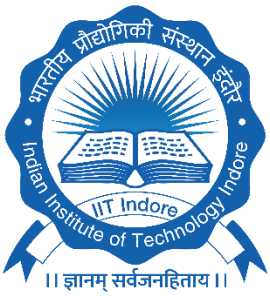
A CRITICAL ASSESSMENT OF REALIZING CAPACITORLESS DRAM WITH INNOVATIVE RECONFIGURABLE MOSFETS

Ph.D. Thesis

By
ROHIT KUMAR NIRALA



DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE

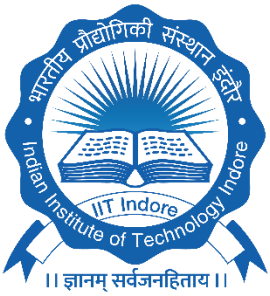
JULY 2025

A CRITICAL ASSESSMENT OF REALIZING CAPACITORLESS DRAM WITH INNOVATIVE RECONFIGURABLE MOSFETS

A THESIS

Submitted in partial fulfillment of the
requirements for the award of the degree
of
DOCTOR OF PHILOSOPHY

by
ROHIT KUMAR NIRALA



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JULY 2025

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I hereby certify that the work which is being presented in the thesis entitled **A CRITICAL ASSESSMENT OF REALIZING CAPACITORLESS DRAM WITH INNOVATIVE RECONFIGURABLE MOSFETS** in the partial fulfillment of the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY** and submitted in the **DEPARTMENT OF ELECTRICAL ENGINEERING, INDIAN INSTITUTE OF TECHNOLOGY INDORE**, is an authentic record of my own work carried out during the time period from August 2020 to July 2025 under the supervision of Dr. Abhinav Kranti, Professor, Department of Electrical Engineering, Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Rohit Kumar Nirala

21-07-2025

Signature of the student with date

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This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

21/07/2025

Signature of Thesis Supervisor with date

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Rohit Kumar Nirala has successfully given his Ph.D. Oral Examination held on November 17, 2025.

17/11/2025

Signature of Thesis Supervisor with date

ACKNOWLEDGEMENTS

My profound appreciation goes out to my Ph.D. thesis advisor, Prof. Abhinav Kranti, for giving me the chance to work in his research group at IIT Indore. I am incredibly appreciative of his advice, inspiration, patience, and criticism throughout my doctoral studies. I would like to sincerely thank my PSPC members, Prof. Prabhat Kumar Upadhyay, and Prof. Abhishek Srivastava, for their comments, helpful recommendations, and constructive criticism during the Ph.D. work.

I would like to express my sincere gratitude to the University Grants Commission, Ministry of Education, Government of India, for the award of Junior Research Fellowship (190520491384) for the entire duration of the Ph.D. program. The research infrastructure at the Department of Electrical Engineering, IIT Indore, for the Ph.D. research is gratefully acknowledged. I would also like to acknowledge the use of research infrastructure under the grant CRG/2019/002937, from the Department of Science and Technology, Government of India. The thesis work would not have been possible without the support, help and cooperation of faculty and staff members of IIT Indore.

I am deeply grateful to my present and former colleagues Nivedita, Bhuvaneshwari, Sandeep, Arghya, Keerthi, Aakash, Abu, Aman, and Devesh for their kind support during my research work. Furthermore, I extend my heartfelt gratitude to Dr. Manish Gupta, BITS Pilani, K K Birla Goa Campus, Goa, for discussions and support on the research work and simulation tool.

I dedicate this work to the loving memory of my parents, Late Mr. Satyendra Narayan Singh and Late Mrs. Mina Singh, whose values and blessings continue to guide and inspire me every day. My deepest gratitude to my elder brother, Mr. Rahul Kumar Nirala, and my sister-in-law, Mrs. Laxmi Singh, for their care, and encouragement, and to my wife, Mrs. Manisha Singh, for her unwavering support. The smiles of my nieces, Aishani and Avani, and my nephew, Ayansh have been a constant source of motivation and joy throughout this journey.

Lastly, I wish to express my profound gratitude to the Almighty, who has bestowed upon me life, faith, and the ability to navigate through this crucial phase of my journey.

Rohit Kumar Nirala

In the Loving Memory of My Parents

ABSTRACT

A CRITICAL ASSESSMENT OF REALIZING CAPACITORLESS DRAM WITH INNOVATIVE RECONFIGURABLE MOSFETS

The evolution of transistor architecture from conventional planar to three-dimensional vertical nanosheet or nanowire coupled with innovation through low power Silicon-on-Insulator (SOI) technology has largely contributed to enhancing transistor density in modern chips. Despite critical innovations in transistor architecture and reduction of parasitic components, a fundamental limitation of Complementary Metal Oxide Semiconductor (CMOS) technology is the requirement of separate n-type and p-type transistors to implement logic circuits. If the polarity (type of transistor) could be obtained through bias in the same structure (device) then separate transistors would not be needed for implementing logic circuits. A three gated (3-gated) reconfigurable MOSFET, also known as reconfigurable field effect transistor (RFET), permits selective carrier injection through modulation of metal-semiconductor (M-S) Schottky contact with an additional gate for channel control.

The possibility of showcasing single transistor (1T) capacitorless (0C) dynamic random access memory (DRAM) through RFET adds to the multifunctional capability of the architecture. The 3-gated RFET is ideal for 1T-DRAM as it facilitates the storage of generated holes in the semiconductor film underneath the control gate (CG). A higher positive (negative) voltage at the polarity gate (PG) causes band bending, and subsequent tunneling of electrons (holes) to the semiconductor which transforms the region underneath PG to function as pseudo source/drain. The location of pseudo source/drain regions away from the semiconductor region underneath the CG due to the presence of underlap/ungated region allows the storage of holes at appropriate biases. The feasibility assessment of implementing 1T-DRAM with RFET has been carried out through well calibrated simulations with appropriate models for capturing inherent physical phenomenon in the device.

The degradation of retention time (RT) with a change in bias is a serious concern in 1T-DRAM. This degradation is critical for 1T-DRAM with RFET due to a greater (three) number of gates. While front and back PGs can be electrically connected, the independent front and back CG

operation is required to implement 1T-DRAM through planar RFET. Therefore, the bias range able to sustain a degradation of 50% of maximum retention time (RT_{max}) in RFET based 1T-DRAM has been investigated to estimate the bias tolerance of retention time. In addition, the sensitivity of key performance metrics of 1T-DRAM on device parameters has also been evaluated.

RFET can be designed with different combinations of lengths of CG (L_{CG}) and PG (L_{PG}) and ungated region (L_{GAP}) for a fixed total length ($L_T = 2(L_{PG}+L_{GAP}) + L_{CG}$)). The storage length ($L_S = L_{CG} + 2L_{GAP}$) depends on CG and separation between PG and CG. This essentially implies that RFET could be designed with various values of L_S/L_T (with typical range of 0.4 to 0.8) for a given L_T (100 nm). Hence, the choice of optimal biases for RFET based 1T-DRAM have been ascertained as a function of L_S/L_T. In addition, the requirements of 1T-DRAM to function as on-chip (embedded) memory is different from that for standalone applications due to the requirement of fast write/read operations. An in-depth analysis in terms of write and read access times has been carried out to ascertain the feasibility of RFET for implementation as embedded 1T-DRAM.

The use of nanowire (NW) transistor architecture has been largely dictated by the progress in logic technology. Investigating the possible realization of 1T-DRAM with NW transistor architecture is crucial for using same type of transistors for logic and memory blocks. Since independent back gate operation is not possible in NW transistor, RFET serves as an ideal topology to realize 1T-DRAM. In addition to exploring 1T-DRAM functionality, the impact of word line (WL) and bit line (BL) disturbance in an array for various operations (write 1, write 0, and read) has been examined for pragmatic memory realization. The biases for 1T-DRAM are usually selected to ensure proper operations – write 1 (program), write 0 (erase), hold, and read. In an array realization, an important parameter for bias selection is array disturbance apart from feasibility of individual memory operations. Hence, bias optimization (for each operation) based on enhancing the duration of disturbance tolerance has been carried out in RFET based 1T-DRAM array.

Overall, this thesis presents a critical assessment of implementing 1T-DRAM through planar and nanowire topologies of RFET. Besides highlighting the working mechanism and device physics for implementing 1T-DRAM, the thesis has introduced fresh perspectives to enhance array retention while focusing on bias selection based on the duration of disturbance tolerance.

LIST OF PUBLICATIONS

A1. <u>In refereed Journals:</u>

1. R.K. Nirala, S. Semwal, Y.V. Bhuvaneshwari, N. Rai and A. Kranti, "Sensitivity implications for programmable transistor based 1T-DRAM", **Solid-State Electronics**, vol. 194, 108353, 2022. DOI: 10.1016/j.sse.2022.108353 (Journal Impact factor: 1.4).
2. R.K. Nirala, S. Semwal, and A. Kranti, "A critique of length and bias dependent constraints for 1T-DRAM operation through RFET", **Semiconductor Science and Technology**, vol. 37, 105013, 2022. DOI: 10.1088/1361-6641/ac8c67 (Journal Impact factor: 1.9).
3. R.K. Nirala, S. Semwal, M. Gupta, and A. Kranti, "Energy and disturbance analysis of 1T-DRAM with nanowire gate-all-around RFET", **IEEE Trans. Electron Devices**, vol. 71, pp. 2950-2956, 2024. DOI: 10.1109/TED.2024.3371950 (Journal Impact factor: 2.9).

A2. <u>In refereed Conferences:</u>

1. R.K. Nirala, S. Semwal, Y.V. Bhuvaneshwari, N. Rai, and A. Kranti, "Scalability and sensitivity assessment of programmable transistor based 1T-DRAM", 8th **Joint International EuroSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS)**, May 18-20, 2022, Accepted (Online presentation).
2. R.K. Nirala, S. Semwal, N. Rai, and A. Kranti, "What are the constraints for 1T-DRAM operation via reconfigurable transistor?", Extended Abstracts of the **2022 International Conference on Solid State Devices and Materials (SSDM)**, Chiba, Japan, September 26-29, 2022, pp. 621-622, 2022. DOI: 10.7567/SSDM.2022.J-10-02.
3. A. Kranti, R.K. Nirala, and S. Semwal, "Dual word line enabled energy-efficient high-speed RFET based 1T-eDRAM", Extended Abstracts of the **2023 International Conference on Solid State Devices and Materials (SSDM)**, Nagoya, Japan, September 5-8, 2023, pp. 685-686, 2023. DOI: 10.7567/SSDM.2023.PS-2-17.
4. R.K. Nirala, M. Gupta, and A. Kranti, "Disturbance induced refresh time lowering in nanowire RFET 1T-DRAM array", Extended Abstracts of the **2024 International Conference on Solid State Devices and Materials (SSDM)**, Himeji, Japan, September 1-4, 2024, pp. 629-630, 2024. DOI: 10.7567/SSDM.2024.PS-02-08.

5. A. Kranti, R.K. Nirala, and M. Gupta, “Duration of disturbance tolerance governed bias selection in 1T-DRAM array”, Extended Abstracts of the **2025 International Conference on Solid State Devices and Materials (SSDM)**, Yokohama, Japan, September 15-18, 2025, pp. 717-718, 2025. DOI: 10.7567/SSDM.2025.PS-02-10.

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NOMENCLATURE

λ	*Characteristics/Natural Length*	*nm*
λ_{CYL}	*Natural Length of Cylindrical MOSFET*	*nm*
λ_{DG}	*Natural Length of Double Gate MOSFET*	*nm*
A	*Constant*	$A^{\circ(-1/3)}$
High-K	*Material with High Dielectric*	*Unitless*
I_0	*Read 0 Current*	*A*
I_1	*Read 1 Current*	*A*
$I_{BL,0}$	*Bit Line 0 Current*	*A*
$I_{BL,1}$	*Bit Line 1 Current*	*A*
I_{DS}	*Drain Current*	*A*
K	*Scaling Factor*	*Unitless*
L_{CG}	*Control Gate Length*	*nm*
L_G	*Gate Length*	*nm*
$L_{G,min}$	*Minimum Gate Length*	*nm*
L_{GAP}	*Ungated Region Length*	*nm*
L_{PG}	*Program Gate Length*	*nm*
L_S	*Storage Length*	*nm*
L_S/L_T	*Ratio of Storage Length and Total Length*	*Unitless*
L_T	*Total Length*	*nm*
n	*Semiconductor Region with Electrons as Majority Carriers*	*Unitless*
N_a	*Acceptor Concentration*	cm^{-3}
n_e	*Electron Concentration*	cm^{-3}
n_h	*Hole Concentration*	cm^{-3}
n_{VL}	*Number of Voltage Levels*	*Unitless*
p	*Semiconductor Region with Holes as Majority Carriers*	*Unitless*
T_{BOX}	*Buried Oxide Thickness*	*nm*
t_{HOLD}	*Hold Time*	*s*
T_{OX}	*Oxide Thickness*	*nm*

t_R	*Read Time*	*s*
T_{Si}	*Silicon Thickness*	*nm*
t_{W0}	*Write 0 Time*	*s*
t_{W1}	*Write 1 Time*	*s*
V_{BCG}	*Back Control Gate Voltage*	*V*
$V_{BCG,H}$	*Hold Back Control Gate Voltage*	*V*
$V_{BCG,W0}$	*Write 0 Back Control Gate Voltage*	*V*
$V_{BCG,W1}$	*Write 1 Back Control Gate Voltage*	*V*
V_{BL}	*Bit Line voltage*	*V*
$V_{BL,W1}$	*Bit Line Write 1 Voltage*	*V*
V_{CG}	*Control Gate Voltage*	*V*
V_D	*Drain Voltage*	*V*
$V_{D,W1}$	*Write 1 Drain Voltage*	*V*
$V_{D.H}$	*Hold Drain Voltage*	*V*
$V_{D.R}$	*Read Drain Voltage*	*V*
V_{DD}	*Supply Voltage*	*V*
V_{DS}	*Drain to Source Voltage*	*V*
V_{FCG}	*Front Control Gate Voltage*	*V*
$V_{FCG,W1}$	*Write 1 Front Control Gate Voltage*	*V*
$V_{FCG.H}$	*Hold Front Control Gate Voltage*	*V*
$V_{FCG.R}$	*Read Front Control Gate Voltage*	*V*
V_{PG}	*Program Gate Voltage*	*V*
$V_{PG,W1}$	*Write 1 Program Gate Voltage*	*V*
$V_{PG.H}$	*Hold Program Gate Voltage*	*V*
$V_{PG.R}$	*Read Program Gate Voltage*	*V*
V_S	*Source Voltage*	*V*
$V_{S.H}$	*Hold Source Voltage*	*V*
$V_{S.R}$	*Read Source Voltage*	*V*
V_{TH}	*Threshold voltage*	*V*
V_{WL1}	*Word Line 1 Voltage*	*V*
$V_{WL1,H}$	*Word Line 1 Hold Voltage*	*V*

$V_{WL1,R}$	*Word Line 1 Read Voltage*	*V*
$V_{WL1,W0}$	*Word Line 1 Write 0 Voltage*	*V*
$V_{WL1,W1}$	*Write 1 Word Line 1 Voltage*	*V*
V_{WL2}	*Word Line 2 Voltage*	*V*
$V_{WL2,H}$	*Word Line 2 Hold Voltage*	*V*
$V_{WL2,R}$	*Word Line 2 Read Voltage*	*V*
$V_{WL2,W0}$	*Word Line 2 Write 0 Voltage*	*V*
$V_{WL2,W1}$	*Write 1 Word Line 2 Voltage*	*V*
W_D	*Drain Depletion Width*	*nm*
W_S	*Source Depletion Width*	*nm*
X_j	*Junction Depth*	*nm*
ΔV	*Potential Change*	*V*
ε_{ins}	*Permittivity of Insulator/Oxide*	*F/m*
ε_{Si}	*Permittivity of Silicon*	*F/m*
$V_{BL,W0}$	*Bit Line Write 0 Voltage*	*V*
$V_{BL,R}$	*Bit Line Read Voltage*	*V*
I_{BL}	*Bit Line Current*	*A*
t_{DT}	*Duration of Disturbance Tolerance*	*s*

ACRONYMS

0C	*Zero Capacitor*
1T	*OneTransistor*
1T0C	*One Transistor Zero Capacitor*
1T1C	*One Transistor One Capacitor*
2G	*Twin Gate*
2T	*Two Transistor*
2T0C	*Two Transistor Zero Capacitor*
3D	*Three-Dimensional*
4T0C	*Four Transistor Zero Capacitor*
ALU	*Arithmetic Logic Unit*
AR	*Aspect Ratio*
BCG	*Back Control Gate*
BL	*Bit Line*
BLD	*Bit Line Disturbance*
BOX	*Buried Oxide Layer*
BTBT	*Band-to-Band Tunneling*
CB	*Conduction Band*
CG	*Control Gate*
CMOS	*Complementary Metal-Oxide-Semiconductor*
CMP	*Chemical Mechanical Polishing*
CR	*Current Ratio*
DEC	*Digital Equipment Corporation*
DG	*Double Gate*
DIBL	*Drain-Induced Barrier Lowering*
DRAM	*Dynamic Random Access Memory*
DTB	*Disturb*
EOT	*Equivalent Oxide Thickness*
F	*Feature Size*
FCG	*Front Control Gate*

FD	*Fully Depleted*
FDSOI	*Fully Depleted Silicon on Insulator*
FET	*Field-Effect Transistors*
FOM	*Figure of Merit*
GAA	*Gate All Around*
H	*Hold*
H0	*Hold 0*
H1	*Hold 1*
HCE	*Hot Carrier Effect*
IMOS	*Impact ionization Metal Oxide Semiconductor*
M	*Metal*
MAJ	*Majority*
MBC	*Multi-Bridge Channel*
MOS	*Metal-Oxide-Semiconductor*
MOSFET	*Metal-Oxide-Semiconductor Field-Effect Transistor*
M-S	*Metal- Semiconductor*
NDTB	*No Disturb*
nMOS	*N-Type Metal-Oxide-Semiconductor*
NW	*Nanowire*
P	*Parameter*
PD	*Partially Depleted*
PG	*Program Gate*
pMOS	*P-Type Metal-Oxide-Semiconductor*
R	*Read*
R0	*Read 0*
R1	*Read 1*
RFET	*Reconfigurable Field-Effect Transistor*
RT	*Retention Time*
RT/RT_{max}	*Ratio of Retention Time with Maximum Retention Time*
RT_{max}	*Maximum Retention Time*
S	*Semiconductor*

SB	*Schottky Barrier*
SBH	*Schottky Barrier Height*
SCE	*Short Channel Effect*
S_{FOM}	*Figure of Merit for Process Sensitivity*
SiO_2	*Silicon Dioxide*
SM	*Sense Margin*
SOC	*System on Chip*
SOI	*Silicon on Insulator*
SRAM	*Static Random Access Memory*
T	*Temperature*
TFET	*Tunnel Field Effect Transistor*
TG	*Twin Gate*
UTB	*Ultra-Thin Box*
UTBB	*Ultra-Thin Body Buried Oxide Layer*
VAX	*Virtual Address Extension*
VB	*Valence Band*
W0	*Write 0*
W1	*Write 1*
WL	*Word Line*
WL1	*Word Line 1*
WL2	*Word Line 2*
WLD	*Word Line Disturbance*
WLs	*Word Lines*
X	*Along the Channel Direction in Planar RFET*
XOR	*Exclusive-OR*
Z	*Along the Channel Direction in Nanowire RFET*
Z^2FET	*Zero Impact Ionization and Zero Subthreshold Swing Field-Effect Transistor*
ΔFOM	*Change in Figure of Merit*
ΔP	*Change in Parameter*

Chapter 1

Introduction

The number of transistors in a semiconductor chip has increased tremendously due to in-depth understanding of transistor physics and operation, and key advancements in processing, fabrication, and characterization [1-8]. This increase in transistor density has followed the empirical prediction of G. Moore [9-20]. The transistor density in the chip has increased since the invention of Intel's 4004 microprocessor, which had 2300 transistors in an area of an eighth of an inch [21]. In stark contrast, Apple's M1 chip contains 57 billion transistors within a die size slightly less than one square inch [22].

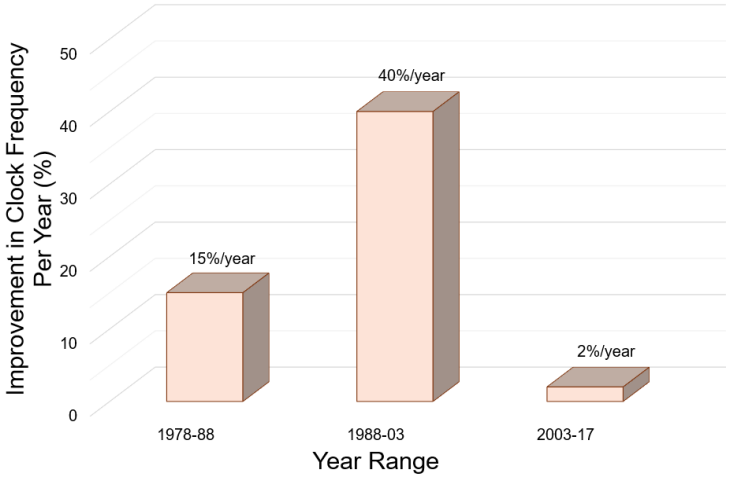

Fig. 1.1 Growth in processor clock frequency from 1978 to 2017 (39 years) [5].

While the semiconductor industry has leveraged innovations in transistors, interconnects, and fabrication processes [7-8], [23-29], the clock rate enhancement of microprocessors, as illustrated in Fig. 1.1, has increase and then decreased over the 39 years from 1978 to 2017. The available data shows a 15 percent increase per year in microprocessor clock rate in the initial years (1978 to 1988) of the microelectronic industry [5]. The clock rate further enhanced to 40 percent per year

from 1988 to 2003, and thereafter to a meager 2 percent improvement per year was observed from 2003 to 2017. The key point is that the increase in the clock rate (per year) has been relatively insignificant since 2003 [5]. The other interesting parameter is to compare the performance of modern processors with respect to the initial computer developed in 1977. The Virtual Address Extension (VAX) model 11/780 was one of the first pioneering computers developed in 1977 by the Digital Equipment Corporation (DEC) [5], [30]. Since 1978, the improvement in processor performance has been variable with respect to VAX 11/780.

Fig. 1.2 Growth in processor performance from 1978 to 2018 (40 years) [5].

As shown in Fig. 1.2, the trends for the 40-year period (1978 to 2018) indicate that the initial years (1978 to 1986) saw an increase of 25 percent per year in processor performance relative to VAX 11/780 [5]. Thereafter, the enhancement in processor performance increased to a significantly high value of 52 percent per year (relative to VAX 11/780) from 1986 to 2003 [5]. The growth then subsided (slowed down) to 23 percent per year (with respect to VAX 11/780) from 2003 to 2011. Subsequently, the improvement in processor performance was 12 percent per year (concerning VAX 11/780) from 2011 to 2015, and 2.5 percent per year (relative to VAX 11/780) from 2015 to 2018 [5]. These results indicate that the rate of improvement in the performance of processors has been slowing down. The data also suggests that the semiconductor industry may not be able to continue following the empirical observation of Moore [20]. Although processor performance has not

seen significant enhancements, the micro/nano electronic industry has achieved remarkable progress through innovations in transistor architecture, fabrication, characterization, and packaging technologies.

1.1 Downscaling Bulk Metal-Oxide-Semiconductor Transistor

A fundamental requirement for the transistor is to function as a switch, with 'low' current in the off-state and 'high' current in the on-state. Besides, the transition from one state to another is governed by capacitances, which should be small to facilitate fast switching [31]. The evolution of transistor architecture from conventional planar (two-dimensional) to nanosheet or nanowire (three-dimensional), coupled with innovation through Silicon-on-Insulator (SOI) technology, has largely contributed to enhancing transistor density in modern chips [7]. The fabricated transistors in the 1970s had a gate length (L_G) of several 100 micrometers. However, to enhance the transistor density in the chip without compromising the performance of transistors, a reduction in the dimensions of the transistor was inevitable. However, a decrease in gate length of a bulk Metal Oxide Semiconductor (MOS) Field Effect Transistor (FET) can result in the space charge region at the drain being close to the space charge region at the source [23]. This reduces the control of the gate over the channel, and an electron could leak from source to drain, which increased the off-current of the transistor. This condition, detrimental to the functioning of the transistor as a switch, is known as short channel effect (SCE) [6], [23], and its suppression is foremost to enable downscaling of MOSFET.

The scaling down of the gate length of the transistor resulted in two-dimensional effects that impacted the current-voltage characteristics. The most prominent among them was the lowering of threshold voltage (V_{TH}) and drain-induced barrier lowering (DIBL) [6], [23]. Both these contributed to an undesired increase in the off-current of the transistor and a degradation of the on-to-off current ratio. In the on-state, the reduction of gate length is beneficial as it enables an increase in the current. However, care should be taken that the increase in drain

current is accompanied by a reduction in source/drain resistances [23]. Also, gate length scaling supports a decrease in capacitance. For capacitance, the gate length downscaling should be accompanied by a reduction in the fringing components as compared to the channel capacitance [23].

The downscaling of MOSFET was primarily attributed to the scaling theory proposed by Dennard *et al.* [32]. This resulted in the formulation of methodology for the miniaturization of MOSFETs. The theory of Dennard *et al.*, [32] suggested to increase or decrease parameters of MOSFET by the scaling factor (K). The data from 1972 to 1992 (two decades) showed an increase in number of transistors (6000 to 3000000) and power consumption (20 mW to 10 W) by 50 times each for a reduction in gate length from 6 μm to 0.4 μm [23]. The actual scaling adopted by the semiconductor industry was different from the ideal theory proposed by Dennard *et al.* [32]. The primary contributor to this difference was supply voltage (V_{DD}) downscaling. The supply voltage was maintained constant to obtain the benefit of high-speed operation [31-33]. Another challenge in V_{DD} reduction was the reduction in V_{TH}. The non-adherence of V_{DD} downscaling was a factor contributing to the high power consumption. The increase in the number of transistors exceeded the projected factor K^2 [31-32]. For each technology generation, the transistor size was reduced by a factor of K (= 0.7, and the area by K^2 (= $0.7 \times 0.7 \approx 0.5$). This would have resulted in an increase in transistor count by a factor of 2 (= 1/0.5). However, the actual transistor count increased by a factor of 4 due to an increase in chip area by a factor of 1.5 [31]. The increase in power consumption was also due to higher number of transistors on a chip.

The industry adopted actual (or pragmatic) scaling described above by clearly identifying challenges for bulk MOSFET downscaling below 0.1 μm. An alternate methodology was suggested to enable MOSFET downscaling from 0.1 μm to 40 nm [34-37]. The approach considered maintaining constant values of substrate doping concentration (10^{18} cm^{-3}), gate oxide (3 nm), and supply voltage (1.5 V) to enable scaling of gate length from 0.1 μm to 40 nm. The parameter which was aggressively scaled (×(1/4)) was junction depth (x_j), i.e., from 40 nm (L_G = 100

nm) to 10 nm (L_G = 40 nm) [34-37]. The result was complete control over SCEs and hot carrier effects (HCEs) with a 30% increase in the on-current. The downside of the approach was high resistance of ultra-shallow source/drain regions due to aggressively scaled junction depth. Various modifications in the downscaling approach were attempted [36-39] to overcome these challenges. One approach was to limit the aggressive scaling of L_G and x_j to 70 nm and 30 nm, respectively, and instead reduce oxide thickness (T_{OX}) from 3 nm to 1.5 nm while maintaining constant V_{DD} (1.5 V) and substrate doping (10^{18} cm^{-3}). This resulted in a high on-current of 1.4 mA/μm and an extremely small direct tunneling leakage current of 2 nA/μm [31]. Although ultra-shallow (14 nm) bias controlled x_j was achieved with additional gates placed over the gate [40], the drawback of such an approach was low on-current (two to three orders lower) in comparison to conventional bulk MOSFET. Based on the different approaches and results of bulk MOSFET, the transistor architecture for downscaling was envisaged to have elevated source/drain regions with an insulator sidewall of 5 nm. For a bulk MOSFET with 5 nm of x_j, the minimum L_G should be around 25 nm with T_{OX} limited to 1.2 nm to avoid SCEs [31]. Besides the technological challenges in ensuring the above criteria, capacitance is indeed critical for speed. The fringing capacitance should not be allowed to be a substantial component of the total gate capacitance. The channel doping concentration was limited to 10^{18} cm^{-3} to reduce parasitic capacitance, mobility degradation, and random dopant fluctuations governed by V_{TH} variability [33].

1.2 Silicon-on-Insulator MOSFET

The problems with the downscaling of bulk MOSFETs can be understood by the following equation, which relates the minimum gate length ($L_{G,min}$) with key transistor parameters.

$$L_{G,min} = (A)\left(T_{ox}x_j(W_S + W_D)^2\right)^{(1/3)} \quad (1.1)$$

where A = 0.41 $A^{\circ(-1/3)}$, W_S and W_D are source and drain depletion widths [41-42]. For a given technology, doping (N_a) required for eq. (1.1) can be obtained [41] as

$$N_a \geq (1.8 \times 10^{17})\left(\sqrt{V_{BI}} + \sqrt{V_{BI} + V_{DS}}\right)^2 \left(\frac{x_j}{50\ \text{nm}}\right)\left(\frac{0.1\mu\text{m}}{L_{G,min}}\frac{T_{OX}}{4\ \text{nm}}\right)^3 \quad (1.2)$$

where V_{BI} and V_{DS} represent built-in voltage and drain bias, respectively.

As gate length is scaled down, the substrate doping increases, which causes several issues for nanoscale MOSFET [1-3]. The problem associated with downscaling can be circumvented if the vertical extension of the depletion width can be limited without increasing the substrate doping. This is possible through SOI technology, which dissociates the dependence of substrate doping and depletion width, provided the semiconductor (Silicon) layer thickness is less than the depletion depth at zero bias. As shown in Fig. 1.3 (a)-(b), SOI MOSFET can be fabricated with thick and thin semiconductor layers [1], [3], [7]. The thick semiconductor region (Fig. 1.3 (a)) will allow partial depletion at zero applied bias and is classified as a partially depleted (PD) SOI MOSFET. The SOI MOSFET with a thin Silicon layer (T_{Si}) is fully depleted at zero bias, and hence, the architecture is referred to as a fully depleted (FD) SOI MOSFET [3], [7], [43-45]. In terms of scaling, FD SOI MOSFET holds promise as SCEs can be effectively controlled. SOI MOSFET architectures with a thin Silicon layer are generally referred to as ultra-thin body (UTB) MOSFETs [1], [7].

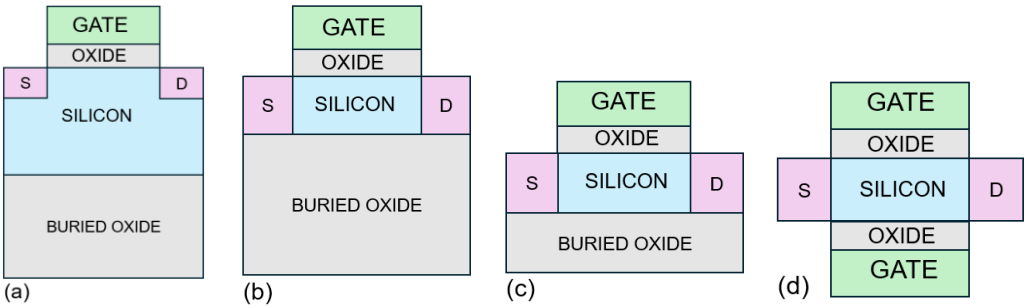

Fig. 1.3 Schematic representation of SOI MOSFET with relatively (a) thick semiconductor layer, (b) thin semiconductor layer, (c) thin buried oxide layer, and (d) double gate architecture. The substrate region (below the buried oxide) is not shown as the focus is on the active semiconductor layer [7].

Apart from reducing the Silicon film thickness, the lateral electric field (associated with the voltage at the drain) also flows through the buried oxide (BOX)

layer. This path of the lateral electric field can be curtailed by reducing the thickness of the BOX layer [46] (Fig. 1.3 (c)). MOSFET comprising of thin Silicon (body) and thin BOX is generally referred to as ultra-thin body BOX (UTBB) MOSFET [1]. Further downscaling of the gate length while maintaining an undoped body can be achieved if the thickness of the buried oxide is kept similar to the front oxide thickness, and another (second) gate is fabricated below the thin buried oxide. This structure, shown in Fig. 1.3 (d), is referred to as the double gate (DG) SOI MOSFET [1], [47].

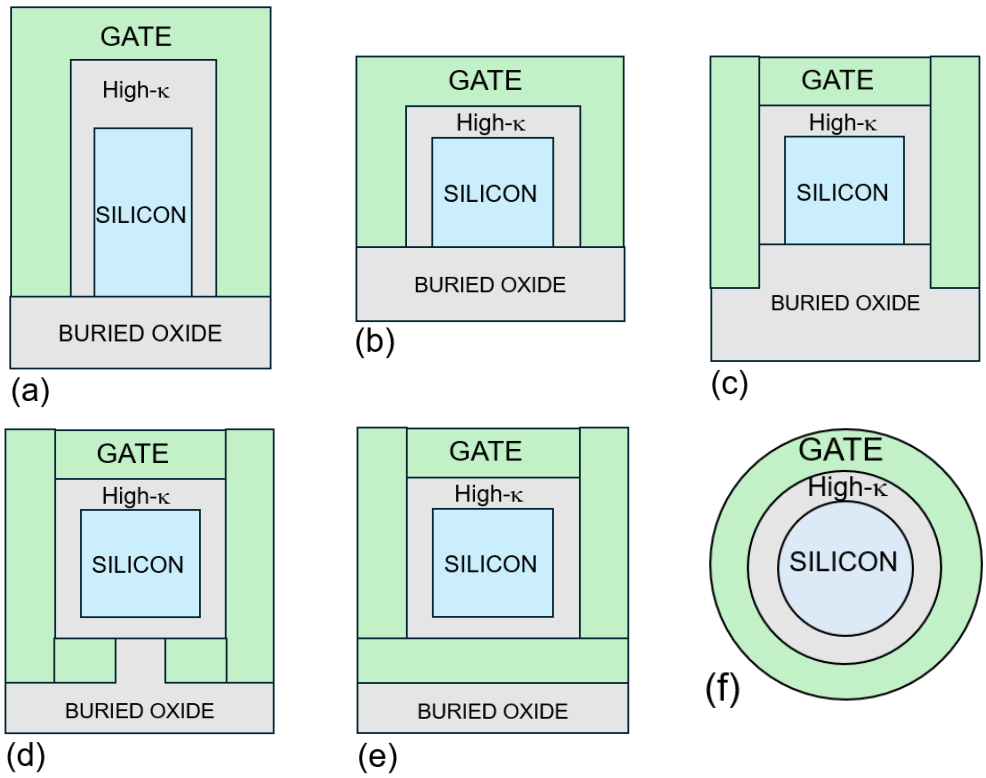

Fig. 1.4 Schematic representation of multi-gate MOSFET cross-section (perpendicular to current flow) for (a) vertical dual gate, (b) triple gate, (c) pi gate, (d) omega gate, (e) quadruple gate, and (f) cylindrical nanowire architecture [1].

FDSOI technology resulted in lower parasitic capacitance, and the strong control of the gate over the channel potential, which was instrumental in lowering the off-current with respect to bulk Silicon technology [3], [7]. Further scaling of transistor dimensions was facilitated through a reduction in BOX thickness (T_{BOX}) and semiconductor layer thickness (T_{Si}). In addition to T_{Si} and T_{BOX}, the gate oxide

thickness (T_{OX}) was also reduced through the incorporation of high permittivity (high-κ) material and metal gate. The most relevant parameter for the high-κ gate stack is the equivalent oxide thickness (EOT) which allows a direct reference with respect to silicon dioxide (SiO_2) layer. The available data for the 28 nm technology node specifies a T_{BOX} of 25 nm, T_{Si} of 7 nm, and EOT of 1.2 nm. Mathematically, the ability of a transistor architecture to limit SCEs can be evaluated through an estimation of natural/characteristic length (λ) [41] through the solution of Poisson's equation with appropriate boundary conditions [48-50]. λ depends on the vertical dimensions (T_{OX}, T_{Si}), permittivity of insulator (ε_{ins}) and Silicon (ε_{Si}) and on the location of conduction channel in the semiconductor. For a planar DG SOI MOSFET shown in Fig. 1.3 (d), λ_{DG} can be obtained [48] as,

$$\lambda_{DG} = \sqrt{\left(\frac{\varepsilon_{Si} T_{Si} T_{ox}}{2\varepsilon_{ins}}\right)\left(1 + \frac{\varepsilon_{ox} T_{Si}}{4\varepsilon_{Si} T_{ox}}\right)} \tag{1.3}$$

To limit SCEs, ($L_G/2\lambda$) should be at least greater than 5. Similarly, a cylindrical nanowire MOSFET [51] is expected to further downscale in comparison to planar MOS architectures as the gate surrounds the Silicon region from all sides [2], [52]. The natural length (λ_{CYL}) for a cylindrical nanowire MOSFET under the approximation $T_{Si}/2 >> T_{OX}$ [50] can be expressed as

$$\lambda_{CYL} = \sqrt{\left(\frac{\varepsilon_{Si} T_{Si} T_{ox}}{4\varepsilon_{ins}}\right)\left(1 + \frac{\varepsilon_{ox} T_{Si}}{4\varepsilon_{Si} T_{ox}}\right)} \tag{1.4}$$

Since the fabrication of vertical dual gate [53] and gate-all-around [54] structures, the MOSFET architecture has considerably evolved (since the late 90s) through the demonstration of planar double gate SOI transistor, vertical (three-dimensional) finFET (Fig. 1.4 (a)), trigate transistor (Fig. 1.4 (b)), pi-gate transistor (Fig. 1.4 (c)), omega gate MOSFET (Fig. 1.4 (f)), quadruple gate transistor (Fig. 1.4 (f)), and nanowire (cylindrical) MOSFET (Fig. 1.4 (f)) [1], [43-45]. These architectures (collectively referred to as multiple gate MOSFETs) essentially increased the control of the gate over the channel through a higher number of gates, and the influence of the drain (lateral) electric field over the channel was consequently suppressed.

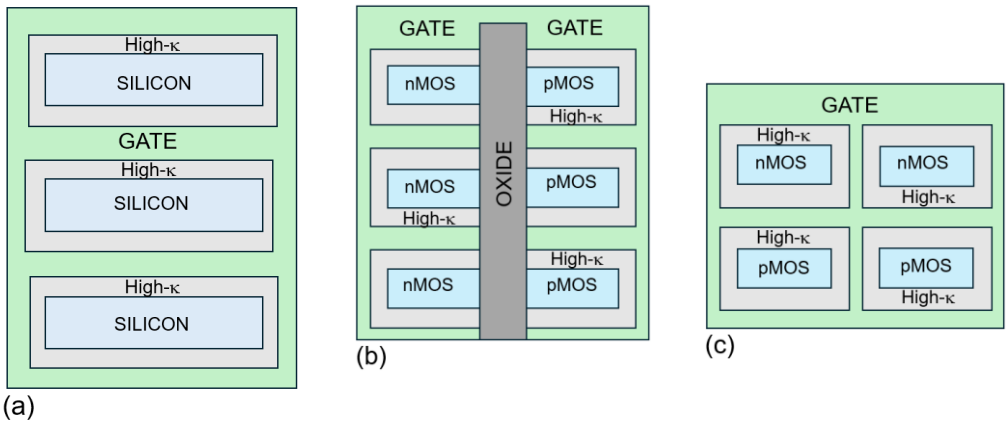

Fig. 1.5 Schematic representation of cross-section (perpendicular to current flow) of (a) multi-bridge-channel MOSFET [55-56], (b) forksheet MOSFET [57-59], and (c) complementary MOSFET [60-61].

While SCEs could be minimized through multiple gate transistors, the current drive in the on-state was limited by the volume of the semiconductor. An increase in semiconductor dimensions (volume) could certainly ease constraints for device fabrication, but could result in SCEs, and consequently, higher off-current. A way to overcome this problem was through the extension of transistor architecture in the vertical direction. This concept was effectively demonstrated in 2002 through the fabrication of a multi-bridge channel (MBC) transistor (Fig. 1.5 (a)) by Samsung [55-56]. Since then, different adaptations of the three-dimensional transistor architecture, such as nanosheet and forksheet transistor (Fig. 1.5 (b)) [57-59] and complementary MOSFET (Fig. 1.5 (c)) [60-61] have evolved. The critical aspect to be noted is that the aspect ratio (AR = height/width) of the semiconductor region in a scaled-down transistor has been largely limited to < 1, i.e., the height of the semiconductor film is lower than its width (separation between two lateral gates).

1.3 Schottky Barrier MOSFET

One of the major concerns of downscaling MOSFET is the reduction in channel resistance which tends to emphasize the importance of ideal source/drain contacts. This reduction can be described through the increase in sheet resistance

of ultra-shallow source/drain regions [62-63]. Therefore, the use of metal source/drain can bypass the limitations of contact resistivity [64]. The source/drain Schottky contact can overcome this problem due to the nearly ideal silicide-silicon interface and low sheet resistance [65]. The reduction in thermal budget enabling integration with metal gate is another advantage of Schottky source/drain regions [66]. A MOSFET with metal source/drain instead of conventional doped source/drain is generally referred to as Schottky barrier (SB) MOSFET [67] is shown in Fig. 1.6. The concept of SB MOSFET was originally proposed by Nishi [68] in 1966. The patent was granted for the same in 1970. To enable circuits with SB MOSFETs either midgap silicide with barrier height nearly equal to half of the Silicon bandgap or complementary silicide (platinum silicide, erbium silicide, ytterbium silicide) which provide two different barrier heights for n-type (low barrier to electrons) or p-type (low barrier for holes) operation [67], [69]. SB MOSFETs have been shown to be cost effective, energy efficient and scalable in comparison to MOSFETs with doped source/drain regions [67], [70-71]. SB MOSFETs may find applications in low-temperature electronics as source/drain contacts do not freeze out at low temperatures [69].

While a metal source/drain can result in lower resistance than that offered by the doped counterpart, a barrier is always present during the device operation. Hence, the resistance essentially re-emerges in the device operation and lowers the current drive [69]. In addition, the problem of higher off-current in SB MOSFETs has also been reported in the literature [67], [69]. The higher junction leakage current in SB MOSFET can contribute to ambipolar behavior [69].

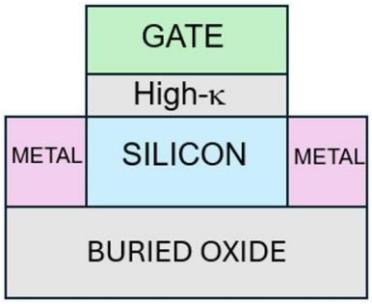

Fig. 1.6 Schematic representation of Schottky barrier (SB) MOSFET [67].

1.4 Reconfigurable Transistors

In order to avoid control of source/drain dopants close to the gate edge, the use of metal source/drain is an interesting alternative. The workfunction of metal contact should be near the midgap energy of the semiconductor. SB MOSFETs, although an interesting choice for dopant free transistor, have been plagued by ambipolar behavior which needs to be suppressed through an appropriate mechanism [72]. Moreover, despite critical innovations in the transistor architecture and reduction of parasitic components, a fundamental limitation of complementary metal-oxide-semiconductor (CMOS) technology is the requirement of separate n-type and p-type transistors to implement logic circuits. If the polarity (type of transistor) could be obtained through bias in the same structure (device) then separate transistors would not be needed for implementing logic circuits. This is true for MOSFETs with Ohmic or Schottky source/drain contacts. As conventional doped source/drain MOSFET is scaled down, the control of source/drain doping near to the gate edge would be challenging [72-77]. Additionally, since the hole mobility is typically lower than that of electrons in Silicon, the current drive of a p-type transistor is lower than that of n-type. The current drive of p-type transistor is generally enhanced by increasing the width of the transistor. This would result in an increase in the layout area of the transistor. Additionally, the semiconductor should be intrinsic to avoid any influence of doping on transistor operation and limit variability.

To achieve n-type or p-type conduction from the same device, the following three possibilities exist:

(i) Selective carrier injection through two independent gates modulating the metal-semiconductor contacts in 2-gated configuration:

In this architecture shown in Fig. 1.7 (a), one of the gates is required for selective carrier injection while the other blocks the flow of opposite type of carrier. This architecture does not require any gate over the middle of the semiconductor (channel) region. Since source/drain are symmetric, any one gate can be utilized to ensure selectivity, i.e., one type of carrier in the channel, while the other gate can

tune the conductance through the channel of allowed carriers. Fully symmetric current-voltage characteristics and logic circuits have been experimentally demonstrated through the concept.

(ii) Selective carrier injection through simultaneous modulation of metal-semiconductor contacts with an additional gate for channel charge control in a 3-gated configuration:
In this topology shown in Fig. 1.7 (b), two gates modulate selectivity by enabling the desired carrier through the Schottky contact while the channel conduction is governed through the additional gate which controls the thermionic barrier. The number of gates in this topology is higher than the previous architecture. Vertically stacked nanowires have been experimentally demonstrated using this topology.

(iii) Carrier selection and injection through front and back gates through 2-gated configuration:
As shown in Fig. 1.7 (c), a back gate positioned below source/drain allows injection of both type carriers which are filtered (polarity checked) in channel through the bias at the top gate. The back gate facilitates ambipolar characteristics similar to that exhibited by SB MOSFET.

All the above architectures (Fig. 1.7 (a)-(c)) have been used to demonstrate a universal transistor, referred to as reconfigurable transistor (RFET), that can function either as n-type or p-type through applied bias. The essential aspect of RFET is to introduce mobile carriers through applied voltage [76]. Hence, depending on the polarity of voltage, either electrons or holes can be injected into the channel. A minimum of two independent gates are required to realize RFET operation [75].

The research on RFETs started in 2000 in Taiwan [78-79], and the early phase of development was from 2000 to 2008, growth was witnessed from 2010-2013 and functional diversification of RFETs was observed from 2014 to 2020 [76]. Initially, the concept of two gates was used to limit the high off-currents in SB transistors. One gate (called as main gate) was placed at the source side while the

other (sub-gate), separated from the main gate by passivation oxide, was placed over the entire channel [78]. The net result was a reduction in off-current and on-to-off current ratio of 10^6 [79]. The word 'reconfigurable' was first introduced in 2011 by Heinzig *et al.*, in the work which demonstrated independent control of Schottky junctions in a 2-gated nanowire heterostructure transistor which exhibited on-to-off current ratio of 10^9 [80].

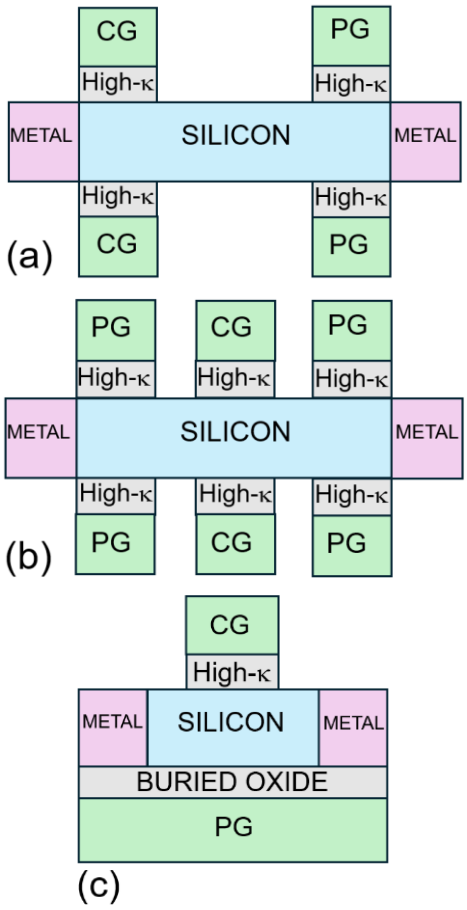

Fig. 1.7 Schematic representation of (a) 2-gated RFET (b) 3-gated RFET, and (c) 2-gated (front and back) RFET architecture [74]. Notations: PG and CG represent program gate and control gate, respectively.

The circuit (inverter) functionality of RFETs was also demonstrated through nanowire transistors with nearly equal electron and hole conduction [81]. Also, a 3-gated RFET was fabricated with vertically stacked nanowires exhibiting n-type as well as p-type functionality with on-to-off current ratio of

10^6 and near ideal subthreshold swing [82]. In addition, exclusive-OR logic (XOR) operation was also demonstrated with 3-gated RFET [83-84]. It was shown that RFETs allow XOR and majority (MAJ) gates to be implemented with lower transistor count than traditional CMOS [82-83]. Research on RFETs has largely focused on fabrication and characterization [85-115], circuit realization [116-132], implementing ferroelectric dielectric layers [133-136], exploiting negative differential resistance [137-138], implementing binary neural network [139], application in hardware security [140], compact modeling [141-145], and analog/RF applications [146-148].

1.5. Comparison with Conventional MOSFETs

A comparison of 3-gated RFET (Fig. 1.7 (b)) with conventional DG FDSOI transistor (Fig. 1.3 (d)) reveals that the total source-to-drain length (L_T) is longer in RFET than that in MOSFET (for the same gate length). This is because of more gates, control gate (CG), and program gate (PG), and the mandatory separation between the gates (L_{GAP}). Intuitively, the longer L_T may not appear to support the downscaling of RFET along the channel direction. However, the presence of a greater number of gates (control and program) allows for dynamic programming which enhances the multifunctionality of RFETs for circuit design [73-78]. In other words, comparison between RFET and MOSFET should be carried out at the circuit level and not through the evaluation of a single device. An inverter with RFET and conventional CMOS technology requires 2 transistors each along with a logical effort of 1 for both [120]. This might appear to be disadvantageous for RFET as a single device would require more footprint owing to the longer L_T. However, the comparison between RFET and CMOS technology becomes interesting if a 3-input NAND or 3-input NOR is designed.

Both logic realizations would require 4 RFETs as compared to 6 FDSOI transistors in CMOS technology [120]. Additionally, the total logical effort would be 5 for implementing 3-input NAND and 7 for 3-input NOR in

conventional CMOS technology. However, for RFET based logic design, the total logical effort would be 3 for implementing both NAND or NOR logic. Similarly, 2-input XNOR implementation requires 8 CMOS transistors whereas RFET count is expected to be 4.

In short, innovative approaches towards circuit design using RFETs are required for a fair performance comparison with CMOS technology. An interesting aspect of the same is through a comparison of 1-bit arithmetic logic unit (ALU) designed with RFET and CMOS technology. Results [120] indicate that 30% area benefit is achieved with respect to CMOS technology if 1-bit ALU is designed efficiently through dynamic programming facilitated by RFET. However, if the same circuit is used as applicable for CMOS technology with RFET then 71% more area is required due to longer L_T of RFET. The reported results also indicate that the reduced critical path in efficient logic design through RFETs contributes to better performance of the 1-bit ALU. The functional range of RFET based 1-bit ALU has also been shown to be higher in comparison with traditional CMOS ALU [120]. In addition, another interesting study proposes the efficient approach of sea-of-tiles to improve manufacturability of RFET circuits [131].

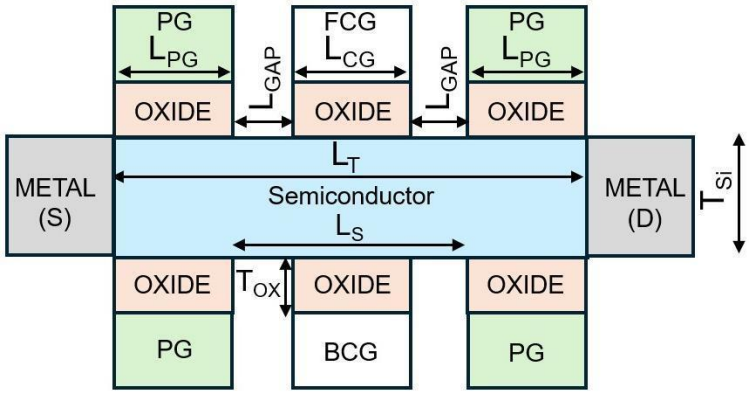

Fig. 1.8 Schematic representation of 3-gated RFET utilized for implementing capacitorless 1T-DRAM. Notations: PG and CG represent program gate and control gate, respectively.

1.6 Memory Architecture

A von Neumann computing architecture is followed in modern computer systems for data processing. In this system, the data is processed by the processor core and stored in memory. In a memory hierarchy [149], memory with the lowest latency (static random access memory (SRAM)) is placed close to the processor core. In contrast, memory with higher latency is placed in lower levels of the memory hierarchy. The SRAM requires a higher number of transistors (8-16) to store the data, which reduces its area efficiency. The processor searches for data in higher levels (L1, L2, L3) of the memory hierarchy (Fig. 1.9). The memory with higher capacity (hard disk drive) lags in latency (in ms). The latency and capacity are both crucial for the processing of data through the processor core. This gap is filled by placing dynamic random access memory (DRAMs) between the SRAM (used for L1 cache to L3 cache levels) and hard disk drives, solid-state drives, and storage-class memory used at lower levels. DRAMs offer the benefits of lower latency (< 10 ns) and moderate capacity (~10 GB). Due to lower latency (< 10 ns) and higher integration density, DRAM is also used in level 4 cache as embedded DRAM memory [149].

There are broadly three different configurations of DRAMs, which differ in terms of charge storage. The one transistor (1T) and one capacitor (1C) based DRAM stores the charge in the physical capacitor [150]. In contrast, the two transistors (2T) and zero capacitor (0C) based DRAM uses the gate of the second transistor (read transistor) as the storage node [151]. The other variant of DRAM is one transistor (1T) and zero capacitor (0C) that stores charge in the body of the transistor [152]. Since the capacitor is not present, the 2T0C DRAM and 1T0C DRAM are often termed as 2T-DRAM and 1T-DRAM, respectively. The logic incompatibility with the presence of a capacitor is the major issue with 1T1C DRAM. The 1T1C can be replaced by 2T-DRAM, but the extra transistor used for storing charge consumes a larger area. The 1T-DRAM overcomes the issue related with 1T1C and 2T-DRAM by utilizing single transistor for storing and reading of

charge. The absence of a capacitor enables it to be logic-compatible [152], and the use of a single transistor consumes less area than a 2T-DRAM.

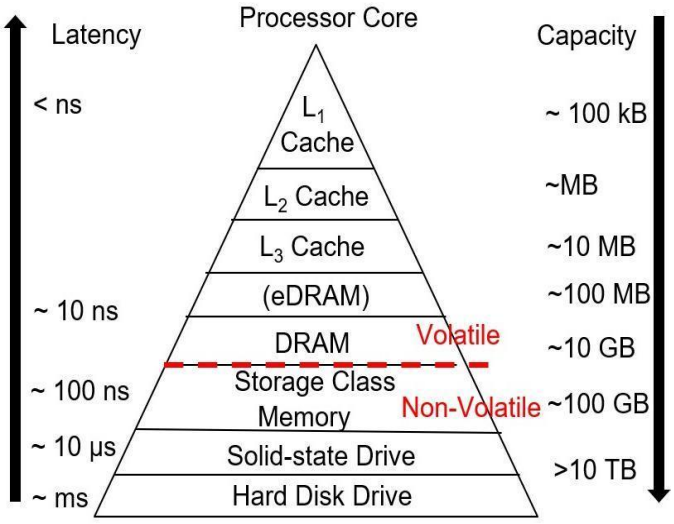

Fig. 1.9 Memory hierarchy based on latency and capacity [149].

1.7 Potential of RFET for Capacitorless Dynamic Random Access Memory (1T-DRAM)

Although 1T-DRAM been demonstrated through conventional FDSOI MOSFET [153-181], tunnel field effect transistor [182-196], junctionless transistor [197-200], feedback FET [201-202], and Schottky FET [203], the possibility of showcasing memory operation through RFET would add to the multifunctional capability of the architecture. Limited studies are available in the literature that focus on the implementation of RFET based capacitorless DRAM [204-205].

Amongst the different RFET architectures shown in Fig. 1.7 (a)-(c), the 3-gated topology is ideal for 1T-DRAM as it facilitates the storage of generated holes in the semiconductor film underneath the back control gate (Fig. 1.8). The architecture of the 3-gated RFET is particularly advantageous, as the holes are stored away from the pseudo source/drain regions due to the inherent separation (L_{GAP}) between the three gates. In a conventional FDSOI MOSFET, the generated holes are stored at the back surface of the semiconductor film through the formation of an electrostatic potential well. However, the proximity of holes to conventional

doped source/drain regions in FDSOI MOSFET tends to degrade the retention characteristics. Hence, gate-source/drain underlap architecture is preferred to separate holes from source/drain [206]. While RFET has shown multi-functional attributes in terms of transistor operation from the same device (n-type and p-type functionality from the same structure) and opportunities for logic design with area benefits, implementing 1T0C DRAM with RFET has been largely unexplored in the literature.

1.8 Hole Generation Mechanism in 1T-DRAM

The 1T-DRAM operation is primarily governed by the difference in the holes generated during programming and those removed during erase. As previously discussed, 1T-DRAM has been implemented in various transistors; however, different architectures require different hole generation mechanisms. A tunnel field effect transistor [182] uses band-to-band tunnelling (BTBT) mechanism to generate holes. In BTBT based mechanism [182], a negative voltage at the gate along with a positive voltage at the drain is used. The bias applied reduces the separation between the conduction band and the valence band at the drain end. Consequently, BTBT occurs and holes are accumulated in the valence band, whereas the electrons move to the conduction band.

In PD SOI-based 1T-DRAM [179], the impact ionization mechanism has been used for generating holes. In this method, a high positive voltage is applied to the gate and drain to initiate impact ionization. The positive voltage at the gate lowers the barrier height for electrons that collide with the atoms near the drain due to the high electric field. This mechanism requires a relatively higher voltage for the generation of holes.

In RFET based 1T-DRAM, the hole generation can be performed by either a positive feedback mechanism induced by impact ionization [207] or through the Schottky tunnelling mechanism [208]. In the impact ionization based mechanism, electron tunneling is facilitated by a positive bias at the PG. Narrow tunnelling width is essential at SB to allow tunnelling of sufficient electrons. A high positive

bias is also applied to the front CG (FCG) and drain of the RFET. The high positive bias is essential to reduce the barrier height underneath the FCG to allow electron flow towards the drain. Consequently, weak impact ionization occurs, resulting in the generation of excess electrons and holes. The generated excess holes accumulate underneath the back CG (BCG) due to the potential well created by applying a negative bias. The generated excess electrons contribute to the current flow. The excess holes stored underneath the BCG raise the potential of the channel, which further reduces the barrier height underneath the FCG. As a result, the rate of impact ionization is enhanced.

The facility of selective carrier injection through Schottky tunneling in RFET provides a unique method for the generation of excess holes. In this mechanism, the excess holes tunnel through the Schottky barrier by applying a negative bias at PG and a positive bias at the drain. The excess holes accumulate underneath the front and back CGs due to the application of a negative bias.

1.9 Problem Formulation and Thesis Objectives

In this work, the potential of 3-gated RFET has been investigated for implementing 1T-DRAM. Based on the literature gap, the following objectives have been defined for the thesis work.

(i) The degradation of retention time (RT) with a change in bias is a concern in 1T-DRAM. This degradation is critical for 1T-DRAM with RFET due to a greater number of gates. While front and back PGs can be electrically connected, the independent front and back CG operation is required to implement 1T-DRAM. Therefore, the bias range able to sustain a degradation of 50% of maximum retention time (RT_{max}) needs to be carefully evaluated to estimate the bias tolerance of 1T-DRAM.

(ii) RFET can be designed with different combinations of lengths of CG (L_{CG}) and PG (L_{PG}) and L_{GAP} for a fixed total length ($L_T = 2(L_{PG} + L_{GAP}) + L_{CG}$). The storage length ($L_S = L_{CG} + 2L_{GAP}$) depends on CG and the

separation between PG and CG. This essentially implies that RFET can be designed with various values of L_S/L_T (0.4 to 0.8) for a given L_T. Optimal bias for RFET based 1T-DRAM should depend on L_S/L_T. In addition, the requirements of 1T-DRAM to function as on-chip (embedded) memory are different from those for standalone applications due to fast write/read operations. An in-depth analysis in terms of write and read access times is required for ascertaining the feasibility of RFET for embedded 1T-DRAM.

(iii) The use of nanowire (NW) transistor architecture has been primarily dictated by logic technology. Hence, investigating the possible realization of 1T-DRAM with NW transistor architecture is crucial. Since independent back gate operation is not possible in NW transistor, RFET serves as an ideal topology to realize 1T-DRAM in NW topology. In addition to exploring 1T-DRAM functionality, the impact of word line disturbance (WLD) and bit line disturbance (BLD) in an array for various operations (write 1 (W1), write 0 (W0), and read (R)) needs to be examined for pragmatic memory realization.

(iv) The biases for 1T-DRAM are usually selected to ensure proper operations – W1, W0, Hold (H), and R. In an array realization, an essential parameter for bias selection is the array disturbance, apart from the feasibility of individual memory operations. Hence, bias optimization (for each operation) should be based on enhancing the duration of tolerance towards WLD and BLD.

1.10 Thesis Outline

The thesis focuses on critically assessing the realization of 1T-DRAM with RFET and has significantly contributed to formulating design guidelines for achieving optimal performance in a 3-gated RFET architecture. The key contributions of the thesis work are given below for each chapter.

In chapter 1, the motivation behind the work has been discussed, which includes (i) evolution of transistor architecture from bulk MOSFET to RFET, (ii) Comparison of RFET with conventional MOSFET, (iii) Potential of 3-gated RFET for 1T-DRAM, (iv) and various mechanisms (BTBT, impact ionization, Schottky tunnelling) for the generation of holes in 1T-DRAM. Finally, problem formulation and thesis objectives are discussed.

Chapter 2 involves details of the simulation models and calibration details of RFET with experimental DC, and transient characteristics of MOSFET based 1T-DRAM. The chapter presents the working methodology of RFET as nMOS and pMOS devices through energy band diagrams and transfer characteristics for different drain voltages (low and high). The formation of pseudo source/drain regions underneath the PG is also discussed. In the subsequent part of the chapter, the working principle of the RFET based 1T-DRAM by adopting a positive feedback mechanism is discussed. RT and Sense margin (SM) are two essential parameters for 1T-DRAM, which have been assessed at different temperatures, i.e., 85 ^{o}C and 125 ^{o}C. The sensitivity analysis for the voltage applied at each gate, i.e., PG, FCG, and BCG, during H and R operations has been carried out. The voltage range capable of supporting a 50% change in RT/RT_{max} has been used to assess the sensitivity towards biases. Finally, the sensitivity of SM, RT, and current ratio (CR) on RFET parameters such as L_{PG}, L_{CG}, L_{GAP}, T_{Si}, and T_{OX} has been evaluated.

Chapter 3 presents a length-dependent assessment of RFET for 1T-DRAM. The chapter starts by showcasing the 1T-DRAM operation in RFET with L_S of 40 nm and L_{CG} of 20 nm. The bias optimization is further extended for L_S of 80 nm and 60 nm for a fixed L_{CG} of 20 nm to investigate the impact of L_S on RT and SM. The length dependence of bias is further studied with respect to L_{CG} for each L_S (40 nm (L_S/L_T = 0.4), 60 nm (L_S/L_T = 0.6), and 80 nm (L_S/L_T = 0.8)) at a fixed L_T of 100 nm. The applicability of RFET for embedded applications

has been analyzed by operating it at a lower duration (sub-5 ns). Finally, the results are benchmarked with published data for different 1T-DRAM.

Chapter 4 presents the 1T-DRAM operation in NW GAA RFET by adopting the Schottky tunneling mechanism to generate holes. The impact of the number of voltage levels (n_{VL}) on RT is showcased. This chapter highlights the impact of WLD and BLD which lowers RT of the 1T-DRAM array. The disturbance analysis for a total of 12 cases by considering each operation, i.e., W1, W0, and R, has been carried out for different voltage levels (3 and 4). Finally, disturbance-centric bias optimization is presented to extend the immunity of the 1T-DRAM array.

Chapter 5 concludes the thesis work by providing a detailed description of the research findings. The chapter also outlines scope for future work on DRAM.

Chapter 2

Working Mechanism of RFET and Implementing Capacitorless DRAM

2.1 Introduction

The continuous downscaling of conventional complementary CMOS technology is approaching its limit, thus presenting a bottleneck for design of high performance system-on-chip (SoC) [81]. RFET, also referred to as a programmable or polarity-controlled device, is an innovative alternative to conventional CMOS transistors. This is due to its unique ability to merge n-type (nMOS) and p-type (pMOS) behaviour through a single device [77]. RFET can be configured as an n-channel or p-channel transistor by applying biases, which can extend the multi-functional attributes without aggressive downscaling [76]. Reduced area requirement of circuit-level implementations of RFET over their conventional CMOS counterpart has been demonstrated through NAND, NOR, and XOR logic gates [118], [209]. Multi-threshold operation of RFET has been shown to reduce static power consumption [210]. A steep subthreshold swing (< 6 mV/decade) with RFET has also been demonstrated, thanks to impact ionization induced by positive feedback [207]. The polymorphic nature of RFETs has opened new avenues in hardware security applications [140], and watermarking [211].

Apart from high-performance logic applications, implementing 1T-DRAM with RFET can be a way forward to improve the overall logic and memory ecosystem. Implementing 1T-DRAM with RFET would serve as an add-on to RFET functionality due to the intrinsic channel and built-in architecture, as

the ungated region separates two PGs from the CG [207] (Fig. 2.1). The factors that support enhanced 1T-DRAM functionality in 3-gated RFET include an undoped Si channel, two carrier generation mechanisms [207-208], a location of the storage region away from the source (S) and drain (D) regions, and a relatively longer L_S. In RFET, L_{GAP}, and L_{CG} contribute to L_S (= $2(L_{GAP}) + L_{CG}$), whereas L_{PG}, L_{GAP}, and L_{CG} contribute to L_T (= $2(L_{PG} + L_{GAP}) + L_{CG}$).

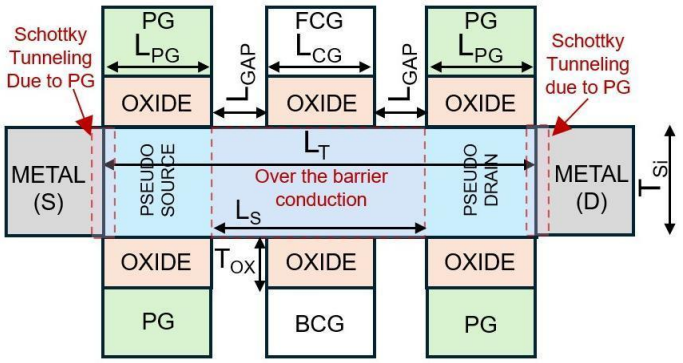

Fig. 2.1 Schematic diagram of a dual (front (F) and back (B)) gate architecture of reconfigurable field effect transistor (RFET) with two polarity gates (PG) and one control gate (CG). The L_{PG}, L_{GAP}, L_{CG}, L_S, L_T, T_{OX}, and T_{Si} are program gate length, ungated region length, control gate length, storage region length, total length, oxide thickness, and Silicon film thickness, respectively.

This chapter provides details regarding the operation of RFET, including the simulation models used to calibrate the results with the transfer characteristics (drain current (I_{DS}) versus control gate bias (V_{CG})) of RFET and the transient characteristics of conventional 1T-DRAM. Following the calibration, simulations of RFET based 1T-DRAM were performed. The calibration of transient characteristics of MOSFET based 1T-DRAM is essential to capture the time-dependent phenomenon (recombination and generation) that governs the hold state of dynamic memory. Thereafter, a detailed explanation of the operating mechanism for different 1T-DRAM operations (W1, W0, H, and R) at 85 ºC is presented. Further, the impact of temperature change (from 85 ºC to 125 ºC) on 1T-DRAM metrics is investigated. As RFET requires appropriate biases at PG (V_{PG}), front CG (V_{FCG}), back CG (V_{BCG}), S (V_S), and D (V_D) for 1T-DRAM, a

sensitivity estimation has been carried further to improve the operating range for V_{BCG} and V_{FCG} during R operation. Along with voltage, 1T-DRAM metrics are also influenced by variation in L_{PG}, L_{CG}, L_{GAP}, T_{Si}, and T_{OX} during fabrication [212]. Hence, sensitivity analysis for device parameters is also discussed in this chapter.

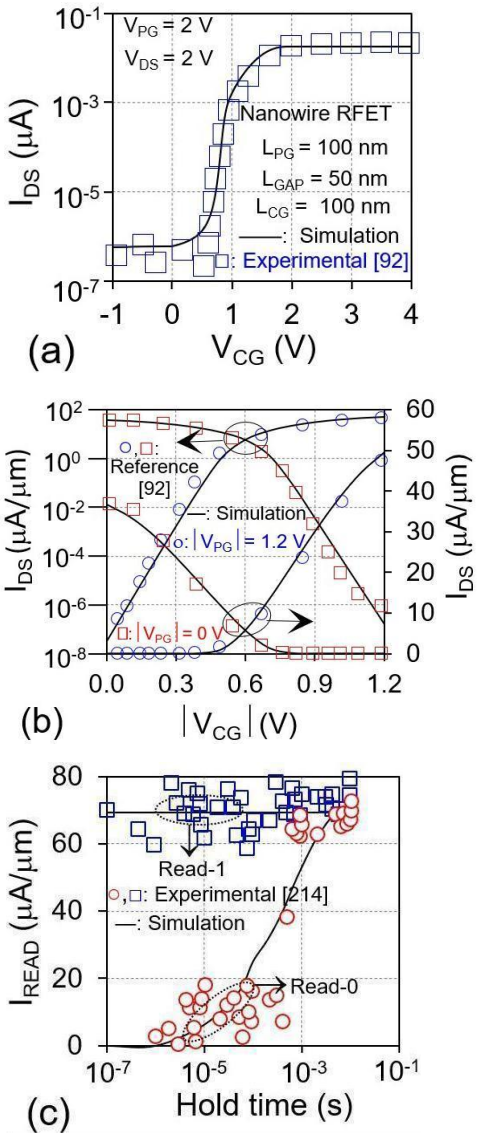

Fig. 2.2 Comparison of simulated with (a) experimental transfer characteristics (I_{DS} versus V_{CG}) of RFET [92], (b) simulated transfer characteristics for both nMOS and pMOS, (c) experimental read current transient as a function of hold (H) time in MOSFET based 1T-DRAM [214].

2.2 Simulation and Device Description

In this work, the potential of 3-gated RFET has been investigated for implementing 1T-DRAM. The analysis has been carried out through well-calibrated simulations [213]. The conduction in RFET, as shown in Fig. 2.1, is controlled through (i) metal–semiconductor (M-S) Schottky barrier (SB), and (ii) CG energy barrier. The positive (negative) PG bias allows electron (hole) tunnelling to form a pseudo-S/D region underneath PGs. The universal Schottky tunneling model [213] was used to capture SB tunneling, while models for over the barrier conduction include field, temperature (T), and doping dependent mobility, along with modules for generation–recombination, impact ionization, and temperature dependent carrier lifetime. The transfer characteristic of RFET shown in Fig. 2.2 (a) agrees well with published data [92]. The comparison of simulation based transfer characteristics, which include nMOS and pMOS behavior, is also shown in Fig. 2.2 (b). In addition, the calibration of transient simulations is also essential for realizing 1T-DRAM. The same was carried out (Fig. 2.2 (c)) through the published experimental data of 1T-DRAM with conventional inversion mode MOSFET [214].

2.3 Working Mechanism of RFET

In this section, the working of RFET is discussed in detail through an energy band diagram. The reconfigurability is achieved by selectively injecting carriers (electrons or holes) through the SB with appropriate bias. $V_{PG} > 0$ allows the tunnelling of electrons through the SB, whereas $V_{PG} < 0$ supports the tunnelling of holes. The conduction of electrons and holes over the energy barrier underneath the CG is achieved by applying $V_{CG} > 0$ and $V_{CG} < 0$, respectively. Understanding the phenomenon behind the operation of RFET is essential for comprehending the implementation of 1T-DRAM because both types of behaviour have been used in 1T-DRAM functionality with RFET.

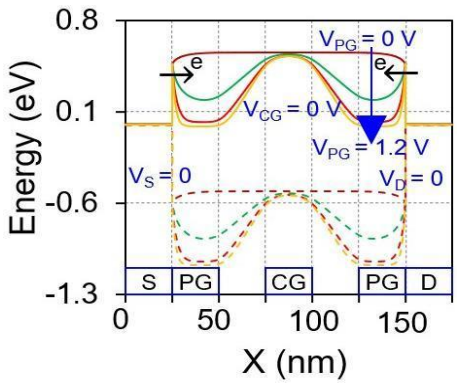

Fig. 2.3 Impact of positive V_{PG} on Schottky barrier (SB) at $V_{CG} = V_S = V_D = 0$ V. The curve is extracted at the surface of the RFET channel.

2.3.1 Impact of Positive V_{PG} on SB

The tunnelling of electrons is governed by the modulation of SB with the application of different positive V_{PG} values. An increase in V_{PG} from 0 V to 0.4 V leads to a reduction in the tunnelling width across the SB that enhances the tunnelling of electrons (Fig. 2.3). The tunneling width is further reduced for $V_{PG} \geq 0.8$ V. The higher energy barrier underneath the CG available for electrons is due to zero voltage at V_{CG}, i.e., $V_{CG} = 0$ V.

2.3.2 N-Type Pseudo Source/Drain Regions

To facilitate the n-type MOSFET, pseudo source/drain regions must be formed in the semiconductor region underneath the PG. The magnitude of V_{PG} applied determines the concentration of electrons available underneath the PG. The application of a low V_{PG} (= 0.4 V) results in an electron concentration (n_e) of ~10^{17} cm^{-3} underneath the PG as shown in Fig. 2.4 (a). The lower n_e is due to a relatively wider tunnelling width (Fig. 2.3). The electron concentration increases to ~10^{20} cm^{-3} after the application of V_{PG} = 1.2 V due to a sufficiently lower tunnelling width (Fig. 2.3), which supports the enhanced tunnelling of electrons through the SB. The presence of a high n_e (~10^{20} cm^{-3}) enables the formation of n-type pseudo-S/D regions underneath the PG, an essential aspect of nMOS operation. The higher energy barrier underneath the CG (V_{CG} = 0 V)

maintains the device in the off-state due to a lower n_e of ~10^{13} cm^{-3}, as observed in the contour plots shown in Fig. 2.4 (a) and (b).

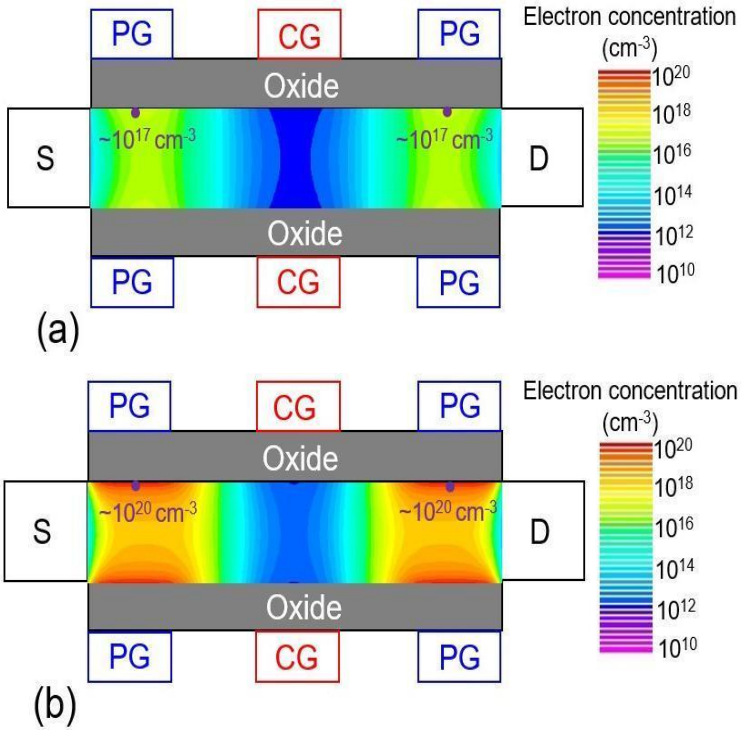

Fig. 2.4 Variation in electron concentration (n_e) underneath the PG after the application of (a) V_{PG} = 0.4 V, (b) V_{PG} = 1.2 V at $V_{CG} = V_S = V_D$ = 0 V. A filled circle denotes the point where the electron concentration (n_e) is mentioned in the contour.

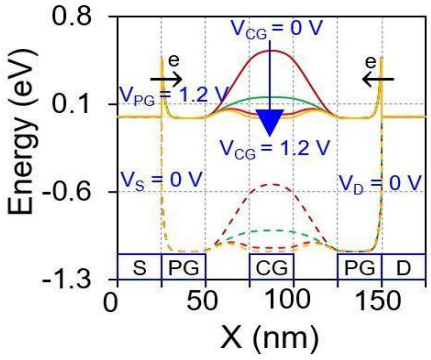

Fig. 2.5 Impact of positive V_{CG} on energy barrier underneath the CG at V_{PG} = 1.2 V, $V_S = V_D$ = 0 V. The curve is extracted at the surface of the RFET channel.

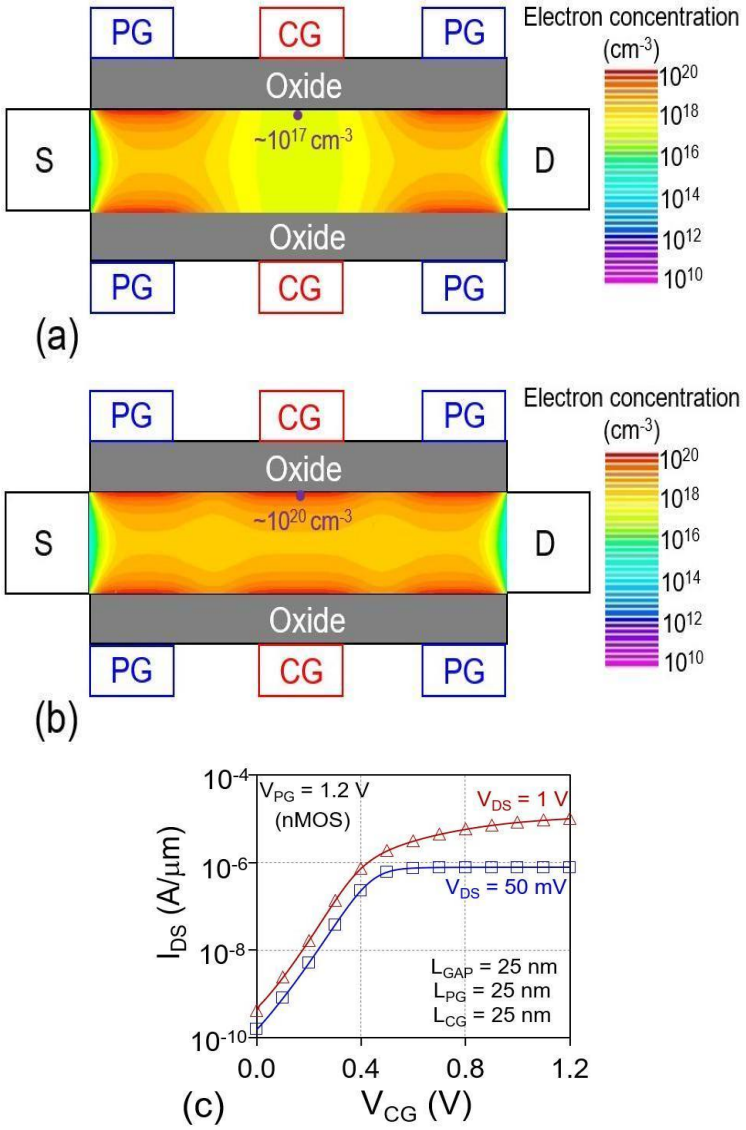

Fig. 2.6 Variation in electron concentration (n_e) underneath the CG after the application of (a) V_{CG} = 0.4 V, (b) V_{CG} = 1.2 V at V_{PG} = 1.2 V, $V_S = V_D$ = 0 V. (c) Transfer characteristics of RFET (I_{DS} versus V_{CG}) showing nMOS behavior at different V_{DS}, i.e., 50 mV and 1 V. A filled circle denotes the point where the electron concentration (n_e) is mentioned in the contour.

2.3.3 Impact of Positive V_{CG} on Energy Barrier Underneath CG

To form the electron-type conducting channel underneath the CG, a positive voltage has to be applied to the V_{CG}. The impact of V_{CG} on the energy barrier is shown in Fig. 2.5. The energy barrier remains high for V_{CG} = 0 V and

reduces to ~0.15 eV after V_{CG} = 0.4 V. The energy barrier further reduces below 0.1 eV for $V_{CG} \geq 0.8$ V. A lower energy barrier underneath the CG facilitates the formation of an electron-type conducting channel underneath the CG. An increase in V_{CG} to 0.4 V results in n_e of ~10^{17} cm^{-3} underneath the CG, as shown in Fig. 2.6 (a). The n_e increases to ~10^{20} cm^{-3} after the application of V_{CG} = 1.2 V (Fig. 2.6 (b)) due to a sufficiently lower energy barrier underneath the CG (Fig. 2.5).

2.3.4 N-Type Conduction in RFET

RFET operates in the on-state, and an electron channel is formed by applying appropriate biases at the PG (V_{PG} = 1.2 V) and CG (V_{CG} = 1.2 V) as shown in Fig. 2.6 (b). The transfer characteristics (I_{DS} versus V_{CG}) at V_{PG} = 1.2 V for V_D = 50 mV and 1 V are shown in Fig. 2.6 (c). For a fixed V_{PG} of 1.2 V, the I_{DS} is equal to 0.23 μA/μm at V_{CG} = 0.4 V, which further increases to 0.77 μA/μm at a higher V_{CG} of 1.2 V for V_{DS} of 50 mV. The enhanced I_{DS} is attributed to a sufficient n_e, as shown in Fig. 2.6 (b). At higher drain to source voltage (V_{DS}) of 1 V, a higher I_{DS} (0.75 μA/μm) is observed. I_{DS} increases to 10 μA/μm at a V_{CG} of 1.2 V, and V_{DS} = 1 V.

2.3.5 Impact of Negative V_{PG} on SB

The tunnelling of holes is governed by the modulation of the SB with the application of negative values of V_{PG} (0 V, -0.4 V, -0.8 V, and -1.2 V). A more negative V_{PG} of -0.4 V (compared to 0 V) leads to a reduction in the tunnelling width across the SB that supports the tunnelling of holes (Fig. 2.7). The tunneling width is further reduced after the application of more negative values of V_{PG} = -0.8 V. At V_{PG} = -1.2 V, a marginal change in tunnelling width is observed as compared to V_{PG} = -0.8 V because the tunnelling width is sufficiently narrow even at V_{PG} = -0.8 V. The higher energy barrier (in the valence band) available for holes underneath the CG is due to zero bias at CG, i.e., V_{CG} = 0 V.

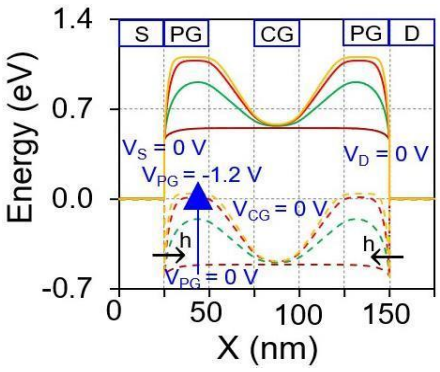

Fig. 2.7 Impact of negative V_{PG} on Schottky barrier (SB) at $V_{CG} = V_S = V_D = 0$ V. The curve is extracted at the surface of the RFET channel.

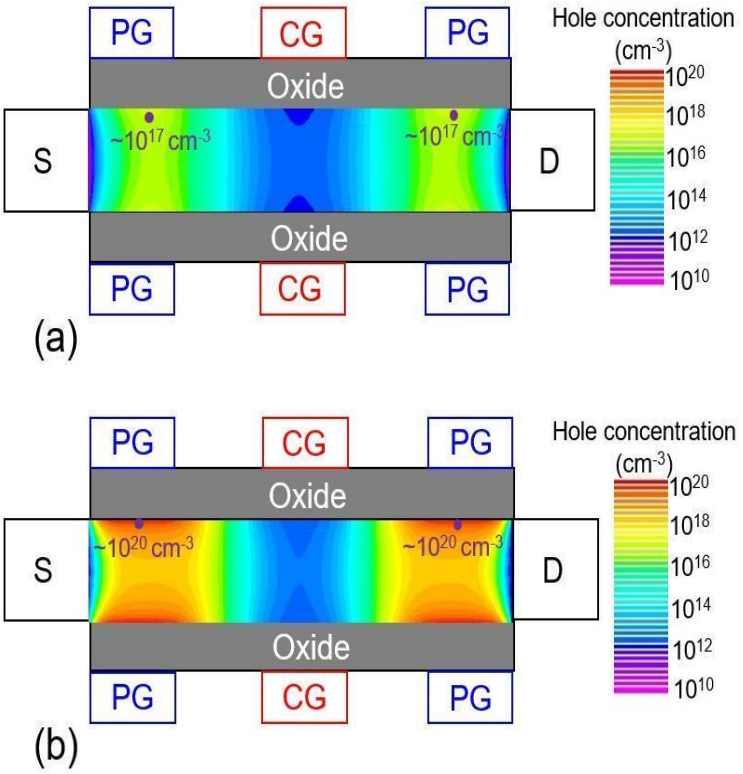

Fig. 2.8 Variation in hole concentration (n_h) underneath the PG after the application of (a) V_{PG} = -0.4 V, (b) V_{PG} = -1.2 V at $V_{CG} = V_S = V_D = 0$ V. Filled circle denotes the point corresponding to that the hole concentration (n_h) has been mentioned in the contour.

2.3.6 P-Type Pseudo Source/Drain Regions

The concentration of holes available underneath the PG is determined by the magnitude of the negative V_{PG} applied. The application of V_{PG} = -0.4 V results in a hole concentration (n_h) of ~10^{17} cm^{-3} underneath the PG as shown in Fig. 2.8 (a). The lower n_h is due to a relatively higher tunnelling width (Fig. 2.7). n_h is further increased to ~10^{20} cm^{-3} after the application of V_{PG} = -1.2 V, which is due to a sufficiently narrow tunnelling width (Fig. 2.7) which supports the enhanced tunnelling of hole through the SB. The presence of n_h (~10^{20} cm^{-3}) enables the formation of a p-type pseudo-S/D regions underneath the PG, an essential aspect of pMOS operation. The higher energy barrier underneath the CG (V_{CG} = 0 V) maintains the device in the off state due to a sufficiently lower n_h ~10^{13} cm^{-3}.

2.3.7 Impact of Negative V_{CG} on Energy Barrier Underneath CG

To form the hole-type conducting channel underneath the CG, a negative V_{CG} has to be applied. The impact of negative V_{CG} on the energy barrier underneath the CG is shown in Fig. 2.9. The energy barrier for holes in the valence band remains high for V_{CG} = 0 V and becomes approximately -0.15 eV at V_{CG} = -0.4 V. The energy barrier for holes further reduces below -0.1 eV for more negative V_{CG}, i.e., -0.8 V, and -1.2 V. A lower energy barrier underneath the CG facilitates the formation of hole-type conducting channel underneath the CG.

2.3.8 P-Type Conduction in RFET

An application of V_{CG} = -0.4 V results in a n_h of ~10^{17} cm^{-3} underneath the CG (Fig. 2.10 (a)). The lower n_h with V_{CG} = -0.4 V is due to a higher energy barrier underneath the CG observed for hole (Fig. 2.9). n_h increases to ~10^{20} cm^{-3} after the application of V_{CG} = -1.2 V (Fig. 2.10 (b)).

RFET operates in on-state, and a hole channel is formed by applying appropriate biases at PG (V_{PG} = -1.2 V) and CG (V_{CG} = -1.2 V) as shown in Fig. 2.10 (b). The transfer characteristics (I_{DS} versus V_{CG}) at V_{PG} = -1.2 V for V_{DS} = -50 mV and -1 V are shown in Fig. 2.10 (c). Conduction of holes occurs after the application of V_{DS}. For a fixed V_{PG} of -1.2 V, I_{DS} of 0.057 μA/μm at V_{CG} = -0.4 V, and 0.11 μA/μm at V_{CG} of -1.2 V, was achieved at V_{DS} of -50 mV. At more negative V_{DS} of -1 V, I_{DS} increases to 0.125 μA/μm) at V_{CG} = -0.4 V and to 1.45 μA/μm at a V_{CG} of -1.2 V.

The above analysis of RFET was performed by applying the same voltage across the front and back CGs. However, in this chapter, 1T-DRAM operation is performed by applying different voltages at front CG and back CG, i.e., an independent CG operation. Independent CG operation is essential W1 operation because positive feedback mechanism requires a negative voltage at the back CG and positive voltage at the front CG for hole generation. PGs are electrically connected during different operations (W1, W0, H, and R) of 1T-DRAM.

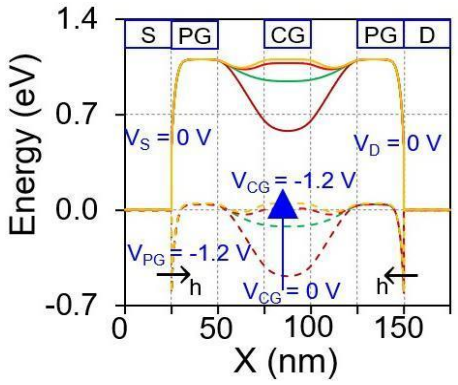

Fig. 2.9 Impact of negative V_{CG} on energy barrier underneath the CG at V_{PG} = -1.2 V, V_S = V_D = 0 V. The curve is extracted at the surface of the RFET channel.

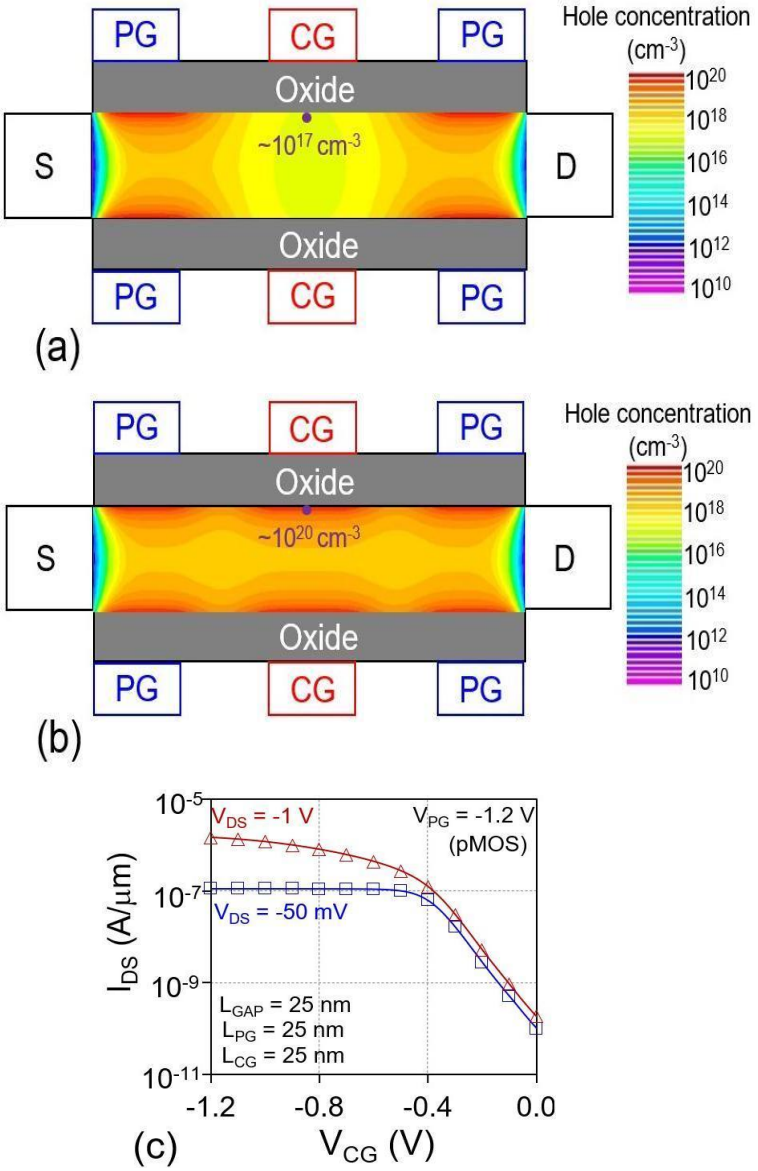

Fig. 2.10 Variation in hole concentration (n_h) underneath the CG after the application of (a) V_{CG} = -0.4 V, (b) V_{CG} = -1.2 V at V_{PG} = -1.2 V, $V_S = V_D$ = 0 V. (c) Transfer characteristics of RFET (I_{DS} versus V_{CG}) showing pMOS behavior at different V_{DS}, i.e., -50 mV and -1 V. The filled circle denotes the point where the hole concentration (n_h) is mentioned in the contour.

2.4 Working Mechanism of RFET-based 1T-DRAM

1T-DRAM consists of two different states i.e. 1 and 0. State 1 is initiated by W1 operation, which is followed by hold operation for state 1 (H1) and read

operation for state 1 (R1) whereas state 0 is initiated by W0 operation, followed by hold operation for state 0 (H0) and read operation for state 0 (R0). The working mechanism of each operation (W1, H1, R1, W0, H0, and R0) by considering the biases shown in Table 2.1 is discussed below. The durations of W1, W0, and R considered are 10 ns, 10 ns, and 40 ns, respectively. No voltage is applied at the source of the RFET during any operation of dynamic memory, i.e., $V_S = 0$ V.

Table 2.1: Biases used for different operations in RFET based 1T-DRAM

Operation	V_{PG} (V)	V_{FCG} (V)	V_{BCG} (V)	V_D (V)	V_S (V)	Time (ns)
W1	1.5	1.5	-1.5	1.5	0.0	10
W0	1.5	1.5	1.5	0.0	0.0	10
H	1.0	0.0	-1.5	0.0	0.0	-
R	1.5	0.5	-1.5	1.5	0.0	40

2.4.1 Write 1 and Write 0 Operations

Generation of sufficient excess holes (n_h) during W1 is essential for the functioning of 1T-DRAM. During W1 operation, excess carriers are generated through the positive feedback mechanism induced by weak impact ionization near the drain side because of a higher electric field [207]. To perform the W1 operation, (i) a higher lateral electric field (due to $V_{D,W1}$), (ii) a lower SB width at the S/D M-S junction (through $V_{PG,W1}$), (iii) a lower front CG barrier (achieved through $V_{FCG,W1}$), and (iv) a potential well near the back CG (negative $V_{BCG,W1}$) are needed, and the same can be enabled through biases outlined in Table 2.1.

A positive PG bias ($V_{PG,W1}$ = 1.5 V) reduces the tunneling width for electrons at the M-S junction. It enables the flow of electrons for an appropriate higher drain bias ($V_{D,W1}$ = 1.5 V), which causes impact ionization near the M-S junction at the drain side. Excess holes stored underneath the back CG ($V_{BCG,W1}$ = -1.5 V) increase the potential of the body, and hence, the barrier at the front

CG is lowered, and a positive feedback mechanism is triggered, which further increases the impact ionization rate. Excess holes generated (~10^{20} cm^{-3} after 10 ns) during W1 are stored in the electrostatic potential well underneath the back CG ($V_{BCG,W1}$ = -1.5 V) as shown in Fig. 2.11. Unlike W1 operation, the W0 operation is performed by applying a positive bias at the back CG ($V_{BCG,W0}$ = 1.5 V) which removes excess holes available underneath the BCG i.e. excess n_h reduces to ~10^4 cm^{-3} (Fig. 2.11). The sufficiently low excess n_h available underneath the BCG after W0 is due to the application of a high magnitude of $V_{BCG,W0}$ = 1.5 V. The bias during W1 operation has been selected such that it can produce sufficient excess holes to initiate 1T-DRAM operation in a given duration of W1 operation (t_{W1} = 10 ns, t_{W1} being the duration over which the W1 operation is performed).

2.4.2 Hold Operation

During H operation (i) a negative back CG bias is applied ($V_{BCG,H}$ = -1.5 V) to hold the excess holes, (ii) a positive PG bias ($V_{PG,H}$ = 1 V) is applied to prevent the tunneling of holes from S/D to channel, (iii) equal bias at source/drain ($V_{S,H}$ = $V_{D,H}$ = 0 V) is used to prevent the leakage of holes, and (iv) a zero front CG bias ($V_{FCG,H}$ = 0 V) is utilized to form a barrier for electrons to prevent recombination of holes. The n_h underneath back CG ($V_{BCG,H}$ = -1.5 V) reaches 10^{17} cm^{-3} after H0 operation due to thermal generation and weak impact ionization (Fig. 2.12). No change in n_h is due to $V_{BCG,H}$ = -1.5 V. Selection of appropriate biases during hold at PG ($V_{PG,H}$), FCG ($V_{FCG,H}$), BCG ($V_{BCG,H}$), S ($V_{S,H}$), and D ($V_{D,H}$) that can balance both recombination during H1 and generation during H0 to achieve higher retention in RFET based 1T-DRAM. Deviation from the bias shown in Table 2.1 during the H operation can lead to enhanced recombination in H1 and enhanced generation in H0. Both tend to degrade the RT of the memory. RT of the 1T-DRAM is defined as the hold time (t_{HOLD}) until the states, i.e., 1 and 0, can be distinguished. The RT of 1T-DRAM

can be estimated through degradation in SM and CR. The two approaches of RT estimation are discussed later in the thesis.

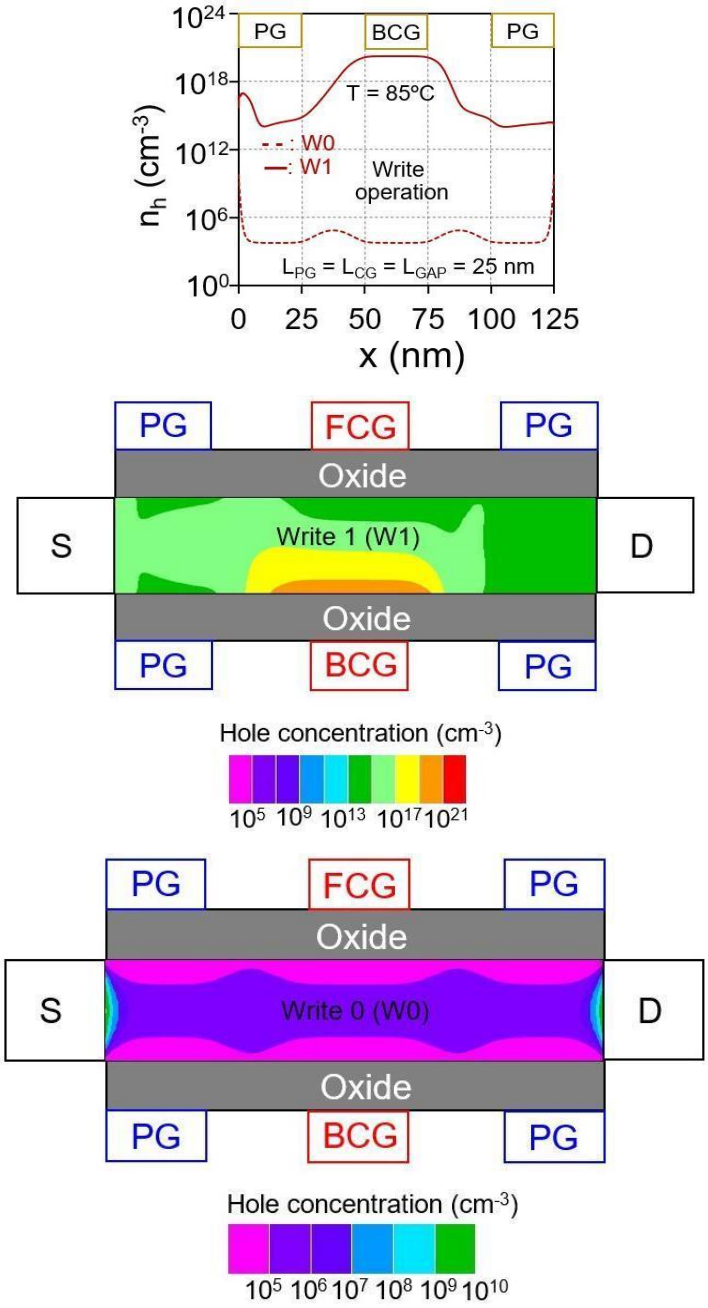

Fig. 2.11 Hole concentration (n_h) along the channel direction underneath the back control gate (BCG) for write 1 (W1) and write 0 (W0) operation at Temperature (T) = 85 °C, along with the contour plots of write 1 (W1) and write 0 (W0). The curve is extracted at the bottom surface of the RFET channel.

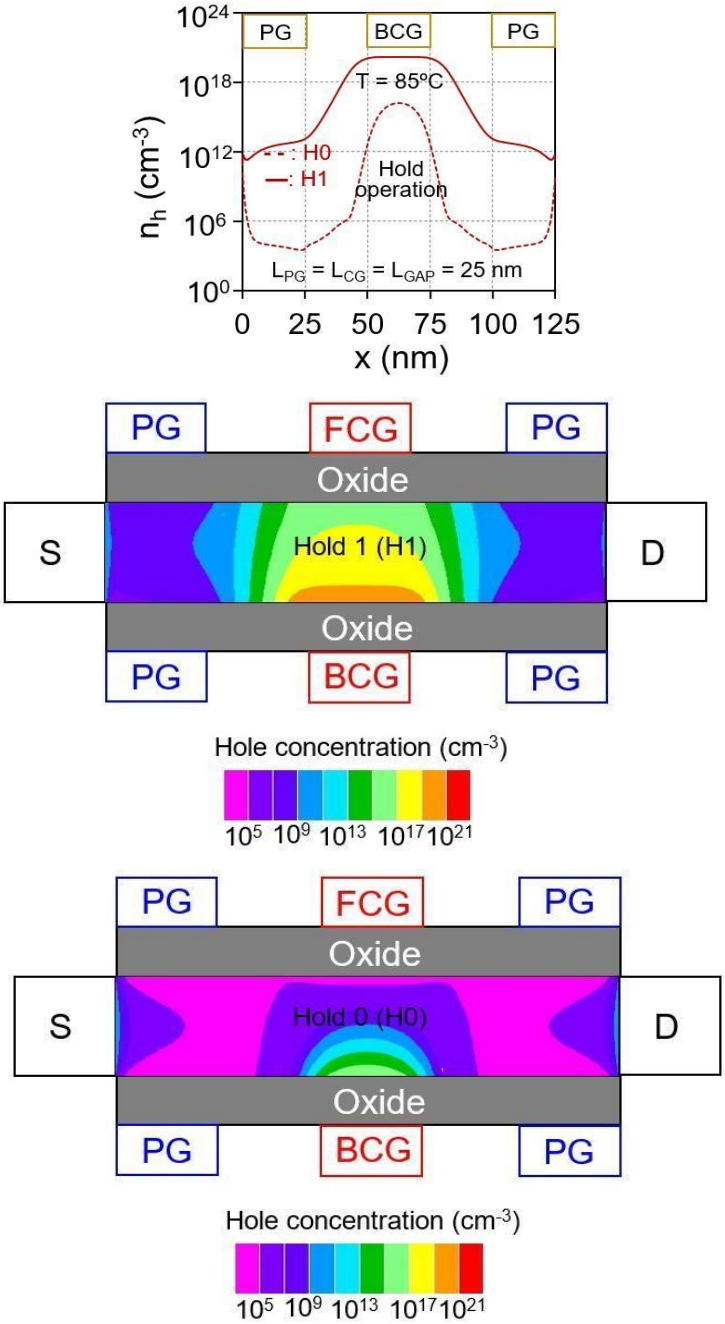

Fig. 2.12 Hole concentration (n_h) along the channel direction underneath the back control gate (BCG) for hold 1 (H1) and hold 0 (H0) operation at Temperature (T) = 85 °C, along with the contour plots of hold 1 (H1) and hold 0 (W0). The curve is extracted at the bottom surface of the RFET channel.

2.4.3 Read Operation

The different values of n_h for H1 and H0, as shown in Fig. 2.12, result in different front CG potentials during R1 and R0 operation (Fig. 2.13 (a)). Thus, the application of an appropriate bias ($V_{PG,R}$ = 1.5 V, $V_{FCG,R}$ = 0.5 V, and $V_{D,R}$ = 1.5 V,) allows RFET to achieve an appreciable difference in the currents of states 1 and 0 i.e. SM (difference in read current for states 1 (I_1) and 0 (I_0) i.e., (I_1 -I_0)) of ~16.6 μA/μm with a high CR (= I_1/I_0) of ~7×10^3. A higher value of n_h results in a higher potential underneath the front CG after R1 operation is performed. While a lower n_h does not significantly influence the front CG barrier, it results in lower potential after the R0 operation. Read operation essentially requires (i) negative $V_{BCG,R}$ to sustain n_h, (ii) $V_{PG,R}$ to enable tunneling of an electron at the SB (iii) $V_{D,R}$ for current conduction, and (iv) positive $V_{FCG,R}$ to lower the barrier for electrons and enable current during read operation (I_1 during R1 and I_0 during R0). A current transient involving different operations is shown in Fig. 2.13 (b). The higher I_1 (current flowing during R1) is due to a higher potential (lower energy barrier) during R1, whereas the lower I_0 is the result of a lower potential (higher energy barrier). The biases selected during the R operation are such that 1T-DRAM performance in terms of RT, SM, and CR is optimal for a given duration over which the R operation is performed (t_R).

2.4.4 Retention Time Estimation

The n_h during the H operation (H1 and H0 states) degrades with t_{HOLD} because of recombination (during H1) and generation (during H0), as shown in Fig. 2.14 (a), which causes a percentage change in SM with t_{HOLD}. The variation in percentage change in SM with t_{HOLD} is shown in Fig. 2.14 (b). The n_h of (~ 10^{20} cm^{-3}) after H1 operation does not deteriorate with t_{HOLD} (from 100 ns to ~ 5 s) due to high $V_{BCG,H}$ = -1.5 V, as shown in Fig. 2.14 (a). The relatively higher magnitude of negative $V_{BCG,H}$ (= -1.5 V) helps in reducing the recombination by increasing the depth of the potential (where the holes are stored). The degradation in n_h is only observed in H0 state (after t_{HOLD} = ~ 10 μs) due to thermal generation

and weak impact ionization. The t_{HOLD} when SM degrades to 50% (~ 8.3 µA/µm) of its maximum (~ 16.6 µA/µm) value is defined as RT [215]. RFET based 1T-DRAM achieves an impressive RT of ~3.2 s (Fig. 2.14 (b)). The percentage change in SM is primarily governed by degradation in I_0, as R operation follows H operation. No change is observed in I_1 due to a negligible degradation in the n_h of the H1 state (Fig. 2.14 (a)).

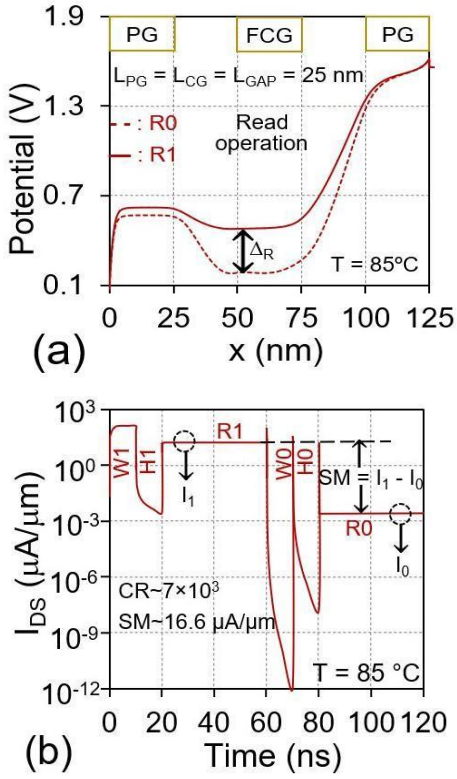

Fig. 2.13 (a) Potential along the channel direction underneath the front control gate (FCG) for read 1 (R1) and read 0 (R0) operation at Temperature (T) = 85 ºC (curve is extracted at the front surface of the RFET channel). (b) Drain current transient for the sequence of 1T-DRAM operation with RFET at temperature (T) = 85 ºC.

2.4.5 Performance at High Temperatures (125 ºC)

This section includes the high temperature operation of RFET based 1T-DRAM [185]. The generation and recombination phenomenon that governs the RT of 1T-DRAM is temperature-dependent. hence, the RT is expected to degrade

at higher temperatures (> 85 ºC). The variation in n_h with t_{HOLD} at 125 ºC is shown in Fig. 2.15 (a). Compared to 85 ºC (Fig. 2.14 (a)), the minor degradation in n_h after t_{HOLD} of 10 µs at 125 ºC is attributed to enhanced recombination during the H1 operation. During the H0 operation at 125 ºC (Fig. 2.15 (a)), n_h starts to degrade after t_{HOLD} = 1 µs (n_h = ~10^{16} cm^{-3}) and reaches ~10^{20} cm^{-3} after t_{HOLD} = 100 ms. The enhanced generation of excess holes during H0 at 125 °C leads to an increase in the percentage change in SM (Fig. 2.15 (b)). Hence, the RT of RFET based 1T-DRAM is reduced to 160 ms at 125 ºC. Despite being operated at higher temperatures, the RFET based 1T-DRAM achieves an impressive RT of 160 ms.

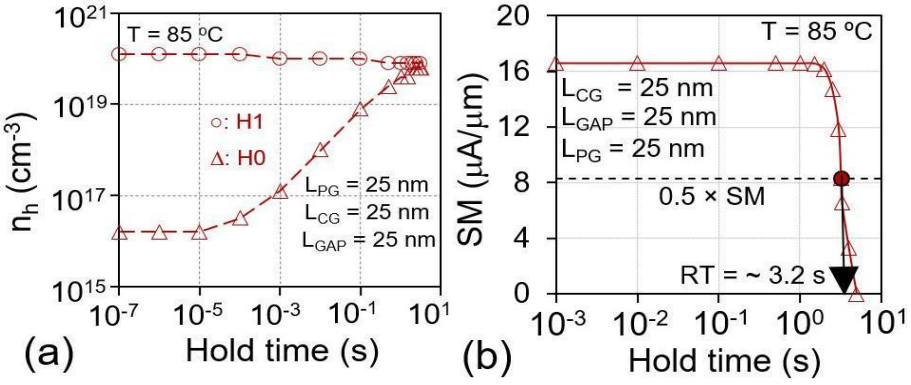

Fig. 2.14 (a) Variation in hole concentration (n_h) with hold time (t_{HOLD}) for H1 and Ho states. (b) Variation in sense margin (SM) with hold time (t_{HOLD}) at temperature (T) = 85 ºC.

2.5 Sensitivity Analysis

The functioning of 1T-DRAM remains susceptible to process and voltage variations. The optimal 1T-DRAM design should ideally exhibit minimal sensitivity to voltage and process variations. In the optimal 1T-DRAM functioning, the voltages applied during W1 and W0 operations do not influence the RT. Hence, only the variation in voltages during H and R operations are considered. Process variations essentially alter the dimensions of RFET. Therefore, the impact of variations in L_{PG}, L_{CG}, L_{GAP}, T_{Si}, and T_{OX} on SM, RT, and CR is discussed in this section.

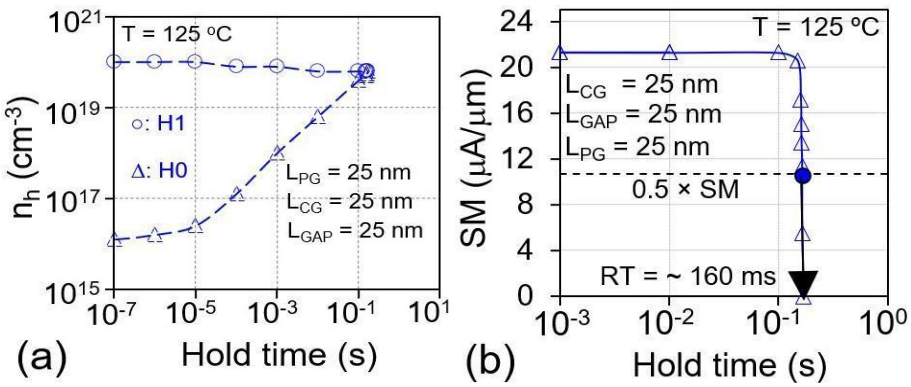

Fig. 2.15 (a) Variation in hole concentration (n_h) with hold time (t_{HOLD}) for H1 and H0 states. (b) Variation in sense margin (SM) with hold time (t_{HOLD}) at temperature (T) = 125 °C.

2.5.1 Analysis of Voltage Sensitivity During Hold Operation

The biases applied during the H operation at PG, CG, S, and D predominantly affects the RT of 1T-DRAM by governing recombination and generation. Hence, an optimal design should exhibit minimal sensitivity towards bias during H operation. A higher PG hold bias ($V_{PG,H}$) reduces the barrier for electrons, whereas a lower PG hold bias ($V_{PG,H}$) supports the tunneling of holes. Either of the two (enhanced electron or hole tunneling) is disadvantageous for 1T-DRAM. RFET based 1T-DRAM shows a RT of 5.2 s at PG hold bias ($V_{PG,H}$) of 0.8 V (Fig. 2.16). A lower value of PG hold bias ($V_{PG,H} < 0.8$ V) can lead to a reduction in maximum normalized RT (RT/RT_{max}) as shown in Fig. 2.16. (a). This can be attributed to enhanced hole tunneling (hole generation), which initiates the generation (deterioration) in the H0 state. The retention has been normalized with respect to the maximum value in the investigation. Hence, RT/RT_{max} value below 1 indicate degradation. A higher value of PG hold bias ($V_{PG,H} > 0.8$ V) leads to enhanced recombination in the H1 state and consequently, the RT/RT_{max} is reduced below 1. Thus, a window of ~580 mV is observed for $V_{PG,H}$ for sustaining 50% degradation in peak RT.

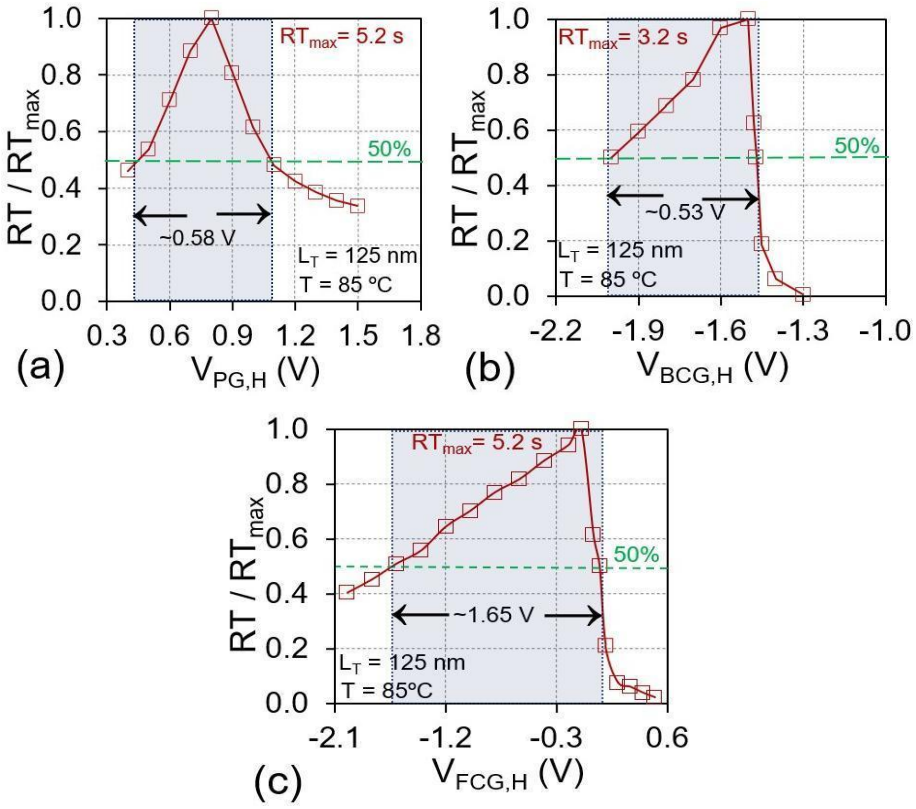

Fig. 2.16 Variation of normalized RT with (a) hold (H) PG bias ($V_{PG,H}$), (b) hold (H) BCG bias ($V_{BCG,H}$), (c) hold (H) FCG bias ($V_{FCG,H}$), at temperature (T) = 85 °C.

A less negative BCG hold bias ($V_{BCG,H} > -1.5$ V) supports the recombination in H1 state, whereas a more negative BCG hold bias ($V_{BCG,H} < -1.5$ V) enhances the hole generation in H0 state. Recombination occurs due to a reduction in the energy barrier whereas generation occurs due to an increase in the energy barrier. Consequently, RT/RT_{max} (RT_{max} = 3.2 s) reduced below 1 for $V_{BCG,H} > -1.5$ V (recombination in H1 state) and $V_{BCG,H} < -1.5$ V (generation in H0 state). A smaller operating bias window (evaluated as the range of bias for which RT reduces by 50% of its peak value (RT_{max})) of ~530 mV is observed for $V_{BCG,H}$ as shown in Fig. 2.16 (b). Similar to the back CG hold bias, the front CG hold bias also governs the RT of the RFET based 1T-DRAM by altering the n_h through recombination (in H1 state) and generation (in H0 state). A $V_{FCG,H} > 0.1$ V leads to a reduction in RT/RT_{max} below 1 because of recombination in the H1 state, while for $V_{FCG,H} < 0.1$ V, RT/RT_{max} is reached below 1 due to hole generation in the H0 state. Recombination ($V_{FCG,H} > 0.1$ V) in the H1 state leads to a sharp degradation in

RT/RT_{max}, whereas the degradation due to generation ($V_{FCG,H} < 0.1$ V) is relatively slower. A higher operating bias window of ~1.6 V is observed for $V_{FCG,H}$ than ~0.53 V for $V_{BCG,H}$.

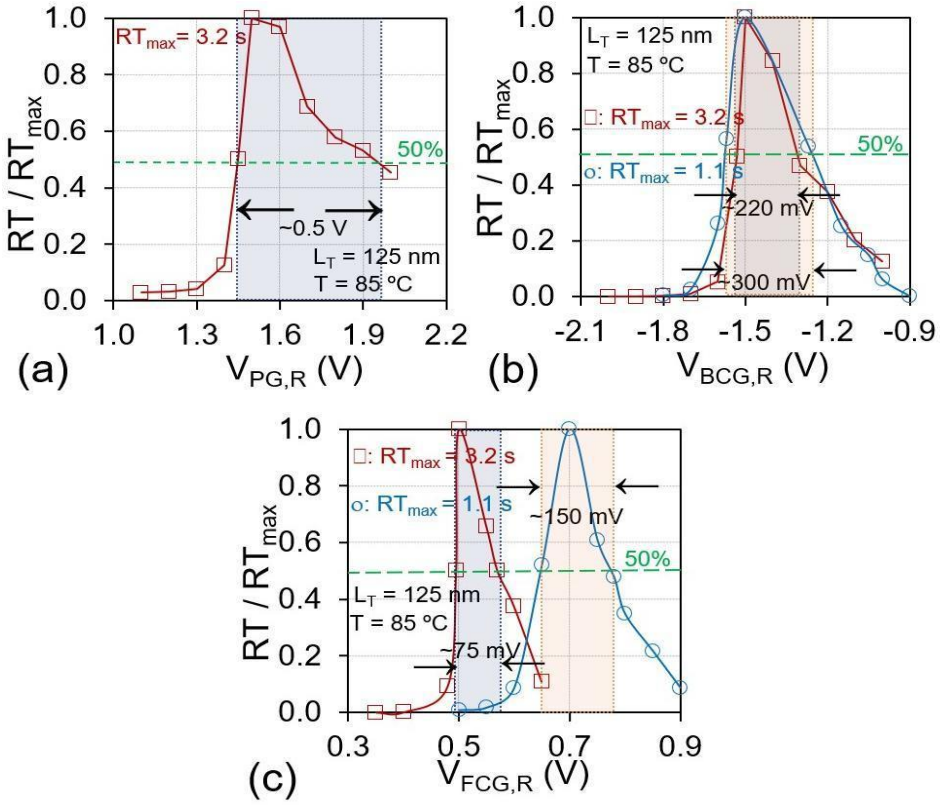

Fig. 2.17 Variation of normalized RT with (a) read (R) PG bias ($V_{PG,R}$), (b) read (R) BCG bias ($V_{BCG,R}$), (c) read (R) FCG bias ($V_{FCG,R}$), at temperature (T) = 85 °C.

2.5.2 Analysis of Voltage Sensitivity During Read Operation

The biases applied during the R operation at PG, CG, S, and D predominantly affect the RT of 1T-DRAM through a degradation in I_1 and I_0. Hence, an optimal design should exhibit minimal sensitivity towards bias during R operation. PG bias during read ($V_{PG,R}$) influences the barrier for electrons. Hence, higher $V_{PG,R}$ enhances SM (= I_1-I_0), which can also result in a rapid degradation of I_0 while smaller $V_{PG,R}$ results in faster degradation of I_1. Consequently, RT/RT_{max} reduces below 1 for $V_{PG,R} > 1.5$ V due to enhanced degradation in I_0, whereas for $V_{PG,R} <$ 1.5 V, RT/RT_{max} is reduced below 1 due to enhanced degradation in I_1. Hence, the optimal operating window is limited to ~0.5 V (Fig. 2.17 (a)).

Achieving high CR requires a reduction of I_0 through a lowering of BCG read bias ($V_{BCG,R}$), which also affects I_1, and consequently, RT is compromised. SM can be enhanced through an increase in I_1 through FCG read bias ($V_{FCG,R}$), which can also degrade I_0, and consequently, a lower RT is obtained.

A reduction in $V_{FCG,R}$ leads to a deterioration in I_1 and a very narrow window (~ 75 mV) for $V_{FCG,R}$ is observed (Fig. 2.17 (c)). An increase in $V_{BCG,R}$ results in faster degradation of I_0 (Fig. 2.17 (b)), which only allows for a narrow window (~ 0.22 V) for $V_{BCG,R}$. The lower bias range for read can be enhanced by using RFET with longer L_{GAP} through the reduction in control (L_{CG} = 20 nm) and program gate length (L_{PG} = 20 nm). This device length change results in a reduction in peak RT (1.1 s at 85 ^{o}C). However, a wider window for $V_{FCG,R}$ (150 mV) and $V_{BCG,R}$ (300 mV) can be obtained through architectural optimization of RFET as shown in Fig. 2.17 (b) and (c), respectively. The relatively wider window for $V_{CG,R}$ can be attributed to suppressed recombination during the H1 state in the optimized architecture due to an increase in L_{GAP} of 32.5 nm (L_{GAP} = 25 nm in the earlier design). The increase in ungated region length also limits generation during H0, and consequently, the optimized architecture provides a wider window of 300 mV (as compared to 200 mV with the earlier architecture).

2.5.3 Process Sensitivity

Sensitivity analysis (S_{FOM} = ((ΔFOM/FOM)/(ΔP/P)) [216] through the impact of parameter (P) such as L_{CG}, L_{GAP}, L_{PG}, T_{OX}, and T_{Si} on figure of merits (FOM such as SM, CR, and RT) is carried out through ±5% variation in a parameter about its mean value (Fig. 2.18). L_{PG} is least sensitive as it does not contribute to storage region whereas L_{GAP} and L_{CG} influence RT due to their contribution to the storage region. T_{Si}, T_{OX}, L_{CG}, and L_{GAP} are critical parameters for 1T-DRAM. T_{Si} can considerably influence I_0, and hence, the sensitivity of CR is higher for T_{Si}. As I_1 strongly depends on resistance, SM is more sensitive to L_{GAP} as compared to L_{CG} and L_{PG}. RT is most sensitive as it is affected by I_1 and I_0. SM is the least sensitive as it is governed by I_1. SM and RT are particularly affected by T_{OX} due to its impact on I_1.

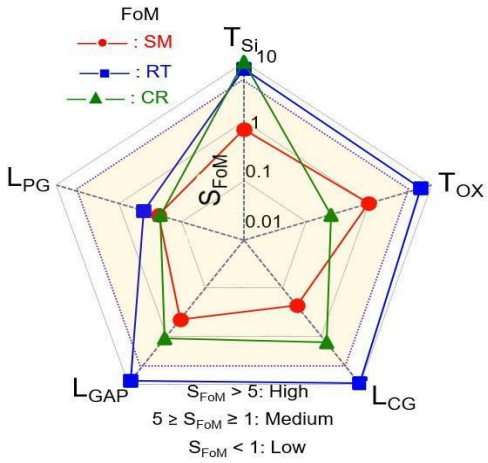

Fig. 2.18 Sensitivity of RT, SM, and CR on RFET parameters (T_{Si}, T_{OX}, L_{CG}, L_{PG}, and L_{GAP}), at temperature (T) = 85 °C. The highlighted region shows medium and low sensitivity.

2.6 Conclusion

In this chapter, the working mechanism of RFET-based 1T-DRAM is presented. Results indicate that RFET based 1T-DRAM can achieve high retention time (3.2 s) along with appreciable SM (> 6 μA/μm) and CR (~10^4). Furthermore, the high-temperature performance of 1T-DRAM is also investigated at 125°C, and a RT of 160 ms was achieved (> 64 ms). Moreover, voltage and parameter sensitivity analysis have also been showcased. The challenge for the practical realization of 1T-DRAM is expected to be the high sensitivity towards read biases, with stringent conditions for the front control gate read bias in terms of an extremely narrow optimal window (75 mV) to withstand a 50% degradation of the peak retention value. However, the high sensitivity towards the front control gate voltage can be reduced to a certain extent by optimizing the L_{CG}. Additionally, precise control of film thickness is necessary due to its contribution towards higher sensitivity of RT and CR.

Chapter 3

Length Dependent Constraints in RFET based 1T-DRAM

3.1 Introduction

As evident from the architecture, RFET consists of different gates, i.e., PG and CG, that are separated by an ungated region [92]. Various applications of RFET have considered different values for L_{PG}, L_{CG}, and L_{GAP} [81]-[148]. The performance of RFET strongly depends on the individual L_{PG} and L_{CG}, as well as on L_{GAP}, as proper etching of PG and CG electrodes is a critical step in the fabrication at nanoscale dimensions [92], [216-218]. A twin-gated RFET has also been employed for realizing 1T-DRAM [204]. Due to better gate controllability and location of the storage region, 3-gated RFET can show a superior performance over 2-gated RFET. It has been intuitively inferred that a longer L_S can enhance RT. However, achieving a longer L_{GAP} (for a given L_T) may be a challenge in devices due to the downscaling trend, as it would add to the series resistance and degrade the current drive [74], [219]. The design guidelines in terms of the ratios of different lengths in RFET remain unexplored in previous work on RFETs. This chapter focuses on understanding the dependence of the ratios of different length components on the operation of RFET based 1T-DRAM.

In chapter 2, the basic working mechanism of RFET based 1T-DRAM was shown at L_T of 125 nm. The variation in L_{PG}, L_{CG}, and L_{GAP} for fixed L_T can affect the 1T-DRAM operation. For example, the variation in L_S (comprising the CG and ungated region) can affect hole generation during W1. Similarly, variation in L_S can also result in variation in currents during the R operation, which can affect the

SM of 1T-DRAM. The RT of 1T-DRAM, governed by the recombination and generation process, is also influenced by variations in L_S due to a change in the lateral electric field. The extension of RFET multi-functionality beyond logic applications requires a feasible memory operation for which an understanding of the impact of various length components on physical mechanisms is essential. Hence, assessing various length components affecting memory operation, bias, and performance metrics associated with RFET architecture is of paramount importance. The analysis is also essential because RFET architecture-supporting logic operations may not be an optimal choice for 1T-DRAM operation.

An assessment of lengths (L_{PG}, $L_{GAP,}$ and L_{CG}) and their impact on biases in RFET-based 1T-DRAM for a fixed L_T = 100 nm is discussed in this chapter. Results indicate that the performance of RFET based 1T-DRAM depends strongly on the contribution of L_{CG} in both L_T and L_S instead of the contribution of L_S in L_T. As RT can vary over a wide range (550 ms to 8.7 s) for a fixed L_T (100 nm), understanding the contribution of L_{CG} in L_T and L_S is advisable rather than focusing on individual lengths. The different lengths associated with RFET are shown in Table 3.1. Through a comprehensive analysis, the reasons for low RT in several RFET topologies are thoroughly investigated. Furthermore, the feasibility of RFET for on-chip memory is also explored for various L_S values. For example, a storage region length of 40 nm can be achieved through various combinations of L_{CG} outlined in Table 3.1. However, all combinations may not exhibit similar memory performance. RT and SM of 1T-DRAM have been estimated for sub-5 ns write (t_{W1}) and read (t_R) durations, making it applicable in on-chip applications. During H operation, the bias at a terminal that achieves maximum RT for the considered L_S value is considered the optimal bias. The bias for R operation is optimized by considering that memory can achieve SM > 6 μA/μm and contribute to enhanced RT. Thereafter, the impact of L_{CG} (for each L_S as shown in Table 3.1) on bias and its contribution to SM and RT are analyzed. Finally, a comparison is made with existing 1T-DRAM technologies.

Table 3.1: Combination of L_{PG}, L_{GAP}, and L_{CG} values for L_T = 100 nm.

L_T (nm)	L_{PG} (nm)	L_{GAP} (nm)	L_{CG} (nm)	L_S (nm)	L_S/L_T
100	30	15	10	40	0.4
		10	20		
		5	30		
	20	25	10	60	0.6
		20	20		
		15	30		
		10	40		
		5	50		
	10	35	10	80	0.8
		30	20		
		25	30		
		20	40		
		15	50		
		10	60		
		5	70		

Table 3.2: Biases for 1T-DRAM with L_S = 40 nm (L_{PG} = 30 nm, L_{CG} = 20 nm).

Operation	V_{PG} (V)	V_{FCG} (V)	V_{BCG} (V)	V_D (V)	V_S (V)	Time (ns)
W1	1.5	0.65	-1.0	1.5	0.0	10
W0	1.0	1.0	1.0	0.0	0.0	10
H	1.0	0.0	-1.3	0.2	0.2	-
R	1.5	0.3	-1.0	1.5	0.0	30

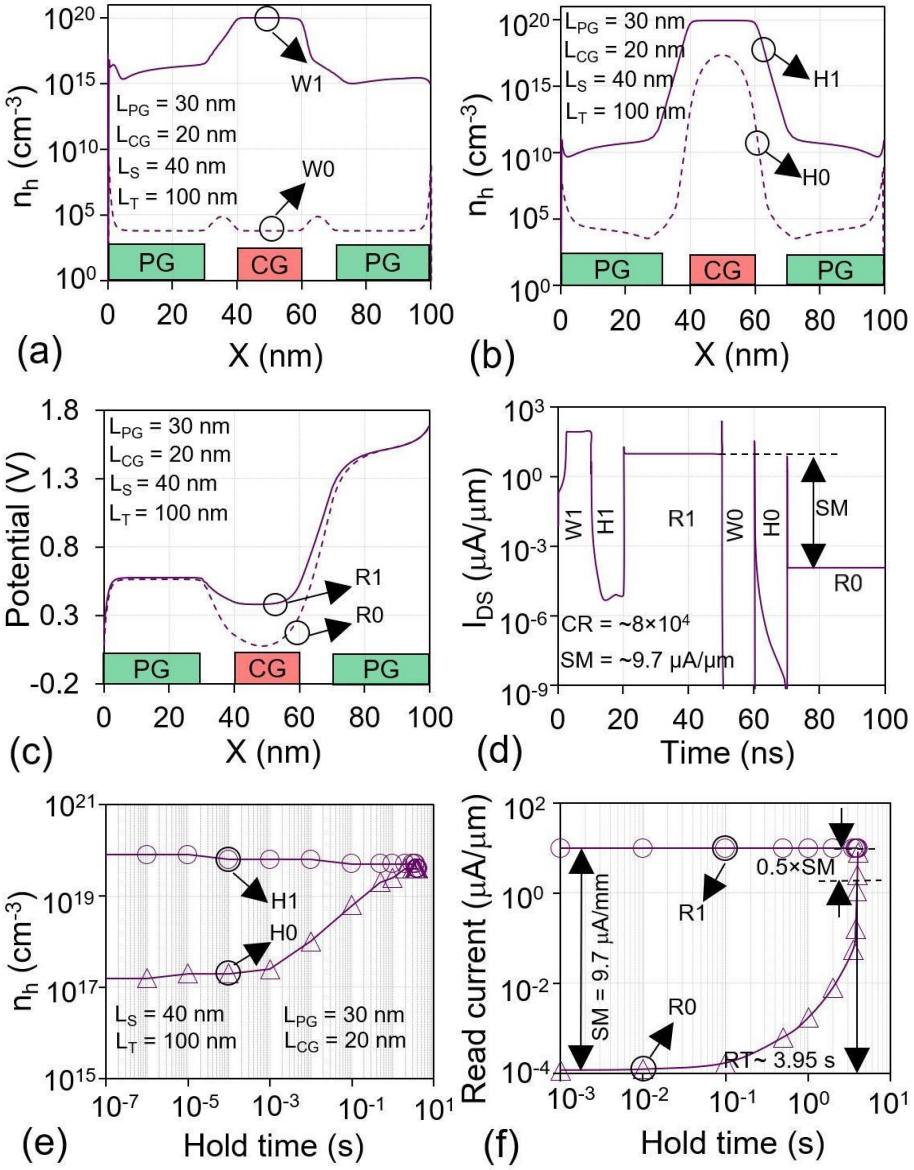

Fig. 3.1 Variation of hole concentration (n_h) at the back surface of RFET along the channel direction (x-direction) during (a) write 1 (W1) and write 0 (W0), (b) hold 1 (H1) and hold 0 (H0) operation. (c) Variation of potential at front surface during read 1 (R1) and read 0 (R0) operation. (d) Current transient of RFET based 1T-DRAM for various operations. Variation of (e) hole concentration (n_h) and (f) read current for R1 and R0 with hold time (t_{HOLD}). Biases are mentioned in Table 3.2.

3.2 Impact of Storage Length on 1T-DRAM Performance

To analyze the impact of variation in L_S, three different values (40 nm, 60 nm, and 80 nm) were considered, as shown in Table 3.1. For L_S of 40 nm, L_{CG} varies from 10 nm to 30 nm, whereas for L_S of 60 nm and 80 nm, L_{CG} varies from 10 nm to 50 nm and 10 nm to 70 nm, respectively. The working mechanism and role of biases during different operating modes are discussed to analyze the influence of L_S on biases (V_{PG}, V_{FCG}, V_{BCG}, V_D, V_S) for 1T-DRAM. The phenomenon of a positive feedback mechanism induced by weak impact ionization is responsible for the W1 operation. The current flow in RFETs of different L_S values can vary due to the variations in L_{CG} and L_{GAP}. The recombination/generation mechanism responsible for RT is influenced by the lateral dimensions (L_{PG}, L_{CG}, and L_{GAP}) through the lateral electric field of the device. Besides W1 and H operations, the R operation is also governed by the contributions of L_{CG} and L_{GAP} in L_S.

3.2.1 IT-DRAM Operation with Different Storage Lengths

To showcase 1T-DRAM functionality, RFET with a 10 nm L_{GAP}, a 30 nm L_{PG}, and a 20 nm L_{CG} has been considered, which accounts for 40 nm and 100 nm of L_S and L_T, respectively. The biasing scheme used for W1, W0, H, and R is shown in Table 3.2. The set of bias values shown in Table 3.2 is optimized to provide maximum RT with L_S = 40 nm and SM > 6 μA/μm. During W1 operation, excess carriers are generated through a positive feedback mechanism induced by weak impact ionization near the drain side due to a higher electric field **[**207**]**. To perform the W1 operation, (i) a higher lateral electric field (due to $V_{D,W1}$), (ii) a lower SB width at the S/D M-S junction (through $V_{PG,W1}$), (iii) a lower front CG barrier (achieved through $V_{FCG,W1}$), and (iv) a potential well near the back CG (due to negative $V_{BCG,W1}$) is needed. A positive PG bias ($V_{PG,W1}$ = 1.5 V) reduces the tunneling width for electrons at the M-S junction. It enables the flow of electrons at a higher drain bias ($V_{D,W1}$ = 1.5 V), which causes impact ionization near the M-S junction at the drain side. Excess holes stored underneath the back CG increase the potential of the body, and hence, the barrier at the front CG is lowered, which

further increases the ionization rate. After 10 ns of operating time for W1 operation, a generation rate ranging between 10^{28} and 10^{30} $cm^{-3}s^{-1}$ is observed (i) between PG and CG, and (ii) near the M-S junction at the drain side ($V_{D,W1}$) in RFET. Excess holes (~10^{20} cm^{-3} after 10 ns) during W1 are stored in the potential well underneath the back CG using a negative back CG bias ($V_{BCG,W1}$ = -1 V) as shown in Fig. 3.1 (a). The W0 operation is performed by applying a positive bias at the back gate ($V_{BCG,W0}$ = 1 V), which removes excess holes available underneath the back control gate, i.e., the excess hole concentration reduces to ~10^4 cm^{-3} (Fig. 3.1 (a)). During H operation (i) a negative back CG bias is applied ($V_{BCG,H}$) to hold the excess holes, (ii) a positive PG bias ($V_{PG,H}$) is applied to prevent the tunneling of holes from S/D to channel, (iii) equal bias at source/drain ($V_{S,H} = V_{D,H}$) is used to prevent the leakage, and (iv) a zero front CG bias ($V_{FCG,H}$) is utilized to form a barrier for electrons to prevent recombination of holes.

Since H operation follows W1 operation, a negative bias is applied at the back CG ($V_{BCG,H}$ = -1.3 V) that accommodates excess holes (~10^{20} cm^{-3}) as shown in Fig. 3.1 (b). Excess hole concentration underneath back CG ($V_{BCG,H}$ = -1.3 V) reaches 10^{17} cm^{-3} after H0 operation due to thermal generation and weak impact ionization (Fig. 3.1 (b)). The different values of hole concentration for H1 and H0 provide different front CG potentials during R1 and R0. Thus, the application of an appropriate read bias ($V_{PG,R}$ = 1.5 V, $V_{FCG,R}$ = 0.3 V, and $V_{DS,R}$ = 1.5 V) allows RFET to achieve an appreciable sense SM (= I_1-I_0) of ~9.77 μA/μm with a high CR (= I_1/I_0) of ~8×10^4. A higher n_h results in a higher potential underneath the front CG when R1 operation is performed. While a lower n_h does not significantly influence the potential underneath the front CG during the R0 operation.

Read operation essentially requires (i) negative $V_{BCG,R}$ to sustain hole concentration, (ii) $V_{PG,R}$ to enable tunneling of an electron at Schottky Barrier (iii) a $V_{D,R}$ for current conduction, and (iv) positive $V_{FCG,R}$ to lower the barrier for electrons and enable current during read operation. A current transient involving different operating modes is shown in Fig. 3.1 (d). The higher I_1 is due to a higher potential (lower energy barrier) during R1, whereas the lower I_0 is the result of a

lower potential (higher energy barrier). The hole concentration during the H operation degrades with t_{HOLD} due to recombination (during H1) and generation (during H0), as shown in Fig. 3.1 (e), which causes degradation in I_1 and I_0 currents, as shown in Fig. 3.1 (f).

The presence of an ungated region in RFET prevents band-to-band tunnelling during H operation, which results in relatively slower degradation of state '0' and contributes to an improved RT. The t_{HOLD} when SM degrades to 50% (~4.88 μA/μm) of its maximum (~9.77 μA/μm) value is defined as RT, and RFET based 1T-DRAM attains an impressive RT of ~3.95 s with an L_{CG} of 20 nm and L_S of 40 nm.

Table 3.3: Biases for 1T-DRAM with L_S = 80 nm (L_{PG} = 10 nm, L_{CG} = 20 nm).

Operation	V_{PG} (V)	V_{FCG} (V)	V_{BCG} (V)	V_D (V)	V_S (V)	Time (ns)
W1	1.5	1.1	-1.0	1.5	0.0	10
W0	1.0	1.0	1.0	0.0	0.0	10
H	1.0	0.0	-1.2	0.2	0.2	-
R	1.5	0.55	-1.0	1.5	0.0	30

3.2.2 Trade-offs Associated with Storage Length and Retention Time

In general, a longer L_S is desirable in 1T-DRAM operation because it can accommodate a higher hole concentration and result in an enhanced RT due to suppressed recombination and generation. In RFET, the lateral electric field is affected by the length of the PG (for fixed L_T). The longer L_{PG} weakens the lateral electric field, whereas the shorter L_{PG} enhances the lateral electric field. Thus, the selection of appropriate lengths (L_{PG}, L_{CG}, and L_{GAP}) is crucial to achieving improved 1T-DRAM performance. Fig. 3.2 (a) shows the transient characteristics of RFETs (L_T = 100 nm) for L_S of 40 nm and 80 nm for a fixed L_{CG} of 20 nm. The variation in SM with t_{HOLD} for each RFET is shown in Fig. 3.2 (b). To showcase 1T-DRAM operation for L_S = 80 nm, a different set of biases has been used, as

shown in Table 3.3. With L_S = 40 nm, the RFET based 1T-DRAM can achieve SM of ~9.7 µA/µm along with a good RT of ~3.95 s. Due to a relatively longer L_{GAP} (= 30 nm) in RFET with L_S = 80 nm (L_{CG} = 20 nm), the series resistance increases, and thus, RFET requires a relatively higher $V_{FCG,W1}$ = 1.1 V to generate sufficient holes, and $V_{FCG,R}$ = 0.55 V to achieve an acceptable SM (> 6 µA/µm). Even at a higher read bias, RFET with a longer L_S (= 80 nm) shows a marginally lower SM (~8.7 µA/µm) due to the longer L_{GAP} (= 30 nm). Apart from lower SM, 1T-DRAM with L_S = 80 nm exhibits a relatively reduced RT (= 1.4 s) because of two main reasons – (a) higher $V_{FCG,R}$ needed for longer L_S (= 80 nm) causes I_0 to increase at a faster rate with t_{HOLD}, and (b) maximizing L_S implies minimizing L_{PG} (for fixed L_T) which contributes to storage region being closer to source/drain, and consequently H0 state is degraded. The CR of both 1T-DRAM designs is reasonable, i.e., over 4 orders. Therefore, for the same L_{CG} (20 nm), RFET with a shorter L_S (40 nm) achieves better RT and SM. The results indicate that longer L_S in RFET may not always ensure better 1T-DRAM performance. With appropriate bias selection during H ($V_{BCG,H}$) and R ($V_{FCG,R}$) operations, a shorter L_S for a fixed L_T may result in enhanced 1T-DRAM performance.

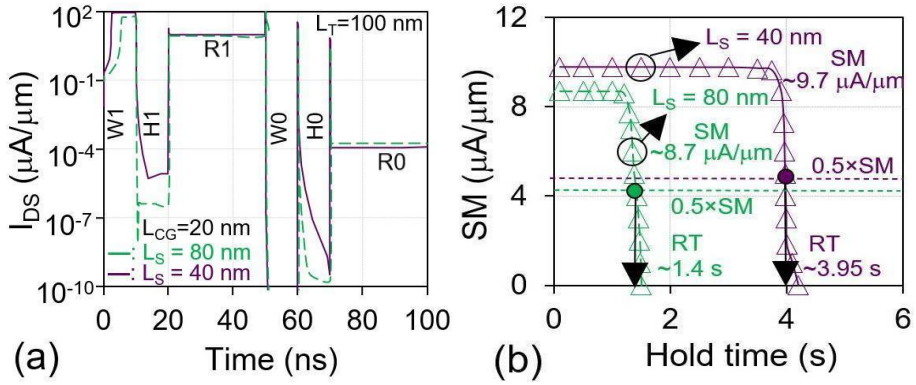

Fig. 3.2 Comparison of (a) Drain current transient and (b) Variation in SM with hold time (t_{HOLD}) of L_S = 40 nm and 80 nm for fixed L_{CG} = 20 nm with optimal bias. For L_S = 40 nm, all biases are the same as shown in Table 3.2, while for L_S = 80 nm, biases are the same as shown in Table 3.3.

3.3 Storage Length Dependent Bias Optimization

The storage length consists of L_{CG} and L_{GAP}. To ensure reasonable L_S (for fixed L_T), L_{PG} should be minimized. Apart from enabling carrier flow at the M-S junction, PG also reduces the influence of the lateral electric field on the storage region, i.e., it maintains the storage region away from the S/D. Therefore, in RFET with a shorter L_S (for fixed L_T), RT is limited by the lower L_S. However, in RFET with longer L_S values, RT is limited by the strong influence of the lateral S/D electric field on the storage region. Thus, an optimal range of L_S is essential to maximize the retention of 1T-DRAM. A longer L_S translates into a longer L_{GAP} or L_{CG}, which introduces a higher series resistance. The different values of L_{PG} and L_{GAP} in RFET with L_S = 40 nm (L_{PG} = 30 nm, L_{GAP} = 10 nm), 60 nm (L_{PG} = 20 nm, L_{GAP} = 20 nm), and 80 nm (L_{PG} = 10 nm, L_{GAP} = 30 nm) for fixed L_T of 100 nm cannot provide optimal 1T-DRAM performance with the applied bias as shown in Table 3.2. To showcase the dependence of L_S on 1T-DRAM behavior, the L_{CG} of 20 nm is fixed for each L_S of 40 nm, 60 nm, and 80 nm. The impact of L_S on W1, H, W0, and R operations, along with corresponding bias optimization to ensure optimal memory performance, is discussed in the next section. The bias shown in Table 3.2 has been applied in different operating modes for each L_S (40 nm, 60 nm, and 80 nm) with L_T = 100 nm and L_{CG} = 20 nm. The deterioration in memory operations is then improved by applying a different set of biases (termed optimal) based on the contribution of L_{PG}, L_{GAP}, and each L_S (40 nm, 60 nm, and 80 nm).

3.3.1 Bias Optimization for Write 1 Operation

The W1 operation is crucial for operating 1T-DRAM. Failing to generate sufficient hole concentration during W1 can lead to non-distinguishable read currents. Hence, bias optimization is essential for W1. To showcase the impact of L_S (for fixed L_{CG} of 20 nm and L_T of 100 nm) on the functioning of 1T-DRAM, a common set of biases, as shown in Table 3.2, is applied at the terminals of the RFET. W1 operation in RFET with L_S = 60 nm and 80 nm exhibits a subdued level of impact ionization compared to the RFET with L_S = 40 nm (for fixed L_T = 100 nm) for the same $V_{PG,W1}$ = 1.5 V, $V_{FCG,W1}$ = 1.1 V, $V_{BCG,W1}$ = -1 V and, $V_{D,W1}$ = 1.5

V. Consequently, lower hole concentration is generated during W1, i.e. ~2.5×10^{18} cm^{-3} for L_S = 60 nm, and ~2.5×10^{17} cm^{-3} for L_S = 80 nm as compared to ~7.9×10^{19} cm^{-3} for L_S = 40 nm (Fig. 3.3 (a)). The RFET design with L_S = 60 nm and 80 nm is expected to achieve a low W1 current due to the subdued impact ionization (Fig. 3.3 (b)). The longer L_{GAP} of 20 nm and 30 nm in L_S of 60 nm and 80 nm, respectively, offers a higher channel resistance compared to the L_{GAP} of 10 nm in L_S = 40 nm (L_{CG} = 20 nm and L_T = 100 nm). Higher channel resistance results in a subdued level of impact ionization. To achieve sufficient hole concentration that can initiate memory operation, a higher $V_{FCG,W1,}$ is essential to lower the front CG barrier in RFET with longer L_S (Fig. 3.3 (c)). The suppressed barrier height enables a higher current flow, which enhances the rate of ionization. For a fixed L_{CG} = 20 nm, RFET with L_S = 40 nm requires a lower $V_{FCG,W1}$ (0.65 V), while RFET with L_S = 80 nm mandates a relatively higher $V_{FCG,W1}$ (1.1 V), to generate sufficient excess carriers as shown in Fig. 3.3 (c). The L_S of 60 nm requires $V_{FCG,W1}$ of 0.9 V to generate an adequate concentration of holes (Fig. 3.3 (c)). After applying optimized biases (Fig. 3.3 (c)) for various L_S, sufficient excess holes can be generated, and a comparable W1 current can be observed in all RFET designs (L_S = 40 nm, 60 nm, and 80 nm), as shown in Fig. 3.3 (d).

3.3.2 Bias Optimization for Hold Operation

Holding of generated holes after W1 operation in the RFET is of paramount importance for 1T-DRAM with enhanced RT. Due to a variation in L_{CG} and L_{GAP}, RFET architectures with different L_S require optimized H and R biases along with optimized W1 bias. Due to non-optimal H and R biases, RFETs with L_S = 60 nm and 80 nm exhibit poor SM (Fig. 3.3 (d)). In general, to hold excess carriers in RFET with a longer storage region, a more negative $V_{BCG,H}$ is needed. However, in RFET-based 1T-DRAM, a less negative $V_{BCG,H}$ is essential for achieving a higher L_S (for a fixed L_T) for optimal retention, as shown in Fig. 3.4 (a). A more negative $V_{BCG,H}$ in longer L_S (shorter L_{PG}) leads to the degradation of the H0 state due to the higher lateral field between S/D and back CG. Hence, RFETs with L_S = 60 nm and 80 nm need to be operated at a less negative $V_{BCG,H}$ (-1.2 V), as shown in Fig. 3.4

(a). RFET with higher L_S (60 nm and 80 nm) can sustain the recombination in H1 even at less negative back CG bias.

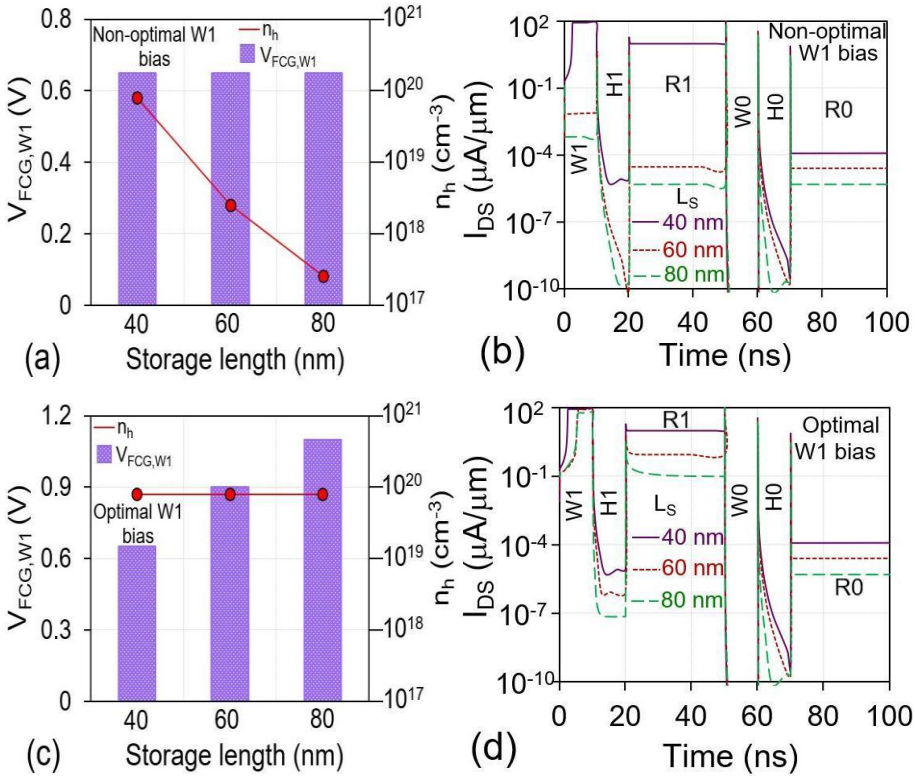

Fig. 3.3 (a) Excess hole concentration (n_h) generated for different L_S values (40 nm, 60 nm, and 80 nm) at $V_{FCG,W1}$ = 0.65 V. (b) Current transient for various L_S values for the same biases (non-optimal for L_S = 60 nm and 80 nm) shown in Table 3.2. (c) Comparison of optimal front CG W1 bias ($V_{FCG,W1}$) for different L_S. (d) Comparison of the current transient for various L_S with optimized $V_{FCG,W1}$. L_{CG} is 20 nm for L_T of 100 nm in each L_S, i.e., 40 nm, 60 nm, and 80 nm.

In RFET with a longer L_{PG} or shorter L_S, a more negative $V_{BCG,H}$ (-1.3 V), is essential to sustain holes in the H1 state. A more negative $V_{BCG,H}$ (-1.3 V) in shorter L_S does not result in enhanced hole generation in H0 state as compared to L_S with 60 nm and 80 nm due to the longer L_{PG}, which reduces the impact of the lateral field. The resistance offered by each RFET topology primarily depends on L_{GAP} and L_{CG}. Hence, for the same read bias (0.3 V), the SM of the RFET with longer L_S is expected to be lower, even after generating sufficient carriers (Fig. 3.4

(b) and (c)). As shown in Fig. 3.4 (c), the RT of RFET with longer L_S (60 nm and 80 nm) is also on the lower side (less than 100 ms) due to fast degradation in I_1.

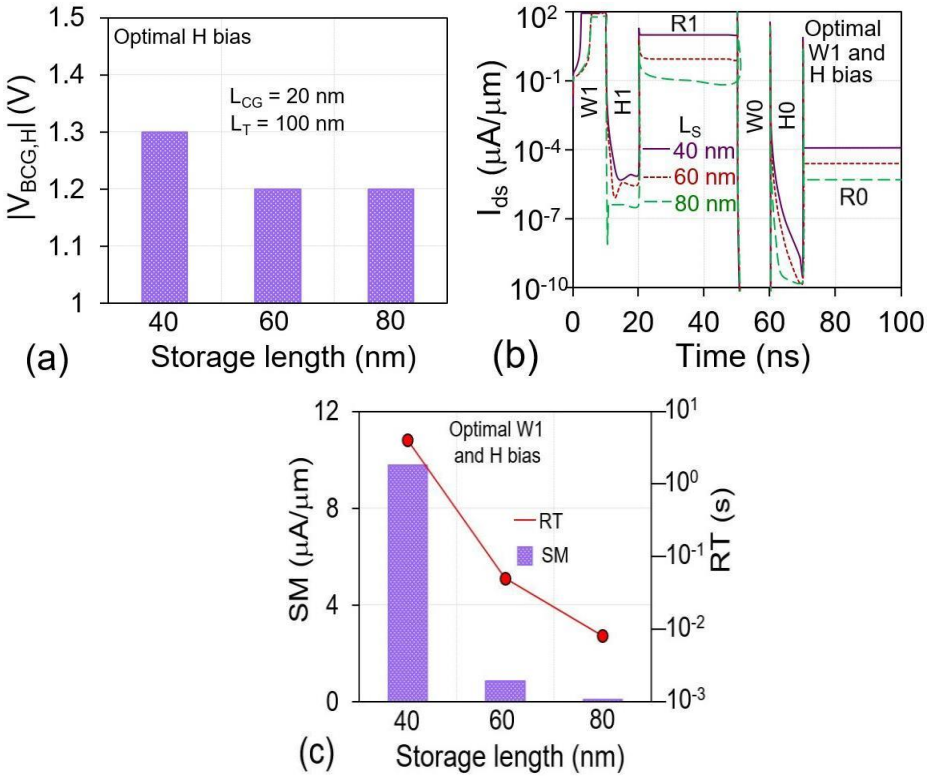

Fig. 3.4 (a) Optimized back CG bias ($V_{BCG,H}$) requirement for hold operation for different L_S values. (b) Comparison of current transient for various L_S values with optimized $V_{FCG,W1}$ and $V_{BCG,H}$. (c) Variation of RT and SM for different L_S values with optimized $V_{FCG,W1}$, and $V_{BCG,H}$ but at a non-optimal $V_{FCG,R}$. L_{CG} is 20 nm for L_T of 100 nm in each L_S, i.e., 40 nm, 60 nm, and 80 nm.

3.3.3 Bias Optimization for Read Operation

Along with W1 and H, the R operation (R1 and R0) also plays an important role in 1T-DRAM functioning because it senses the hole concentration (through current) available after H1 and H0 operations. During R1 operation, weak impact ionization prevents the degradation of R1 state for a relatively longer H time. However, if RFET exhibits lower SM, a relatively fast degradation in R1 current results in a lower RT as shown in Fig. 3.4 (c). Thus, RFET with longer L_S essentially requires a higher $V_{FCG,R}$ to achieve a good SM and RT i.e. $V_{FCG,R}$ = 0.4

V for L_S = 60 nm, and $V_{FCG,R}$ = 0.55 V for L_S = 80 nm (Fig. 3.5 (a)). An increase in $V_{FCG,R}$ results in an enhancement in I_1 and I_0, and all RFET architectures attain comparable SM and CR as shown in Fig. 3.5 (b) as compared to Fig. 3.4 (b). However, I_0 is degraded in RFET with longer L_S (60 nm and 80 nm), and hence, a lower RT is achieved. Thus, a longer L_S (for a fixed L_T) does not necessarily translate into an enhanced RT. From Fig. 3.5 (c), it is clear that for the same L_{CG} (= 20 nm), a device with lower L_S (= 40 nm) shows a higher RT among other topologies because of an optimal separation of storage region from S/D.

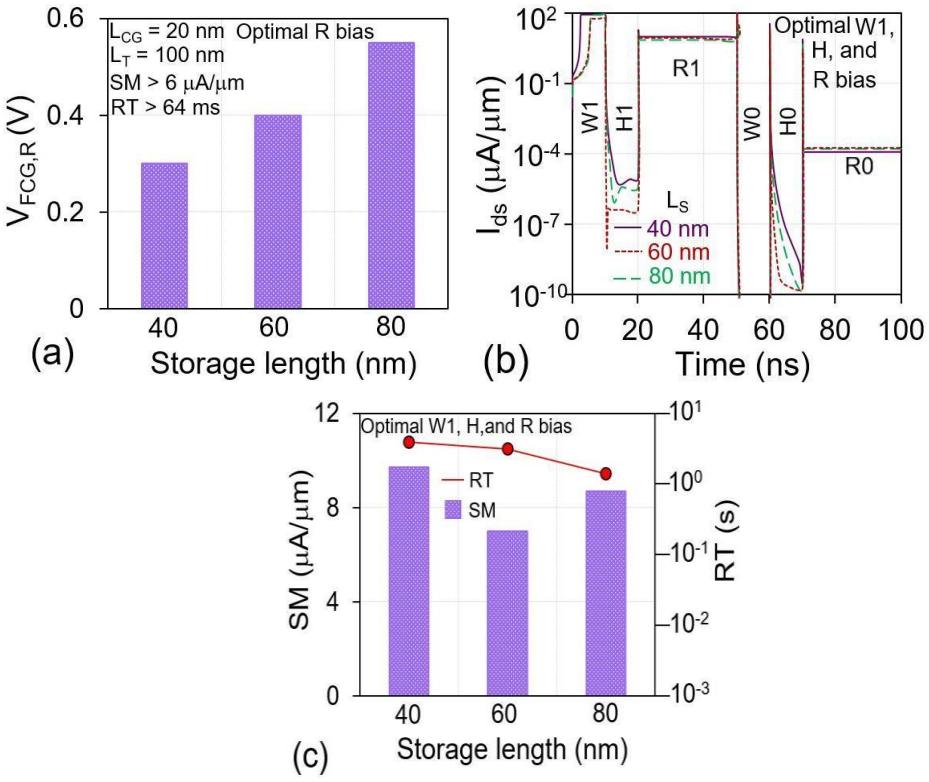

Fig. 3.5 (a) Comparison of optimal front CG read bias ($V_{FCG,R}$) for different L_S values. (b) Comparison of current transients for various L_S with optimized $V_{FCG,W1}$, $V_{BCG,H}$, and $V_{FCG,R}$. (c) Variation of RT and SM for different L_S with optimized $V_{FCG,W1}$, $V_{BCG,H}$, and $V_{FCG,R}$. L_{CG} is 20 nm for L_T of 100 nm in each L_S, i.e., 40 nm, 60 nm, and 80 nm.

3.4 Impact of Non-Optimal Bias on Retention Time

Optimal bias during H and R operations is the bias that leads to maximum RT in any L_S i.e. 40 nm, 60 nm, and 80 nm. However, the bias higher or lower than the optimal value during the H and R operation can lead to degraded RT. The application of non-optimal bias during H can lead to enhanced generation and recombination, whereas during R operation, non-optimal biases can increase or decrease the rate of I_1 and I_0 with t_{HOLD}. Hence, in this section, the impact of non-optimal H and R biases on RT is investigated.

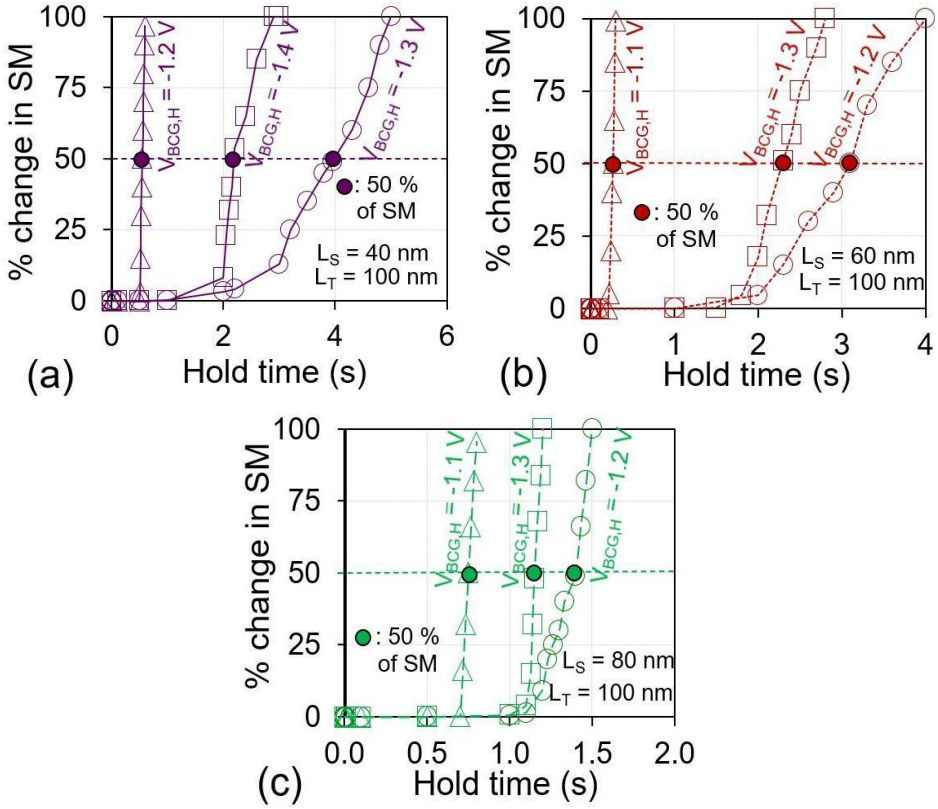

Fig. 3.6 Variation in percentage change in SM with the hold time (t_{HOLD}) for biases above and below the optimized $V_{BCG,H}$ for (a) L_S = 40 nm, (b) L_S = 60 nm, and (c) L_S = 80 nm.

3.4.1 Variation in Retention Time with Non-Optimal Hold Bias

After the W1 operation is performed, the RT in RFET based 1T-DRAM is affected due to the application of non-optimal bias at the back CG during hold and

front CG during read operation. To showcase the impact of non-optimal bias during H operation, the percentage change in SM with t_{HOLD} is shown in Fig. 3.6 (a)-(c) for various H biases i.e. 100 mV above and below the optimal $V_{BCG,H}$. Deviation in $V_{BCG,H}$ from the optimal bias leads to enhanced recombination and generation during H1 and H0, respectively, which degrades SM as shown in Fig. 3.6 (a)-(c). A higher recombination rate during H1 severely affects I_1, whereas an increase in hole generation during H0 deteriorates the I_0 current at a faster rate. However, non-optimal H bias does not affect SM because SM is calculated after a shorter t_{HOLD} of 10 ns. Its effect on read current can be observed if RFET holds the holes for a longer duration (longer t_{HOLD}) as generation and recombination increase with t_{HOLD}. All RFETs (with L_S = 40 nm, 60 nm, and 80 nm) show lower RT if a less negative $V_{BCG,H}$ is used (than the optimal H bias) due to the sharp degradation of state '1' (due to recombination in H1). However, a more negative $V_{BCG,H}$ bias (in comparison to optimal) also leads to the degradation of RT because of the degradation of state '0' (due to generation in H0), although at a lower rate. The degradation in state 1 is higher because recombination in H1 sharply deteriorates the I_1. Consequently, SM is degraded.

3.4.2 Variation in Retention Time with Non-Optimal Read Bias

To demonstrate the impact of non-optimal bias during R operation, a bias value being 50 mV above and below the optimal $V_{FCG,R}$ is considered, and the corresponding effect on RT is estimated by evaluating the percentage change in SM. Similar to H operation, the deviation in $V_{FCG,R}$ from optimal bias leads to degradation in I_1 and I_0, which degrades the SM as shown in Fig. 3.7 (a)-(c). SM degrades at a faster rate (due to sharp deterioration in I_1) at a lower read bias than that for an optimal $V_{FCG,R}$ in RFET with L_S = 40 nm and 60 nm, and RFET eventually ends up exhibiting lower RT as shown in Fig. 3.7 (a)-(c). RFET with L_S = 80 nm shows enhanced RT (greater than the optimal) due to a lower rate of degradation in I_1 at lower $V_{FCG,R}$ because of a longer underlap region as shown in Fig. 3.7 (c). However, a longer underlap causes SM to reduce below 6 µA/µm for RFET with L_S = 80 nm. At a higher read bias, the rate of degradation of I_0 current

governs RT. Hence, a faster degradation in SM in RFET for L_S = 80 nm leads to a reduced RT as compared to the other two topologies (L_S = 40 nm and 60 nm).

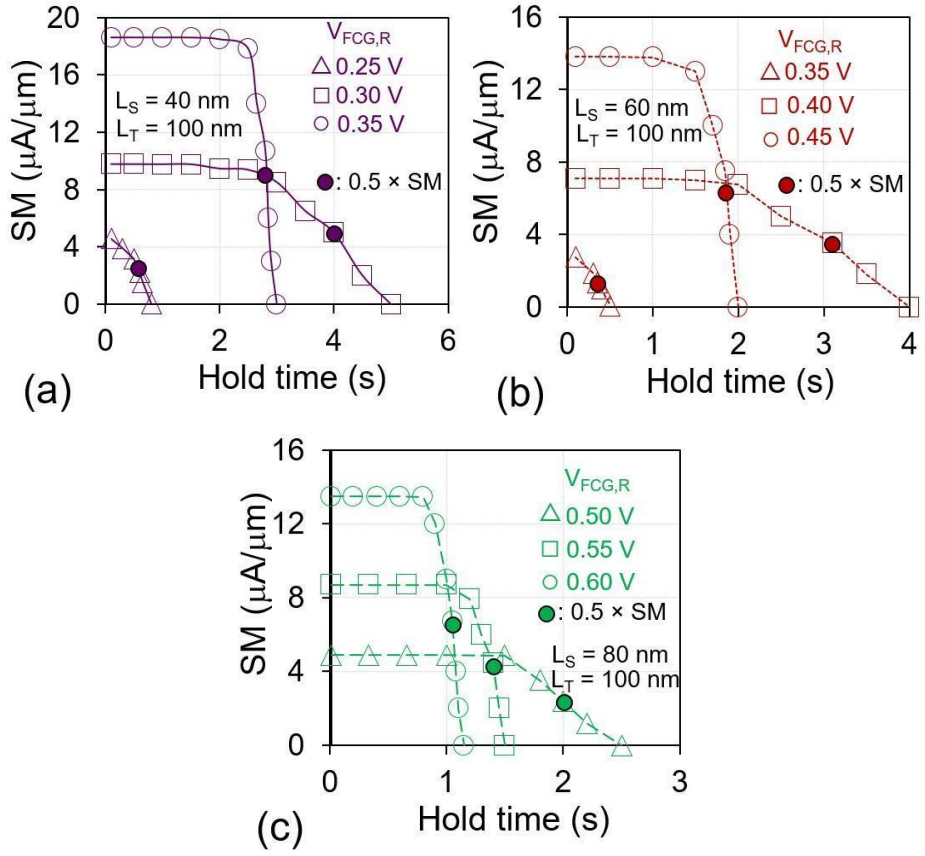

Fig. 3.7 Variation in SM with the hold time (t_{HOLD}) for biases above and below the optimized $V_{FCG,R}$ for (a) L_S = 40 nm, (b) L_S = 60 nm, and (c) L_S = 80 nm.

3.5 Control Gate Length Dependent Bias Optimization

The storage length comprises of L_{CG} and L_{GAP} in RFET based 1T-DRAM. L_{GAP} and L_{CG} regions have different contributions on the performance of 3G-RFET i.e. subthreshold swing (SS) varies from 62 mV/dec to 80 mV/dec for various combinations resulting in L_S = 40 nm, 61 mV/dec to 71 mV/dec for different combinations resulting in L_S = 60 nm, and 60 mV/dec to 67 mV/dec for different combinations resulting in L_S = 80 nm (for fixed L_T = 100 nm) as listed in Table 3.1. The variation in SS is due to different L_{CG} values for the given storage region (L_S). Hence, the contribution of L_{CG} and L_{GAP} in L_S can significantly affect the requirements of W1, H, W0, and R biases, while also impacting RT and SM.

Amongst these two lengths (L_{GAP} and L_{CG}), L_{CG} is critical for the storage region as it governs the storage of holes under the back CG.

The optimal $V_{BCG,H}$ during H operation and $V_{FCG,R}$ during R operation for each L_{CG} is shown in Fig. 3.8 (a), (c), and (e). The corresponding SM and RT values are also shown in Fig. 3.8 (b), (d), and (f). For a fixed L_S = 40 nm, an increase in L_{CG} shifts $V_{BCG,H}$ to more negative values (to hold excess holes) as shown in Fig. 3.8 (a) i.e. $V_{BCG,H}$ of -1.2 V and -1.4 V for L_{CG} = 10 nm and 30 nm, respectively, is more appropriate for 1T-DRAM operation. For L_S = 40 nm, L_{GAP} varies from 5 nm (L_{CG} = 30 nm) to 15 nm (L_{CG} = 10 nm). A shorter L_S (or L_{CG}) indicates an enhanced degree of SCEs in RFET, which tends to increase the current drive. Consequently, SM increases with a reduction in L_{CG} from 30 nm to 15 nm (for L_S = 40 nm) for the same read bias of 0.3 V. RFET designed with L_{CG} = 10 nm and operating at the same read bias, will not be optimal as a faster degradation of I_0 due to SCEs is envisaged. Therefore, RFET with L_{CG} = 10 nm has been operated at a relatively low read bias (0.25 V), as shown in Fig. 3.8 (a), which also lowers SM, as shown in Fig. 3.8 (b). SM varies from 7.4 µA/µm to 11.2 µA/µm with L_{CG} for a fixed L_S = 40 nm. Also, an increase in L_{CG} results in an enhancement of RT with values (> 64 ms) ranging from 1.5 s to 6.1 s (Fig. 3.8 (b)).

RFET based 1T-DRAM with L_S = 60 nm also requires a more negative $V_{BCG,H}$ with increasing L_{CG} as shown in Fig. 3.8 (c). In this case, L_{GAP} varies from 5 nm (L_{CG} = 50 nm) to 25 nm (L_{CG} = 10 nm). Due to the relatively longer L_{GAP} with L_S = 60 nm, SCEs are suppressed in comparison to RFET with L_S = 40 nm. Thus, 1T-DRAM can attain SM > 6 µA/µm for all L_{CG} for a $V_{FCG,R}$ of 0.4 V (Fig. 3.8 (d)). As read bias is the same for each L_{CG}, SM marginally varies from 7.1 µA/µm to 8.1 µA/µm. SM degrades as L_{CG} reduces from 40 nm to 20 nm (unlike the case corresponding to L_S = 40 nm) due to the relatively lower degree of SCEs and the higher resistance offered by the longer L_{GAP}. At lower L_{CG} values (< 20 nm), SM increases even with a longer L_{GAP} because of a higher degree of SCEs corresponding to a shorter L_{CG}. Even for L_{CG} > 40 nm, SM decreases even for shorter L_{GAP} because of a reduction in the resistive component for L_{GAP} < 10 nm.

RT increases with an increase in L_{CG} for L_S = 60 nm due to enhanced storage region length, and RT lies in a range of 1.1 s to 8.7 s (Fig. 3.8 (e)).

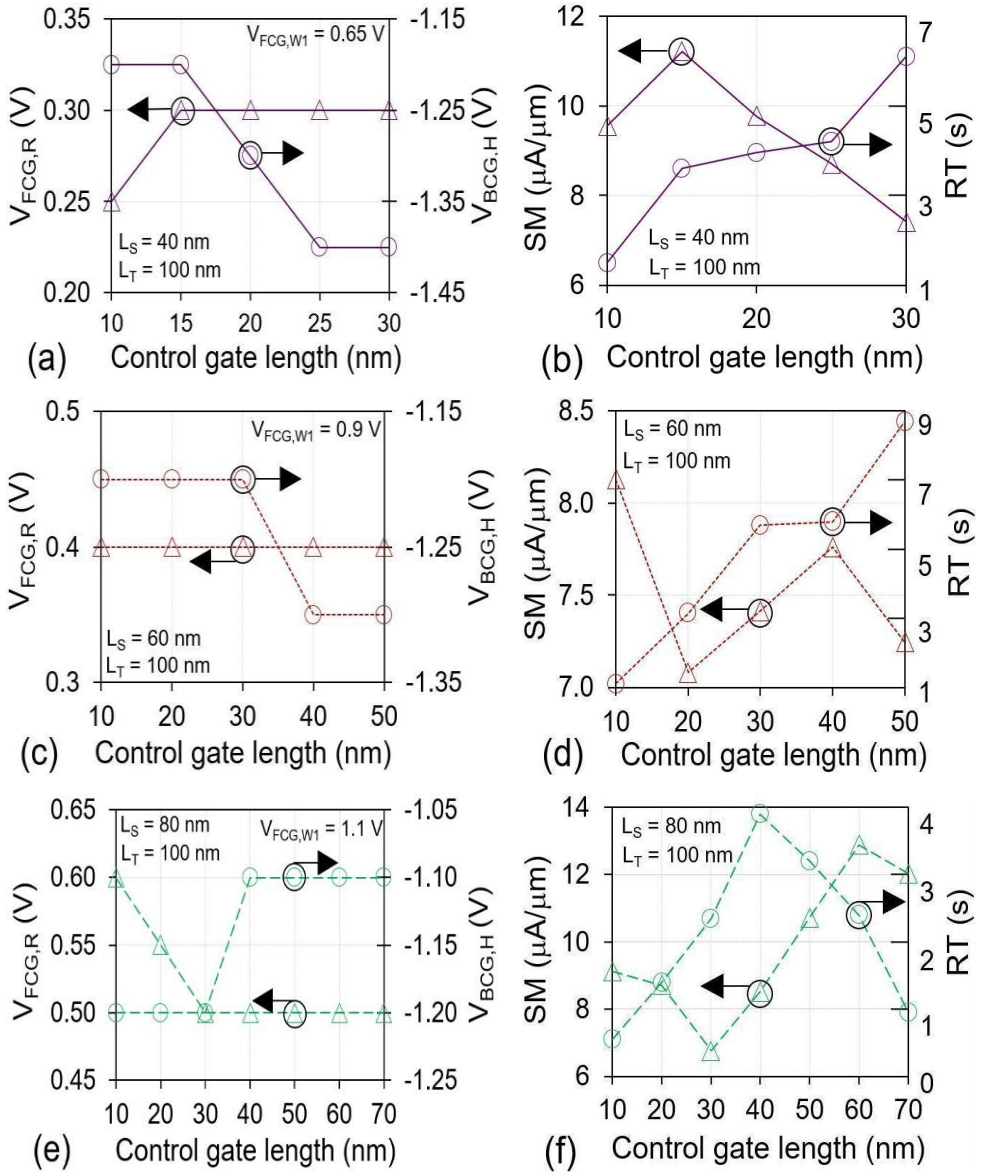

Fig. 3.8 (a) Variation of optimal back CG hold bias ($V_{BCG,H}$) and front CG read bias ($V_{FCG,R}$) with control gate length (L_{CG}) and corresponding (b) SM and RT for L_{CG} in L_S = 40 nm. (c) Variation of optimal back CG hold bias ($V_{BCG,H}$) and front CG read bias ($V_{FCG,R}$) with control gate length (L_{CG}) and corresponding (d) SM and RT for L_{CG} in L_S = 60 nm. (e) Variation of optimal back CG hold bias ($V_{BCG,H}$) and front CG read bias ($V_{FCG,R}$) with control gate length (L_{CG}) and corresponding (f) SM and RT for L_{CG} in L_S = 80 nm.

RFET with a longer L_{CG} (for a fixed L_T) always requires a more negative $V_{BCG,H,}$ for optimal performance. However, a more negative $V_{BCG,H}$ causes an increase in the lateral electric field between S/D and the back CG. This triggers weak impact ionization during H0, and consequently, state '0' degrades. By maintaining the storage region away from S/D through a longer L_{PG}, the effect of the lateral field can be reduced. Thus, the RT of 1T-DRAM with a higher L_S value is severely degraded due to the state '0' if the device operates at a more negative $V_{BCG,H}$. For longer L_{CG} values, a reduction in L_{GAP} enhances the field between S/D and back CG during H0 operation. If L_{PG} is relatively longer (20 nm for L_S = 60 nm and 30 nm for L_S = 40 nm), the lateral electric field can be suppressed which lowers the extent of degradation of the H0 state, and an enhanced RT (for higher L_{CG}) is obtained. However, if RFET with a lower L_{PG} (10 nm for L_S = 80 nm) operates at a more negative $V_{BCG,H}$, a significant degradation in H0 state is observed due to the relatively higher values of the lateral electric field. For higher RT (> 64 ms at 85 °C) at longer L_{CG} (from 40 nm to 70 nm for L_S = 80 nm), a less negative $V_{BCG,H}$ i.e., -1.1 V as compared to -1.2 V for RFET with lower L_{CG} (10 nm to 30 nm for L_S = 80 nm) should be considered. For RFET with an L_S of 80 nm, the L_{GAP} varies from 5 nm to 35 nm.

For the same $V_{FCG,R}$ (0.5 V), RFET can attain SM > 6 µA/µm for L_{CG} values in between 30 nm and 70 nm (Fig. 3.8 (e)) even though the degradation in SM can be observed for L_{CG} lying within the range 60 nm (L_{GAP} = 5 nm) to 30 nm (L_{GAP} = 25 nm) as shown in Fig. 3.8 (f). When the same read bias (0.5 V) is applied to RFET with shorter L_{CG} values (10 nm and 20 nm), a poor SM is observed (< 6 µA/µm) due to a longer L_{GAP} (30 nm and 35 nm). Thus, to obtain a decent SM, RFET with lower L_{CG} (10 nm and 20 nm) requires a slightly higher $V_{FCG,R}$ i.e., 0.6 V and 0.55 V for L_{CG} = 10 nm and 20 nm, respectively. Due to the relatively higher $V_{FCG,R}$, a slight improvement in SM can be observed compared to L_{CG} = 30 nm. Additionally, at higher L_{CG} (> 60 nm), SM decreases even with a shorter $L_{GAP.}$ A longer L_{PG} helps reduce the impact of S/D on the storage region. Thus, for a longer L_{PG}, increasing L_{CG} (for L_S = 40 nm and 60 nm) enhances RT because of the longer L_S afforded by a longer L_{CG}. In RFET with higher L_S (= 80 nm), RT initially increases with L_{CG}

(because of longer storage region), and thereafter, decreases at L_{CG} (> 40 nm) due to the degradation of state 0 due to higher lateral field. As a result, RT varies from 550 ms to 3.9 s for L_S = 80 nm. It can be observed that RFET based 1T-DRAM can achieve an appreciable SM (> 6 μA/μm) and RT (> 64 ms), provided optimal bias is applied at the terminals.

3.6 Feasibility of RFET for On-Chip 1T-DRAM

Recently, on-chip memory has been gaining significant attention due to the increasing number of cores. The data-hungry cores require large amounts of data to process on a regular basis. The off-chip memory often fails to provide data to the powerful cores at a high speed due to its limited bandwidth and relatively slow read/write performance. Operating memory close to the core results in an enhanced bandwidth, which helps the cores process data more quickly. However, these on-chip memory needs to perform write/read operations at a relatively higher speed to fulfill the data required for the core. Since SM and RT are highly dependent on operating W1 and R time, analyzing RFET-based 1T-DRAM with faster access time is essential for on-chip applications.

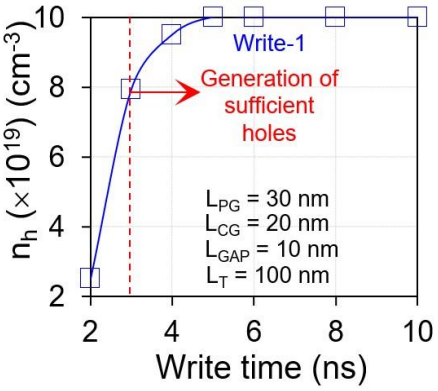

Fig. 3.9 Variation of hole concentration (n_h) at back surface of RFET during write 1 (W1) for various values of write time (t_{W1} = 2 ns to 10 ns). All biases are mentioned in Table 3.2.

3.6.1 Impact of Write Time Reduction on Hole Concentration

In the above analysis (in section 3.2.1) for L_S = 40 nm (L_{CG} = 20 nm), a relatively higher t_{W1} (= 10 ns), t_{W0} (= 10 ns), and t_R (= 30 ns) were considered. However, in the case of on-chip 1T-DRAM (embedded 1T-DRAM), a much lower t_{W1}, t_{W0}, and t_R is required for fast memory access. The t_{W1} of 1T-DRAM is limited by the mechanism responsible for generating excess holes. In RFET-based 1T-DRAM, excess holes are generated through the positive feedback mechanism induced by weak impact ionization [207]. Fig. 3.9 shows that RFET can generate sufficient excess holes (~10^{20} cm^{-3}) in a relatively short t_{W1} between 4 ns and 10 ns. However, hole concentration reduces to ~7.9×10^{19} cm^{-3} for a t_{W1} of 3 ns. RFET can only function with SM (~9.7 µA/µm) and RT (~3.95 s) up to 3 ns of t_{W1}. SM reduces to a value lower than 6 µA/µm for a t_{W1} of 2 ns because of the reduced hole concentration (~2.5×10^{19} /cm^3). Therefore, for RFET designed with L_{GAP} = 10 nm, L_{PG} = 30 nm, and L_{CG} = 20 nm, t_{W1} can be lowered to 3 ns without any significant degradation in RT and SM. Faster W1 operation with RFET can also result in reduced energy consumption. Lower energy consumption is a prerequisite for embedded memory applications.

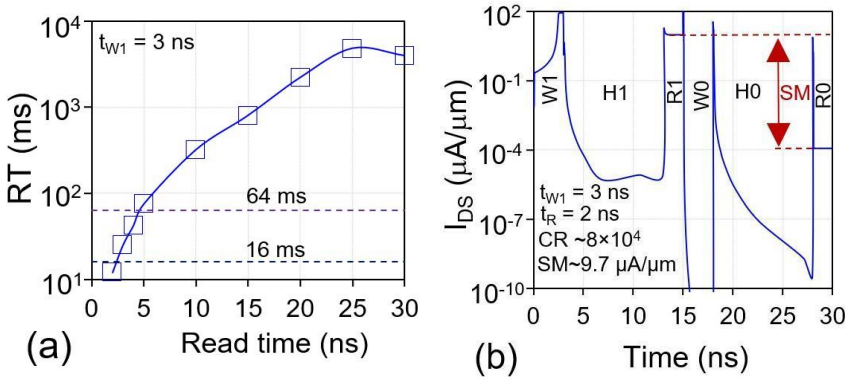

Fig. 3.10 (a) Variation of RT with read time (t_R = 2 ns to 30 ns) for a fixed t_{W1} of 3 ns. (b) Current transient for a minimum t_{W1} (3 ns) and t_R (2 ns). Parameters: L_{PG} = 30 nm, L_{CG} = 20 nm, L_{GAP} = 10 nm and L_T = 100 nm. All biases are mentioned in Table 3.2.

Table 3.4: Benchmarking of RFET based 1T-DRAM with existing topologies.

Device	L_T (nm)	t_{W1} (ns)	t_{R1} (ns)	RT (ms)	SM (µA/µm)	Reconfigur-able
FD-SOI [220]	350	5	5	100	12	No
DG-FinFET [221]	60	1	2	10	5	
Z^2FET [222]	60	1	1	150	39	
TFET [223]	245	5	50	600	0.18	
R-S/D MOSFET [224]	30	5	10	15	3.3	
2G-RFET [204]	100	1	2	560	21	Yes
	60	1	2	60	31	
This work	100 (L_S = 40 nm)	5	2	40	7.4	
	100 (L_S = 60 nm)	1	2	30	7.2	
	100 (L_S = 80 nm)	2	6	35	8.5	

3.6.2 Impact of Read Time Reduction on Retention Time

The impact of t_R on RT is shown in Fig. 3.10 (a) where t_R varies from 2 ns to 30 ns for a fixed t_{W1} of 3 ns. A minimum t_{W1} of 3 ns ensures SM > 6 µA/µm for all values of t_R. RT is limited by the degradation of both I_1 and I_0. For a longer t_R (> 25 ns), I_0 rises, which causes a degradation in RT from 4.8 s (t_R = 25 ns) to 3.95 s (t_R = 30 ns). However, for a smaller t_R (< 25 ns), I_1 is degraded, and hence, a

degradation in RT occurs. For a t_R of 5 ns, 1T-DRAM shows an RT of 75 ms (> 64 ms), indicating suitability for standalone 1T-DRAM. Also, a retention time of 25 ms (> 16 ms) is achieved for a smaller t_R of 3 ns, which also reflects the potential for embedded applications. Fig. 3.10 (b) shows the current transient, indicating feasible memory operation for a minimum t_{W1} and t_R of 3 ns and 2 ns, respectively.

3.6.3 Benchmarking

The impact of various architectures on t_R and t_{W1} has been demonstrated for RFETs with maximum RT (Fig. 3.8 (b), (d), and (f)). The architecture considered are L_S = 40 nm (L_{CG} = 30 nm), L_S = 60 nm (L_{CG} = 50 nm), and L_S = 80 nm (L_{CG} = 40 nm). Apart from the operating bias requirement, SM and RT, t_R, and t_{W1} will be function of individual lengths of the RFET. $V_{FCG,W1}$ shown above has been optimized for L_S = 40 nm, L_S = 60 nm, and L_S = 80 nm for a fixed L_{CG} = 20 nm to generate sufficient excess holes for a t_{W1} of 10 ns. However, in RFET, the minimum t_{W1} to generate excess holes varies with the contribution of L_{CG} and L_{GAP}. The optimal RFET with L_S = 40 nm (L_{CG} = 30 nm) exhibits a lower degree of impact ionization compared to a device designed with L_S = 40 nm (L_{CG} = 20 nm) due to its higher L_{CG}. RFET with L_S = 40 nm (L_{CG} = 30 nm) will not be able to generate sufficient excess holes below a t_{W1} of 5 ns. RFET designed with L_S = 60 nm (L_{CG} = 50 nm) shows a greater degree of impact ionization as compared to a device with L_S = 60 nm (L_{CG} = 20 nm) at $V_{FCG,W1}$ = 0.9 V because of the shorter ungated region. Thus, RFET with L_S = 60 nm (L_{CG} = 50 nm) generates sufficient excess holes at $V_{FCG,W1}$ = 0.9 V even with a minimum t_{W1} of 1 ns. RFET with L_S = 80 nm (L_{CG} = 40 nm) exhibits a greater degree of impact ionization as compared to a device with L_S = 80 nm (L_{CG} = 20 nm) for $V_{FCG,W1}$ = 1.1 V because of a shorter ungated region. Thus, RFET with L_S = 80 nm (L_{CG} = 40 nm) can generate sufficient excess holes at $V_{FCG,W1}$ = 1.1 V for a minimum t_{W1} of 2 ns.

The minimum t_R strongly depends on I_1, which is significantly affected by the length of the ungated region. RFET with L_S = 80 nm (L_{CG} = 40 nm) and L_{GAP} = 20 nm offers high resistance and consequently limits the minimum t_R to 6 ns. However, other RFET architectures with L_S = 40 nm (L_{CG} = 30 nm) and L_S = 60

nm (L_{CG} = 20 nm) offer low resistance, and a minimum t_R of 2 ns is feasible. Thus, RFET with L_S = 60 nm can outperform other RFET topologies (L_S = 40 nm and L_S = 80 nm) by functioning at lower t_{W1} (1 ns) and t_R (2 ns), as shown in Table 3.4. The results indicate that 3G-RFET (with optimum dimension and operating biases) can be a promising solution for high-speed and high-density 1T-DRAM. Zero-impact ionization zero-slope (Z^2FET) [222] can potentially limit its use for high-density processor design. Additionally, the requirement for gate misalignment in twin-gated (2G) RFET [204] necessitates extra and complex fabrication steps, which can be a limiting factor for large-scale integration. However, the RFET analyzed in this work can function with a minimum t_{W1} and t_R of 1 ns and 2 ns, respectively (L_S = 60 nm and L_{CG} = 50 nm), which indicates its potential inclusion in a system-on-chip application where a smaller device footprint is a primary concern.

3.7 Fabrication Flow of RFET

The step-by-step fabrication flow of RFET is shown in Fig. 3.11. The process starts with the formation of a lightly p-type-doped Silicon-on-Insulator substrate. In the RFET architecture, the channel can be patterned into the desired shape using electron beam lithography [225], followed by the formation of a SiO_2 layer via dry oxidation [225]. Then, the Schottky-barrier (SB) region is patterned using electron-beam lithography. After that, a polysilicon layer is deposited (conformal polysilicon deposition) with the same mask (length L_{CG}) to form CG and PG. For independent gate operation, Chemical Mechanical Polishing (CMP) is employed to separate the gates [226]. After forming an independent gate, a nickel layer is deposited by sputtering, and a specific annealing process is performed to form NiSi at the S/D [225]. The process and flow mentioned above are based on well-known technology, which has already been used in literature to implement nanowire and fin-shaped RFET structures [225], [227] and an independent gate [226] DG structure. Thus, by maturing the technology, it is possible to integrate the proposed RFET structure, which can be used as a capacitorless DRAM while retaining its reconfigurability feature.

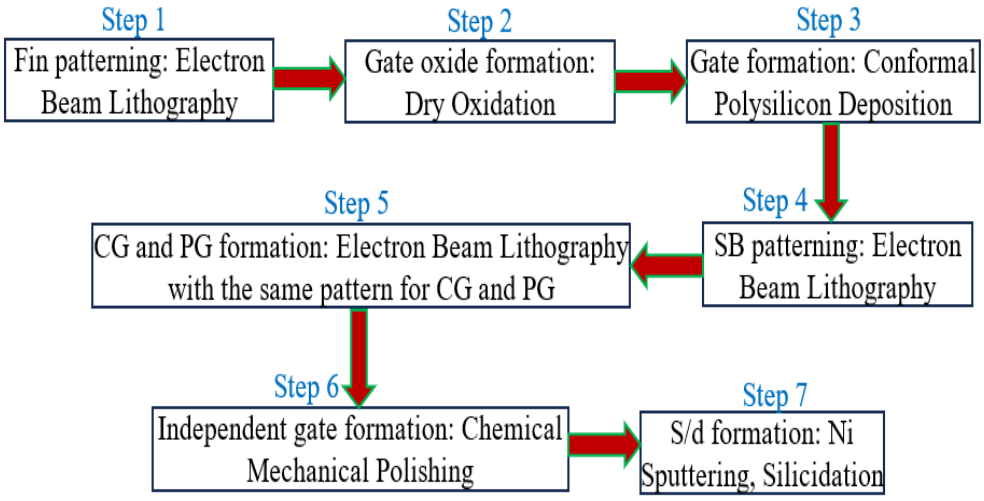

Fig. 3.11 Possible fabrication flow for RFET structure through well-known fabrication steps used in [225], [227].

Quantum confinement effects are observed in a device when the T_{Si} and T_{OX} reach below 10 nm and 1 nm, respectively, [228]. However, in this work, the considered values of T_{Si} and T_{OX} are not below 10 nm and 1 nm, respectively. Hence, the quantum confinement effect does not affect the device performance. If the Si thickness is scaled below 10 nm, quantum confinement in the vertical direction will occur. This confinement will be similar to that in a SOI MOSFET and can be estimated through the self-consistent solution of Poisson's and Schrodinger's equations.

3.8 Impact of Traps on SM and RT

In a non-ideal Schottky contact, the Schottky barrier height (SBH) gets affected by Fermi-level pinning due to traps at the M-S interface [229], whereas these effects are absent in an ideal Schottky contact. The Fermi level pinning can lead to an increase in the SBH in non-ideal Schottky contacts. An increase in SBH due to Fermi level pinning depends on the work function of the metal and the interface trap charge density [229]. For a typical M-S interface with a trap charge density (D_{it}) of 10^{12} cm^{-2} eV^{-1}, SBH for electrons increases from 0.35 eV to 0.43 eV, which causes degradation in SM as shown in Fig. 3.12 (a). Along with non-

ideal Schottky contacts (presence of traps in M-S junction), the 1T-DRAM performance is also affected by traps formed at the Si/SiO_2 interface (due to an immature fabrication process). The traps at the Si/SiO_2 interface become a hindrance for 1T-DRAM performance by increasing the recombination rate [13]. Thus, traps can affect the carrier lifetime [230] that governs the RT of the 1T-DRAM. To capture the effect of traps on RT, a lower carrier lifetime (10 ns instead of 76 ns at 358 K) has been considered [230]. To consider the impact of traps (at Schottky contact and Si/SiO_2 interface) on various RFET architectures, three different topologies that have shown maximum RT have been considered, and the same is shown in Table 3.5.

Table 3.5: Retention time (RT) of three different topologies without traps.

L_S (nm)	L_{CG} (nm)	L_T (nm)	L_S/L_T	RT (s)
40	30	100	0.4	6.1
60	50	100	0.6	8.7
80	40	100	0.8	3.9

Table 3.6: Retention time (RT) of three different topologies with traps.

L_S (nm)	L_{CG} (nm)	L_T (nm)	L_S/L_T	RT (ms)
40	30	100	0.4	900
60	50	100	0.6	1300
80	40	100	0.8	500

The increased SBH at M-S junctions due to Fermi-level pinning primarily degrades $I_{BL,R1}$ after read 1 operation (at the same bias at each terminal), leading to a reduction in the SM of the 1T-DRAM, as shown in Fig. 3.12 (a). In the presence

of traps, RT reduces to ~900 ms (from 6.1 s), ~1300 ms (from 8.7 s), and 500 ms (from 3.9 s) for $L_S/L_T = 0.4$ ($L_{CG}/L_T = 0.3$), $L_S/L_T = 0.6$ ($L_{CG}/L_T = 0.5$), and $L_S/L_T = 0.8$ ($L_{CG}/L_T = 0.4$), respectively at 85 °C as shown in Fig. 3.12 (b). Even though RT is reduced in the presence of traps, it remains above 64 ms.

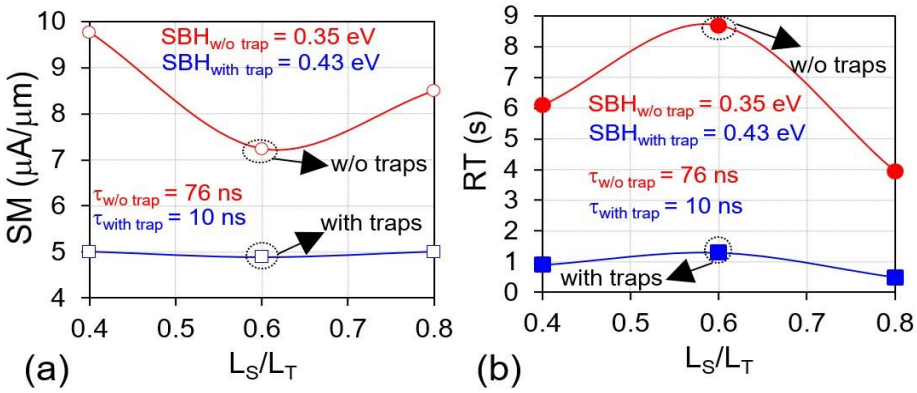

Fig. 3.12. Impact of traps on (a) sense margin (SM) and (b) retention time (RT) of RFET based 1T-DRAM.

3.9 Conclusion

In this chapter, the length-dependent constraints for feasible 1T-DRAM operation in nanoscale RFETs are critically investigated. Results indicate that RFET exhibits higher values of RT and SM over a broader range of L_{CG}. The analysis shows that a longer L_S (for a fixed L_T) does not necessarily imply enhanced RT. Retention can be improved by maximizing L_{CG} for moderate or lower L_S (40 nm to 60 nm). For a longer L_S (> 80 nm), RT can be maximized by ensuring $L_{CG}/L_S \approx 0.5$. An optimally designed RFET with $L_S = 60$ nm with $L_{CG} = 50$ nm outperforms other topologies with best retention ~8.7 s due to advantages attributed to appropriate values of L_{CG} at fixed L_T, which suppresses the degradation of state 0. The SM of RFET-based 1T-DRAM lies within the range of 7 µA/µm to 13 µA/µm with a minimum CR of ~10^4 for all architectures. The SM and RT is further reduced in the presence of traps. However, the values remain higher than 64 ms. Results. The enhancement in SM and RT is further possible with appropriate bias selection for memory operations. while showcasing new insights, highlight the versatility of optimally designed nanoscale RFET for utility as 1T-DRAM. Additionally, an

optimally designed RFET-based 1T-DRAM (L_S = 60 nm and L_{CG} = 50 nm) demonstrates feasibility for operation at lower t_{W1} and t_R values of 1 ns and 2 ns, respectively, making it a viable alternative for on-chip memory.

Chapter 4

Word Line and Bit Line Disturbance in Nanowire Gate-All-Around RFET

4.1 Introduction

The compatibility with CMOS process, low write latency, and low power consumption favorably position 1T-DRAM for on-chip (embedded) memory [231]. The RT of DRAM typically ranges from tens of microseconds to a few milliseconds [232], which often demands energy-consuming refresh cycles. Traditionally, 1T-DRAM has been realized in planar CMOS technologies, such as FD-SOI and DG MOSFET, through substrate biasing or independent gate biasing to create a lower potential region for storing holes [160]. While independent gate biasing is feasible in a planar transistor architecture, a NW gate-all-around (GAA) transistor topology capable of high integration density may not permit the same [233]. Hence, a transistor architecture compatible with logic technology and supporting 3-dimensional (3D) integration [234] may not be suitable for 1T-DRAM. The challenge is to design a transistor architecture compatible with logic and on-chip memory to enhance the data transfer rate between the processor and memory block [235].

1T-DRAM operation has been realized through 4 to 6 distinct voltage levels (in addition to 0 V) [174], [185], [199], [200], [204], [224], [236]. While multiple bias levels ensure higher charge retention [204], [174], it comes with the requirement of additional voltage blocks to generate different biases along with associated routing complexities [237]. The non-availability of a back bias-induced dedicated charge storage region in NW GAA transistors can be circumvented by using RFET. As already demonstrated, RFETs have shown significant potential for

high-density logic applications when comparing the transistor count to implement logic functionality. The challenge in implementing on-chip capacitorless DRAM, i.e., 1T-DRAM with NW GAA RFET, is to minimize the number of voltage levels (n_{VL}), reduce refresh rates, and achieve low t_{W1} and t_R, while maintaining lower energy consumption with a logic-compatible V_{DD}. The above-mentioned performance parameters govern the operating behavior of single (isolated) 1T-DRAM (when not incorporated in an array). Furthermore, the bias-dependent disturbance caused by the shared word line (WL) and bit line (BL) remains a major challenge in the array-level operation of 1T-DRAM.

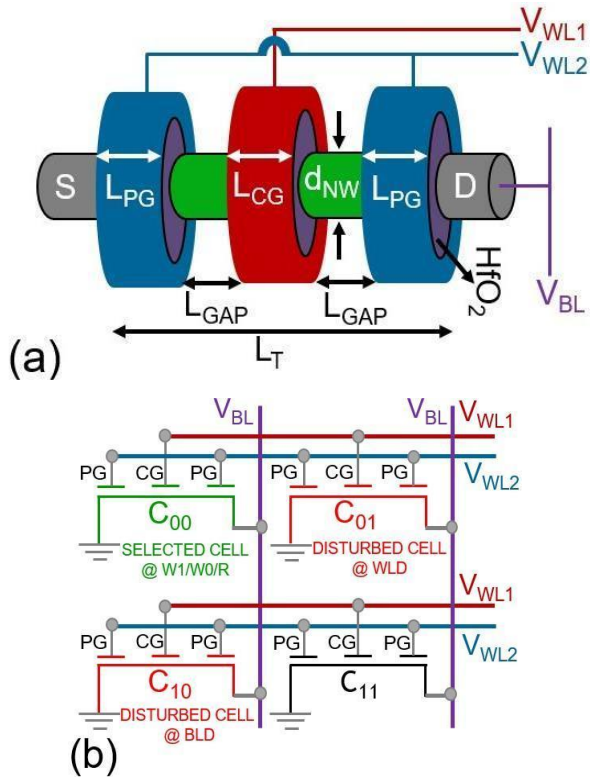

Fig. 4.1 (a) Schematic of an independent gate-all-around RFET used for 1T-DRAM operation. The notation for WL or BL bias is V with the subscript denoting WLs (WL1 and WL2) or BL. V_{WL1} and V_{WL2} are connected to CG and PG, respectively, whereas V_{BL} is connected to the D. (b) A 2 × 2 array consists of NW GAA RFET in each cell, i.e., cell 00, cell 01, cell 10, and cell 11. Each cell in the array consists of two WLs and one BL.

In Chapter 4, the working mechanism of a single cell NW GAA RFET based 1T-DRAM (Fig. 4.1 (a)) is first discussed, followed by an analysis of WL and BL disturbances through the 1T-DRAM array (Fig. 4.1 (b)). The analysis starts by highlighting the influence of the number of bias levels for realizing 1T-DRAM (single cell) with GAA NW RFET. In NW GAA RFET, electrically connected PGs, CG, S, and D constitute four distinct electrodes. Considering the requirements of four operations: W1, W0, H, and R for 1T-DRAM, the number of voltage levels (n_{VL}) should be carefully minimized. RFET (n-type and p-type) has been shown to operate at $\pm V_{DD}$ (± 1 V) for logic applications. Hence, bias schemes for three different values of n_{VL}, i.e., 2 (±1 V), 3 (±1 V, –0.5 V), and 4 (±1 V, ±0.5 V), are considered with a focus on RT, WL, and BL disturbance analysis.

The operation of an independent cell is illustrated for different n_{VL} values, i.e., 2, 3, and 4. In disturbance analysis, RFET 1T-DRAM operating with n_{VL} = 3 and 4 are considered. The n_{VL} = 2 is discarded in the disturbance analysis due to its lower RT than 1T-DRAM independent cell with n_{VL} = 3 as WL and BL disturbances are expected to deteriorate the RT further. A decay (or change) in individual read currents ($I_{BL,1}$ and $I_{BL,0}$) is considered to quantify the disturbance. The disturbance is estimated by calculating the 1/10 and ×10 change in the bit line current corresponding to state 1 ($I_{BL,1}$) and state 0 ($I_{BL,0}$), respectively, from their initial values. WL and BL disturbance centric bias optimization has been performed, and the duration of disturbance tolerance (t_{DT}) has been evaluated, respectively. Additionally, performance metrics were benchmarked with published data on WL and BL array disturbance. Fig. 4.1 (b) shows a 2×2 1T-DRAM array implemented through NW GAA RFET, where each cell, i.e., one NW GAA RFET, consists of two WLs (WL1 and WL2) and one BL. In NW GAA RFET, PGs and CG are connected to WL2 and WL1, respectively, whereas D is connected to BL. Throughout the chapter, no voltage is applied at the source. For the realization of NW GAA RFET based 1T-DRAM as shown in Fig. 4.1 (a), the diameter (d_{NW}), HfO_2 physical high-permittivity (high-κ) T_{OX}, L_{CG}, L_{PG}, and L_T were fixed at 15 nm, 5 nm, 40 nm, 20 nm, and 100 nm, respectively. The considered L_{CG} (40 nm)

and L_{GAP} of 10 nm between PG and CG ensure suppressed SCEs, which aid in higher RT, as shown in Chapter 3.

4.2 1T-DRAM Operation in NW GAA RFET

The presence of a surrounded CG in NW GAA RFET may not support the bias scheme used for an independent DG RFET discussed in previous chapters. The 1T-DRAM operation in NW GAA RFET with bias supporting feasible memory operation is discussed in this chapter. Surrounding CG requires a W1 mechanism other than a positive feedback mechanism induced by weak impact ionization. The inherent architecture of NW GAA RFET supports the same through Schottky tunneling with the application of appropriate bias across PGs and D [208]. The trade-offs associated with n_{VL} and RT in the operation of 1T-DRAM are also discussed in this chapter.

4.2.1 Write 1 and Write 0 Operations

Fig. 4.2 (a) represents the biases applied at WLs (V_{WL1} and V_{WL2}) and BL (V_{BL}) while assessing the performance of NW RFET 1T-DRAM single cell (Fig. 4.1 (a)) with n_{VL} = 3. The only difference between n_{VL} = 2 and 3 is the application of V_{WL1} = 0 (for n_{VL} = 2) versus V_{WL1} = -0.5 V (for n_{VL} = 3) during R operation. The bias applied at the PGs (WL2), CG (WL1), and D (BL) remains the same with either of the $n_{VL,}$ i.e., 2 and 3, during other operations of 1T-DRAM. The W1 operation is performed by the Schottky tunneling mechanism [208]. As shown in Fig. 4.2 (b), W1 operation in independent (single) cell with n_h of ~5×10^{19} cm^{-3} was realized by reducing the tunneling width between valance band (VB) and M (NiSi) with V_{WL2} = 0 V and V_{BL} = 1 V. Since tunneling of holes is relatively faster (as compared to impact ionization), the W1 operation could be performed within t_{W1} = 5 ns. Unless otherwise stated, the S is maintained at 0 V for the sequence of memory operation. Holes are stored in a potential well underneath CG through a V_{WL1} = -1 V. For W0 operation (Fig. 4.2 (c)), V_{WL2} = +1 V is used with V_{BL} = 0 V to enable tunneling of electrons by reducing the tunneling width between conduction band (CB) and M. The electrons recombine with holes present underneath the CG region

due to V_{WL2} = +1 V. After the W0 operation, a lower n_h = ~10^4 cm^{-3} is achieved in 1T-DRAM (single cell).

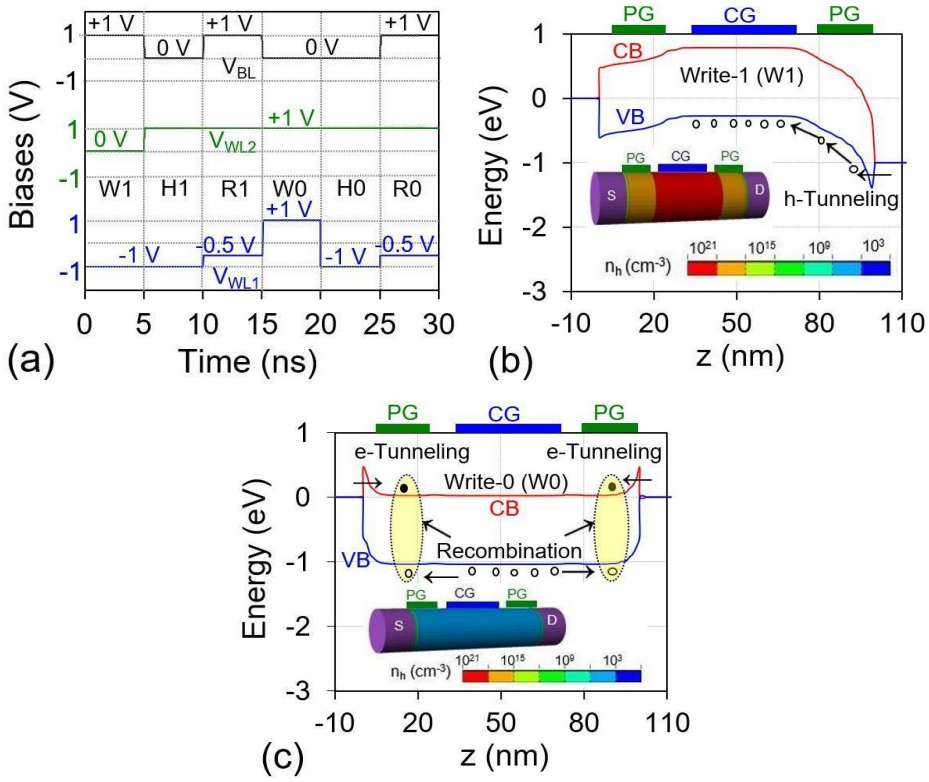

Fig. 4.2 (a) Bit line (BL) and word line (WLs) biases for 1T-DRAM corresponding to bias n_{VL} = 3. V_{WL1} = 0 V during the read (R) operation corresponds to bias scheme for n_{VL} = 2. Contour plot for hole concentration (n_h) and variation of conduction (CB) and valence (VB) band along the channel direction (z) for (b) Write 1 (W1) and (c) Write 0 (W0) operations.

4.2.2 Hold Operation

To sustain holes after W1 and W0 operations, a negative V_{WL1} = -1 V, and a positive V_{WL2} = +1 V are used during the H operation. Fig. 4.3 (a)-(b) shows the variation of n_h with t_{HOLD} during H1 and H0, respectively. The degradation of n_h during H1 is due to recombination, which depends on the depth of the potential well (ΔV), which decreases from the surface (ΔV = 0.7 V) to the center (ΔV = 0.42 V) due to the lesser impact of V_{WL1} on the center of NW. Even though ΔV is lower at the center of NW (indicating the possibility of recombination), its value is sufficient

to maintain the H1 state. During H0, n_h degrades with t_{HOLD} (Fig. 4.3 (b)) because of generation. In contrast, degradation of n_h starts from the surface during H0 state because of a higher electric field at the surface (~ 10^6 V/cm) as compared to that at the center (~ 5×10^5 V/cm) of the ungated region. Thus, at t_{HOLD} ~1.5 s, the difference between n_h during H1 and H0 vanishes as shown in Fig. 4.3 (a) and (b). V_{WL1} = -1 V contributes towards higher RT in NW GAA RFET as the H1 state does not degrade with t_{HOLD}.

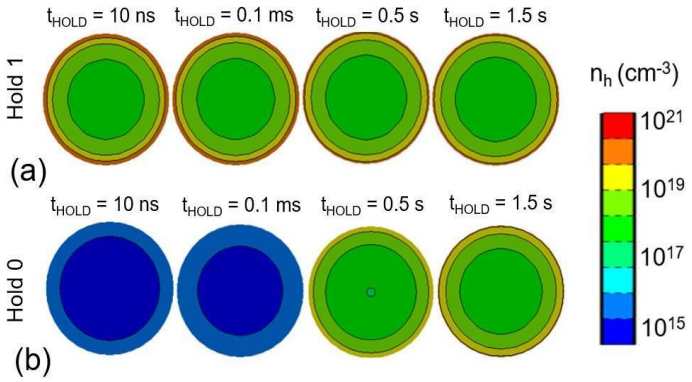

Fig. 4.3 Contour plots showing hole concentration (n_h) with hold time (t_{HOLD}) during (a) Hold 1 (H1), and (b) Hold 0 (H0) operations at mid-CG position.

4.2.3 Read Operation

The difference between n_h after H1 and H0 states can be used to distinguish between R1 and R0 currents through their ratio, i.e., CR = $I_{BL,1}/I_{BL,0}$, where $I_{BL,1}$ and $I_{BL,0}$ are R1 and R0 currents, respectively (Fig. 4.4 (a)). With bias levels shown in Fig. 4.2 (a), the NW GAA RFFET based 1T-DRAM shows a CR of ~3.5×10^3 (Fig. 4.4 (a)), which is sufficient to distinguish between states 1 and 0. Increasing V_{WL1} to 0 (instead of -0.5 V) for R operation indicates feasible 1T-DRAM operation with only 2 voltage levels (± 1 V) with CR of ~10^2. A degradation in n_h during H1 and H0 with t_{HOLD} (Fig. 4.3 (a) and (b)) results in the deterioration of CR with t_{HOLD} (Fig. 4.4 (b)).

In literature [183], [161], [238-239], several methods for estimating RT are available. Among them, the utilization of CR for ascertaining RT is beneficial for quantifying the energy efficiency of 1T-DRAM operating at lower currents. The

value of t_{HOLD} where the ratio of $I_{BL,1}$ and $I_{BL,0}$ reaches 10 is defined as RT i.e. RT = t_{HOLD} at CR = 10 [238]. 1T-DRAM operation with n_{VL} = 3 shows higher RT (~1.35 s) as compared to that exhibited through n_{VL} = 2 (~ 180 ms). An enhanced RT with n_{VL} = 3 is due to V_{WL1} = -0.5 V, which prevents the degradation of $I_{BL,0}$ as compared to 0 V (n_{VL} = 2). Fig. 4.4 (c) shows the variation of RT with V_{WL1} during R operation. A less negative V_{WL1} supports $I_{BL,1}$ while a more negative V_{WL1} supports $I_{BL,0}$, due to their impact on the barrier offered by CG. Thus, for V_{WL1} < -0.5 V, a sharp reduction in RT is observed due to the deterioration of $I_{BL,1}$ i.e., enhanced barrier for electrons. For V_{WL1} > -0.4 V, RT primarily deteriorates due to the degradation of $I_{BL,0}$, i.e., a reduced barrier for electrons. Thus, RT and CR can be enhanced by optimizing V_{WL1}. NW GAA RFET 1T-DRAM exhibits the potential to operate with n_{VL} = 2 along with modest CR and RT (Fig. 4.4 (c)).

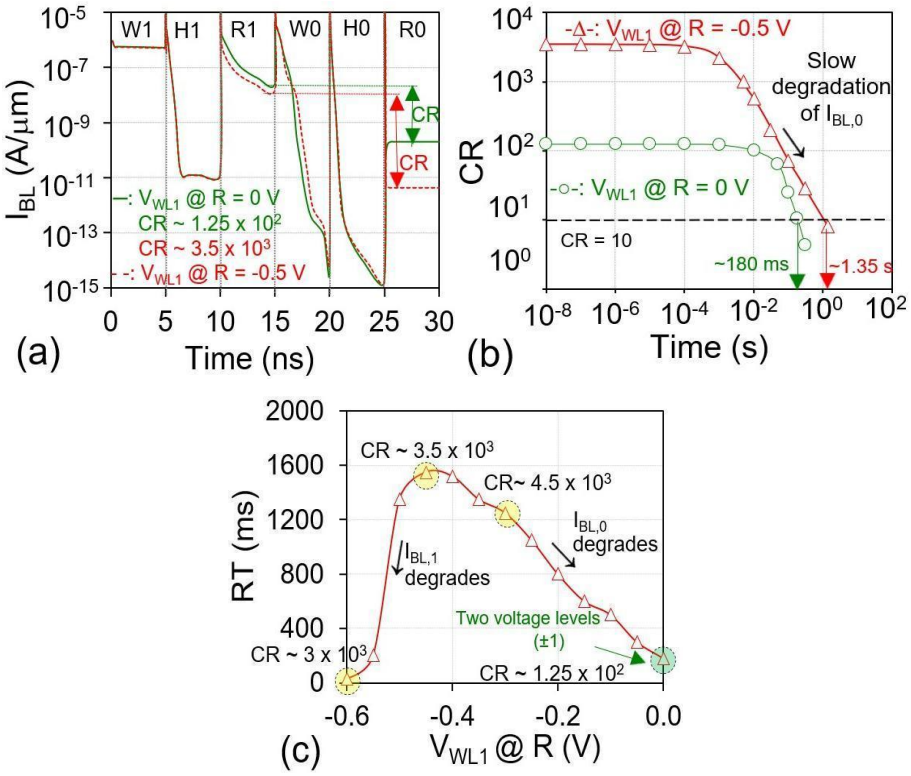

Fig. 4.4 (a) Current transient for different CG read biases V_{WL1} (= 0 V with n_{VL} = 2 and -0.5 V with n_{VL} = 3). (b) Variation of current ratio (CR) with t_{HOLD} for V_{WL1} = 0 V and -0.5 V. (c) Retention time (RT) as a function of V_{WL1} (n_{VL} = 3).

4.2.4 1T-DRAM Operation with Four Voltage Levels

In this section, the impact of an additional voltage level (total of 4 levels) on the CR and WL/BL disturbance analysis is analyzed. The V_{BL} of 1 V (n_{VL} = 3) used during W1 and R operation is reduced to 0.5 V (n_{VL} = 4) as shown in Fig. 4.5 (a). The change in V_{BL} (during R operation) from 1 V to 0.5 V increases n_{VL} from 3 to 4, but CR is also improved by two decades, as shown in Fig. 4.5 (b). V_{WL1} (-0.5 V) and V_{WL2} (1 V) remain same for R operation as used in n_{VL} = 3. Lowering V_{BL} from 1 V to 0.5 V while maintaining V_{WL2} = 0 V results in insufficient tunneling of holes from the D side, which is detrimental for W1 operation. To compensate for this, a negative voltage level (V_{WL2}) of -0.5 V is applied during W1 operation to initiate the 1T-DRAM operation. The voltage levels used for 1T-DRAM operation, with n_{VL} = 4, are shown in Fig. 4.5 (a). There is no change in bias for the W0 operation. A lower V_{BL} = 0.5 V (along with V_{WL2} = 1 V, V_{WL1} = -0.5 V) in a single cell during R operation contributes towards higher CR of ~ 7.3×10^5 (as opposed to ~ 3.7×10^3 with n_{VL} = 3) due to relatively lower $I_{BL,0}$ (Fig. 4.5 (b)). A minor change is observed in $I_{BL,1}$. However, the minor change in $I_{BL,1}$ does not contribute towards a significant change in CR.

W1, W0, H, and R operations, along with their corresponding biases have been performed for 5 ns. The dependence of CR and RT on V_{WL1} for R operation is shown in Fig. 4.5 (c). V_{WL2} and V_{BL} are fixed at 1 V and 0.5 V, respectively. The CR first increases from V_{WL1} = 0 V to -0.5 V due to a decrease in $I_{BL,0}$. For more negative V_{LW1} than -0.5 V, the CR starts to degrade due to the reduction in $I_{BL,1}$. As a result, the CR for V_{WL1} = -0.6 V is reduced to ~10^5. The maximum CR of ~ 7×10^5 has been demonstrated by NW RFET-based 1T-DRAM at V_{WL1} = -0.5 V. The improved RT for V_{WL1} > -0.5 V for n_{VL} = 4 (compared to n_{VL} = 3) is due to the suppressed degradation of $I_{BL,0}$ with t_{HOLD} (due to V_{BL} = 0.5 V). Degradation in $I_{BL,1}$ with t_{HOLD} at V_{WL1} = -0.6 V is severe and as a result, RT is sharply reduced to ~ 400 ms compared to ~1800 ms with V_{WL1} = -0.5 V. Higher n_{VL} of 4 can exhibit an improved RT (~1800 ms as compared to 1350 ms for n_{VL} = 3) for V_{WL1} = -0.5 V (V_{WL2} = 1 V, V_{BL} = 0.5 V) due to an improved CR. The enhanced number of voltage

levels used at V_{WL1}, V_{LW2}, and V_{BL} during each operation (W1, W0, H, and R) can yield improved 1T-DRAM metrics. The impact of the number of voltage levels (n_{VL}) is further extended to WL and BL disturbance in NW RFET based 1T-DRAM array, and this is discussed in the next section.

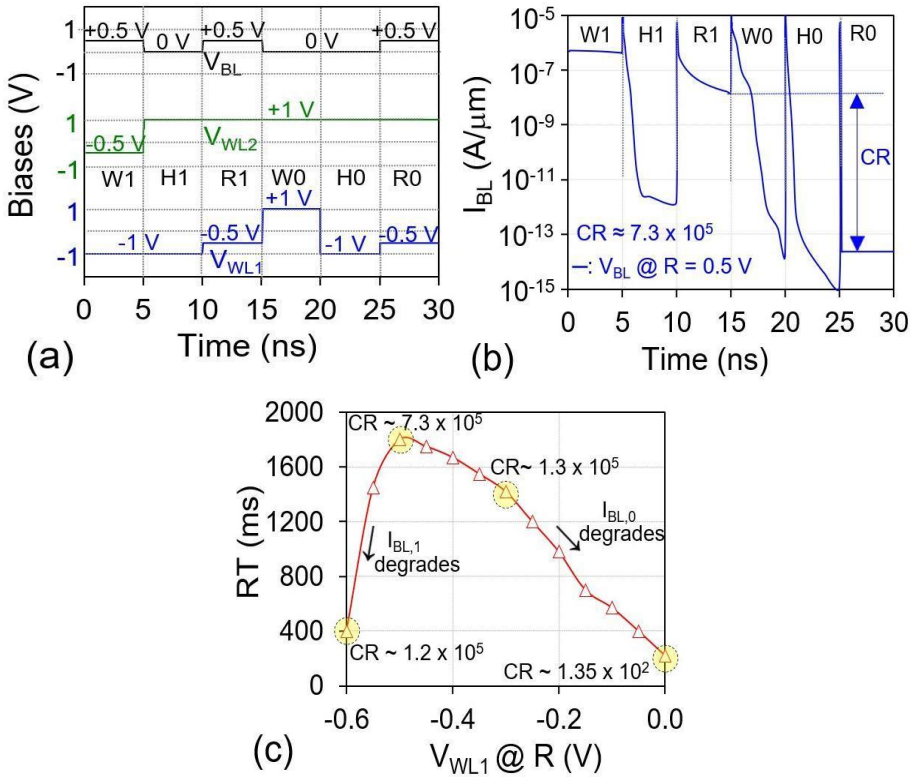

Fig. 4.5 (a) Bit line (BL) and word line (WL) biases for 1T-DRAM corresponding to bias $n_{VL} = 4$. (b) Current transient showing 1T-DRAM operations for $n_{VL} = 4$. (c) Retention time (RT) as a function of V_{WL1} ($n_{VL} = 4$).

4.3 Disturbance Analysis in RFET based 1T-DRAM Array

1T-DRAM cell array consists of many independent devices and is operated with a shared WL and BL as shown in Fig. 4.1 (b). The disturbance due to shared WLs (WL1 and WL2) or BL remains a crucial issue in array implementation [240]. In the 1T-DRAM array shown in Fig. 4.1 (b), cell 01 and cell 10 are connected with cell 00 through the same WLs and BL, respectively. Hence, the states of cell 01 and cell 10 are likely to be affected when W1, W0, and R operations are performed on cell 00. The impact of disturbance can be severe because same memory locations

may be accessed repetitively. Hence, the disturbance analysis is essential for a more pragmatic understanding of 1T-DRAM. The disturbance analysis with a prime focus on extending immunity from disturbance via n_{VL} = 3 and 4 is elaborated below.

The impact of disturbance on non-selected cells i.e., cell 10 (due to shared BL) and cell 01 (due to shared WLs) shown in Fig. 4.1 (b), is investigated up to 10^8 cycles for different memory operations (W1, W0, and R) on cell 00. In some cases, disturbance analysis has been carried out for less than 10^8 cycles if the cells are disturbed earlier. The number of cycles is defined as the number of W1/W0/R operations performed on cell 00, which is calculated by dividing the t_{HOLD} by W1 time (t_{W1} = 5 ns), W0 time (t_{W0} = 5 ns), and R time (t_R = 5 ns). The H1 state of cell 10 and cell 01 is considered free from disturbance until their corresponding $I_{BL,1}$ degrades by 1/10 of maximum current ($I_{BL,1}$ current during independent cell operation) whereas H0 of cell 10 and cell 01 is considered free until the corresponding $I_{BL,0}$ increases by a factor of 10 with respect to the minimum current level ($I_{BL,0}$ current during independent/single cell operation). WL and BL disturbance is an open problem that requires a methodology to estimate the duration for disturbance tolerance (t_{DT}) of cell 01 and cell 10 in response to any operation on cell 00.

4.3.1 Disturbance Analysis with Three Voltage Levels

In section 4.2, the analysis with the number of voltage levels was restricted to the performance improvement of only independent 1T-DRAM. In this section, the impact of the number of voltage levels on the performance improvement of the 1T-DRAM array has been investigated. The set of bias values used for independent 1T-DRAM with 3 (Fig. 4.2 (a)) and 4 (Fig. 4.5 (a)) voltage levels has been further extended for WL and BL disturbance analysis. Ideally, WLs (V_{WL1} = -1 V, V_{WL2} = 1 V) and BL (V_{BL} = 0 V) voltages are applied at cell 10 and cell 01 using the bias during the hold state for single 1T-DRAM cell as it provides optimal RT. The bias required across the BL (V_{BL}) and WLs (V_{WL1}, V_{WL2}) of cell 00 to perform W1, W0, and R is mentioned in Table 4.1 and 4.2, respectively. Due to the common WLs

between cell 00 and cell 01, the voltages applied to WLs of cell 00 (V_{WL1}, V_{WL2}) impact cell 01 as shown in Fig. 4.1 (b). Similarly, due to the common BL between cell 00 and cell 10, the voltage applied to the BL of cell 00 (V_{BL}) affects cell 10 as shown in Fig. 4.1 (b). Since the WL voltage (V_{WL1}, V_{WL2}) of cell 10 is not shared with cell 00, the WL voltage of cell 10 is not affected by W1, W0, and R operations on cell 00. Similarly, the BL voltage (V_{BL}) of cell 01 is not shared with cell 00. Therefore, cell 01 remains unaffected by W1, W0, and R operations on cell 00. To showcase the WL and BL disturbance first, its impact on hole density during H1 and H0 operation is shown. This is further followed by its impact on $I_{BL,1}$ and $I_{BL,0}$ during the R operation.

Table 4.1: BL bias for cells 10 and 00 in H state and W1/W0/R, respectively (n_{VL} = 3).

Operations	**V_{BL}**
Hold (H1 and H0) in cell 10	0 (V)
Write 1 (W1) in cell 00	1 (V)
Write 0 (W0) in cell 00	0 (V)
Read (R) in cell 00	1 (V)

Table 4.2: WL bias for cells 01 and 00 in H state and W1/W0/R, respectively (n_{VL} = 3).

Operations	**V_{WL2}**	**V_{WL1}**
Hold (H1 and H0) in cell 01	1 (V)	-1 (V)
Write 1 (W1) in cell 00	0 (V)	-1 (V)
Write 0 (W0) in cell 00	1 (V)	1 (V)
Read (R) in cell 00	1 (V)	-0.5 (V)

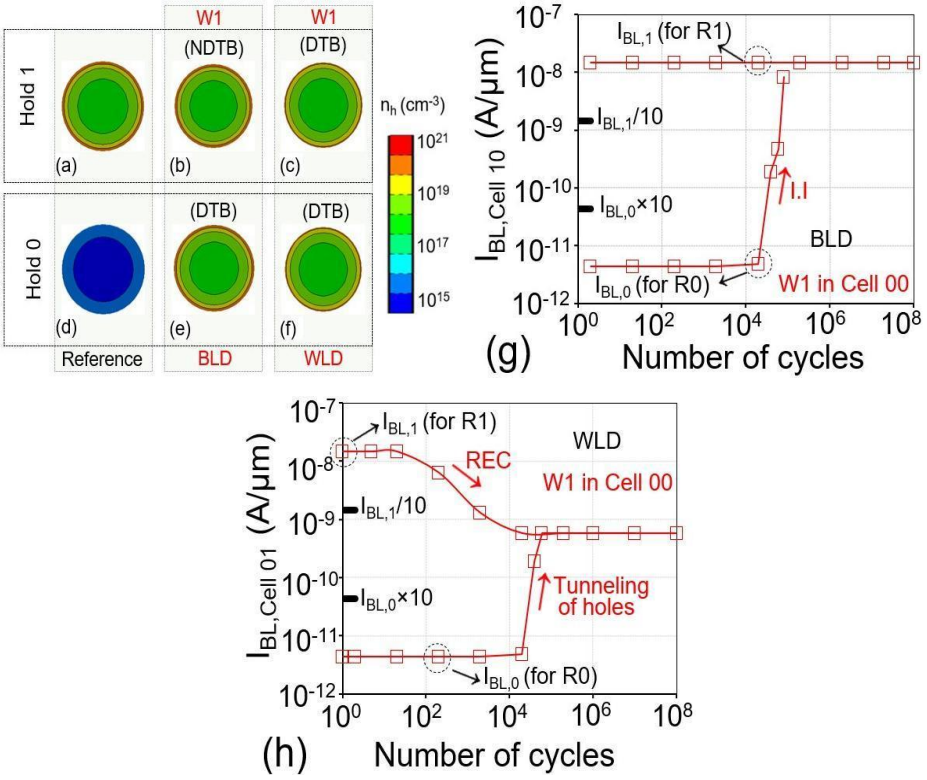

Fig. 4.6 Contour plots, extracted at mid-CG position after 10^4 cycles, showing hole concentration n_h after H1 state for (a) reference cell (independent cell), (b) cell 10 after W1, (c) cell 01 after W1. Hole concentration n_h after H0 state for (d) reference cell (independent cell), (e) cell 10 after W1, (f) cell 01 after W1. (g) Impact of BL disturbance on $I_{BL,1}$ and $I_{BL,0}$ of cell 10 due to W1 (n_{VL} = 3). (h) Impact of WL disturbance on $I_{BL,1}$ and $I_{BL,0}$ of cell 01 due to W1 (n_{VL} = 3). DTB and NDTB denote disturbed or not disturbed.

4.3.1.1 WL/BL Disturbance due to Write 1 Operation

Different operations, i.e., W1/W0/R on cell 00, have a distinct impact on cells 10 and 01 due to BL and WL disturbances, respectively. Hence, the analysis has been carried out for each W1/W0/R. For W1 operation in cell 00, the V_{LW1} (voltage at CG), V_{WL2} (voltage at PG), and V_{BL} (voltage at D) is set to -1 V, 0 V, and 1 V, respectively, to enable tunneling of holes through D side, and subsequently accumulate underneath the CG. This bias is different from BL and WLs (WL1 and WL2) bias used for H1 and H0 operation, as shown in Table 4.1 and 4.2, respectively. As a result, the BL bias (V_{BL}) of cell 10 is modified to 1 V, and the

WL2 bias (V_{WL2}) of cell 01 is changed to 0 V due to disturbance, as shown in Table 4.1 and 4.2. There is no change in WL1 bias (V_{WL1}) because the same bias is used for H and W1 operations (Table 4.2).

A V_{BL} of 1 V, along with V_{WL1} = -1 V and V_{WL2} = 1 V in cell 10 results in a positive feedback mechanism by weak impact ionization during H1 and H0. Consequently, the hole generation takes place during H1 and H0 operations in cell 10. The n_h in cell 10 due to BL disturbance after 10^4 cycles of W1 in cell 00 is shown in Fig. 4.6 (b) and (e). The BL disturbance due to W1 in cell 00 disturbs the H0 state of cell 10, whereas the H1 is unaffected. A significant change in n_h of the H0 state of cell 10 as compared to n_h of the H0 state of the reference cell can be observed in Fig. 4.6 (e) and (d). The $I_{BL,0}$ of cell 10 starts to degrade after ~10^4 cycles while $I_{BL,1}$ retains its value for >10^4 cycles (Fig. 4.6 (g)) due to BL disturbance in cell 10.

During the W1 operation, V_{WL1} of cell 00 remains the same as that of the H operation (-1) of cell 01 (Table 4.2). However, a different V_{WL2} of cell 00 (0 V) as compared to H bias of cell 01 (1 V) results in (i) tunneling of holes in cell 01 during H0, and (ii) a reduced potential well depth in cell 01 during H1. The reduced potential well depth results in a marginal reduction in the n_h of the H1 state (Fig. 4.6 (c)), whereas the H0 state is severely degraded (Fig. 4.6 (f)). Hence, $I_{BL,1}$ degrades before 10^4 cycles (Fig. 4.6 (h)). The H0 state of cell 01 exhibits marginal degradation up to 10^4 cycles due to slow generation processes. However, the state is disturbed immediately after 10^4 cycles (before 10^6 cycles), as shown in Fig. 4.6 (f), due to the tunneling of holes (Fig. 4.6 (h)). The disturbance is quantified based on a stringent criterion, where a 1/10 reduction in $I_{BL,1}$ and a ×10 increase in $I_{BL,0}$ of cell 10 and cell 01 is considered for disturbance analysis.

4.3.1.2 WL/BL Disturbance due to Write 0 Operation

For W0 operation in cell 00, V_{WL1} (voltage at CG), V_{WL2} (voltage at PG), and V_{BL} (voltage at D) are 1 V, 1 V, and 0 V, respectively, to deplete holes from underneath the CG. However, the bias applied differs from that of the BL and WLs

(WL1 and WL2) used for H1 and H0 operations, as shown in Table 4.1 and 4.2. respectively. As a result, WL1 bias (V_{WL1}) of cell 01 is changed to 1 V as shown in Table 4.2. There is no change in V_{BL} (Table 4.1), and V_{WL2} (Table 4.2) is due to the same bias used for W0 and H, as shown in Table 4.1 and 4.2. The hole generation takes place during H0, and hole recombination occurs during H1 operations in cell 10, which is emphasized by the number of cycles of W0 on cell 00.

After 10^4 cycles of W0 on cell 00, there is no change in n_h of the H1 state of cell 10 is observed compared to H1 state of reference (Fig. 4.7 (a) and (b)). Similarly, the n_h in the H0 state of cell 10 is also not significantly increased after 10^4 cycles on cell 00. This can also be observed in Fig. 4.7 (d) and (e). The suppressed recombination and generation in the H1 and H0 states, respectively, of cell 10 is due to the application of the same bias across the V_{WL1} (-1 V), V_{WL2} (1 V), and V_{BL} (0 V) as in H operation. Consequently, $I_{BL,1}$ and $I_{BL,0}$ of cell 10 do not show any degradation till 10^4 cycles of W0 in cell 00, as shown in Fig. 4.7 (g). Cell 10 remains non-disturbed until 10^4 cycles (and possibly even higher numbers of cycles) due to BL bias. V_{WL2} of cell 00 remains the same as that of the H operation (1 V) of cell 01 (Table 4.2), and hence, V_{WL2} does not contribute to the WL disturbance. However, a different V_{WL1} of cell 00 (1 V) as compared to the H bias of cell 01 (-1 V) results in enhanced recombination in H1 and H0 states of cell 01. The reduced potential well depth underneath the CG results in a significant reduction in the n_h of the H1 state of cell 01 as compared to the reference (Fig. 4.7 (a) and (c)). The H1 state of cell 01 is disturbed before 10^4 cycles due to WL disturbance whereas the H0 state of cell 01 does not encounter any change as compared to the reference (Fig. 4.7 (d) and (f)). The H0 state of cell 01 remains non-disturbed due to WL disturbance. As a result, the $I_{BL,1}$ of cell 01, is degraded (severely) before 10^4 cycles due to WL disturbance as shown in Fig. 4.7 (h). Unlike $I_{BL,1}$, $I_{BL,0}$ of cell 01 is not degraded before 10^4 cycles due to WL disturbance as shown in Fig. 4.7 (h). The number of cycles has been calculated by dividing the t_{HOLD} by W1, W0, and R time.

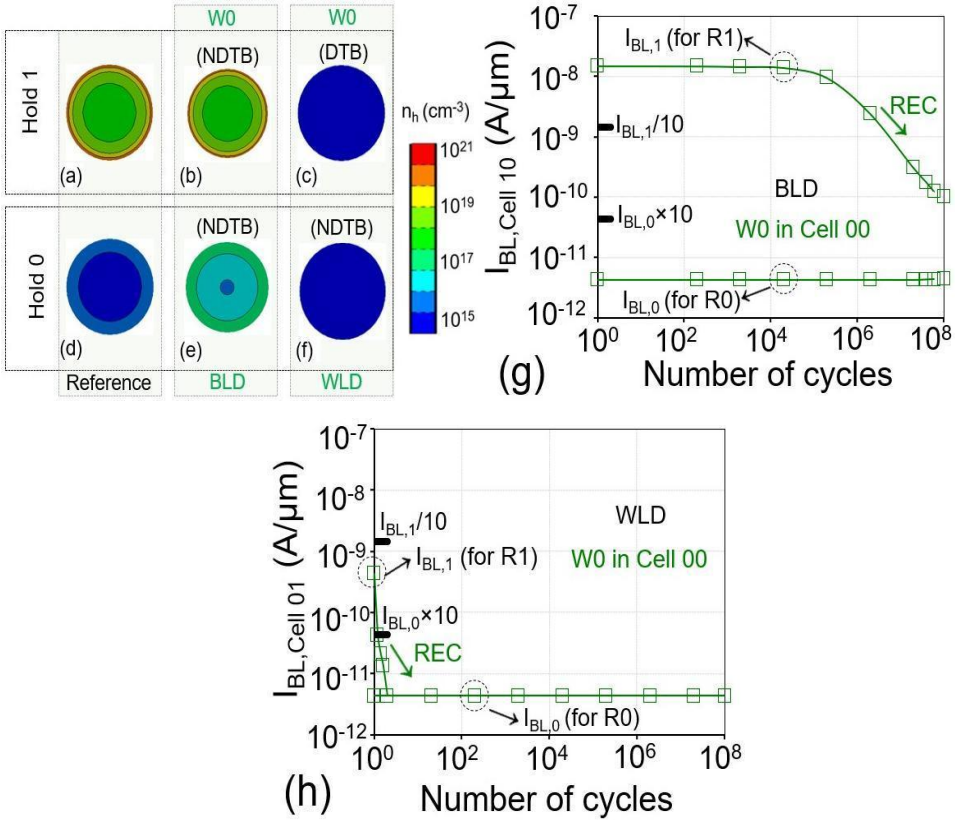

Fig. 4.7 Contour plots, extracted at mid-CG position after 10^4 cycles, showing hole concentration n_h after H1 state for (a) reference cell (single cell), (b) cell 10 after W0, (c) cell 01 after W0. Hole concentration n_h after H0 state for (d) reference cell (single cell), (e) cell 10 after W0, (f) cell 01 after W0. (g) Impact of BL disturbance on $I_{BL,1}$ and $I_{BL,0}$ of cell 10 due to W0 (n_{VL} = 3). (h) Impact of WL disturbance on $I_{BL,1}$ and $I_{BL,0}$ of cell 01 due to W0 (n_{VL} = 3). DTB and NDTB denote disturbed or not disturbed.

4.3.1.3 WL/BL Disturbance due to Read Operation

For R operation in cell 00, V_{LW1} (voltage at CG), V_{WL2} (voltage at PG), and V_{BL} (voltage at D) are -0.5 V, 1 V, and 1 V, respectively. However, the bias applied differs from that of BL and WLs (WL1 and WL2) used for H1 and H0 operations, as shown in Table 4.1 and 4.2, respectively. As a result, the BL bias (V_{BL}) of cell 10 is modified to 1 V, and the WL1 bias (V_{WL1}) of cell 01 is modified to -0.5 V, as shown in Table 4.1 and 4.2. There is no change in WL2 bias (V_{WL2}) because the same bias is used for H and R operations (Table 4.2). The V_{BL} of 1 V, along with

V_{WL1} = -1 V and V_{WL2} = 1 V in cell 10, results in a positive feedback mechanism during H1 and H0. Consequently, hole generation occurs during H1 and H0 operations in cell 10, as indicated by the number of cycles. The n_h in cell 10 due to BL disturbance after 10^4 cycles of R in cell 00 is shown in Fig. 4.8 (b) and (e). The BL disturbance due to R operation in cell 00 disturbs the H0 state of cell 10, whereas the H1 is unaffected. Significant change in n_h of the H0 state of cell 10 as compared to n_h of the H0 state of the reference cell can be observed in Fig. 4.8 (e) and (d). The $I_{BL,0}$ of cell 10 starts to degrade after ~10^4 cycles while $I_{BL,1}$ retains its value for >10^4 cycles (Fig. 4.8 (g)) due to BL disturbance in cell 10. A different V_{WL1} of cell 00 (-0.5 V) as compared to the H bias of cell 01 (-1 V) results in enhanced recombination in the H1 and H0 states of cell 01. The reduced potential well depth underneath the CG results in a reduction in n_h of the H1 state of cell 01, as compared to the n_h of the reference cell (Fig. 4.8 (a) and (c)). The H1 state of cell 01 is disturbed before 10^4 cycles due to WL disturbance whereas the H0 state of cell 01 does not encounter any change as compared to the reference (Fig. 4.8 (d) and (f)). The H0 state of cell 01 remains non-disturbed due to WL disturbance. As a result, the $I_{BL,1}$ of cell 01, is degraded (severely) before 10^4 cycles due to WL disturbance as shown in Fig. 4.7 (h).

Amongst all (12) possible cases of WL and BL disturbances [240] with n_{VL} = 3, the NW GAA RFET based 1T-DRAM shows immunity toward all 6 possible cases of BL disturbance for up to ~10^4 cycles, whereas 3 cases can preserve their original states after 10^4 cycles due to WL disturbance. Amongst these 9 cases (including BL and WL disturbance), only 6 cases (4 BL and 2 WL cases) correspond to the cell being immune for >10^4 disturbance cycles. Enhancing the number of immunity cases and extending the number of cycles for disturbance-free operation requires the addition of an extra voltage level (n_{VL} = 4), which can enhance tolerance towards BL (cell 10) and WL (cell 01) disturbances (discussed in the next section). In the next section, the impact of adding an extra voltage level (0.5 V for W1 and R operation) on the disturbance immunity of cells 10 and 01 has been discussed in detail.

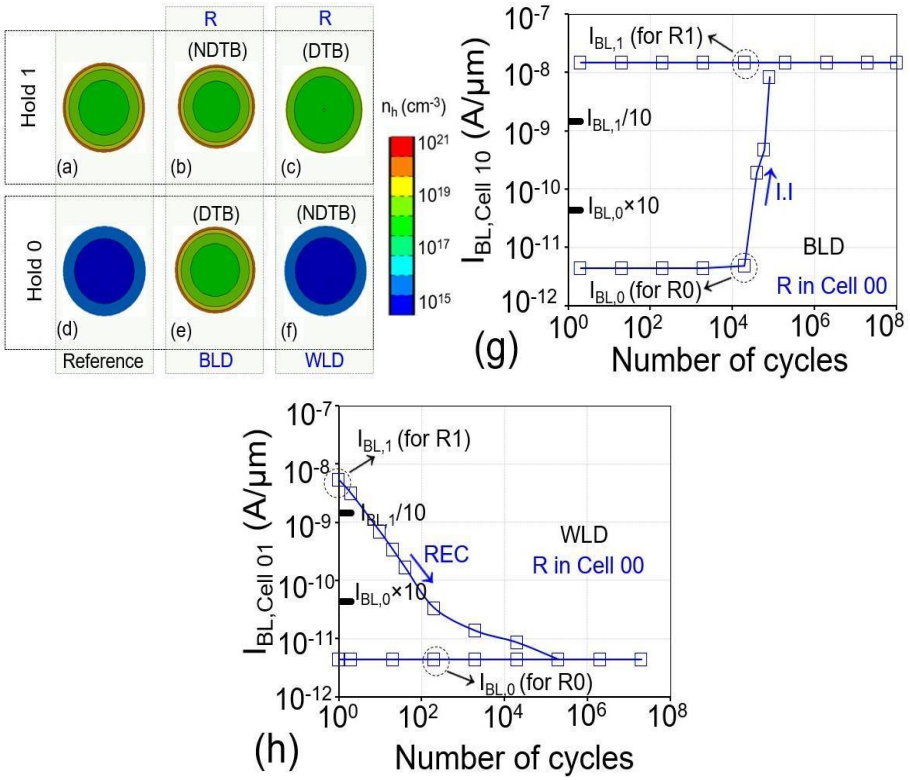

Fig. 4.8 Contour plots, extracted at mid-CG position after 10^4 cycles, showing hole concentration n_h after H1 state for (a) reference cell (independent cell), (b) cell 10 after R, (c) cell 01 after R. Hole concentration n_h after H0 state for (d) reference cell (independent cell), (e) cell 10 after R, (f) cell 01 after R. (g) Impact of BL disturbance on $I_{BL,1}$ and $I_{BL,0}$ of cell 10 due to R (n_{VL} = 3). (h) Impact of WL disturbance on $I_{BL,1}$ and $I_{BL,0}$ of cell 01 due to R (n_{VL} = 3). DTB and NDTB denote disturbed or not disturbed.

4.3.2 Disturbance Analysis with Four Voltage Levels

In the disturbance analysis with n_{VL} = 3 described above, a relatively lower immunity (< 10^6 cycles) towards BL disturbance in cell 10 (H0 state) due to W1 and R operations on cell 00 is the result of a high V_{BL} of 1 V (Table 4.1) due to weak impact ionization in cell 10 during H0 state. Hence, a relatively lower V_{BL} of 0.5 V (Table 4.3) during W1 and R operations can be a possible solution to improve tolerance from disturbance through n_{VL} = 4. However, a smaller positive V_{BL} (0.5 V) along with other biases, as shown in n_{VL} = 3 (V_{WL2} = 0 V), results in insufficient hole tunneling from the D side, which degrades W1 operation. To compensate for

the same, a negative V_{WL2} (-0.5 V) is also used during W1 operation. The V_{BL} = 0.5 V during W1 and R on cell 00 adds to extra voltage levels, which leads to n_{VL} = 4. The impact of W1, W0, and R operations on cell 00 with n_{VL} = 4, as well as on cells 10 and 01, is discussed below.

Table 4.3: BL bias for cells 10 and cell 00 in H state and W1/W0/R, respectively (n_{VL} = 4).

Operations	V_{BL}
Hold (H1 and H0) in cell 10	0 (V)
Write 1 (W1) in cell 00	0.5 (V)
Write 0 (W0) in cell 00	0 (V)
Read (R) in cell 00	0.5 (V)

Table 4.4: WL bias for cell 01 and cell 00 in H state and W1/W0/R, respectively (n_{VL} = 4).

Operations	V_{WL2}	V_{WL1}
Hold (H1 and H0) in cell 01	1 (V)	-1 (V)
Write 1 (W1) in cell 00	-0.5 (V)	-1 (V)
Write 0 (W0) in cell 00	1 (V)	1 (V)
Read (R) in cell 00	1 (V)	-0.5 (V)

A V_{BL} of 0.5 V (during W1 and R operations in cell 00) results in a slower generation of holes in H0 state of cell 10 (Fig. 4.9 (i) and (j)) due to the reduced impact ionization, and therefore, $I_{BL,0}$ retains its original state for a higher number of cycles (> 10^6) as compared to n_{VL} = 3 (< 10^6) and the same is shown in Fig. 4.9 (o). A marginal degradation in $I_{BL,1}$ in cell 10 (Fig. 4.9 (o)) is the result of the reduced rate of impact ionization during H1 operation. The V_{BL} of 0 V during W0 operation in cell 00 does not affect the H state of cell 10, i.e., $I_{BL,1}$ and $I_{BL,0}$ of cell 10 remain non-disturbed for cycles greater than 10^6 (Fig. 4.9 (o)).

The reduction in V_{BL} from 1 V to 0.5 V, while performing W1 and R operations on cell 00, remains instrumental in improving immunity (>10^6 cycles) towards BL disturbance in cell 10 for all 6 cases. In the process of enhancing the immunity towards BL disturbance in cell 10 shown above, the tolerance of cell 01 due to WL disturbance is affected because of V_{WL2} of -0.5 V in cell 00 during W1 operation. When W1 operation is performed on cell 00, a negative V_{WL2} (-0.5 V) enables tunneling of holes from metal to semiconductor which improves the tolerance of H1 state (Fig. 4.9 (e)) of cell 01 (> 10^6 cycles) whereas H0 state of cell 01 is still degraded before 10^6 cycles and the same is shown through the variation in $I_{BL,1}$ and $I_{BL,0}$ in Fig. 4.9 (p).

The WL disturbance in cell 01 (H1 and H0) due to R and W0 operations exhibit the same behavior as in n_{VL} = 3, resulting from the same biases. With extra voltage levels (n_{VL} = 4), the total number of cases that can exhibit enhanced tolerance (> 10^6 cycles) towards BL and WL in cell 10 and cell 01, respectively, is improved to 9 (from 6 with n_{VL} = 3). With either of the n_{VL}s, i.e., 3 and 4, R and W0 operations on cell 00 disturb the H1 state of cell 01, whereas the W1 operation on cell 00 disturbs the H0 state of cell 01 before 10^6 cycles. The method used to quantify disturbance is very stringent because the $I_{BL,1}$ and $I_{BL,0}$ of corresponding disturbed cells (cell 10 and cell 01) encounter changes of 1/10 and ×10, respectively, to their initial values. The $I_{BL,1}$ of cell 01, is degraded before 10 cycles of R and W0 operation on cell 00 (Fig. 4.9 (p)). In either of the cases, no change in $I_{BL,0}$ is observed. Similarly, $I_{BL,0}$ of cell 01 is degraded before 100 cycles after W1 operation on cell 00 as shown in Fig. 4.9 (p), and no change in $I_{BL,1}$ is observed. The method used for analysis so far only shows the severity of WL and BL disturbance on cells 01 and 10, respectively. The approach does not provide insights into the optimal bias values for each W1, W0, and R operation. For the pragmatic realization of 1T-DRAM with RFET, array centric bias optimization of different operations (W1, W0, and R) on cell 00 that can affect cells 01 and 10 is essential.

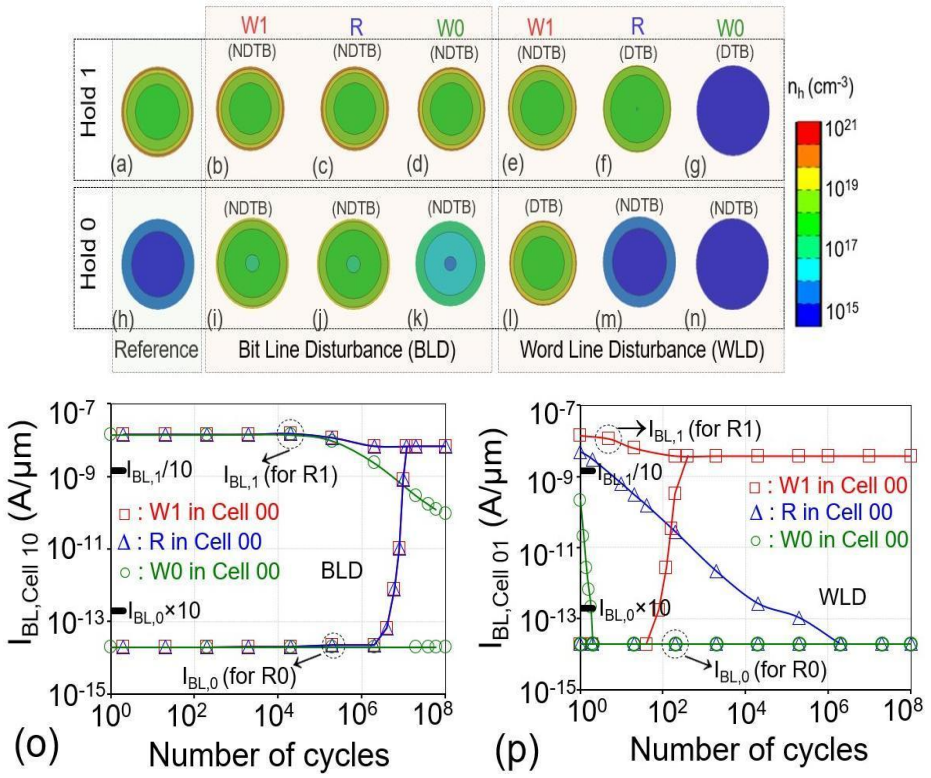

Fig. 4.9 Contour plots, extracted at mid-CG position after 10^6 cycles, showing n_h for (a) reference cell (independent cell) H1 state and impact of BL disturbance for (b) W1, (c) R, and (d) W0 operations, and WL disturbance for (e) W1, (f) R, and (g) W0 operations for H1 state. Contour plots showing n_h for (h) reference cell H0 state and impact of BL disturbance for (i) W1, (j) R, and (k) W0 operations, and WL disturbance for (l) W1, (m) R, and (n) W0 operations for H0 state. (o) Impact of BL disturbance on $I_{BL,1}$ and $I_{BL,0}$ of cell 10 due to W1, W0, and R operations (n_{VL} = 4). (p) Impact of WL disturbance on $I_{BL,1}$ and $I_{BL,0}$ of cell 01 due to W1, W0, and R operations (n_{VL} = 4). DTB and NDTB denote disturbed or not disturbed.

4.4 Duration of Disturbance Tolerance in RFET based 1T-DRAM Array

W1/W0/R operation is crucial for the appropriate functioning of 1T-DRAM. However, the bias used for W1/W0/R does not consider its impact on WL/BL disturbance. The set of bias values used for W1/W0/R operation in an independent cell may not be optimal for the array. Hence, a separate bias optimization strategy is required for the array. A key metric of a 1T-DRAM array

is the duration of disturbance tolerance (t_{DT}), which should be maximized through appropriate bias selection. The t_{DT} is defined as the t_{HOLD} after which CR becomes equal to 10 when any cell (cell 01 or cell 10) is experiencing WL/BL disturbance. The choice of biases is usually based on optimizing individual operations (W1, W0, and R) in the independent cell and may not include t_{DT}. As shown in Fig. 4.9 (p), the WL disturbance causes a rapid degradation (10 ns) of $I_{BL,1}$, which significantly affects the retention time.

Since the impact of WL disturbance is significant, a different device dimension ($L_{PG} = L_{GAP} = L_{CG}$ = 20 nm (L_T = 100 nm)) has been adopted than that considered previously. The impact of WL disturbance on $I_{BL,1}$ can be further suppressed by using a relatively longer L_{GAP} of 20 nm (compared to 10 nm in the previous case). To assess the t_{DT} of RFET based 1T-DRAM array, the biases for the hold state have been fixed, and the impact of each operation is evaluated through t_{DT} at 85 °C. The duration of W1 and W0 operations ($t_{W1} = t_{W0}$) is 10 ns, while that for R operation (t_R) is 5 ns. Unless affected by WL disturbance or BL disturbance, cells 01 and 10 remain in hold (H) state with WL biases of $V_{WL1,H}$ = -1 V and $V_{WL2,H}$ = 1 V, and BL bias ($V_{BL,H}$) of 0 V. If the bias at an electrode (WL1, WL2, and BL) is equal to bias for hold state, then electrode does not contribute to disturbance. Since $V_{WL1,W1} = V_{WL1,H}$, the WL1 does not contribute to WLD. Similarly, WL2 will not contribute to WLD during W0 and R operations ($V_{WL2,W0} = V_{WL2,R} = V_{WL2,H}$).

4.4.1 Optimizing Write 1 to Maximize Duration of Disturbance Tolerance

The cell 00 has been realized with $V_{WL1,W1}$ being equal to H bias ($V_{WL1,H}$) i.e. $V_{WL1,W1} = V_{WL1,H}$ = -1 V. As W1 impacts cell 01 (due to WLD) and cell 10 (due to BLD), the biases (WL2 and BL) which maximize t_{DT} are desirable for $V_{WL2,W1} \leq 0$ V (tunneling of holes) and $V_{BL,W1} \geq 0$ V. A more negative $V_{WL2,W1}$ reduces the tunneling width. It supports hole tunneling from M-S junction during H0, leading to a faster degradation of BL current ($I_{BL,0}$) in cell 01 (Fig. 4.10 (a)). A lower recombination in H1 results in a minor degradation in BL current ($I_{BL,1}$) in cell 01.

The degradation in BL current increases due to a bias change from $V_{WL2,W1}$ = 0 V to $V_{WL2,W1}$ = -0.2 V due to a reduction in potential depth. As shown in Fig. 4.10 (b), the degradation in CR is limited in $V_{WL2,W1}$ = 0 V, which results in a t_{DT} of 120 μs as compared to 23 μs at $V_{WL2,W1}$ = -0.2 V. Since the rate of degradation in $I_{BL,0}$ is higher than $I_{BL,1}$, $I_{BL,0}$ primarily governs the variation in CR. The upper limit on $V_{WL2,W1}$ (= 0 V) is imposed by electron tunneling that restricts the W1 operation in cell 00. The range of biases ($V_{WL2,W1}$ and $V_{BL,W1}$) which result in feasible W1 at $V_{WL1,W1}$ = -1 V have been considered to showcase the impact of W1 operation (cell 00) on cell 01 and cell 10. $V_{BL,W1}$ varying from 1 V to 1.2 V results in BLD in cell 10 (Fig. 4.10 (c)). However, weak impact ionization (rate ~10^{18} $cm^{-3}s^{-1}$) does not cause a significant change in $I_{BL,0}$ for t_{HOLD} < 10 μs. Impact ionization depends on t_{HOLD}, and becomes effective (rate ~10^{23} $cm^{-3}s^{-1}$) to cause an increase in $I_{BL,0}$ for t_{HOLD} > 10 μs. The suppressed recombination due to weak impact ionization in H1 for $V_{BL,W1}$ = 1 to $V_{BL,W1}$ = 1.2 V results in no change in $I_{BL,1}$ with t_{HOLD} as shown in Fig. 4.10 (c). The CR variation is primarily governed by $I_{BL,0}$ (remains independent of $I_{BL,1}$) as shown in Fig. 4.1.1 (d). Hence, maximum t_{DT} (Fig. 4.10 (d)) for cell 10 of 300 μs is obtained at $V_{BL,W1}$ = 1 V. According to Fig. 4.10 (e), the highest t_{DT} (120 μs) due to WL disturbance is achieved at $V_{WL2,W1}$ = 0 V, whereas the highest t_{DT} (300 μs) due BL disturbance is achieved at $V_{BL,W1}$ = 1 V. Also, t_{DT} due to WL disturbance (120 μs) is lower than t_{DT} due to BL disturbance (300 μs) for W1 operation.

4.4.2 Optimizing Write 0 to Maximize Duration of Disturbance Tolerance

W0 operation in cell 00 has been realized with $V_{WL2,W0}$ equal to H bias ($V_{WL2,H}$ = 1 V). W0 causes a reduction in $I_{BL,1}$ in cell 01 due to WL disturbance (Fig. 4.11 (a)) with the degradation being stronger at less negative WL1 bias ($V_{WL1,W0}$ = -0.5 V). A more negative $V_{WL1,W0}$ (-0.7 V) leads to lower recombination in the H1 state due to an increase in the energy barrier, which helps in sustaining holes for a relatively longer duration (t_{DT} = 100 ms) as shown in Fig. 4.11 (b). The

CR variation is primarily governed by the degradation in $I_{BL,1}$ because no change in n_h during the H0 state is observed for $V_{WL1,W0}$ = -0.7 V to $V_{WL1,W0}$ = -0.5 V. Similarly, reduced recombination in H1 state of cell 10 with $V_{BL,W0}$ = -0.7 V (as compared to $V_{BL,W0}$ = -0.9 V) results in subdued degradation of $I_{BL,1}$ due to BL disturbance (Fig. 4.11 (c)). Similar to WL disturbance, the CR variation is primarily governed by the degradation in $I_{BL,1,}$ because no change in n_h during the H0 state is observed. Consequently, t_{DT} improves to 700 μs at $V_{BL,W0}$ = -0.7 V from 5 μs at $V_{BL,W0}$ = -0.9 V (Fig. 4.11 (d)). According to Fig. 4.11 (e), the highest t_{DT} (100 ms) due to WL disturbance is achieved at $V_{WL1,W0}$ = -0.7 V, whereas the highest t_{DT} (700 μs) due to BL disturbance is achieved at $V_{BL,W0}$ = -0.7 V. Also, t_{DT} due to BL disturbance (700 μs) is lower than t_{DT} due to BL disturbance (100 ms) for W0 operation. Since $V_{WL1,W1} = V_{WL1,H}$ = -1 V, WL1 will not contribute to WLD. The optimal biases for W0 operation are $V_{WL2,W0}$ = 1 V, $V_{WL1,W0}$ = -0.7 V, and $V_{BL,W0}$ = -0.7 V.

4.4.3 Optimizing Read to Maximize Duration of Disturbance Tolerance

During R operation (in cell 00), $V_{WL2,R}$ is fixed at H bias ($V_{WL2,H}$ = 1 V). WLD shown in Fig. 4.12 (a) indicates a lower degradation of $I_{BL,1}$ (in cell 01) at $V_{WL1,R}$ = -0.5 V due to reduced recombination (increase in energy barrier) in H1 state at a more negative $V_{WL1,R}$ (= -0.5 V). Hence, t_{DT} improves (Fig. 4.12 (b)) to 140 μs as compared to 3 μs ($V_{WL1,R}$ = -0.3). The subdued degradation of $I_{BL,0}$ (due to BLD) at $V_{BL,R}$ = 0.5 V is a consequence of weak impact ionization in H0 state (Fig. 4.12 (c)). Hence, t_{DT} improves to 28 ms ($V_{BL,R}$ = 0.5 V) as compared to 7 ms ($V_{BL,R}$ = 0.7 V) as shown in Fig. 4.12 (d). WLD (t_{DT} = 140 μs) is severe as compared to BLD (t_{DT} = 28 ms) due to R operation (Fig. 4.12 (e)). WLD, due to W1 and R operations being severe, results in nearly similar t_{DT} values of 120 μs and 140 μs, respectively, while BLD, due to the W1 operation, yields a marginally higher t_{DT} of 300 μs. Since $V_{WL1,W1} = V_{WL1,H}$ = -1 V, WL1 will not contribute towards WLD. Optimal biases for W1 operation are $V_{WL2,W1}$ = 0 V, $V_{WL1,W1}$ = -1 V, and $V_{BL,W1}$ = 1 V. Amongst all operations, W0 contributes least towards disturbance as t_{DT} is higher.

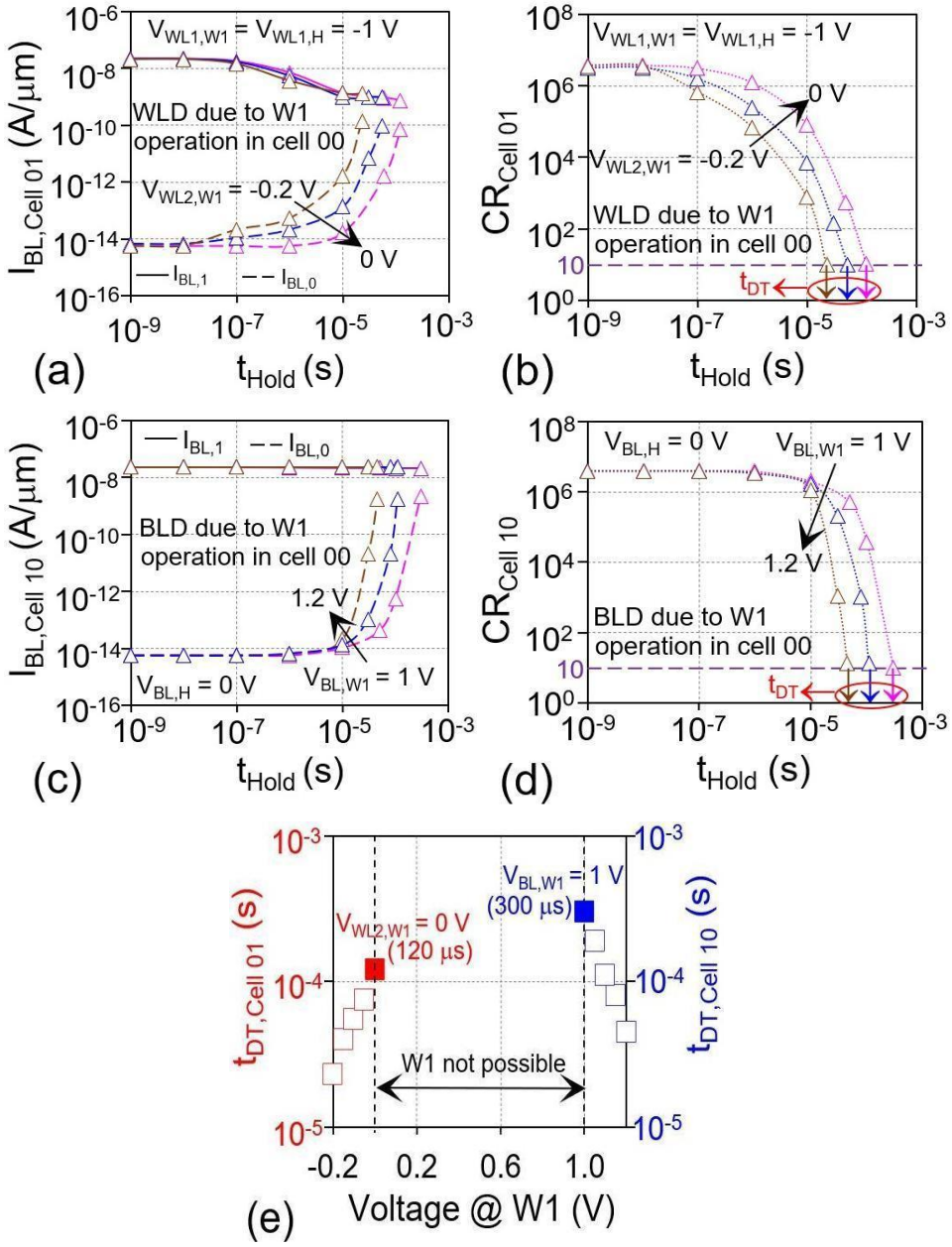

Fig. 4.10 (a) Bit line currents ($I_{BL,1}$, $I_{BL,0}$) and (b) Current Ratio (CR = $I_{BL,1}/I_{BL,0}$) as a function of hold time (t_{HOLD}) due to WLD for W1 operation in cell 00. (c) BL currents and (d) CR as a function of t_{HOLD} due to BLD for W1 operation in cell 00. (e) Dependence of t_{DT} on WL2 and BL for W1 operation. Since $V_{WL1,W1} = V_{WL1,H}$ = -1 V, WL1 will not contribute towards WLD. Optimal biases for W1 operation are $V_{WL2,W1}$ = 0 V, $V_{WL1,W1}$ = -1 V, and $V_{BL,W1}$ = 1 V.

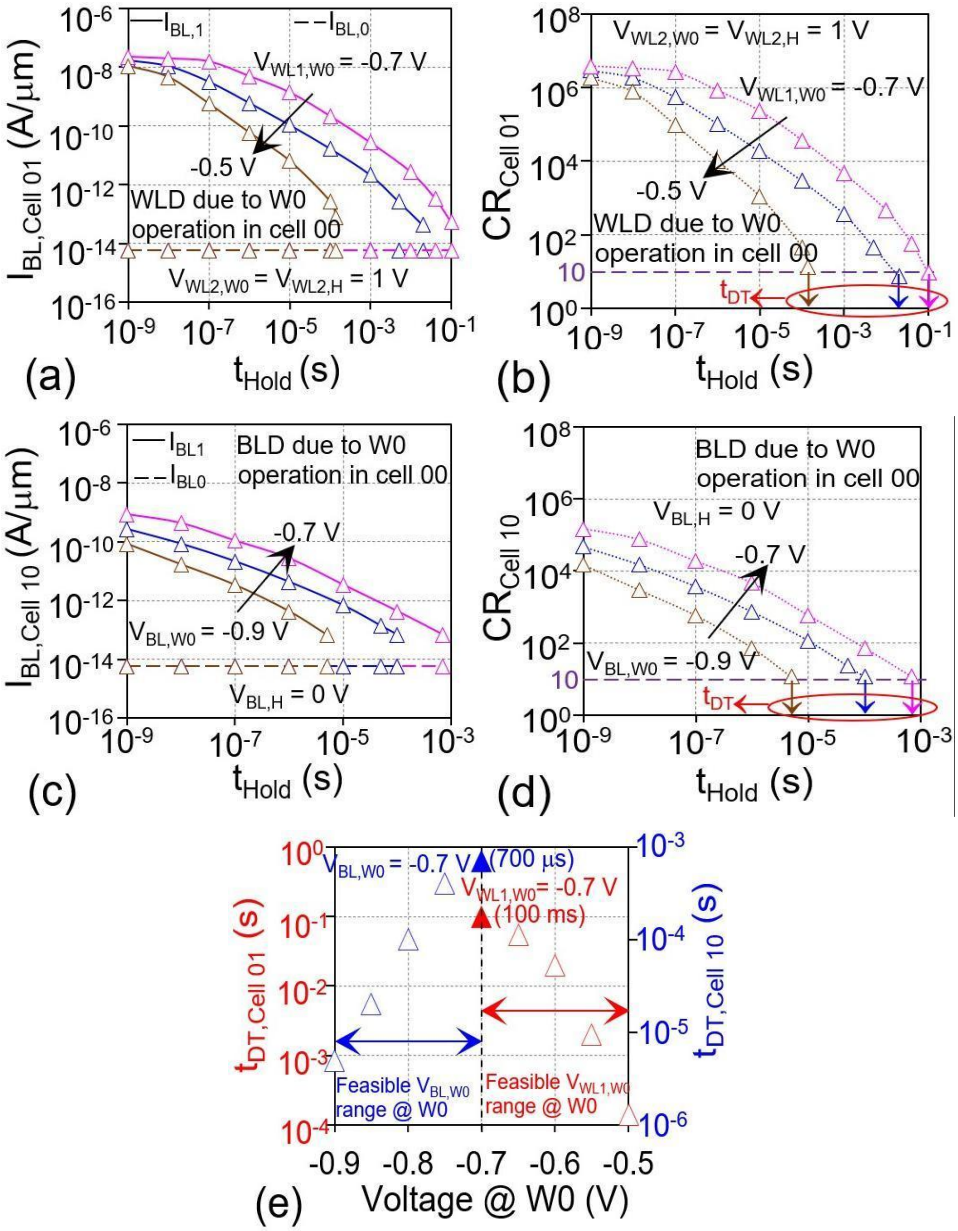

Fig. 4.11 (a) Bit line currents ($I_{BL,1}$, $I_{BL,0}$) and (b) Current Ratio (CR = $I_{BL,1}/I_{BL,0}$) as a function of hold time (t_{HOLD}) due to WLD for W1 operation in. (c) BL currents and (d) CR as a function of t_{HOLD} due to BLD for W1 operation. (e) Dependence of t_{DT} on WL2 and BL for W1 operation. Since $V_{WL2,W0} = V_{WL2,H} = 1$ V, WL2 will not contribute towards WLD. Optimal biases for W0 operation are $V_{WL1,W0} = -0.7$ V, $V_{WL2,W0} = 1$ V, and $V_{BL,W0} = -0.7$ V.

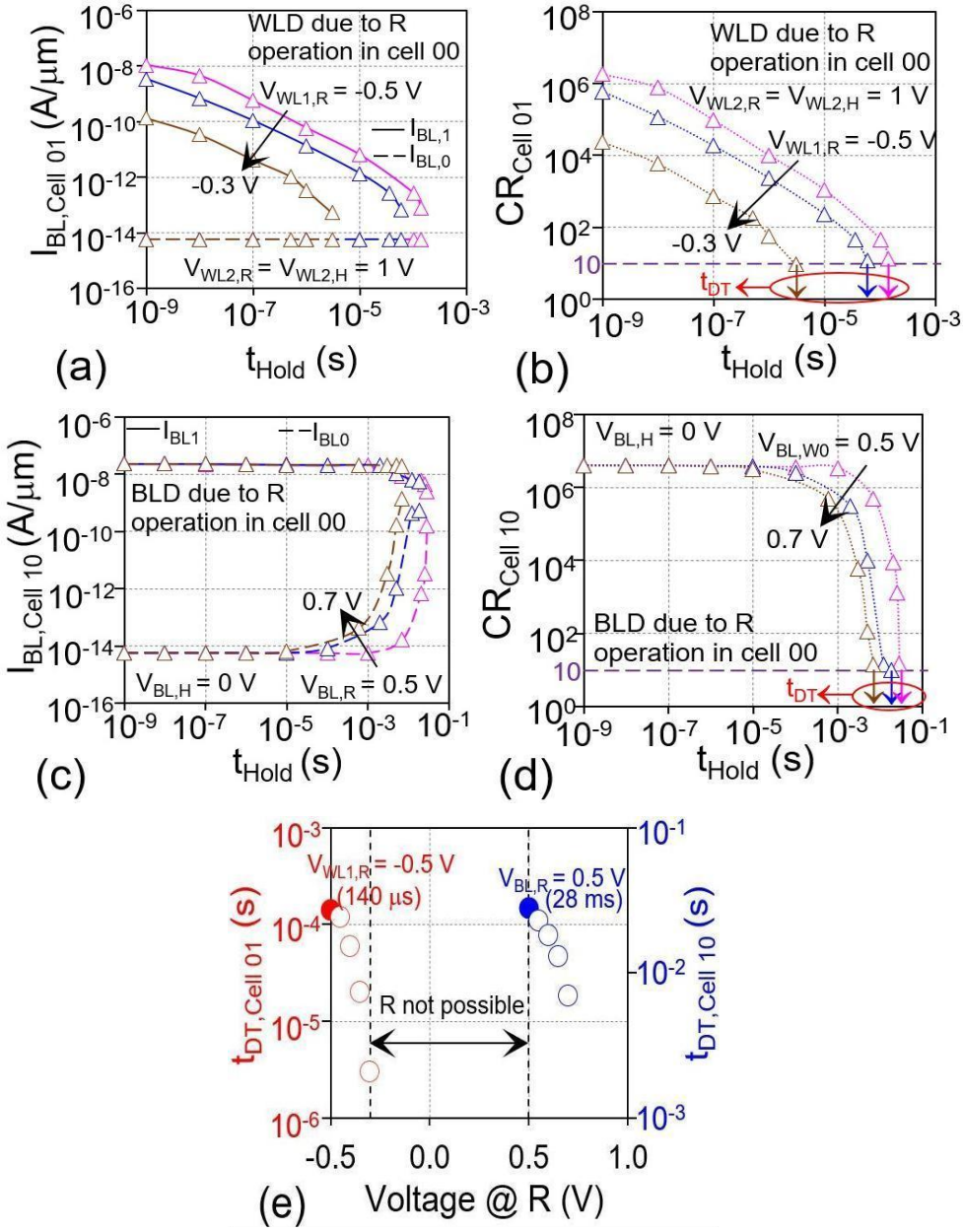

Fig. 4.12 (a) Bit line currents ($I_{BL,1}$, $I_{BL,0}$) and (b) Current Ratio (CR = $I_{BL,1}/I_{BL,0}$) as a function of hold time (t_{HOLD}) due to WLD for W1 operation. (c) BL currents and (d) CR as a function of t_{HOLD} due to BLD for W1 operation. (e) Dependence of t_{DT} on WL2 and BL for W1 operation. Since $V_{WL2,R}$ = $V_{WL2,H}$ = 1 V, WL2 will not contribute towards WLD. Optimal biases for R operation are $V_{WL1,R}$ = -0.5 V, $V_{WL2,R}$ = 1 V, and $V_{BL,R}$ = 0.5 V.

4.4.4 Disturbance through Hole Concentration Contours

Hole concentration (n_h) contours corresponding to minimum t_{DT} (120 µs) due to W1 operation and maximum t_{DT} (100 ms) due to W0 operation are shown in Fig. 4.13 (a)-(b). It is evident from Fig. 4.13 (a) that the minimum t_{DT} is primarily governed by the degradation in the H0 state due to Schottky tunneling whereas the maximum t_{DT} is primarily governed by the degradation in the H1 state due to recombination (Fig. 4.13 (b)). The recombination is suppressed due to the application of V_{WL1} = -0.7 V during W0 operation.

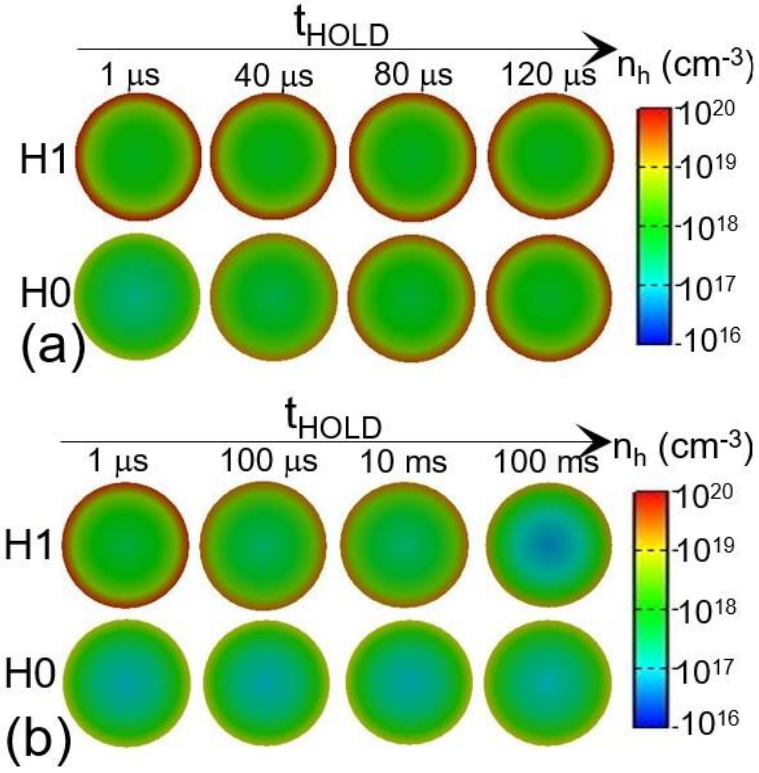

Fig. 4.13 Mid-CG contour plots for hole concentration (n_h) for (a) minimum t_{DT} = 120 µs (H0 degradation) and (b) maximum t_{DT} = 100 ms (H1 deterioration).

4.4.5 Optimized Biases and Corresponding Current Transient

The optimal biases corresponding to W1, W0, and R operations that result in the highest t_{DT} (Figs. 4.10 (e), 4.11 (e), and 4.12 (e)) in the NW GAA RFET-based 1T-DRAM array are shown in Fig. 4.14 (a). One of the WL in each of W1, W0, and R operations is maintained equal to hold bias. The set of biases shown can

be used for 1T-DRAM operation so that it can provide enhanced immunity to WL/BL disturbance in RFET based 1T-DRAM array. The current transient after selecting the biases that provide the highest t_{DT} following W1/W0/R operation on cell 00 is shown in Fig. 4.14 (b). The developed approach provides a guideline for selecting biases during W1/W0/R operation for obtaining highest t_{DT} (maximum immunity) due to WL/BL disturbance.

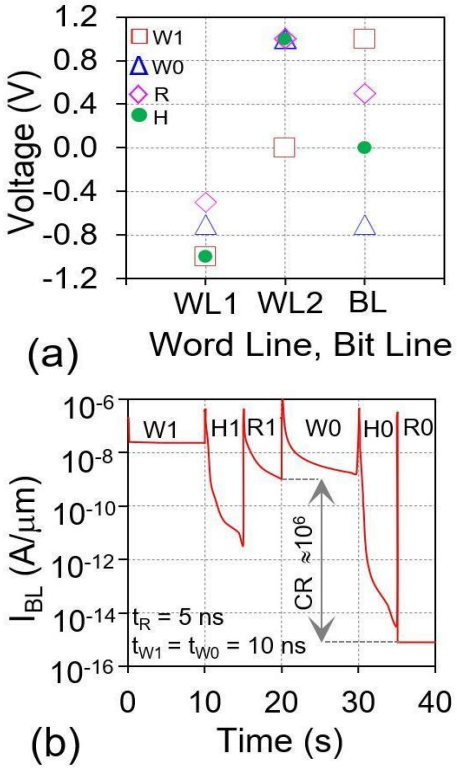

Fig. 4.14 Optimized biases for W1, W0 and R operations based on maximum t_{DT} values for each operation shown in Figs. 4.10 (e), 4.11 (e) and 4.12 (e). (d) Current (I_{BL}) transient in cell 00 for optimized RFET 1T-DRAM. Duration of W1 (t_{W1}) and W0 (t_{W0}) operations is 10 ns, while that of R operation (t_R) is 5 ns.

4.5 Benchmarking

Benchmarking performance metrics are essential to gauge the potential of RFET 1T-DRAM. t_{DT} is a unique metric that can be used to measure the impact of WL and BL disturbance on neighboring cells while performing W1, W0, and R operations. Table 4.5 compares the results of this work with published data for

Body on Gate [241], Wide Trench Surrounding Gate [240], Twin Gate Nanowire [242], and Double Gate Vertical Channel [243] based 1T-DRAM array. NW GAA RFET-based 1T-DRAM exhibits t_{DT} from 120 μs (minimum) to 100 ms (maximum). The minimum t_{DT} of 120 μs is still higher than 10 ns [241], and 100 ns [240] at comparable t_{W1} with lower maximum bias. The higher bias (2 V) with t_{W1} of 20 ns in [243] indicates further scope for 1T-DRAM array optimization. Although [242] exhibits relatively higher t_{DT} (100 ms), the analysis is restricted to a few disturbance cases. In our work, the maximum t_{DT} is 100 ms while considering all disturbance types. The electrical tunability of RFET serves as a distinguishing feature from other transistor topologies, supporting the implementation of RFET as an on-chip memory. RT evaluation through the estimation of CR is useful in scenarios when current drive is limited. Hence, in NW architecture, CR offers a pragmatic way to optimize 1T-DRAM array.

Table 4.5: Benchmarking results of t_{DT} in 1T-DRAM array.

1T-DRAM Reference	**Performance Metrics of 1T-DRAM Array**				
	Electrical Tunability	Disturbance Cases	t_{DT}	t_{W1} (ns)	Maximum Bias (V)
[241]	No	6	10 ns	13	1.3
[240]	No	6	100 ns	10	1.6
[242]	No	< 6	100 ms	10	1.0
[243]	No	< 6	5 μs	20	2.0
This work	Yes	6	120 μs – 100 ms	10	1.0

Most of the research on DRAM has concentrated on enhancing single cell RT and neglected WL and BL disturbance. In such cases, RT should be compared along with access speed and energy efficiency to place the results of RFET single cell RT in proper perspective. Fig. 4.15 shows that NW GAA RFET based 1T-DRAM exhibits a significantly lower energy consumption (< 1 fJ) while requiring a lesser number of voltage levels (n_{VL}) i.e. 2, 3 or 4, and lower supply voltage (V_{DD} = ± 1 V) as compared to the existing 1T-DRAM topologies [224], [174], [204],

[185], [236], [200], [199]. The energy consumption during H1 and H0, W0, and R0 operations remains almost negligible due to the significantly low current drive [196]. The energy consumption is considerable only during W1 and R1 operations due to higher current drive. Hence, energy consumption has been estimated for W1 and R1 operations. The lower energy consumption with n_{VL} = 3 (0.36 fJ) is due to the lower $I_{BL,R1}$ as compared to n_{VL} = 2 (0.55 fJ). A further reduction in the current drive during W1 and R1 operation with n_{VL} = 4 results in relatively lower energy consumption (0.3 fJ), compared to n_{VL} = 2 and 3. Amongst all 1T-DRAMs, twin gate (TG) tunnel field effect transistor (TFET) exhibits maximum RT (~ 1500 ms) but at the cost of higher V_{DD} (3 V) and n_{VL} (6). Only impact-ionization MOS (IMOS) based 1T-DRAM (~ 2.8 fJ) and raised source/drain (RSD) MOSFET based 1T-DRAM (~ 3.8 fJ) show comparable energy to NW GAA RFET 1T-DRAM, but with relatively higher V_{DD} (1.5 V) and n_{VL} (4 to 6). In 1T-DRAM, low energy consumption, less n_{VL}, lower V_{DD}, high CR, and reduced access (read and write) are essential. Thanks to the inherent architecture of NW RFET, all the above can be achieved.

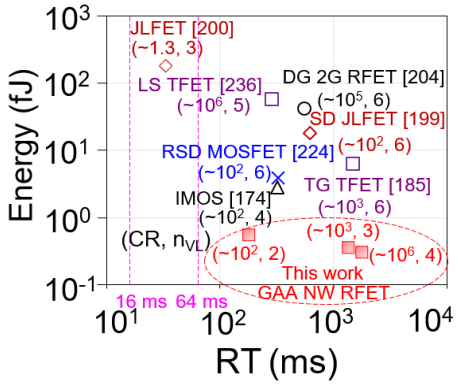

Fig. 4.15 Comparison of energy consumed and single cell RT of NW GAA RFET with existing 1T-DRAM architectures.

Besides energy consumption, the comparison of t_{W1} and t_R, along with V_{DD} for different 1T-DRAM technologies, is shown in Table 4.6. The optimal values t_{W1} and t_R are governed by V_{DD} through the relevant mechanism. The faster write/read operation is often achieved at the cost of high V_{DD}. Hence, an inherent trade-off exists between the three parameters. However, achieving faster write and

read operations at lower supply voltage is an asset for embedded 1T-DRAM. NW GAA RFET has the potential to outperform other 1T-DRAM topologies by achieving sub-5 ns write/read operation at V_{DD} of 1 V. The credit goes to the inherent tunnelling mechanism of RFET that does not require high V_{DD} for W1 operation. The low voltage, faster write/read operation, along with nanowire architecture supporting $4F^2$ integration (where F is the feature size), can become a strong contender for on-chip applications.

Table 4.6: Comparison of write time (t_W), read time (t_R), and supply voltage (V_{DD}) required for optimum RT with existing 1T-DRAM technologies.

1T-DRAM Architecture	t_W (ns)	t_R (ns)	V_{DD} (V)
RSD MOSFET [224]	20	10	2
IMOS [174]	10	10	1.5
DG 2G RFET [204]	1	2	1.5
TG TFET [185]	50	50	2
LS TFET [236]	10	10	2
JLFET [200]	50	100	1.6
SD JLFET [199]	50	100	1.6
This work	5	5	1

4.6 Conclusion

This chapter showcases the feasibility of 1T-DRAM through NW GAA RFET. The higher CR (~10^5) and RT (1.8 s at 85 ºC), low latency (sub-10 ns), and logic-compatible biases (±1 V, ±0.5 V) serve as key indicators supporting the realization of 1T-DRAM with RFETs. The critical aspect of 1T-DRAM array remains WL and BL disturbance, which is essentially governed through bias magnitudes and number of bias levels. Biases should not be selected for enhancing performance indicators but also for minimizing WL and BL disturbance. The biases

used for independent 1T-DRAM operation may not be optimal for array. Hence, separate bias optimization for each cell of the array corresponding to W1, W0, and R operation is essential. Additionally, the set of bias values optimal for logic (±1 V, ±0.5 V) operations may not yield improved performance in 1T-DRAM arrays. Hence, 1T-DRAM operations require a customized set of bias values (± 1 V, ±0.5 V, ±0.7 V) for optimal performance with respect to WLD and BLD.

Chapter 5

Conclusions and Scope for Future Work

5.1 Conclusion

The semiconductor industry has witnessed phenomenal growth over the last sixty years. This has largely been possible through advancements in transistor design, fabrication and characterization, packaging and reliability of materials, devices, circuits and systems. The driving force behind the growth has been the desire to fulfil the prophecy (or observation) of G. Moore on the number of transistors in a semiconductor chip doubling every two years [244]. This historic statement, commonly referred to as Moore's law, along with device scaling strategies [32] has been instrumental for the progress of the semiconductor industry.

Downscaling the gate length while minimizing short channel effects has resulted in significant benefits of smaller, faster and powerful transistors. However, the advantages are also accompanied by challenges. While the number of transistors per die have approached ~10^{10}, the power density of processors has surpassed 100 Wcm^{-2} [244]. The local 'hot spots' on the chip lead to temperature rise and gradients which exceed threshold values leading to reliability concerns. To circumvent the issue, operation at lower supply voltages (than predicted by scaling theories) is desired. Another option is to re-think the approach adopted to downscale devices with a focus on reducing the number of transistors for implementing a particular logic rather than transistor physical size reduction. In terms of conventional Silicon FDSOI CMOS technology, the above two options suggest the use of innovative devices operating with a reduced current drive.

Transistor architecture optimization has vastly contributed to downscaling while limiting short channel effects. The conventional Silicon transistor has

evolved from planar in bulk technology to nanosheet topology in FDSOI technology. Although the innovation has been nothing short of remarkable, the scaling approach focuses on a single transistor without considering multifunctionality. Polymorphic transistor architecture opens new avenues for circuit design which can reduce the transistor count for implementing logic functions. One such architecture is the reconfigurable field effect transistor (also known as programmable transistor) which can function as n-type and p-type transistor from the same physical device [76]. RFET has shown considerable potential for reducing the transistor count to implement logic circuits thereby countering its scaling limitations due to its relatively longer source-to-drain total length. The current drive of RFET is lower than conventional MOSFET due to the presence of ungated regions in the total length and pseudo source/drain regions, both of which contribute to the total resistance. Apart from logic, RFET has shown potential for analog/RF applications at lower current drives [148]. This thesis has contributed to extending the polymorphic features of RFET by exploring its feasibility for dynamic memory implementation. Key outcomes of the thesis work on RFETs are given below.

5.2 Implementing 1T-DRAM with RFET

A planar RFET supports independent front and back control gate operation. While the four program gates, responsible for the formation of pseudo-source/drain regions, can be electrically connected, independent control gate operation is critical for the functioning of 1T-DRAM. The Write 1 operation of RFET based 1T-DRAM is characterized by generating excess holes through the positive feedback mechanism, achieved by applying appropriate biases at the control and program gates and the drain. Excess holes generated (~10^{20} cm^{-3} after 10 ns) during write 1 operation are stored in the electrostatic potential well underneath the back control gate (negative bias). A positive bias at the program gate prevents tunneling of holes from source/drain to channel. The front control gate voltage can be lowered to avoid the generation of electrons in the semiconductor region. Write 0 operation in RFET can be performed by applying a positive bias at the back control gate to remove

(~10^4 cm^{-3}) the excess holes. The most essential aspect is the presence of ungated regions which separate the pseudo source/drain regions (underneath program gates) from the stored holes in the electrostatic potential well. The difference in the hole concentration in write 1 and write 0 states can be sensed through a difference in drain current by appropriate read biases. RFET based 1T-DRAM exhibits a high retention time of 3.2 seconds with a SM > 6 μA/μm at 85 °C. Although retention reduces with an increase in temperature, retention of 160 ms has been obtained at 125 °C. Results indicate the suitability of multifunctional RFET based planar 1T-DRAM to extend the multifunctional attributes of RFET beyond logic and analog/RF applications.

While high retention is an asset for 1T-DRAM, optimal biases at each electrode are crucial for memory functionality. A sensitivity analysis of different voltages was carried out to ascertain the voltage range able to sustain a 50% reduction in the retention while maintaining retention > 64 ms at 85 °C. The analysis of program gate, back control gate, and front control gate biases during hold operation reveals that a wider bias range of at least 0.5 V is available to sustain a reduction of 50% in peak retention. However, during read operation, front and back control voltages are critical for 1T-DRAM, and a minor change of even 75 mV in front control gate bias, and 200 mV in back control gate bias can change the retention by 50%. The biases (front and back control gate) during read are more sensitive to retention. The sensitivity can be reduced to a certain extent through a change in the architecture (lengths) of the RFET. The tradeoff with lower sensitivity will result in a reduction in peak retention time (> 64 ms at 85 °C).

5.3 RFET Length Dependent Bias Optimization

For a fixed total source-to-drain length, RFET can be designed with many different combinations of ungated region length, control gate length and polarity gate length. Each combination will contribute differently towards the storage region and 1T-DRAM functionality. The thesis has explored the impact of varying lengths of different regions and their bias dependencies for implementing 1T-DRAM. The

optimization of length-dependent 1T-DRAM biases starts with the write 1 operation. RFET with longer storage regions (for a fixed total length of 100 nm) exhibits subdued impact ionization for the same set of biases. Hence, a relatively higher front control gate bias is required to generate sufficient excess holes in devices with longer storage regions to enable write 1 operation. A marginally lower back control gate bias is needed to hold excess holes in RFET with longer storage regions. To obtain suitable sense margin, read biases must be optimized for different storage region lengths. RFETs with longer storage regions require higher front control gate biases to achieve a decent read current, which translates into a sense margin > 6 μA/μm and retention time > 1 sec. The methodology adopted in the work is based on modifying one bias per operation while maintaining the same voltage at other electrodes. For on-chip 1T-DRAM with a total length of 100 nm, the minimum write time of 3 ns is sufficient to generate excess holes, while a read duration of 2 ns ensures a minimum retention time of 4 ms at 85 °C.

5.4 1T-DRAM with Nanowire RFET and Array Disturbance

Transistor architecture has evolved considerably due to the push by logic technology requirements. A gate-all-around architecture allows the gate electrode to control the channel potential in an effective manner thus permitting downscaling. Nanowire transistor architecture does not permit separate biasing of front and back gates. Hence, 1T-DRAM operation enabled through independent gate operation cannot be implemented in a nanowire transistor. An alternative way forward for enabling 1T-DRAM functionality is to use the surrounding gate for creating electrostatic potential well. In contrast, the program gates can be used for generating excess holes through Schottky tunneling. 1T-DRAM functionality was demonstrated in a nanowire RFET with a CR of 5 orders and retention of 1.8 s at 85 °C with four distinct voltage levels. A reduction in the number of voltage levels to three resulted in a decrease in CR (3 orders) and retention (1.5 s at 85 °C) for implementing 1T-DRAM. While the performance of a single 1T-DRAM cell (nanowire architecture) was promising, memory is implemented through an array

of cells. For the proper functioning of 1T-DRAM array, the disturbance due to common (shared) word line and bit line should be minimized.

RFET based 1T-DRAM cell has dual word lines due to control and program gates, and one bit line for the drain terminal. Investigating the impact of shared word lines and bit lines on 1T-DRAM performance indicates that word line disturbance due to write 0 operation is severe in comparison to bit line disturbance if the same biases are used as those utilized for an individual cell. The write 0 operation on the desired cell causes hole recombination (due to the lower depth of the potential well) in the adjacent cell connected through the shared word line. An improvement in the retention of 1T-DRAM array requires separate array centric bias optimization. Each 1T-DRAM cell was considered to be in the hold state before the application of bias for realizing an operation (write 1, write 0, read). Since the disturbance due to bias impacts the current ratio, the t_{HOLD} corresponding to current ratio of 10 is considered as the duration of array tolerance of a particular operation. Biases supporting higher values of duration of disturbance tolerance should be selected to minimize array disturbance. It has been shown that the impact of word line disturbance can be suppressed if one word line can be maintained at hold bias while ensuring the feasibility of each 1T-DRAM operation. The challenge of such an approach will be the limited range of biases for which memory operation can be realized. Nevertheless, the approach has shown the capability to improve the duration of disturbance tolerance to a minimum of 120 μs with a current ratio of 6 orders at 85 °C due to write 1 operation. The maximum value of duration of disturbance tolerance was estimated to be 100 ms due to write 0 operation. Results also indicate that word line disturbance due to write 1 (120 μs) and read (140 μs) operations result in minimum values of the duration of disturbance tolerance. A possible way for utilizing these results would be through the implementation of selective refresh cycles focusing on the operations which yield minimum disturbance tolerance (120 μs to 140 μs).

5.5 Scope for Future Work

The thesis focused on implementing 1T0C DRAM through RFET. WLD and BLD can degrade the retention time of array. A possible way of enhancing retention would be through 2T0C DRAM gain cell [245]. The gain cell has been extensively studied with conventional FDSOI transistors and its challenges for achieving higher retention are well understood. The retention of 2T0C gain cell is expected to be higher than that exhibited by 1T0C DRAM. Since RFET can be implemented as n-type and p-type transistor, a 2T0C gain cell can be implemented through RFETs. Two topologies can be implemented: (i) both RFETs function as n-type device, and (ii) each RFET functions as n-type and p-type transistor. While both topologies are interesting, p-type RFET for enabling write operation and n-type RFET for realizing read operation appears to be an interesting choice for enhancing retention. The functionality of both circuit topologies can be explored and retention benchmarked with respect to the published data of gain cells designed with conventional FDSOI transistor. The coupling between the terminals is expected to influence the storage node voltage. Hence, appropriate optimization strategies (for each topology) will be required for an optimal 2T0C RFET gain cell.

Another interesting extension of the proposed work is to explore computing within memory using RFETs. Prior research [245] on 2T0C DRAM has mostly concentrated on improving retention properties with not much literature on enabling in-memory computing. Capacitorless (0C) implementations of compute in-memory have focused on four transistor zero capacitor (4T0C) cell at a 65 nm node [246]. Analog computing requires storage at different voltage levels; hence, an optimization strategy is needed to achieve the desired voltage levels of the transistor. Problems with short channel effects, which tend to deteriorate the input range and weight for analog computing, R-squared value, and standard error, arise when implementing computing with 2T0C DRAM gain cell. RFET based 2T0C gain cell can be explored for realizing computing within memory. Statistical study of device-to-device variations can also be an interesting study for DRAM array optimization with RFETs.

REFERENCES

[1] Colinge J.-P. (2004), Silicon-on-insulator technology: Materials to VLSI, Springer, New York, ISBN: 978-1-4613-4795-8.

[2] Colinge J. -P. (2008), FinFETs and other multi-gate transistors, Springer, New York, ISBN: 978-0-387-71751-7.

[3] Cristoloveanu S. and Li S. S. (1995), Electrical characterization of silicon-on-insulator materials and devices, Springer, New York, ISBN: 978-0-7923-9548-5.

[4] Deleonibus S. (2009), Electronic device architectures for the nano-CMOS era: From ultimate CMOS scaling to beyond CMOS device, Pan Stanford Publishing, Singapore, ISBN: 978-981-4241-28-1.

[5] Hennessy J. L. and Patterson D. A. (2019), Computer architecture - A quantitative approach, Morgan Kaufmann, Cambridge MA, ISBN: 978-0-12-811905-1

[6] Taur Y., and Ning T. K. (2009), Fundamentals of modern VLSI devices, Cambridge University Press, Cambridge, ISBN: 978-0-521-83294-6.

[7] Cristoloveanu S. (2021), Fully depleted silicon-on-insulator nanodevices, mechanisms and characterization, Elsevier, Amsterdam, ISBN: 978-0-12-823165-4.

[8] Liu T. J. K., and Kuhn K. J. (2015), CMOS and beyond: Logic switches for terascale integrated circuits, Cambridge University Press, Cambridge, ISBN: 978-1-107-04318-3.

[9] Moore G. E. (1965), Cramming more components onto integrated circuits, IEEE Solid-State Circuit Newsletter, 38, 114-117, DOI: 10.1109/N-SSC.2006.4785860.

[10] DeBenedictis E. P. (2017), It's time to redefine Moore's law again, Computer, 40, 72-75, DOI: 10.1109/MC.2017.34.

[11] Koomey J. G. (2010), Outperforming Moore's law, IEEE Spectrum, 47, 68-68, DOI: 10.1109/MSPEC.2010.5421913.

[12] Kahng A. B. (2010), Scaling: More than Moore's law, IEEE Design & Test of Computers, 27, 86-87, DOI: 10.1109/MDT.2010.71.

[13] Williams R. S. (2017), What's Next? [The end of Moore's law], Computing in Science & Engineering, 19, 7-13, DOI: 10.1109/MCSE.2017.31.

[14] Chien A. A., Karamcheti V. (2013), Moore's law: The first ending and a new beginning, Computer, 46, 48-53, DOI: 10.1109/MC.2013.431.

[15] Keyes R. W. (2008), Moore's Law today, IEEE Circuits and Systems Magazine, 8, 53-54, DOI: 10.1109/MCAS.2008.923058.

[16] Adee S. (2008), The data: 37 years of Moore's law, IEEE Spectrum, 45, 56-56, DOI: 10.1109/MSPEC.2008.4505312.

[17] Mody C. C. M (2016), The long arm of Moore's law - Microelectronics and American Science, The MIT Press, Cambridge MA, ISBN: 9780262035491.

[18] Moore G. E. (1975), Progress in digital integrated electronics, Proceedings of IEEE International Electron Devices Meeting, 11-13, DOI: 10.1109/N-SSC.2006.4804410.

[19] Mollick E. (2006), Establishing Moore's law, IEEE Annals of the History of Computing, 28, 62-75, DOI: 10.1109/MAHC.2006.45.

[20] Waldrop M. M. (2016), The chips are down for Moore’s law, Nature News, 530, 144-147, DOI:10.1038/530144a.

[21] https://www.microchipusa.com/articles/the-first-intel-microprocessor-the-chip-that-changed-everything.

[22] https://www.apple.com/in/newsroom/2021/10/introducing-m1-pro-and-m1-max-the-most-powerful-chips-apple-has-ever-built/.

[23] Arora N. (2007), MOSFET modeling for VLSI simulation-theory and practice, World Scientific, ISBN: 978-981-256-862-5.

[24] Chauhan Y. S., Lu D. D., Vanugopalan S., Khandelwal S., Duarte J. P., Paydavosi N., Niknejad A., and Hu C. (2015), FinFET modeling for IC simulation and design using the BSIM-CMG standard, Elsevier, San Diego CA, ISBN: 978-0-12-420031-9.

[25] Campbell S. A. (2001), The science and engineering of microelectronic fabrication, Oxford University Press, New York, ISBN: 978-0195136050.

[26] Deleonibus S. (2014), Intelligent integrated systems: Devices, technologies and architectures - Volume 1, Pan Stanford, Singapore, ISBN: 978-981-4411-42-4.

[27] Deleonibus S. (2017), Intelligent nanodevice and nanosystem fabrication: Materials, techniques and new opportunities - Volume 2, Pan Stanford, Singapore, ISBN 978-981-4774-22-2.

[28] Deleonibus S. (2018), Emerging devices for low-power and high-performance nanosystems: Devices physics, new functions, and data processing - Volume 3, Pan Stanford, Singapore, ISBN: 978-981-4800-11-2.

[29] Deleonibus S. (2020), Convergence of more Moore, more than Moore, and beyond moore: Materials, devices, and nanosystems, Pan Stanford, Singapore, ISBN: 978-981-4877-12-1.

[30] https://ed-thelen.org/comp-hist/VAX-11-750.html.

[31] Iwai H. (1999), CMOS technology-year 2010 and beyond, IEEE Journal of Solid-State Circuits, 34, 357-366, DOI: 10.1109/4.748187.

[32] Dennard R. H., Gaensslen F. H., Yu H. N, Rideout V. L., Bassous E., and LeBlanc A. R. (1974), Design of ion-implanted MOSFETs with very small physical dimensions, IEEE Journal of Solid-State Circuits, 9, 256-268, DOI: 10.1109/JSSC.1974.1050511.

[33] Fiegna C., Iwai H., Wada T., Saito M., Sangiorgi E., and Ricco B. (1994), Scaling the MOS transistor below 0.1μm: Methodology, device structures, and technology requirements, IEEE Transactions on Electron Devices, 41, 941-951, DOI: 10.1109/16.293306.

[34] Ono M., Saito M., Yoshitomi T., Fiegna C., Ohguro T., and Iwai H. (1993), Sub-50 nm gate length n-MOSFETs with 10 nm phosphorus source and drain junctions, Proceedings of IEEE International Electron Devices Meeting, 119-122, DOI: 10.1109/IEDM.1993.347385.

[35] Momose H. S., Ono M., Yoshitomi T., Ohguro T., Nakamura S., Saito M., and Iwai H. (1994), Tunneling gate oxide approach to ultra-high current drive in small-geometry MOSFETs, Proceedings of IEEE International Electron Devices Meeting, 593-596, DOI: 10.1109/IEDM.1994.383340.

[36] Momose H. S., Morifuji E., Yoshitomi T., Ohguro T., Saito M., Morimoto T., Katsumata Y., and Iwai H. (1996), High frequency AC characteristics of 1.5 nm gate oxide MOSFETs, Proceedings of IEEE International Electron Devices Meeting, 105-108, DOI: 10.1109/IEDM.1996.553132.

[37] Momose H. S., Ono M., Yoshitomi T., Ohguro T., Nakamura S., Saito M., and Iwai H. (1996), 1.5 nm direct-tunneling gate oxide Si MOSFETs, IEEE Transactions on Electron Devices, 43, 1233-1242, DOI: 10.1109/16.506774.

[38] Chatterjee A., Chapman R. A., Dixit G., Kuehne J., Hattangady S., Yang Y., Brown G. Y., Aggarwal R., Erdogan U., He Q., Hanratty M., Rogers D., Murtaza S., Fang S. J., Kraft R., Potondaro A. L. P., Hu J. C., Terry M., Lee W., Fernando C., Konecni A, Wells G., Frystak D., Bowen C., Rodder M., and Chen I. C. (1997), Sub-100 nm gate length metal gate NMOS transistors fabricated by a replacement gate process, Proceedings of IEEE International Electron Devices Meeting, 821-824, DOI: 10.1109/IEDM.1997.650507.

[39] Timp G., Agarwal A., Baumann F. H., Boone T., Buonanno M., Cirelli R., Donnelly V., Foad M., Grant D., Green M., Gossman H., Hillenisu S., Jackson J., Jacobson D., Kleiman R., Kornblit A., Klemens F., Lee J. T. -C., Mansfield W., Moccio S., Murrell A., O'Malley M., Rosamilia J., Sapjeta J., Siverman P., Sorsch T., Tai W. W., Tennant D., Vuong H., and Weir B. (1997), Low leakage, ultra-thin gate oxides for extremely high performance sub-100 nm nMOSFETs, Proceedings of IEEE International Electron Devices Meeting, 930-932, DOI: 10.1109/IEDM.1997.650534.

[40] Kawaura H., Sakamoto T., Ochiai Y., Fujita J., and Baba T. (1997), Fabrication and characterization of 14-nm-gate length EJ-MOSFETs, Extended Abstracts of Solid State Devices and Materials, 572-573. DOI: 10.7567/SSDM.1997.C-11-5.

[41] Yan R. -H., Ourmazd A., and Lee K. F. (1992), Scaling the Si MOSFET: From bulk to SOI to bulk, IEEE Transactions on Electron Devices, 39, 1704-1710, DOI: 10.1109/16.141237.

[42] Agrawal B., De V. K., Pimbley J. M., and Meindl J. D. (1994), Short channel models and scaling limits of SOI and bulk MOSFETs, IEEE Journal of Solid-State Circuits, 29, 122-125, DOI: 10.1109/4.272115.

[43] Park J. -T., and Colinge J. -P. (2002), Multiple-gate SOI MOSFETs: Device design guidelines, IEEE Transactions on Electron Devices, 49, 2222-2229, DOI: 10.1109/TED.2002.805634.

[44] Colinge J.-P. (2004), Multiple-gate SOI MOSFETs, Solid-State Electronics, 48, 897-905, DOI: 10.1016/j.sse.2003.12.020.

[45] Colinge J. -P. (2007), Multi-gate SOI MOSFETs, Microelectronic Engineering, 84, 2071-2076, DOI: 10.1016/j.mee.2007.04.038.

[46] Koh R. (1999), Buried layer engineering to reduce the drain-induced barrier lowering of sub-0.05 μm SOI-MOSFET, Japanese Journal of Applied Physics, 38, 2294, DOI: 10.1143/JJAP.38.2294.

[47] Sekigawa T., and Hayashi Y. (1984), Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate, Solid-State Electronics, 27, 827-828, DOI: 10.1016/0038-1101(84)90036-4.

[48] K. Suzuki, Tanaka T., Tosaka Y., Horie H., and Arimoto Y. (1993), Scaling theory for double-gate SOI MOSFETs, IEEE Transactions on Electron Devices, 40, 2326-2329, DOI: 10.1109/16.249482.

[49] Tosaka Y., Suzuki K., and Sugii T. (1994), Scaling-parameter-dependent model for subthreshold swing S in double-gate SOI MOSFETs, IEEE Electron Device Letters, 15, 466-468, DOI: 10.1109/55.334669.

[50] Frank D. J., Taur Y., and Wong H. -S. P. (1998), Generalized scale length for two-dimensional effects in MOSFETs, IEEE Electron Device Letters, 19, 385-387, DOI: 10.1109/55.720194.

[51] Auth C. P., and Plummer J. D. (1997), Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFETs, IEEE Electron Device Letters, 18, 74-76, DOI: 10.1109/55.553049.

[52] Ferain I., Colinge C. A., and Colinge J. -P. (2011), Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors, Nature, 479, 310-316, DOI: 10.1038/nature10676.

[53] Hisamoto D., Kaga T., Kawamoto Y., and Takeda E. (1989), A fully depleted lean-channel transistor (DELTA)- A novel vertical ultra-thin SOI MOSFET, Proceedings of IEEE International Electron Devices Meeting, 833-836, DOI: 10.1109/IEDM.1989.74182.

[54] Colinge J. -P., Gao M. H., Romano-Rodriguez A., Maes H., and Claeys C. (1990), Silicon-on-insulator 'gate-all-around device', Proceedings of IEEE International Electron Devices Meeting, 595-598, DOI: 10.1109/IEDM.1990.237128.

[55] Lee S. -Y., Kim S. -M., Yoon E. -J., Oh C. -W., Chung I., Park D., and Kim K. (2003), A novel multibridge-channel MOSFET (MBCFET): fabrication technologies and characteristics, IEEE Transactions on Nanotechnology, 2, 253-257, DOI: 10.1109/TNANO.2003.820777.

[56] Lee S. -Y., Kim S. -M., Yoon E. -J., Oh C. -W., Chung I., Park D., and Kim K. (2004), Three-dimensional MBCFET as an ultimate transistor, IEEE Electron Device Letters, 25, 217-219, DOI: 10.1109/LED.2004.825199.

[57] Weckx P., Ryckaert J., Litta E. D., Yakimets D., Matagne P., Schuddinck P., Jang D., Chehab B., Baert R., Gupta M., Oniki Y., Ragnarsson L. -A., Horiguchi N., Spessot A., and Verkest D. (2019), Novel forksheet device architecture as ultimate logic scaling device towards 2 nm, Proceedings of IEEE International Electron Devices Meeting, 1-4, DOI: 10.1109/IEDM19573.2019.8993635.

[58] Gupta M. K., Weckx P., Schuddinck P., Jang D., Chehab B., Cosemans S., Ryckaert J., and Dehaene W. (2021), A comprehensive study of nanosheet and forksheet SRAM for beyond N5 node, IEEE Transactions on Electron Devices, 68, 3819-3825, DOI: 10.1109/TED.2021.3088392.

[59] Ritzenthaler R., Mertens H., Eneman G., Simoen E., Bury E., Eyben P., Bufler F. M., Oniki Y., Briggs B., Chan B. T., Hikavyy A., Mannaert G., Parvais B., Chasin A., Mitard J., Litta E. D., Samavedam S., and Horiguchi N. (2021), Comparison of electrical performance of co-integrated forksheets and nanosheets transistors for the 2nm technological node and beyond,

Proceedings of IEEE International Electron Devices Meeting, 1-4, DOI: 10.1109/IEDM19574.2021.9720524.

[60] Ryckaert J., Schuddinck J. P., Weckx P., Bouche G., Vincent B., Smith J., Sherazi Y., Mallik A., Mertens H., Demuynck S., Bao T. H., Veloso A., Horiguchi N., Mocuta A., Mocuta D., and Boemmels J., (2018), The complementary FET (CFET) for CMOS scaling beyond N3, Proceedings of IEEE Symposium on VLSI Technology, 1-2, DOI: 10.1109/VLSIT.2018.8510618.

[61] Vincent B., Boemmels J., Ryckaert J., and Ervin J. (2020), A benchmark study of complementary-field effect transistor (CFET) process integration options done by virtual fabrication, IEEE Journal of Electron Devices Society, 8, 668-673, DOI: 10.1109/JEDS.2020.2990718.

[62] Connelly D., Faulkner C., and Grupp D. E. (2003), Performance advantage of Schottky source/drain in ultrathin-body silicon-on-insulator and dual-gate CMOS, IEEE Transactions on Electron Devices, 50, 1340-1345, DOI: 10.1109/TED.2003.813229.

[63] Connelly D., Faulkner C., Grupp D. E., and Harris J. S. (2004), A new route to zero-barrier metal source/drain MOSFETs, IEEE Transactions on Nanotechnology, 3, 98-104, DOI: 10.1109/TNANO.2003.820774.

[64] Tsui B. -Y., and Lin C. -P. (2004), A novel 25-nm modified Schottky-barrier FinFET with high performance, IEEE Electron Device Letters, 25, 430-432, DOI: 10.1109/LED.2004.828980.

[65] Zhu S., Yu H. Y., Whang S. J., Chen J. H., Shen C., Zhu C., Lee S. J., Li M. F., Chan D. S. H., Yoo W. J., Du A., Tung C. H., Singh J., Chin A., and Kwong D. L. (2004), Schottky-Barrier S/D MOSFETs with high-K gate dielectrics and metal-gate electrode, IEEE Electron Device Letters, 25, 268-270, DOI: 10.1109/LED.2004.826569.

[66] Larrieu G., and Dubois E. (2004), Schottky-barrier source/drain MOSFETs on ultrathin SOI body with a tungsten metallic midgap gate, IEEE Electron Device Letters, 25, 801-803, DOI: 10.1109/LED.2004.838053.

[67] Larson J. M., and Snyder J. P. (2006), Overview and status of metal S/D Schottky-barrier MOSFET technology, IEEE Transactions on Electron Devices, 53, 1048-1058, DOI: 10.1109/TED.2006.871842.

[68] Nishi Y. (1970), Insulated gate field effect transistor and its manufacturing method, Japanese Patent, 587527.

[69] Schwarz M., Vethaak T. D., Derycke V., Francheteau A., Iniguez B., Kataria S., Kloes A., Lefloch F., Lemme M., Snyder J. P., Weber W. M., and Calvet L. E. (2023), The Schottky barrier transistor in emerging electronic devices, Nanotechnology, 34, 352003, DOI: 10.1088/1361-6528/acd05f.

[70] Bestelink E., Galderisi G., Golec P., Han Y., Iniguez B., Kloes A., Knoch J., Matsui H., Mikolajick T., Niang K. M., Richstein B., Schwarz M., Sistani M., Sporea R. A., Trommer J., Weber W. M., Zhao Q. -T., and Calvet L. E. (2024), Roadmap for Schottky barrier transistors, Nano Futures, 8, 042001, DOI: 10.1088/2399-1984/ad92d1.

[71] Cho W.- S., Gupta S. K., and Roy K. (2014), Device-circuit analysis of double-gate MOSFETs and Schottky-barrier FETs: A comparison study for sub-10-nm technologies, IEEE Transactions on Electron Devices, 61, 4025-4031, DOI: 10.1109/TED.2014.2364791.

[72] Schwarz M., Calvet L. E., Snyder J. P., Krauss T., Schwalke U., and Kloes A. (2017), On the physical behavior of cryogenic IV and III–V Schottky barrier MOSFET devices, IEEE Transactions on Electron Devices, 64, 3808-3815, DOI: 10.1109/TED.2017.2726899.

[73] Weber W. M., Heinzig A., Trommer J., Martin D., Grube M., and Mikolajick T. (2014), Reconfigurable nanowire electronics – A review, Solid-State Electronics, 102, 12-24, DOI: 10.1016/j.sse.2014.06.010.

[74] Navarro C., Barraud S., Martinie S., Lacord J., Jaud M. -A., and Vinet M. (2017), Reconfigurable field effect transistor for advanced CMOS: Advantages and limitations, Solid-State Electronics, 128, 155-162, DOI: 10.1016/j.sse.2016.10.027.

[75] Weber W. M., and Mikolajick T. (2017), Silicon and germanium nanowire electronics: Physics of conventional and unconventional transistors, Reports on Progress in Physics, 80, 066502, DOI: 10.1088/1361-6633/aa56f0.

[76] Mikolajick T., Heinzig A., Trommer J., Baldauf T., and Weber W. M. (2017), The RFET-a reconfigurable nanowire transistor and its application to novel electronic circuits and systems, Semiconductor Science and Technology, 32, 043001, DOI: 10.1088/1361-6641/aa5581.

[77] Mikolajick T., Galderisi G., Simon M., Rai S., Kumar A., Heinzig A., Weber W. M., and Trommer J. (2021), 20 years of reconfigurable field-effect transistors: From concepts to future applications, Solid-State Electronics, 186, 108036, DOI: https://doi.org/10.1016/j.sse.2021.108036.

[78] Mikolajick T., Galderisi G., Rai S., Simon M., Bockle R., Sistani M., Cakirlar C., Bhattacharjee N., Mauersberger T., Heinzig A., Kumar A., Weber W. M., Trommer J. (2022), Reconfigurable field effect transistors: A technology enablers perspective, Solid-State Electronics, 194, 108381, DOI: 10.1016/j.sse.2022.108381.

[79] Lin H. C., Lin C. Y., Yeh K. L., Huang R. G., Wang M. F., Yu C. M., Huang T. Y., and Sze S. M. (2000), A novel implantless MOS thin-film transistor with simple processing, excellent performance and ambipolar operation capability, Proceedings of International Electron Devices Meeting, 857-859, DOI: 10.1109/IEDM.2000.904452.

[80] Lin H. C, Yeh K. L., Huang R. G., Lin C. Y., and Huang T. Y. (2001), Schottky barrier thin-film transistor (SBTFT) with silicided source/drain and field-induced drain extension, IEEE Electron Device Letters, 22, 179-181, DOI: 10.1109/55.915606.

[81] Heinzig A., Slesazeck S., Kreupl F., Mikolajick T., and Weber W. M. (2011), Reconfigurable silicon nanowire transistors, Nano Letters, 12, 119-124, DOI: 10.1021/nl203094h.

[82] Heinzig A., Mikolajick T., Trommer J., Grimm D., and Weber W. M. (2013), Dually active silicon nanowire transistors and circuits with equal electron and hole transport, Nano Letters, 13, 4176-4181, DOI: 10.1021/nl401826u.

[83] Marchi M. D., Sacchetto D., Frache S., Zhang J., Gaillardon P. -E., Leblebici Y., and Micheli G. D. (2012), Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs, Proceedings of International Electron Devices and Meeting, 8.4.1-8.4.4, DOI: 10.1109/IEDM.2012.6479004.

[84] Marchi M. D., Sacchetto D., Zhang J., Frache S., Gaillardon P. -E., Leblebici Y., and Micheli G. D. (2014), Top-down fabrication of gate-all-around vertically stacked silicon nanowire FETs with controllable polarity, IEEE Transactions on Nanotechnology, 13, 1029-1038, DOI: 10.1109/TNANO.2014.2363386.

[85] Zhang J., Marchi M. D., Sacchetto D., Gaillardon P. -E., Leblebici Y., and Micheli G. D. (2014), Polarity-controllable silicon nanowire transistors with dual threshold voltages, IEEE Transactions on Electron Devices, 61, 3654-3660, DOI: 10.1109/TED.2014.2359112.

[86] Ghosh S., Khan M. B., Chava P., Watanabe K., Taniguchi T., Prucnal S., Hübner R., Mikolajick T., Erbe A., and Georgiev Y. M. (2023), Novel mixed-dimensional hBN-passivated silicon nanowire reconfigurable field effect transistors: Fabrication and characterization, ACS Applied Materials and Interfaces, 15, 40709-40718, DOI: 10.1021/acsami.3c04808.

[87] Trommer J., Heinzig A., Mühle U., Löffler M., Winzer A., Jordan P. M., Beister J., Baldauf T., Geidel M., Adolphi B., Zschech E., Mikolajick T., and Weber W. M. (2017), Enabling energy efficiency and polarity control in germanium nanowire transistors by individually gated nanojunctions, ACS Nano, 11, 1704-1711, DOI: 10.1021/acsnano.6b07531.

[88] Ghosh S., Khan M. B., Prucnal S., Hübner R., Chava P., Mauersberger T., Mikolajick T., Erbe A., and Georgiev Y. M. (2025), High-performance silicon nanowire reconfigurable field effect transistors using flash lamp annealing, ACS Applied Electronic Materials, 7, 2284-2297, DOI: 10.1021/acsaelm.4c01896.

[89] Trommer J., Heinzig A., Baldauf T., Slesazeck S., Mikolajick T., and Weber W. M. (2015), Functionality-enhanced logic gate design enabled by

symmetrical reconfigurable silicon nanowire transistors, IEEE Transactions on Nanotechnology, 14, 689-698, DOI: 10.1109/TNANO.2015.2429893.

[90] Baldauf T., Heinzig A., Trommer J., Mikolajick T., and Weber W. M. (2015), Stress-dependent performance optimization of reconfigurable silicon nanowire transistors, IEEE Electron Device Letters, 36, 991-993, DOI: 10.1109/LED.2015.2471103.

[91] Pregl S., Heinzig A., Baraban L., Cuniberti G., Mikolajick T., and Weber W. M. (2016), Printable parallel arrays of Si nanowire Schottky-barrier-FETs with tunable polarity for complementary logic, IEEE Transactions on Nanotechnology, 15, 549-556, DOI: 10.1109/TNANO.2016.2542525.

[92] Marchi M. D., Sacchetto D., Zhang J., Frache S., Gaillardon P.-E., and Leblebibi Y. (2014), Top-down fabrication of gate-all-around vertically stacked silicon nanowire FETs with controllable polarity, IEEE Transactions on Nanotechnology, 13, 1029-1038, DOI: 10.1109/TNANO.2014.2363386.

[93] Baldauf T., Heinzig A., Mikolajick T., and Weber W. M. (2018), Vertically integrated reconfigurable nanowire arrays, IEEE Electron Device Letters, 39, 1242-1245, DOI: 10.1109/LED.2018.2847902.

[94] Yao Y., Sun Y., Li X., Shi Y., and Liu Y. (2020), Novel reconfigurable field effect transistor with asymmetric spacer engineering at drain side, IEEE Transactions on Electron Devices, 67, 751-757, DOI: 10.1109/TED.2019.2961212.

[95] Li X., Sun Y., Li X., Shi Y., and Liu Z. (2020), Electronic assessment of novel arch-shaped asymmetrical reconfigurable field-effect transistor, IEEE Transactions on Electron Devices, 67, 1894-1901, DOI: 10.1109/TED.2020.2973004.

[96] Trommer J., Simon M., Slesazeck S., Weber W. M., and Mikolajick T. (2020), Inherent charge-sharing-free dynamic logic gates employing transistors with multiple independent inputs, IEEE Journal of Electron Devices Society, 8, 740-747, DOI: 10.1109/JEDS.2020.2986940.

[97] Li X., Sun Y., Liu Z., Li X., Shi Y., Wang T., and Xu J. (2020), Analysis of metal work-function modulation effect in reconfigurable field-effect

transistor, IEEE Transactions Electron Devices, 67, 3745-3752, DOI: 10.1109/TED.2020.3007364.

[98] Li X., Yang X., Zhang Z., Wang T., Sun Y., Liu Z., Li X., Shi Y., and Xu J. (2021), Impact of process fluctuations on reconfigurable silicon nanowire transistor, IEEE Transactions on Electron Devices, 68, 885-891, DOI: 10.1109/TED.2020.3045689.

[99] Sun B., Richstein B., Liebisch P., Frahm T., Scholz S., Trommer J., Mikolajick T., and Knoch J. (2021), On the operation modes of dual-gate reconfigurable nanowire transistors, IEEE Transactions on Electron Devices, 68, 3684-3689, DOI: 10.1109/TED.2021.3081527.

[100] Sun Y., Li X., Liu Z., Liu Y., Li X., and Shi Y. (2022), Vertically stacked nanosheets tree-type reconfigurable transistor with improved on-current, IEEE Transactions on Electron Devices, 69, 370-374, DOI: 10.1109/TED.2021.3126266.

[101] Zhang R., Yang Y., Sun Y., Liu Z., Liu Y., Li X., and Shi Y. (2022), Novel 3-D Fin-RFET with dual-doped source/drain to improve on-state current, IEEE Transactions on Electron Devices, 69, 6569-6575, DOI: 10.1109/TED.2022.3216969.

[102] Hu J., Sun Y., Liu Z., Li X., and Shi Y. (2023), Novel reconfigurable field-effect transistor with arch-shaped gate to improve on-state current, IEEE Transactions on Electron Devices, 70, 4980-4986, DOI: 10.1109/TED.2023.3301457.

[103] Fuchsberger A., Wind L., Nazzari D., Kühberger L., Popp D., Aberl J., Navarrete E. P., Brehm M., Vogl L., Schweizer P., Lellig S., Maeder X., Sistani M., and Weber W. M. (2024), A run-time reconfigurable Ge field-effect transistor with symmetric on-states, IEEE Journal Electron Devices Society, 12, 83 - 87, DOI: 10.1109/JEDS.2024.3350209.

[104] Ye H., Hu J., Liu Z., Wang C., Li X., Shi Y., Mao Z. and Sun Y. (2024), Novel reconfigurable transistor with extended source/drain beyond 3 nm technology node, IEEE Transactions on Electron Devices, 71, 2265-2270, DOI: 10.1109/TED.2024.3359581.

[105] Wang C., Hu J., Liu Z., Li X., Shi Y., and Sun Y. (2024), TCAD simulations of reconfigurable field-effect transistor with embedded-fin-contact to improve on-current, IEEE Transactions on Electron Devices, 71, 2849-2855, DOI: 10.1109/TED.2024.3375829.

[106] Zhang J., Sun Y., Li X., Shi Y., and Liu Z. (2025), Electronic assessment of novel nanosheet RFET with dual-doped source/drain, IEEE Transactions on Electron Devices, 72, 564-571, DOI: 10.1109/TED.2024.3514828.

[107] Ye H., Hu J., Zou X., Sun Z., Li X., Shen Y., Liu Z., Li X., Shi Y., Mao Z., and Sun Y. (2025), Novel negative capacitance reconfigurable transistor with arch-shaped source, IEEE Transactions on Nanotechnology, 24, 209-215, DOI: 10.1109/TNANO.2025.3531844.

[108] Mikolajick T., Heinzig A., Trommer J., Pregl S., Grube M., Cuniberti G., and Weber W. M. (2013), Silicon nanowires-a versatile technology platform, Physica Status Solidi-RRL, 7, 793–799, DOI: 10.1002/pssr.201307247.

[109] Banerjee S., Loffler M., Muehle U., Berent K., Heinzig A., Trommer J., Weber W. M. and Zschech E. (2016), TEM study of Schottky junctions in reconfigurable silicon nanowire devices, Advanced Engineering Materials, 18, 180-184, DOI: 10.1002/adem.201400577.

[110] Böckle R., Sistani M. R., Lipovec B., Pohl D., Rellinghaus B., Lugstein A., and Weber W. M. (2022), A top-down platform enabling Ge based reconfigurable transistors, Advanced Material Technologies, 7, 2100647, DOI: 10.1002/admt.202100647.

[111] Fuchsberger A., Wind L., Sistani M., Behrle R., Nazzari D., Aberl J., Navarrete E. P., Vukŭsić L., Brehm M., Schweizer P., Vogl L., Maeder X., and Weber W. M. (2023), Reconfigurable field-effect transistor technology via heterogeneous integration of SiGe with crystalline Al contacts, Advanced Electronic Materials, 9, 2201259, DOI: 10.1002/aelm.202201259.

[112] Jin X., Zhang S., Li M., and Liu X. (2023), A novel single gate controlled nonvolatile floating program gate reconfigurable FET, Advanced Theory and Simulations, 6, 2200823, DOI: 10.1002/adts.202200823.

[113] Lu B., Liu X., Li Z., Di J., Wang D., Chen Y., Dong L., and Miao Y. (2024), A novel nanosheet reconfigurable field effect transistor with dual-doped source/drain, Microelectronics Journal, 147, 106178, DOI: 10.1016/j.mejo.2024.106178.

[114] Cakirlar C., Simon M., Galderisi G., O'Connor I., Mikolajick T., and Trommer J. (2023), Cross-shape reconfigurable field effect transistor for flexible signal routing, Materials Today Electronics, 4, 100040, DOI: 10.1016/j.mtelec.2023.100040.

[115] Lee S. -H., Park H., Cho W. -J. (2025), Reconfigurable field-effect transistors based on complementary metal-oxide semiconductor-compatible synaptic transistors with hybrid polymer-inspired materials, Journal of Alloys and Compounds, 1032, 181106, DOI: 10.1016/j.jallcom.2025.181106.

[116] Fuchsberger A., Wind L., Nazzari D., Aberl J., Navarrete E. P., Brehm M., Hartmann J. -M., Fournel F., Vogl L., Schweizer P., Minor A. M., Sistani M., and Weber W. M. (2025), Temperature-dependent electronic transport in reconfigurable transistors based on Ge on SOI and strained SOI platforms, Solid-State Electronics, 226, 109055, DOI: 10.1016/j.sse.2024.109055.

[117] Jin X., Yuan X., Zhang S., Li M., and Liu X. (2023), Complementary doped source-based reconfigurable Schottky diode as an equivalence logic gate, ACS Omega, 8, 23120−23129, DOI: 10.1021/acsomega.3c02541.

[118] Trommer J., Heinzig A., Slesazeck S., Mikolajick T., and Weber W. M. (2014), Elementary aspects for circuit implementation of reconfigurable nanowire transistors, IEEE Electron Device Letters, 35, 141-143, DOI: 10.1109/LED.2013.2290555.

[119] Weber W. M., Heinzig A., Trommer J., Grube M., Kreupl F., and Mikolajick T. (2014), Reconfigurable nanowire electronics-enabling a single CMOS circuit technology, IEEE Transactions on Nanotechnology, 13, 1020-1028, DOI: 10.1109/TNANO.2014.2362112.

[120] Rai S., Trommer J., Raitza M., Mikolajick T., Weber W. M., and Kumar A. (2019), Designing efficient circuits based on runtime-reconfigurable field-

effect transistors, IEEE Transactions on Very Large Scale Integration Systems, 27, 560-572, DOI: 10.1109/TVLSI.2018.2884646.

[121] Raitza M., Märcker S., Trommer J., Heinzig A., Klüppelholz S., Baier C., and Kumar A. (2020), Quantitative characterization of reconfigurable transistor logic gates, IEEE Access, 8, 112598-112614, DOI: 10.1109/ACCESS.2020.3001352.

[122] Galderisi G., Mikolajick T., and Trommer J. (2022), Reconfigurable field effect transistors design solutions for delay-invariant logic gates, IEEE Embedded Systems Letters, 14, 107-110, DOI: 10.1109/LES.2022.3144010.

[123] Rai S., Calvino A. T., Riener H., Micheli G. D., and Kumar A. (2023), Utilizing XMG-based synthesis to preserve self-duality for RFET-based circuits, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, 42, 914-927, DOI: 10.1109/TCAD.2022.3184633.

[124] Kavand N., Darjani A., Rai S., and Kumar A. (2023), Design of energy-efficient RFET-based exact and approximate 4:2 compressors and multipliers, IEEE Transactions on Circuits and Systems II: Express Briefs, 70, 3644-3648, DOI: 10.1109/TCSII.2023.3275983.

[125] Galderisi G., Mikolajick T., and Trommer J. (2024), The RGATE: An 8-in-1 polymorphic logic gate built from reconfigurable field effect transistors, IEEE Electron Device Letters, 45, 496-499, DOI: 10.1109/LED.2023.3347397.

[126] Wind L., Fuchsberger A., Demirkiran O., Vogl L., Schweizer P., Maeder X., Sistani M., and Weber W. M. (2024), Reconfigurable Si field-effect transistors with symmetric on-states enabling adaptive complementary and combinational logic, IEEE Transactions on Electron Devices, 71, 1302-1307, DOI: 10.1109/TED.2023.3346361.

[127] Wind L., Maierhofer M., Fuchsberger A., Sistani M., and Weber W. M. (2024), Realization of a complementary full adder based on reconfigurable transistors, IEEE Electron Device Letters, 45, 724-727, DOI: 10.1109/LED.2024.3368110.

[128] Fuchsberger A., Dobler A., Wind L., Kramer A., Kulenkampff J., Reuter M., Nazzari D., Galderisi G., Navarrete E. P., Aberl J., Brehm M., Mikolajick T., Trommer J., Hofmann K., Sistani M., and Weber W. M. (2025), Reconfigurable Ge transistors enabling adaptive differential amplifiers, IEEE Transactions on Electron Devices, 72, 2868-2873, DOI: 10.1109/TED.2025.3559912.

[129] Amarú L., Gaillardon P. -E., Zhang J., and Micheli G. D. (2013), Power-gated differential logic style based on double-gate controllable-polarity transistors, IEEE Transactions on Circuits and Systems II: Express Briefs, 60, 672-676, DOI: 10.1109/TCSII.2013.2277958.

[130] Amarú L., Gaillardon P. -E., and Micheli G. D. (2014), A circuit synthesis flow for controllable-polarity transistors, IEEE Transactions on Nanotechnology, 13, 1074-1083, DOI: 10.1109/TNANO.2014.2361059.

[131] Bobba S. and Micheli G. D. (2015), Layout technique for double-gate silicon nanowire FETs with an efficient sea-of-tiles architecture, IEEE Transactions on Very Large Scale Integration Systems, 26, 2103-2115, DOI: 10.1109/TVLSI.2014.2358884.

[132] Han J., Son J., Jeon J., Shin Y., Cho K., and Kim S. (2023), Reconfigurable logic-in-memory cell comprising triple-gated feedback field-effect transistors, Advanced Electronic Materials, 9, 2300526, DOI: 10.1002/aelm.202300526.

[133] Nazzari D., Wind L., Sistani M., Mayr D., Kim K., Wahler V., and Weber W. M. (2025), Nonvolatile reconfigurable transistor via ferroelectrically induced current modulation, ACS Applied Materials and Interfaces, 17, 10784-10791, DOI: 10.1021/acsami.4c16400.

[134] Zhao R., Liu H., Yang M., Lu T., Li Z., Shi Z., Wang Z., Liu J., Yang Y., and Ren T. -L. (2024), Reconfigurable aJ-level ferroelectric transistor-based boolean logic for logic-in-memory, Nano Letters, 24, 10957-10963, DOI: 10.1021/acs.nanolett.4c02873.

[135] Niu J., Kim D., Li J., Lyu J., Lee Y., and Lee S. (2025), Reconfigurable sequential-logic-in-memory implementation utilizing ferroelectric field

effect transistors, ACS Nano, 19, 5493−5502, DOI: 10.1021/acsnano.4c14062.

[136] Zhu Z., Persson A. E. O., and Wernersson L. -E. (2025), A reconfigurable ferroelectric transistor as an ultra-scaled cell for low-power in-memory data processing, Advanced Electronic Materials, 11, 2400335, DOI: 10.1002/aelm.202400335.

[137] Sistani M., Böckle R., Falkensteiner D., Luong M. A., Hertog M. I., Lugstein A., and Weber W. M. (2021), Nanometer-scale Ge-based adaptable transistors providing programmable negative differential resistance enabling multivalued logic, ACS Nano, 15, 18135-18141, DOI: 10.1021/acsnano.1c06801.

[138] Fuchsberger A., Wind L., Nazzari D., Dobler A., Aberl J., Navarrete E. P., Brehm M., Vogl L., Schweizer P., Lellig S., Maeder X., Sistani M., and Weber W. M. (2024), A reconfigurable Ge transistor functionally diversified by negative differential resistance, IEEE Journal of Electron Devices Society, 12, 541-547, DOI: 10.1109/JEDS.2024.3432971.

[139] Bae J. -H., Kim H., Kwon D., Lim S., Lee S. -T., Park B. -G., and Lee J. -H. (2019), Reconfigurable field-effect transistor as a synaptic device for XNOR binary neural network, IEEE Electron Device Letters, 40, 624-627, DOI: 10.1109/LED.2019.2898448.

[140] Rai S., Patnaik S., Rupani A., Knechtel J., Sinanoglu O., and Kumar A. (2022), Security promises and vulnerabilities in emerging reconfigurable nanotechnology-based circuits, IEEE Transactions on Emerging Topics in Computing, 10, 763-778, DOI: 10.1109/TETC.2020.3039375.

[141] Roemer C., Darbandy G., Schwarz M., Trommer J., Heinzig A., Mikolajick T., Weber W. M., Iñíguez B., and Kloes A. (2022), Physics-based DC compact modeling of Schottky barrier and reconfigurable field-effect transistors, IEEE Journal of Electron Devices Society, 10, 416-423, DOI: 10.1109/JEDS.2021.3136981.

[142] Quijada J. N., Baldauf T., Rai S., Heinzig A., Kumar A., Weber W. M., Mikolajick T., and Trommer J. (2022), Germanium nanowire reconfigurable

transistor model for predictive technology evaluation, IEEE Transactions on Nanotechnology, 21, 728-736, DOI: 10.1109/TNANO.2022.3221836.

[143] Bhattacharjee A., and Dasgupta S. (2018), A compact physics-based surface potential and drain current model for an S/D spacer-based DG-RFET, IEEE Transactions on Electron Devices, 65, 448-455, DOI: 10.1109/TED.2017.2786302.

[144] Park J. W., Lee S. H., Kim S. H., Roh T. M., and Suh D. (2022), Analysis of temporal carrier build-up in reconfigurable field-effect transistor, IET Electronics Letters, 58, 35-37, DOI: 10.1049/ell2.12344.

[145] Hasan M., Gaillardon P. -E, and Rodriguez B. S. (2017), A continuous compact DC model for dual-independent-gate FinFETs, IEEE Journal of Electron Devices Society, 5, 23-31, DOI: 10.1109/JEDS.2016.2632709.

[146] Cadareanu P., Gonzalez J. R., and Gaillardon P. -E. (2021), Parasitic capacitance analysis of three-independent-gate field-effect transistors, IEEE Journal of Electron Devices Society, 9, 400-408, DOI: 10.1109/JEDS.2021.3070475.

[147] Bhattacharjee A., Saikiran M., and Dasgupta S. (2017), A first insight to the thermal dependence of the DC, analog and RF performance of an S/D spacer engineered DG-ambipolar FET, IEEE Transactions on Electron Devices, 64, 4327-4334, DOI: 10.1109/TED.2017.2740320.

[148] Deshpande A. A., Semwal S., Raskin J. -P., and Kranti A. (2023), Insights into parasitic capacitance and reconfigurable FET architecture for enhancing analog/RF metrics, IEEE Transactions on Electron Devices, 70, 5983-5990, DOI: 10.1109/TED.2023.3310943.

[149] Yu S. (2022), Semiconductor memory devices and circuits., CRC Press, ISBN: 9781003138747.

[150] Spessot A., and Oh H. (2020), 1T-1C Dynamic random access memory, status, challenges, and prospects, IEEE Transactions on Electron Devices, 67, 1382-1393, DOI: 10.1109/TED.2020.2963911.

[151] Bonetti A., Golman R., Giterman R., Teman A. and Burg A. (2020), Gain-cell embedded DRAMs: Modeling and design space, IEEE Transactions on

Very Large Scale Integration Systems, 28, 646-659, DOI: 10.1109/TVLSI.2019.2955933T.

[152] Okhonin S., Nagoga M., Sallese J. M., and Fazan P. (2002), A capacitorless 1T-DRAM cell, IEEE Electron Device Letters, 23, 85-87, DOI: 10.1109/55.981314.

[153] Hu C., King T. -J., and Hu C. (2002), A capacitorless double-gate DRAM cell, IEEE Electron Device Letters, 23, 345-347, DOI: 10.1109/LED.2002.1004230.

[154] Kuo C., King T. -J, and Hu C. (2013), A capacitorless double gate DRAM technology for sub-100-nm embedded and stand-alone memory applications, IEEE Transactions on Electron Devices, 50, 2408-2416, DOI: 10.1109/TED.2003.819257.

[155] Villaret A., Ranica R., Malinge P., Masson P., Martinet B., Mazoyer P., Candelier P., and Skotnicki T. (2005), Further insight into the physics and modeling of floating-body capacitorless DRAMs, IEEE Transactions on Electron Devices, 52, 2447-2454, DOI: 10.1109/TED.2005.857933.

[156] Ohsawa T., Fujita K., Hatsuda K., Higashi T., Shino T., Minami Y., Nakajima H., Morikado M., Inoh K., Hamamoto T., Watanabe S., Fujii S., and Furuyama T. (2006), Design of a 128-Mb SOI DRAM using the floating body cell (FBC), IEEE Journal of Solid-State Circuits, 41, 135-145, DOI: 10.1109/JSSC.0051.859018.

[157] Yoshida E., and Tanaka T. (2006), A capacitorless 1T-DRAM technology using gate-induced drain-leakage (GIDL) current for low-power and high-speed embedded memory, IEEE Transactions on Electron Devices, 53, 692-697, DOI: 10.1109/TED.2006.870283.

[158] Jeong H., Song K. -W., Park I. H., Kim T. -H., Lee Y. S., Kim S. -G., Seo J., Cho K., Lee K., Shin H., Lee J. D., and Park B. -G (2007), A new capacitorless 1T DRAM cell: surrounding gate MOSFET with vertical channel (SGVC cell), IEEE Transactions on Nanotechnology, 6, 352-357, DOI: 10.1109/TNANO.2007.893575.

[159] Fossum J. G., Lu Z., and Trivedi V. P. (2007), New insights on capacitorless floating-body DRAM cells, IEEE Electron Device Letters, 28, 513-516, DOI: 10.1109/LED.2007.896883.

[160] Ertosun M. G., Cho H., Kapur P., and Saraswat K. C. (2008), Improving energy efficiency of embedded DRAM caches for high-end , IEEE Electron Device Letters, 29, 615-617, DOI: 10.1109/LED.2008.922969.

[161] Bawedin M., Cristoloveanu S., and Flandre D. (2008), A capacitorless 1T-DRAM on SOI based on dynamic coupling and double-gate operation, IEEE Electron Device Letters, 29, 795-798, DOI: 10.1109/LED.2008.2000601.

[162] Ertosun M. G., Kapur P., and Saraswat K. C. (2008), A highly scalable capacitorless double gate quantum well single transistor DRAM: 1T-QW DRAM, IEEE Electron Device Letters, 29, 1405-1407, DOI: 10.1109/LED.2008.2007508.

[163] Lu Z., Fossum J. G., Yang J. -W., Harris H. R., Trivedi V. P., Chu M., and Thompson S. E. (2009), A simplified superior floating-body/gate DRAM cell, IEEE Electron Device Letters, 30, 282-284, DOI: 10.1109/LED.2008.2012006.

[164] Choi S. -J., Han J. -W., Moon D. -I., and Choi Y. -K. (2010), Analysis and evaluation of a BJT-based 1T-DRAM, IEEE Electron Device Letters, 31, 393-395, DOI: 10.1109/LED.2010.2042675.

[165] Giusi G., Alam M. A., Crupi F., and Pierro S. (2010), Bipolar mode operation and scalability of double-gate capacitorless 1T-DRAM cells, IEEE Transactions on Electron Devices, 57, 1743-1750, DOI: 10.1109/TED.2010.2050104.

[166] Lee W., and Choi W. Y. (2011), A novel capacitorless 1T DRAM cell for data retention time improvement, IEEE Transactions on Nanotechnology, 10, 462-466, DOI: 10.1109/TNANO.2010.2046743.

[167] Lu Z., Fossum J. G., and Zhou Z. (2011), A floating-body/gate DRAM cell upgraded for long retention time, IEEE Electron Device Letters, 32, 731-733, DOI: 10.1109/LED.2011.2134065.

[168] Shim K. -S, Chung I. -Y., and Park Y. J. (2012), A BJT-based heterostructure 1T-DRAM for low-voltage operation, IEEE Electron Device Letters, 33, 14-16, DOI: 10.1109/LED.2011.2172389

[169] Shin J. S., Choi H., Bae H., Jang J., Yun D., Hong E., Kim D. H., and Kim D. M. (2012), Vertical-gate Si/SiGe double-HBT-based capacitorless 1T-DRAM cell for extended retention time at low latch voltage, IEEE Electron Device Letters, 33, 134-136, DOI: 10.1109/LED.2011.2174025.

[170] Wu Q., Chen J., Lu Z., Zhou Z., Luo J., Chai Z., Yu T., Qiu C., Li L., Pang A., Wang X., and Fossum J. G. (2012), Experimental demonstration of the high-performance floating-body/gate DRAM cell for embedded memories, IEEE Electron Device Letters, 33, 743-745, DOI: 10.1109/LED.2012.2190031.

[171] Lin J. -T., Lin P. -H., Eng Y. -C., and Chen Y. -R. (2013), Novel vertical SOI-based 1T-DRAM with trench body structure, IEEE Transactions on Electron Devices, 60, 1872-1877, DOI: 10.1109/TED.2013.2259171.

[172] Kim D. -O., Moon D. -I., and Choi Y. -K. (2014), Optimization of bias schemes for long-term endurable 1T-DRAM through the use of the biristor mode operation, IEEE Electron Device Letters, 35, 220-222, DOI: 10.1109/LED.2013.2295240.

[173] Lin J. -T, Lee W. -H, Lin P. -H, Haga S. W., Chen Y. -R., and Kranti A. (2017), A new electron bridge channel 1T-DRAM employing underlap region charge storage, IEEE Journal of Electron Devices Society, 5, 59-63, DOI: 10.1109/JEDS.2016.2633274.

[174] Lahgere A., and Kumar M. J. (2017), 1T capacitorless DRAM using bandgap-engineered silicon-germanium bipolar I-MOS, IEEE Transactions on Electron Devices, 64, 1583-1590, DOI: 10.1109/TED.2017.2669096.

[175] Lahgere A., and Kumar M. J. (2018), 1T capacitorless DRAM using laterally bandgap engineered Si-Si:C heterostructure bipolar I-MOS for improved sensing margin and retention time, IEEE Transactions on Nanotechnology, 17, 543-551, DOI: 10.1109/TNANO.2018.2825394.

[176] Bashir M. Y., Jaiswal A. K., Patel S. D., and Sahay S. (2024), Revisiting lateral-BTBT gate-induced drain leakage in nanowire FETs for 1T-DRAM, IEEE Transactions on Electron Devices, 71, 2714-2720, DOI: 10.1109/TED.2024.3365773.

[177] Kuo P. -Y. (2024), One-transistor poly-Si memory devices with near-zero subthreshold swing and extended retention time, IEEE Electron Device Letters, 45, 1008-1011, DOI: 10.1109/LED.2024.3387438.

[178] Xie H., Zhang W., Zhou P., Cristoloveanu S., Xu Y., Liu F. Y., and Wan J. (2024), A novel 1T-DRAM fabricated with 22 nm FD-SOI technology, IEEE Electron Device Letters, 45, 558-561, DOI: 10.1109/LED.2024.3368522.

[179] Bae J. -H, Back J. -W., Kwon M. -W., Seo J. H., Yoo K., Woo S. Y., Park K., Park B. -G., and Lee J. -H. (2019), Characterization of a capacitorless DRAM cell for cryogenic memory applications, IEEE Electron Device Letters, 40, 1614-1617, DOI: 10.1109/LED.2019.2933504.

[180] Wan J., Royer C. L, Zaslavsky A., and Cristoloveanu S. (2012), A compact capacitor-Less high-speed DRAM using field effect-controlled charge regeneration, IEEE Electron Device Letters, 33, 179-181, DOI: 10.1109/LED.2011.2176908.

[181] Kwon S., and Yun I. (2024), Asymmetric and double-layered gate-all-around structures of 1T-DRAM for sensing margin and retention improvement, IEEE Transactions on Electron Devices, 71, 3627-3632, DOI: 10.1109/TED.2024.3385394.

[182] Biswas A., and Ionescu A. M. (2015), 1T capacitor-less DRAM cell based on asymmetric tunnel FET design, IEEE Journal of Electron Devices Society, 3, 217-222, DOI: 10.1109/JEDS.2014.2382759.

[183] Biswas A., Dagtekin N., Grabinski W., Bazigos A., Royer C.L., Hartmann J. -M., Tabone C., Vinet M., and Ionescu A. M. (2014), Investigation of tunnel field-effect transistors as a capacitor-less memory cell, Applied Physics Letters, 104, 092108, DOI: 10.1063/1.4867527.

[184] Navlakha N., Lin J. -T., and Kranti A. (2016), Improving retention time in tunnel field effect transistor based dynamic memory by back gate

engineering, Journal of Applied Physics, 119, 214501, DOI: 10.1063/1.4953086.

[185] Navlakha N., Lin J. -T., and Kranti A. (2016), Improved retention time in twin gate 1T DRAM with tunneling based read mechanism, IEEE Electron Device Letters, 37, 1127-1130, DOI: 10.1109/LED.2016.2593700.

[186] Navlakha N., Lin J. -T., and Kranti A. (2017), Retention and scalability perspective of sub-100-nm double gate tunnel FET DRAM, IEEE Transactions on Electron Devices, 64, 1561-1567, DOI: 10.1109/TED.2017.2662703.

[187] Kwon S., Navarro C., Gamiz F., Cristoloveanu S., Kim Y. -T., and Ahn J. (2021), Memory operation of Z^2-FET without selector at high temperature, IEEE Journal of Electron Devices Society, 9, 658-662, DOI: 10.1109/JEDS.2021.3094104.

[188] Kwon S., Navarro C., Gamiz F., Galy P., Cristoloveanu S., Kim Y. -T, and Ahn J. (2021), Improved retention characteristics of Z^2-FET employing half back-gate control, IEEE Transactions on Electron Devices, 68, 1041-1044, DOI: 10.1109/TED.2021.3053514.

[189] Kwon S., Navarro C., Galy P., Cristoloveanu S., Gamiz F., Ahn J., and Kim Y. -T. (2020), Memory operations of zero impact ionization, zero subthreshold swing FET matrix without selectors, IEEE Electron Device Letters, 41, 361-364, DOI: 10.1109/LED.2020.2967773.

[190] Navarro S., Navarro C., Marquez C., Salazar N., Galy P., Cristoloveanu S., and Gamiz F. (2019), Reliability study of thin-oxide zero-ionization, zero-swing FET 1T-DRAM memory cell, IEEE Electron Device Letters, 40, 1084-1087, DOI: 10.1109/LED.2019.2915118.

[191] Navarro S., Navarro C., Marquez C., Dirani H. E., Galy P., Bawedin M., Pickering A., Cristoloveanu S., and Gamiz F. (2018), Experimental demonstration of operational Z^2-FET memory matrix, IEEE Electron Device Letters, 39, 660-663, DOI: 10.1109/LED.2018.2819801.

[192] Navarro C., Duan M., Parihar M. S., Adamu-Lema F., Coseman S., Lacord J., Lee K., Sampedro C., Cheng B., Dirani H. E., Barbe J. -C., Fonteneau P.,

Kim S. -I., Cristoloveanu S., Bawedin M., Millar C., Galy P., Royer C. L., Karg S., Riel H., Wells P., Kim Y. -T, Asenov A., and Gamiz F. (2017), Z^2-FET as capacitor-less eDRAM cell for high-density integration, IEEE Transactions on Electron Devices, 64, 4904-4909, DOI: 10.1109/TED.2017.2759308.

[193] Fonteneau p., Bawedin M., Millar C., Galy P., Royer C. L., Karg S., Wells P., Kim Y. -T., Asenov A., Cristoloveanu S., and Gamiz F. (2017), Extended analysis of the Z^2-FET: Operation as capacitorless eDRAM, IEEE Transactions on Electron Devices, 64, 4486-4491, DOI: 10.1109/TED.2017.2751141.

[194] Martinie S., Lacord J., Lee K., Bawedin M., and Cristoloveanu S. (2021), Pragmatic Z^2-FET compact model including DC and 1T-DRAM memory operation, Solid-State Electronics, 179, 107960, DOI: 10.1016/j.sse.2021.107960

[195] Navarro S., Marquez C., Lee K. H., Navarro C., Parihar M. S., Park H., Galy P., Bawedin M., Kim Y. -T., Cristoloveanu S., and Gamiz F. (2019), Investigation of thin gate-stack Z^2-FET devices as capacitor-less memory cells, Solid-State Electronics, 159, 12-18, DOI: 10.1016/j.sse.2019.03.040

[196] Cristoloveanu S., Lee K. H., Parihar M. S., Dirani H. E., Lacord J., Martinie S., Royer C. L., Barbe J. -C., Mescot X., Fonteneau P., Galy P., Gamiz F., Navarro C., Cheng B., Duan M., Adamu-Lema F., Asenov A., Taur Y., Xu Y., Kim Y. -T., and Bawedin M. (2019), A review of the Z^2-FET 1T-DRAM memory: Operation mechanisms and key parameters, Solid-State Electronics,143, 10-19, DOI: 10.1016/j.sse.2017.11.012.

[197] Ansari M. H. R., Navlakha N., Lin J. -T, and Kranti A. (2018), Doping dependent assessment of accumulation mode and junctionless FET for 1T DRAM, IEEE Transactions on Electron Devices, 65, 1205-1210, DOI: 10.1109/TED.2018.2789901.

[198] Ansari M. H. R., Navlakha N., Lin J. -T., and Kranti A. (2018), High retention with n-oxide-p junctionless architecture for 1T DRAM, IEEE Transactions on Electron Devices, 65, 2797-2803, DOI: 10.1109/TED.2018.2829983.

[199] Ansari M. H. R., Navlakha N., Lin J. -T., and Kranti A. (2019), 1T-DRAM with shell-doped architecture, IEEE Transactions on Electron Devices, 66, 428-435, DOI: 10.1109/TED.2018.2882556.

[200] Ansari M. H. R., Navlakha N., Lee J. Y., and Cho S. (2020), Double-gate junctionless 1T DRAM with physical barriers for retention improvement, IEEE Transactions on Electron Devices, 67, 1471-1479, DOI: 10.1109/TED.2020.2976638.

[201] Kim D., and Lim D. (2025), Logic and static memory functions of an inverter comprising a feedback field effect transistor, Nanotechnology, 36, 175201, DOI: 10.1088/1361-6528/adbf27.

[202] Han S., Kim Y., Son D., Baac H. W., Won S., and Shin C. (2022), Study on memory characteristics of fin-shaped feedback field effect transistor, Semiconductor Science and Technology, 36, 065006, DOI: 10.1088/1361-6641/ac643e.

[203] Lin J. -T., Sun W. -T., Lin H. -H., Chen Y. -J., Navlakha N., and Kranti A. (2019), Raised body doping-less 1T-DRAM with source/drain Schottky contact, IEEE Journal of Electron Devices Society, 7, 276-281, DOI: 10.1109/JEDS.2019.2896412.

[204] Roy A. S., Semwal S., and Kranti A. (2022), An insightful assessment of 1T-DRAM with misaligned polarity gate in RFET, IEEE Transactions on Electron Devices, 69, 3163-3168, DOI: 10.1109/TED.2022.3170284.

[205] Zou X., Gong F., Jin M., Liu Z., Li X., Shen Y., Ye B., Zhang Y., Shi Y., Chen S., and Sun Y. (2025), Evaluation of 1T-DRAM based on novel triple-gate nanosheet RFET with surrounded SiGe channel, IEEE Transactions on Electron Devices, 72, 2292-2298, DOI: 10.1109/TED.2025.3549398.

[206] Song K. -W., Jeong H., Lee J. -W., Hong S. I., Tak N.-K., Kim Y.-T., Choi Y. L., Joo H. S., Kim S. H., Song H. J., Oh Y. C., Kim W. S., Lee Y.-T., Oh K., and Kim C. (2008), 55 nm capacitor-less 1T DRAM cell transistor with non-overlap structure, Proceedings of IEEE International Electron Devices Meeting,797-800, 2008, DOI: 10.1109/IEDM.2008.4796818.

[207] Zhang J., Marchi M. D., Gaillardon P. -E., and Micheli G. D. (2014), A Schottky-barrier silicon FinFET with 6.0 mV/dec subthreshold slope over 5 decades of current, Proceedings of IEEE International Electron Devices Meeting, 13.4.1-13.4.4, DOI: 10.1109/IEDM.2014.7047045.

[208] Padilla J. L., Knoll L., Gamiz F., Zhao Q. T., Godoy A., and Mantl S. (2012), Simulation of fabricated 20-nm Schottky barrier MOSFETs on SOI: Impact of barrier lowering, IEEE Transactions on Electron Devices, 59, 1320-1327, DOI: 10.1109/TED.2012.2187657.

[209] Reuter M., Pfau J., Krauss T. A., Becker J., and Hofmann K. (2021), From MOSFETs to ambipolar transistors: Standard cell synthesis for the planar RFET technology, IEEE Transactions on Circuits and Systems I: Regular Papers, 68, 114-125, DOI: 10.1109/TCSI.2020.3035889.

[210] Zhang J., Gaillardon P. -E., and Micheli G.D. (2013), Dual-threshold-voltage configurable circuits with three-independent-gate silicon nanowire FETs, Proceedings of IEEE International Symposium on Circuits and Systems, 2111-2114, DOI: 10.1109/ISCAS.2013.6572291.

[211] Rai S., Rupani A., Nath P., and Kumar A. (2019), Hardware watermarking using polymorphic inverter designs based on reconfigurable nanotechnologies, Proceedings of IEEE Computer Society Annual Symposium on VLSI, 663-669, DOI: 10.1109/ISVLSI.2019.00123.

[212] Marchi M. D. (2015), Polarity control at runtime: From circuit concept to device fabrication, Doctoral dissertation, ´Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, DOI: 10.5075/epfl-thesis-6821.

[213] ATLAS User's Manual, (2016), Silvaco Inc., USA.

[214] Nicoletti T., Aoulaiche M., Almeida L. M., Santos S. D., Martino J. A., Veloso A., Jurczak M., Simoen E., and Claeys C. (2012), The dependence of retention time on gate length in UTBOX FBRAM with different source/drain junction engineering, IEEE Electron Device Letters, 33, 940-942, DOI: 10.1016/j.sse.2014.04.031.

[215] Ansari M. H. R., and Singh J. (2020), Capacitorless 2T-DRAM for higher retention time and sense margin, IEEE Transactions on Electron Devices, 67, 902-906, DOI: 10.1109/TED.2020.2963995.

[216] Lim T. C., Armstrong G. A. (2005), Parameter sensitivity for optimal design of 65 nm node double gate SOI transistors, Solid-State Electronics, 49, 1034-43, DOI: 10.1016/j. sse.2005.03.023.

[217] Marchi M. D., Zhang J., Frache S., Sacchetto D., Gaillardon P. -E., Leblebici Y., and Micheli G.D. (2014), Configurable logic gates using polarity-controlled silicon nanowire gate-all-around FETs, IEEE Electron Device Letters, 35, 880-882, DOI: 10.1109/LED.2014.2329919.

[218] Arnold W. H. (2007), Challenges for lithography scaling to 32 nm and below, International Symposium on VLSI Technology, Systems and Applications, 1-4, DOI: 10.1109/VTSA.2007.378926.

[219] Mane S., Semwal S., and Kranti A. (2021), Improved mobility extraction methodology for reconfigurable transistors considering resistive components and effective drain bias, IEEE Transactions on Electron Devices, 68, 4797-4800, DOI: 10.1109/TED.2021.3096500.

[220] Puget S., Bossu G., Fenouiller C. B., Perreau P., Masson P., Mazoyer P., Lorenzini P., Portal P., Bouchakour R., and Skotnicki T. (2009), FDSOI floating body cell eDRAM using gate-induced drain-leakage (GIDL) write current for high speed and low power applications, Proceedings of IEEE International Memory Workshop, 1-2, DOI: 10.1109/IMW.2009.5090590.

[221] Hou J., Shao Z., and Miao X. (2009), A high speed low power capacitorless SOI-DRAM cell using impact ionization and GIDL effect, Proceedings of IEEE International Conference of Electron Devices and Solid-State Circuits, 517-20, DOI: 10.1109/EDSSC.2009.5394198.

[222] Parihar M. S., Lee K. H., Dirani H. E., Navarro C., and Lacord J. (2017), Low-power Z^2-FET capacitorless 1T-DRAM, Proceedings of IEEE International Memory Workshop, 1-4, Doi: 10.1109/IMW.2017.7939093.

[223] Navlakha N., Ansari M. H. R., Lin J. -T., and Kranti A. (2018), Performance assessment of TFET architectures as 1T-DRAM, Proceedings of IEEE SOI-

3D-Subthreshold Microelectronics Technology Unified Conference, 1-3, DOI: 10.1109/S3S.2018.8640200.

[224] Ansari M. H. R., and Cho S. (2021), Performance improvement of 1T DRAM by raised source and drain engineering, IEEE Transactions on Electron Devices, 68, 1577-1584, DOI: 10.1109/TED.2021.3056952.

[225] Zhang J., Trommer J., Weber W. M., Gaillardon P. E, and Micheli G. D. (2015), On temperature dependency of steep subthreshold slope in dual-independent-gate FinFET, IEEE Journal of the Electron Devices Society, 3, 452-456, DOI:10.1109/JEDS.2015.2482123.

[226] Liu Y., Matsukawa T., Endo K., Masahara M., Ishii K., Yamauchi H., Tsukada J., Ishikawa Y., and Suzuki E. (2007), Cointegration of high-performance tied-gate three-terminal FinFETs and variable threshold-voltage independent-gate four-terminal FinFETs with asymmetric gate-oxide thicknesses, IEEE Electron Device Letters, 28, 517-9, DOI: 10.1109/LED.2007.896898.

[227] Zhang J., Marchi M. D., Gaillardon P. -E., and Micheli G. D. (2014), A Schottky-barrier silicon FinFET with 6.0 mV/dec subthreshold slope over 5 decades of current, Proceedings of IEEE International Electron Devices Meeting, 13.4.1-13.4.4, DOI: 10.1109/IEDM.2014.7047045.

[228] Song J., Yu B., Yuan Y., and Taur Y. (2009), A Review on Compact Modeling of Multiple-Gate MOSFETs, IEEE Transactions on Circuits and Systems I, 56, 1858-1869, DOI: 10.1109/TCSI.2009.2028416.

[229] Tung R. T. (2014), The physics and chemistry of the Schottky barrier height, Applied Physics Review, 1, 0111304.

[230] Wan J., Royer C. L., Zaslavsky A., and Cristoloveanu S. (2013), Progress in Z^2-FET 1T-DRAM: retention time, writing modes, selective array operation, and dual bit storage, Solid State Electronics, 84, 147–54, DOI: 10.1016/j.sse.2013.02.010.

[231] Kim S. K., and Popovici M. (2018), Future of dynamic random-access memory as main memory, MRS Bulletin, 43, 334-339, DOI: 10.1557/mrs.2018.95.

[232] Mittal S., Vetter J. S., and Li D. (2014), Improving energy efficiency of embedded DRAM caches for high-end computing systems, Proceedings of International ACM Symposium on High Performance and Parallel Distributed Computing, 99-110, DOI: 10.1145/2600212.2600216.

[233] Veloso A., Huynh-Bao T., Matagne P., Jang D., Eneman G., Horiguchi N., and Ryckaert J. (2020), Nanowire & nanosheet FETs for ultra-scaled, high-density logic and memory applications, Solid-State Electronics, 168, 107736, DOI: 10.1016/j.sse.2019.107736.

[234] Ebrahimi M. S., Hills G., Sabry M. M., Shulaker M. M., Wei H., Wu T. F., Mitra S., and Wong H. S. P. (2014), Monolithic 3D integration advances and challenges: From technology to system levels, Proceedings of IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, 1-2, DOI: 10.1109/S3S.2014.7028198.

[235] Takato H., Koike H., Yoshida T., and Ishiuchi H. (1999), Embedded DRAM technology: Past, present and future," Proceedings of IEEE International Symposium on VLSI Technology, System, and Applications, 239–242, DOI: 10.1109/VTSA.1999.786044.

[236] Kamal N., Kamal A. K., and Singh J. (2021), L-shaped tunnel field-effect transistor-based 1T DRAM with improved read current ratio, retention time, and sense margin, IEEE Transactions on Electron Devices, 68, pp. 2705-2711, DOI: 10.1109/TED.2021.3074348.

[237] Steyaert M., Breussegem T. V., Meyvaert H., Callemeyn P., and Wens M. (2011), DC-DC converters: from discrete towards fully integrated CMOS, Proceedings of IEEE European Solid-State Circuit Research Conference, 42-49, DOI: 10.1109/ESSDERC.2011.6044234.

[238] Yu E., Cho S., Shin H., and Park B. -G. (2019), A band-engineered one-transistor DRAM with improved data retention and power efficiency, IEEE Electron Device Letters, 40, 562-565, DOI: 10.1109/LED.2019.2902334.

[239] Kim Y., Kwon M. -W., Ryoo K. -C., Cho S., and Park B. -G. (2018), Design and electrical characterization of 2-T thyristor RAM with low power

consumption, IEEE Electron Device Letters, 39, 355-358, DOI: 10.1109/LED.2018.2796139.

[240] Lin J. -T., Lin P. H., Haga S. W., Wang Y. -C., and Lu D. R. (2015), Transient and thermal analysis on disturbance immunity for $4F^2$ surrounding gate 1T-DRAM with wide trenched body, IEEE Transactions on Electron Devices, 62, 61-68, DOI: 10.1109/TED.2014.2372789.

[241] Lin J. -T., Lin H. H., Chen Y. J., Yu C, Y., Kranti A., Lin C. C., and Lee W. H. (2017), Vertical transistor with n-bridge and body on gate for low-power 1T-DRAM application, IEEE Transactions on Electron Devices, 64, 4937-4945, Dec. DOI: 10.1109/TED.2017.2766563.

[242] Jang S. H., and Kim T. W. (2022), Retention time analysis in a 1T-DRAM with a vertical twin gate and p+/i/n+ silicon nanowire, IEEE Transactions on Electron Devices, 69, 4909-4913, DOI: 10.1109/TED.2022.3193349.

[243] Kwon W., Liu T. J. (2010), A highly scalable capacitor-less cell having a doubly gated vertical channel, Japanese Journal of Applied Physics, 49, 04DD04, DOI: 10.1143/JJAP.49.04DD04.

[244] Smoyer J. L., and Norris P. M. (2018), Brief historical perspective in thermal management and the shift toward management at the nanoscale, Heat Transfer Engineering, 40, 269-282, DOI: 10.1080/01457632.2018.1426265.

[245] Kong S. H., and Shim W. (2024), Advanced 2T0C DRAM technologies for processing-in-memory-part I: vertical transistor on gate (VTG) DRAM cell structure, IEEE Transactions on Electron Devices, 71, 6633-6638, DOI: 10.1109/TED.2024.3447612.

[246] Yoo T., Kim H., Chen Q., Kim T. T-H., and Kim B. (2019), A logic compatible 4T dual embedded DRAM array for in-memory computation of deep neural networks, Proceedings of ACM/IEEE International Symposium on Low Power Electronics and Design, 1-6, DOI: 10.1109/ISLPED47221.2019.