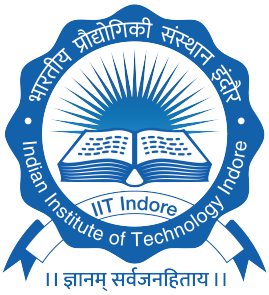
Resonant LLC Converter Based E-bike Charger

M.Tech. Thesis

by

Sumeet Raghunath Khannukar



CENTER FOR ELECTRIC VEHICLE AND

INTELLIGENT TRANSPORT SYSTEM

INDIAN INSTITUTE OF TECHNOLOGY INDORE

May 2025

Resonant LLC Converter Based E-bike Charger

A THESIS

Submitted in partial fulfillment of the

requirements for the award of the degree

of

Master of Technology

by

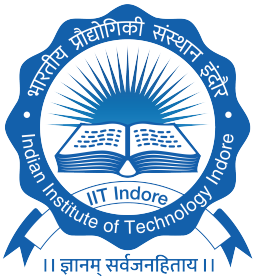
Sumeet Raghunath Khannukar

(Roll no: 2302106007)

Under the guidance of

Dr. Amod Umarikar

Dr. Vijay A. S.



CENTER FOR ELECTRIC VEHICLE AND

INTELLIGENT TRANSPORT SYSTEM

INDIAN INSTITUTE OF TECHNOLOGY INDORE

May 2025

INDIAN INSTITUTE OF TECHNOLOGY INDORE

DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **Resonant LLC Converter based E-Bike Charger** in the partial fulfillment of the requirements for the award of the degree of **Master of Technology** and submitted in the **Center for Electric Vehicle and Intelligent Transport System, Indian Institute of Technology Indore,** is an authentic record of my own work carried out during the period from June 2024 to May 2025 under the supervision of **Dr. Amod Umarikar** , Indian Institute of Technology Indore, India and **Dr. Vijay A. S.**, Indian Institute of Technology, India.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

27|05|2025

Signature of the Student with Date

(Sumeet Raghunath Khannukar)

2302106007

M. Tech. Project Approval Certificate

This is to certify that the dissertation titled **"Resonant LLC Converter Based E-bike Charger"** submitted by **Sumeet Khannukar** (Roll No: 2302106007) is approved for the award of the degree of **Master of Technology** in **Electric Vehicle Technology**.

29/05/2025

Dr. Amod Umarikar
Centre for Electric Vehicle and
Intelligent Transport Systems
Indian Institute of Technology Indore

29-05-2025

Dr. Vijay A. S.
Centre for Electric Vehicle and
Intelligent Transport Systems
Indian Institute of Technology Indore

ACKNOWLEDGEMENT

I would like to express my heartfelt gratitude to my guides, Dr. Amod Umarikar and Dr. Vijay A. S., for their constant support, guidance and encouragement throughout the course of this project. Right from the beginning, their insights and expertise helped shape the direction of the work. Whether it was researching industry standards or moving into practical aspects like hardware implementation and debugging, their suggestions gave me the clarity and confidence to move forward. They were always available to provide guidance and valuable feedback whenever I was stuck. It has truly been an honor to work under their guidance.

I am thankful to my friends and peers who supported me throughout this journey with their constant encouragement. The support and companionship made this experience both rewarding and enjoyable. I extend my heartfelt gratitude to my family for their love, patience, and faith in me.

This project has been an incredible learning experience, and I am genuinely thankful to everyone who contributed, whether directly or indirectly, to its successful completion.

ABSTRACT

This thesis presents the development of a high-efficiency electric bicycle (e-bike) charger based on a two-stage power conversion architecture. The proposed charger integrates a Boost Power Factor Correction (PFC) converter with an LLC resonant DC-DC converter to address the challenges of power quality, efficiency, and compactness in modern electric mobility solutions. With the growing adoption of e-bikes as a sustainable mode of transportation, the need for chargers that comply with international harmonic and power factor standards has become increasingly important.

The front-end PFC stage is designed to shape the input current waveform, reduce harmonic distortion, and enhance compatibility with grid infrastructure. Both continuous and critical conduction modes are explored to optimize performance under different load conditions. The second stage employs an LLC resonant converter, selected for its ability to achieve soft switching, notably Zero Voltage Switching (ZVS), thereby reducing switching losses and electromagnetic interference (EMI). A frequency modulation-based control strategy is adopted for regulating output voltage across a wide load range while maintaining efficient operation.

Comprehensive modeling and design of the resonant tank, transformer, and key passive components are carried out with consideration for thermal performance and form factor. Simulation results confirm the desired soft-switching behavior and demonstrate effective voltage regulation.

The hardware prototype of the PFC stage is successfully implemented and validated using current waveform analysis and frequency-domain THD evaluation. Although the LLC stage remains to be fully integrated in hardware, the groundwork laid through simulation and design analysis provides a reliable path forward.

This work underscores the viability of a compact, efficient, and standards-compliant e-bike charger architecture and serves as a foundation for future enhancements in digital control, full-stage integration, and real-world deployment in electric mobility ecosystems.

Contents

List of Figures

List of Tables

Acronyms

AC	Alternating Current
ADC	Analog to Digital Converter
CCM	Continuous Conduction Mode
CRM	Critical Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
EV	Electric Vehicle
FHA	First Harmonic Approximation
FFT	Fast Fourier Transform
LLC	Inductor-Inductor-Capacitor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PFC	Power Factor Correction
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RMS	Root Mean Square
SiC	Silicon Carbide
THD	Total Harmonic Distortion
TI	Texas Instruments
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1

Introduction

1.1 Background and Motivation

The increasing global emphasis on sustainable transportation has accelerated the adoption of electric bicycles (e-bikes), driven by their affordability, energy efficiency, and environmental benefits. As the demand for e-bikes grows, so does the need for efficient, compact, and reliable charging systems that align with modern energy regulations and user expectations. Traditional power converters, while functionally sufficient, fall short in meeting critical performance metrics such as high efficiency, power factor correction, harmonic reduction, and thermal management—especially under compact form-factor constraints [7].

One of the most significant challenges in designing e-bike chargers arises from the inherent characteristics of battery loads. Lithium-ion batteries, which dominate the e-bike sector, exhibit capacitive behavior that draws nonlinear, distorted current from AC sources, introducing harmonics and leading to a poor power factor [8]. This not only results in energy losses but also imposes stress on the utility grid, causing interference and voltage distortion. The problem is exacerbated when multiple chargers operate simultaneously in dense urban

charging networks.

To mitigate these issues, Power Factor Correction (PFC) has become a fundamental requirement in charger design. PFC circuits are designed to ensure that the input current waveform closely follows the input voltage waveform, thereby minimizing reactive power and lowering Total Harmonic Distortion (THD). Regulatory standards such as IEC 61000-3-2 enforce strict limits on input current harmonics for electrical equipment, including battery chargers. Failing to comply with these standards can lead to regulatory penalties, grid instability, and inefficiencies in power delivery [9].

Among the PFC techniques, the boost converter topology is widely adopted due to its simplicity, high reliability, and ability to operate over a wide input voltage range. Operating in either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM), the boost PFC stage ensures effective harmonic mitigation and improves the power factor to values exceeding 0.95. Despite its effectiveness, the PFC stage adds complexity to the system, necessitating coordinated control strategies, especially when integrated with a downstream resonant converter.

The second stage of the charger architecture typically consists of an isolated DC-DC converter, responsible for voltage regulation and galvanic isolation. LLC resonant converters are particularly well-suited for this application due to their ability to operate with soft switching (Zero Voltage Switching and Zero Current Switching), which drastically reduces switching losses, EMI, and thermal stress on the devices. This makes LLC converters ideal for high-frequency operation, allowing for the use of smaller passive components, improved power density, and better thermal performance.

The motivation for this project lies at the intersection of several key challenges: designing a

charger that is compact yet powerful, compliant with international power quality standards, efficient under varying load conditions, and thermally robust for long-term reliability. By integrating a boost PFC front-end with a high-frequency LLC resonant DC-DC stage, this work aims to develop a practical, standards-compliant charger tailored for e-bikes.

The proposed architecture also supports zero-voltage switching (ZVS) across a wide operating range, which further enhances energy efficiency and component longevity. Control strategies for soft switching and harmonic minimization are implemented to ensure optimal performance under both steady-state and dynamic conditions.

This comprehensive approach not only addresses current technical limitations but also anticipates future trends in electric mobility and grid-connected devices, establishing a robust foundation for scalable and sustainable e-bike charger development.

1.2 Overall Objectives

The overarching goal of this thesis is to design and implement a 120 W e-bike charger that combines power quality, efficiency, and portability by utilizing a two-stage architecture: a front-end Power Factor Correction (PFC) boost converter followed by an LLC resonant DC-DC converter.

The PFC stage is incorporated to ensure that the charger draws nearly sinusoidal current from the AC mains with a high power factor, thereby reducing total harmonic distortion (THD) and complying with international standards (e.g., IEC 61000-3-2). This not only improves grid compatibility but also enhances overall system efficiency.

The LLC stage, optimized for Zero Voltage Switching (ZVS), enables low-loss conversion across a wide output voltage range while reducing EMI.

The project involves complete system modeling, control strategy development for soft switching, PCB-level implementation, and experimental validation. Special emphasis is placed on ensuring harmonic mitigation, efficient power utilization, and safe operation across varying load conditions. The final outcome aims to deliver a compact, standards-compliant e-bike charger suited to modern electric mobility demands.

1.3 Thesis Outline

This thesis is organized into seven chapters. The introduction outlines the motivation, objectives, and challenges in e-bike charger design. The literature survey reviews electric bicycle systems and charger architectures, emphasizing DC-DC topologies. The third chapter discusses Power Factor Correction, including boost-based methods and harmonic standards. Chapter 4 details LLC resonant converter operation, modeling, and control strategies. Chapter 5 focuses on design methodology, component selection, and hardware aspects. Chapter 6 presents simulation and experimental results, including waveform analysis and THD reduction. Finally, the conclusion summarizes the findings and outlines future work, including LLC hardware implementation and digital control integration for a complete, standards-compliant charger.

Chapter 2

Literature Survey

2.1 Overview of Electric Bicycle Ecosystems

Electric bicycles (e-bikes) have gained remarkable traction as a sustainable alternative to traditional transportation. The growing urban congestion, rising fuel prices, and environmental concerns have pushed both consumers and manufacturers toward e-mobility. At the core of e-bike performance lies the power electronics interface—specifically the battery charging system—which must be efficient, reliable, and grid-compliant. The charging infrastructure must accommodate varying grid conditions, ensure battery longevity, and adhere to harmonic and power factor standards [7]. The power supply chain in an e-bike charger typically involves an AC-DC front-end for rectification and power factor correction, followed by a high-frequency isolated DC-DC stage for voltage regulation and galvanic isolation.

2.2 Architecture of a Typical E-bike Charger

A standard electric bicycle (e-bike) charger architecture typically consists of two major stages—namely, the Power Factor Correction (PFC) stage and the isolated DC-DC conver-

sion stage. This two-stage approach is designed to meet regulatory requirements for power quality, ensure safe and efficient battery charging, and minimize electromagnetic interference (EMI).

As illustrated in Fig. 2.1, the charger architecture begins with a **230 V AC grid supply**, which is initially passed through an **EMI filter**. This filter suppresses high-frequency noise generated by switching devices in the charger, preventing it from propagating back into the grid.

The **PFC converter**, forming the core of Stage-I, serves the dual purpose of rectifying the AC input and shaping the input current to be sinusoidal and in phase with the input voltage. This not only enhances the power factor but also reduces the total harmonic distortion (THD), enabling compliance with standards. The output of the PFC stage is a regulated high-voltage DC signal, which acts as the input to the next stage.

Stage-II begins with a **high-frequency inverter**, which converts the DC output of the PFC stage into a high-frequency AC waveform. This AC signal is passed through a **high-frequency transformer**, which provides galvanic isolation between the input and output sides while stepping down the voltage. The **rectifier** then converts the transformer output back into DC, followed by a **DC filter** that smoothens the voltage to meet battery charging specifications.

The final output is a well-regulated DC voltage—typically 48V in the context of e-bike batteries—suitable for charging a **Li-ion battery** pack. Each stage in this architecture is carefully optimized to ensure compactness, high efficiency, and reliable performance under a wide range of operating conditions [10].

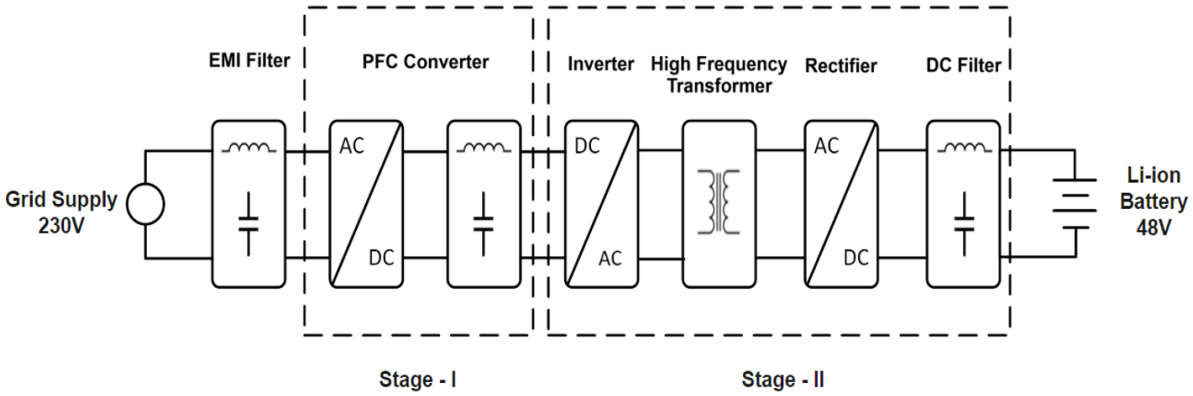


Figure 2.1: Typical architecture of an electric bicycle charger.

This architecture not only supports compliance with grid-interface standards but also ensures safe, efficient, and fast charging of e-bike batteries, aligning with the rising demands of electric mobility solutions.

2.3 DC-DC Converter Topologies for Charger Applications

DC-DC converters serve as the backbone of regulated power delivery in charger systems. These converters fall under three broad categories: linear regulators, hard-switching converters, and resonant (soft-switching) converters.

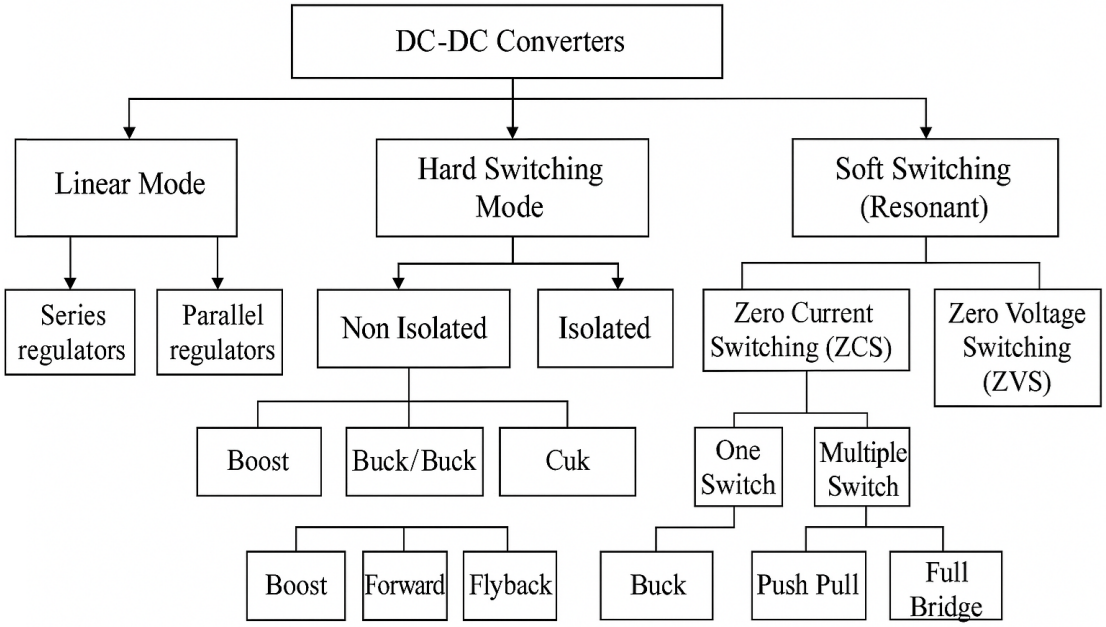


Figure 2.2: Classification of DC-DC converters.

2.3.1 Linear Regulators

Although simple and cost-effective, linear regulators suffer from significant power loss and are unsuitable for medium- or high-power applications due to their low efficiency. They are now largely confined to low-current auxiliary rails in charger systems.

2.3.2 Hard Switching Converters

Hard switching topologies like the *buck*, *boost*, and *flyback* converters are widely used in moderate power applications. However, their inherent switching losses and EMI issues make them less suitable for high-frequency operation and compact form factors. Among hard-switching isolated topologies, flyback and forward converters are often employed for low-power chargers but struggle with efficiency at higher power levels.

2.3.3 Resonant (Soft-Switching) Converters

Soft-switching topologies such as the LLC resonant converter address many of the drawbacks of hard-switching designs. By operating in either **Zero Voltage Switching (ZVS)** or **Zero Current Switching (ZCS)** modes, they minimize switching losses and EMI [11]. The LLC topology is especially attractive for high-frequency, high-efficiency isolated DC-DC conversion due to:

- Reduced switching stress on semiconductors
- High power density
- Natural voltage regulation capability through frequency modulation

2.4 Discussion

This chapter provides an overview of electric bicycle systems, emphasizing the critical role of efficient and grid-compliant chargers. It outlines a standard e-bike charger architecture composed of a PFC stage followed by an isolated DC-DC converter. Various DC-DC topologies are compared—linear regulators, hard switching, and resonant converters. The LLC resonant converter is identified as the most suitable for its high efficiency, soft switching, and ability to support compact designs, making it ideal for modern e-bike applications.

Chapter 3

Power Factor Correction

3.1 Definition of Power Factor

Power Factor (PF) is a crucial metric in evaluating the efficiency and quality of electrical power systems, particularly in applications involving power electronics and converter-based technologies such as electric vehicle (EV) and e-bike chargers. It measures the proportion of electrical power that is effectively converted into useful work, compared to the total power supplied from the source [12]. Mathematically, power factor is expressed as the ratio of real power (P) to apparent power (S):

$$PF = \frac{P}{S}$$

For sinusoidal waveforms, this relationship can be expanded as:

$$PF = \frac{V_1 \cdot I_1 \cdot \cos(\phi_1)}{V \cdot I}$$

Where:

- V_1 and I_1 are the RMS values of the fundamental components of voltage and current,
- ϕ_1 is the phase angle between them,
- V and I are the total RMS values of voltage and current, including harmonics.

In ideal linear systems with resistive loads, voltage and current waveforms are perfectly sinusoidal and in phase, yielding a unity power factor ($PF = 1$). However, in practical applications—particularly those utilizing switching power converters—the current waveform often deviates from a pure sinusoid due to nonlinearities, thus reducing the power factor.

This distortion can be evaluated through the **Total Harmonic Distortion (THD)** of the current [13]. In the presence of harmonics, only the fundamental portion of the current contributes to real power transfer. This leads to the concept of the *distortion power factor*, defined as:

$$\frac{I_1}{I} = \frac{1}{\sqrt{1 + (THD)^2}}$$

Therefore, the overall or *true power factor* can be written as:

$$PF = \frac{1}{\sqrt{1 + (THD)^2}} \cdot \cos(\phi_1)$$

This equation demonstrates that the power factor is degraded both by phase displacement and by current waveform distortion. In systems without proper power factor correction mechanisms, the effective power usage is significantly compromised, leading to suboptimal

energy efficiency and potential instability in power grid operations.

3.2 Need for Power Factor Correction

The goal of Power Factor Correction (PFC) is to reduce reactive power and improve real power usage. Without PFC, offline power supplies draw distorted currents, leading to high harmonic distortion, poor power factor, and grid interference. Regulatory standards like IEC 61000-3-2 limit harmonics for devices over 75 W, preserving system integrity. PFC lowers I^2R losses, eases transformer stress, and reduces capacitor sizing. It also enhances EMI performance, system reliability, and energy efficiency [13].

3.3 Harmonic Emission Standards

Harmonic emissions are unwanted frequencies from nonlinear loads and switching in power converters that degrade power quality and cause equipment issues. To address this, the IEC enforces standards like IEC 61000-3-2 for devices with $\leq$16 A input per phase, limiting harmonics up to the 39th order. For higher currents, IEC 61000-3-12 applies similar restrictions [9].

- **Harmonics range** (up to $\sim$2 kHz): Targeted toward grid compatibility.
- **Low-frequency EMI** (2–9 kHz): Currently undergoing evaluation.
- **Conducted EMI** (9 kHz–30 MHz): Regulated by CISPR 11, 12, 14, 15.
- **Radiated EMI** (30 MHz–3 GHz): Governed by radiated emission standards.

Compliance with these standards is essential to prevent equipment from introducing undue disturbances to the electrical grid. Employing effective Power Factor Correction (PFC)

techniques plays a vital role in reducing these emissions, thereby supporting system stability, enhancing electromagnetic compatibility (EMC), and aligning with regulatory requirements.

3.4 Full Bridge Rectifier Harmonics

Full bridge rectifiers with large DC-side capacitors cause significant harmonic distortion by producing non-sinusoidal input currents. Conduction occurs only at AC voltage peaks, generating short, high-amplitude pulses that increase harmonic content.

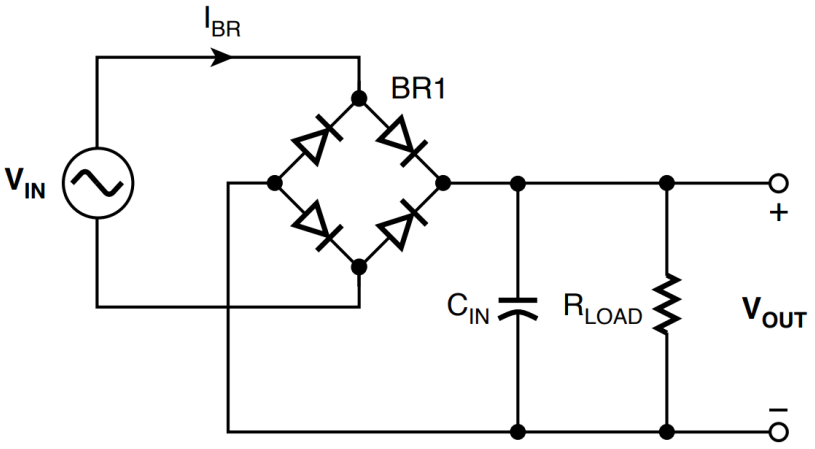


Figure 3.1: Full Bridge Rectifier

Low-frequency harmonics from pulsed currents degrade power quality, increase transformer losses, and may violate IEC standards. They can cause overheating, line losses, and system instability. These effects are critical in high-density applications like e-bike chargers. Peak currents also lead to poor power factor and elevated I^2R losses. To mitigate these issues, active PFC is used after the rectifier to shape input current sinusoidally, improving power factor, reducing harmonics, and enhancing system efficiency. Active PFC ensures regulatory

compliance and supports reliable, efficient power conversion [1].

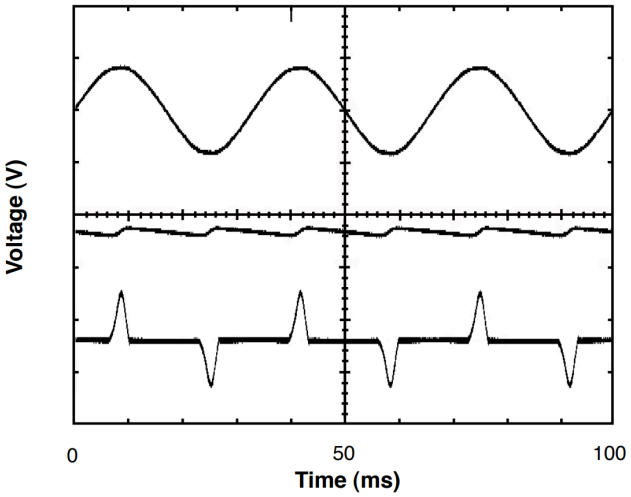


Figure 3.2: Full Bridge Rectifier Stage Waveforms. Top: Input Voltage. Middle: Output Voltage. Bottom: Input Current. [1]

3.5 Types of Power Factor Correction (PFC)

PFC strategies can be broadly classified into two categories: **Passive** and **Active** methods.

Passive PFC approach utilize passive components such as inductors and capacitors to mitigate harmonics and improve the overall power factor. These systems are inherently simple, robust, and cost-effective. However, they tend to be bulky and inefficient over wide input voltage ranges. Passive PFC techniques are less adaptive to variations in load and supply conditions and are therefore generally suited for low-power applications with relatively stable operating environments.

Active PFC, in contrast, leverages power electronic converters combined with sophisticated control algorithms to dynamically shape the input current. These systems commonly employ topologies like boost, buck, or buck-boost converters. Active PFC circuits regulate the input current to track the voltage waveform closely, often achieving power factors ap-

proaching unity. Compared to passive techniques, active PFC offers superior efficiency, better harmonic attenuation, and adaptability across a broad input voltage range.

Among the various active configurations, the **boost PFC** topology is the most widely adopted. It is especially favored in applications requiring a well-regulated high-voltage DC output and minimal current distortion at the input. The widespread use of boost PFC is driven by its compatibility with stringent regulatory requirements and its effectiveness in supporting compact, high-efficiency power conversion systems.

3.6 Boost Power Factor Correction

The Boost-type Power Factor Correction (PFC) converter is one of the most prevalent topologies employed in active PFC implementations due to its high efficiency, simplicity, and capability to deliver a regulated output voltage greater than the input. The typical configuration consists of a diode bridge rectifier at the input, followed by a high-frequency controlled boost converter [14]. This boost stage typically comprises an inductor, a switch (commonly a MOSFET), a diode, and an output capacitor.

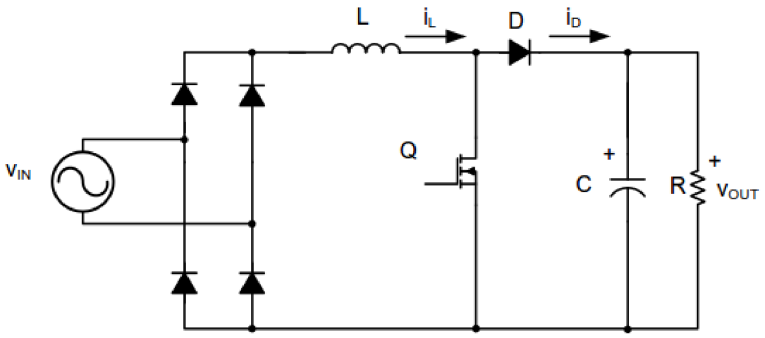


Figure 3.3: Boost Power Factor Correction Circuit

A notable advantage of the boost PFC topology lies in its ability to draw a continuous current from the AC source. This continuous input current profile minimizes input current harmon-

ics and simplifies the design of the Electromagnetic Interference (EMI) filter. Moreover, the boost converter modulates the input current to closely follow the shape of the input voltage waveform, enabling near-unity power factor operation. The strategic placement of the inductor at the input stage also plays a crucial role in smoothing the current and attenuating the Total Harmonic Distortion (THD) [15].

This configuration is particularly suitable for medium to high-power applications. When operated in Continuous Conduction Mode (CCM), it further reduces peak current stress on the switching devices, leading to improved thermal performance and overall system reliability. However, precise digital or analog control strategies are necessary to ensure stable performance under varying load and line conditions. Advanced controllers are employed to dynamically adjust the duty cycle of the switch, thereby ensuring sinusoidal input current waveforms and compliance with international grid standards.

3.7 Conduction Modes: CCM, DCM, BCM

The operation of a boost Power Factor Correction (PFC) converter is heavily influenced by the conduction mode of the inductor current. The three principal conduction modes are [2]:

Continuous Conduction Mode (CCM)

In CCM, the inductor current never falls to zero during the switching cycle. This results in lower peak current levels, reduced electromagnetic interference (EMI), and enhanced efficiency due to reduced RMS current levels. However, CCM requires a larger inductor and encounters switching losses as it operates with hard switching. To mitigate these losses, modern CCM designs employ advanced devices such as SiC Schottky diodes and high-performance MOSFETs.

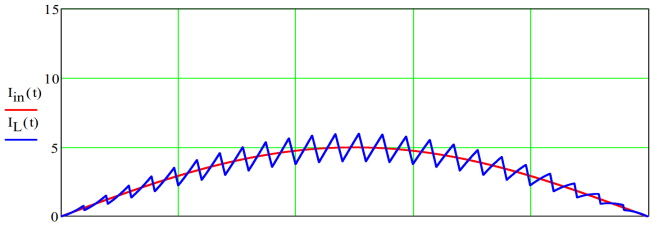


Figure 3.4: Continuous Conduction Mode [2]

Discontinuous Conduction Mode (DCM)

In DCM, the inductor current drops to zero before the commencement of the next switching cycle. This mode allows for the use of smaller inductors and facilitates soft switching, which reduces turn-on losses. However, DCM incurs higher peak and RMS currents, leading to increased conduction losses and EMI, making it less suitable for high-power designs.

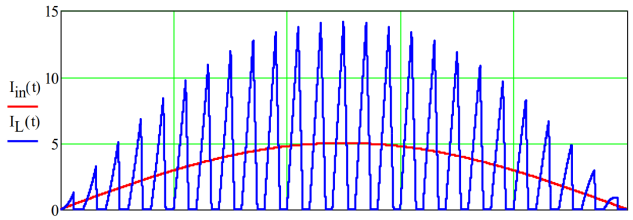


Figure 3.5: Discontinuous Conduction Mode [2]

Boundary Conduction Mode (BCM)

Also referred to as Critical Conduction Mode (CrCM), BCM operates at the boundary between CCM and DCM. The inductor current reaches zero at the end of each switching cycle, enabling soft switching and reduced switching losses. Nevertheless, the switching frequency in BCM varies with input voltage and load, complicating both EMI filter and controller design. BCM is generally more applicable for low-to-medium power levels unless interleaved operation is used to suppress ripple and maintain performance.

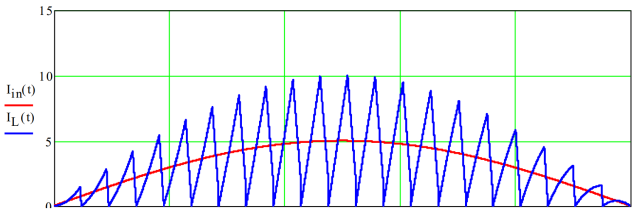


Figure 3.6: Boundary Conduction Mode [2]

Each conduction mode presents its own set of trade-offs involving efficiency, size, control complexity, and EMI characteristics. For high-power applications such as e-bike chargers, **CCM** is often the preferred choice. This is due to its superior handling of power levels and simplified filter requirements, despite the penalty of increased switching losses [2].

3.8 Discussion

Chapter 3 details the importance of maintaining high power factor and minimizing harmonic distortion in grid-connected chargers. It explains power factor basics, its relation to THD, and why standards like IEC 61000-3-2 mandate PFC in chargers exceeding 75W. The contrast between passive and active PFC methodologies is systematically explored, with the Boost PFC topology identified as the most scalable and efficient approach. Furthermore, detailed attention is given to conduction mode selection (CCM, DCM, BCM), evaluating their implications on ripple, EMI, and efficiency in PFC design.

Chapter 4

LLC Resonant Converter

In recent decades, LLC resonant converters have gained significant traction in modern power electronics, finding applications across distributed power systems, renewable energy infrastructures, and consumer electronics. Earlier resonant topologies such as the Series Resonant Converter (SRC) and Parallel Resonant Converter (PRC) often suffered from substantial power losses in their resonant tanks, limiting their efficiency and adaptability. To address these limitations, researchers in the 1990s introduced advanced multi-resonant topologies, notably the LCC and LLC resonant converters. Among these, the LLC topology has been particularly valued for its ability to maintain operational stability across a wide range of input voltages and load conditions [16].

A critical advantage of the LLC converter lies in its capacity for Zero Voltage Switching (ZVS), which significantly reduces switching losses during conduction. This feature not only improves thermal efficiency but also extends the lifespan of power semiconductor devices [17]. Compared to traditional phase-shifted full-bridge converters, which are prevalent in utility-grade systems, the LLC topology demonstrates superior efficiency—largely due to its inherent mitigation of reverse recovery losses in output diodes. Owing to these merits,

LLC resonant converters are increasingly deployed in grid-tied and distributed energy systems, where both high efficiency and robust dynamic response are essential for maintaining grid stability and power quality.

4.1 Principles of Operation

Fig. 4.1 depicts the configuration of a half-bridge LLC resonant converter, which includes critical parameters such as the resonant frequency f_0, quality factor Q, and the inductance ratio L_n, representing the relationship between the magnetizing inductance L_m and the resonant inductance L_r. As shown in Fig. 4.2, the voltage gain varies depending on load conditions. In this topology, voltage gain is described by the ratio $nV_o/(V_{in}/2)$, where n is the transformer turns ratio. The normalized switching frequency is defined as $f_n = f_s/f_0$, where f_s is the switching frequency [18, 19].

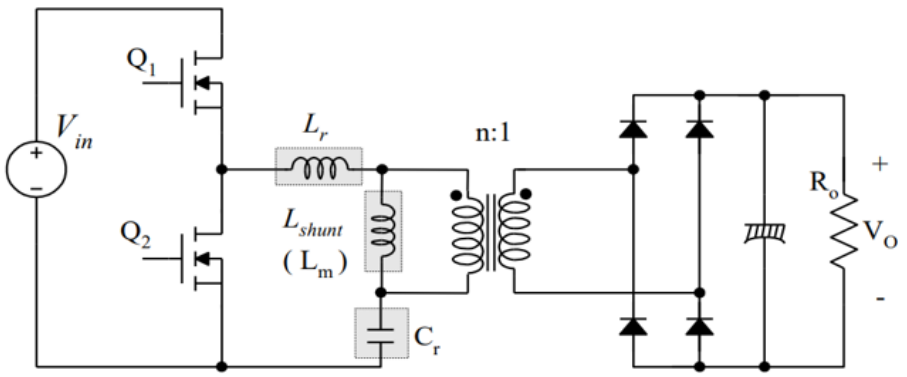


Figure 4.1: LLC resonant converter topology

At the resonant frequency, the converter exhibits a gain of unity regardless of load variations. When $f_s > f_0$, the gain drops below 1, enabling Zero Voltage Switching (ZVS) for the primary switches. Conversely, when $f_s < f_0$, the converter can potentially operate in Zero Current Switching (ZCS) mode. For most practical applications using MOSFETs, ZVS

is preferred to reduce switching losses. Notably, the gain increases above unity when the system operates in the capacitive region where $f_s < f_0$.

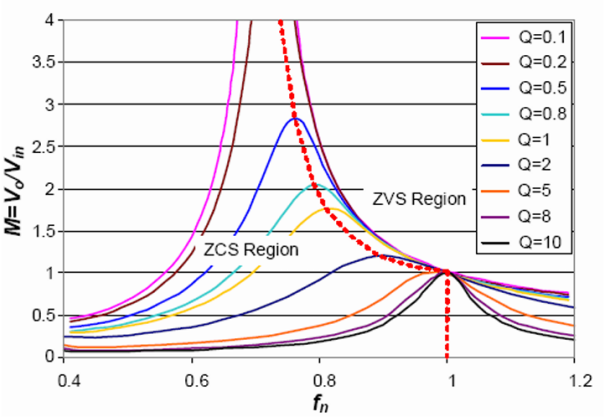


Figure 4.2: Voltage gain characteristics of LLC resonant converter [3]

Fig. 4.2 also illustrates the variation of gain with normalized frequency and different quality factors Q, demarcating the regions for ZVS and ZCS operations.

Several modes of ZVS are attainable based on the relationship between the switching frequency and the resonant frequency. Fig. 4.3 shows the waveform behavior at the resonant condition.

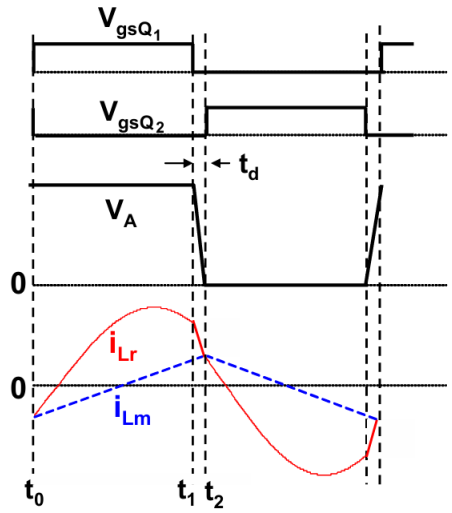


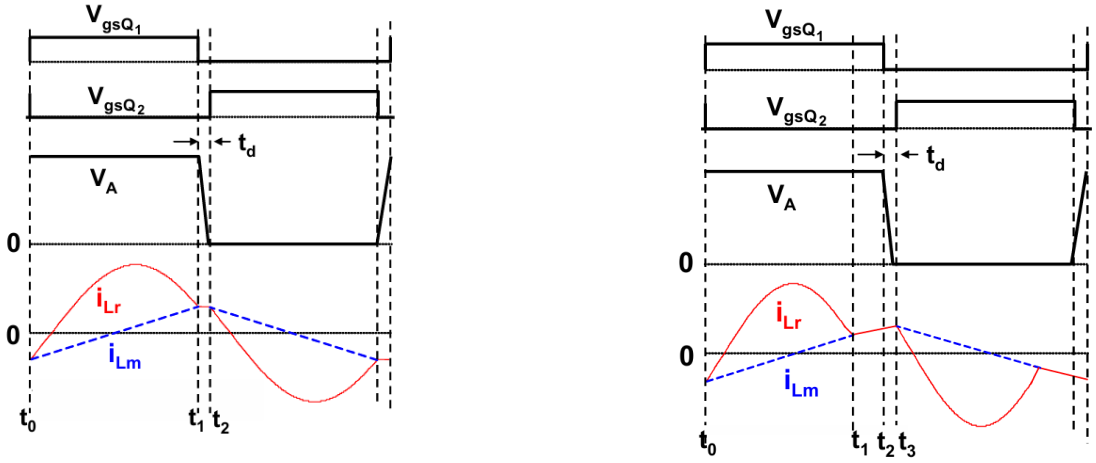
Figure 4.3: Waveforms with $f_s = f_0$ [4]

During the interval between t_0 and t_1, the primary switch Q_1 conducts, and the diode D_2 on the secondary side is forward-biased, conducting according to the polarity across the transformer. Energy is transferred from the primary side to the output. The magnetizing current i_{Lm} increases linearly due to the reflected voltage. When the resonant current i_{Lr} aligns with the magnetizing current, Q_1 turns off at t_1.

In the dead-time between t_1 and t_2, both switches are off. During this interval, the magnetizing current discharges the output capacitance of the switches, enabling ZVS turn-on for Q_2 at time t_2. The complementary half-cycle then begins.

When operating at $f_s = f_0$, the resonant tank current aligns with the peak magnetizing current precisely at the instant the switch turns off. This ensures ideal ZVS performance for the primary switches.

The converter's operation under $f_s < f_0$ and $f_s > f_0$ is shown in Figures 4.4a and 4.4b, respectively. In the $f_s < f_0$ condition, energy transfer occurs early in the switching cycle, i.e., during t_0 to t_1, with resonance continuing between t_1 and t_2. Here, both L_m and L_r resonate with the capacitor C_r, and the peak magnetizing current dictates the ZVS condition.



(a) $f_s < f_0$ (b) $f_s > f_0$

Figure 4.4: Operation waveforms of LLC resonant converter [4]

In the $f_s > f_0$ scenario, the resonant current does not reach the magnetizing current level before turn-off, resulting in a higher switch turn-off current. This can lead to increased switching losses and diminished efficiency. The discrepancy between tank and magnetizing current at turn-off depends on the load and the deviation of f_s from f_0.

Additionally, the di/dt experienced by the output diodes increases in this mode, potentially inducing greater reverse recovery stress and voltage overshoots. Hence, operating above the resonant frequency is generally avoided unless necessary.

When LLC resonant converters are implemented as DC/DC converters in the front-end of power systems, they are typically designed to operate at resonance under normal conditions. This approach ensures optimal efficiency, while variations in output voltage during low-line conditions or hold-up time are managed by reducing the switching frequency.

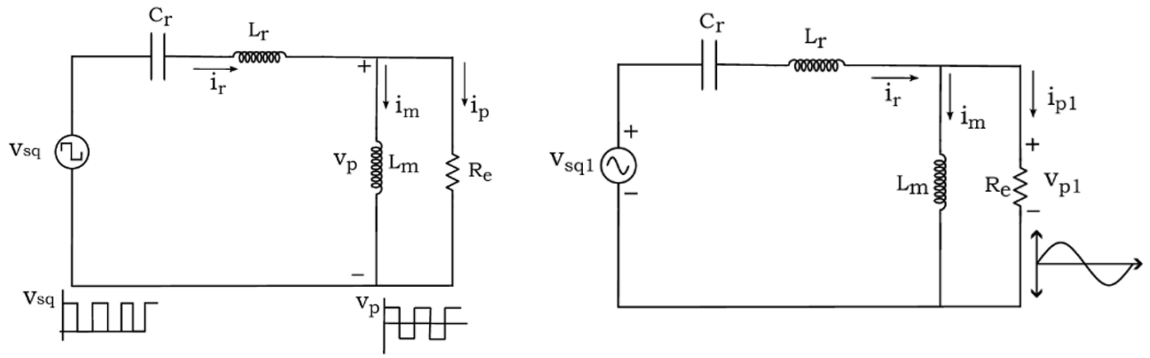
4.2 Modeling of LLC Half-Bridge Converter

4.2.1 First Harmonic Approximation

The First Harmonic Approximation (FHA) is a common method for analyzing LLC resonant converters near their series resonant frequency. It simplifies modeling by considering only the fundamental components of voltage and current, neglecting higher-order harmonics. FHA treats the square wave inverter output and resonant tank current as sinusoids, enabling closed-form expressions for gain and impedance. The equivalent circuit ignores output capacitance and transformer secondary leakage, with all secondary parameters reflected to the primary side for simplified analysis [20].

The equivalent circuit derived using FHA, as illustrated in Fig. 4.5, excludes the effect of output capacitance and ignores the leakage inductance of the transformer's secondary wind-

ing. Additionally, all secondary-side parameters are reflected to the primary side for ease of analysis. The resulting FHA-based circuit model serves as a single-frequency approximation that provides analytical clarity without significantly compromising accuracy [21].



(a) Equivalent circuit without FHA (b) Equivalent circuit with FHA

Figure 4.5: Model of LLC Resonant Half-bridge Converter

4.2.2 Parameter Estimation in the FHA Circuit Model

The fundamental component of the input square wave voltage $v_{sq_1}(t)$ is given by:

$$v_{sq_1}(t) = \frac{2V_{DC}}{\pi} \sin(2\pi f_s t) \tag{4.1}$$

where V_{DC} is the DC link voltage.

Its RMS value is:

$$V_{sq_1} = \frac{2\sqrt{2}V_{DC}}{\pi} \tag{4.2}$$

The fundamental voltage on the secondary side referred to the primary is:

$$v_{p1}(t) = \frac{4V_o}{\pi} \cdot \frac{N_1}{N_2} \sin(2\pi f_s t - \phi_v) \tag{4.3}$$

The RMS value:

$$V_{p1} = \frac{2\sqrt{2}V_o}{\pi} \cdot \frac{N_1}{N_2} \tag{4.4}$$

The average load current:

$$I_o = \frac{2I_{s1,m}}{\pi} \tag{4.5}$$

The current $i_{p1}(t)$ is:

$$i_{p1}(t) = \frac{\pi}{2} \cdot \frac{N_2}{N_1} I_o \sin(2\pi f_s t - \phi_i) \tag{4.6}$$

Since $\phi_i = \phi_v$, the RMS value:

$$I_{p1} = \frac{\pi}{2\sqrt{2}} \cdot \frac{N_2}{N_1} I_o \tag{4.7}$$

The reflected AC load resistance R_e is:

$$R_e = \frac{8}{\pi^2} \left(\frac{N_1}{N_2}\right)^2 R_L \tag{4.8}$$

Angular switching frequency:

$$\omega_s = 2\pi f_s \tag{4.9}$$

Impedances:

$$X_{Cr} = \frac{1}{\omega_s C_r}, \quad X_{L_r} = \omega_s L_r, \quad X_{L_m} = \omega_s L_m \tag{4.10}$$

- X_{C_r}: Reactance of the resonant capacitor
- X_{L_r}: Reactance of the resonant inductor
- X_{L_m}: Reactance of the magnetizing inductor
- ω_s: Switching angular frequency (rad/s), i.e., $\omega_s = 2\pi f_s$

- C_r: Resonant capacitor value
- L_r: Resonant inductor value
- L_m: Magnetizing inductor value

Magnetizing current RMS:

$$I_m = \frac{2\sqrt{2}}{\pi} \cdot \frac{N_1}{N_2} \cdot \frac{V_o}{\omega_s L_m} \tag{4.11}$$

Resonant current:

$$I_r = \sqrt{I_m^2 + I_{p1}^2} \tag{4.12}$$

4.2.3 Voltage Gain Function

DC voltage gain:

$$M_{g,DC} = \frac{N_1}{N_2} \cdot \frac{V_o}{V_{sq}/2} \tag{4.13}$$

AC voltage gain:

$$M_{g,AC} = \frac{V_p}{V_{sq}} = \frac{V_{p1}}{V_{sq_1}} \tag{4.14}$$

Substituting:

$$M_{g,DC} = \frac{\pi}{2\sqrt{2}} \cdot \frac{V_{p1}}{V_{sq_1}} \tag{4.15}$$

Voltage division:

$$\frac{V_{p1}}{V_{sq_1}} = \frac{jX_{L_m} \parallel R_e}{(jX_{L_m} \parallel R_e) + j(X_{L_r} - X_{Cr})} \tag{4.16}$$

Gain:

$$M_g = \frac{(j\omega_s L_m) \parallel R_e}{(j\omega_s L_m) \parallel R_e + j\omega_s L_r + \frac{1}{j\omega_s C_r}} \tag{4.17}$$

Simplified:

$$M_g = \frac{-L_m C_r \omega_s^2}{1 - L_r C_r \left[1 + \frac{L_m}{L_r}\right] \omega_s^2 + j \left[\frac{L_m \omega_s}{R_e} - \frac{L_r L_m C_r \omega_s^3}{R_e}\right]} \tag{4.18}$$

Normalized values:

$$L_n = \frac{L_m}{L_r}, \quad f_n = \frac{f_s}{f_r}, \quad Q_e = \frac{1}{R_e}\sqrt{\frac{L_r}{C_r}} \tag{4.19}$$

Gain in normalized form:

$$M_g = \frac{L_n f_n^2}{[(L_n + 1)f_n^2 - 1] + j[(f_n^2 - 1) f_n Q_e L_n]} \tag{4.20}$$

Magnitude:

$$M_g = \frac{L_n f_n^2}{\sqrt{[(L_n + 1)f_n^2 - 1]^2 + [(f_n^2 - 1) f_n Q_e L_n]^2}} \tag{4.21}$$

Final voltage relation:

$$V_o = M_g(f_n, L_n, Q_e) \cdot \frac{N_2}{N_1} \cdot \frac{V_{DC}}{2} \tag{4.22}$$

4.3 Soft Switching in LLC Resonant Converters

In power electronic systems, switching transitions affect efficiency and thermal performance. **Hard switching** involves turning devices on or off with non-zero voltage and current, leading to high losses, EMI, and device stress. *Soft switching* methods like Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) minimize these effects by ensuring transitions occur at low voltage/current levels. In **LLC resonant converters**, soft switching is naturally supported by the resonant tank. ZVS is commonly implemented on the primary switches, where the magnetizing current and tank impedance discharge the MOSFET's output capacitance before turn-on. This enables low-loss switching, reduced

EMI, and better thermal behavior—especially at high frequencies. Due to their symmetrical waveforms, LLC converters can maintain ZVS across a wide load range without complex controls [22, 23].

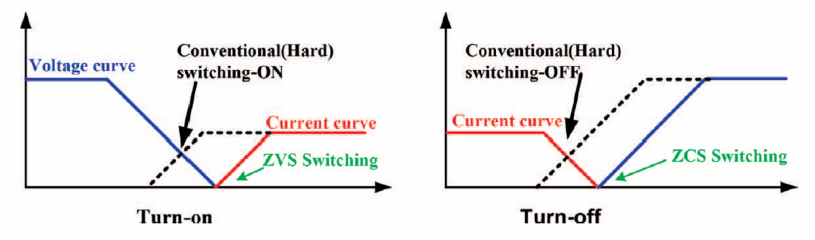


Figure 4.6: Current and voltage waveforms of hard-switching and soft-switching scenarios [5]

4.3.1 Ensuring Zero Voltage Switching

To achieve Zero Voltage Switching (ZVS) in an LLC resonant converter, the energy in the resonant inductors must be sufficient to discharge the parasitic capacitances of the power switches before switching. This is expressed as:

$$\frac{1}{2}(L_M + L_r)I_{m,peak}^2 \geq \frac{1}{2}(2C_{eq})V_{in}^2 \tag{4.23}$$

Here, $I_{m,peak}$ is the magnetizing current, $C_{eq} \approx 2C_{ds}$, and V_{in} is the input voltage. The dead-time t_{dead} must be long enough for the voltage to fall to near zero:

$$t_{dead} \geq 8C_{eq}f_{sw}L_M \tag{4.24}$$

To preserve soft-switching, the resonant capacitor must satisfy:

$$C_r > C_{eq} \tag{4.25}$$

Failure to meet these conditions may lead to Zero Current Switching (ZCS), which, while lossless at turn-off, increases EMI and turn-on losses due to reverse recovery. High di/dt during these transitions stresses devices and lowers efficiency. Reliable ZVS is crucial in high-performance LLC designs [24].

4.4 Operating Regions of the LLC Resonant Converter

The switching mode in an LLC converter—ZVS or ZCS—depends on the input impedance of the resonant tank. When the impedance is inductive, the input current lags the voltage, causing parasitic body diodes to conduct before switch turn-on. This ensures nearly zero voltage across the switch, enabling ZVS. Conversely, if the impedance is capacitive, the current leads the voltage, causing the opposite body diode to conduct. This results in hard switching at turn-on and ZCS at turn-off [25].

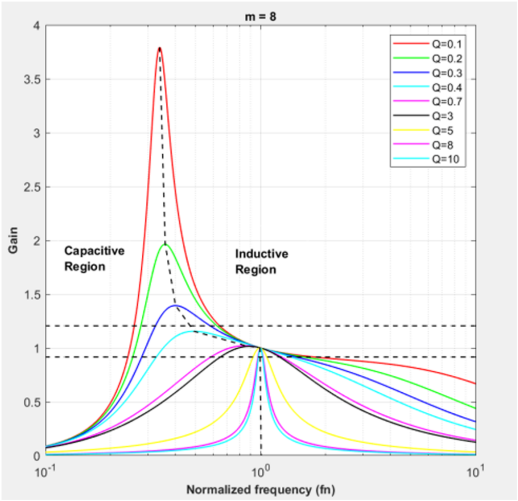


Figure 4.7: Voltage gain (Gain) with respect to normalized frequency (f_n) [3]

The impedance profile in an LLC converter becomes fixed once the design and load are set, meaning it cannot freely switch between ZVS and ZCS. Its operation is governed by the input impedance's imaginary part. A positive imaginary component indicates inductive behavior, enabling ZVS. This is described by the expression for the tank's input impedance:

$$\text{Im}\left(\bar{Z}_{\text{in}}(j\omega_s)\right) = \omega_s L_r - \frac{1}{\omega_s C_r} + \frac{64N^4 R_L^2 L_m \omega_s}{\pi^4 \omega_s^2 L_m^2 + 64N^4 R_L^2} \tag{4.26}$$

As the load resistance increases, the zero-crossing point of the imaginary impedance shifts, ultimately defining the threshold angular frequency ($\omega_s = \omega_r$) at which the transition between capacitive and inductive behavior occurs. A DC characteristic curve of the LLC converter is conventionally divided into three regions based on this behavior (see Fig. 4.7).

- **Region 1 (ZCS)**: Characterized by capacitive impedance, where the input current leads the voltage. This region is generally not preferred, especially when using MOSFETs, due to the absence of ZVS, resulting in increased losses and EMI.

- **Region 2 (ZVS)**: Defined by inductive impedance. This region is further sub-divided into Region 2.1 (where $\omega_1 < \omega_s < \omega_r$) and Region 2.2 (where $\omega_s > \omega_r$). In both zones, ZVS is possible, making them ideal for MOSFET-based LLC topologies.

LLC converters, using MOSFETs in high-frequency designs, are optimized to operate in Region 2 (inductive region) where ZVS is achievable. Operating in the capacitive region must be avoided due to hard switching losses. At full load, ZVS is more reliable as the reflected load dominates. However, at light loads, the magnetizing inductance limits ZVS performance. For efficiency, the converter should be designed to operate near the resonant frequency—sub-resonant for low voltage and super-resonant for high voltage—while avoiding the capacitive region [26].

4.5 Dead-Time Optimization

Achieving optimal performance in LLC resonant converters necessitates a careful balance between maintaining high efficiency and ensuring adequate voltage regulation during hold-up intervals. A critical factor influencing this performance is the appropriate selection of dead-time (t_d). To attain Zero Voltage Switching (ZVS), the magnetizing inductance L_m must be tuned precisely. This is guided by the expression [27]:

$$L_m = \frac{T_s \cdot t_d}{16 C_j} \tag{4.27}$$

where T_s is the switching period, and C_j denotes the equivalent junction capacitance of the MOSFET. While this formula prescribes an optimal L_m for a given t_d, the reverse—determining t_d for a chosen L_m—requires further insight.

Increasing the dead-time permits the use of a higher L_m without compromising ZVS, thereby reducing the magnetizing current i_{Lm} and consequently minimizing turn-off losses. However, longer dead-times also reduce the effective duty cycle for energy transfer, potentially increasing the conduction loss due to a larger difference between i_{Lr} and i_{Lm}.

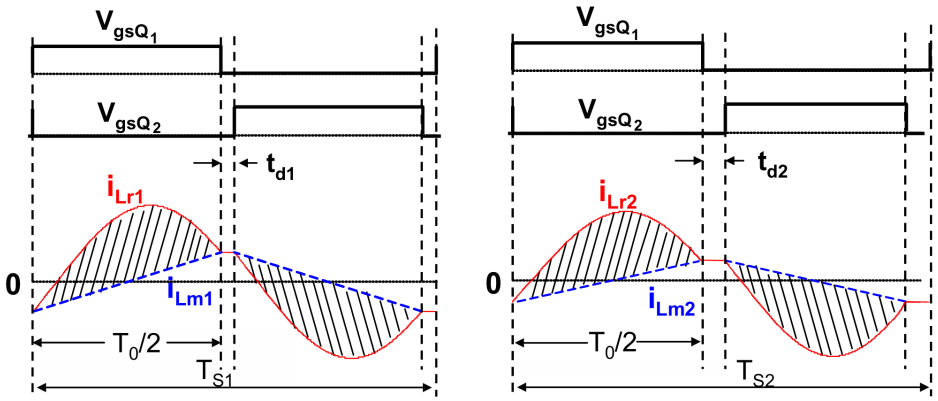


Figure 4.8: Operation waveforms with different dead-time t_d ($t_{d1} < t_{d2}$) [6]

Fig. 4.8 illustrates two operational cases with different dead-times. As t_d increases, T_s becomes $T_0 + 2t_d$, effectively stretching the switching cycle. A longer T_s necessitates an elevated $i_{Lr} - i_{Lm}$ to maintain consistent power delivery, which complicates loss optimization.

Conversely, reducing the dead-time increases the peak magnetizing current I_{Lm}, which heightens switching losses [28]. Hence, identifying the dead-time that minimizes both switching and conduction losses is vital.

To satisfy the ZVS criterion, the peak magnetizing current must fulfill:

$$I_{Lmp} > \frac{2V_{in}C_j}{t_d} \tag{4.28}$$

Assuming the current remains constant during the dead-time interval, the peak current is approximated by:

$$I_{Lmp} = \frac{nV_oT_0}{4L_m} \tag{4.29}$$

where n is the transformer turns ratio and T_0 is the resonant half-cycle. Rearranging for L_m gives:

$$L_m \leq \frac{T_0 \cdot t_d}{16C_j} \tag{4.30}$$

Therefore, minimizing conduction losses favors a larger L_m, while ZVS constraints limit how large it can be. The optimal L_m aligns with:

$$L_m = \frac{T_0 \cdot t_d}{16 C_j} \tag{4.31}$$

This outcome confirms the balance established by prior design strategies, emphasizing the pivotal role of dead-time in optimizing both switching and conduction performance in LLC resonant converters.

4.6 Control Strategies for LLC Resonant Converters

Efficient regulation of LLC resonant converters is fundamental to ensuring stable output voltage and current, particularly in demanding applications such as electric vehicle (EV) chargers. These converters inherently support soft switching, facilitating operation at elevated frequencies, which significantly reduces switching losses. This operational advantage makes LLC converters particularly suitable for compact, high-efficiency systems. A number of strategies have been developed to regulate LLC converters effectively, each with unique benefits and limitations [29, 30].

4.6.1 Methods for Regulating the LLC Converter

Frequency Modulation (FM): Frequency modulation is the most common control method for LLC converters. It involves varying the switching frequency of the primary-side MOSFETs to achieve the desired output voltage or current. The converter operates in different modes depending on whether the switching frequency is below, at, or above the resonant frequency. At resonance, output impedance is minimized, leading to maximum gain. Below resonance, the circuit enters capacitive mode, while above resonance, it operates inductively.

Pros: Simple implementation and a wide control range.

Cons: Nonlinear control characteristics and reduced efficiency at frequencies far from resonance due to high circulating currents.

Pulse-Width Modulation (PWM): In certain architectures, PWM is combined with FM to enhance control. While FM adjusts frequency, PWM manipulates duty cycle to regulate output.

Pros: Enhanced regulation and improved light-load performance.

Cons: Risk of disrupting resonance, introducing additional losses and complexity.

Burst Mode Control: This technique is typically deployed in low-power applications requiring high efficiency. The converter switches in short bursts followed by idle periods. The average output is regulated by controlling the length of these bursts.

Pros: Excellent light-load efficiency.

Cons: May introduce voltage ripple and audible noise due to intermittent operation.

Phase-Shift Modulation: By varying the phase between the gate signals of the switches, this method enables finer control of output power and voltage. The power transferred is modulated by the phase difference.

Pros: Precise control while maintaining high efficiency near resonance.

Cons: Higher design complexity and potentially reduced performance across varying loads.

Variable Resonant Tank Parameters: Advanced designs may incorporate tunable induc-

tance or capacitance within the resonant tank, enabling real-time adjustment of converter characteristics.

Pros: Offers adaptability and enhanced regulation across varying conditions.

Cons: Increases overall system complexity and cost.

Each control technique presents its own advantages and trade-offs. Frequency modulation remains the preferred method due to its simplicity and effectiveness in most scenarios. However, advanced applications with dynamic conditions may benefit from a hybrid or adaptive control strategy that combines elements from multiple techniques. The ultimate choice of control strategy should be governed by application-specific requirements including load dynamics, cost considerations, and efficiency goals.

4.7 Discussion

This chapter delves into the principles and modeling of LLC resonant converters, known for enabling soft switching (ZVS and ZCS), minimizing losses, and supporting compact high-frequency designs. Theoretical modeling using First Harmonic Approximation (FHA) is introduced to predict voltage gain. Operational regions based on switching frequency are analyzed, highlighting conditions for ZVS. The importance of dead-time optimization and various control methods (like frequency modulation) are covered to ensure stable and efficient operation across load conditions.

Chapter 5

Design and Simulation Results

5.1 Charger Specifications and Requirements

The charger designed in this work is specifically tailored to meet the operational and energy demands of typical e-bikes, considering both performance metrics and real-world deployment constraints.

The primary design requirements for the charger were established based on standard battery configurations commonly found in electric bicycles. The charger is expected to operate from a standard 230 V AC mains input and deliver a regulated DC output suitable for lithium-ion battery packs. The target output voltage is 48 V, which aligns with many commercially available e-bike battery systems. Additionally, the charger is designed to support an output power rating of 120 W, which ensures compatibility with medium-capacity battery modules while maintaining safe thermal and electrical operation.

Given the emphasis on efficiency and miniaturization, the resonant frequency for the LLC stage was selected to be 100 kHz. This enables the use of high-frequency switching devices

and smaller magnetic components, thus improving power density and overall form factor. These specifications were carefully chosen to ensure that the charger delivers stable performance under a wide range of operating conditions while adhering to regulatory standards on power factor and harmonic distortion.

Charger Specifications	
Parameter	**Value**
Output power	120 W
Input voltage	230 V AC
Output voltage	48 V
Resonant frequency f_r	100 kHz

Table 5.1: Charger Specifications

5.2 Design Methodology for LLC Resonant Converter

The design of an LLC resonant converter is a systematic process that integrates the principles of soft-switching, frequency-controlled regulation, and high-efficiency conversion. This section outlines the comprehensive procedure for designing an LLC resonant converter, as informed by industry-standard practices and detailed in the Infineon Application Note [31, 32].

The process begins with the definition of system specifications, including the input voltage range ($V_{in_{min}}, V_{in_{nom}}, V_{in_{max}}$), output voltage V_{out}, output power $P_{out_{max}}$, and the target resonant frequency f_r. These parameters are fundamental in determining the gain requirements, which are expressed as:

$$M_{nom} = \frac{V_{out}}{V_{in_{nom}} \cdot n}, \quad M_{max} = \frac{V_{out}}{V_{in_{min}} \cdot n},$$

where n is the transformer turns ratio (N_s/N_p).

Subsequently, the designer selects a suitable maximum quality factor Q_{max}, generally within the range of 0.4 to 0.7. This factor is related to the load and impacts the resonant tank's bandwidth and regulation capability. The quality factor is defined as:

$$Q = \frac{R_{ac}}{\omega_r L_r}, \quad \text{with} \quad R_{ac} = \frac{8}{\pi^2} \cdot \left(\frac{N_p}{N_s}\right)^2 \cdot \frac{V_{out}^2}{P_{out}}.$$

An essential design parameter is the inductance ratio $m = L_m/L_r$, which controls the gain profile and circulating current. A moderate value of m, typically between 4 and 8, is recommended to balance the gain range and efficiency.

From the gain versus frequency plots, the minimum normalized switching frequency $F_{x_{min}}$ is identified by locating the gain peak for the chosen Q and m values. This frequency, $f_{s_{min}} = F_{x_{min}} f_r$, ensures inductive operation across the full load range. It is critical to validate that the maximum gain K_{max} at light load satisfies:

$$K_{max} \geq M_{max}.$$

If not, the inductance ratio m must be adjusted accordingly.

With these parameters defined, the resonant tank elements can be calculated. The resonant capacitor C_r is derived from:

$$C_r = \frac{1}{(2\pi f_r)^2 L_r},$$

and the values of L_r and L_m follow from the relations:

$$L_r = \frac{R_{ac}}{2\pi f_r Q_{max}}, \quad L_m = m \cdot L_r.$$

The transformer design should then be completed to ensure the target voltage ratio and

accommodate the calculated inductances while minimizing leakage.

Next, the appropriate power stage topology must be selected. A full-bridge converter is preferred for higher power levels due to its current handling capabilities, whereas a half-bridge configuration is more economical and compact for lower power levels.

The final stage involves simulation and experimental validation. Through simulation, designers verify Zero Voltage Switching (ZVS), gain response, and overall performance. The hardware prototype is then fine-tuned using waveform analysis and efficiency measurements to meet all operational and regulatory requirements.

The LLC resonant converter design methodology requires careful selection of tank parameters and resonant frequency in conjunction with transformer and power stage considerations. This approach ensures high-efficiency, soft-switched operation suitable for demanding power conversion applications.

Resonant Tank Parameters	
Parameter	**Value**
Quality factor Q	0.3
Normalized resonant inductor $m = \frac{L_m}{L_r}$	6.3
Transformer turns ratio $N_p : N_s$	1:6.76
Leakage (resonant) inductor L_r	2.48 μH
Resonant capacitor C_r	0.64 μF
Magnetizing inductor L_m	13.144 μH

Table 5.2: Resonant Tank Parameters

5.3 Simulation Setup

The simulation environment was developed using MATLAB/Simulink to validate the behavior of the boost PFC and LLC resonant converter stages prior to hardware implementation. The models include idealized switching elements, parasitic components, and real-time load conditions emulating a typical e-bike battery. The PFC model was configured to operate in both Continuous and Critical Conduction Modes (CCM and CRM), while the LLC stage was tuned to switch at a nominal frequency of 100 kHz.

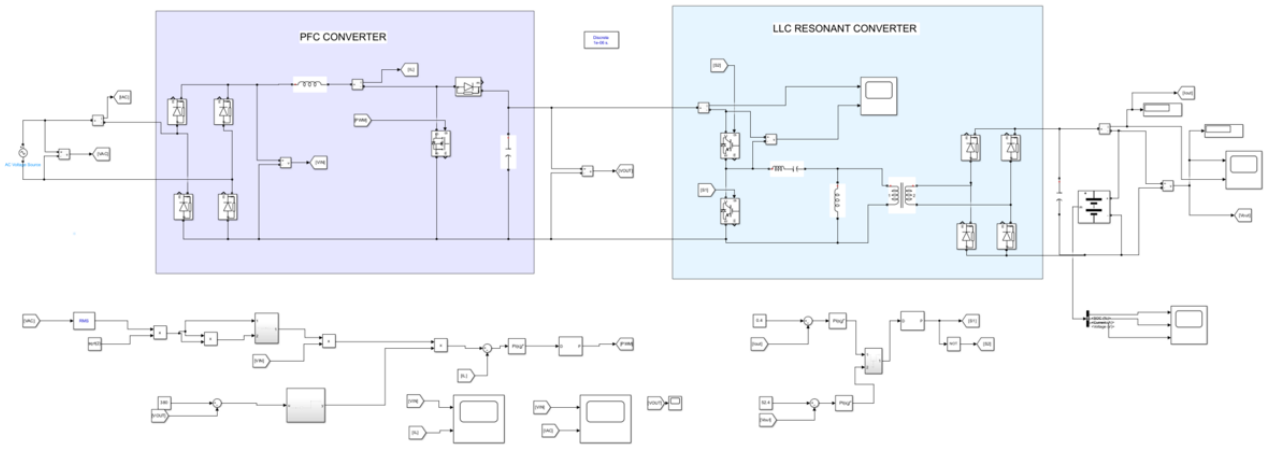


Figure 5.1: Simulink model for Battery Charger

5.3.1 PFC Stage Simulation Results

The boost PFC simulation demonstrated proper shaping of the input current in accordance with the input voltage waveform. The rectified AC input was followed by a high-frequency switching boost converter, which maintained continuous current flow through the inductor. The resulting waveforms confirm that the circuit meets the current shaping objectives necessary for effective harmonic mitigation and power factor correction.

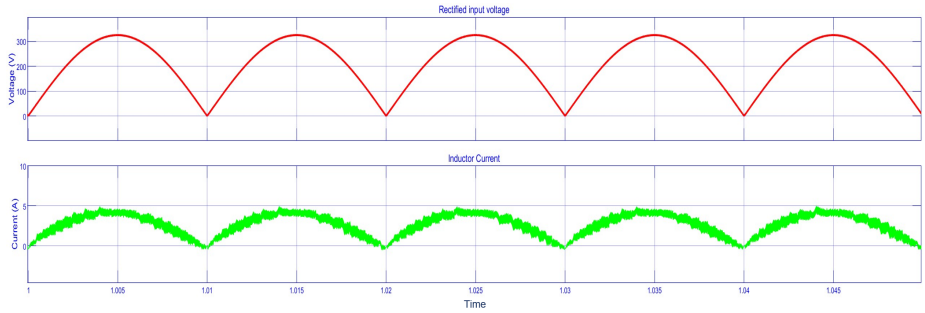


Figure 5.2: Rectified Input Voltage and Inductor Current

5.3.2 LLC Resonant Converter Stage Simulation Results

In the LLC stage, simulation results revealed soft-switching characteristics under nominal load. Voltage and current waveforms at the primary side of the transformer exhibited the expected phase relationships, validating Zero Voltage Switching (ZVS). These results affirm that the designed converter operates in the intended inductive region, achieving efficient energy transfer with minimal switching losses.

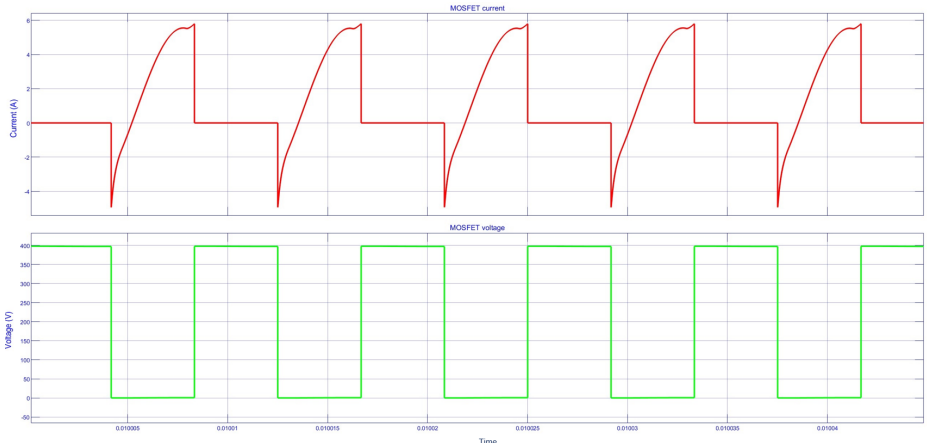


Figure 5.3: Waveforms of Primary side Current and Voltage

Chapter 6

Hardware Implementation and Experimental Results

6.1 Component Selection Considerations

Selecting appropriate components is a fundamental aspect of designing efficient and reliable power electronic systems. Within this thesis, attention is devoted to both the Power Factor Correction (PFC) stage and the LLC Resonant Converter stage. Proper component selection impacts system efficiency, electromagnetic compatibility, thermal performance, and cost. This section outlines the design considerations and selection criteria for both the PFC and the LLC stages.

6.1.1 Power Factor Correction Circuit

The PFC stage commonly adopts a boost converter topology owing to its simplicity, ability to produce higher DC voltage from an AC source, and high efficiency. The effectiveness of this stage relies heavily on the careful selection of its passive and active components [15].

6.1.1.1 PFC Inductor

The inductor, also referred to as the PFC choke, governs current shaping and energy buffering. Its selection is based on peak current capacity, core losses, and thermal stability. In Continuous Conduction Mode (CCM), the inductance tends to be higher to sustain continuous current, while Discontinuous Conduction Mode (DCM) allows smaller inductors. Core materials such as ferrite are often selected for their low loss characteristics. Toroidal geometries offer economical solutions, whereas bobbin-wound inductors can simplify assembly.

6.1.1.2 PFC Diode

The diode used in the boost PFC circuit must handle high voltages and fast switching. Reverse recovery characteristics are critical in reducing switching losses and EMI. Selection must account for reverse voltage ratings, peak current capacity, and forward voltage drop.

6.1.1.3 PFC Switch

Typically implemented using MOSFETs, the switch is chosen based on its breakdown voltage, current rating, $R_{DS(on)}$, and gate charge. Low $R_{DS(on)}$ reduces conduction losses, while a lower gate charge enables faster transitions and reduced dynamic power dissipation. Trade-offs between cost and performance are evaluated depending on system constraints.

6.1.2 LLC Resonant Converter Circuit

Component selection in the LLC stage is driven by resonance behavior, soft-switching requirements, and power density goals. Major elements include the resonant transformer, resonant inductor, resonant capacitor, and switching devices.

6.1.2.1 Resonant Transformer

The transformer ensures galvanic isolation and contributes to the resonant network. Its design should precede inductor and capacitor selection due to its impact on magnetizing inductance (L_m). High-frequency operation prioritizes low core losses, and core selection aims to minimize flux density. Magnetizing inductance is controlled via turns ratio and air gap. Toroidal or planar transformers are often used for their compactness and thermal performance.

6.1.2.2 Resonant Inductor

If not integrated within the transformer, the resonant inductor must independently accommodate the resonant tank current. It is designed with sufficient air gap to manage flux density without saturation. As it handles the full tank current, larger gaps are often required compared to transformers.

6.1.2.3 Resonant Capacitor

Capacitor selection focuses on its ability to handle peak voltage and RMS current. Due to voltage amplification during resonance, capacitors must be derated accordingly. Film capacitors or MLCCs (Multi-Layer Ceramic Capacitors) are favored due to their low ESR and temperature stability. Often, a capacitor bank is employed rather than a single unit to meet both voltage and current requirements.

These design considerations ensure that the LLC converter maintains soft switching, minimizes losses, and achieves stable operation across a wide load and line range. Together with the PFC stage, component selection defines the overall efficacy and robustness of the e-bike charger system.

6.1.2.4 MOSFET Selection Criteria

The selection of MOSFETs plays a pivotal role in determining the performance and efficiency of both the PFC and LLC stages. Key parameters influencing the choice include drain-to-source breakdown voltage (V_{DS}), on-state resistance ($R_{DS(on)}$), gate charge (Q_g), and switching speed. For high-frequency applications, such as LLC resonant converters, low Q_g and minimal $R_{DS(on)}$ are essential to reduce both switching and conduction losses. Adequate voltage margin above the peak drain voltage is necessary to ensure reliable operation under transient conditions. Thermal resistance and package type also influence heat dissipation, which becomes critical in compact designs. In resonant topologies, achieving Zero Voltage Switching (ZVS) relaxes some constraints on switching loss, allowing trade-offs favoring lower conduction loss. Devices with optimized body diode performance are preferred to mitigate reverse recovery losses, especially in soft-switching environments. The final selection must strike a balance between electrical performance, thermal limits, cost, and PCB layout constraints to meet the stringent efficiency and size requirements of e-bike chargers [33].

6.2 Hardware Implementation of PFC Stage

A laboratory-scale prototype of the boost PFC circuit was fabricated and tested under varying input and load conditions. The experimental setup included a diode bridge rectifier followed by a boost inductor, ultrafast diode, and high-frequency MOSFET. A LEM current transducer was employed to accurately measure the input current. This sensor offered galvanic isolation and was capable of capturing dynamic changes in current with high precision. For voltage measurement, TI TL082 IC was used to scale down the high rectified input voltage to a level suitable for analog-to-digital conversion. These voltages were then

fed into a Texas Instruments LAUNCHXL-F28379D development board, which houses the TMS320F28379D DSP.

This DSP system utilized its onboard ADC modules to sense both the input current and scaled voltage in real time. Based on this data, the controller generated corresponding PWM signals to regulate the MOSFET switch in the boost converter. This closed-loop implementation enabled precise control of the input current waveform, facilitating effective PFC and reducing harmonic distortion.

To assess power quality, the input current waveforms and their associated Total Harmonic Distortion (THD) levels were analyzed using the FFT functionality of a digital oscilloscope. The experiment was carried out under three different configurations to highlight the progressive improvements achieved at each stage. Fig 6.1 shows the hardware setup of boost power factor correction circuit in lab.

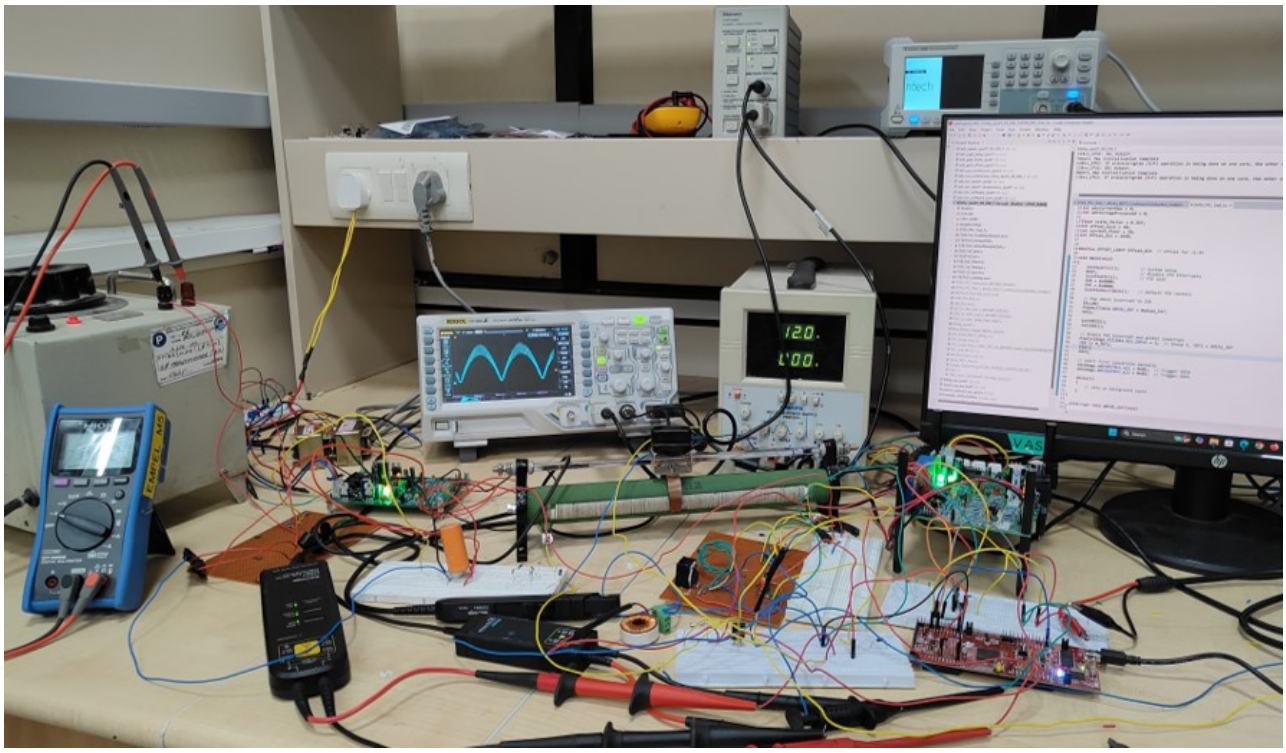


Figure 6.1: Hardware setup of PFC circuit in Lab

6.3 Hardware Results with THD Analysis

To comprehensively evaluate the impact of power factor correction (PFC) strategies and validate simulation findings, a series of hardware experiments were conducted using a prototype charger system. The analysis focused on the input current waveform characteristics and the corresponding Total Harmonic Distortion (THD), measured using the FFT feature of a digital oscilloscope. The evaluation was performed for three distinct configurations to illustrate the progressive improvement in power quality: (a) a basic diode bridge with capacitive filter, (b) a boost PFC operating in Critical Conduction Mode (CRM), and (c) a boost PFC operating in Continuous Conduction Mode (CCM).

6.3.1 Current Waveform: Diode Bridge with Capacitor Filter

Figure 6.2: Experimental Results: Current waveform of Diode Bridge

The first test used the most elementary AC-DC conversion method: a full-wave diode bridge followed by a bulk capacitor. This topology, while cost-effective and simple to implement, suffers from fundamental limitations in terms of power quality. The capacitor charges only during the peaks of the AC input voltage, resulting in narrow, high-amplitude current pulses. These pulses contain significant harmonic components, particularly in the lower orders (3rd,

5th, 7th), which contribute to electromagnetic interference (EMI) and cause substantial reactive power flow.

Figure 6.3: THD analysis of Diode Bridge Rectifier

Measured THD for this setup was found to be approximately 84.85%, indicating a highly distorted current waveform. From a standards compliance perspective, this level of distortion is well above the limits set by IEC 61000-3-2 Class C requirements for battery-powered devices. Furthermore, the non-sinusoidal current draw introduces voltage dips and line distortion when multiple chargers operate on the same feeder, posing a threat to grid stability.

6.3.2 Current Waveform: Boost PFC in Critical Conduction Mode (CRM)

Figure 6.4: Experimental Results: Critical Conduction Mode

To address the shortcomings of passive filtering, a boost converter configured to operate in Critical Conduction Mode was integrated after the rectifier. In CRM, the switch turns on immediately after the inductor current reaches zero, minimizing switching losses and eliminating reverse recovery stress on the diode. While simpler to implement than CCM and inherently efficient at light loads, CRM produces a current waveform that, though improved, still exhibits discontinuities.

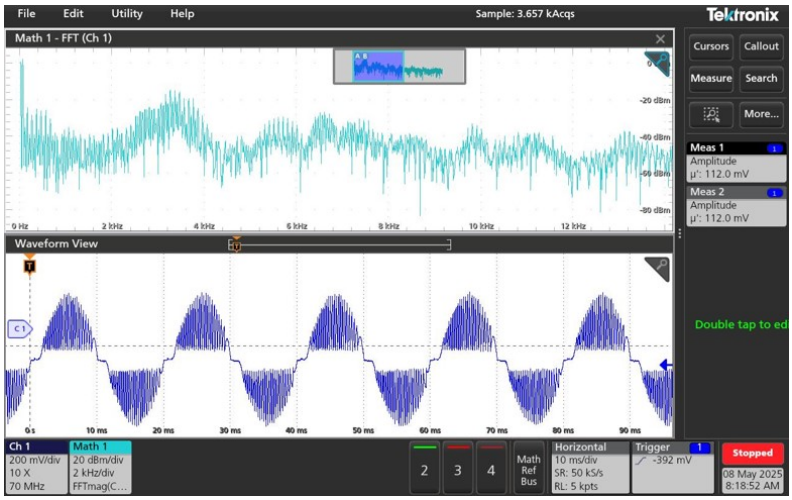


Figure 6.5: THD analysis of Critical Conduction Mode

Experimental results demonstrated a significant improvement in harmonic profile. The input current waveform became wider and more sinusoidal, with a measured THD reduced to 29.41%. The waveform closely followed the voltage envelope, improving the power factor and reducing stress on both upstream and downstream components. This setup illustrates how active control, even with modest complexity, can result in meaningful gains in power quality.

6.3.3 Current Waveform: Boost PFC in Continuous Conduction Mode (CCM)

Figure 6.6: Experimental Results: Continuous Conduction Mode

The most refined test setup used a boost converter operating in Continuous Conduction Mode, in which the inductor current never falls to zero. This mode is preferred in high-power or high-performance designs due to its ability to deliver a nearly ideal current waveform. The continuous inductor current minimizes ripple, and the switch transitions are smoother, reducing both EMI and switching stress.

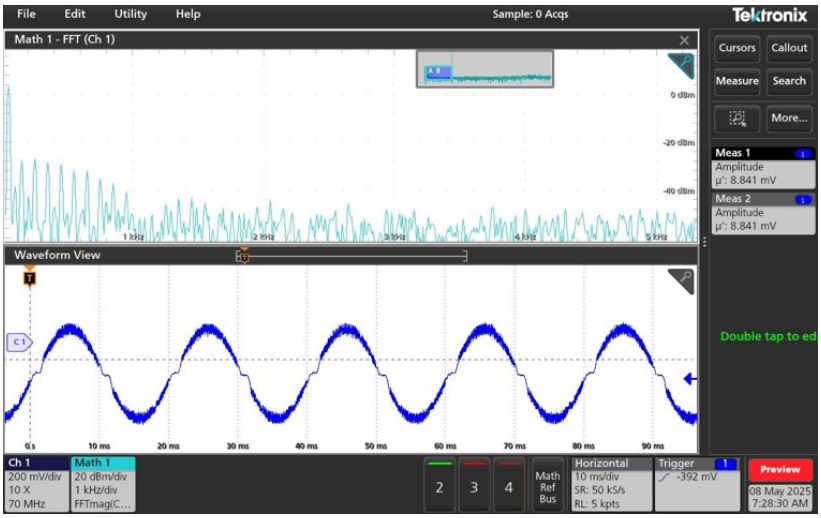


Figure 6.7: THD analysis of Continuous Conduction Mode

The hardware implementation yielded a THD of 13.4%, marking a substantial reduction from previous configurations. The input current waveform was nearly sinusoidal and maintained a close phase alignment with the voltage waveform, indicating a near-unity power factor. This setup fully complies with IEC standards and provides excellent performance across a range of load conditions. Moreover, the low harmonic content reduces the size and cost of input filters and contributes to overall converter efficiency and thermal stability.

6.4 Discussion

The comparative study of the three configurations highlights the critical role of active PFC in meeting modern electrical standards and achieving high-performance energy conversion. While a passive diode-capacitor network is inadequate for any serious application beyond the hobbyist level, even a basic CRM implementation can yield substantial improvements in waveform quality. However, it is the CCM operation that emerges as the most viable solution for commercial and industrial-grade e-bike chargers.

Beyond compliance, the smoother current waveform in CCM reduces the RMS and peak

current stresses on components, extending their lifespan and enabling thermal optimization. These experimental findings validate the simulation assumptions and support the broader system-level strategy of integrating a CCM-based PFC stage with an LLC resonant converter for efficient, reliable, and standards-compliant charging.

Chapter 7

Conclusion and Further Work

7.1 Conclusions

This thesis presented the design, simulation, and partial hardware implementation of a high-efficiency, two-stage charger for electric bicycle applications. The system architecture comprises a boost Power Factor Correction (PFC) stage followed by an LLC resonant converter stage, aimed at achieving superior power quality, energy efficiency, and compliance with modern grid standards.

The boost PFC stage was simulated and experimentally validated in both Continuous Conduction Mode (CCM) and Critical Conduction Mode (CRM). Hardware implementation confirmed the converter's ability to improve power factor and reduce Total Harmonic Distortion (THD), with measurements showing THD reductions from 84.85% in the diode-bridge configuration to 13.4% in CCM. These results validate the efficacy of the active PFC circuit in shaping the input current and minimizing harmonic content.

The LLC resonant converter, forming the second stage, was fully modeled and simulated to

confirm key performance features such as soft-switching operation (Zero Voltage Switching) and resonant behavior. Simulation results supported its suitability for high-frequency, high-efficiency DC-DC conversion.

Together, the simulation and experimental results substantiate the core design proposition: a hybrid PFC-LLC architecture is a viable solution for compact and efficient e-bike chargers.

7.2 Further Works

While significant milestones were achieved in the design and validation of the PFC stage, several avenues remain open for further research and development:

- **Hardware Implementation of the LLC Stage:** Completion of the LLC converter's hardware design, including the resonant tank and transformer, is essential to fully validate the two-stage architecture.
- **Component Optimization:** Selection and testing of magnetic components (planar or wound) for improved thermal handling and power density in the LLC stage.
- **Digital Control Integration:** Deployment of closed-loop digital control strategies on the F28379D DSP for output voltage regulation and adaptive soft-switching.
- **System Integration:** Full integration of PFC and LLC stages to create a complete and functional e-bike charger system.
- **Thermal and EMI Testing:** Extensive analysis of thermal behavior and electromagnetic interference under varying load conditions.
- **Packaging and Productization:** Design and development of a compact mechanical enclosure suitable for field deployment.

Pursuing these goals will elevate the project from a functional prototype to a production-ready solution, aligned with global trends in sustainable mobility and smart grid technologies.

References

[1] Power Integrations, Inc., “HiperPFS Family Design Guide, Appl. Note AN-52,” 2017. Rev. C, Dec. 2017.

[2] S. Abdel-Rahman. ”CCM PFC Boost Converter Design.” Design Note DN 2013-01, Ver. 1.0, Jan. 2013.

[3] S. Yu, “Power Tips: Designing an LLC Resonant Half-bridge Power Converter.” Texas Instruments, Appl. Report, Jul. 2015.

[4] STMicroelectronics ”An Introduction to LLC Resonant Half-Bridge Converter,” Appl. Note AN2644, Sept. 2008.

[5] Toshiba Corporation. ”Resonant Circuits and Soft Switching (LLC Resonant Converter and Resonant Inverter),” Appl. Note, Nov. 2019.

[6] H. Choi “Half-bridge LLC resonant converter design using FSFR-series Fairchild power switch (FPS™),” Appl. Note AN-4151, Fairchild Semiconductor, Oct. 2014.

[7] B. Bilgin, P. Magne, P. Malysz, Y. Yang, V. Pantelic, M. Preindl, A. Korobkine, W. Jiang, M. Lawford, and A. Emadi, “Making the case for electrified trans.,” *IEEE Trans. Transp. Electrific*, vol. 1, no. 1, pp. 4–17, May 2015.

[8] S. S. Williamson, A. K. Rathore, and F. Musavi, "Industrial electronics for electric transportation: Current state-of-the-art and future challenges," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3021–3032, Mar. 2015.

[9] E. Compatibility, "Limits for harmonic current emissions (equipment input current 16a per phase)," *IEC Standard IEC*, pp. 61000–3, 2006.

[10] L. Wang, J. Liang, G. Xu, K. Xu, and Z. Song, "A novel battery charger for plug-in hybrid electric vehicles," pp. 168–173, Jul. 2012.

[11] G. Hua and F. Lee, "Soft-switching techniques in pwm converters," *IEEE Trans. Ind. Electron.*, vol. 42, no. 6, pp. 595–603, Dec. 1995.

[12] C. Qiao and K. Smedley, "A topology survey of single-stage power factor corrector with a boost type input-current-shaper," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 360–368, Feb. 2001.

[13] M. Zhang, Y. Jiang, F. Lee, and M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Proceedings of 1995 IEEE Appl. Power Electron. Conference and Exposition - APEC'95*, vol. 1, pp. 434–439 vol.1, Mar. 1995.

[14] Toshiba Corporation, "Power factor correction (PFC) circuits," Appl. Note, Nov. 2019.

[15] J. Turchi, D. Dalal, P. Wang, and L. Jenck, *Power Factor Correction (PFC) Handbook: Choosing the Right Power Factor Controller Solution*. ON Semiconductor, rev. 5 ed., 2014.

[16] X. Xie, J. Zhang, Z. Zhao, and Z. Qian, "Analysis and optimization of llc resonant converter with a novel over-current protection circuit," *IEEE Trans. Power Electron.*, vol. 22, pp. 435 – 443, Apr. 2007.

[17] Pavol, J. Kandrac, M. Frivaldsky, and P. Drgona, "Verification of operation modes of designed llc resonant converter," *Commun. - Scientific letters of the University of Zilina*, vol. 13, pp. 67–73, Jul. 2011.

[18] Y. Chen, H. Wang, Y.-F. Liu, J. Afsharian, and Z. Yang, "Llc converter with auxiliary switch for hold up mode operation," pp. 2312–2319, Mar. 2016.

[19] A. Hillers, D. Christen, and J. Biela, "Design of a highly efficient bidirectional isolated llc resonant converter," in *2012 15th International Power Electron. and Motion Control Conference (EPE/PEMC)*, pp. DS2b.13–1–DS2b.13–8, Sept. 2012.

[20] H. Huang, "Fha-based voltage gain function with harmonic compensation for llc resonant converter," in *in Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC), 2010, pp. 1770–1777.*, pp. 1770–1777, Feb. 2010.

[21] J. Lazar and R. Martinelli, "Steady-state analysis of the llc series resonant converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC), 2001, vol. 2, pp. 728–735.*, vol. 2, pp. 728–735 vol.2, Aug. 2001.

[22] J. Gao, J. Zhang, Q. Song, Z. Zhu, and L. Qian, "An llc resonant single-stage inverter with high-frequency link and soft-switching," *IEEE Journal of Emerg. and Sel. Topics Power Electron.*, vol. 10, no. 3, pp. 2959–2974, Jan. 2022.

[23] B. Li, X. Zhang, D. Zhou, S. Sun, Y. Wang, and D. Xu, "Soft-switching characteristics analysis based on llc resonant converter," in *IEEE Trans. Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*, pp. 1–6, Jun. 2018.

[24] U. Kundu, K. Yenduri, and P. Sensarma, "Accurate zvs analysis for magnetic design and efficiency improvement of full-bridge llc resonant converter," *IEEE Trans. Power*

Electron., vol. 32, no. 3, pp. 1703–1706, Aug. 2017.

[25] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Using llc resonant converter for designing wide-range voltage source," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1746–1756, Jun. 2011.

[26] Z. Fang, T. Cai, S. Duan, and C. Chen, "Optimal design methodology for llc resonant converter in battery charging applications based on time-weighted average efficiency," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5469–5483, Oct. 2015.

[27] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Optimizing the normalized dead-time and maximum switching frequency of a wide-adjustable-range llc resonant converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 462–472, Feb. 2011.

[28] C. Sun, Q. Sun, R. Wang, Y. Li, and D. Ma, "Adaptive dead-time modulation scheme for bidirectional llc resonant converter in energy router," *CSEE Journal of Power and Energy Syst.*, vol. 10, no. 4, pp. 1710–1721, Dec. 2024.

[29] B.-R. Lin and G.-Y. Wu, "Bidirectional resonant converter with half-bridge circuits: Analysis, design, and implementation," *Energies*, vol. 11, no. 5, Apr. 2018.

[30] H. Al Attar, M. A. Hamida, M. Ghanes, and M. Taleb, "Review on modeling and control strategies of dc–dc llc converters for bidirectional electric vehicle charger applications," *Energies*, vol. 16, no. 9, May 2023.

[31] S. Abdel-Rahman "Resonant llc converter: Operation and design," Appl. Note AN 2012-09, Infineon Technologies North America (IFNA) Corp., Sept. 2012.

[32] J. Deng, S. Li, S. Hu, C. Mi, and R. Ma, "Design methodology of llc resonant converters for electric vehicle battery chargers," *IEEE Trans. Veh. Technol.*, vol. 63, pp. 1581–1592, May 2014.

[33] Infineon Technologies AG, "Primary side MOSFET selection for LLC topology," Appl. Note, Revision 1.0, Jun. 2014.