Design of Wide Band Power Amplifier

M.Tech. Thesis

By

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DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE

May 2026

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Thesis

Submitted in partial fulfillment of the requirements for the award of the degree of

Master of Technology

by

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DEPARTMENT OF ELECTRICAL ENGINEERING

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May 2026

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **Design of Wide Band Power Amplifier** in the partial fulfillment of the requirements for the award of the degree of **Master of Technology - VLSI Design And Nanoelectronics** and submitted in the Department of Electrical Engineering, Indian Institute of Technology Indore, is an authentic record of my own work carried out during the time period from July 2025 to June 2026 under the supervision of Dr. Rinke Chopra, Professor, Indian Institute of Technology Indore, Indore, India.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

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Signature of the Student with Date

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This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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Date: 21-05-2026

ACKNOWLEDGEMENTS

I would like to convey my deep gratitude to **Dr. Rinkee Chopra**, my respected supervisor at IIT Indore, whose remarkable mentorship has played a pivotal role in my research journey. Her enthusiasm for scientific inquiry and unwavering dedication to excellence have continually inspired me. Her careful guidance and insightful feedback have profoundly influenced both my research and my personal development. I will always be grateful to her for her invaluable assistance, which has been crucial in helping me articulate and present my work with clarity and accuracy. Additionally, I wish to express my heartfelt thanks to **Dr. Rinkee Chopra**, the Co-Ordinator of my thesis evaluation committee, and the committee itself. Their fair assessments and stimulating questions have greatly enriched my research perspective.

I am immensely grateful to **Dr. Saptarishi Ghosh** and **Applied Electromagnetics Laboratory research group**, for providing me the SDR for testing my power amplifier design. I am so thankful for their support throughout my project work. I am extremely grateful to my colleagues from the Radio Frequency Lab (RF Lab)—Ms. Prachi Joshi, Mr. Adhithya Pathak, Ms. Sagnika Sen.

— I am thankful for their support and encouragement throughout the experimental work. Our collaborative lab experiences and conversations greatly improved my understanding and skills in this area. My heartfelt thanks go to my loving parents, Shri. Manchala Ramesh and Smt. Manchala Shobha, and my younger brother, Mr. Manchala Abhichand . The countless sacrifices they have made, their endless support, and unwavering faith in my capabilities have served as my strongest source.

I am profoundly grateful to my friends from the VLSI Design and Nanoelectronics Batch – 2026, for their endless encouragement and steadfast belief in my abilities. Their companionship has made this journey far more rewarding and enjoyable. Finally, I would like to express my appreciation to everyone—both familiar and unfamiliar—who has played a role, whether directly or indirectly,

in helping me complete my thesis successfully. Your contributions, regardless of their size, have made a significant impression on this work. To each of you, I extend my heartfelt thanks and genuine gratitude.

This thesis is dedicated to
all the people who have supported me
throughout this journey

ABSTRACT

Wideband, high-efficiency power amplifiers (PAs) must be developed in order to meet the growing need for multi-band and high-data-rate wireless communication systems. The design and execution of a wideband power amplifier with a multi-octave bandwidth that operates between 0.45 GHz and 2.9 GHz are presented in this thesis. The Advanced Design System (ADS) is used to carry out the design, and both simulation and hardware realization are used to validate it.

CGH40010F GaN HEMT transistor, selected for its outstanding power handling capability and efficiency, is used in the suggested amplifier. A appropriate impedance matching network is constructed in conjunction with extended continuous mode-inspired harmonic tuning approaches to achieve broadband performance. High efficiency throughout a broad frequency range is made possible by this method's efficient regulation of fundamental and harmonic impedances.

The simulated findings of the amplifier show good agreement. Throughout the operating band, it attains maximum output power of 40.8 dBm, maximum power-added efficiency (PAE) of 58.19 percentage , and maximum drain efficiency of 60.3 percentage. Furthermore, the amplifier exhibits steady and effective performance in both linear and nonlinear operating circumstances, with a small-signal gain of 13.6 dB and a large-signal gain of 12.13 dB.

The findings verify that the suggested wideband power amplifier is a good fit for contemporary RF applications where high efficiency and broad frequency coverage are essential, such as wireless communication systems, radar, and broadband transmitters.

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List of Abbreviations

RF	-	Radio Frequency
ECCE	-	Extended Continuous Class E
CCE	-	Continuous Class E
ADS	-	Advanced Design System
GaN	-	Gallium Nitride
HEMT	-	High Electron Mobility Transistor
PAE	-	Power Added Efficiency
DE	-	Drain Efficiency
SDR	-	Software Defined Radio
PCB	-	Printed Circuit Board
ZVS	-	Zero Voltage Switching
ZVDS	-	Zero Voltage Derivative Switching
IRP	-	Intrinsic Reference Plane
ERP	-	Extrinsic Reference Plane
IMN	-	Input Matching Network
OMN	-	Output Matching Network
LPF	-	Low Pass Filter
HPF	-	High Pass Filter
BPF	-	Band Pass Filter
CCA	-	Current Conduction Angle
BW	-	Bandwidth
HD	-	Harmonic Distortion
MLIN	-	Microstrip Line
MLOC	-	Microstrip Open Stub
MTEE	-	Microstrip Tee Junction
MSTEP	-	Microstrip Step Transition

Chapter 1

Introduction

1.1 Fundamentals of Power Amplifiers

Power amplifiers (PAs) are essential components in radio frequency (RF) and microwave communication systems, as they amplify low-power signals to a level that can be transmitted effectively through antennas. The performance and efficiency of a communication system largely hinge on the attributes of the power amplifier, such as gain, efficiency, linearity, and bandwidth. In RF transmitters, the PA typically serves as the last stage, consuming a considerable portion of the overall power, which makes efficiency a crucial aspect of the design.

Power amplifiers are categorized into several classes, including Class A, Class B, Class AB, Class C, Class E, Class F, and Class J, depending on their conduction angle and operating mechanisms. Among these, switching-mode amplifiers such as Class E are commonly utilized in high-efficiency applications because they theoretically can achieve nearly 100 percentage efficiency by reducing the overlap between voltage and current waveforms. Nonetheless, traditional high-efficiency amplifiers tend to be narrowband since they depend on precise harmonic tuning at specific frequencies.

Enhancing energy efficiency while preserving high output power and signal integrity is a major focus of contemporary communication systems. Advanced PA architectures have been developed in response to the growing need for small and energy-efficient devices.

Parameters including output power, power-added efficiency (PAE), drain efficiency (DE), and gain are commonly used to assess a PA's performance. Finding the ideal balance between these factors is a significant design issue.

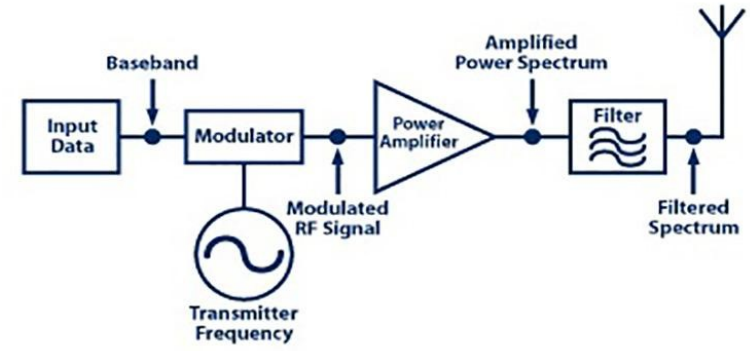


Figure 1.1: Block diagram of a typical RF transmitter showing the role of the power amplifier as the final stage before transmission.[6]

Additionally, the PA performance is greatly impacted by the active device selection. Gallium nitride (GaN) and other wide bandgap semiconductor technologies have become popular because of their excellent thermal performance, high breakdown voltage, and high electron mobility. The design of high-power, high-efficiency amplifiers appropriate for broadband applications is made possible by these features.

1.2 Need for Wideband Power Amplifiers

The wireless communication technologies such as 4G, 5G, satellite communication and radar systems are rapidly evolving that demands power amplifier to be operated with very wide frequency range. Legacy narrowband amplifiers do not meet the capacity of modern day applications which are needed to operate in multi-band and broadband fashion. Consequently wideband power amplifiers have emerged as an important field of research.

By replacing power amplifiers with wideband amplifiers, however, one hardware platform can cover a number of frequency bands, resulting in lower weight and cost for the system. Furthermore, they are critical in applications including cognitive radio, software defined radio (SDR), and broadband communication systems due to their flexibility and adaptability.In addition, wideband operation is necessary for systems that use carrier aggregation and high data rate transmission.

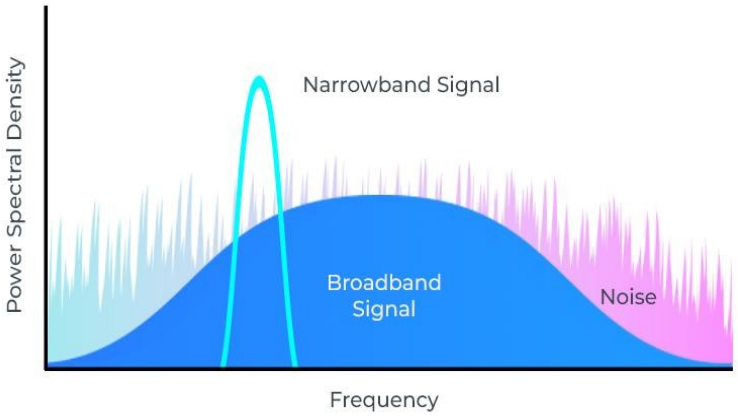


Figure 1.2: Narrow Band Vs Wide Band power amplifier response.[7]

Creating wideband power amplifiers presents a number of challenges. The impedance observed by the transistor changes considerably with frequency, complicating the process of achieving proper matching throughout the entire frequency band. Additionally, efficiency generally diminishes at frequencies that are distant from the design's center frequency. To address these challenges, contemporary design strategies concentrate on broadening the bandwidth by loosening harmonic restrictions and accommodating a variety of impedance scenarios.

Recent developments in continuous mode operation have shown that integrating fundamental and harmonic impedance conditions can facilitate multi-octave bandwidth performance. This approach allows the amplifier to sustain high efficiency across an expanded frequency range in comparison to conventional designs. Consequently,

the advancement of wideband power amplifiers is crucial to satisfy the increasing requirements of next-generation communication systems.

1.3 Design Challenges and Techniques for Wideband PA's

Developing a wideband power amplifier involves tackling various technical issues related to impedance matching, efficiency, gain stability, and harmonic management. A crucial challenge is obtaining broadband impedance matching at both the transistor's input and output. Since impedance fluctuates with frequency, traditional matching methods fall short for wideband applications. To achieve the necessary performance, advanced matching networks that utilize distributed elements and multi-section transmission lines are typically used.

Another major challenge is ensuring high efficiency across the complete frequency spectrum. To operate efficiently, it is essential to have precise control over harmonic components. In switching-mode amplifiers like Class E, efficiency is secured by achieving zero-voltage switching (ZVS) and zero-voltage derivative switching (ZVDS) conditions. However, these conditions depend on frequency, making it challenging to maintain them throughout the entire range.

To address these issues, modern techniques such as continuous mode operation and harmonic tuning are used. Continuous modes, including extended Class E, Class F, and Class J, allow a continuum of impedance conditions rather than fixed harmonic terminations. This flexibility enables the amplifier to operate efficiently over a wider frequency range. The introduction of resistive components in harmonic impedance further expands the design space, allowing overlap between fundamental and harmonic loads, which is crucial for multi-octave operation .

Additionally, the use of advanced semiconductor devices such as GaN HEMTs significantly enhances the performance of wideband amplifiers. These devices offer high power density, high efficiency, and excellent thermal stability. Load-pull analysis is commonly

used to determine the optimal impedance conditions for maximum power and efficiency. The design process also involves extensive simulation using tools like Advanced Design System (ADS), followed by hardware implementation and validation.

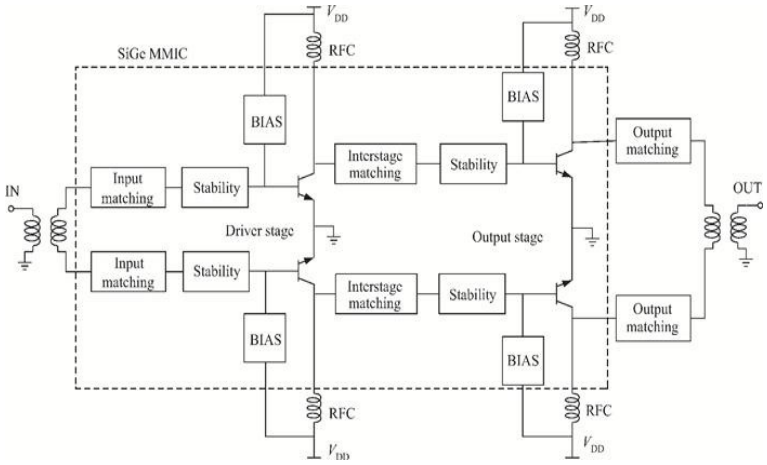


Figure 1.3: Wideband Power Amplifier Design Concept (Matching and Harmonic Control)[8].

1.4 Scope and Organization Of Thesis

1. **Chapter 1: Introduction**
   This chapter offers a foundational overview of power amplifiers and their significance in contemporary communication systems. It discusses the necessity for wideband and high-efficiency amplifiers while outlining the goals of the proposed research. Additionally, it provides a concise explanation of the ECCE mode approach utilized in this project.

2. **Chapter 2: Literature Review**
   This chapter examines prior studies related to power amplifier design, encompassing both traditional methods and modern wideband techniques.

3. **Chapter 3: Schematic Methodology and Simulation**
   This chapter details the design process of the amplifier in ADS using the ECCE approach. It elaborates on the schematic, matching networks, and biasing circuits. Furthermore, it out-

lines the entire simulation process, including S-parameter and harmonic balance analyses employed to assess performance.

4. **Chapter 4: Hardware Design and Verification**
   This chapter showcases the practical realization of the designed amplifier in hardware. It describes the PCB design, fabrication procedures, and measurement setup. The results obtained from simulations are validated through real-time hardware measurements.

5. **Chapter 5: Results and Analysis**
   It contrasts the simulated outcomes with the actual measurements, focusing on parameters such as gain, output power, efficiency, and bandwidth. The enhancements made compared to the reference design are thoroughly evaluated and articulated.

6. **Chapter 6: Summary and Future Directions**
   This section encapsulates the overall project work and its significant accomplishments. It emphasizes the advancements made in bandwidth through the proposed design and outlines potential future developments.

Chapter 2

Literature Review

2.1 Conventional Power Amplifier Modes

The effectiveness of power amplifiers (PAs), crucial components in RF and microwave communication systems, significantly influences signal integrity and overall system performance. PAs are typically categorized into Class A, B, AB, C, E, F, and J based on their conduction angles and operational characteristics. While Class A and Class AB linear amplifiers exhibit excellent linearity, their low efficiency makes them impractical for high-power uses. In contrast, Class E and Class F switching-mode amplifiers are designed to reduce the overlap between voltage and current waveforms, thereby enhancing efficiency.

Particularly noteworthy is the class E amplifier, which is extensively researched for its potential to achieve 100 percentage efficiency. This is accomplished through techniques such as zero-voltage switching (ZVS) and zero-voltage derivative switching (ZVDS), ensuring that the switching device operates under optimal conditions. Similarly, Class F amplifiers enhance efficiency by managing higher-order harmonics, effectively shaping voltage and current waveforms through harmonic tuning. Traditional amplifier designs are fundamentally narrowband, even with their advantages. Their ability to operate across a wide frequency spectrum is limited due to their dependence on precise harmonic termination at specific frequencies. These limitations have motivated researchers to explore innovative design

approaches that expand bandwidth while maintaining high efficiency, as modern communication systems increasingly demand broadband capabilities.

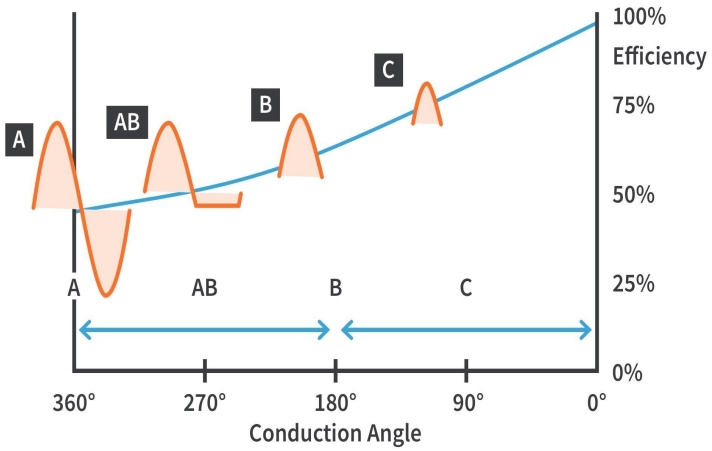


Figure 2.1: Classification Of Power Amplifiers[10]

2.2 Continuous Mode Power Amplifiers

Innovative continuous mode amplifier techniques have been introduced to address the bandwidth limitations of conventional power amplifiers (PAs). These techniques allow for a range of impedance conditions instead of fixed values, with continuous modes—such as continuous Class B/J, continuous Class F, and continuous Class E—relaxing the strict harmonic termination requirements. This flexibility enables the amplifier to maintain high efficiency across a broader frequency spectrum.

In continuous Class J amplifiers, the second harmonic impedance can be reactive, which contributes to outstanding efficiency and wideband performance. Likewise, by modifying harmonic impedance conditions, continuous Class F and inverse Class F configurations broaden the design possibilities. Continuous Class E (CCE) amplifiers further improve performance by introducing variations in load impedance while ensuring switching conditions like Zero Voltage Switching (ZVS) and Zero Voltage Derivative Switching (ZVDS) are upheld.

These continuous modes provide significant bandwidth increases

over conventional systems. However, they still face challenges when extended to multi-octave operation. One major disadvantage is that fundamental and harmonic impedance conditions do not overlap. Real wideband or multi-octave amplifiers cannot function well across widely spaced frequency bands as a result.

Therefore, even though continuous modes constitute a major advancement in PA design, further modifications are needed to achieve the wideband performance demanded by modern RF systems.

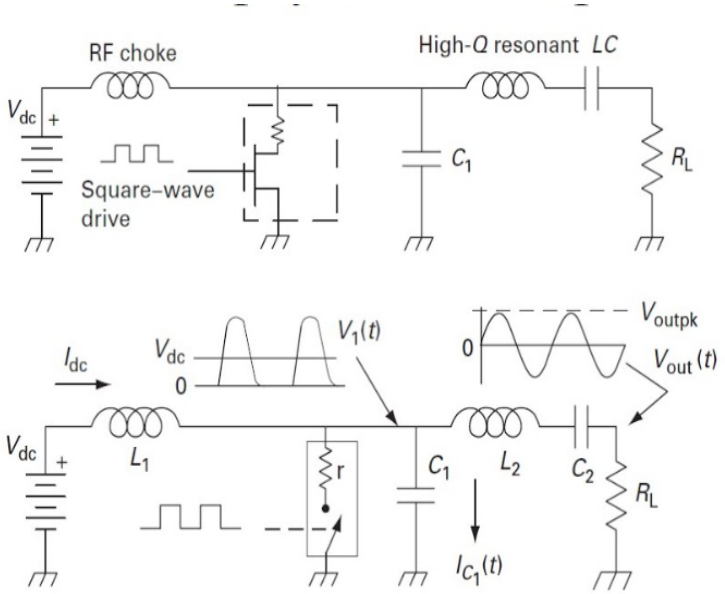


Figure 2.2: Class E amplifier basic operation[5]

2.2.1 Extending the Design Space of Class E Mode to Design a Multi-Octave Power Amplifier[1]

This study presents a methodology aimed at developing a wideband power amplifier capable of functioning across multiple octaves by enhancing the standard Class E amplifier design. The central concept is to broaden the operational range of the amplifier, enabling it to sustain high efficiency and output power throughout an extensive frequency spectrum. This is accomplished by facilitating an overlap between the fundamental and harmonic impedance conditions, a feature not achievable in conventional designs.

The design process begins with adjustments to the fundamental Class E operation. In this framework, the transistor is regarded as an ideal switch that operates under Zero Voltage Switching (ZVS) and Zero Voltage Derivative Switching (ZVDS) conditions. These conditions are instrumental in minimizing power loss by ensuring minimal overlap between voltage and current. In contrast to the traditional Class E amplifier, which features purely reactive harmonic loads, this approach incorporates a resistive element in the second harmonic impedance. This minor modification is crucial, as it enables the overlap of fundamental and second harmonic impedances, which is vital for realizing wideband (multi-octave) functionality. Subsequently, the circuit's behavior is examined through waveform-based analysis techniques.

Subsequently, the circuit's performance is evaluated through waveform analysis methods. The voltage and current waveforms are mathematically represented, introducing design parameters like phase angles (ϕ_1 and ϕ_2) and a tuning factor (δ). These parameters are essential for managing the impedance variations with frequency. By fine-tuning these elements, the designer achieves optimal waveform shaping and mitigates the risk of excessive voltage or current stress on the device.

A crucial aspect of this methodology involves analyzing the impedance space, which illustrates how the necessary impedance values fluctuate across various frequencies. The impedance plot in Figure 2.3 reveals a significant overlap between the fundamental and second harmonic impedance regions. This overlap is essential for wideband operation, as it enables the impedance at one frequency to facilitate operation at another frequency. Subsequently, the impedance values are distributed throughout the required frequency range. The entire spectrum is segmented into several sections (octaves), and appropriate impedance points are chosen for each segment. These values are then converted from the intrinsic reference plane (IRP) to the extrinsic reference plane (ERP), taking into account practical device effects such as parasitics.

The output matching network design is the following stage, which

guarantees that the intended impedance requirements are really met. Unlike classic approaches that need fixed circumstances, this method has the advantage of allowing a wide range of third harmonic impedances. This simplifies and increases the flexibility of the matching network architecture.

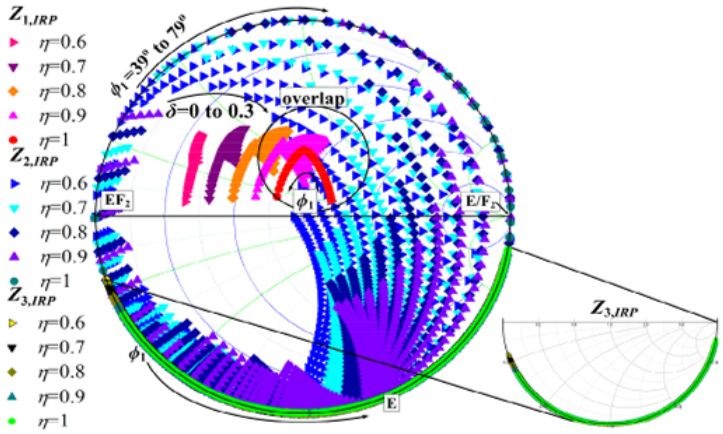


Figure 2.3: Fundamental, second harmonic, and third harmonic impedance space of ECCE mode when ϕ [39o,79o], δ [0,0.31], and η [0.6,1].

Ultimately, a CGH40010F GaN transistor is used to create the amplifier, and both simulation and hardware testing are used to confirm the design. The outcomes attest to the amplifier's great efficiency, steady gain, and steady output power across the whole frequency range.

2.2.2 High Gain Broadband Power Amplifier Design Based on Integrated Diplexing Networks[4]

The approach taken in this paper significantly diverges from conventional wideband power amplifier designs. Rather than attempting to create a single amplifier that functions across the entire frequency spectrum, the authors adopt a more intelligent and practical strategy: they integrate two smaller amplifiers, each tailored for a specific frequency range, and subsequently combine their outputs to achieve comprehensive wideband performance.

This fundamental concept is illustrated in Figure 2.4, which depicts the use of two power amplifiers. One amplifier is designated for the lower frequency range (for instance, 2–3 GHz), while the other is intended for the higher frequency range (3–4 GHz). These amplifiers are not directly linked; instead, they are merged through a specialized circuit known as a diplexer. A diplexer functions as a three-port network that either separates or combines signals according to their frequency. It incorporates two filters: a low-pass filter (LPF) for lower frequencies and a high-pass filter (HPF) for higher frequencies.

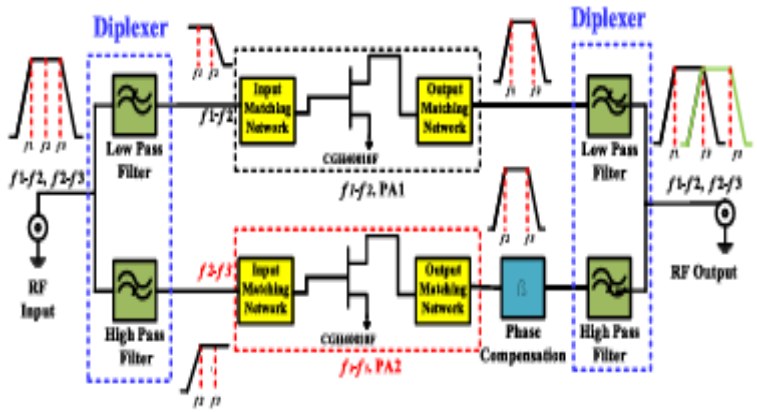


Figure 2.4: Simplified Schematic of broad band PA

In this design, the diplexer ensures that: In this design, the diplexer ensures that:

1. Low-frequency signals are routed through the first amplifier.
2. High-frequency signals are routed through the second amplifier.

After amplification, the diplexer combines both outputs into a single wideband output signal.

2.2.3 Design of a 0.4–3.9-GHz Wideband High-Efficiency Power Amplifier Based on a Novel Bandwidth Extended Matching Network[3]

This paper presents a methodology aimed at developing a highly efficient and very wideband (multi-octave) power amplifier by in-

tegrating two fundamental concepts they are Extended Continuous Class-B/J (ECB/J) operation, and An innovative bandwidth-extended matching network.

Rather than depending on conventional amplifier design techniques that impose strict harmonic constraints and restrict bandwidth, this strategy employs a more adaptable concept known as ECB/J mode. Essentially, this approach enables the amplifier to function effectively even when impedance conditions are variable. It broadens the range of impedance values (termed the "design space"), facilitating the achievement of wideband performance. A significant benefit of this technique is its ability to allow the fundamental and second harmonic impedances to overlap, which is crucial for multi-octave functionality.

Nonetheless, merely having an expansive design space is insufficient. The primary challenge with wideband amplifiers is that the optimal impedance varies with frequency. This fluctuation complicates the design of a matching network that performs well across the entire frequency range. To address this issue, the authors propose a novel type of matching network capable of accommodating multiple frequencies simultaneously.

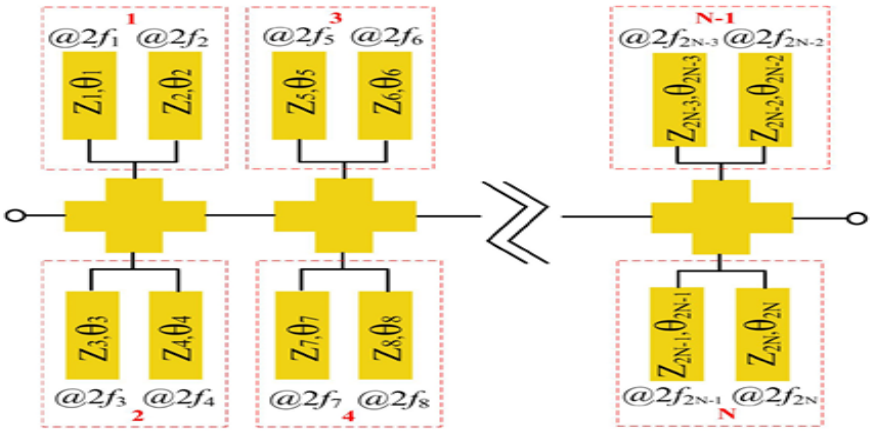


Figure 2.5: Unique Topology

The fundamental concept of this matching network involves segmenting the entire frequency spectrum into several key points and designing the circuit to meet impedance requirements at all these points

concurrently. This study identifies six frequency points throughout the band. The matching network is constructed using various transmission lines and stubs to ensure the correct impedance is achieved at each of these frequencies. This methodology is referred to as multi-frequency or multi-point matching, which aids in sustaining optimal performance across a broad range.

To implement this, the authors utilize a unique configuration comprising multiple branches with open stubs, as illustrated in Figure 2.5. Each branch plays a crucial role in managing impedance at designated harmonic frequencies. By meticulously selecting the lengths and impedances of these transmission lines, the circuit can effectively regulate both fundamental and second harmonic frequencies at the same time. This capability is essential, as effective harmonic management significantly enhances efficiency.

2.2.4 High-Efficiency High-Power Wideband Power Amplifier Design With Hybrid Class AB[5]

This paper presents a method aimed at developing a wideband, high-efficiency power amplifier by meticulously balancing three key elements: efficiency, bandwidth, and distortion. Rather than relying solely on conventional amplifier classes, the authors propose a hybrid Class A/AB design that operates between Class A and Class AB modes to achieve an optimal compromise.

A central theme of this research is the exploration of the interplay between current conduction angle (CCA), bandwidth (BW), and harmonic distortion (HD). Typically, transitioning an amplifier from Class A to Class AB enhances efficiency but leads to increased distortion. However, the authors do not merely accept this compromise; they conduct a thorough analysis of the distortion introduced and its impact on bandwidth.

To facilitate this analysis, they first develop a simplified transistor model that behaves nearly linearly while still reflecting the influence of conduction angle. As illustrated in Figure 2.6, they

apply a sinusoidal input signal and process the output through a band-pass filter (BPF) that simulates the characteristics of a real amplifier output network. This setup helps them study how different conduction angles affect distortion across different bandwidths.

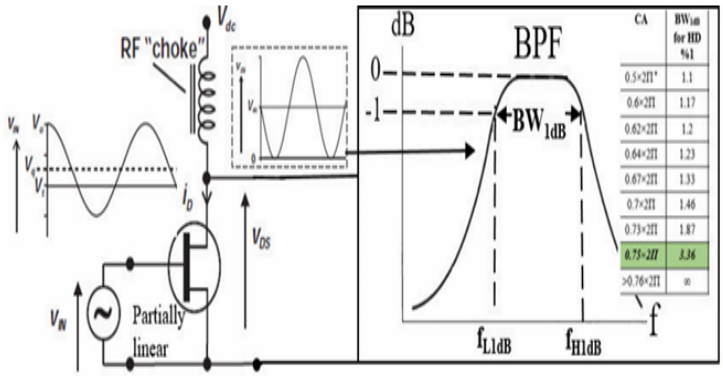


Figure 2.6: Block diagram illustrating analysis of CCA-BW based on HD

After determining the optimal bias point, the subsequent task is to design the amplifier circuit itself. This process includes the development of the input matching network (IMN) and the output matching network (OMN). These networks play a crucial role in ensuring that the transistor encounters the appropriate impedance throughout the entire frequency spectrum.

To achieve wideband performance, a stepped impedance matching method utilizing Chebyshev response is employed. Essentially, this approach involves the use of several transmission lines with varying impedances to smoothly transition the impedance across a broad frequency range. Given that the transistor's gain fluctuates within the band, a gain flattening technique is also implemented, where the matching network is fine-tuned at various frequency segments to maintain a stable gain.

Chapter 3

Design of 10W Power Amplifier

3.1 Introduction

This chapter describes the complete schematic design and simulation methodology of the proposed wideband power amplifier. The design is based on the Extended Continuous Class E (ECCE) mode, which enables multi-octave operation by extending the impedance design space of conventional Class E amplifiers. The implementation is carried out using ADS (Advanced Design System) and validated through harmonic balance and S-parameter simulations.The methodology follows a structured approach that includes:

1. Theoretical impedance derivation
2. Load selection at intrinsic reference plane (IRP)
3. Mapping to extrinsic reference plane (ERP)
4. Matching network design
5. Full schematic implementation

3.2 ECCE Mode-Based Design Approach[1]

The foundation of this design lies in the ECCE mode, where the transistor operates as a switching device under Zero Voltage

Switching (ZVS) and Zero Voltage Derivative Switching (ZVDS) conditions. These conditions minimize the overlap between voltage and current, thereby improving efficiency.

Unlike conventional Class E design, the ECCE method introduces a resistive component in the second harmonic impedance, which creates an overlap between:

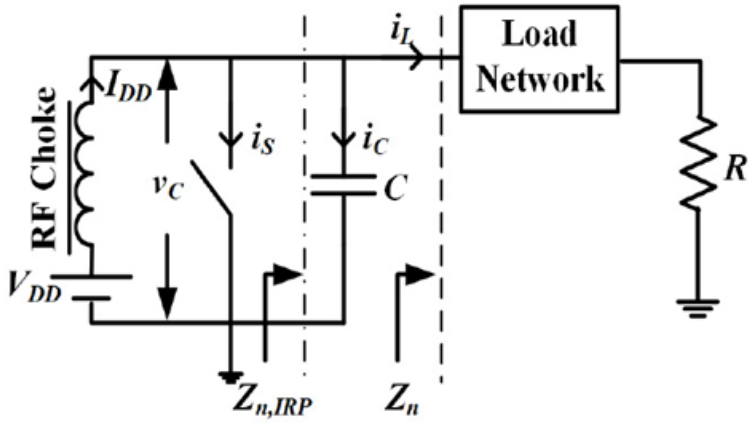


Figure 3.1: Basic circuit configuration of extended continuum of class E

- Fundamental impedance (Z)
- Second harmonic impedance (Z)

This overlap is the key reason why multi-octave bandwidth becomes possible.The overlapping region allows the second harmonic load at a lower frequency to act as the fundamental load at a higher frequency. This concept forms the backbone of the wide band design.

3.2.1 Determination of Target Impedances (IRP Loads)

The determination of target impedances at the Intrinsic Reference Plane (IRP) is one of the most important steps in the design of the wideband ECCE power amplifier. In this stage, the required fundamental, second harmonic, and third harmonic impedances are calculated so that the transistor operates with high efficiency over a wide frequency range. The IRP loads are obtained based on the

ECCE theoretical equations derived using Zero Voltage Switching (ZVS) and Zero Voltage Derivative Switching (ZVDS) conditions. The design parameters such as phase angles ϕ_1 and ϕ_2, design factor δ, and efficiency η are selected carefully to obtain suitable impedance values. The overlap between the fundamental impedance $Z_{1,IRP}$ and second harmonic impedance $Z_{2,IRP}$ enables multi-octave operation, which is the key advantage of the ECCE approach. The intrinsic loads are calculated by considering the parallel combination of the load impedance and the transistor output capacitance. These target impedance values are later mapped to the Extrinsic Reference Plane (ERP) by including package parasitics and device capacitances. The obtained IRP loads provide the required design targets for developing the broadband matching network of the power amplifier.

The obtained final Z_1 and Z_2 equations by the ratio of capacitor voltage and load current at first and second harmonics are given below (3.1) and (3.2).

$$\begin{aligned} Z_1 = \Bigg[& 12I_{01}\left(\pi \sin\phi_1 + 2\cos\phi_1\right) - 24\sin^2\phi_1 \\ & + 8I_{21}\left(\cos\phi_1\cos\phi_2 + 2\sin\phi_1\sin\phi_2\right) \\ & + j\Bigg(6\pi + 12I_{01}\left(\pi\cos\phi_1 - 2\sin\phi_1\right) - 12\sin 2\phi_1 \\ & \quad + 8I_{21}\left(2\cos\phi_1\sin\phi_2 - \sin\phi_1\cos\phi_2\right)\Bigg)\Bigg] \Big/ 12\pi\omega C \end{aligned} \tag{3.1}$$

$$\begin{aligned} Z_2 = \Big[& -4\big(2\cos\phi_1\cos\phi_2 + \sin\phi_1\sin\phi_2\big) \\ & + j\big(3\pi I_{21} + 4(2\cos\phi_1\sin\phi_2 - \sin\phi_1\cos\phi_2)\big)\Big] / 12\pi\omega C I_{21} \end{aligned} \tag{3.2}$$

3.2.2 Frequency Mapping for Multi-Octave Operation

Frequency mapping is an important process used in the ECCE power amplifier design to achieve continuous operation over multiple octaves of bandwidth. In this approach, the operating frequency

range is divided into different octaves, and suitable impedance conditions are assigned to each frequency band. The overlap between the fundamental impedance and second harmonic impedance allows the amplifier to maintain efficient operation across wide frequency ranges. For example, the second harmonic impedance at a lower frequency behaves like the fundamental impedance at a higher frequency, which helps in extending the bandwidth beyond a single octave. The design variables such as ϕ_1, δ, and efficiency η are mapped with frequency to obtain proper impedance trajectories across the operating band. Using this method, the ECCE amplifier is capable of maintaining good output power, gain, and efficiency over a multi-octave frequency range. Frequency mapping also simplifies the design of the matching network by ensuring smooth impedance transition between adjacent frequency bands. This mapping strategy is shown in Figure.3.2

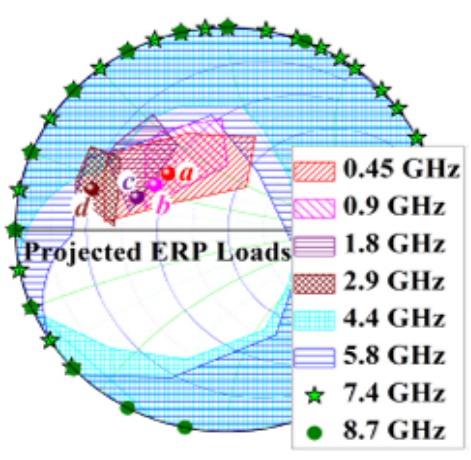


Figure 3.2: Loads of ECCE projected on ERP

3.2.3 Conversion from IRP to ERP Loads

In practical RF power amplifier design, the transistor does not directly observe the intrinsic reference plane (IRP) impedances because of the presence of package parasitics, bonding wire inductances, and device capacitances. Therefore, the calculated IRP loads must be converted into Extrinsic Reference Plane (ERP) loads before implementing the matching network. This conversion process helps in obtaining the actual impedance values seen at the external ter-

minals of the transistor. During this stage, the transistor output capacitance and parasitic elements are included in the impedance calculations to achieve accurate load conditions. The IRP load is mathematically transformed by considering the parallel combination of the load impedance and capacitive reactance. This mapping from IRP to ERP ensures that the designed matching network provides the required harmonic terminations at the transistor terminals under practical operating conditions. The ERP loads obtained after conversion are then used for designing the broadband input and output matching networks of the power amplifier.

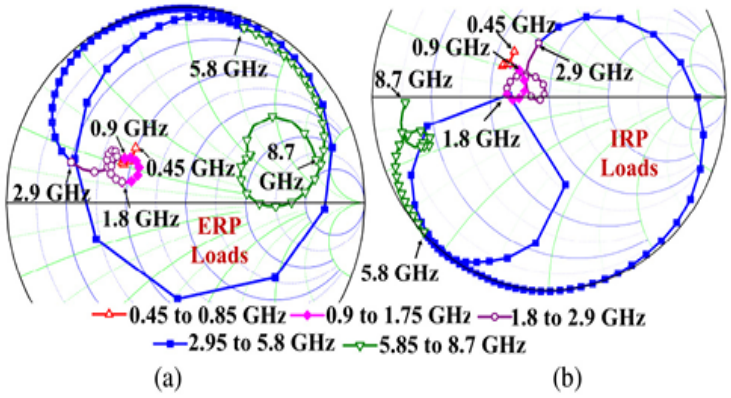


Figure 3.3: Mapped ERP (a) and IRP (b) loads

3.3 Schematic of Direct Implementation

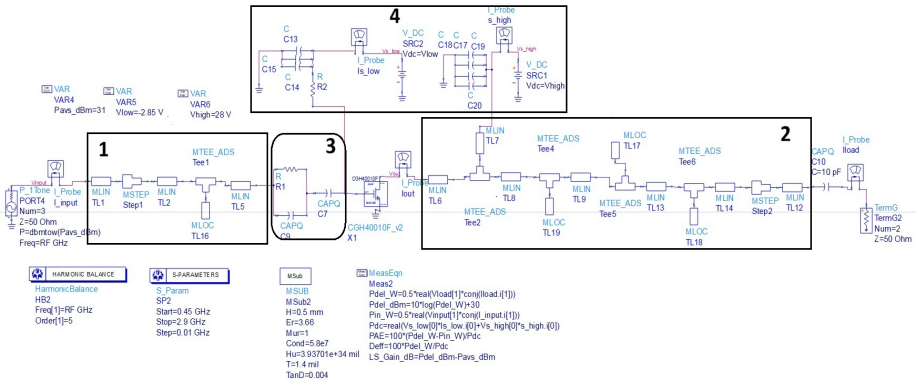


Figure 3.4: 0.45 – 2.9 GHz Wide band power amplifier schematic

The above power amplifier schematic consists of four different blocks.They are 1.Input Matching Network, 2. Output Matching Network, 3. Stability Network and 4. Biasing Network.

3.3.1 Input Matching Network:

The input matching network is the first stage of the power amplifier and plays a crucial role in ensuring efficient signal transfer from the source to the transistor. In this design, the RF signal is applied through a 50Ω input port and then passes through a series of microstrip transmission lines (MLIN) and impedance transition elements (MSTEP). Since the input impedance of the GaN transistor is not naturally equal to 50Ω and varies with frequency, this network is carefully designed to transform the standard source impedance to the required transistor input impedance over the entire operating bandwidth.

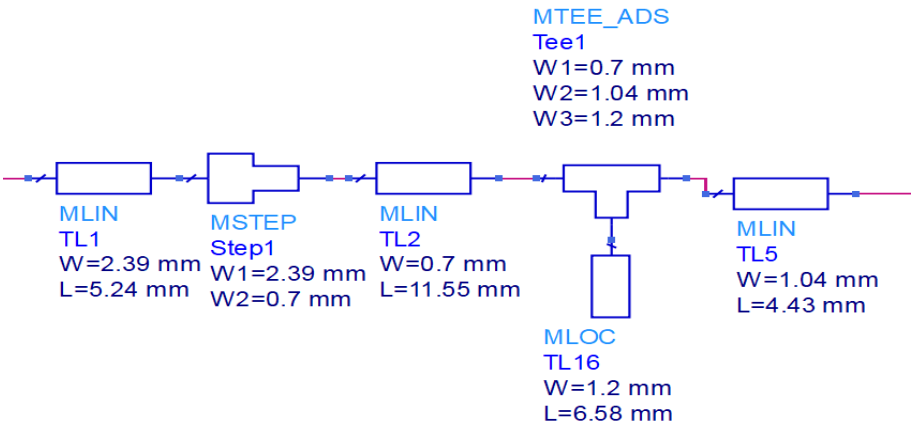


Figure 3.5: Input Matching Network

Capacitors and transmission lines are used together to achieve fine tuning and broadband matching. The use of distributed elements such as microstrip lines helps in maintaining consistent performance across a wide frequency range, which is essential for wideband amplifier operation. Overall, the input matching network minimizes signal reflection (S11), maximizes power transfer, and ensures that the transistor receives sufficient input power for proper amplification.

3.3.2 Output Matching Network:

On the other hand, the output matching network is more complex and plays a critical role in determining the overall performance of the amplifier. Its primary purpose is to transform the transistor's output impedance to a standard 50Ω load across the entire bandwidth while also controlling harmonic components. In this design, the output network is implemented using multiple sections of microstrip lines, T-junctions (MTEE), and open stubs (MLOC), forming a distributed broadband matching structure. Unlike narrowband amplifiers, where matching is done at a single frequency, this network is designed to provide proper impedance at multiple frequencies simultaneously.

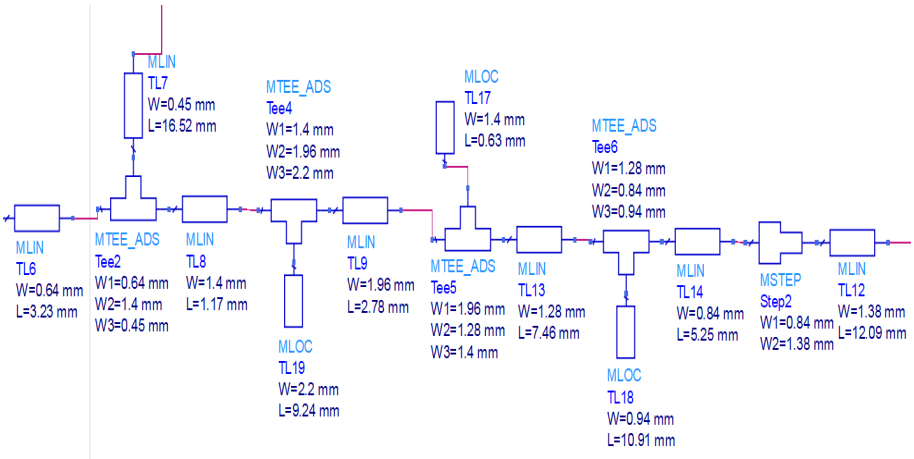


Figure 3.6: Output Matching Network

According to the methodology, the output network must realize specific impedance conditions at the **fundamental, second harmonic, and third harmonic frequencies**, which are derived using ECCE mode theory . The presence of a resistive component in the second harmonic impedance allows overlap between fundamental and harmonic loads, enabling multi-octave operation. The open stubs and transmission lines are carefully designed to control these harmonic impedances, improving efficiency by shaping voltage and current waveforms. Overall, the output matching network ensures maximum power transfer, high efficiency, and stable wideband operation, making it the most critical and sophisticated part of the amplifier design.

3.3.3 Stability and Biasing Network

In this power amplifier design, the biasing and stability networks play a very important role in ensuring that the transistor operates properly and the amplifier remains stable across the entire wide frequency range. The GaN transistor (CGH40010F) is biased using a drain voltage of around 28 V and a gate voltage of approximately –2.85 V, as also mentioned in the paper design section . The biasing network is carefully designed using DC sources, RF chokes, and capacitors so that it supplies the required DC voltages to the transistor without allowing RF signals to leak into the DC path. The RF choke (implemented using high-impedance transmission lines or inductive paths) allows DC to pass while blocking RF signals, and the bypass capacitors provide a low-impedance path to ground for RF components, ensuring clean biasing. This separation of RF and DC paths is essential to maintain proper amplifier operation and avoid unwanted signal distortion.

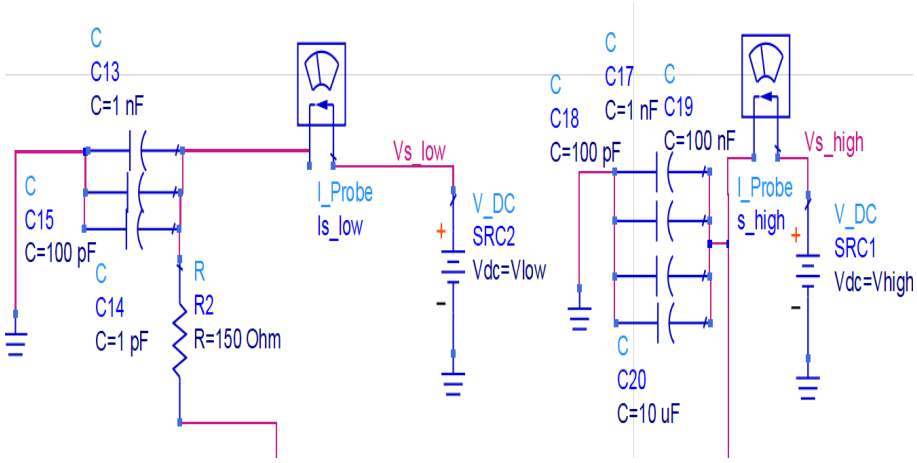


Figure 3.7: Biasing Network

At the same time, the stability network ensures that the amplifier does not oscillate at any frequency within or outside the operating band. Since wideband amplifiers are more prone to instability due to gain variations and feedback effects, resistors and small capacitive elements are introduced near the input and bias paths to damp unwanted oscillations. In your schematic, components like series resistors and RC networks help in improving stability by reducing

excessive gain at low or high frequencies. These elements prevent the transistor from self-oscillating when no input signal is present or when reflections occur. Overall, the biasing network ensures correct operating conditions of the transistor, while the stability network guarantees reliable and stable amplifier performance across the entire wideband range.

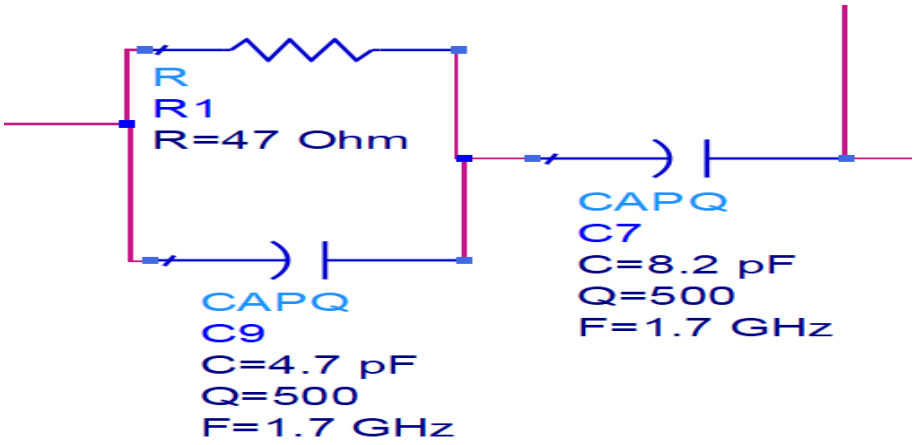


Figure 3.8: Stability Network

3.4 S-Parameter Analysis

The **S-parameter results** of the power amplifier obtained from ADS simulation, which are used to evaluate the small-signal performance of the design. These parameters mainly include **S21 (gain), S11 (input return loss), and S22 (output return loss)** over the operating frequency range.

In the Figure 3.9 the gain (S21) is shown by the blue curve. It can be observed that the gain is relatively stable across the frequency range from **0.45 GHz to around 2.9 GHz**, with a peak value of approximately **13.56 dB at 1.7 GHz**. This indicates that the amplifier provides consistent amplification over a wide bandwidth. The input return loss (S11), shown in magenta, remains below –2 dB for most of the band, which means that the input matching is good and 37% of the power is actually delivered to the amplifier. Similarly, the output return loss (S22), shown in cyan, also stays well below –10 dB across a major portion of the band, indicating

proper output matching. However, some variations can be seen at higher frequencies, where matching slightly degrades, which limits the bandwidth to around 2.9 GHz in the original design.

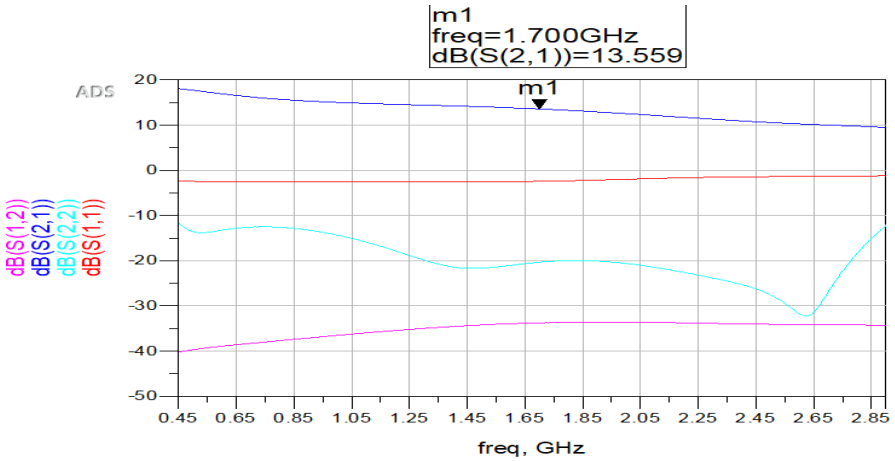


Figure 3.9: 'S' Parameters

3.5 Large Signal Analysis Performance

The below graphs represent the **large-signal performance of the power amplifier obtained from direct implementation**, including efficiency, output power, gain, and waveform behaviour. These results are very important because they show how the amplifier performs under real operating conditions.

The Figure. 3.10 **(PAE and Drain Efficiency vs Frequency)**shows how efficiently the amplifier converts DC power into RF output power. It can be observed that both **PAE and drain efficiency remain above 55% across most of the band**, with a peak efficiency of around **65–66% near 1.9–2.0 GHz**. This indicates that the amplifier is highly efficient over a wide frequency range. The smooth variation of efficiency shows that the ECCE design approach maintains good performance across multiple frequencies. As mentioned in the paper, ECCE mode helps achieve high efficiency by controlling harmonic components and minimizing power loss.

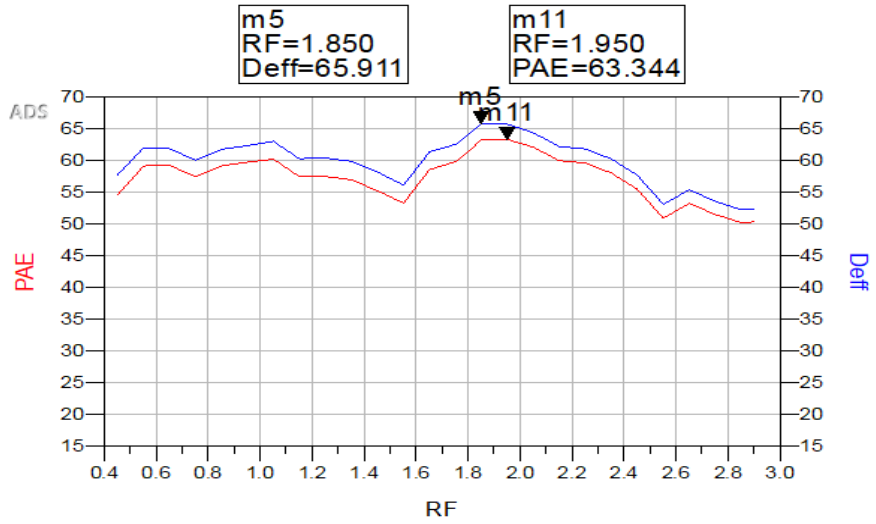


Figure 3.10: Performance of (PAE and Deff) Vs Frequency (GHz)

In Figure 3.11 (PAE and Drain Efficiency vs Input Power) shows that both **PAE and drain efficiency increase as input power increases**. Initially, efficiency is low at lower input power levels, but as the amplifier approaches its operating region, efficiency improves significantly. At around **31 dBm input power**, the drain efficiency reaches about **62%**, and PAE is around **58.8%**. This indicates that the amplifier is operating close to its optimal region. After this point, efficiency tends to saturate, which is expected in power amplifiers.

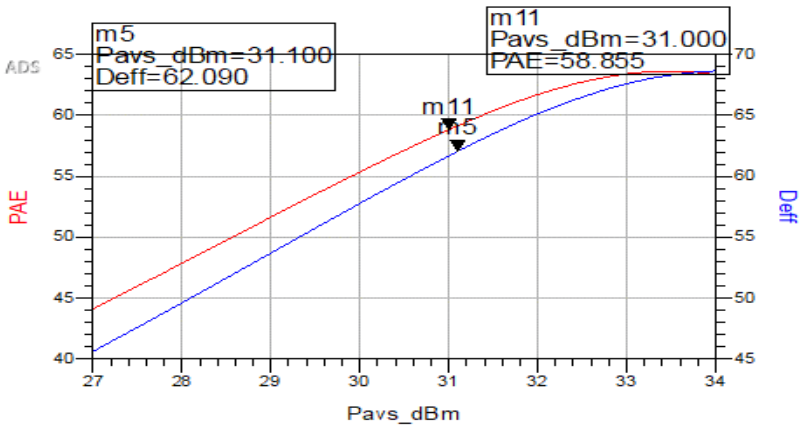


Figure 3.11: Performance of (PAE and Deff) Vs Input Power (dBm)

The Figure 3.12 (Output Power and Large Signal Gain vs Frequency) shows the output power (Pdel) and large-signal gain of the amplifier(LS_Gain). The output power is around**41 dBm near 2 GHz**, which is close to the expected performance of the design. The gain is around **10 dB**,which is slightly lower than small-signal gain, as expected due to nonlinear effects at high power. The output power remains fairly stable across the band, indicating good power performance. A slight drop at higher frequencies is normal due to device limitations and matching losses.

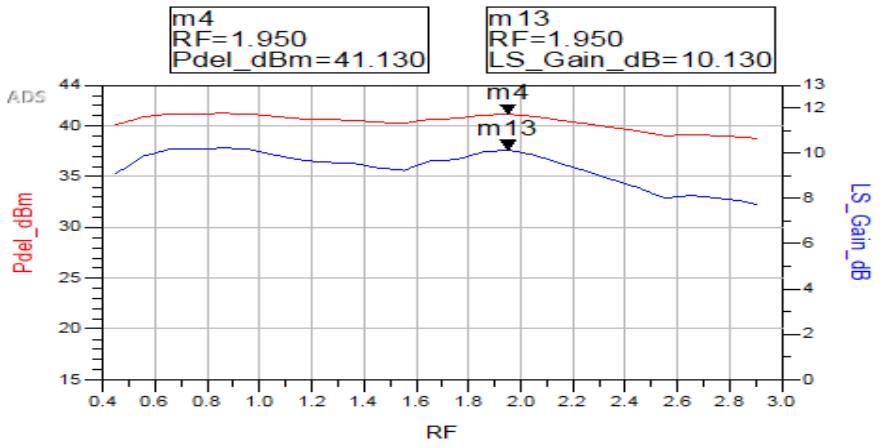


Figure 3.12: Performance of (Pdel and LS_Gain) Vs Frequency (GHz)

In the **Figure 3.13 (Output Power and Gain vs Input Power)** shows how output power and gain change with increasing input power. The output power increases steadily and reaches around **40.6 dBm at 31 dBm input**, indicating good power amplification. At the same time, the gain gradually decreases as input power increases, which is a normal effect known as **gain compression**. The gain at this point is around **9.59 dB**, which is slightly lower than small-signal gain due to nonlinear operation.The graph clearly shows the transition of the amplifier from the linear region toward the saturation region. Even though slight gain compression is observed, the amplifier still maintains stable output power performance across the operating range. The smooth variation of the curves indicates proper impedance matching and stable bias operation. The obtained

results confirm that the amplifier can deliver good power performance while maintaining acceptable gain characteristics over the selected operating conditions.

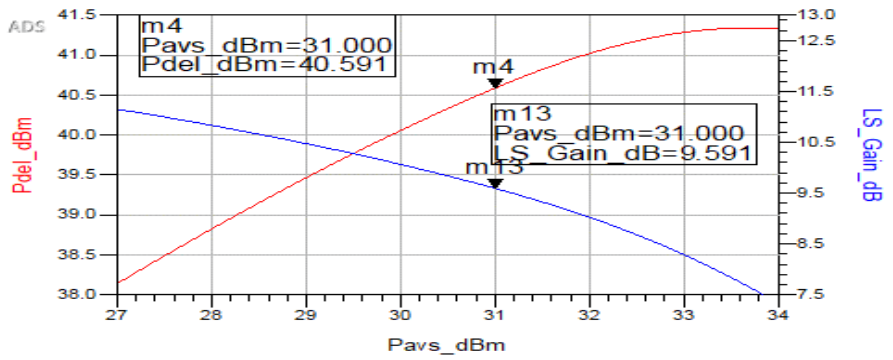


Figure 3.13: Performance of (Output Power and LS_Gain) Vs Input Power (dBm)

In the Figure 3.14 **(Voltage and Current Waveforms at 0.45 GHz)** is very important for understanding the working principle of the amplifier. It shows **the drain voltage and current waveforms**, where it can be clearly seen that they do not overlap significantly. This is a key feature of **ECCE mode operation**, where the transistor behaves like a switch. Because voltage is low when current is high and vice versa, power loss is minimized. This condition is known as **Zero Voltage Switching (ZVS) and Zero Voltage Derivative Switching (ZVDS)**, which helps in achieving high efficiency.

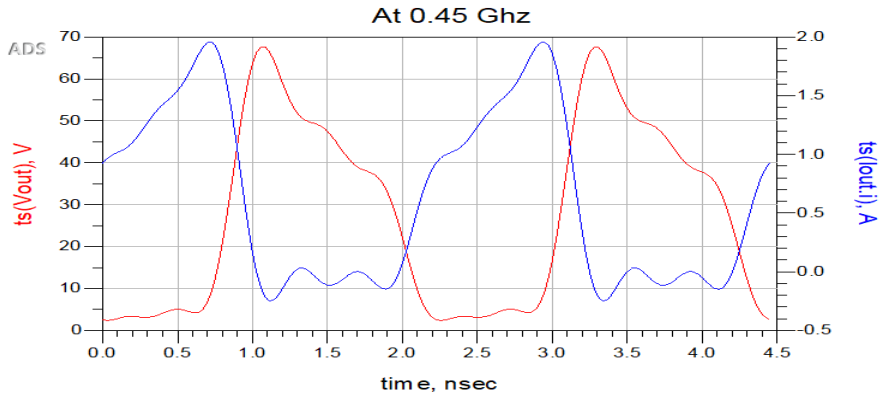


Figure 3.14: Simulated IRP waveforms at 0.45 GHz

Overall, these graphs confirm that the amplifier achieves **high efficiency (above 60%), good output power (41 dBm), and proper waveform behaviour**, validating the effectiveness of the ECCE-based design.

Chapter 4

Experimental Validation of 10W PA

4.1 Ki Cad Schematic and Layout of ECCE PA

The PCB layout for the proposed power amplifier was designed using KiCad software, following a systematic process to convert the schematic into a practical hardware implementation. The complete procedure involves schematic creation, footprint assignment, board layout, routing, and verification.

The process begins with the schematic design, as shown in the first figure. In KiCad's schematic editor, all components such as the transistor (Q1), resistors (R1, R2, R3), capacitors (C1–C6), and connectors (J1–J4) are placed and connected based on the circuit design. The input and output are provided through coaxial connectors, while proper grounding is ensured using GND symbols. Special attention is given to the biasing network, where resistors and capacitors are arranged to provide stable gate and drain voltages. After completing the schematic, an Electrical Rule Check (ERC) is performed to identify and correct connection errors.

Once the schematic is verified, the next step is assigning footprints to each component. Each schematic component is linked to a physical footprint that represents its actual size and pad configuration on

the PCB. For RF design, suitable footprints are selected to ensure accurate implementation of high-frequency signals. The transistor footprint is chosen carefully to match the package of the device, and connectors are assigned footprints compatible with SMA or pin connectors.

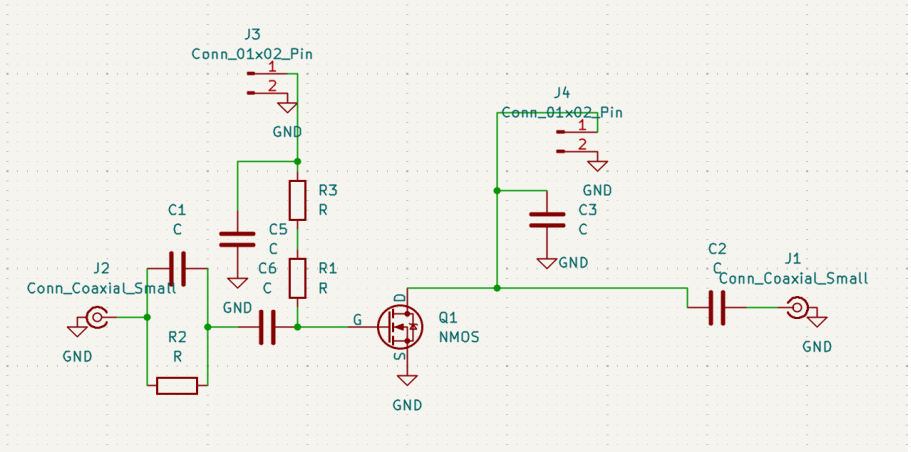


Figure 4.1: Ki Cad Schematic of ECCE PA

After footprint assignment, the design is transferred to the PCB layout editor. In this stage, all components are placed on the board as shown in the second figure. The placement is done carefully to minimize signal path length and reduce losses. The transistor is placed at the center, with input and output networks arranged on either side to maintain symmetry and proper signal flow. The biasing components are placed close to the transistor to reduce unwanted parasitic effects.

The next step is routing of tracks, where electrical connections are converted into copper traces. For RF signals, wider tracks are used to maintain proper impedance, and microstrip-like routing is followed. The input and output paths are kept as short and straight as possible to reduce reflections and losses. Grounding is an important aspect in RF design, so a solid ground plane is implemented, and multiple vias are used to ensure good grounding and reduce noise. In the layout, the red areas represent copper traces, while the blue region indicates the ground plane.

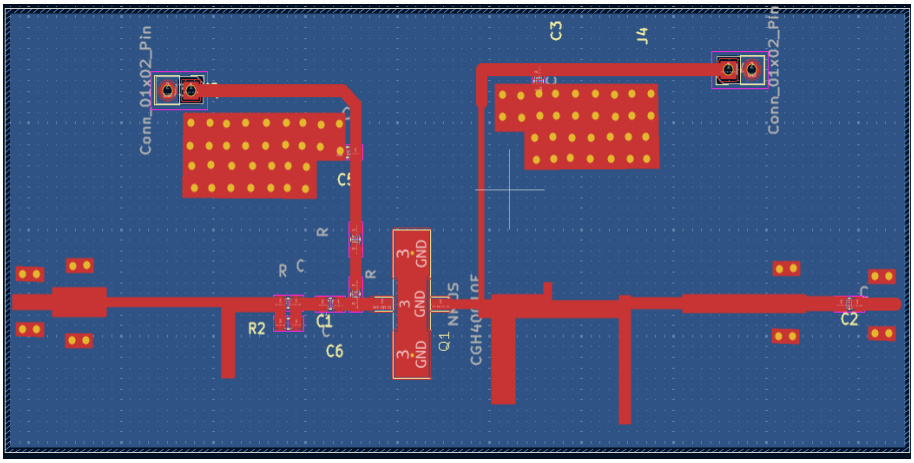


Figure 4.2: Ki Cad Layout of ECCE PA

Following routing, a Design Rule Check (DRC) is performed to ensure that all spacing, width, and clearance rules are satisfied. This step helps in avoiding manufacturing issues. Any errors found are corrected before finalizing the design.

Finally, the PCB layout is reviewed for practical considerations such as component accessibility, heat dissipation, and connector placement. Once verified, the design is exported as Gerber files, which are used for PCB fabrication.Overall, the KiCad design process ensures that the schematic is accurately translated into a physical layout while maintaining RF performance, proper grounding, and manufacturability.

4.2 PCB Design and Layout

The fabrication and assembly of the proposed power amplifier involve converting the designed PCB layout into a physical hardware circuit and carefully mounting all components to ensure proper operation. The fabricated PCB, as shown in the figure, is developed on a suitable RF substrate with a continuous ground plane and copper traces that implement the designed microstrip lines.

The fabrication process begins with exporting the PCB design from KiCad in the form of Gerber files, which are then used by the PCB manufacturer to produce the board. The board is fabricated using standard processes such as etching, drilling, and copper

plating, where unwanted copper is removed to form the required circuit pattern. The green coating visible on the board is the solder mask, which protects the copper traces and prevents short circuits. After fabrication, the board is cleaned and prepared for component assembly.

The next step is the assembly of components. The main active device, which is the GaN transistor (CGH40010F), is mounted at the center of the board. This placement is important to maintain symmetry between the input and output matching networks. The transistor is carefully soldered to ensure good electrical contact and proper heat dissipation. Passive components such as resistors and capacitors (used for matching and biasing) are soldered close to the transistor to minimize parasitic effects. These components are placed exactly as per the layout to maintain the designed impedance characteristics.

The RF input and output are connected using SMA connectors, which are mounted on both sides of the PCB. These connectors allow easy connection to measurement instruments such as signal generators and spectrum analyzers. Proper soldering of these connectors is very important to avoid signal loss and reflection. The microstrip lines connecting the transistor to the SMA connectors are kept short and uniform to maintain impedance matching.

The biasing network is implemented using pin connectors (J3 and J4), which provide the required gate and drain voltages. Decoupling capacitors are placed near these bias points to filter out noise and ensure stable DC supply. The ground plane is connected using multiple vias and large copper areas to ensure good grounding and reduce unwanted noise. During assembly, special care is taken to avoid common issues such as:

- Poor soldering joints
- Excess solder causing short circuits
- Misalignment of components

Finally, the assembled board is visually inspected and tested for continuity before applying power. The completed hardware, as shown in the figure, clearly demonstrates the practical implementation of

the designed wideband power amplifier.

Overall, the fabrication and assembly process ensures that the designed schematic and PCB layout are accurately realized in hardware while maintaining proper RF performance and reliability.

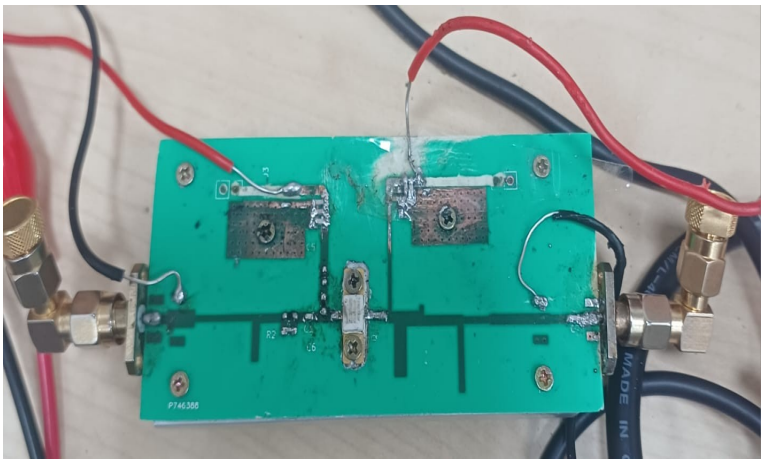


Figure 4.3: Fabricated Power Amplifier

4.3 Measurement Setup and Verification

The entire experimental setup utilized to test the manufactured PCB is depicted in the second figure. The configuration consists of:

- Spectrum analyzer
- Signal Generator
- DC power supply
- Fabricated power amplifier PCB
- 6 dB Attenuator

SMA connections are used to feed the RF signal produced by Signal Generator into the amplifier PCB's input. The attenuator is connected to the amplifiers output.The spectrum analyzer, which examines the amplified signal properties including power and frequency responsiveness, is attached to the attenuator output. The gate and drain voltages needed to correctly bias the transistor are provided by the DC power supply. This configuration validates the hardware's realistic operation and allows for real-time amplifier performance evaluation.

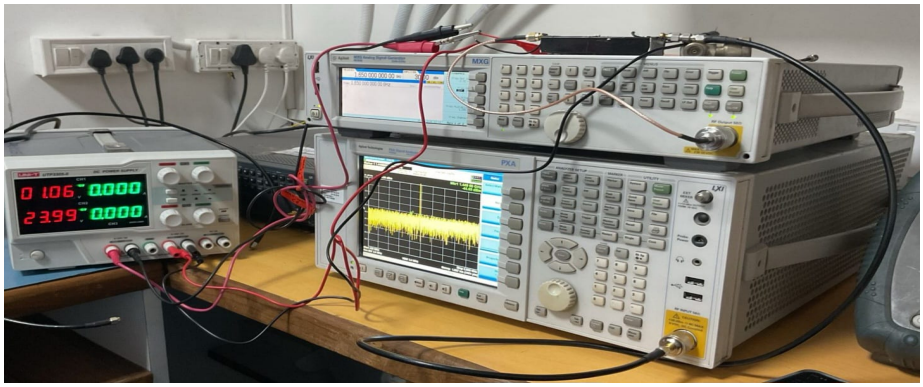


Figure 4.4: Complete Measurement Setup

The figure 4.5 shows the experimental measurement setup using a spectrum analyzer to observe the output signal of the RF power amplifier. The spectrum analyzer is used to measure the output power spectrum of the amplifier over the operating frequency range. In the displayed measurement, a strong output signal is observed at approximately **1.449 GHz**. The marker on the spectrum analyzer indicates a measured output power of around **34.2 dBm**. During the measurement process, a **6 dB attenuator** and approximately **4 dB cable/wire loss** were present between the amplifier output and the spectrum analyzer input to protect the instrument from excessive RF power and reduce measurement reflections. Therefore, the actual output power generated by the amplifier is higher than the displayed measured value. By including both attenuation and cable losses, the estimated amplifier output power becomes approximately:**34.2dBm+6dB+4dB=44.2dBm**

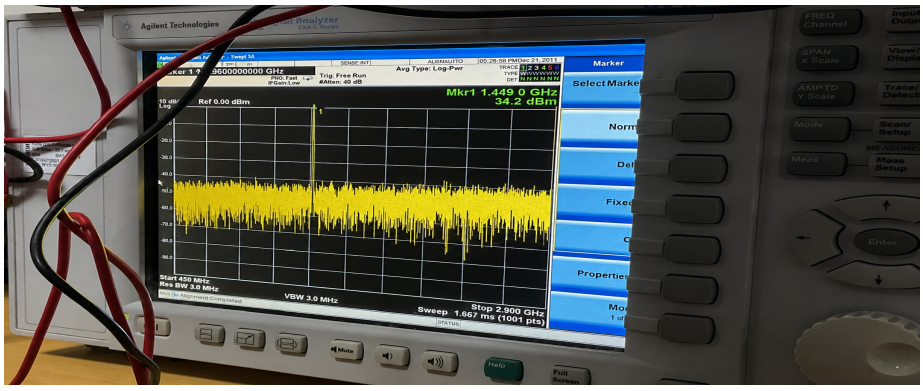


Figure 4.5: Output Power at 1.5GHz in Spectrum Analyzer

This indicates that the proposed amplifier is capable of delivering high RF output power at the selected operating frequency. The sharp spectral peak observed on the analyzer confirms proper amplification and stable operation of the power amplifier.The measured hardware results closely agree with the simulated performance, thereby validating the effectiveness of the proposed ECCE-based wideband power amplifier design.



Figure 4.6: Complete Measurement Setup

The DC bias voltages applied to the amplifier during testing are depicted in the above figure 4.6. Both are necessary for the transistor:

- A gate voltage that is negative (around –2.9 V)
- A drain voltage that is positive (around 28 V)

The transistor's operating current during amplifier operation is shown by the current values that are presented. Because it guarantees that the transistor runs in the appropriate ECCE region, proper biasing is crucial. Inaccurate bias conditions can harm the equipment or decrease efficiency. For the amplifier to operate steadily and safely, the power supply configuration is crucial.

4.4 Hardware Results:

The Figure 4.7 presents the comparison between the simulated output power and the measured hardware output power of the directly implemented wideband RF power amplifier over the operating

frequency range. The black curve represents the simulated output power obtained from ADS simulation, while the red curve represents the experimentally measured output power obtained from hardware testing. From the graph, it can be observed that the simulated output power remains relatively stable around 40 dBm to 41 dBm across the complete operating bandwidth. The measured output power also follows a similar trend, which validates the practical implementation of the amplifier design.

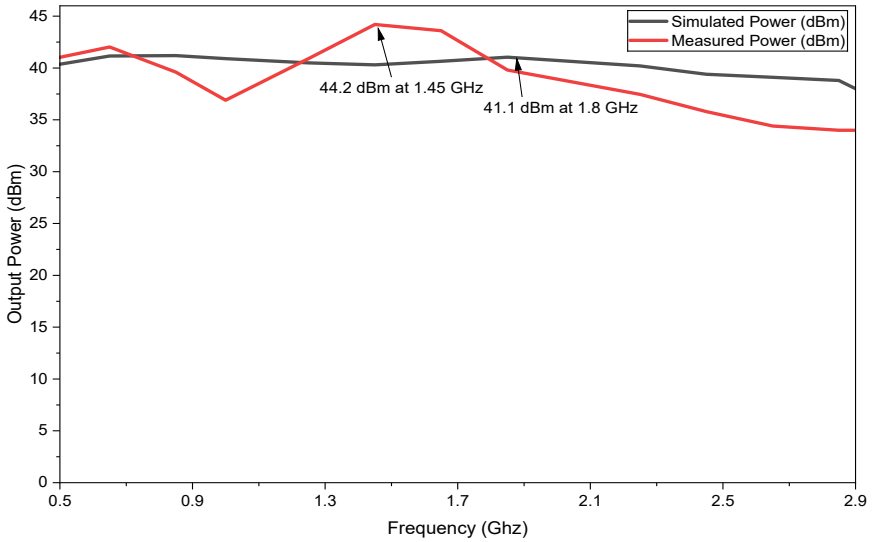


Figure 4.7: Output Power Vs Frequency (GHz)

The hardware measurement shows a maximum output power of approximately **44.2 dBm** near **1.45 GHz**, indicating strong amplification performance at this frequency. Around **1.8 GHz**, the measured output power is nearly **41.1 dBm**, which closely matches the simulated result. Small variations between simulated and measured curves are expected in practical RF hardware due to PCB parasitic effects, connector losses, fabrication tolerances, soldering imperfections, and transmission line discontinuities. At higher frequencies, a gradual reduction in measured output power can be observed because of increased dielectric losses, impedance mismatch, and device parasitic capacitances.Overall, the measured hardware results show good agreement with the simulated performance over

a wide frequency range. The graph confirms that the proposed ECCE-based wideband power amplifier is capable of maintaining high output power across multiple octaves of operation.

The Figure 4.8 presents the comparison between the simulated gain and the measured hardware gain of the directly implemented wideband RF power amplifier over the operating frequency range. The black curve represents the simulated gain obtained from ADS simulation, whereas the red curve represents the experimentally measured gain obtained from hardware testing. From the graph, it can be observed that the simulated gain remains relatively stable across the operating band, with values mostly ranging between 12 dB and 14 dB. The measured gain also follows a similar trend, confirming the successful practical implementation of the amplifier design.

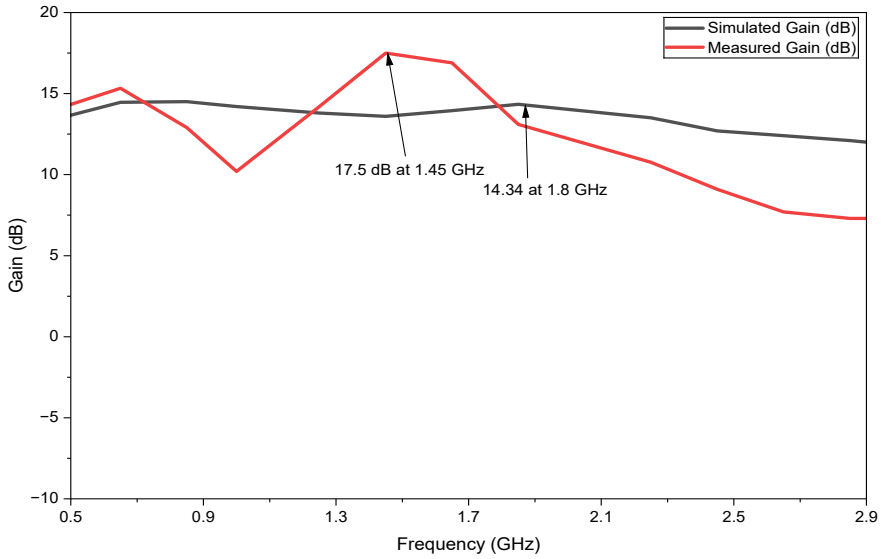


Figure 4.8: Large Signal Gain Vs Frequency (GHz)

The hardware measurement shows a maximum gain of approximately **17.5 dB** near **1.45 GHz**, indicating strong amplification performance at this frequency. Around **1.8 GHz**, the measured gain is nearly **14.34 dB**, which closely matches the simulated value. At lower frequencies, the measured gain is slightly higher than the simulated response, while at higher frequencies a gradual reduction in gain is observed. This reduction mainly occurs because of

practical RF effects such as transmission line losses, PCB parasitic effects, connector losses, impedance mismatch, and device parasitic capacitances. Fabrication tolerances and soldering imperfections can also contribute to slight variations between simulation and hardware results.Despite these practical variations, the amplifier maintains acceptable gain performance across the complete operating bandwidth. Overall, the graph confirms that the implemented power amplifier is capable of providing stable broadband gain performance.

Chapter 5

Bandwidth and Power Enhancement

5.1 Four-Way Power Combiner Based ECCE Power Amplifier Architecture

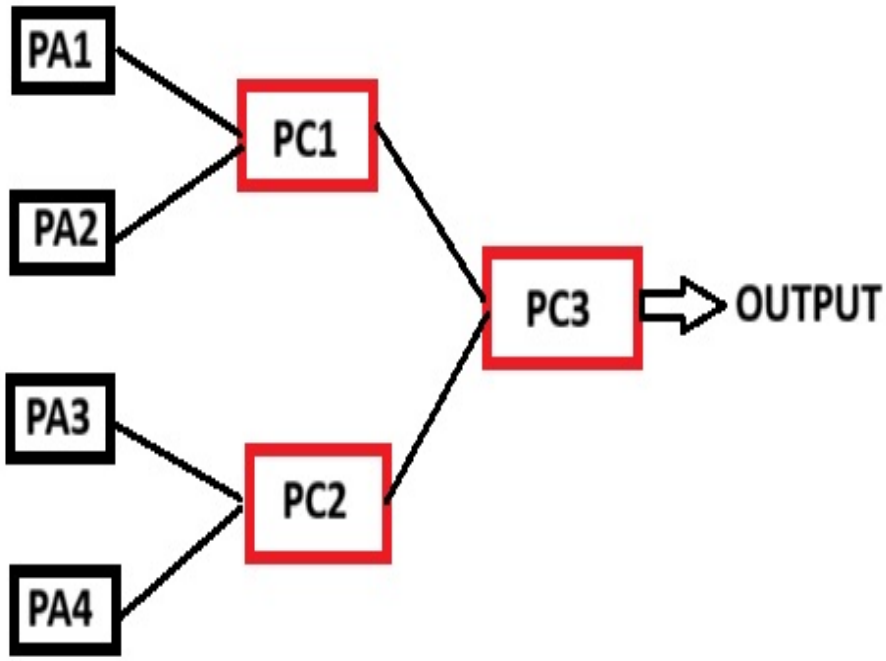


Figure 5.1: Block Diagram of 4-Way Power combiner

The ECCE Power amplifer(PA) which is used earlier in Figure 3.4,this amplifer is used four times in PA1, PA2, PA3 and PA4.The power combiner(PC) as shown in Figure 5.2 is used in PC1,PC2 and PC3.

5.1.1 Four-Way Power Combiner Based ECCE Power Amplifier Architecture

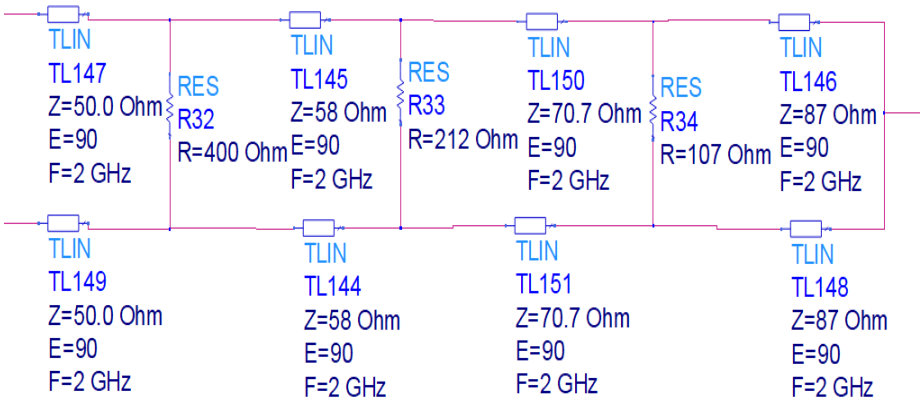


Figure 5.2: Schematic of 4-Way Power combiner

The complete schematic consists of four identical direct implementation ECCE power amplifier blocks connected to a four-way power combiner network. Each amplifier block is designed using the CGH40035 GaN transistor and operates over a wide frequency range to achieve broadband high-power amplification. The outputs of all four amplifier stages are combined together using a microstrip transmission-line based power combining structure in order to obtain higher overall output power while maintaining stable gain and efficiency characteristics.

The power combiner is implemented using multiple quarter-wave transmission line sections and isolation resistors. In the combining network, transmission lines with characteristic impedances of 50 Ω, 58 Ω, 70.7 Ω, and 87 Ω are used to provide proper impedance transformation between the amplifier outputs and the final load impedance. The resistor elements connected between adjacent transmission line

branches improve port isolation and reduce mismatch effects between amplifier modules. These resistors also help in suppressing unwanted reflections and maintaining stable power combining performance over the complete operating bandwidth.

The four ECCE amplifier blocks are connected symmetrically to the combining network to ensure equal power distribution and phase alignment. Proper phase matching is very important in a multi-way power combiner because any phase imbalance can reduce the overall combining efficiency and output power. The transmission line lengths are carefully optimized at the center frequency to maintain constructive power addition at the output port. The combined output is finally terminated with a 50 Ω load impedance to match standard RF measurement systems and communication interfaces.

The implemented four-way power combiner improves the overall output power capability of the amplifier while preserving the wideband characteristics of the ECCE design methodology. The distributed transmission-line architecture also helps in broadband impedance matching and harmonic suppression. By combining the outputs of multiple amplifier cells, the proposed architecture achieves higher power handling capability compared to a single amplifier stage. The overall structure demonstrates good scalability, wideband operation, and stable RF performance suitable for high-power wireless communication and broadband RF transmission applications.This reduces the electrical and thermal stress on an individual transistor, thereby improving device reliability and operational stability. The symmetrical structure of the combiner helps maintain uniform current distribution and phase balance between all amplifier paths. In addition, the transmission-line based implementation provides low insertion loss and supports broadband impedance transformation across the operating frequency range. The use of isolation resistors in the combiner network further minimizes mutual coupling effects and enhances stable wideband power combining performance.

5.1.2 Large Signal Analysis

The graphs illustrate the simulated performance of the proposed four-way combined ECCE wideband power amplifier over the operating frequency range. The Figure 5.3 represents the variation of delivered output power (*Pdel_finaldBm*) and large signal gain (*LS_Gain_dB*) with respect to frequency. From the graph, it can be observed that the amplifier achieves a maximum output power of approximately **47.07 dBm** near **0.64 GHz**. The large signal gain at this frequency is around **18.38 dB**, indicating strong amplification capability after combining the outputs of the four amplifier blocks. The output power remains above 43 dBm across most of the operating band, which confirms the effectiveness of the four-way power combining structure. The gain also remains relatively stable over the complete bandwidth with only gradual reduction at higher frequencies due to increased transmission line losses, parasitic effects, and matching limitations. Small variations in the curves are mainly caused by harmonic interactions and impedance variations within the broadband matching network.

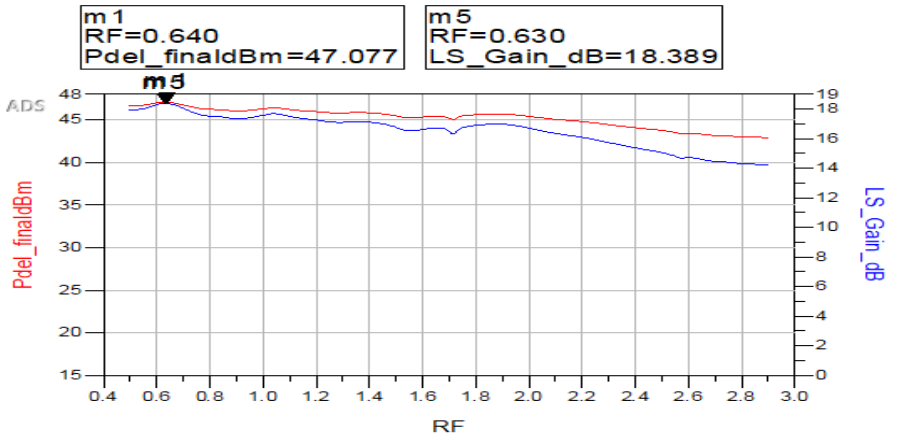


Figure 5.3: (Output Power and Large Signal Gain) Vs Freq (GHz)

The Figure 5.4 shows the variation of *Power Added Efficiency (PAE)* and *Drain Efficiency (Deff)* with frequency for the combined amplifier structure. The amplifier achieves a peak PAE of approximately **62.19%** and drain efficiency of around **62.62%** near **0.58**

GHz. The efficiency remains above 50% across a large portion of the operating band, which demonstrates efficient RF power conversion performance. The close overlap between the PAE and drain efficiency curves indicates that the amplifier operates efficiently with relatively low input drive loss. Some efficiency reduction at higher frequencies is expected due to increased dielectric losses, impedance mismatch, and device parasitic effects. Overall, the obtained results confirm that the proposed four-way combined ECCE power amplifier successfully achieves high output power, good gain, and wideband efficiency performance suitable for broadband RF transmitter applications.

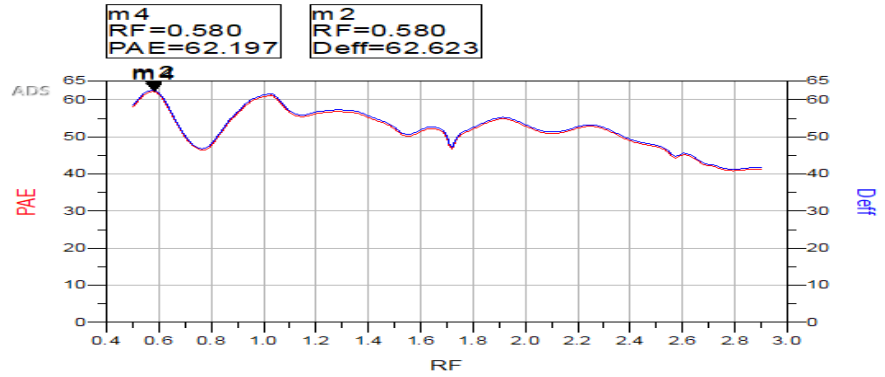


Figure 5.4: (PAE and Deff) Vs Freq (GHz)

5.2 Proposed Wideband High-Power Amplifier

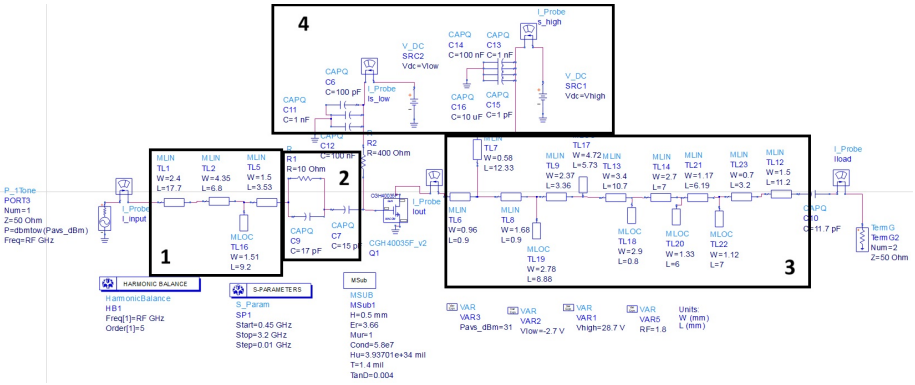


Figure 5.5: 0.45 – 3.2 GHz Wide band power amplifier schematic

The above mentioned blocks in the schematic are:

1. Input Matching Network

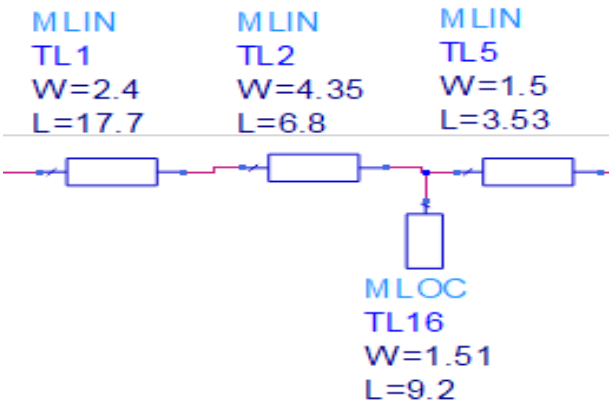


Figure 5.6: Input Matching Network

2. Stability Network

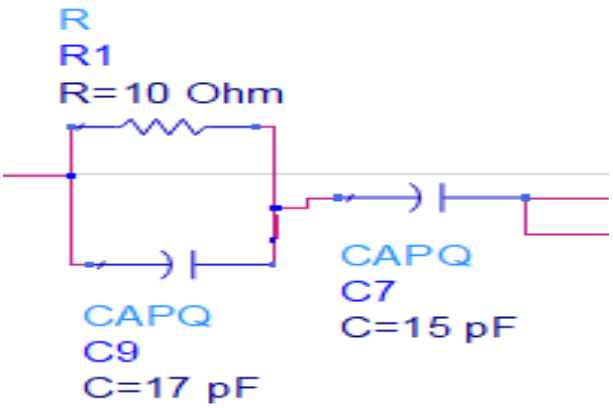


Figure 5.7: Stability Network

3. Output Matching Network

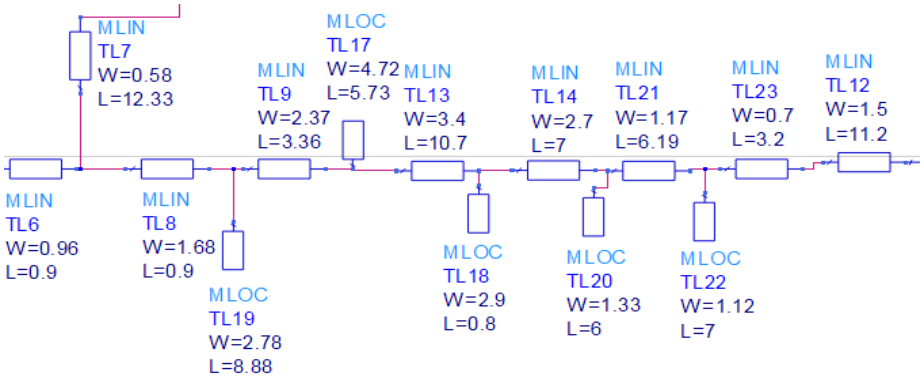


Figure 5.8: Output Matching Network

4. Biasing Network

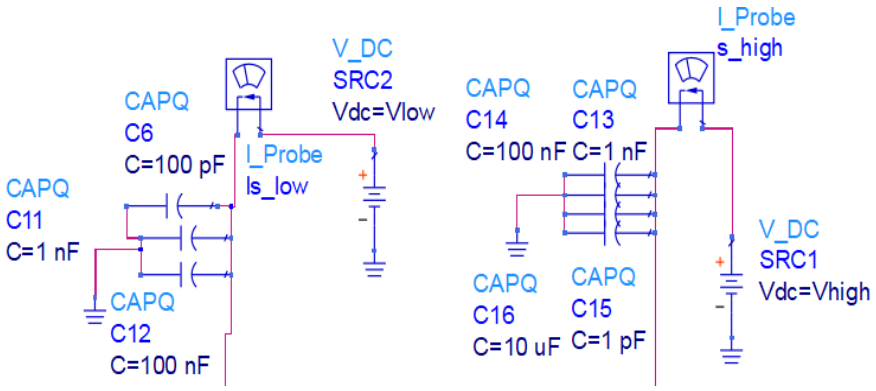


Figure 5.9: Biasing Network

The first major improvement in my design is the addition of two extra stub sections in the output matching network. In the original paper, the output matching network is designed mainly to satisfy the required fundamental and harmonic impedances over the band of 0.45–2.9 GHz. However, achieving wider bandwidth beyond this range is challenging because impedance matching becomes more difficult at higher frequencies. To overcome this limitation, I introduced additional stub elements in the output side.

These stubs act as reactive tuning elements, which help in better controlling impedance variation across frequency. In simple terms, they provide extra flexibility to shape the impedance trajectory so that it continues to follow the required ECCE load conditions even at higher frequencies. Using the necessary equations from reference paper I have calculated transmission line widths and lengths of input

and output matching network with ZL and Zs values CGH40035 device. As a result, my design successfully extends the bandwidth up to 3.2 GHz, which is higher than the maximum frequency achieved in the reference work. This is a significant practical enhancement because wideband power amplifiers are highly desirable in modern communication systems.

Another important contribution in my work is the **replacement of the transistor device**. The original paper uses the CGH40010F GaN HEMT, which delivers around 40–41 dBm output power. In my design, you have upgraded the device to **CGH40035**, which is capable of handling higher power levels and offers better gain characteristics. Because of this change, my amplifier achieves a **higher output power of around 43.3 dBm** and an improved **gain of approximately 14.577 dB**, which is noticeably better than the results reported in the paper. This improvement is not just due to the device itself, but also because I have successfully adapted the ECCE design methodology to suit the new transistor characteristics, including proper matching and biasing adjustments.

Additionally, by combining the ECCE mode design with these practical enhancements, my work improves the overall design flexibility. The added stubs and higher-power device allow the amplifier to maintain good performance over a wider frequency range without significantly degrading efficiency or stability. This shows that the ECCE approach is not only theoretically strong but can also be extended and modified effectively for higher-performance designs.

5.3 S-Parameter Analysis

In the Figure 5.10 represents the **S-parameter performance of the proposed power amplifier design**, which includes optimized performance using the ECCE-based approach with **CGH40035 ic.**

In this proposed design, the gain (S21) reaches approximately **14.57 dB at 1.8 GHz**, as indicated by marker m3. The gain remains above 10 dB across most of the operating band, which confirms that the amplifier provides consistent amplification over a wide frequency

range. Compared to the earlier direct implementation graphs, the gain here is more uniform and stable, with less fluctuation across frequencies.

The output return loss In (S22) shows good performance, remaining below –10 dB across most of the frequency range. The smoother variation of S22 compared to earlier graphs indicates improved output matching, which directly contributes to better power transfer and efficiency.The proposed bandwidth is about **0.45 GHz to 3.2 GHz.**

When comparing this proposed graph with the previously obtained direct implementation results, a few key improvements can be clearly observed. First, the gain is slightly higher and more stable across the band. Second, both S11 and S22 show more consistent matching behaviour, especially at higher frequencies where earlier designs showed more variation. Third, the overall bandwidth performance appears improved, as the amplifier maintains good gain and matching over a wider frequency range.

These improvements are mainly due to optimization of circuit parameters. Overall, the proposed approach demonstrates a clear enhancement over the basic implementation in terms of gain and frequency band, validating the effectiveness of the design modifications in achieving a more reliable and wideband power amplifier.

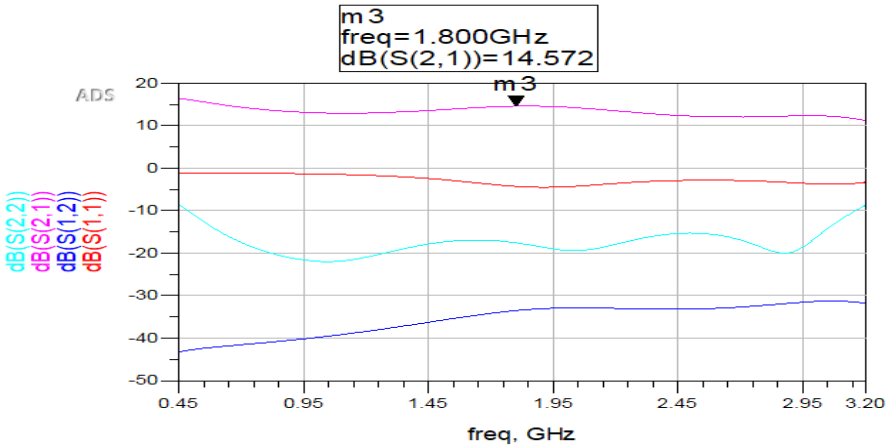


Figure 5.10: 'S' Parameters

5.4 Large Signal Analysis Performance

The Figure 5.11 represents how efficiently the amplifier converts DC power into RF output across frequency. The efficiency is highest (around **58–60%)** at lower frequencies and gradually decreases as frequency increases. A sharp dip is observed near 1.8–1.9 GHz, which corresponds to the mismatch seen in the previous graph. After this region, efficiency recovers and then slowly reduces at higher frequencies. Overall, the amplifier shows good efficiency performance across a wide bandwidth, which is a key requirement for power amplifiers.

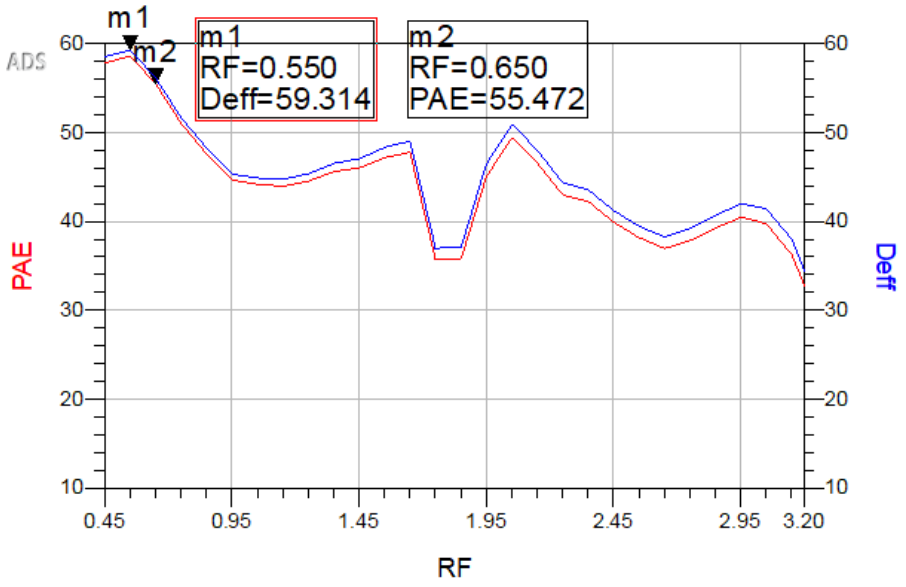


Figure 5.11: Performance of (PAE and Deff) Vs Frequency (GHz)

The Figure 5.12 shows how the Power Added Efficiency (PAE) and Drain Efficiency (Deff) change as the input power (Pavs) increases. Both efficiencies increase steadily with input power, indicating that the amplifier becomes more efficient as it is driven closer to its operating region. At around **31 dBm input power**, the PAE reaches about **59%**, and drain efficiency is around **59.7%**, showing strong performance. The smooth rise in both curves indicates stable operation without sudden drops. Overall, this graph confirms that

the amplifier achieves **high efficiency at higher input power levels**, which is desirable for power amplifier applications.

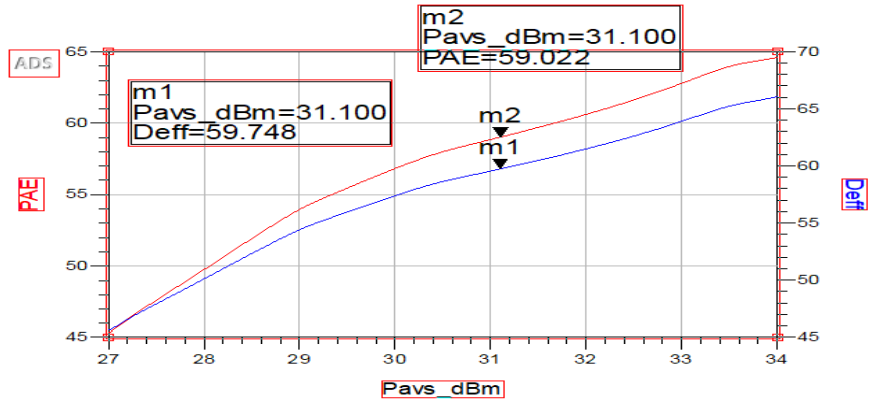


Figure 5.12: Performance of (PAE and Deff) Vs Input Power (GHz)

The Figure 5.13 shows how the output power and large-signal gain vary with frequency. The output power reaches a maximum of around **44.2 dBm near 1.64 GHz**, indicating strong power capability of the amplifier. The gain is around **13 dB**, which remains relatively stable across the operating band. A small dip around 1.8–1.9 GHz is observed, which is due to impedance mismatch at that frequency. Overall, the amplifier maintains **high output power and good gain over a wide frequency range**, confirming effective wideband operation.

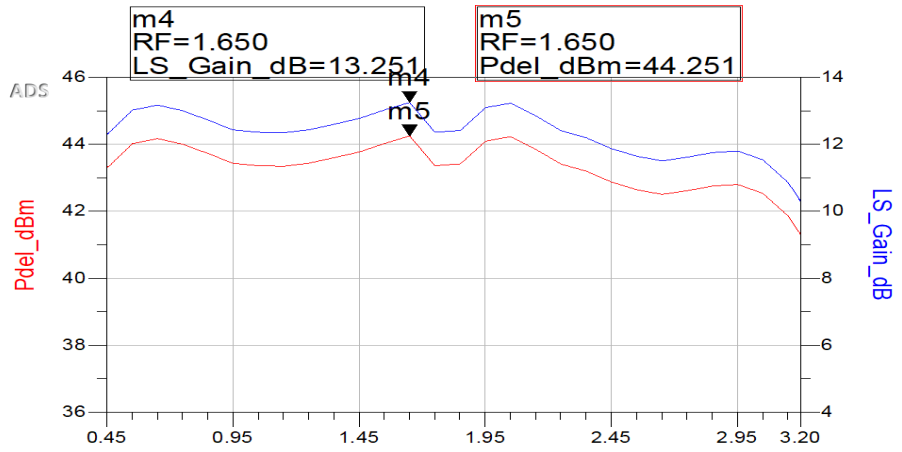


Figure 5.13: Performance of (Pdel and LS_Gain) Vs Frequency (GHz)

The Figure 5.14 shows the relationship between output power and gain with increasing input power. The output power increases gradually and reaches around 4**3.7 dBm at 31 dBm input**, indicating strong amplification capability. At the same time, the large-signal gain decreases as input power increases, which is a normal behavior known as gain compression. The gain is around **12.8 dB near 31 dBm input**, which is still a good value for high-power operation. This graph clearly shows that the amplifier delivers **high output power while maintaining reasonable gain under large-signal conditions.**

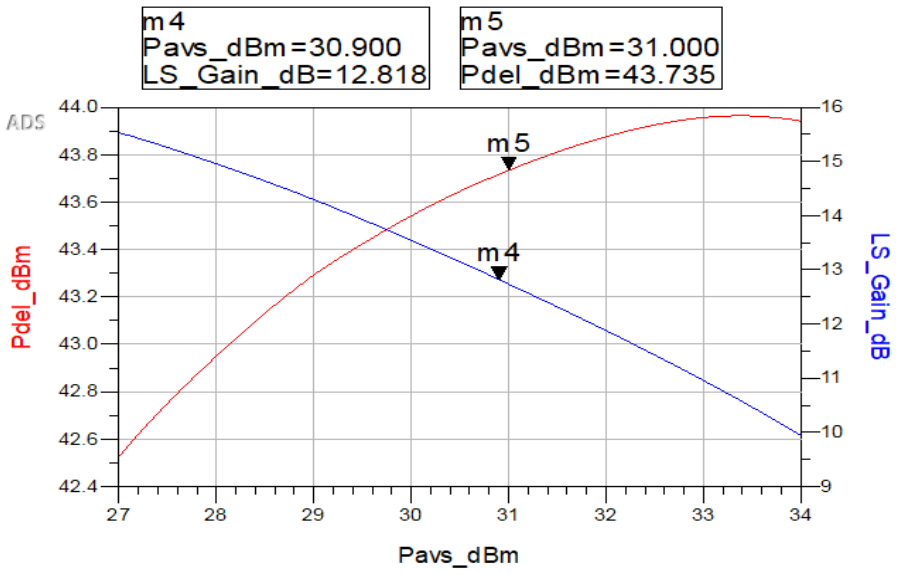


Figure 5.14: Performance of (Pdel and LS_Gain) Vs Input Power (GHz)

The Figure 5.15 shows the drain voltage and current waveforms of the transistor at 1.8 GHz. It can be seen that the voltage (red) and current (blue) waveforms are mostly **out of phase**, meaning when voltage is high, current is low and vice versa. This reduces the overlap between them, which minimizes power loss in the transistor. This behavior confirms efficient operation similar to switching mode amplifiers. Overall, the waveform indicates **proper operation with reduced power dissipation and improved efficiency**.

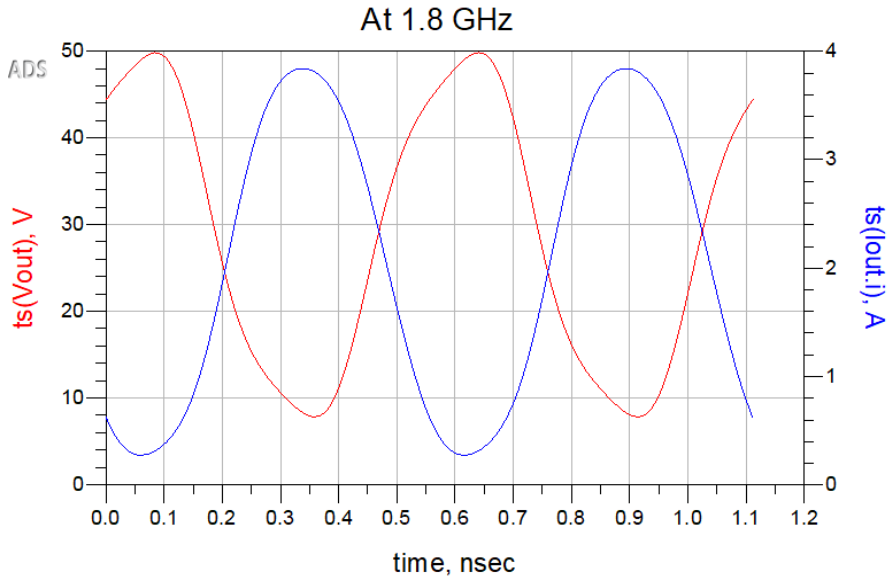


Figure 5.15: Simulated IRP waveforms at 0.45 GHz

5.5 Comparison and Discussion of Results

The comparison results clearly show that the proposed ECCE-based wideband power amplifier provides improved performance when compared with the previously reported research works. The referenced CCE approach achieves output power in the range of 39.4–41.9 dBm with gain values between 9.3–13.3 dB over the frequency range of 1.5–2.9 GHz. Similarly, the Novel Bandwidth Extended Matching Network method provides a wider operating bandwidth from 0.4–3.9 GHz, but its output power and gain are comparatively moderate. The Hybrid Class AB amplifier covers frequencies up to 6 GHz; however, it provides lower output power and gain performance. The previously reported ECCE approach achieves good efficiency values up to 63.3% PAE, but the gain and output power gradually reduce at higher frequencies. Overall, these existing approaches provide either high efficiency or wide bandwidth, but maintaining all performance parameters together remains challenging.

The implemented ECCE power combiner and the proposed ECCE approach demonstrate significant improvements in output power and

gain while maintaining wideband operation. The ECCE power combiner achieves very high output power ranging from 46.58 dBm to 42.8 dBm along with gain values up to 17.8 dB, which are much higher than the referenced methods. Similarly, the proposed ECCE amplifier achieves output power up to 44.23 dBm with gain values around 13.23 dB while operating over a wider frequency range of 0.45–3.2 GHz. Although slight reduction in efficiency is observed at higher frequencies, the amplifier still maintains acceptable PAE performance over the complete operating band.

Table 5.1: Comparison of Different Wideband Power Amplifier Approaches

Method	**Frequency Range (GHz)**	**Output Power (dBm)**	**Gain (dB)**	**Power Added Efficiency (%)**
[2] CCE Approach	1.5–2.9	39.4–41.9	9.3–13.3	60.2–76.5 (DE)
[3] Novel Bandwidth Extended Matching Network	0.4–3.9	38–42.3	10–13	57–68 (DE)
[5] Hybrid Class AB	1.8–6	∼37.6	∼9.6	42–51 (PAE)
[1] ECCE Approach	0.45–1.9	40.11–41.13	9.11–10.13	54.7–63.3 (PAE)
	2–2.9	40.9–38.7	9.9–7.7	63.3–50.3 (PAE)
ECCE Power Combiner	0.45–1.9	46.58–45.58	17.8–16.8	55.94–54.3 (PAE)
	2–2.9	45.21–42.8	16.5–14.1	51.4–41.2 (PAE)
ECCE Proposed Approach	0.45–2.05	43.2–44.23	12.29–13.23	57.8–49.4 (PAE)
	2.15–3.2	43.84–40.7	12.84–9.7	46.5–30 (PAE)

Chapter 6

Conclusion and Future Scope

6.1 Summary of Work

In this work, a wideband power amplifier was designed using the ECCE (Extended Continuous Class-E) mode approach, which is known for achieving high efficiency over a wide frequency range. The design was first implemented and analyzed in ADS software, where both small-signal and large-signal simulations were performed. The amplifier was designed to operate from 0.45 GHz to above 3 GHz, ensuring wideband performance.

Initially, the design was implemented using the CGH40010F transistor, and its performance was analyzed. Later, improvements were made by replacing it with the CGH40035 transistor, which provided higher output power and gain. Additional modifications such as improving the output matching network helped in extending the bandwidth and enhancing overall performance. The design was further converted into a PCB layout using KiCad, followed by fabrication and assembly of the hardware prototype. Finally, the performance was evaluated in terms of gain, output power, efficiency, and bandwidth, and compared with the reference design.

6.2 Conclusion

From this work, it can be concluded that the ECCE-based power amplifier design is highly effective for wideband applications. The

amplifier achieved high output power (around 43–44 dBm), good gain (around 12–14 dB), and efficiency above 55–60%, which confirms the success of the design approach. The use of the CGH40035 transistor significantly improved the performance compared to the initial implementation, especially in terms of output power and gain.

The results also show that proper design of the input/output matching networks and biasing circuits plays a key role in achieving stable and efficient operation. The waveform analysis confirmed that voltage and current do not overlap significantly, which validates the high-efficiency switching operation of the amplifier. The hardware implementation further demonstrates that the simulated design can be practically realized with good agreement between expected and actual performance.

Overall, the project successfully meets the objective of designing a high-power, high-efficiency wideband amplifier, making it suitable for modern RF communication systems.

6.3 Future Scope

Although the proposed design shows good performance, there is still scope for further improvement and extension. In the future, the bandwidth can be further increased by using more advanced matching techniques or multi-stage amplifier configurations.

Thermal management can be enhanced by using proper heat sinks or advanced packaging techniques, especially for high-power operation. The design can also be optimized for specific applications such as 5G, radar, or satellite communication systems. In addition, integrating the amplifier into a complete RF front-end system can be explored.

Further work can also include full hardware characterization using advanced measurement setups, and comparison with commercial amplifiers. Advanced simulation tools such as EM simulation can be used to improve accuracy by considering parasitic effects. These improvements can make the design more robust and suitable for real-world applications.

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