B. TECH. PROJECT REPORT

On

Resources efficient MAC unit for ANN using CORDIC

BY
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DISCIPLINE OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE
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Resources efficient MAC unit for ANN using CORDIC

A PROJECT REPORT

Submitted in partial fulfillment of the
requirements for the award of the degrees

of
BACHELOR OF TECHNOLOGY
IN
ELECTRICAL ENGINEERING

Submitted by:
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INDIAN INSTITUTE OF TECHNOLOGY INDORE
December 2019

CANDIDATE'S DECLARATION

I hereby declare that the project entitled **Resources efficient MAC unit for ANN using CORDIC** submitted in partial fulfillment for the award of the degree of Bachelor of Technology in **Electrical engineering** completed under the supervision of **DR. SANTOSH KUMAR VISHVAKARMA, Assistant Professor, Electrical Engineering,** IIT Indore is an authentic work.

Further, I declare that I have not submitted this work for the award of any other degree elsewhere.

RAHUL SINGH GURJAR

DATE: 3/12/2019

CERTIFICATE by BTP Guide(s)

It is certified that the above statement made by the students is correct to the best of my knowledge.

SIGNATURE:

SUPERVISOR: Dr. SANTOSH KUMAR VISHVAKARMA,

ASSISTANT PROFESSOR,

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IIT INDORE

Preface

This report on "**Resources efficient MAC unit for ANN using CORDIC** " is prepared under the guidance of **Dr. SANTOSH KUMAR VISHVAKARMA, Assistant Professor, Electrical Engineering, IIT Indore**

Throughout this report, detailed description of the technologies that have been used to design and implement the Resources efficient MAC unit is provided. The implemented efficient MAC unit is tested for its different inputs and results are presented in a clear and concise manner. I have tried to the best of my ability and knowledge to explain the content in a lucid manner. I have also added figures to make it more illustrative

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We wish to thank Dr. SANTOSH KUMAR VISHVAKARMA for their kind support and valuable guidance.

It is their help and support, due to which we became able to complete the design and technical report.

Without their support this report would not have been possible.

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Abstract

ASIC or FPGA based hardware implementation of neural network suffers from the problem of limited chip area, and therefore an area efficient architecture is required to fully harness the capacity of parallel processing of ASIC and FPGA in contrast to general purpose processors. We have proposed a architecture for neuron implementation based on add and shift algorithm known as CORDIC algorithm that is having a wide range of application.

This report explains how the CORDIC algorithm investigates the area and power efficient computational unit for ANN application

The goal is to present area and power efficient MAC unit for ANN.

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Chapter1: INTRODUCTION

This chapter tells about the background and motivation of the project. The problem statement of the project has been described and the importance of the results is also clearly shown. At the end, the objectives are briefly outlined and the future scope is also discussed.

1.1 Background

For real time inference of (NN) neural networks attractive hardware architectures have been developed by many researchers. An ANN is very popular for many problems that are not easy for other models like, pattern recognition, and image processing. Consequently, a significant amount of research effort has been spent on the hardware implementation of neural network.

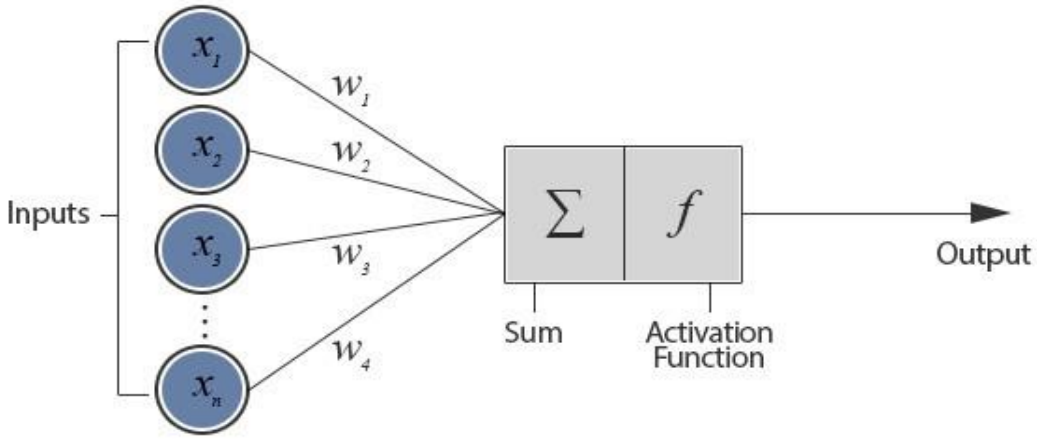

Figure 1.0 Sum and activation function in neuron

1.2 Motivation of work

1. We know there is a huge demand of portable electronics around the world .Portable products like mobile phones, laptops and other electronic gadgets require low power consumption and MAC operation is the main computational operation in these designs and the speed of processor depends on the speed of MAC unit.so coming with a design which optimize the performance or reduce the cost of implementation is the main motive of this project.

Chapter 2: MAC UNIT

2.1 Introduction to MAC unit

In present time, Multiply-Accumulate (MAC) unit is developing for various high performance-applications. In computing devices MAC unit is a fundamental block, especially Digital-Signal Processor (DSP). MAC unit performs multiplication and accumulation process. Basic MAC unit have accumulator, adder, and multiplier.

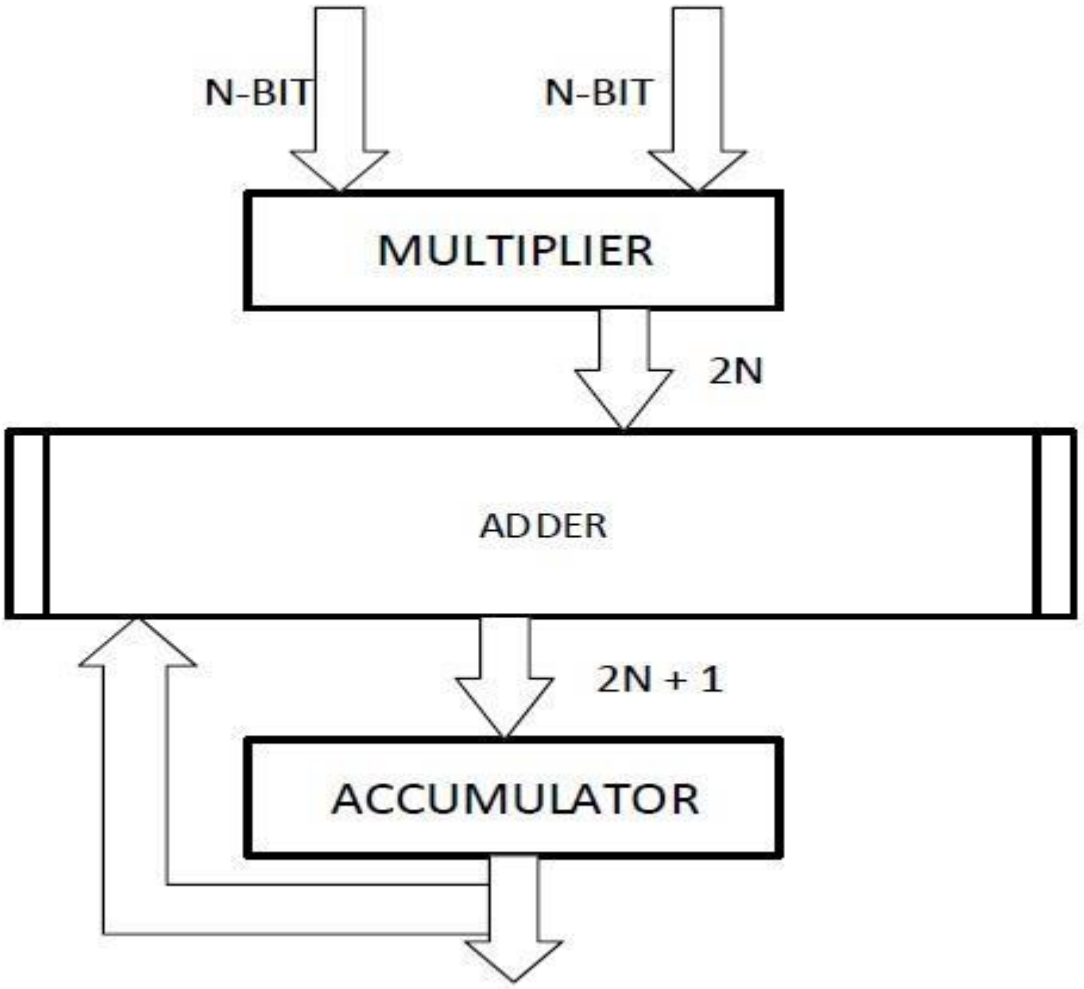

Figure 2.1 General N bit MAC unit

2.2 Applications

1. MAC unit plays an important role in many digital signal processing (DSP) applications.

2. Artificial neural networks found many problems easy that are difficult for other computational models like pattern recognition classification, image processing. And if we see a model architecture of single neuron we will came to know that MAC operation is taking place in computational part of neuron.

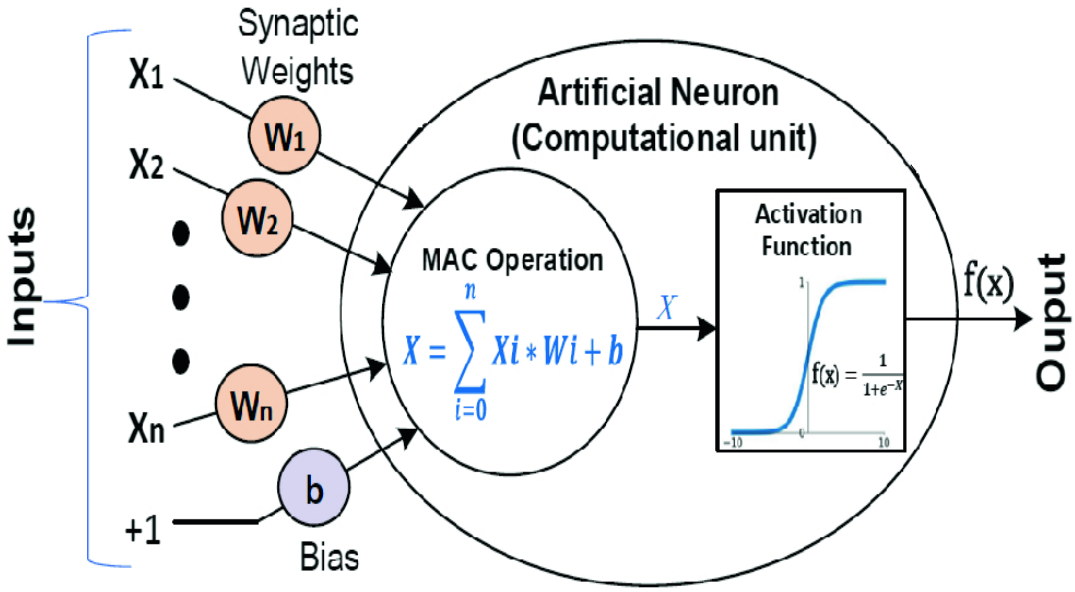

Figure 2.2 Artificial neuron model architecture

3. Used in microprocessors for data intensive applications

Chapter3: ABOUT CORDIC ALGORITHM

3.1 COORDINATE TOTATION DIGITAL COMPUTER

CORDIC (coordinate rotation digital computer) is an efficient and simple way to calculate trigonometric functions like sine, cosine and hyperbolic functions. In 1959 Jack E. VOLDER describes the CORDIC algorithm, so also known as VOLDER'S algorithm.

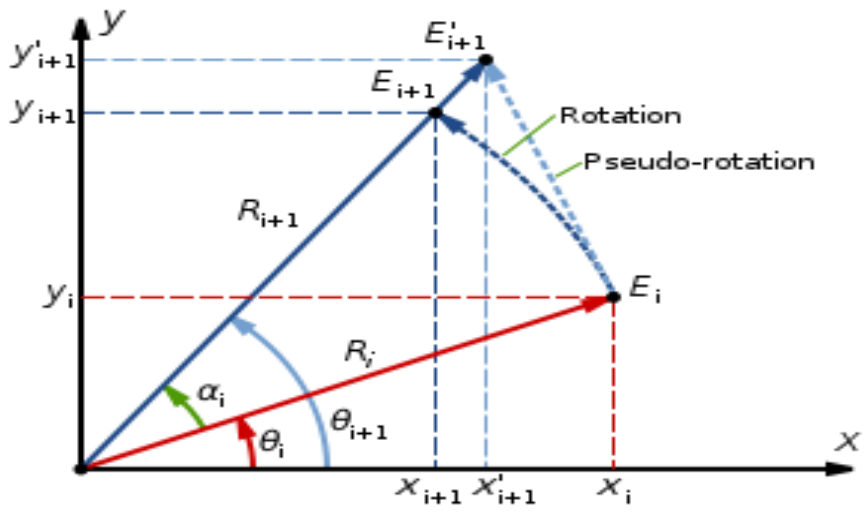

Figure 3.1 Pseudo-rotation and rotation about an angle with origin

CORDIC algorithm works by rotating the coordinate system through constant angles(pre-defined angles) until the angle is reduces to zero. The angle offsets are selected such that the operations on X and Y are only shifts and adds.

3.2 WHY CORDIC ?

1. The most beneficial part of CORDIC algorithm is that it can be used to realize both MAC as well as ACTIVATION function by running it in different modes.

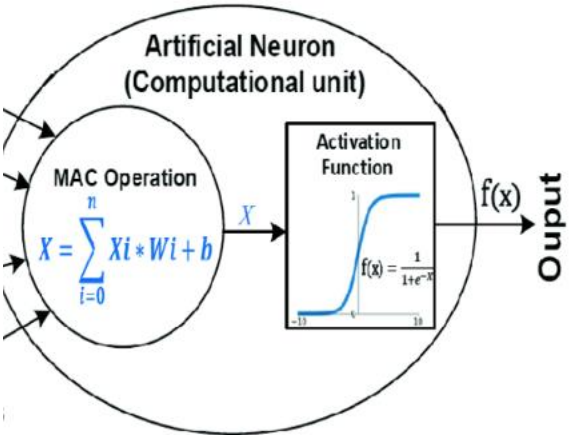

Figure 3.2 Realizing both MAC unit and ACTIVATION function in single neuron

2. Logic implementation using the CORDIC algorithm is over four times more efficient for FPGA's and controllers
3. CORDIC can be used to calculate useful operation such as exponential, hyperbolic and arithmetic
4. CORDIC helps to save hardware cost
5. In built in multiplier or dedicated hardware for sigmoid function CORDIC algorithm is having a good compromise of accuracy over speed.

3.3 UNIQUENESS OF CORDIC

1. Basically, CORDIC algorithm selects special angles of rotation such that it can perform the rotation operation by simple additions and shifts instead of multiplying functions. Thus, we can use the CORDIC algorithm rather than hardware multipliers, so that our gate count and cost will decrease. Uniqueness of the algorithm is no hardware multiplier is used and the only operation it requires are addition, subtraction, bit-shift and table lookup.

$$X_{i+1} = X_i - m.Y_i.d_i.2^{-i}$$

$$Y_{i+1} = Y_i + X_i.d_i.2^{-i}$$

$$Z_{i+1} = Z_i - d_i.\tan^{-1}2^{-i}$$

We can see from the above figure that each iteration requires

- 2 shifts
- 1 table look-up
- 3 additions

3.4 Mathematical explanation of CORDIC

The standard method of rotating a point (X_1,Y_1) by degrees in XY plane to a point (X_2,Y_2) is given by well- known equations

$X_2= X_1COS\theta-Y_1SIN\theta$

$Y_2= X_1SIN\theta+ Y_1COS\theta$

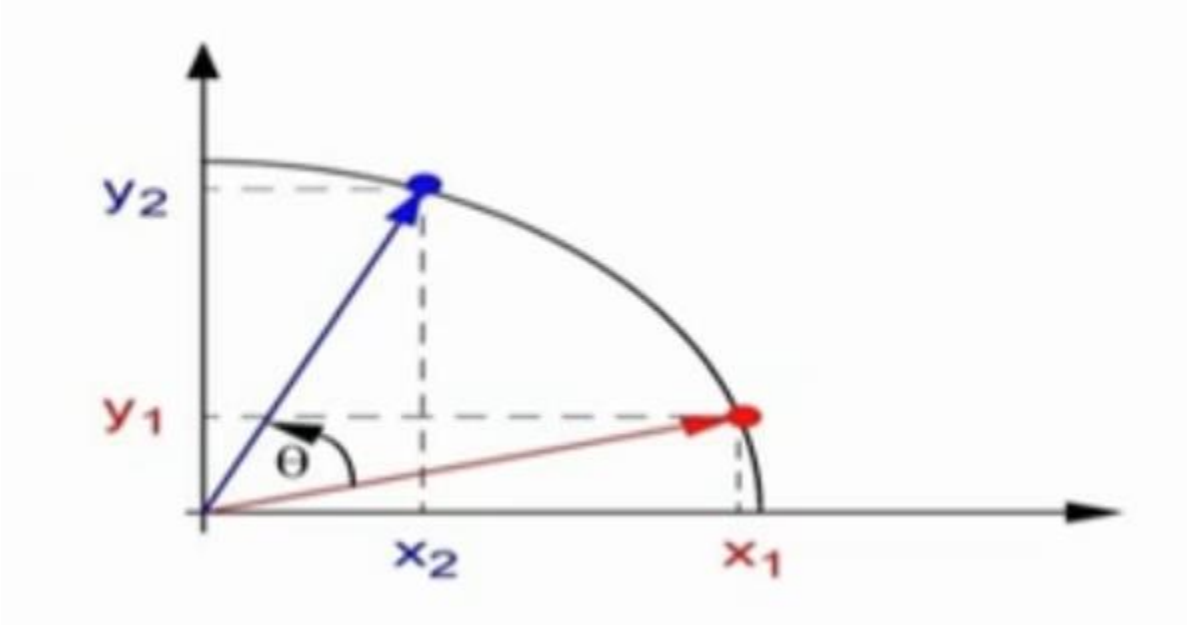

Figure 3.3 Rotating vector in x-y plane

By taking out the $COS\theta$ term common and after dropping that term we get pseudo-rotation. ie. After pseudo rotation the angle of rotation is same but x and y values are scaled by $COS^{-1}\theta$. There is no mathematical justification for dropping the $COS\theta$ term however it makes the computations of plane rotation more amenable to simple operations.

the general equations of CORDIC in rotation mode are as follows:

$$X^{(i+1)} = X^{(i)} - d_i Y^{(i)} 2^{-i}$$

$$Y^{(i+1)} = Y^{(i)} + d_i X^{(i)} 2^{-i}$$

$$Z^{(i+1)} = Z^{(i)} - d_i \tan^{-1} 2^{-I} = Z^{(i)} - d_i e^{(i)}$$

i	$e^{(i)}$ in degrees (approximate)	$e^{(i)}$ in radians (precise)
0	45.0	0.785 398 163
1	26.6	0.463 647 609
2	14.0	0.244 978 663
3	7.1	0.124 354 994
4	3.6	0.062 418 810
5	1.8	0.031 239 833
6	0.9	0.015 623 728
7	0.4	0.007 812 341
8	0.2	0.003 906 230
9	0.1	0.001 953 123

Figure 3.4 Look-up table

Chapter4: DESIGN OF MODULE AND TOOLS USED

4.1 overview of this project

NOTE: In this chapter the number of tools we used and how we used the tools are explained.

In this chapter the design of CORDIC based proposed architecture is explained clearly. As we know power consumption and area is major issue so for optimization hardware multiplier is removed.

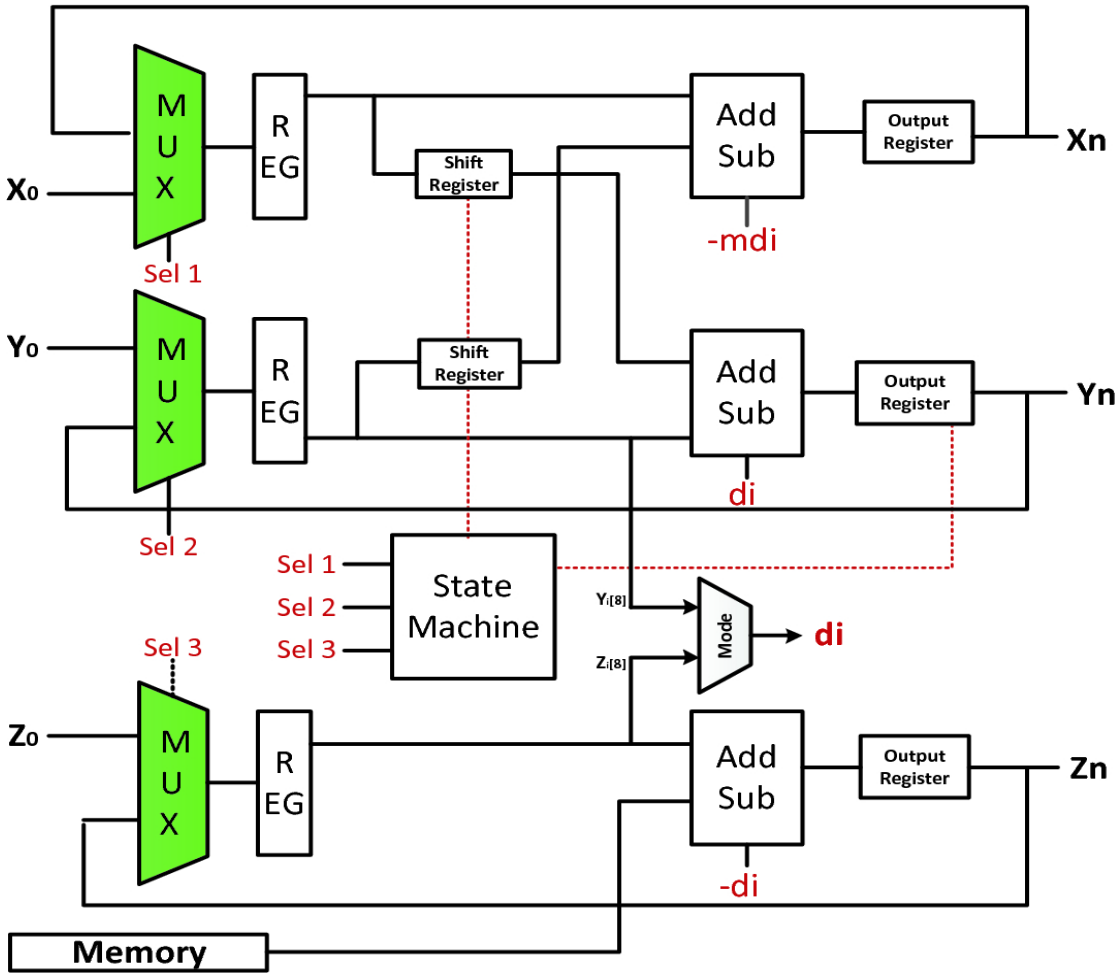

Figure 4.1 CORDIC based proposed architecture

We can realize MAC operation using CORDIC based architecture that we have proposed by making value of mode variable (m=0). In linear mode, the general equations are:

$X_N = X_0$

$Y_N = Y_0 + X_0 * Z_0$

$Z_N = 0$

where y0 and z0 represent the bias and weight value and x0 represents the input. In our proposed architecture the output and input parameters and the constants for the angle to converge to the desired final rotation is stored look-up-values in memory (LUT).to generate select signals sel1, sel2 and sel3 and to complete the feedback input after each iteration we need state machine. Signum(y_i) and signum(z_i) generate d_i which depends on running modes whether it is vectoring or rotation mode. The value of the signum function will be decided by the most significant bit (MSB) which will further decide which operation is to be performed.

4.2 Work Done

- Design process begins with the theoretical design where we have to define what the circuit have to do
- Then we start describing our circuit in high level hardware language .
- Then our code needs to be simulated to make sure VHDL description defines the wanted functionality correctly
- If we are done with functional description then we proceed to synthesis. Synopsys Design Compiler is used for synthesis.
- As a result DC returns a gate level netlist of the circuit
- After that Formality is done to check whether the synthesized netlist is logically equivalent to our VHDL code
- After formality is done we have to use cadence encounter tool to generate the physical layout of our circuit.

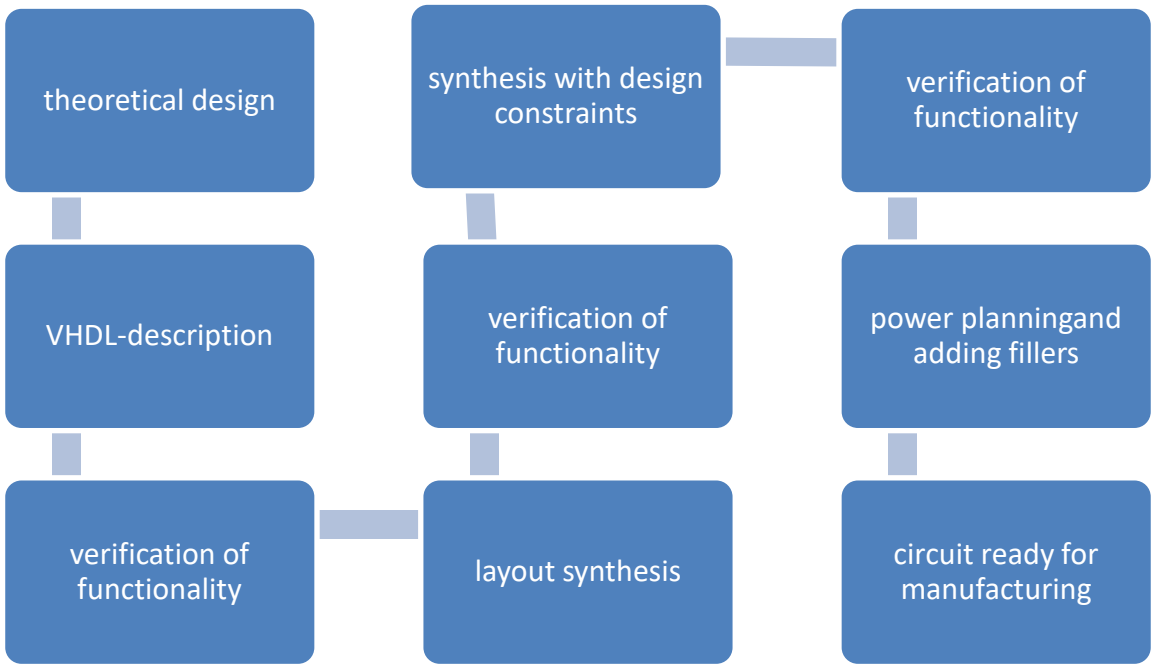

Figure 4.2 typical design flow of a digital circuit

4.3 Tools Used

1. **XILINX VIVADO**

   CORDIC algorithm of our proposed architecture is coded in VHDL .When we are done with functional description VHDL code is simulated in VIVADO.

2. **SYNOPSYS DESIGN COMPILER**

   After simulating in VIVADO we are synthesizing the VHDL description into a gate level - netlist . Circuit manufacture provide logic library from which gates are selected.

3. **ENCOUNTER TOOL FOR LAYOUT GENERATION**

   Before encounter tool check whether the synthesized netlist is logically equivalent to VHDL code . After that use Cadence encounter tool to generate physical layout of our circuit.

CHAPTER: 5 RESULTS

5.1 Synopsys Result

Shown below are the area and power reports of design vision for different process corners for **8*8** conventional MAC

```
Report : area
Design : mac_NbOvrf3_NbitIn8_NbitC8
Version: K-2015.06-SP4
Date   : Mon Aug 26 13:57:34 2019
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    tsl18fs120_scl_ss (File: /prog/cadence/FOUNDRY/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_ss.db)

Number of ports:                         49
Number of nets:                         427
Number of cells:                        342
Number of combinational cells:          306
Number of sequential cells:              36
Number of macros/black boxes:             0
Number of buf/inv:                       46
Number of references:                    25

Combinational area:              7262.600103
Buf/Inv area:                     338.659997
Noncombinational area:           2144.880066
Macro/Black Box area:               0.000000
Net Interconnect area:            188.293466

Total cell area:                 9407.480169
Total area:                      9595.773635
```

Figure 5.1 Area report of SS corner

```
Report : area
Design : mac_NbOvrf3_NbitIn8_NbitC8
Version: K-2015.06-SP4
Date   : Mon Aug 26 14:09:56 2019
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    tsl18fs120_scl_ff (File: /prog/cadence/FOUNDRY/scl_pdk/stdlib/fs120/liberty/lib_flow_ff/tsl18fs120_scl_ff.db)

Number of ports:                         49
Number of nets:                         375
Number of cells:                        309
Number of combinational cells:          273
Number of sequential cells:              36
Number of macros/black boxes:             0
Number of buf/inv:                       47
Number of references:                    27

Combinational area:             5964.600054
Buf/Inv area:                    313.509999
Noncombinational area:          2144.880066
Macro/Black Box area:              0.000000
Net Interconnect area:           204.848927

Total cell area:                8109.480120
Total area:                     8314.329047
```

Figure 5.2 Area report of SF corner

```
Report : area
Design : mac_NbOvrf3_NbitIn8_NbitC16
Version: K-2015.06-SP4
Date   : Mon Aug 26 17:37:25 2019
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    tsl18fs120_scl_ss (File: /prog/cadence/FOUNDRY/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_ss.db)

Number of ports:                         73
Number of nets:                         606
Number of cells:                        487
Number of combinational cells:          435
Number of sequential cells:              52
Number of macros/black boxes:             0
Number of buf/inv:                       35
Number of references:                    31

Combinational area:            8345.370109
Buf/Inv area:                   247.679999
Noncombinational area:         3098.160095
Macro/Black Box area:             0.000000
Net Interconnect area:          321.281641

Total cell area:               10235.143604
Total area:                    10504.302545
```

Figure 5.3 Area report of FS corner

```
Report : area
Design : mac_NbOvrf3_NbitIn8_NbitC8
Version: K-2015.06-SP4
Date   : Mon Aug 26 14:32:03 2019
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    tsl18fs120_scl_ff (File: /prog/cadence/FOUNDRY/scl_pdk/stdlib/fs120/liberty/lib_flow_ff/tsl18fs120_scl_ff.db)

Number of ports:                        49
Number of nets:                        375
Number of cells:                       309
Number of combinational cells:         273
Number of sequential cells:             36
Number of macros/black boxes:            0
Number of buf/inv:                      47
Number of references:                   26

Combinational area:             5958.320055
Buf/Inv area:                    307.229999
Noncombinational area:          2144.880066
Macro/Black Box area:              0.000000
Net Interconnect area:           205.624427

Total cell area:                8103.200120
Total area:                     8308.824547
```

Figure 5.4 Area report for FF corner

POWER REPORTS

Shown below are the power reports for different process corners of **8*8** conventional MAC.

```
Global Operating Voltage = 1.62
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 315.3622 uW   (69%)
  Net Switching Power  = 144.0492 uW   (31%)
                         ---------
Total Dynamic Power    = 753.4114 uW  (100%)

Cell Leakage Power     = 109.4597 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000           0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000           0.0000  (   0.00%)
register           0.1961       1.2897e-02          2.8336e+04           0.2090  (  45.49%)
sequential         0.0000           0.0000              0.0000           0.0000  (   0.00%)
```

Figure 5.5 Power report of SS corner

```
Global Operating Voltage = 1.62
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 520.4700 uW   (79%)
  Net Switching Power  = 142.0255 uW   (21%)
                         ---------
Total Dynamic Power    = 1171.4955 uW  (100%)

Cell Leakage Power     =   12.8065 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
---------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000           0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000           0.0000  (   0.00%)
register           0.3185        1.1877e-02          3.7728e+03           0.3304  (  49.87%)
sequential         0.0000           0.0000              0.0000           0.0000  (   0.00%)
```

Figure 5.6 Power report for SF corner

```
Global Operating Voltage = 1.98
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 530.4460 uW   (57%)
  Net Switching Power  = 404.4607 uW   (43%)
                         ---------
Total Dynamic Power    = 934.9068 uW  (100%)

Cell Leakage Power     = 90.6376 nW


                 Internal         Switching           Leakage           Total
Power Group      Power            Power               Power             Power   (   %    ) Attrs
--------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000            0.0000  (   0.00%)
register           0.2850        2.6526e-02          4.0929e+04           0.3116  (  33.32%)
sequential         0.0000           0.0000              0.0000            0.0000  (   0.00%)
```

Figure 5.7 Power report for FS corner

```
Global Operating Voltage = 1.98
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 508.3862 uW   (71%)
  Net Switching Power  = 212.3048 uW   (29%)
                         ---------
Total Dynamic Power    = 1234.4910 uW  (100%)

Cell Leakage Power     =   12.8065 nW


                Internal         Switching           Leakage           Total
Power Group     Power            Power               Power             Power   (   %    )  Attrs
---------------------------------------------------------------------------------------------
io_pad            0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory            0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box         0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network     0.0000           0.0000            0.0000            0.0000  (   0.00%)
register          0.3176        1.7513e-02        3.7728e+03            0.3351  (  46.50%)
sequential        0.0000           0.0000            0.0000            0.0000  (   0.00%)
```

Figure 5.8 Power report for FF corner

REPORTS FOR PROPOSED MAC

Shown below are the results for 8*8 proposed MAC for 180 nm SCL technology.

```
Report : area
Design : Top
Version: M-2016.12-SP5-3
Date   : Sat Nov  2 16:42:22 2019
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    tsl18fs120_scl_ss (File: /prog/cadence/FOUNDRY/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_ss.db)

Number of ports:                        58
Number of nets:                        315
Number of cells:                       260
Number of combinational cells:         187
Number of sequential cells:             73
Number of macros/black boxes:            0
Number of buf/inv:                      33
Number of references:                   23

Combinational area:             4365.270060
Buf/Inv area:                    238.299998
Noncombinational area:          4349.340134
Macro/Black Box area:              0.000000
Net Interconnect area:           180.694905

Total cell area:                8714.610193
Total area:                     8895.305098
```

Figure 5.9 Area report for SS corner

```
Report : area
Design : Top
Version: M-2016.12-SP5-3
Date   : Sun Nov  3 16:29:24 2019
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    tsl18fs120_scl_ff (File: /prog/cadence/FOUNDRY/scl_pdk/stdlib/fs120/liberty/lib_flow_ff/tsl18fs120_scl_ff.db)

Number of ports:                        58
Number of nets:                        304
Number of cells:                       249
Number of combinational cells:         176
Number of sequential cells:             73
Number of macros/black boxes:            0
Number of buf/inv:                      27
Number of references:                   21

Combinational area:             4261.740059
Buf/Inv area:                    184.969999
Noncombinational area:          4349.340134
Macro/Black Box area:              0.000000
Net Interconnect area:           185.343774

Total cell area:                8611.080193
Total area:                     8796.423967
```

Figure 5.10 Area report for SF corner

```
Report : area
Design : Top
Version: M-2016.12-SP5-3
Date   : Sat Nov  2 16:42:22 2019
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    tsl18fs120_scl_ss (File: /prog/cadence/FOUNDRY/scl_pdk/stdlib/fs120/liberty/lib_flow_ss/tsl18fs120_scl_ss.db)

Number of ports:                         58
Number of nets:                         315
Number of cells:                        260
Number of combinational cells:          187
Number of sequential cells:              73
Number of macros/black boxes:             0
Number of buf/inv:                       33
Number of references:                    23

Combinational area:             4365.270060
Buf/Inv area:                    238.299998
Noncombinational area:          4349.340134
Macro/Black Box area:              0.000000
Net Interconnect area:           180.694905

Total cell area:                8685.3468
Total area:                     8840.4256
```

Figure 5.11 Area report for FS corner

```
Report : area
Design : Top
Version: M-2016.12-SP5-3
Date   : Sat Nov  2 17:09:21 2019
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    tsl18fs120_scl_ff (File: /prog/cadence/FOUNDRY/scl_pdk/stdlib/fs120/liberty/lib_flow_ff/tsl18fs120_scl_ff.db)

Number of ports:                         58
Number of nets:                         304
Number of cells:                        249
Number of combinational cells:          176
Number of sequential cells:              73
Number of macros/black boxes:             0
Number of buf/inv:                       27
Number of references:                    21

Combinational area:             4261.740059
Buf/Inv area:                    184.969999
Noncombinational area:          4349.340134
Macro/Black Box area:              0.000000
Net Interconnect area:           184.083774

Total cell area:                8611.080193
Total area:                     8795.163967
```

Figure 5.12 Area report for FF corner

POWER

```
Global Operating Voltage = 1.62
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 561.2855 uW   (75%)
  Net Switching Power  = 191.8828 uW   (25%)
                         ---------
Total Dynamic Power    = 459.4683 uW  (100%)

Cell Leakage Power     = 113.8740 nW


                 Internal         Switching           Leakage           Total
Power Group      Power            Power               Power             Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000            0.0000  (   0.00%)
register           0.4610       6.0012e-02          5.7458e+04            0.5211  (  69.17%)
sequential         0.0000           0.0000              0.0000            0.0000  (   0.00%)
combinational      0.1003           0.1319          5.2001e+04            0.2322  (  30.83%)
--------------------------------------------------------------------------------------------------
```

Figure 5.13 Power report for SS corner

```
Global Operating Voltage = 1.62
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 520.4700 uW   (79%)
  Net Switching Power  = 142.0255 uW   (21%)
                         ---------
Total Dynamic Power    = 662.4955 uW  (100%)

Cell Leakage Power     =   9.8909 nW


                 Internal         Switching           Leakage           Total
Power Group      Power            Power               Power             Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000            0.0000  (   0.00%)
register           0.3185       1.1877e-02          3.7728e+03            0.3304  (  49.87%)
sequential         0.0000           0.0000              0.0000            0.0000  (   0.00%)
```

Figure 5.14 Power report for SF corner

```
Global Operating Voltage = 1.98
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 653.5047 uW   (77%)
  Net Switching Power  = 281.7917 uW   (23%)
                         ---------
Total Dynamic Power    =   0.7206 mW  (100%)

Cell Leakage Power     =  9.8924 nW


                 Internal         Switching           Leakage           Total
Power Group      Power            Power               Power             Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000            0.0000  (   0.00%)
register           0.7558       9.6806e-02          7.6504e+03            0.8526  (  69.08%)
sequential         0.0000           0.0000              0.0000            0.0000  (   0.00%)
combinational      0.1967           0.1850          5.1561e+03            0.3817  (  30.92%)
--------------------------------------------------------------------------------------------------
```

Figure 5.15 Power report for FF corner

```
Global Operating Voltage = 1.98
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 653.5047 uW   (77%)
  Net Switching Power  = 281.7917 uW   (23%)
                         ---------
Total Dynamic Power    =   0.8623 mW  (100%)

Cell Leakage Power     =  180.8241 nW
```

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	0.7558	9.6806e-02	7.6504e+03	0.8526	(69.08%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	0.1967	0.1850	5.1561e+03	0.3817	(30.92%)	

Figure 5.16 Power report for FS corner

5.2 Result from encounter tool

After getting correct output in all stages then I generate a physical layout using ENCOUNTER (CADENCE TOOL)

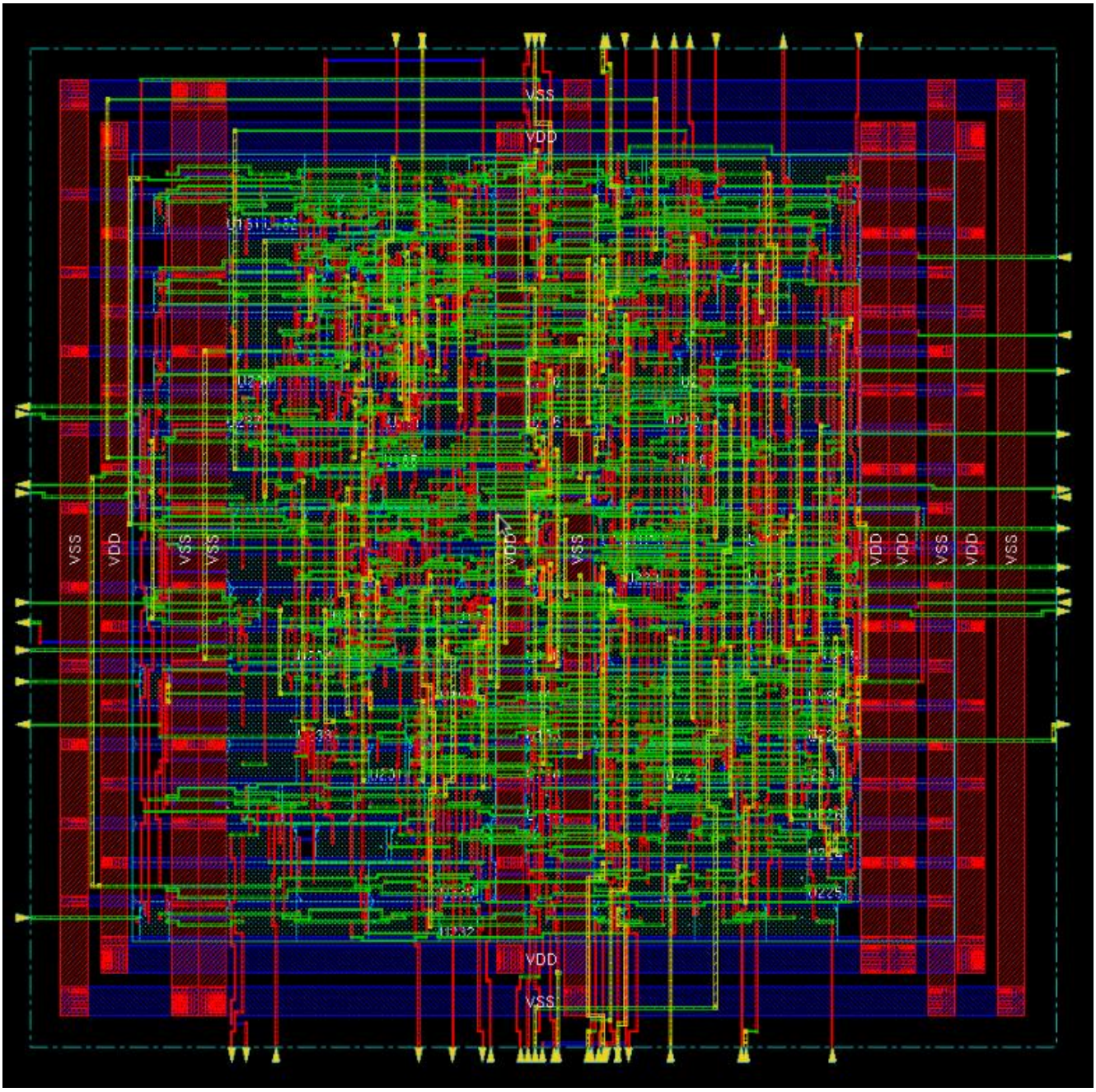

Figure 5.17 Physical layout

CHAPTER 6: Conclusion and future work

6.1 Conclusion

In this work, a design of area efficient and low power MAC structure is presented. Power dissipation of proposed MAC was found to be 7.76% less than the CONVENTIONAL MAC and similarly the proposed MAC architecture improved with the 15.83% of area

8*8 conventional MAC

CORNERS	TOTAL CELL AREA(μm^2)	TOTAL AREA(μm^2)	TOTAL DYNAMIC POWER(mw)	CELL LEAKAGE POWER(nw)
SS	9407.4801	9595.7736	0.7531	109.4597
SF	8109.7501	8314.3290	1.1714	12.8065
FF	8103.2001	8308.8245	1.2343	12.8065
FS	10235.1436	10504.3025	0.9349	90.6376

8*8 Proposed MAC

CORNERS	TOTAL CELL AREA(μm^2)	TOTAL AREA(μm^2)	TOTAL DYNAMIC POWER(mw)	TOTAL CELL LEAKAGE POWER(nw)
SS	8714.6101	8895.3050	0.4594	113.8740
SF	8611.0801	8796.4239	0.6624	9.8909
FS	8685.3468	8840.4256	0.8623	180.8241
FF	8611.0801	8795.1639	0.7206	9.8924

2.5 Future work

As my present project focus on design of the architecture using CORDIC algorithm for 180 nm SCL Technology. My future work will be design of the architecture using CORDIC algorithm for lower technology like 45 nm,32nm,22nm for 16*16, 32*32 bit MAC unit.

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