B. TECH. PROJECT REPORT

On

Performance Assessment of Negative Capacitance MOSFET

BY

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requirements for the award of the degrees

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in

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Submitted by:

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INDIAN INSTITUTE OF TECHNOLOGY INDORE

December 2019

CANDIDATE'S DECLARATION

We hereby declare that the project entitled **"Performance Assessment of Negative Capacitance MOSFET"** submitted in partial fulfillment for the award of the degree of Bachelor of Technology in 'Electrical Engineering' completed under the supervision of **Dr. Abhinav Kranti, Professor, Discipline of Electrical Engineering, IIT Indore** is an authentic work.

Further, I declare that I have not submitted this work for the award of any other degree elsewhere.

Veldanda Pranay Reddy

CERTIFICATE by BTP Guide(s)

It is certified that the above statement made by the students is correct to the best of my knowledge.

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Preface

This report on “Performance Assessment of Negative Capacitance MOSFET" is prepared under the guidance of Prof. Abhinav Kranti.

In this project, the potential use of negative capacitance resolving the power crisis in improving the performance of MOSFET is studied. Working of NCFET and the role of sub-60 mV/decade subthreshold swing in improving switching characteristics are studied. Performance of GAA-NCFET is studied. The constraints for stable hysteresis free operation of NCFET and the operating limits for stable operation are determined. The improvement in current characteristics is studied. The greater scalability of doped hafnia-based ferroelectrics over perovskite-based ferroelectrics is studied.

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Abstract

An important factor that characterizes the efficient switching performance of MOS devices is the Subthreshold Swing (SS). A steep SS can be advantageous for fast switching, high on-current and high on-to-off current ratio. In a conventional MOSFET, SS cannot be reduced below 60 mV/decade limit at 300 K. This phenomenon is known as Boltzmann tyranny. Negative Capacitance Field-Effect Transistor (NCFET) can be utilised to achieve a sub-60mV/decade SS. NCFET exhibits Metal-Ferroelectric-Insulator-Semiconductor (MFIS) architecture. The objective of this project is to understand the working of NCFET which ensures sub-60 mV/decade switching and also determine the constraints and operating limits for stable and hysteresis free operation of the device.

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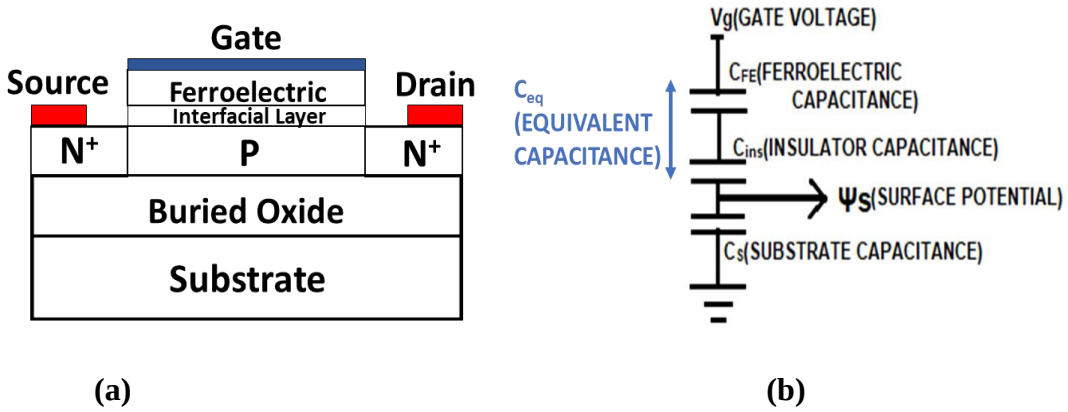
Chapter 1

Introduction

1.1 Power Crisis in the Semiconductor Industry

After the invention of internet, the data consumption has seen a rapid growth. With the invention of new cutting-edge technologies, it is projected to increase even more rapidly. The Semiconductor industry opted for scaling down the CMOS transistors to handle the booming data consumption. The industry has done a very good job in scaling down the devices in past several decades [1]. In 1970s, transistors were at 10 micron scale and now the industry is racing towards sub-10 nanometre devices. It is possible in the near future that we may reach a maximum scaling limit and could not scale the devices further [1]. Due to closely packed transistors, the power dissipation density has been increasing. The power supply voltage of a microprocessor (V_{DD}) could not be reduced below 1V due to physical constraints. Hence, the operating clock frequency could not increase beyond 3GHz for past two decades [1].

The reason behind the inability of decreasing the supply voltage below 1V is the fact that the Subthreshold Swing (SS) [2] for a MOSFET cannot be reduced below 60mV/decade at room temperature. This phenomenon is known as the "Boltzmann Tyranny" [3]. Due to the Boltzmann distribution of charge carriers in a semiconductor, to increase the drain current (I_{ds}) by one order of a magnitude the gate bias should be increased by a minimum of $kTln10 = 60\text{mV}$ at room temperature, k and T are the Boltzmann constant and temperature, respectively. To maintain the I_{ON}/I_{OFF} i.e. the on-to-off current ratio to be at least at 10^6 [4], the power supply voltage could not be reduced below 1V in a conventional MOSFET.



(a) **(b)**

Fig. 1. Schematic diagram of **(a)** a typical NCFET [5] structure and **(b)** its equivalent series capacitance model [6]. Interfacial layer is assumed to be SiO_2 with dielectric constant of 3.9.

1.2 Subthreshold Swing

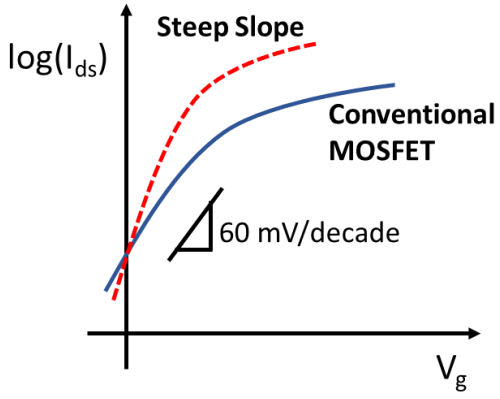


Fig. 2. Drain current characteristics depicting normal slope and steep slope [3].

The subthreshold swing (SS), represents the minimum gate bias (V_g) required to change the drain current (I_{ds}) by one decade [7]. Mathematically [7],

$$SS = \frac{\partial V_g}{\partial(log(I_{ds}))} = \frac{\partial V_g}{\partial \psi_s} \times \frac{\partial \psi_s}{\partial(log(I_{ds}))} = m \times \frac{\partial \psi_s}{\partial(log(I_{ds}))} \quad (1)$$

where 'ψ_s' indicates surface potential at semiconductor-insulator interface and 'm' denotes the body factor and is given [6] by

$$m = 1 + (C_s/C_{eq}) \quad (2)$$

The notations C_{eq} and C_s indicate equivalent gate insulator capacitance and the substrate capacitance, respectively.

The minimum achievable value of the term $(\partial\psi_s/\partial(\log(I_{ds})))$ of equation (1) is 60 mV/decade at room temperature [1]. Band to band tunnelling [8] and impact ionization [9] techniques can be used to reduce it further but are beyond the scope of this study.

For a conventional MOSFET,

$$C_{eq} = C_{ins}$$

$$m = 1 + (C_s/C_{ins})$$

The notation C_{ins} indicates the insulating oxide capacitance.

The body factor is always greater than unity as both the capacitances (C_s and C_{ins}) are positive [6]. A possible approach to obtain lower SS is to reduce the body factor below unity. For that, conventional MOSFET can be re-modelled by introducing a negative capacitance in between the gate and the substrate forming a Negative Capacitance Field Effect Transistor (NCFET) [5], as shown in fig. 1(a). A Ferroelectric (FE) gate insulating oxide serves the purpose of achieving negative capacitance.

Chapter-2

Ferroelectrics

2.1 Introduction to Ferroelectrics

Pyroelectric crystals exhibit spontaneous polarization in certain range of temperatures [10]. In most of them, the direction of polarization can be reversed by applying external electric field [10]. Such materials are characterised as ferroelectrics. Another important characteristic is the hysteresis loop [11], i.e. the polarisation is double valued function of applied electric field. Ferroelectrics exhibit negative capacitance in certain region of operation in contrast to dielectrics which always exhibit only positive capacitance. Negative capacitance state is thermodynamically unstable. When we move along the path A to B as shown in fig. 3, a direct jump is observed from state C to B, making the NC state form C to D unobservable. Similarly, when we move along B to A, direct jump is observed from state D to A, making the NC state form D to C unobservable. Hence, negative capacitance cannot be measured directly with the help of regular impedance measurement equipment.

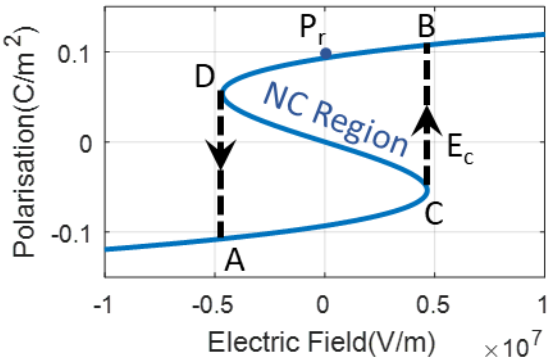


Fig. 3. Polarisation vs. Electric Field characteristics depicting unstable nature of NC state [3].

Non-zero Remanent Polarization (P_r) is observable in the fig. 3 as ferroelectrics retain some amount of Polarization even after the electric field is removed completely. Also, the direction of the remaining Polarization can be reversed by reversing the electric field as observed in the fig. 3.

2.2 Ferroelectric Characteristics

Ferroelectrics are characterized by remanent Polarization (P_r) and coercive field strength (E_c). Barium titanate (BTO), Lead zirconate titanate (PZT), Strontium Bismuth tantalate (SBT) and doped Hafnia (HfO2 doped with Al, Si, Sr, Y) are best examples of FE materials. BTO, PZT, SBT are conventional Perovskite based ferroelectrics and they exhibit low coercive field strengths (in kV/cm) [12],[13],[14]. They could not meet the scaling targets of the nanodevices as lower coercive field strength corresponds to lower scaling capability.

Table. 1. List of conventional perovskite-based FE with their respective P_r and E_c [12],[13],[14].

Perovskite-based FE	Remanent Polarisation (P_r) in ($\mu C/cm^2$)	Coercive Field Strength (E_c) in (kV/cm)
BTO	25 $\mu C/cm^2$	100 kV/cm
SBT	10 $\mu C/cm^2$	38 kV/cm
PZT	36 $\mu C/cm^2$	4 kV/cm

The doped Hafnia-based ferroelectrics exhibit higher coercive field strength (in MV/cm) and relatively same remanent Polarization (P_r) [15],[16],[17]. They show superior scaling properties compared to Perovskite materials.

Table. 2. List of doped Hafnia-based FE with their respective P_r and E_c [15],[16],[17].

Doped Hafnia-based FE	Remanent Polarisation (P_r) in ($\mu C/cm^2$)	Coercive Field Strength (E_c) in (MV/cm)
Al doped HfO_2	12 $\mu C/cm^2$	1 MV/cm
Si doped HfO_2	17.3 $\mu C/cm^2$	3 MV/cm
Sr doped HfO_2	23 $\mu C/cm^2$	2 MV/cm

2.3 Free Energy of Ferroelectrics

The ferroelectric layer is modeled using the Landau-Khalatnikov (L-K) equation [3]. As the voltage profile is non-uniform along the channel, the L-K equation cannot be valid across the ferroelectric. So, the Interfacial Layer (IL) is necessary because it ensures that the non-uniform potential is averaged out at the FE and IL interface, making the L-K equation of the system valid [5]. The equivalent capacitance of FE and IL should remain negative to achieve voltage amplification at the surface of the substrate. In an FE material, the free energy (U) is related to electric Polarization (P) and charge density (Q) according to the L-K theory [3].

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - E P \quad (3)$$

where α, β and γ are ferroelectric landau coefficients listed out in table 2 and $\alpha < 0$ for any FE material. α is a material dependent parameter which also depends on temperature. Whereas β and γ are only material dependent and temperature independent parameters. The parameter α majorly determines the negative capacitance behavior. Perovskite-based materials exhibit α in the order of 10^7 [6]. Whereas the hafnia-based materials exhibit higher order of α at 10^9 [18] and thus show superior scaling properties.

Table. 3. List of FE with their respective ferroelectric Landau coefficients [6],[18].

Parameters	**BTO**	**PZT**	**SBT**	**Al doped Hafnia**
α(m/F)	-1×10^7	-4.5×10^7	-6.5×10^7	-3×10^9
β($m^5F/coul^2$)	-8.9×10^8	5.2×10^8	3.75×10^9	6×10^{11}
γ($m^9F/coul^4$)	4.5×10^{10}	5.9×10^8	0	0

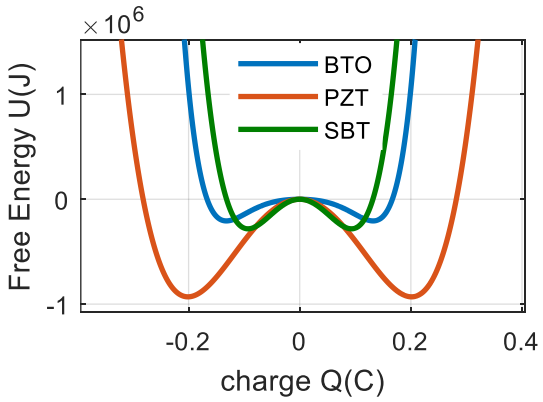


Fig. 4. Free energy characteristics for three different FE materials BTO, PZT and SBT depicting double well shaped curve.

The free energy plot of any FE material shows unique double-well or double 'U' shaped characteristics as shown in fig. 4 in contrast with a regular dielectric which shows single 'U' shaped characteristics.

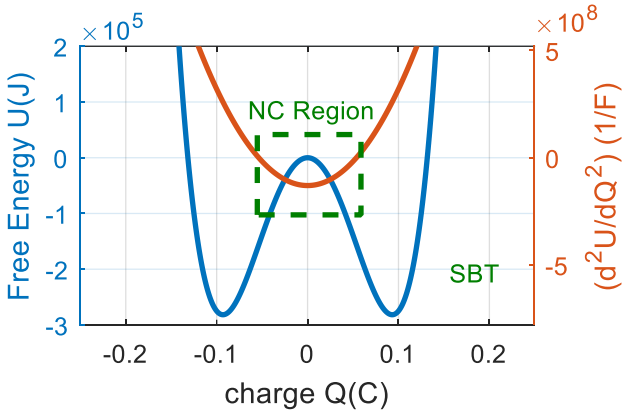


Fig. 5. Variation of free energy and its double derivative with respect to charge for SBT FE material showing the NC state.

The negative radius of curvature (or) double derivative of the free energy plot as shown in fig.5 implies negative capacitance behavior of a ferroelectric.

2.4 Polarization - Electric Field Characteristics

The applied electric field (E) is related to electric polarization (P) and charge density (Q) by [5],

$$E = \alpha_0 P + \beta_0 P^3 + \gamma_0 P^5 \approx \alpha_0 Q + \beta_0 Q^3 + \gamma_0 Q^5 \quad (4)$$

$\alpha_0 = 2\alpha$, $\beta_0 = 4\beta$, $\gamma_0 = 6\gamma$.

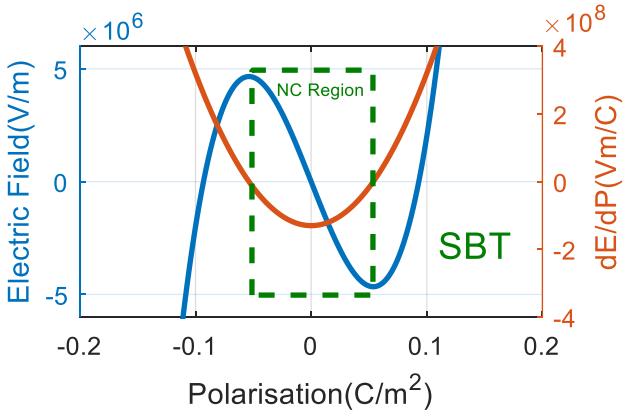


Fig. 6. Polarization vs. electric field curve and the derivative curve showing the NC region for FE material SBT.

FE materials exhibit "S" shaped P-E and Q-V characteristics. The negative slope (or) negative derivative of the P-E and Q-V curves imply the negative capacitance behavior.

2.5 Charge - Voltage Characteristics

The ferroelectric voltage (V_{FE}) and capacitance (C_{FE}) for a ferroelectric material of thickness t_{FE} can be expressed as [6]:

$$V_{FE} = t_{FE} \times (\alpha_0 Q + \beta_0 Q^3 + \gamma_0 Q^5) \quad (5)$$

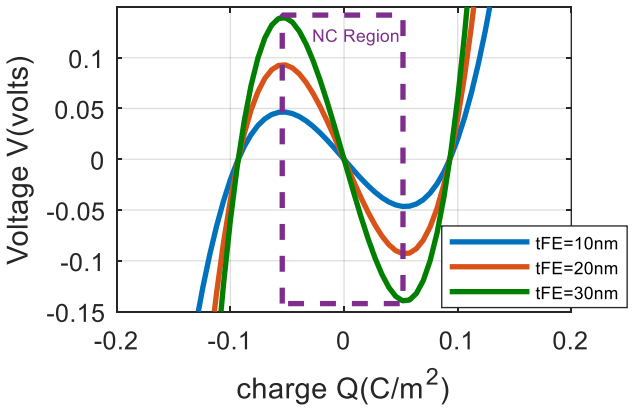


Fig. 7. Voltage-charge characteristics for various FE thicknesses illustrating negative capacitance behavior of SBT FE material.

Chapter 3

Negative Capacitance Behaviour

3.1 Series Capacitance Analysis

The most fundamental aspect of NCFET is the Gate voltage Amplification. If we represent an NCFET as a series capacitance equivalent model, we can observe that the gate voltage would be amplified at the surface if the equivalent gate insulator capacitance is negative. The Interfacial oxide layer is modelled with 1nm thick Silica (SiO_2 with thickness t_{ins}=1nm). In spite of adding an interfacial layer which is a series positive capacitance (C_{ins}), the equivalent capacitance (C_{eq}) should still show negative capacitance behaviour for the gate amplification to be possible. Also, as the negative capacitance is thermodynamically unstable, a positive series capacitance is necessary for its stabilization. The positive capacitances in the device structure such as the channel capacitance or substrate capacitance (C_s) can stabilize the ferroelectric in its negative capacitance state leading to a stable amplification [6].

$$C_{eq}^{-1} = C_{ins}^{-1} + C_{FE}^{-1} \quad (6)$$

$$C_{overall}^{-1} = C_s^{-1} + C_{eq}^{-1} \quad (7)$$

$C_{overall} > 0$ for stable hysteresis free operation. Hence,

$$|C_s| \leq |C_{eq}| \quad (8)$$

The body factor should be minimised to achieve the minimum possible SS. Hence, the obvious choice is $|C_s| \approx |C_{eq}|$ and C_s slightly less than C_{eq} for which we achieve zero SS and abrupt switching.

The FE capacitance (C_{FE}) is given by [6]

$$C_{FE} = [\partial^2 U/\partial Q^2]^{-1} = dQ/dV_{FE} \quad (9)$$

$$\text{(or) } C_{FE} = 1/[t_{FE} \times (\alpha_0 Q + 3\beta_0 Q^2 + 5\gamma_0 Q^4)] \quad (10)$$

3.2 Negative Capacitance Behavior of SBT

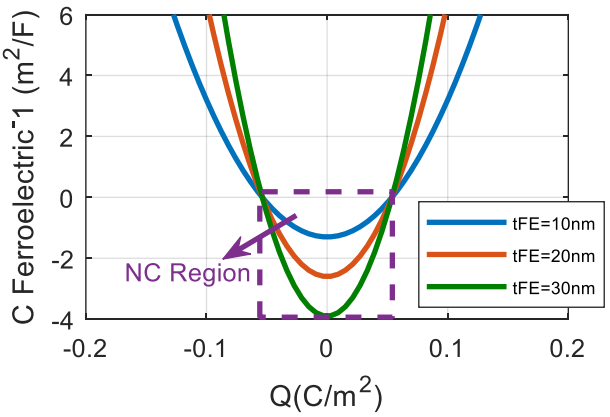


Fig. 8. FE capacitance-charge characteristics for various FE thicknesses illustrating negative capacitance behavior of SBT FE material.

Now, the interfacial layer is modeled with SiO_2 dielectric constant (K=3.9) and thickness (t_{ins}= 1nm). The gate insulator equivalent capacitance (C_{eq}) can be visualized as a series combination of FE capacitance (C_{FE}) which shows negative capacitance in certain region and an always positive dielectric insulator capacitance (C_{ins}). Even in spite of adding a positive capacitance, the equivalent capacitance (C_{eq}) should show negative behavior, so as to achieve gate voltage amplification.

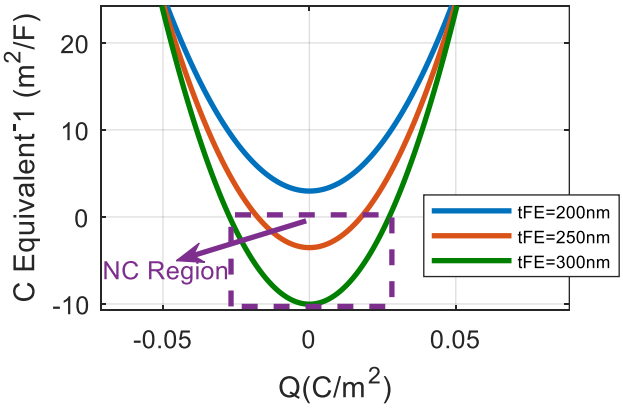


Fig. 9. Gate insulator equivalent capacitance-charge characteristics of SBT FE material for various FE thicknesses after modelling the interfacial layer with 1nm thick SiO_2.

After adding an interfacial layer to the existing FE layer of SBT, the FE thickness has to be increased over 200nm for retaining the negative capacitance behaviour. The device thickness

has to be within nano meter range for better scaling capability. Hence, conventional perovskite-based ferroelectrics exhibit low scaling capability. There is a need to use special kind of ferroelectrics to improve scaling properties.

3.3 Negative Capacitance Behavior of Aluminum Doped Hafnia

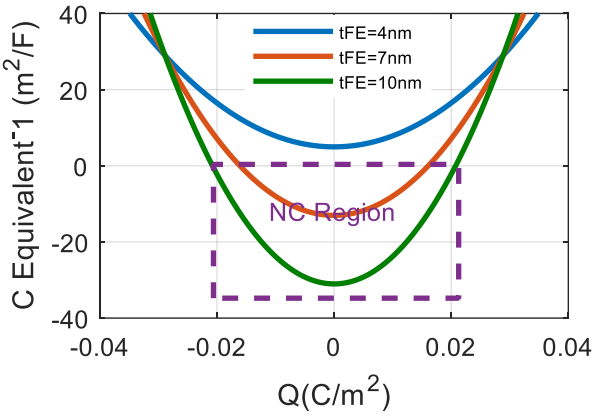


Fig. 10. Gate insulator equivalent capacitance-charge characteristics for Al doped Hafnia as Fe material for various FE thicknesses after modelling the interfacial layer with 1nm thick SiO_2.

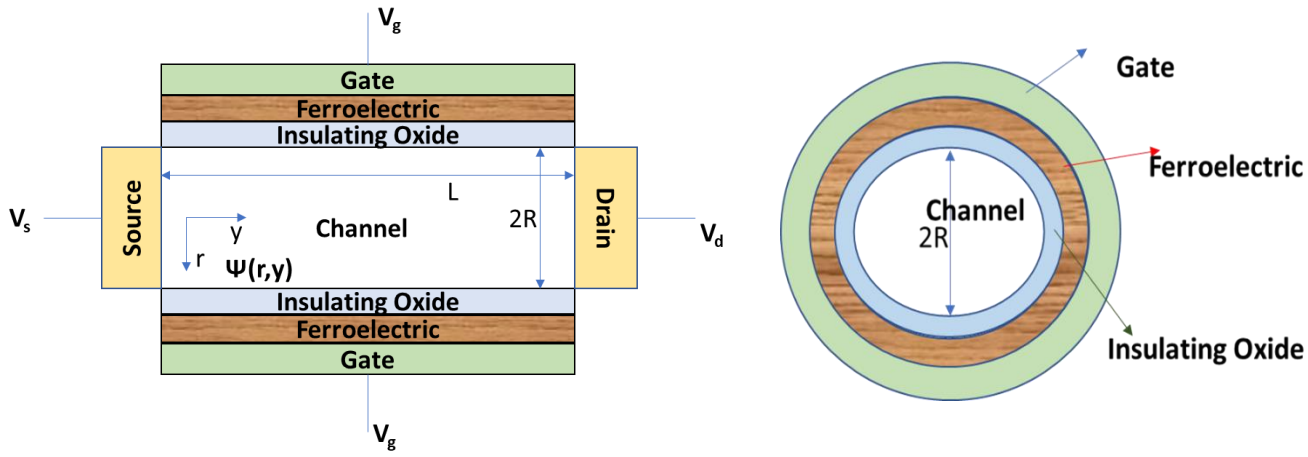
Hafnia-based ferroelectrics provide an excellent solution to the scaling inability problem of NCFET. After the addition of an interfacial layer aluminium doped hafnia retains its negative capacitance behaviour within sub 10nm range FE thickness as shown in fig. 10.

Chapter 4

GAA-NCFET

4.1 Description of GAA-NCFET

To study the performance of an NCFET, we consider a cylindrical nanowire MOSFET with Gate-All-Around architecture with channel radius R and channel length L.



(a) **(b)**

Fig. 11. (a) Schematic diagram of a GAA-NCFET [18], and **(b)** Cross sectional view of a GAA-NCFET.

1D Poisson's equation along radial direction for an undoped (or) lightly doped GAA-FET is given by [19]

$$\frac{1}{r}\frac{d\psi}{dr} + \frac{d^2\psi}{dr^2} = \frac{q}{\epsilon_{si}} n_i e^{\frac{q(\psi - v)}{kT}} \qquad (11)$$

The surface potential (ψ_s) across the channel is obtained by solving the above differential equation.

$$\psi_s = V - \frac{2kT}{q} \ln\left[\frac{R}{2L_{Di}\beta}(1-\beta^2)\right] \text{ and } 0 < \beta < 1 \qquad (12)$$

$L_{Di} = \left(\frac{2E_{Si}kT}{q^2 n_i}\right)^{\frac{1}{2}}$ is the intrinsic Debye length, β is the intermediate parameter and V is the quasi Fermi potential.

$V_{FE} = a_0 Q + b_0 Q^3$ from the LK equation.

$$a_0 = 2aR \ln\left[1 + \frac{t_{FE}}{(R+t_{ins})}\right], \quad b_0 = 2bR^3 \left[\frac{1}{(R+t_{ins})^2} - \frac{1}{(R+t_{ins}+t_{FE})^2}\right]$$

By applying voltage law [18],

$$V_g - V_{ins} - \Delta\phi - \psi_s = a_0 Q + b_0 Q^3$$

$$V_{ins} = \frac{Q}{C_{ins}} \quad \Rightarrow V_g - \Delta\phi - \psi_s = \left(a_0 + \frac{1}{C_{ins}}\right) Q + b_0 Q^3$$

From Gauss law [18], $Q = \epsilon_{Si} \frac{d\psi}{dr}|_{r=R} = \left(\frac{2kT}{q}\right)\left(\frac{2\epsilon_{Si}}{R}\right)\left(\frac{\beta^2}{1-\beta^2}\right)$, we obtain [18],

$$\ln(\beta) - \ln(1-\beta^2) + m\left(\frac{\beta^2}{1-\beta^2}\right) + n\left(\frac{\beta^2}{1-\beta^2}\right)^3 - G = 0 \qquad (14)$$

$$G = \frac{q(V_g - \Delta\phi - V)}{2kT} - \ln\left(\frac{2L_{Di}}{R}\right) \qquad (15)$$

$$m = \left(a_0 + \frac{1}{C_{ins}}\right)\left(\frac{2\epsilon_{Si}}{R}\right) \qquad n = b_0\left(\frac{2\epsilon_{Si}}{R}\right)^3\left(\frac{2kT}{q}\right)^2 \qquad (16)$$

Aluminium doped hafnia is used as the FE material due to superior scaling properties, which has ferroelectric landau coefficients, a = -3×10^9 m/F and b = 6×10^{11} m^5/C^2F [18]. The interfacial layer is modelled with 1nm thick SiO_2. $\Delta\Phi = -0.3V$ is the work function difference between the gate metal and the substrate [18]. The intermediate parameter β is an implicit function of gate voltage (V_G), quasi Fermi potential, ferroelectric material and its thickness (t_{FE}), channel radius (R) and intermediate oxide thickness(t_{ins}). As β could not be evaluated explicitly, it can be approximated by making an initial guess followed by a number of iterations to improve the initial guess. Or else, β could be evaluated implicitly by graphically solving it by load line analysis.

4.2 Load Line Analysis to Solve for the Intermediate Parameter

From equations (14) and (15),

$F(\beta) = G_1$ at the drain end of the channel where $V = V_d = V_{ds} \Rightarrow \beta = \beta_d$.

$$G_1 = \frac{q(V_g - \Delta\phi - V_{ds})}{2kT} - \ln\left(\frac{2L_{Di}}{R}\right) \qquad (17)$$

$F(\beta) = G_2$ at the source end of the channel where $V = V_s = 0 \Rightarrow \beta = \beta_s$.

$$G_2 = \frac{q(V_g - \Delta\phi)}{2kT} - \ln\left(\frac{2L_{Di}}{R}\right) \qquad (18)$$

G_1 and G_2 are the load lines which are functions of gate voltage. The intersection point of the load line G_1 with F(β) gives β_d and the intersection point of the load line G_2 with F(β) gives β_s.

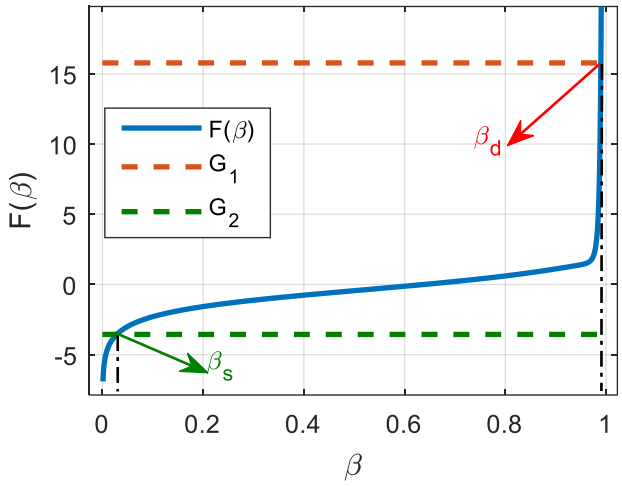


Fig. 12. Load line analysis for determining intermediate parameter β at t_{FE}=8nm and R=10nm.

4.3 Explicit Approximation of Intermediate Parameter

For lower values of gate voltage, β is also small. Hence, the logarithm term becomes dominant and equation (14) can be approximated by neglecting other terms [18]. β_l is the lower asymptotical value of β. For lower values of gate voltage β is close to β_l.

$$ln(\beta_l) = G$$

$$\Rightarrow \beta_l = \exp(G) \qquad (19)$$

For higher values of gate voltage, β is also large. Hence, the logarithm term becomes insignificant. Either second or third term becomes dominant in this case. For the sake of avoiding imaginary values of β, G is replaced by G_0, so that G_0 is always positive [18].

$$G_0 = G + ln(2L_{Di}/R) + qV/2kT \qquad (20)$$

$$\beta_{H1} = \left(\frac{G0}{m + G0}\right)^{0.5} \qquad (21)$$

$$\beta_{H2} = \left(\frac{G0^{\frac{1}{3}}}{n^{\frac{1}{3}} + G0^{\frac{1}{3}}}\right)^{0.5} \qquad (22)$$

$$\beta_{H12} = \beta_{H1} - \beta_{H2} - \Delta$$

Δ is the smoothing parameter used to smoothly join β_{H1} and β_{H2}.

Let $\Delta = 0.15$ for the best possible smoothing approximation.

$$\beta_H = \beta_{H1} - 0.5\left(\beta_{H12} + \sqrt{\beta_{H12}^2 + 4\Delta\beta_{H1}}\right) \qquad (23)$$

β_H is the initial guess for higher asymptotical value of β. For higher values of gate voltage β is close to β_H. To improve the initial guess, β_H is further approximated by carrying out higher order iterations [18],[20].

Let $\left(\frac{\beta^2}{1-\beta^2}\right) = z$

$$\Rightarrow \beta = \sqrt{z/(z+1)}$$

$$\ln\left(\sqrt{z+z^2}\right) + mz + nz^3 - G = 0 \qquad (24)$$

$$\left(\frac{\beta_H^2}{1-\beta_H^2}\right) = z_0$$

Since logarithm term in equation (24) is insignificant for higher asymptotical values, it can be omitted [20].

$$f(z) = mz + nz^3 - G = 0$$

$$f0 = f(z_i) \quad f1 = f'(z_i) \quad f2 = f''(z_i)$$

$$z_{i+1} = z_i - \frac{f0}{f1}\left(1 + \frac{f0f2}{2f1^2}\right) \qquad (25)$$

$$\beta_H(corrected) = \sqrt{z_{i+1}/(z_{i+1}+1)} \qquad (26)$$

Now, β can be obtained by smoothly joining β_H and β_l.

$$\beta_d = \beta_H - \beta_l - \Delta$$

$$\Delta = 0.15$$

$$\beta = \beta_H - 0.5\left(\beta_d + \sqrt{\beta_d^2 + 4\Delta\beta_H}\right) \quad (27)$$

To further improve of the initial guess of β, similar approximation as shown above is carried out.

$$\left(\frac{\beta^2}{1-\beta^2}\right) = z_0$$

$$g(z) = \ln\left(\sqrt{z+z^2}\right) + mz + nz^3 - G = 0 \quad (28)$$

$$g0 = g(z_i) \quad g1 = g'(z_i) \quad g2 = g''(z_i)$$

$$z_{i+1} = z_i - \frac{g0}{g1}\left(1 + \frac{g0g2}{2g1^2}\right) \quad (29)$$

$$\beta(corrected) = \sqrt{z_{i+1}/(z_{i+1}+1)} \quad (30)$$

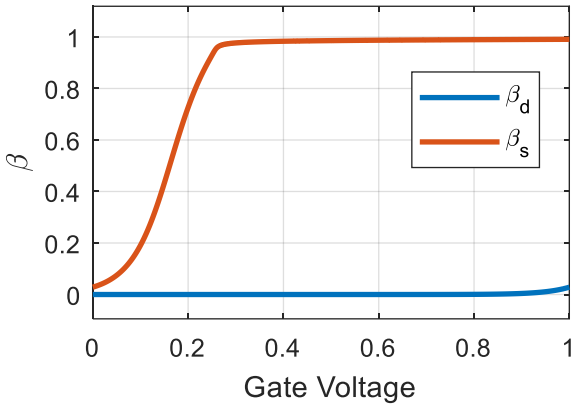


Fig. 13. Intermediate parameter β vs. gate voltage after series of approximations at t_{FE}=8nm and R=10nm [18].

Chapter 5

Performance of GAA-NCFET

5.1 Constraints for Stable Operation

$$SS = \left(60 \times \frac{dV_g}{d\psi_s}\right) mv/dec \qquad (31)$$

$$\frac{dV_g}{d\psi_s} = 1 + \frac{2\beta^2}{(1-\beta^4)}\left[m + \frac{3n\beta^4}{(1-\beta^2)^2}\right] \qquad (32)$$

For $\frac{dV_g}{d\psi_s} < 0$, surface potential is a doubled valued function of gate bias, which is not desirable. Hence, $\frac{dV_g}{d\psi_s} \geq 0$ for stable operation. And $\frac{dV_g}{d\psi_s} < 1$ to achieve gate voltage amplification at the interface, thus achieving the steep slope. Hence, for hysteresis free operation, the condition to be satisfied is

$$0 \leq \frac{dV_g}{d\psi_s} < 1 \qquad (33)$$

The FE material used, FE thickness (t_{FE}), channel radius (R) and insulating oxide thickness (t_{ins}) determine the operational characteristics of GAA-NCFET. The surface potential (ψ_s) is plotted as a function of gate voltage (V_g) using implicit formulation.

5.2 Impact of FE oxide thickness on GAA-NCFET operation

$$body\ factor = m = 1 + \left(C_s/C_{eq}\right) = 1 + (C_s/C_{FE}) + (C_s/C_{ins}) \qquad (34)$$

$$SS = 60 \times [1 + (C_s/C_{FE}) + (C_s/C_{ins})]\ mV/decade \qquad (35)$$

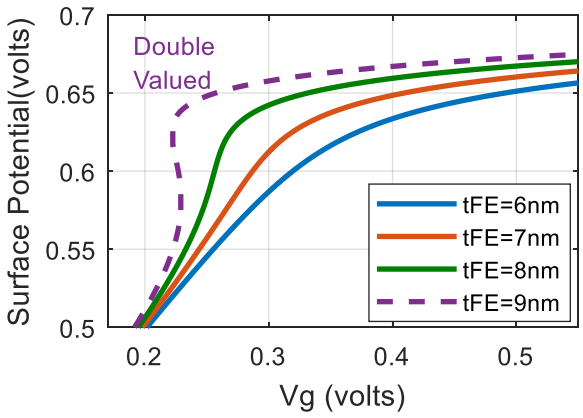


Fig. 14. Variation of Surface potential vs. gate voltage for various FE thickness at R=10nm [18].

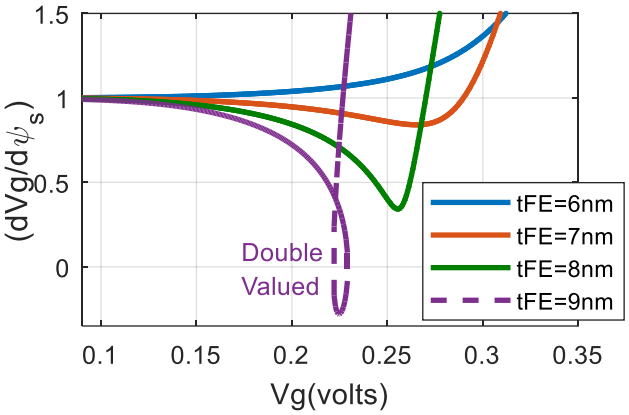


Fig. 15. Variation of derivative function ($dV_g/d\psi_s$) vs. gate voltage for various FE thickness at R=10nm.

As the FE thickness is increased, the FE capacitance (C_{FE}) becomes less negative leading to greater gate voltage amplification and lower SS. But if the FE thickness is increases beyond a particular limit, the surface potential becomes double valued function of gate voltage leading to unstable hysteretic operation. In the fig. 14 stable operation is observed until t_{FE} = 8nm and double valued function is observed at t_{FE} = 9nm and above. The negative slope in the plot in fig. 14 corresponds to double valued function. Thus, the derivative plot gives a clear picture about the stable operation. Negative value of the derivative shown in the fig. 15 indicates the double valued function.

5.3 Impact of channel radius on GAA-NCFET operation

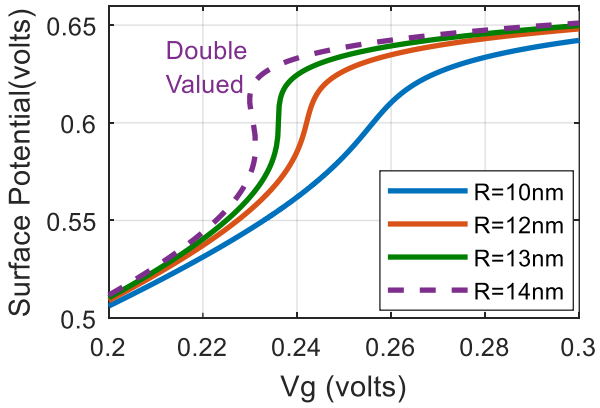


Fig. 16. Variation of Surface potential vs. gate voltage for various channel radii (R) at t_{FE} =8nm.

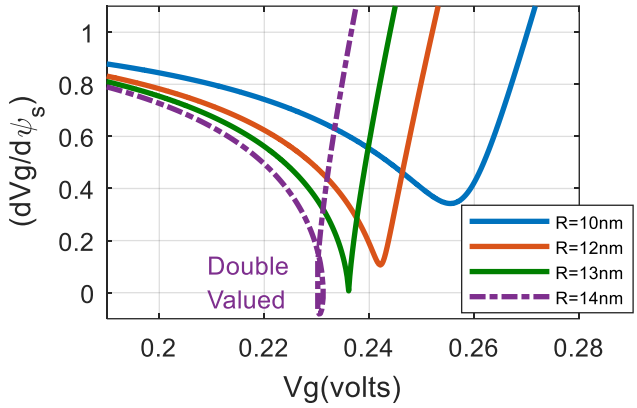


Fig. 17. Variation of derivative function ($dV_g/d\psi_s$) vs. gate voltage for various channel radii at t_{FE} =8nm.

As the channel radius (R) increases, the channel capacitance (or) the substrate capacitance (C_s) decreases leading to lower SS. But if R increases beyond a particular limit, the surface potential becomes double valued function of gate voltage leading to unstable hysteretic operation. In the fig. 16 stable operation is observed until R=13nm and double valued function is observed at R=14nm and above. The negative slope in the plot in fig. 16 corresponds to double valued function. Negative value of the derivative shown in the fig. 17 indicates the double valued function.

5.4 Impact of insulating oxide thickness on GAA-NCFET operation

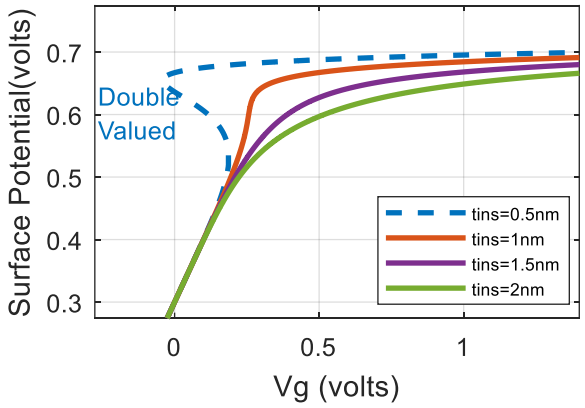


Fig. 18. Variation of Surface potential vs. gate voltage for various t_{ins} at R=10nm and t_{FE}=8nm.

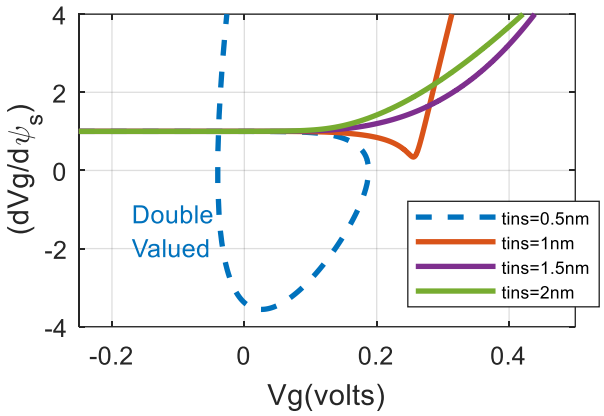


Fig. 19. Variation of derivative function ($dV_g/d\psi_s$) vs. gate voltage for various t_{ins} at R=10nm and t_{FE}=8nm.

As the insulating oxide thickness (t_{ins}) decreases, the insulator capacitance (C_{ins}) decreases leading to lower SS. But if t_{ins} is decreased below a particular limit, the surface potential becomes double valued function of gate voltage leading to unstable hysteretic operation. In the fig. 18 stable operation is observed at t_{ins} =1nm and double valued function is observed at t_{ins} =0.5nm and below. The negative slope in the plot in fig. 18 corresponds to double valued function. Negative value of the derivative shown in the fig. 19 indicates the double valued function.

5.5 Operating limits of GAA-NCFET

The stable operational limits of GAA-NCFET can be determined by studying the derivative function ($dV_g/d\psi_s$). The lower limit of the operation comes from the condition that gate voltage amplification should happen leading to sub-kT SS. The upper limit comes from the stability (or) hysteresis free operation condition.

5.5.1 Lower limit of operation

$$SS < 60\ mV/decade \Rightarrow \frac{dV_g}{d\psi_s} < 1$$

From the equation (32)

$b_0 > 0$ for the FE materials SBT as well as Aluminium doped hafnia.

$\Rightarrow n > 0$

$\frac{dV_g}{d\psi_s} < 1 \Rightarrow m < 0$ (36)

Hence, m < 0 defines the lower limit of operation. It is observed that at the lower limit, SS is exactly 60 mV/decade.

5.5.2 Upper limit of operation

$$\frac{dV_g}{d\psi_s} \geq 0\ for\ stable\ operation$$

The upper limit can be determined graphically by plotting the derivative function ($dV_g/d\psi_s$) and ensuring that the derivative is non negative. It is observed that at the upper limit zero SS and abrupt switching is achieved.

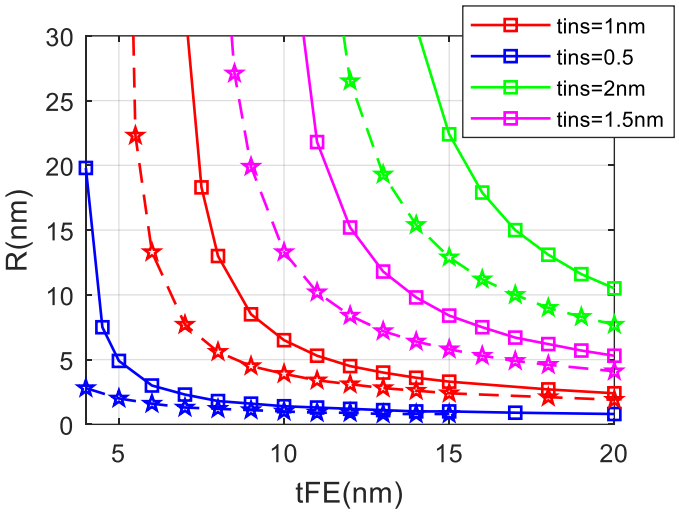


Fig. 20. Operating limits of GAA-NCFET with Al doped hafnia as FE material.

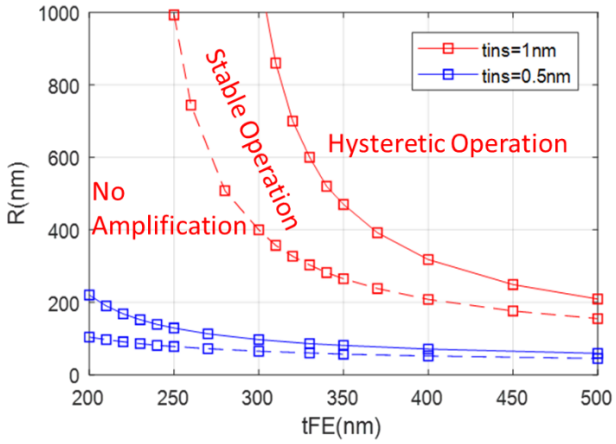


Fig. 21. Operating limits of GAA-NCFET with SBT as FE material.

The stable operating range of GAA-NCFET is shown in fig. 20 and fig. 21. The solid line represents upper limit of operation and the dashed line represents the lower limit of operation. Region in between the lower limit and upper limit is the stable operating region. The FE thickness, channel radius and insulating oxide thickness should be chosen within the stable operating region. Region above the upper limit represents the unstable (or) hysteretic operation and the region below represents the no amplification (or) no steep slope region. Greater scalability of Hafnia-based FE over perovskite-based FE is also observed while comparing fig. 20 and fig. 21, as the former operates at very low values of t_{FE} and R while compared to the latter.

5.6 Drain Current Characteristics

The drain current (I_{ds}) is given by [18],

$$I_{ds} = (2\pi R)\mu Q\frac{dV}{dy} \;\Rightarrow\; I_{ds} = \mu\frac{2\pi R}{L}\int_{V_s}^{V_d} Q(V)\,dV$$

$$I_{ds} = \mu\frac{2\pi R}{L}\int_{\alpha_s}^{\alpha_d} Q(\alpha)\frac{dV}{d\alpha}d\alpha \quad \text{where } \alpha = 1-\beta^2$$

$$I_{ds} = \frac{8\pi\epsilon_{Si}\mu}{L}\left(\frac{kT}{q}\right)^2[f(\alpha_d)-f(\alpha_s)]$$

$$f(\alpha) = -\frac{2}{\alpha} - \ln(\alpha) + m\left(-\frac{1}{\alpha^2}+\frac{2}{\alpha}\right) + n\left(\frac{6}{\alpha}-\frac{9}{\alpha^2}+\frac{6}{\alpha^3}-\frac{3}{2\alpha^4}\right)$$

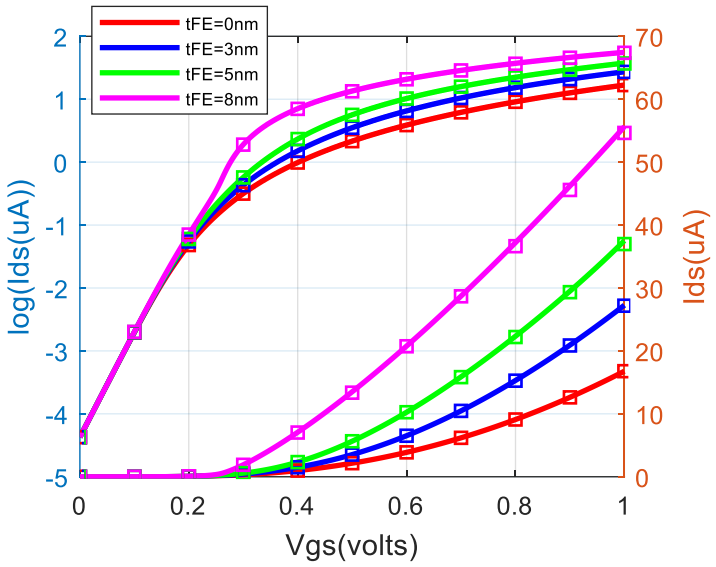


Fig. 22. Drain Current vs. gate voltage characteristics for R=10nm, t_{ins}=1nm and Al doped hafnia as FE material [18].

GAA-NCFET shows significant improvement in the current characteristics from the conventional GAA-FET [18]. The ON current is observed to be higher than that of conventional device. The OFF current is observed to be approximately same for both the devices. Hence, the ON to OFF current ratio is higher for a negative capacitance device.

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

The potential use of negative capacitance resolving the power crisis in improving the performance of MOSFET is studied. Working of NCFET and the role of sub-60 mV/decade subthreshold swing in improving switching characteristics are studied. Performance of GAA-NCFET is studied. The constraints for stable hysteresis free operation of NCFET and the operating limits for stable operation are determined. Significant improvement in ON current is observed. The greater scalability of doped hafnia-based ferroelectrics over perovskite-based ferroelectrics is observed.

6.2 Future Scope

We studied the performance of MOSFET with Gate-All-Around Architecture in this project. Similar analogy can be extended to study the performance of MOSFET with different topology like a double gate MOSFET and a FinFET. The operational limits are determined graphically in our work. An explicit mathematical model can be developed for determining the operational limits in the future.

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