B. TECH. PROJECT REPORT

On

‘‘OPTIMISATION AND EFFECTIVE GaN SURFACE PASSIVATION BY PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION OF SILICON OXIDE’’

BY

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DISCIPLINE OF

METALLURGY ENGINEERING AND MATERIALS SCIENCE

INDIAN INSTITUTE OF TECHNOLOGY INDORE

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OPTIMISATION AND EFFECTIVE GaN SURFACE PASSIVATION BY PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION OF SILICON OXIDE

A PROJECT REPORT

Submitted in partial fulfillment of the
requirements for the award of the degrees

of
BACHELOR OF TECHNOLOGY
in

METALLURGY ENGINEERING AND MATERIALS SCIENCE

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INDIAN INSTITUTE OF TECHNOLOGY INDORE

DECEMBER, 2019

CANDIDATE'S DECLARATION

I hereby declare that the project entitled **''Optimisation and effective GaN surface passivation by Plasma Enhanced Chemical Vapor Deposition of silicon oxide"** submitted in partial fulfillment for the award of the degree of Bachelor of Technology in 'Metallurgy Engineering and Materials Science' completed under the supervision of **Dr. Parasharam M. Shirage, Head of Department**, Metallurgy Engineering and Materials Science, **IIT Indore** & **Dr. Abdelatif Jaouad, Associate Professor**, Department of Electrical and Computer Engineering, **University of Sherbrooke,** at IIT Indore is an authentic work.

Further, I declare that I have not submitted this work for the award of any other degree elsewhere.

20-11-2019

Ashutosh Gupta

Signature and name of the student(s) with date

CERTIFICATE by BTP Guide(s)

It is certified that the above statement made by the students is correct to the best of my/our knowledge.

Dr. Parasharam M. Shirage	Dr. Abdelatif Jaouad
(Head of Department)	(Associate Professor)
IIT Indore	University of Sherbrooke

Signature of BTP Guide(s) with dates and their designation

Preface

This report on "**Optimisation and effective GaN surface passivation by plasma enhanced chemical vapor deposition of silicon oxide**" is prepared under the guidance of Dr. Parasharam M. Shirage and Dr. Abdelatif Jaouad.

This report is concerned with surface passivation and development of the metal-oxide-semiconductor capacitors (MOSCAP) in a class 100 CLEANROOM (3IT.Nano Platform) and its electrical characterization in the Laboratory of Characterization and Synthesis of Materials (LCSM). This report describes the necessary concepts involved in the fabrication of MOSCAP. The main objective of this report is to optimize the PECVD parameters (pressure, temperature, silane flow, etc.) in order to reduce the interface state density and improve the electrical characteristics and stability of the device.

The introductory part presents the basic layout of this report. It introduces the reader to III-V group semiconductors and application of GaN in electronic devices. In the next chapter, experimental procedures along with the development of the LabVIEW program for the electrical characterization of the device is described to introduce the reader to the concept of Nano-fabrication and effective surface passivation of GaN. Further, the analytical method used such as Terman's method is described. In the last chapter, conclusions about the applicability of the standard PECVD process and suggestions for the future modifications and enhancements are given. The content of the report is tried to be explained in a lucid manner with the best of my abilities and knowledge.

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I wish to thank Dr. Parasharam M. Shirage and Dr. Abdelatif Jaouad for their kind support and valuable guidance. I thank Dr. Abdelatif for allowing me the pleasure to join his group, allocating financial support and providing guidance that has helped me to mature inside and outside of the laboratory. The knowledge and experience I gained while working in Dr. Abdelatif`s group will serve as a solid foundation as I move forward into my academic and professional career. I would like to give special thanks to Mr. Olivier Richard (Ph.D. research fellow) for guiding me throughout the project. Together, we have maintained equipment within our labs and worked with each other on understanding our data.

It is their help and support, due to which I became able to complete the design and technical report.

Without their support this report would not have been possible.

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Abstract

This report deals on an effective and stable process for GaN surface passivation by plasma enhanced chemical vapor deposition (PECVD) of silicon oxide (SiOx) which was developed by optimisation of PECVD parameters. Metal-oxide-semiconductor (MOS) capacitors were fabricated on Mg-doped p-GaN and unintentionally doped n-GaN layers grown by Hybrid Vapor Phase Epitaxy on sapphire (Al_2O_3) substrates and characterized using capacitance-voltage (C-V), conductance-voltage (G-V), conductance-frequency (G-w) and current-voltage (I-V) measurements at room temperature and at temperatures ranging from 20 °C to 140 °C with a step of 20 °C. A high level of surface potential modulation, a small voltage shift, a small hysteresis, and no evident frequency dispersion are observed on C-V characteristics, indicating a high SiOx/GaN interface quality with a low electronic surface state density. Effect of different PECVD deposition parameters (temperature, pressure, SiH4 flux, and RF Power) on interface state density (D_{it}), Hysteresis, and flat-band-voltage (V_{fb}) was also analysed. It was found that Pressure (P) and temperature are the most important parameters in affecting D_{it}; Silane (SiH4) flux and RF power (W) are the most important parameters in affecting V_{fb}; Pressure (P) and temperature are the most important parameters in affecting Hysteresis. Apart from this, in order to understand the properties in the bulk of SiO_x film, Fourier-transform infrared spectroscopy (FTIR) was performed on SiO_x deposited over silicon samples using same parameters in PECVD. In order to remove the affect of native oxide during spectroscopy, samples were treated with buffered oxide etch (BOE) solution. It was found that a peak of SiO2 is present at around 1100 cm^{-1} wavenumber along with Si-O rocking and Si_2O_3 as well as Si-OH bond was found for few samples. C-V measurement was done for the n-type samples at a very low delay time for around 5-6 times in order to determine the stability of the device.

Keywords: Gallium nitride; passivation; semiconductor-insulator interfaces; FTIR; PECVD.

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Chapter 1

Introduction

This chapter describes the aim of the research project and various challenges faced in passivation of III-V group semiconductor devices. Methods involved for the development and characterization of GaN metal-oxide semiconductor capacitor (MOSCAP) and the contents of corresponding chapters are briefly explained.

1.1 Introduction to III-V group semiconductors

The important III–V compound semiconductors are derived from atomic combinations arising from columns III A (e.g., Al, Ga, In) and V A (e.g., N, P, As) of the periodic table. III–V semiconductors (such as InP, InAs, GaAs, GaN, and InSb) [shown in Table 1.1] find wide applications in high-performance optoelectronic devices owing to their superior electronic properties including high electron mobility, direct band gap, and low exciton binding energy [1]. Optoelectronic devices based on nitride ternary alloys can operate at energies in the mid ultraviolet all the way to infrared. Recent interest in short wavelength light emitting diodes (LEDs) and laser diodes (LDs) has led to the development of nitride-based blue LEDs and ultraviolet LDs, with a wide range of applications. Due to its superior fundamental properties such as direct wide band gap, large critical electric field and high electron saturation velocity, gallium nitride (GaN) is an attractive material for high-power and high-frequency electronic devices operating at high temperature [2].

TABLE 1.1

Group III-V elements

Group III	**Group V**
B	N
Al	P
Ga	As
In	Sb

1.2 Gallium Nitride – a promising III-V group semiconductor

Gallium nitride (GaN) is a binary III/V direct bandgap semiconductor commonly used in light-emitting diodes since the 1990s. The compound is a very hard material that has a Wurtzite crystal structure and can also be grown with zinc blende structure (but wurtzite is more common) [3]. Its wide band gap of 3.4 eV affords it special properties for applications in optoelectronic. GaN transistors are suitable for high frequency, high voltage, high temperature and high efficiency applications. Commercially, GaN crystals can be grown using molecular beam epitaxy or metalorganic vapour phase epitaxy. This process can be further modified to reduce dislocation densities. First, an ion beam is applied to the growth surface in order to create nanoscale roughness. Then, the surface is polished. This process takes place in a vacuum. Since, GaN semiconductors have the capability to operate at higher voltages, temperatures and switching frequencies with greater efficiencies compared to existing Si devices [4], these characteristics not only result in less losses but enables significantly reduced system volume, due to decreased cooling requirements and smaller passive components contributing to overall lower system costs.

1.3 Problem Definition

One of the major challenge is to achieve long-term thermal stability of the contact. At high power and high temperature operating conditions, substantial leakage current occurs, which deteriorates the device performance [5]- [6]. The use of insulated gates in order to reduce this current is limited by the poor quality of dielectric- GaN interfaces which is characterized by a high interface states density (Dit). The achievement of a stable and fully controlled insulator/GaN interface with low Dit has been identified as a critical point for high power GaN technology to increase both voltage break-down and device reliability [7]. Among the large variety of dielectrics investigated for GaN surface passivation, silicon oxide (SiO_x) deposited by plasma enhanced chemical vapor deposition (PECVD) has been explored [8]. The lowest reported D_{it} on an AlGaN/GaN MOS-HEMT device using a PECVD deposition technique is 3.9×10^{11} cm^{-2} eV^{-1} [9] . Successful coupling of dielectrics with high mobility III-V semiconductor requires careful substrate cleaning [10]. The MOS device fabricated on GaN sample was pre-treated with KOH/HCl for best C-V characteristics with an excellent surface modulation, small flat-band shift, and no significant frequency dispersion [11].

In this report, the surface passivation of p- and n-type GaN by PECVD-deposited silicon oxide is investigated. Capacitors with an Al/SiO_x/GaN structure were fabricated and characterized using C-V, G-w, G-V, and I-V measurements. A good surface potential modulation, a small voltage shift, a small hysteresis and no evident frequency dispersion are deduced. This indicates a high quality of the SiO_x/GaN interface with a low electronic

surface state density. The main aim was to fabricate a device with low interface state density, low flat-band voltage shift, and have low hysteresis loss.

Since a complex phenomenon takes place inside the PECVD chamber (Fig. 1.1), with no direct relation between PECVD parameters and the property of the deposited film. So, it was important to optimize these conditions. Hence, eighteen samples (9 of each type) were taken and different parameters were used for each of them for deposition of the film. So that after analysing each sample, best deposited film with assigned parameters can be used further for screening.

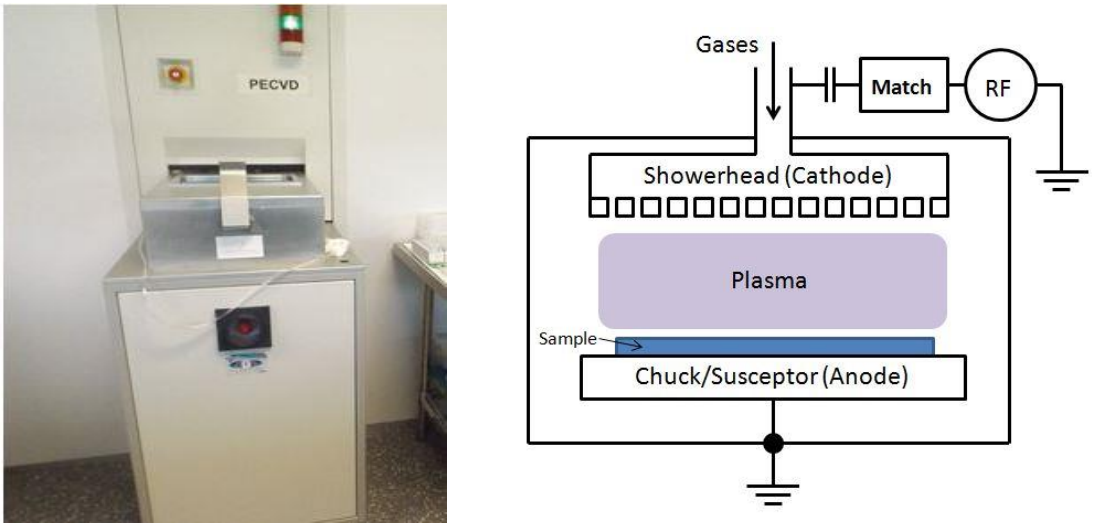


Fig. 1.1. PECVD chamber and its schematic.

1.4 Objectives of the Project

GaN-based devices are considered to be the emerging front-runners to meet the ever growing demand for improved performance in terms of power, operation speed, and efficiency [12]. Needless to say, the high critical electric field of GaN that has allowed unprecedented high voltage operation, also leads to a higher degree of charge injection and trapping, inducing more severe current collapse. Among the different approaches reported in literature to address the current collapse problem, surface passivation has become the standard technique because of its efficacy and simplicity. The main objective of the project is to attain the low flat-band voltage shift, low threshold voltage for device operation, low hysteresis loss, low series resistance, least leakage current, and low interface state density. These parameters contribute to the success of these devices in faster switching power devices with higher breakdown voltage, making it an ideal for advanced power electronic components. In this report we proceed with the surface passivation of GaN MOSCAP in order to reduce interface trap density, and improve other parameters in order to increase the efficiency of these devices.

Chapter 2

Experimentations and Analysis

2.1 Fabrication of GaN MOS capacitors

Gallium nitride MOS capacitors were fabricated (Fig. 2.1 & Fig. 2.2) on commercial, Mg-doped p- and unintentionally doped n-type GaN layer grown by hybrid vapor phase epitaxy (HVPE) on sapphire substrates. The thickness of the GaN layer was around 4.5 µm (p-type) and 5 µm (n-type). The doping concentration is in the range of (1-3) × 10^{16} cm^{-3} for the n-type samples as extracted from C-V measurements, while for p-type, doping concentration can't be extracted as devices have pinned surface fermi level. The samples (8 p-type and 8 n-type) were cleaned with organic solvents- acetone and isopropyl alcohol (IPA). Samples are first dipped in acetone for 15 min and then kept for 10 min in IPA.

After cleaning with these solvents, samples are rinsed with deionized (DI) water for around 5 min and finally dried using nitrogen blow. Prior to the oxide layer deposition, the samples are treated sequentially in KOH and HCl aqueous solutions for around 3 min and 1 min 30 sec respectively, with being rinsed with DI water between each step for 30 sec. Finally, they are dried with nitrogen blow. Special precautions were taken during cleaning to avoid GaN surface recontamination. The samples were then immediately transferred into the PECVD reactor chamber and a 20-30 nm silicon oxide (SiO_x) layer was deposited onto the GaN surface (the thickness vary for each sample). Silane (SiH_4), nitrous oxide (N_2O), and nitrogen (N_2) were used as gas mixture. The pressure in the deposition chamber, platen power and deposition temperature were varied for each sample for the optimisation. After the deposition of the oxide layer, metal grid of Aluminium (Al) of thickness 350nm was deposited over the insulating oxide. A standard photolithography process, followed by a wet etch in a mixture of H_3PO_4, HNO_3 and CH_3COOH-based solution around 30-35 °C was used to define circular insulator regions.

Again, the samples were cleaned with organic solvents (in acetone for 30 min - 1 hr and in IPA for 5 min) in order to remove resin, rinsed with DI water and dried with N_2 blow. A second photolithography process was used for the deposition of a bi-layer resin followed by oxygen plasma cleaning and finally wet etched in HF-based solution. Ohmic contacts, consisting of a Ti/Al (35/315 nm) layer stack, were then evaporated on the GaN surface to form a large metal contact around the MOS capacitors. Finally, a liftoff process was used to define circular aluminium contacts on top of the SiO_x.

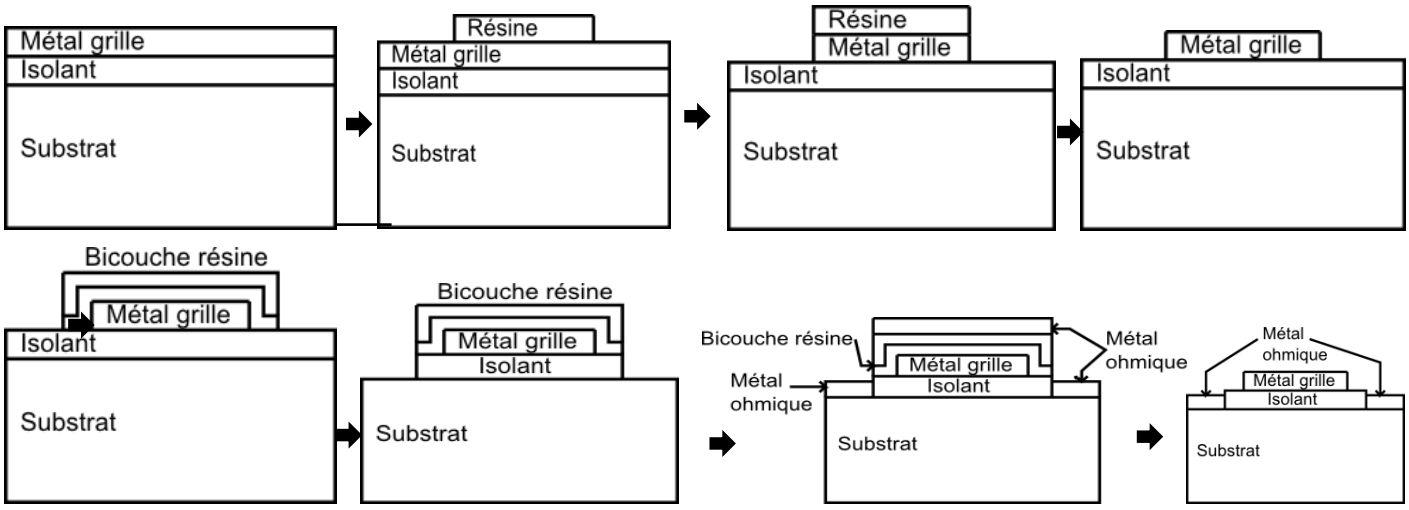
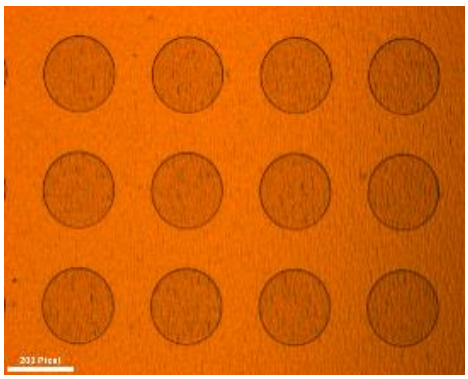
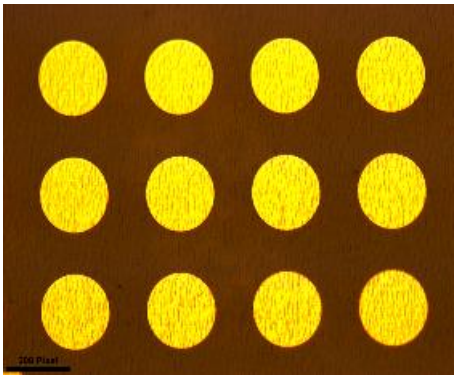


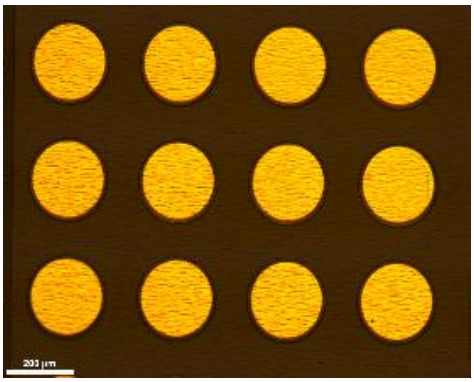
Fig. 2.1. Overall fabrication process of GaN MOSCAP.



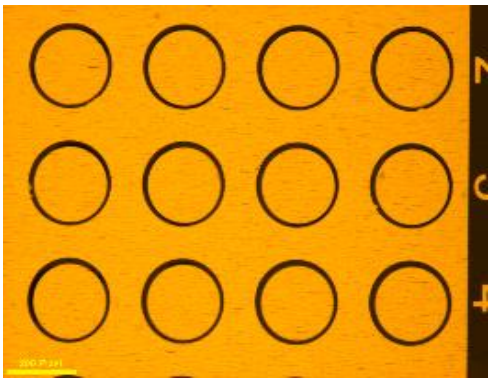
Photolithography I



Al- etch



Photolithography II



Lift-off

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Fig. 2.2 Microscopic images of fabricated GaN MOSCAP.

2.2 LabVIEW program for electrical characterization of MOSCAP

Electrical characterization (C-V, G-w measurements) were performed on Solartron SI 1260 Impedance Gain-Phase Analyzer which uses GPIB module to operate it. In order to operate automatically, a LabVIEW program was required. The old version of the program with the research group doesn't had enough operating conditions and wasn't able to deliver results required for the project.

The concept used in the program is given in Fig. 2.3. The program needed to include this algorithm with a delay at each voltage step in order to stabilize the measurements plus a delay between the frequency sweeps in order for Solartron to record and store the data.

The modified program had many benefits such as- it includes a STOP button functioning, less time consuming measurements, and having only particular readings while skipping other that are not required.

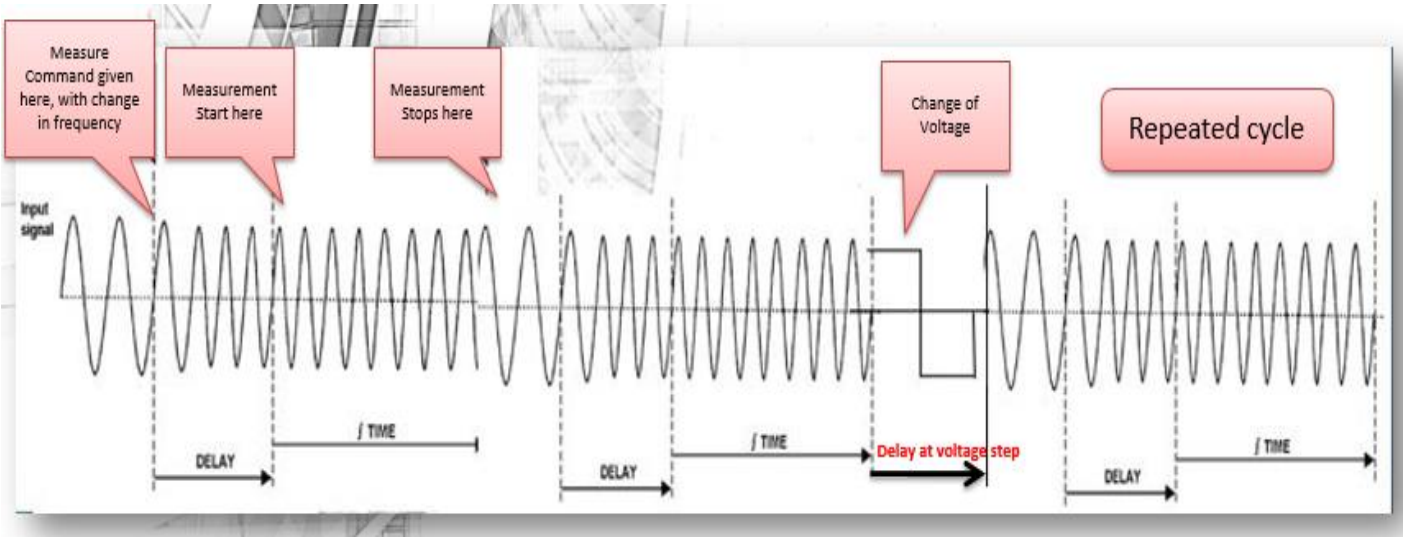


Fig. 2.3 Algorithm for measurement of G-w using Solartron

The interface of the program is shown in Fig. 2.4. The overall program was deigned during the research project to meet the needs of the experiments. C-V measurements were performed using this program at 10 KHz, 100 KHz, 500 KHz, 1 MHz, 3 MHz, and 5 MHz. Similarly, G-w measurements were performed from -4V to +4V with a step of 0.05V and a time delay of 0.2 sec. The frequency range kept was from 10 KHz to 1.2 MHz. The files were saved in the opted folder with the name given plus a suffix automatically incorporated by the LabVIEW program to the name.

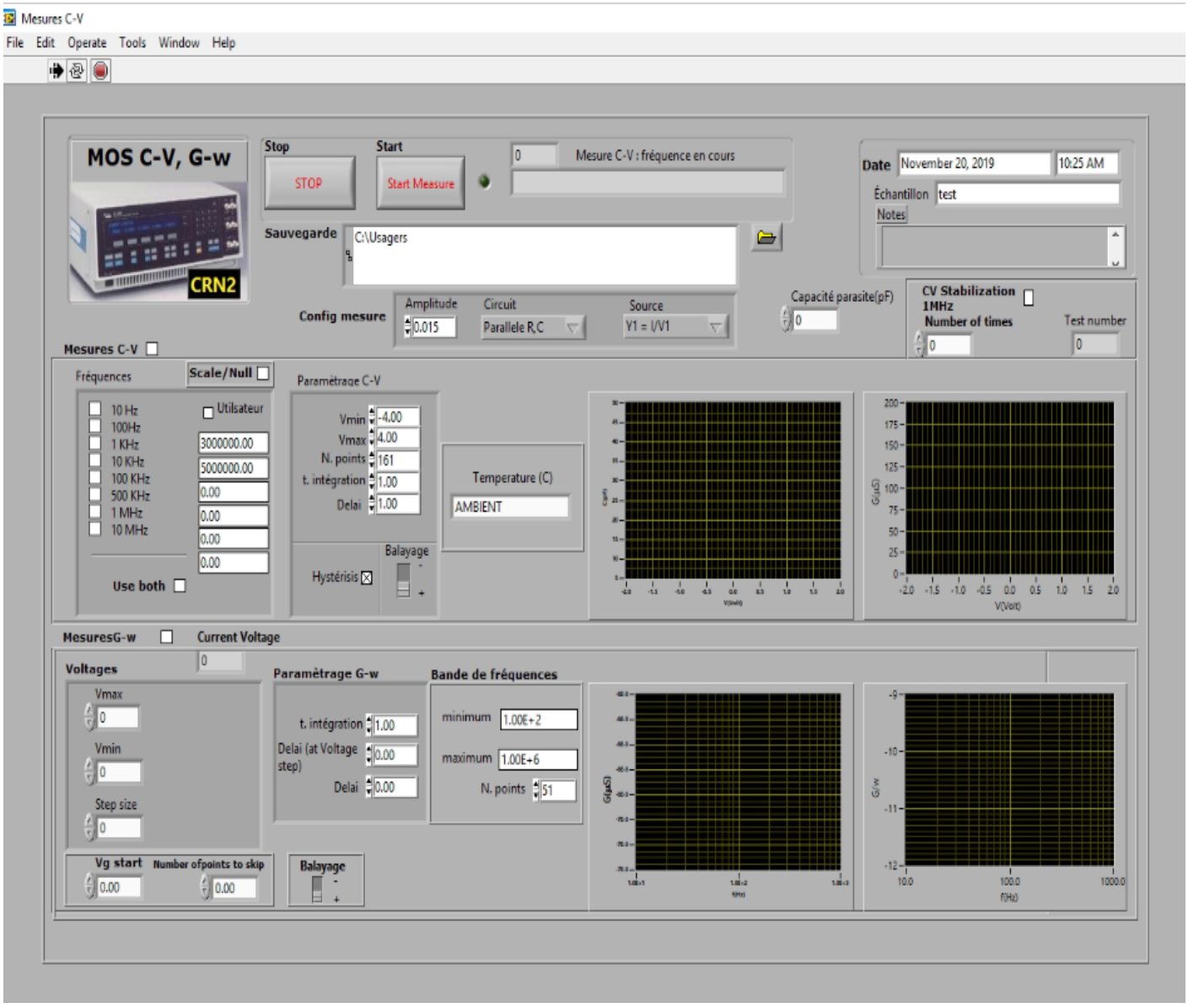


Fig. 2.4 Interface of the C-V and G-w measurement LabVIEW program.

2.3 Characterization of GaN MOS capacitors

Fabricated MOS capacitors were electrically characterized by C-V, G-V, and G-w measurements performed at frequencies between 10 kHz 5 MHz and temperature ranging from 20 ℃ to 140 ℃ using Keithley solartron SI 1260 impedance-gain-phase analyzer on the heating probe station (Fig. 2.5). C-V and G-V measurements were taken for all the eighteen samples for the frequencies 10 KHz, 100 KHz, 500 KHz, 1 MHz, 3 MHz, and 5 MHz at ambient temperature as well as at higher temperatures ranging from 20 ℃ to 140 ℃ with a step of 20 ℃. The voltage sweep was from +4 V to – 4 V (both the direction) with a step of 0.05 V and a varying delay of 0.5 sec to 5 sec. Also, G-w measurements were taken for the frequency range 1 KHz to 12 MHz in the depletion region. The voltage sweep starts from positive to negative voltage for n-type samples and opposite for p-type samples with a step of 0.05 V. Current-voltage (I-V) measurements were taken for all the samples with a voltage sweep same as that for C-V measurements to analyze the leakage current.

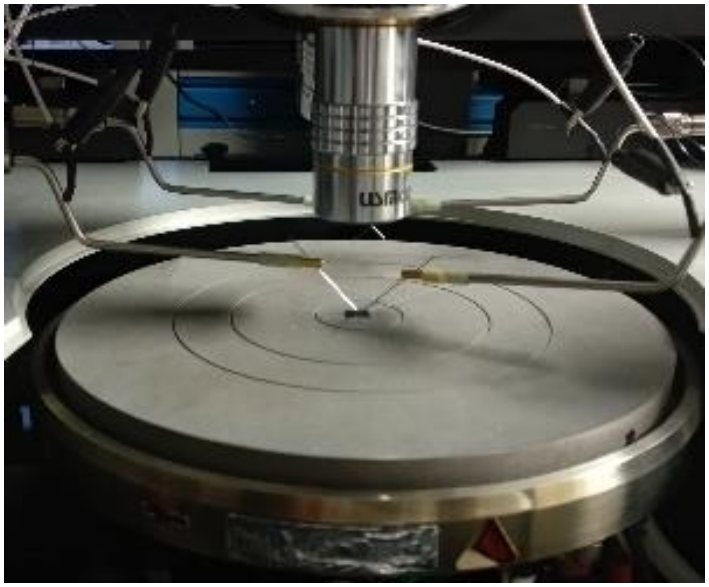


Fig. 2.5. Heating probe station.

In order to determine the stability of the device, again C-V measurements were done but at a low delay time at 1 MHz for approximately 5-6 runs. It was found that the hysteresis loss was reduced and a stable curve was obtained.

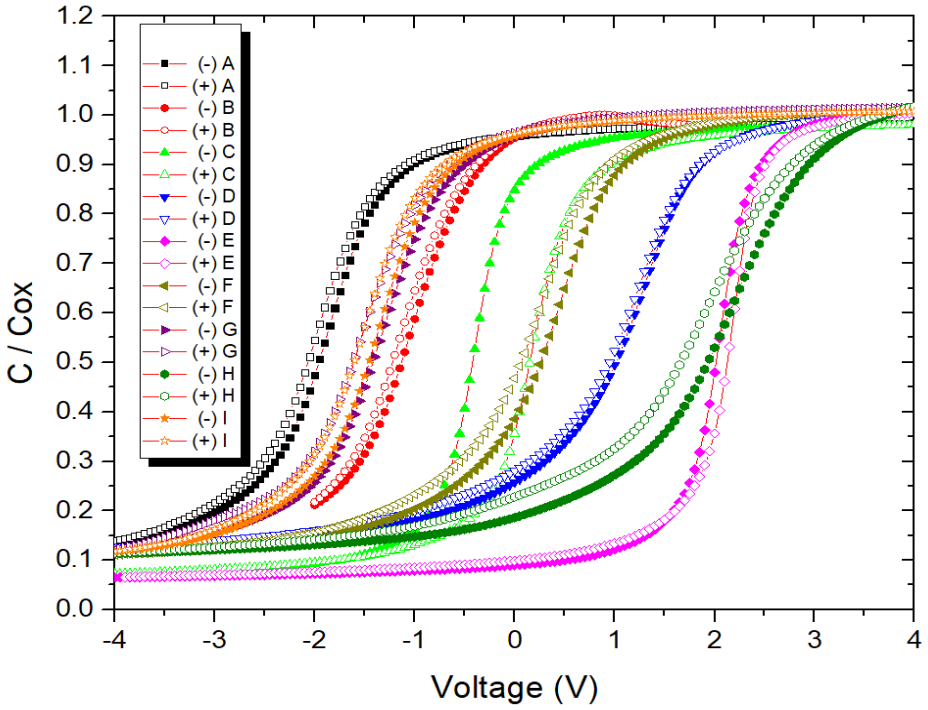
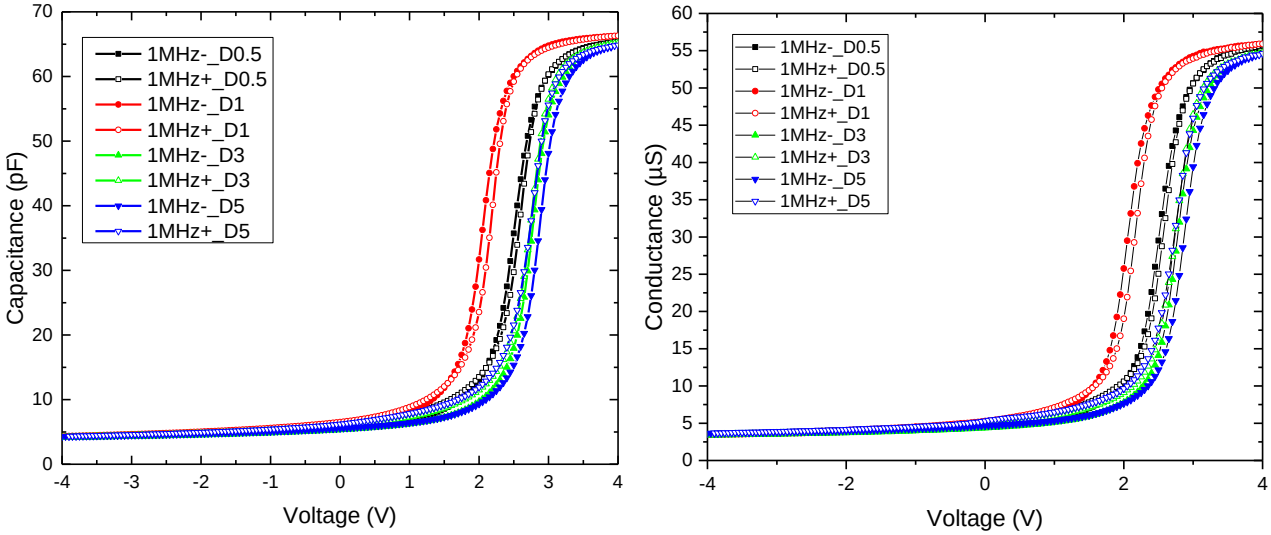


Fig. 2.6. The 1 MHz C-V characteristics of MOS capacitors fabricated on n-type GaN samples pre-treated KOH/HCl.

C-V measurements for different samples at 1 MHz frequency and 1 sec delay time can be seen in Fig. 2.6. Sample –E showed the best C-V and G-V characteristics (Fig. 2.7) among all samples. Consequently, capacitance-frequency and conductance-frequency were plotted in order to analyse the sample (Fig. 2.8).



(i) **(ii)**

Fig. 2.7. The 1 MHz (i) C-V and (ii) G-V characteristics for different Delay time.

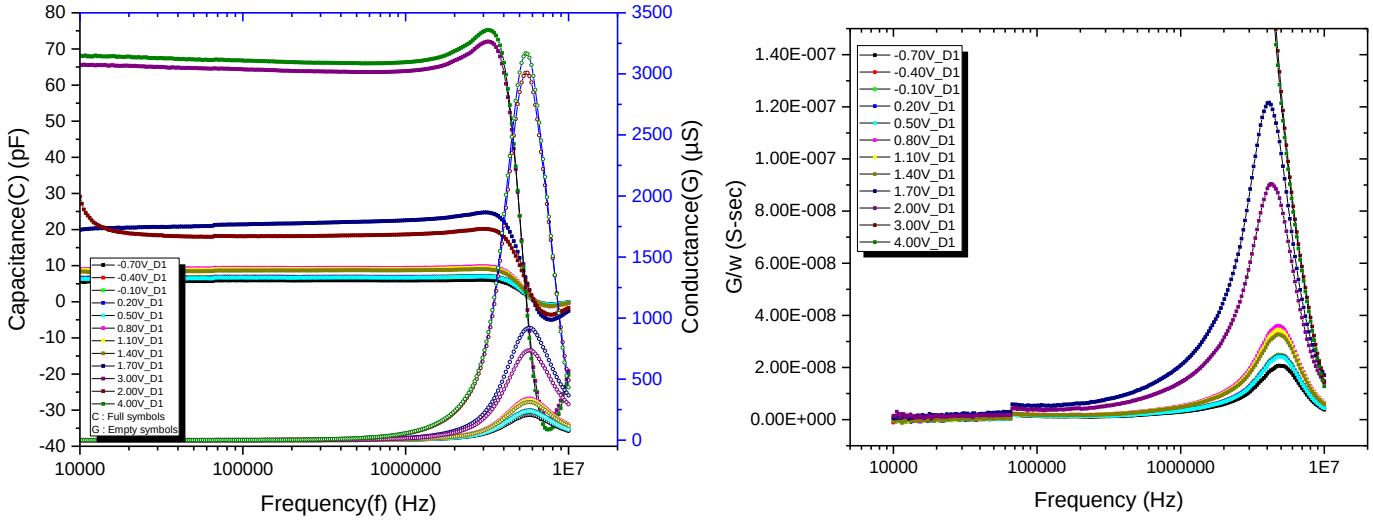


Fig. 2.8. The 1 MHz (i) C-w and (ii) G-w characteristics for different Delay time.

Electrical characterization of all the samples were done once again with same delay time and frequencies but at higher temperatures. C-V measurements were done at 40 °C, 60 °C, 80 °C, 100 °C, 120 °C, and 140 °C and compared with the room temperature measurements (Fig. 2.9).

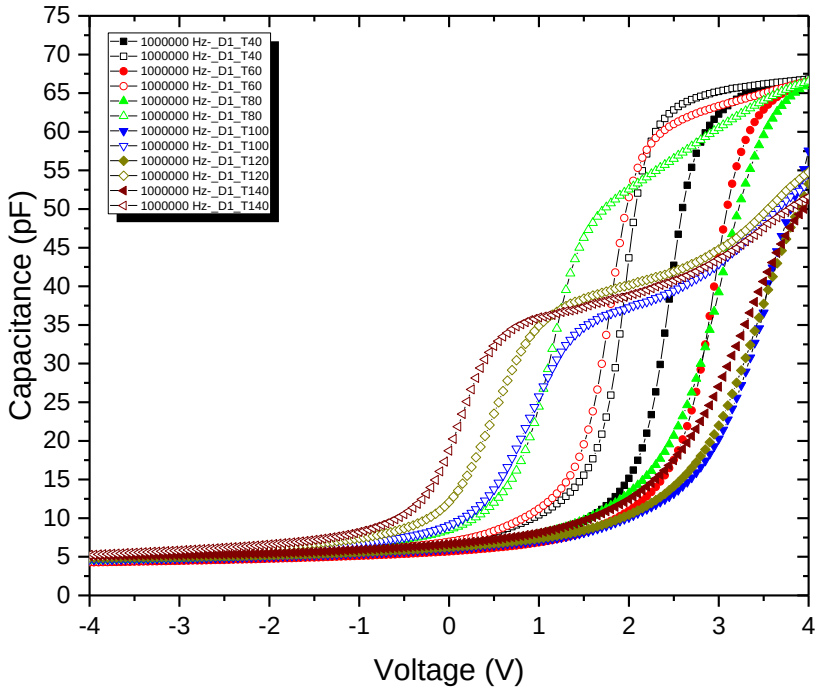


Fig. 2.9. The 1 MHz C-V characteristics of MOS capacitors fabricated on n-type GaN samples at elevated temperatures.

2.4 Extraction of dopant concentration

Extraction of dopant concentration (Fig. 2.10) from high frequency (H.F.) C-V measurements is done by-

$$N(w) = -\frac{2}{q \in_s \frac{d\left(1/C_m{}^2\right)}{dV_g}} \quad (H.F.) \qquad (1)$$

Where N (w) is the dopant concentration; q is the electronic charge; C_m is the measured capacitance; V_g is the gate voltage; and $\in_s = 9 \times 8.85 \times 10^{-12}\ F.m^{-1}$ is the permittivity of the material.

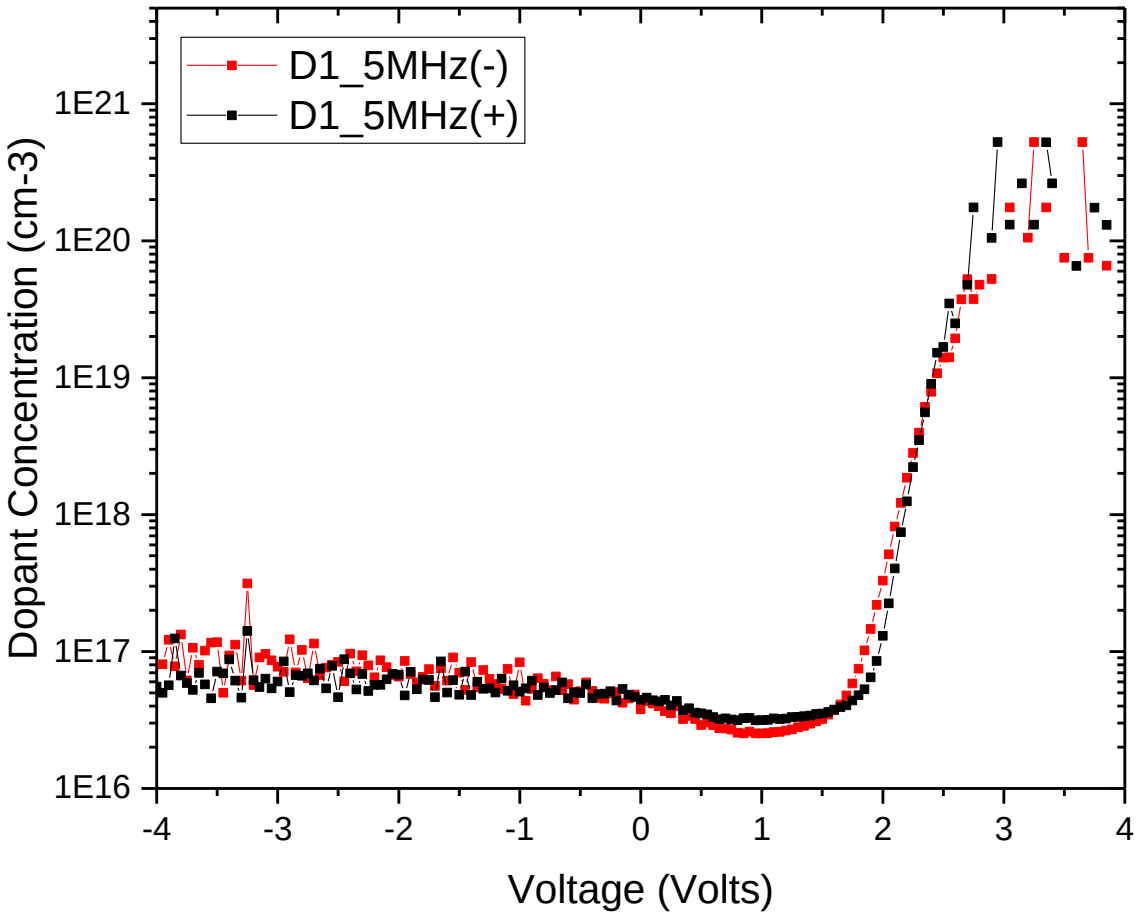


Fig. 2.10. Dopant concentration against gate voltage extracted from H.F. C-V curve.

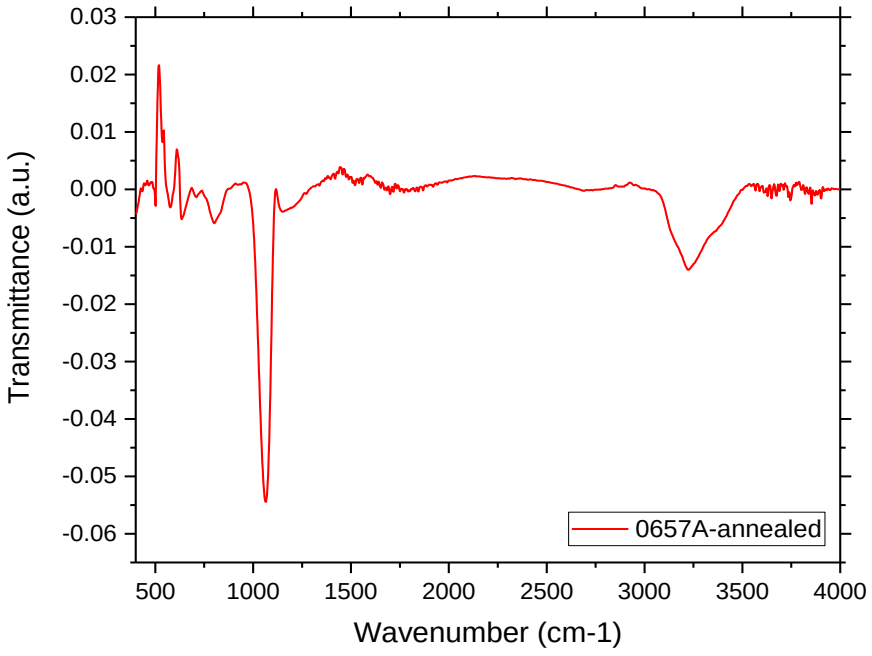
2.5 FTIR spectroscopy of SiO_x deposited over silicon samples

Fourier-transform infrared spectroscopy (FTIR) is a technique used to obtain an infrared spectrum of absorption or emission of a solid, liquid or gas. An FTIR spectrometer simultaneously collects high-spectral-resolution data over a wide spectral range.

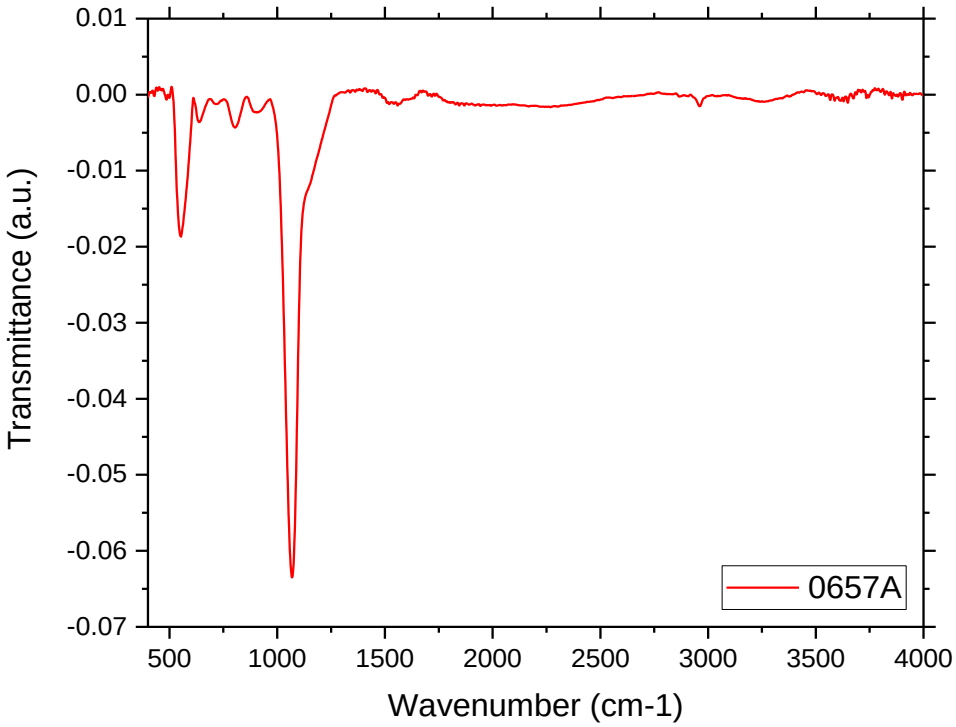
FTIR spectroscopy of PECVD deposited SiO_x over silicon sample is done in the spectral region 4000–400 cm^{-1} (Fig. 2.11) to determine the surface species (especially Si-O bond) for appropriate SiH_4 flow. Film thickness was measured by ellipsometery. Samples are cleaned with organic solvents (for 2 min in each solvent), dried with N_2 blow, and heated at 150 °C for 5 min, prior to FTIR spectroscopy.

In order to neglect the effect of native oxide grown over the samples, they were treated with BOE solution (NH_4F and HF) in order to remove the native oxide. However, treating directly with BOE will etch the PECVD deposited oxide too. So in order to solve this problem, samples were coated with the resin (AZ-1512) using spin coater. Etching was done for 2-3 sec followed by an immediate rinsing with DI water. Finally, the resin was removed by treating the samples with acetone for 30 min and IPA for 5 min followed by rinsing and nitrogen blow.

Bruker OPUS 5 was used for the FTIR spectroscopy. Before measuring the sample, a background check was done using bare silicon sample in order to remove noise in the final measurements. FTIR was performed two time, one before annealing and the other after annealing at 150 °C (Fig. 2.11).



(i)



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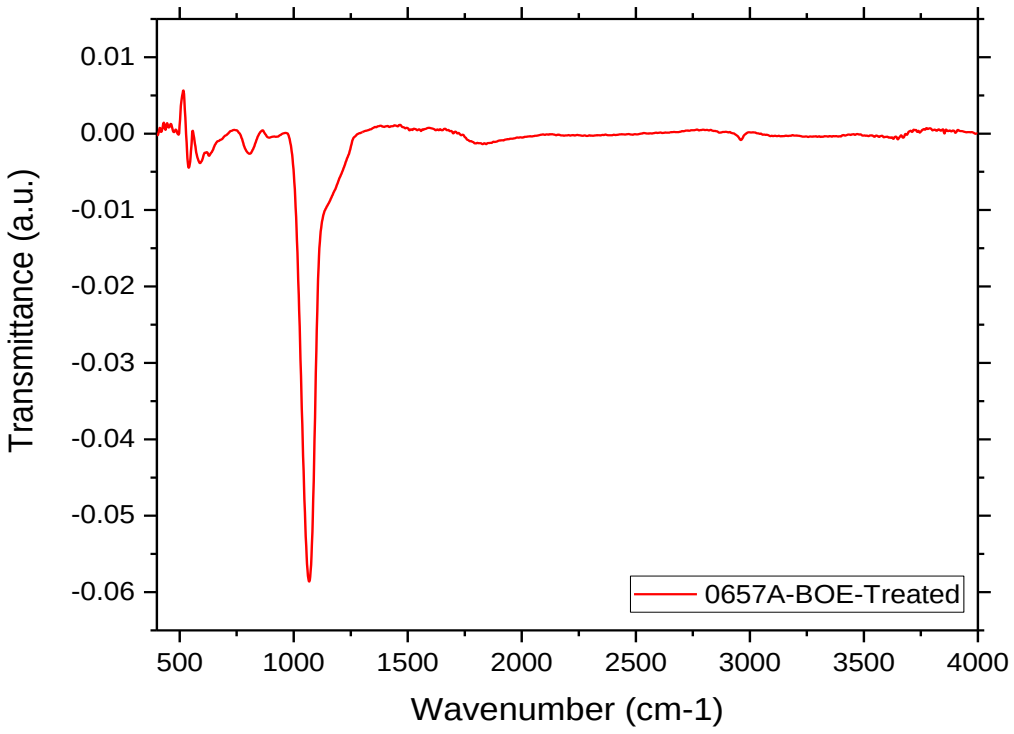

(iii)

Fig. 2.11. FTIR spectroscopy of SiO_x deposited over silicon sample (i) as-deposited, (ii) annealed at 150 °C, and (iii) BOE-treated.

Chapter 3

Results and Discussion

3.1 Results and interpretation

Fig. 2.6 shows the 1 MHz C-V characteristics of the different fabricated MOS capacitors showing high variability of MOS-GaN properties with SiO_x PECVD deposition. It is obvious from this figure that the electrical properties of the MOS devices are drastically affected by the variability of different PECVD deposition parameters (SiH_4, temperature, pressure, and RF power). Accumulation, depletion and deep depletion regimes are well defined, which is a sign of a low D_{it} and a free surface Fermi level (especially for sample E). A similar behaviour was previously reported on GaN [11]- [13]. Compared to the other samples, the sample-E MOS capacitor displays very less stretch-out which shows almost ideal behaviour. The C-V measurements shape was stable and reproducible at all measurement frequencies and extremely low frequency dispersion was observed for this device (Fig. 3.1) especially for the frequency range of 10 KHz – 1 MHz

The fall of the capacitance at 5 MHz is due to the parasitic inductance and series resistance.The measured curve exhibits a small stretch-out and a small flat-band voltage shift (ΔV_{fb}) and a Debye length ($\lambda_n \approx 0.022\ \mu m$). Furthermore, a small hysteresis ($\Delta V \approx 0.1$ V) was observed which is generally attributed to the presence of a low density of slow traps in the SiO_x layer [14]. All these behaviors are signs of good interface properties.

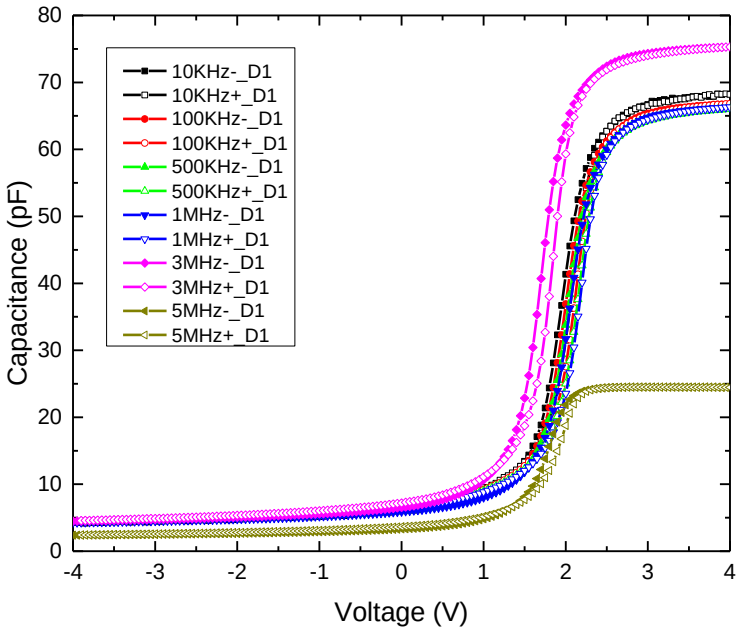

Fig. 3.1. C-V characteristics of Sample-E MOS capacitor for different frequencies.

3.2 Interface state density –Terman's analysis

Interface state density (D_{it}) for sample-E was as low as $\approx 10^{11}$ eV^{-1} cm^{-2} which was estimated from C-V characteristic using Terman's method (Fig. 3.2). The interface state density was extracted from the C-G-w curve (Fig. 3.3) using the following method-

1. For single level: $\frac{G}{w} = \frac{1}{2} C_{it}$; F_{it} : $\frac{G}{w} = \frac{C_{it} w\zeta}{1+(\tau w)^2}$; $Peak\ Position: \zeta w = 1$ (2)

2. Distribution of traps: $\frac{G}{w} = 0.4 \times C_{it}$; F_{it} : $\frac{G}{w} = \frac{C_{it}}{2\zeta w} \ln(1 + (\zeta w)^2)$; (3)

$Peak\ Position: \zeta w = 1.98$ And $q = C_{it} \times D_{it}$;

Where G is conductance; w is the frequency; C_{it} is the capacitance (per unit area); ζ is the response time for the interface states.

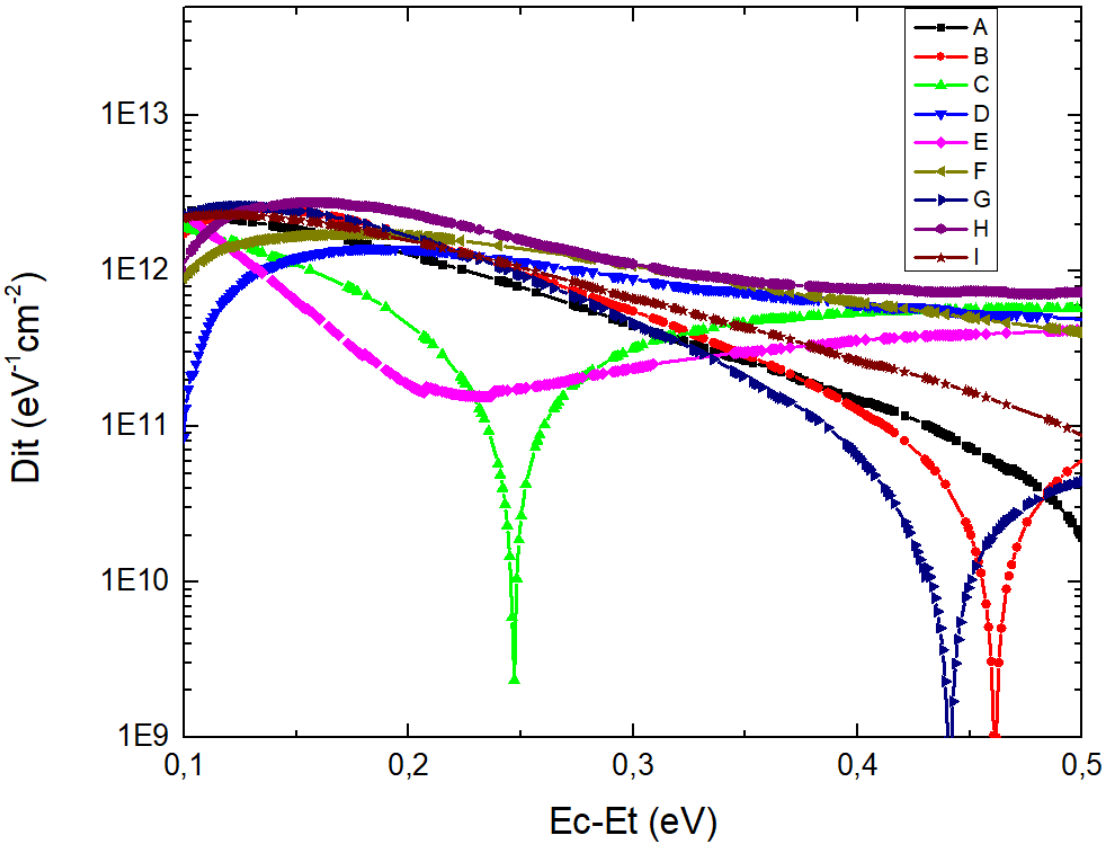

Fig. 3.2. Terman's method for estimation of interface state density.

The curve fitting (Fig. 3.4) was done using eq. (2) and (3) which is compared with the corrected curve (Fig. 3.5) of measured data. The variation of dopant concentration with voltage extracted from high frequency C-V measurements was also analysed using eq. (1). The carrier concentration at the edge of the depletion region was found to be in the order of $\approx 10^{16}$ cm^{-3} in the depletion region as can be seen from (Fig. 2.10). The Debye length was calculated using eq. (4) for each MOS capacitors which is the distance at which charge fluctuations are screened out.

$$\lambda_n = \sqrt{\frac{\epsilon_s KT}{q^2 N_{dl}}} \tag{4}$$

Where λ_n is Debye length; T is room temperature (293.15 K); N_{dl} is the dopant concentration.

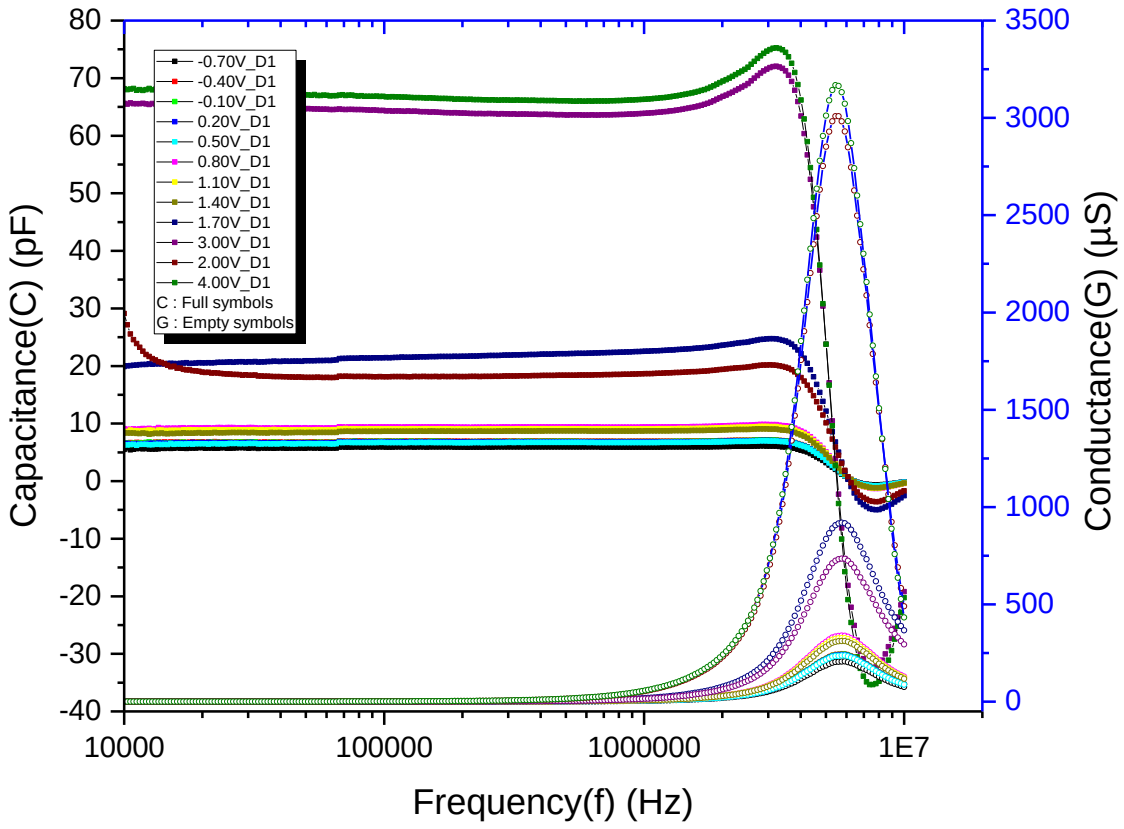

Fig. 3.3. C-w and G-w characteristics for sample-E MOS capacitor at different voltages.

When the C-V characteristics of the MOS capacitors were analysed for different delays (Fig. 2.7), a lateral shift is the curve is found for each delay. Here the delay is time given to reach equilibrium at each voltage change. This can be attributed to the evolution of the capacitance with time. There might be some other unknown reasons, but this is the primary reason causing the shift.

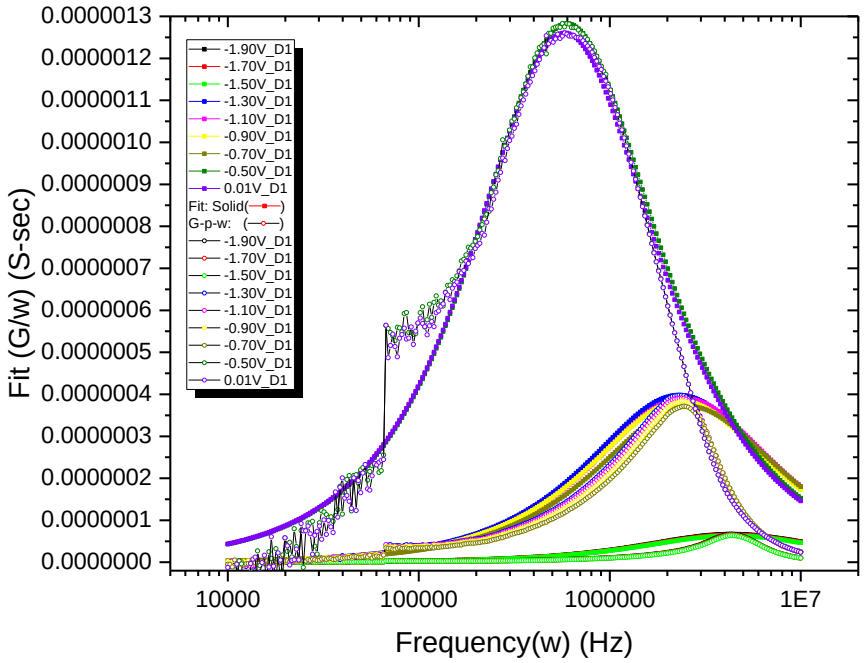

Fig. 3.4. Fitted curve for the analysis of interface trap density.

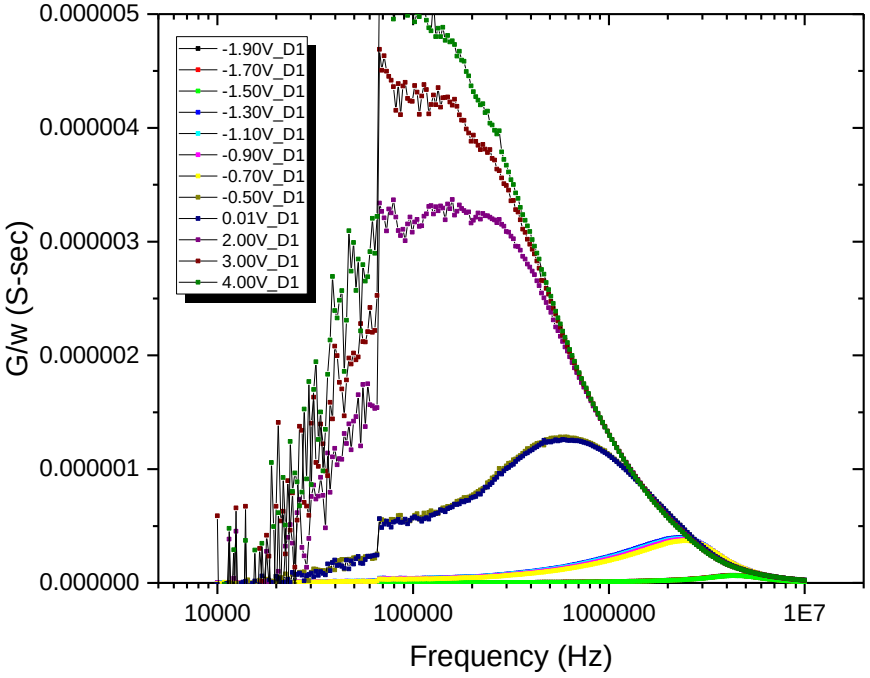

Fig. 3.5. Corrected curve of measured data.

Ideally there should be no shift or a slight lateral shift with increasing delay time. The optimized process based on KOH and HCl pre-treatment prior to PECVD SiO_x deposition and based on various PECVD parameters altered for each sample shows one of the most effective GaN passivation results as it can be seen in Table 3.1.

TABLE 3.1
GaN Passivation results

Samples	Average dopant concentration (cm^{-3})	Debye length (λ_n) (cm)	Flat band voltage shift (Volts) (ΔV_{fb})	Hysteresis (Volts) (ΔV)
A	1.602E+16	2.800E-06	-1.756E+00	0.101
B	2.227E+16	2.375E-06	-9.020E-01	0.088
C	1.441E+16	2.952E-06	-3.666E-01	-0.5851
D	2.450E+16	2.264E-06	1.424E+00	0.0426
E	2.595E+16	2.200E-06	2.111E+00	-0.1052
F	2.168E+16	2.407E-06	5.491E-01	0.1811
G	1.548E+16	2.848E-06	-1.210E+00	0.191
H	2.240E+15	7.487E-06	1.792E+00	0.285
I	1.582E+16	2.817E-06	-1.285E+00	0.147

3.3 Behaviour of electrical properties of device with PECVD parameters

Linear regression is performed for the set of experimental data in order to determine the relation between PECVD parameters (silane flow, pressure, temperature, and RF power) and the electrical properties (D_{it}, V_{fb}, and hysteresis) of the device. Linear regression is a linear approach to modelling the relationship between a scalar response and one or more explanatory variables. Linear regression plot (Fig. 3.6, 3.7 & 3.8), although not representative of the main effects the parameters or their interactions, they show which PECVD deposition parameters have the largest main effect on the property of the device, is plotted between the PECVD parameters used for various samples and the properties of the device (interface state density, flat-band voltage, and hysteresis).

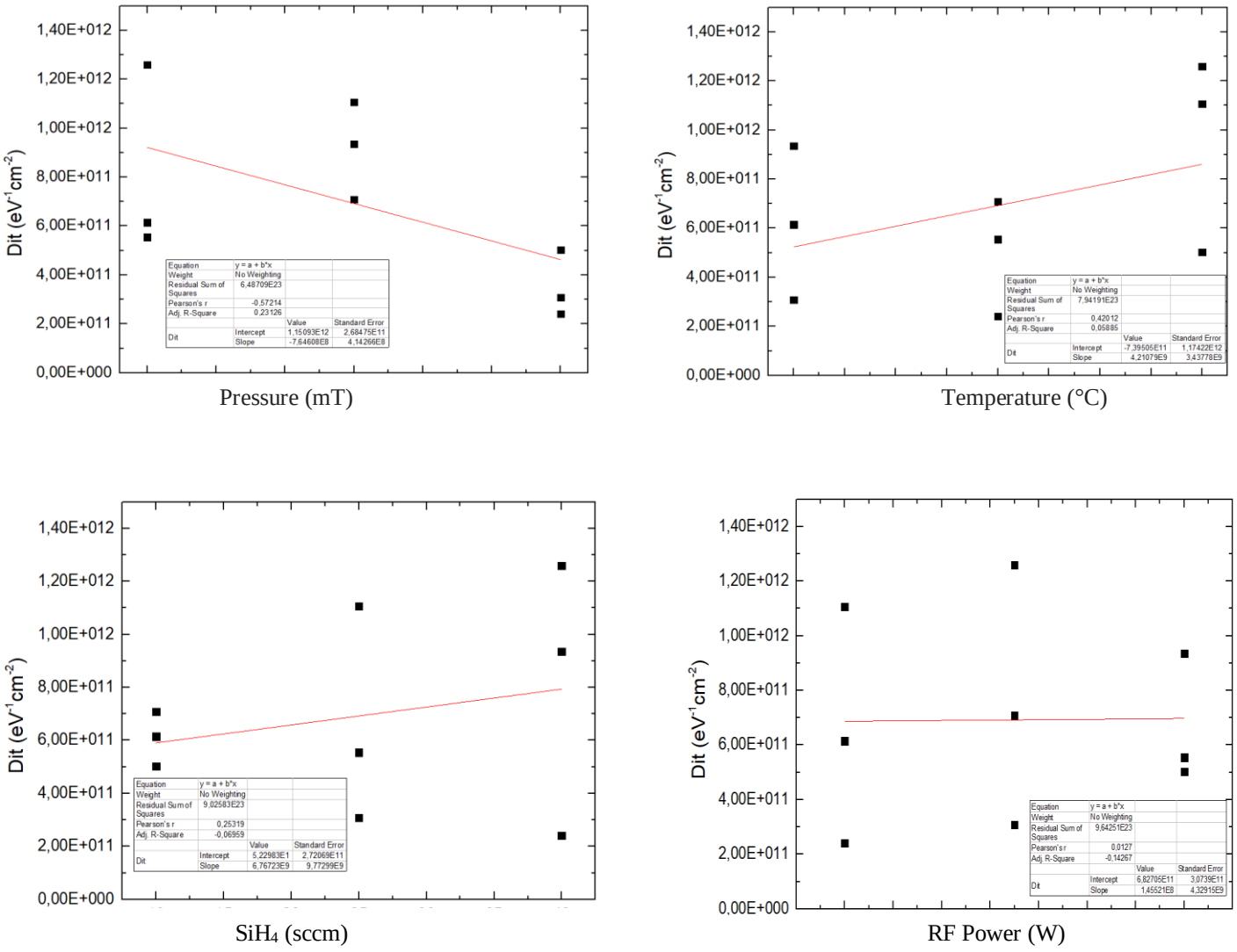

Fig. 3.6. Interface state density versus PECVD deposition parameters.

It is found that varying pressure and temperature has a significant effect on the interface state density (D_{it}) with prior having a greater impact, while silane (SiH_4) flux and RF power has negligible impact as can be seen in the Fig.3.6. When the linear regression plot for flat-band voltage is analysed it came into presence that silane flux and RF power are the most important parameters affecting it while impact of pressure and temperature was found to be negligible as shown in the Fig. 3.7.

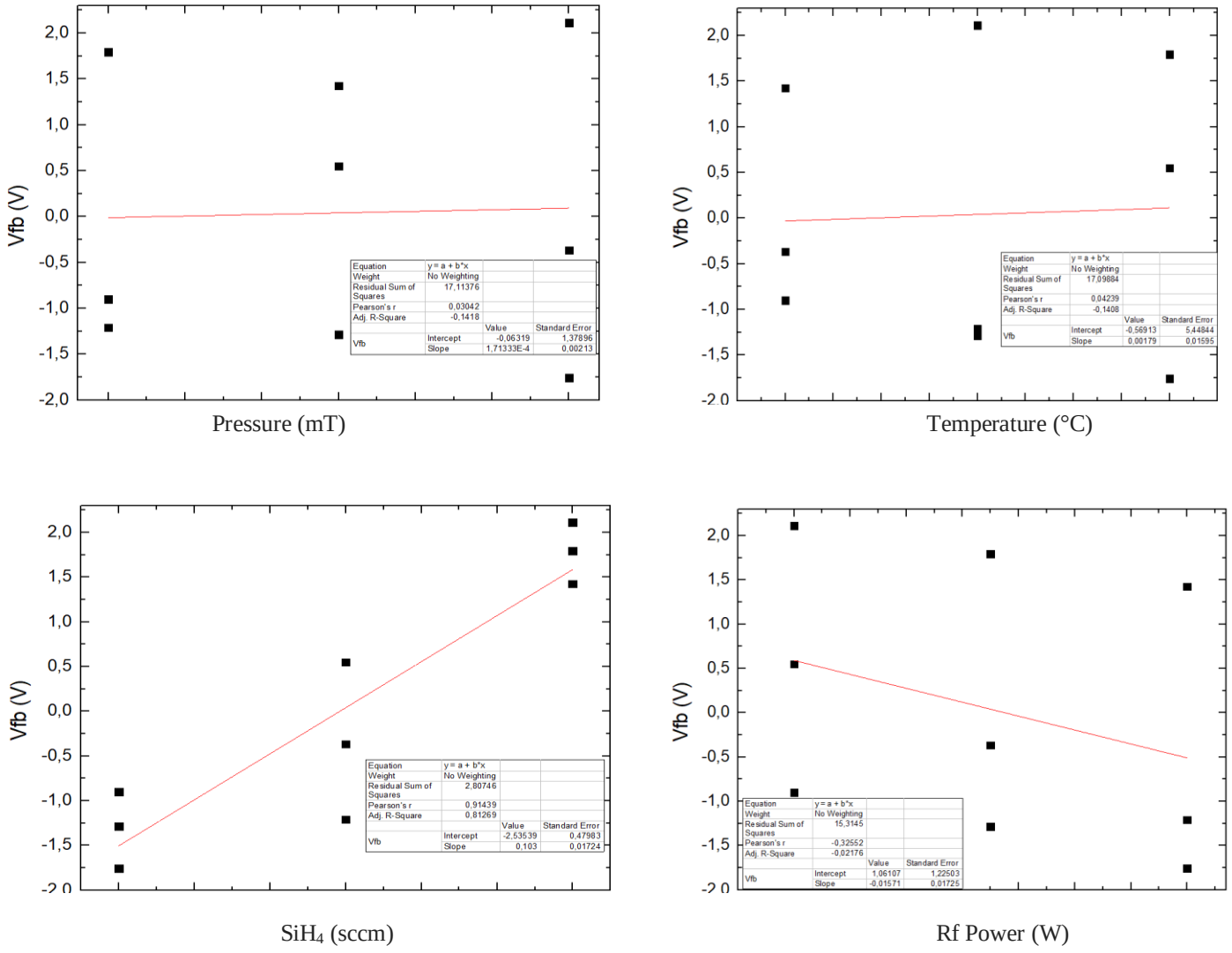

Fig. 3.7. Flat-band voltage versus PECVD deposition parameters.

A similar trend as that of the interface state density was found for the hysteresis loss with pressure and temperature having the largest impact on the properties (Fig. 3.8). Hence, optimization of these parameters which can attribute to the screening process for the best passivated GaN MOS device can be done using the best combination of the above parameters.

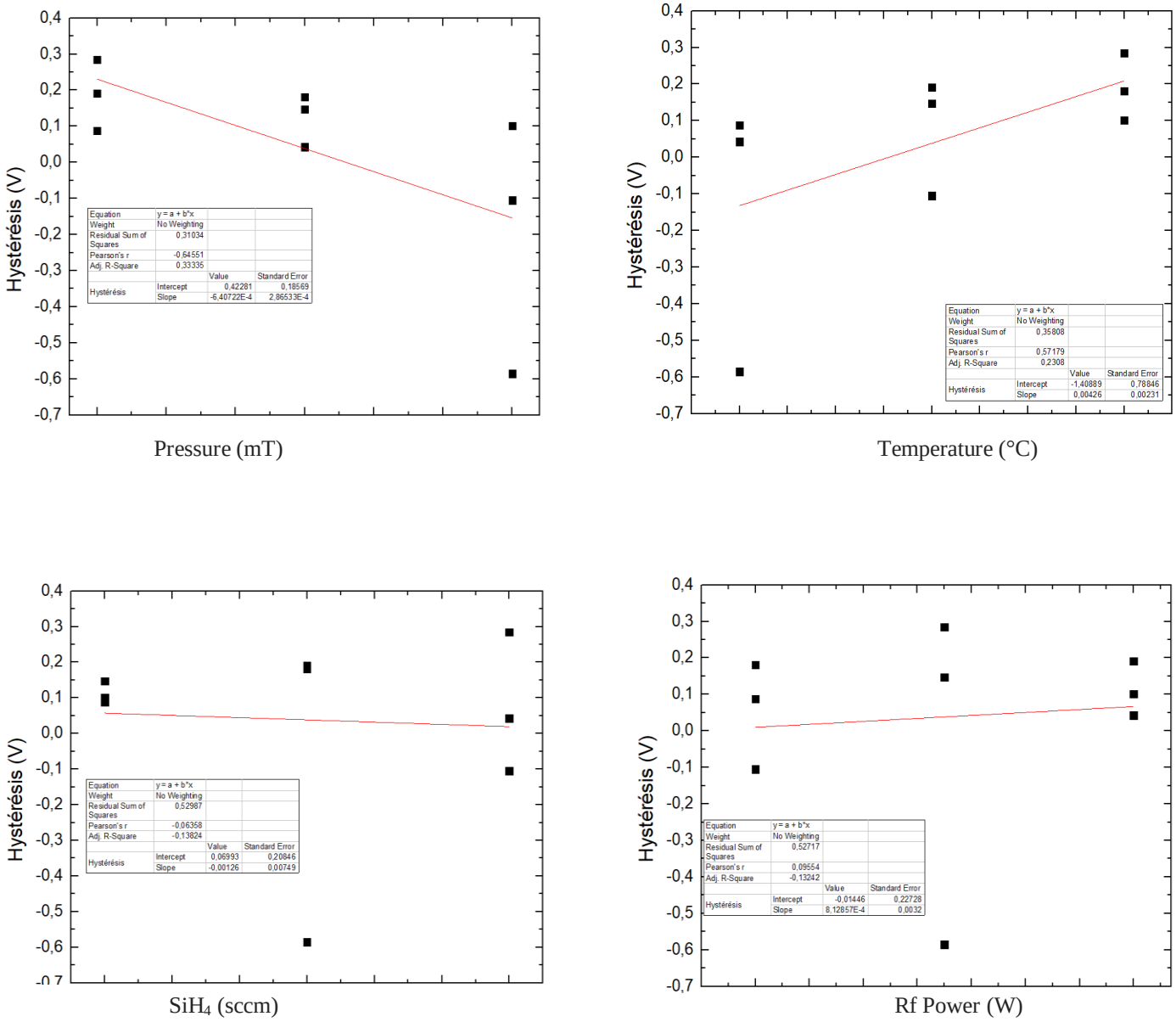

Fig. 3.8. Hysteresis loss versus PECVD deposition parameters.

Overall, it was found that pressure and temperature are the two most important PECVD parameters which affects the interface state density and hysteresis to a large extent. In contrast, flat band voltage is rarely affected by these factors. So, in order to reduce interface state density and improve electrical characteristics of the device, optimization of PECVD parameters in terms of pressure and temperature is important.

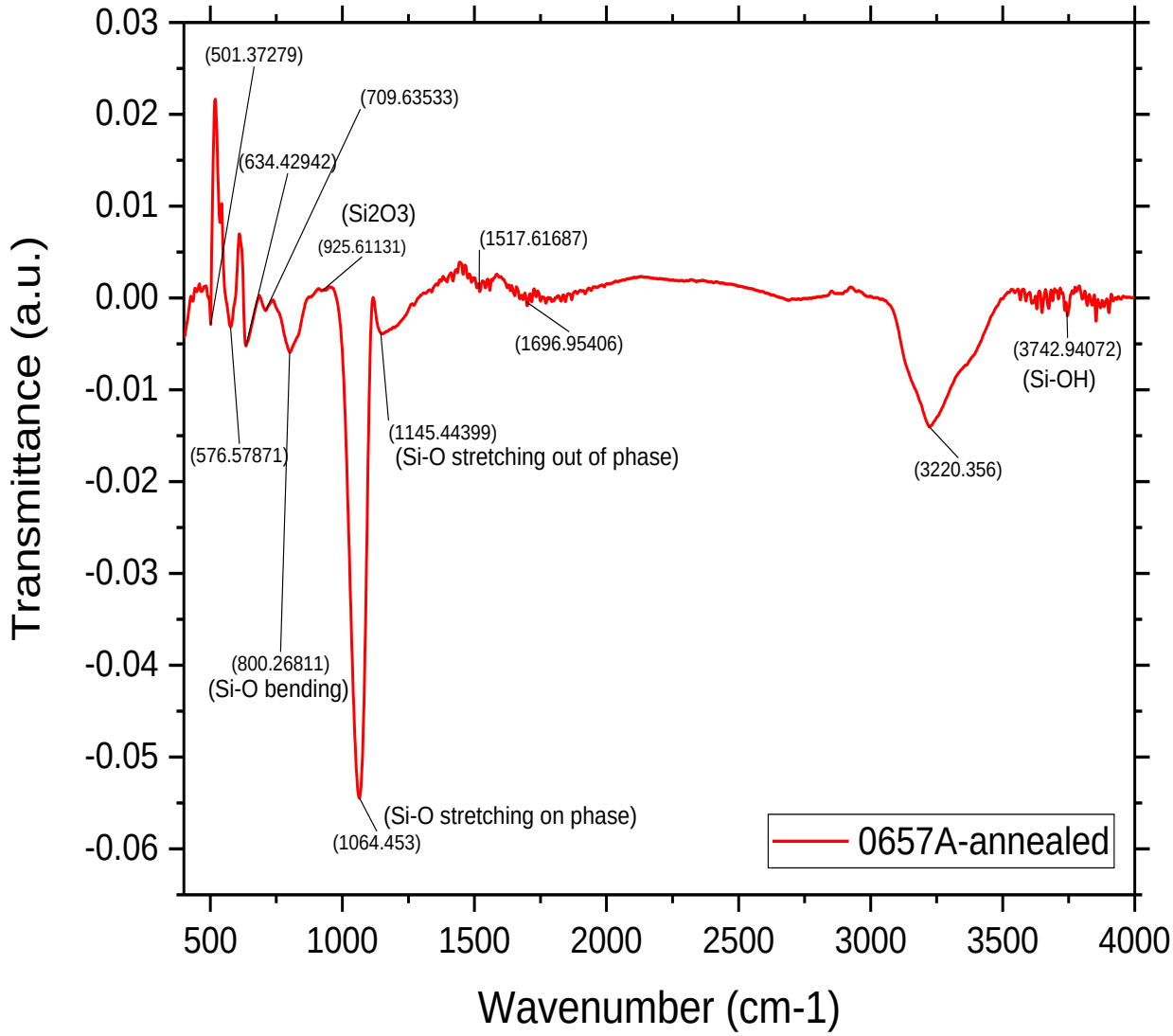

Fig. 3.9. FTIR spectroscopy of annealed sample at 150 °C.

FTIR spectroscopy of PECVD deposited SiO_x over bare silicon tells us about the various bonds present in the bulk of oxide which can be responsible for such electrical characteristics of the device. Si-O bond present at 1064 cm^{-1} spectrum states that the oxide over the silicon is near stoichiometry. Also, presence of Si_2O_3 peaks were found in few samples. The presence of Si-OH peak at higher spectrum region around 3740 cm^{-1} can be due to the presence of silicon-water bonds which can be responsible for the charges at interface and could lead to the electrical properties as obtained.

Chapter 4

Conclusions and Future Work

4.1 Summary of Results

In summary, the basic requirements for power semiconductor device are efficiency, reliability, controllability, and cost effectiveness. Without these attributes, a new device structure would have no chance of economic viability. GaN is a promising material for power devices having high electron mobility, extremely fast switching speed, and excellent reverse-recovery performance, critical for low-loss, high-efficiency operations. An effective GaN surface passivation process was developed by optimizing PECVD parameters for silicon oxide deposition. Al/SiO_x/GaN based MOS structures were fabricated on GaN layers with different PECVD conditions and characterized using C-V, G-w, and I-V measurements. Based on the 1-MHz C-V measurements, the surface state density extracted is in the 10^{11} eV^{-1} cm^{-2} range.

Lastly, an effective device is one with low interface state density, low flat-band voltage shift, and have low hysteresis loss. Surface passivation is one of the most important employed technique. Due to complex phenomenon going on inside PECVD chamber, with no direct relation between PECVD parameters and the property of the deposited film, it was important to optimize these conditions. Furthermore, improvements in other properties such as low leakage current and low series resistance significantly improves the device performance for its application in high voltage and high frequency operations. The obtained results demonstrate the effectiveness of the developed passivation process for high power and high frequency devices.

FTIR spectroscopy gives the valuable information on the bonds present in the bulk of silicon oxide which are essential to determine the electrical characteristics of the device. It was found that two types of Si-O bond was present- Si-O stretching on phase (1064 cm^{-1}) and Si-O stretching out of phase (1145 cm^{-1}) which depicts the presence of near stoichiometric silicon oxide. Moreover, bending of Si-O bond is found at 800 cm^{-1} spectrum. Due to incomplete removal of water over the surface after annealing, Si-OH bonds are detected at around 3700 cm^{-1} spectrum (Fig. 3.9, Chapter 3).

It was n-type GaN samples which displayed good results while p-type samples indicates that another process should be developed, as the surface fermi level was pinned in all cases of p-type samples. Hence, for such passivation method on GaN, n-type is most suitable structure.

4.2 Scope for Future Work

Gallium nitride (GaN) is a material that can be used in the production of semiconductor power devices as well as RF components and light emitting diodes (LEDs). GaN has demonstrated the capability to be the displacement technology for silicon semiconductors in power conversion, RF, and analog applications. GaN devices were designed to replace power MOSFETs in applications where switching speed or power conversion efficiency is critical and are cost efficient as compared to silicon devices. GaN based MOSFET and MESFET transistors also offer advantages including lower loss in high power electronics, especially in automotive and electric car applications [15].

In this research project, electrical characterization was done over capacitor devices. But in order to study the properties in more depth, post-electrical characterization of the fully fabricated transistors should be performed. Moreover, electrical characterization under UV illumination should be performed in order to generated charge carriers in the depletion regime too extract the interface state density more precisely [13]. The research project only focusses on optimization of PECVD parameters and characterization of MOSCAP. Further experiments under UV-illumination is being performed and fabrication of full transistors for the post electrical characteristics is yet to be processed.

Surface passivation of GaN using PECVD deposited SiO_x has shown a tremendous improvement in its electrical properties. However, the optimization of PECVD parameters using screening process has not yet developed. A standard model is required to define the optimum parameters (SiH_4 flow, pressure, temperature) in order to achieve desired electrical and physical properties. Moreover, there is no research over the chemical composition of the oxide and interfaces that are responsible for such electrical characteristics. For instance, investigation of charges present at the interface and in the bulk of oxide should be researched deeply in order to evaluate the origin of such electrical characteristics.

In order to analyze the interface properties and charges present, secondary ion mass spectroscopy (SIMS) analysis along with TEM should be performed. SIMS analysis will determine the presence of species which are responsible for the charge accumulation at the interfaces and ultimately for the electrical properties of the device.

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