Yttria based Memristive System for Neuromorphic Applications

Ph.D. Thesis

By

MANGAL DAS

DISCIPLINE OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

October 2019

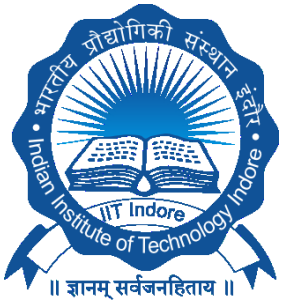
Yttria based Memristive System for Neuromorphic Applications

A THESIS

Submitted in partial fulfillment of the
requirements for the award of the degree
of
DOCTOR OF PHILOSOPHY

by

MANGAL DAS



DISCIPLINE OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE
October 2019

INDIAN INSTITUTE OF TECHNOLOGY INDORE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **Yttria based Memristive System for Neuromorphic Applications,** in the partial fulfillment of the requirements for the award of the degree of **Doctor of Philosophy** and submitted in the **Discipline of Electrical Engineering, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from **May, 2015** to **October, 2019** under the supervisions of **Dr. Shaibal Mukherjee**, Associate Professor, Electrical Engineering, IIT Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Mangal Das 22/10/2019
Signature of the student with date

MANGAL DAS

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

-S. Mukherjee 22/10/2019
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Dr. SHAIBAL MUKHERJEE

MANGAL DAS has successfully given his Ph.D. Oral Examination held on March 16th 2020

Signature of Chairman OEB
Date: 16/3/2020

Signature of External Examiner
Date: 16/3/2020

S. Mukherjee
Signature of Thesis Supervisor
Date: 16/3/2020

Signature of PSPC Member #1
Date: 16/3/2020

Signature of PSPC Member #2
Date: 16/3/2020

Signature of Convener, DPGC
Date: 16-3-2020

16/03/2020
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Date:

ACKNOWLEDGEMENTS

First and foremost, I would like to thank Almighty (ब्रह्म) for giving me the strength, knowledge, ability, and opportunity to undertake this research study and to persevere and complete it satisfactorily. Without his blessings, this achievement would not have been possible.

There are many people who have made significant contributions to this dissertation. It would be impossible to list everyone who contributed or to completely list the extent of the contributions for those who are mentioned.

I would like to express my deep sense of gratitude to my supervisor **Dr. Shaibal Mukherjee** for his outstanding mentorship and support that they provided over the past five years. He was always accessible and have been a constant source of advice to keep my project headed toward its main goal. Dr. Mukherjee played an influential role in developing my research skills and personality. I benefited immensely from his vast technical expertise and insight; he could not even realize how much I have learned from him.

I am incredibly grateful to my doctoral committee members **Dr. Apurba K. Das** and **Dr. Amod C. Umarikar,** for giving me valuable advice on my research and kindly going through my dissertation. I am thankful to **Dr. Mukul Gupta** and **Dr. Varimalla Raghavendra Reddy** of the University Grants Commission, Department of Atomic Energy Consortium for Scientific Research, Indore for their help in recording XRD and GIXRD data. Furthermore, I would like to acknowledge the support from **Dr. Myo Than Htay** and **Mr. Tomohiko Yamakami** of the Technical Division, Faculty of Engineering, Shinshu University for TEM imaging.

I would like to thank **Dr. Pradeep Mathur**, Director, IIT Indore for providing the essential experimental facilities and financial support in attending international conferences. I want to acknowledge the support provided by sophisticated instrumentation center (SIC) at IIT Indore, for performing SEM, EDX and XRD measurements. I would like to thank my fellow group members including **Dr. Vishnu Awasthi, Dr. Pankaj Sharma, Aaryashree, Vivek Garg, Brajendra Singh Sengar, Amitesh Kumar, Md Arif Khan,**

Ritesh Bhardwaj, Rohit Singh, Biswajit Mandal, Gaurav Siddharth, Pawan Kumar, Sanjay Kumar, Ruchi Singh, and others for their valuable support and co-operation during this research work.

I would like to thank, Ministry of Electronics and Information Technology (MeitY), Government of India, for providing fellowship under Visvesvaraya Ph.D. Scheme for Electronics and Information Technology. Thiswork was supported by the research and development work undertaken in the project under the Visvesvaraya Ph.D. Scheme of Ministry of Electronics and Information Technology (MeitY), Government of India, being implemented by Digital India Corporation (formerly Media Lab Asia). My sincere gratitude to department of science and technology-science and engineering research board (DST-SERB) and MeitY for providing me international travel grant to attend the conferences.

Last, but far from least, I must thank my parents, brother, and my wife, who have supported me in all of my academic accomplishments. I owe a lot to them.

Mangal Das

Dedicated to them who helped me

LIST OF PUBLICATIONS

A: Publications from Ph.D. thesis work

A1. In refereed journals

1. **Mangal Das,** Amitesh Kumar, Rohit Singh, Myo Than Htay, and Shaibal Mukherjee*, "Realization of synaptic learning and memory functions in Y_2O_3 based memristive device fabricated by dual ion beam sputtering",* **Nanotechnology,** vol. 29, no. 5, 2018. (**Impact Factor: 3.404**)
2. **Mangal Das,** Amitesh Kumar, Biswajit Mandal, Myo Than Htay, and Shaibal Mukherjee**,** *"Impact of Schottky junctions in the transformation of switching modes in amorphous Y_2O_3-based memristive system",* **Journal of Physics D: Applied Physics,** vol. 51, no. 31, 2018. (**Impact Factor: 2.373**)
3. **Mangal Das,** Amitesh Kumar, Sanjay Kumar, Biswajit Mandal, Md. Arif Khan, and Shaibal Mukherjee**,** *"Effect of Surface Variations on the Performance of yttria Based Memristive System,"* **IEEE Electron Device Letters,** vol. 39, no. 12, 2018. (**Impact Factor: 3.443**)
4. **Mangal Das,** Amitesh Kumar, Sanjay Kumar, Biswajit Mandal, Gaurav Siddharth, Pawan Kumar, Myo Than Htay and Shaibal Mukherjee, **"***Impact of Interfacial SiO_2 on Dual Ion Beam Sputtered Y_2O_3-based Memristive System*," **IEEE Transactions on Nanotechnology.** (**In Communication**)

A2. In refereed conferences

1. **Mangal Das**, Sanjay Kumar, Amitesh Kumar, Biswajit Mandal, and Shaibal Mukherjee*, "Effect of roughness on the resistive switching of yttrium oxide based system,"* **10th International Conference on Materials for Advanced Technologies (ICMAT)**, Singapore, June 23-28, 2019.
2. **Mangal Das**, Sanjay Kumar, Md. Arif Khan, Biswajit Mandal, Myo Than Htay, and Shaibal Mukherjee, *"Effect of roughness on the resistive switching of yttrium oxide based system,"* **7th International Symposium on Organic and Inorganic Electronic Material and Related Nanotechnologies (EM-NANO)**, Nagano, Japan, June 19-22, 2019.

3. **Mangal Das,** Amitesh Kumar, Sanjay Kumar, Biswajit Mandal, Pawan Kumar, and Shaibal Mukherjee, *"Impact of Schottky Junction on the Resistive Switching of Yttrium Oxide,"* **9th International Conference on Key Engineering Materials (ICKEM 2019)**, Oxford, United Kingdom, 2019.
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6. **Mangal Das**, Amitesh Kumar, Sanjay Kumar, Biswajit Mandal, Myo Than Htay and Shaibal Mukherjee, "*Effect of Schottky interfaces in yttria based memristive devices*", **International Conference on Computational Mathematics in Nanoelectronics and Astrophysics (CMNA 2018),** IIT Indore, India during November 1-3, 2018.
7. **Mangal Das**, Amitesh Kumar, Biswajit Mandal, Brajendra Sengar and Shaibal Mukherjee, *"Synaptic learning and memory functions in amorphous Yttria-based memristive systems,"* **MRS Spring Meeting**, **Arizona**, USA, 2018.
8. **Mangal Das**, Amitesh Kumar, Biswajit Mandal, and Shaibal Mukherjee, *"Influence of crystallinity on memristance in n-Si/Y_2O_3/Al structure"*, **19th IWPSD**, **IIT Delhi**, India, 2017.
9. **Mangal Das**, Amitesh Kumar, Biswajit Mandal, and Dr. Shaibal Mukherjee, *"Influence of Deposition Temperature on Memristance in n-Si/Y2O3/Al Structure"*, **6th ISIF**, **Delhi**, India, 2017.

A3. Book chapters

Nil

B: Other publications during PhD

B1. In refereed journals

1. Amitesh Kumar**, Mangal Das,** Vivek Garg, Brajendra S. Sengar, Myo Than Htay, Shailendra Kumar, Abhinav Kranti, and Shaibal Mukherjee*, "Forming-free high-endurance Al/ZnO/Al memristor fabricated by dual ion beam sputtering,"* **Applied Physics Letters ,** vol.110, no. 25, 2017. **(Impact Factor: 3.495)**
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4. Biswajit Mandal, Aaryashree, **Mangal Das,** Myo Than Htay, and Shaibal Mukherjee**,** *"Architecture tailoring of MoO_3 nanostructures for superior ethanol sensing performance,"* **Materials Research Bulletin,** vol. 109, 2018. **(Impact factor 2.873)**
5. Arif Khan, Pawan Kumar, **Mangal Das**, Myo Than Htay, and Shaibal Mukherjee, "*Drain Current Optimization in DIBS-grown MgZnO/CdZnO HFET*," IEEE Transactions on Electron Devices. **(In communication)**
6. Arif Khan, Pawan Kumar, Gaurav siddharth, **Mangal Das**, and Shaibal Mukherjee, "*Analysis of Drain Current in Polycrystalline MgZnO/ZnO and MgZnO/CdZnO HFET*", **IEEE Transactions on Electron Devices**, vol. 66, no. 12, 2019.
7. Sanjay Kumar, Rajan Agrawal, Mangal Das, Pawan Kumar, Shaibal Mukherjee, "*Analytical Modeling of Y_2O_3-based Memristive System for*

Synaptic Applications", Journal of Physics D: Applied Physics. **(In communication)**

B2. In refereed conferences

1. Md Arif Khan, Pawan Kumar, **Mangal Das,** Gaurav Siddharth, and Shaibal Mukherjee, *"Analytical model for DC characterizations of ZnO based HFET utilizing interface states density modulation,"* **10th International Conference on Materials for Advanced Technologies (ICMAT),** Singapore, June 23-28, 2019.
2. Sanjay Kumar, **Mangal Das,** Amitesh Kumar, Myo Than Htay, and Shaibal Mukherjee, *"Yttrium oxide based resistive switching device for synaptic applications,"* **6th Nano Today Conference,** Lisbon, Portugal, June 17-20, 2019.
3. Amitesh Kumar, **Mangal Das**, Md Arif Khan, Aaryashree, Vivek Garg, Abhinav Kranti and Shaibal Mukherjee, "*Dual ion beam sputtered low-power and high-endurance resistive switching memory device with memristive behavior*," **34th International Conference on the Physics of Semiconductors (ICPS 2018)**, Montpellier, France, July 29-Aug 03, 2018.
4. Amitesh Kumar, **Mangal Das**, Biswajit Mandal, Ritesh Bhardwaj, Aaryashree, Abhinav Kranti, and Shaibal Mukherjee, "*Nano-scaled ZnO based resistive memory device fabricated by dual ion beam sputtering*," **18th IEEE International Conference on Nanotechnology (IEEE NANO 2018)**, Cork, Ireland, July 23-26 2018.
5. Amitesh Kumar, **Mangal Das**, Aaryashree, Md Arif Khan, Ritesh Bhardwaj, Abhinav Kranti, and Shaibal Mukherjee, "*Interface-engineered forming-free dual ion beam sputtered ZnO based memristive device*," **20th International Conference on Superlattices, Nanostructures and Nanodevices (ICSNN2018)**, Madrid, Spain, July 23-26, 2018.
6. Amitesh Kumar, **Mangal Das,** Brajendra S. Sengar, Biswajit Mandal, Rohit Singh, Abhinav Kranti and Shaibal Mukherjee**, "**Novel forming-free resistive memory based on dual ion beam sputtering engineered oxygen vacancies/interstitial defects in ZnO," **Materials Research Society (MRS) Spring Meeting, Phoenix,** Arizona, USA, April 2-6, 2018.

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8. Biswajit Mandal, Aaryashree, **Mangal Das** and Shaibal Mukherjee, "*Synthesis of micrograss like a-MoO_3 and their enhance ethanol sensing performance*", (**ISIF, 2017**), New Delhi, India, December 10-13, 2017.
9. Aaryashree, Biswajit Mandal, Rohit K Jadhav, **Mangal Das**, Apurba K Das and Shaibal Mukherjee, *"Study of ZnO-Oligophenylenevinylene nano-hybrid for Optoelectronic Applications*", (**ISIF,2017**), New Delhi, India, December 10-13, 2017.
10. Biswajit Mandal, Aaryashree, **Mangal Das** and Shaibal Mukherjee, "*Synthesis of high crystalline nanobelt like α-MoO3 and their alcohol sensing performance*", (**19th IWPSD**), **IIT Delhi**, India, December 11-15, 2017.

B3. Book chapters

1. Amitesh Kumar, **Mangal Das**, and Shaibal Mukherjee, *"Oxide based memristors: fabrication, mechanism, and application,"* Invited by Prof. Saleem Hashmi (editor-in-chief), **Reference Module in Materials Science and Materials Engineering, Elsevier**, August 2018.
2. Amitesh Kumar, **Mangal Das**, and Shaibal Mukherjee, *"Film Deposition Processes Based on Eco-Friendly, Flexible, and Transparent Materials for High-Performance Resistive Switching,"* **Reference Module in Materials Science and Materials Engineering, Elsevier**, September 2018.

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ACRONYMS

C-AFM	*Conductive-Atomic Force Microscopy*
DIBS	*Dual Ion Beam Sputtering*
FESEM	*Field Emission Scanning Electron Microscopy*
HRS	*High Resistance State*
HRTEM	*High Resolution Transmission Electron Microscopy*
I-V	*Current-Voltage*
LRS	*Low Resistance State*
LTP	*Long-Term Plasticity*
MIM	*Metal-Insulator-Metal*
MIS	*Metal-Insulator-Semiconductor*
RRAM	*Resistive Random Access Memory*
RS	*Resistive Switching*
SBD	*Schottky Barrier Diode*
STDP	*Spike-Timing-Dependent Plasticity*
STP	*Short-Term Plasticity*
XRD	*X-Ray Diffractometer*
Y_2O_3	*Yttrium Oxide*

NOMENCLATURE

φ_m	Magnetic flux linkage
q	Electric charge
V_r	Reverse bias voltage
N_D	Electron density near Fermi level
ϵ	Dielectric constant
d_{th}	Thickness of Schottky barrier
A^*	Richardson constant
α	Ideality factor
k_B	Boltzmann constant
τ	Relaxation time

ABSTRACT

Yttria based Memristive System for Neuromorphic Applications

by

Mangal Das

Hybrid Nanodevice Research Group, Discipline of Electrical Engineering

Indian Institute of Technology Indore

Supervisor: Dr. Shaibal Mukherjee

Memristor, the so-called fourth fundamental circuit element, has drawn extensive attention in recent years for its enormous potential as the next-generation non-volatile memory (NVM). Resistive random-access memory (RRAM), being one of the major applications of memristor, is a promising candidate to replace conventional charge-based flash memory in future data storage applications. The primary advantages of RRAMs over conventional memories are their simple structure, fast switching mechanism, low-power consumption, and high stacking density. Yttria (Y_2O_3) has been studied as a replacement of SiO_2 for gate oxide material in thin-film transistor-based memory devices. Yttria offers an attractive substitute of SiO_2 as gate oxide for thin-film transistor-based memory applications due to excellent physical properties such as low lattice mismatch with Si substrate, high dielectric constant (~10-18) for gate oxide. However, minimal literature is present on yttria-based RRAM. The fabrication of yttria-based RRAM by dual ion beam sputtering (DIBS) system has not been reported to date. DIBS system is noteworthy since it produces high-quality thin films with reasonably good compositional stoichiometry, small surface roughness, and excellent adhesion to the substrate even for films grown even at room temperature.

In this research work, firstly, the optimization of deposition conditions of yttria switching layer is performed in order to find out the favorable

conditions for resistive switching (RS) behavior. This is important as DIBS system has many parameters that can be changed during deposition, such as temperature, oxygen partial pressure, and ion beam voltage, etc. These parameters affect the properties of deposited thin films such as crystallinity, resistance, and interface, etc. The deposition temperature is optimized in the first step of this study. In this stage, DIBS deposition temperature during the growth of yttria on Si is optimized. During this stage, Substrate temperature of the device is varied from 100 to 500 °C (100 (N1), 200 (N2), 300 (N3), 400 (N4), to 500 °C (N5)) while all other DIBS deposition parameters are kept constant. The XRD patterns of yttria thin films show that the crystallinity of yttria films (N1→N5) is observed to change from highly textured (N1, N2) to amorphous (N3, N4) and then to polycrystalline (N5) as the deposition temperature increases. The current-voltage measurement of these devices indicated that amorphous yttria layer shows RS characteristics, while a highly crystalline yttria layer is not very useful for RS application. SiO_2 layer, present at yttria and Si interfaces, influences the grain surface area at the top surface of the yttria layer. As the thickness of SiO_2 layer increases along with deposition temperatures, the grain surface area variations in yttria film also increases. As the level of surface area variation and thickness for the SiO_2 layer decreases, the endurance of the device improves. Moreover, the devices with amorphous oxide layer show the smaller distribution in set-reset voltage than devices with polycrystalline oxide. The quantitative analysis of current-voltage characteristics shows that variation in the switching voltage (set/reset or both) correlates with grin surface area of grains present in the Y_2O_3 films. Such direct observation of the correlation is shown in this first time. The endurance measurements carried out for least variable amorphous RS device show high repeatability for ~23000 switching cycles.

After the optimization of deposition temperature, the correct Ar:O_2 flow rate needed to be explored, which can further enhance the RS behavior in DIBS grown yttria based devices. The effect of oxygen partial pressure variation has been studied with respect to the RS behavior. The ratio of Ar to O_2 partial pressure has been varied for devices N50 (5:0), N41 (4:1), N32

(3:2) at this stage. It is observed that N50 and N41 do not show any RS whereas N32 shows RS for a small number of cycles (~4) initially, and subsequently the RS behavior has disappeared. It is found that the device (N3), which has a deposition temperature of 300°C and a mixture of Ar: O_2 with a ratio of 2:3, shows the best RS characteristics.

After the optimization of yttrium oxide layer for the RS behavior, the effect of schottky interface on the RS behavior of yttria has been investigated via changing bottom electrodes (BE) in Al/Y_2O_3/BE-type device structure. In this stage of our study, three devices N3, P3, and A3 are used to further understand the effect of the interface on the behavior of yttria-based RRAM. Devices P3 (Al/Y_2O_3/*p*-Si) and A3 (Al/Y_2O_3/Al) are fabricated under the same condition (deposition temperature = 300°C and Ar:O_2 = 2:3) as in case of N3 but with different BE. N3, P3, and A3 have *n*-Si, *p*-Si and Al as their bottom electrode, respectively. It is important to note that N3 has one Schottky interface between Al and Y_2O_3, while A3 has two Schottky interfaces between Al and Y_2O_3. Also, the transformation from unipolar (Al/Y_2O_3/*n*-Si) to bipolar (Al/Y_2O_3/Al) switching modes has taken place after moving to a system of single SBD (Al/Y_2O_3/*n*-Si) to double SBD (Al/Y_2O_3/Al). This transformation confirms the predominant role of Schottky interface between Al and Y_2O_3 in our fabricated Al/Y_2O_3/BE type structures.

In the last chapter of this thesis, the neuromorphic behavior of optimized Al/Y_2O_3/*n*-Si device is discussed. Synaptic functions such as nonlinear transmission characteristics, long-term plasticity, short-term plasticity and "learning behavior" are achieved using a single synaptic device based on cost-effective metal-insulator-semiconductor (MIS) structure. A "learning behavior" function is demonstrated for yttria based memristive device, which bears resemblance to certain memory functions of biological systems. The realization of essential synaptic functions in a cost-effective MIS structure would promote much cheaper synapse for artificial neural networks.

Chapter 1

Introduction

The current technological era is full of products like smartphones, gaming consoles, tablets, and several other devices; this is made possible because of advancements in semiconductor technology. The ever-increasing demand for processing speed and high-density memory present a tough challenge to engineers and scientist who remain in a constant search for newer technologies to meet this demand. Although, very high-density integrated chips are available today due to miniaturization of the components which are present in a semiconductor memory. Yet, the new consumer electronic market is keen for more and more densification to satisfy the needs of emerging technologies. Semiconductor memories are an essential part of current electronics systems that uses computer processing technology. To meet the growing needs for denser and faster semiconductor memory, the existing types and technologies are being further developed.

Semiconductor memories, such as static random access memory (SRAM), dynamic random access memory (DRAM), flash memory, and hard disk, etc., are designed according to the needs of different applications. To elucidate, flash memory cards, and hard drives are non-volatile and cost-effective memory devices, but they are slow, whereas SRAM and DRAM are faster but volatile and expensive. Therefore, it is required to subside the insufficiencies and failures of these memory devices and find out a universal solution such as resistive random access memory (RRAM) [1].

In recent years, scientists are looking to imitate the computational power of the human brain, along with advancements in modern computer architecture. Nowadays, the term neuromorphic has been used to describe any analog, digital, mixed-mode system, and software systems that try to mimic the behavior of neural networks for different applications. The hardware-level implementation of neuromorphic computing may be realized by RRAMs, spintronic memories, and threshold switches.

This chapter provides a description of the basic understandings of non-volatile memory, *i.e.,* resistive random access memory (RRAM) or Memristor [2]. The basic properties, operating principle, performance parameters, and advantages of RRAM are also being discussed in this chapter.

1.1 Background

In 1971, "Memristor," the so-called fourth fundamental circuit constituent, was proposed by Dr. Leon Chua [3] in addition to the resistor, capacitor, and inductor. However, Considering symmetry, it was anticipated the memristor to be a passive two-terminal component that can relate magnetic flux (φ) to charge (q) as shown in figure 1.1. For the interaction of charge and flux, the memristor will be behaving as the non-linear circuit component possessing memory characteristics. Richard Stanley Williams, who is a research scientist at HP Labs, claimed to have synthesized a memristor-based on his analysis of a thin film of TiO_2 [4]. After this, Leon Chua further expanded the concept of memristor to RRAMs [1], [2]. Memristor is a nanoscale device that requires comparatively very less physical space to build data storing memory cells and hence is capable of increasing the storage capacity of current memory technologies. It is a great asset in the continuous trend of densification of semiconductor memories in this technological era, because of its prospective high-density, low-power consumption, low-cost-per-bit, and fast-switching characteristics.

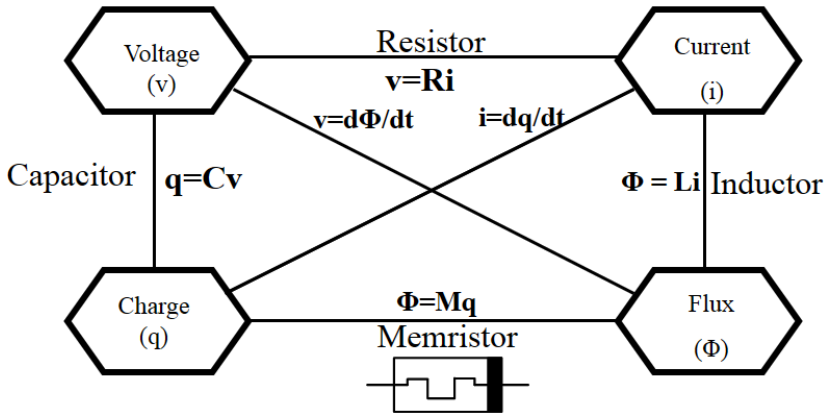

Figure 1.1: Memristor, a missing link in electrical circuit theory.

1.2 Resistive Random Access Memory (RRAM)

New non-volatile memories like phase-change random access memory (PCRAM) [5], magnetic random access memory (MRAM) [6], ferroelectric random access memory (FRAM) [7], and resistive random access memory (RRAM) [2] have been explored to meet vibrant and massive data storage requirements. Nevertheless, evolving technologies like MRAM and FRAM also face severe technical hitches while scaling. RRAM, grounded on resistance alteration modulated by electrical incitement, has of late fascinated technical and commercial interests. The underlying principle of RRAM is the state change phenomenon in memory device due to resistance change, which is termed as "Resistive Switching" (RS). Memristor is a specific case of RRAM, as depicted in figure 1.2, where a device exhibits specifically defined characteristics.

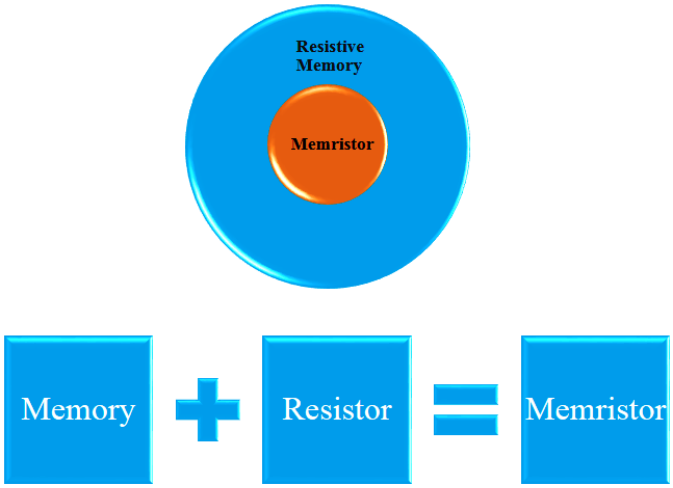

Figure 1.2: Resistive memory and memristor.

RRAM has been drawing considerable attention in contemporary years as a strong candidate for non-volatile memory (NVM) due to its small and straightforward structure, low-power depletion, fast operation, and resilient potential for formulating multilevel per-cell memories [8].

1.2.1 Memristor as RRAM

The memristance was initially hypothesized by Chua in 1976 [9] as a non-linear functional relationship between magnetic flux linkage $\varphi_m(t)$ and electric charge, $q(t)$ [3].

$$f\big(\varphi_m(t), q(t)\big) = 0 \qquad (1)$$

The magnetic flux linkage ($\varphi_m(t)$) is generalized from of the circuit characteristic of an inductor. Memristance is mathematically defined as the charge-dependent rate of change of flux with charge.

$$M(q) = \frac{d\varphi_m}{dq} \tag{2}$$

The flux can be substituted as the time integral of the voltage, and charge as the time integral of current, which leads us to equation 3;

$$M(q(t)) = \frac{d\varphi_m(t)}{dq(t)} = \frac{V(t)}{I(t)} \tag{3}$$

A memristor has a mathematically scalar state, whereas a memristive system has a vector state and a number of state variables. These state variables are independent of the number of terminals of a memristive system. Mouttet [10] attempted to extend the theory of memristive systems by including higher-order derivatives of the input signal u(t):

$$\begin{aligned} y(t) = \; & g_0(x,u)\, u(t) + g_1(x,u)\, \frac{d^2u}{dt^2} + g_2(x,u)\, \frac{d^4u}{dt^4} \\ & + \cdots \ldots \ldots \ldots . + g_m(x,u)\, \frac{d^mu}{dt^m} \end{aligned} \tag{4}$$

Where m belongs to the set of positive integers, u(t) and y (t) are an input and output signal, respectively.

$$\dot{x} = f(x,u) \tag{5}$$

Here, vector x represents a set of n state variables that describe the system.

Some researchers have further improved HP's memristor models to explain the behavior of RRAM [11].

$$y(t) = \; g_0(x,u)\, (u(t) - a) \tag{6}$$

$$\dot{x} = f(x,u) \tag{7}$$

A memristor is a specific case of resistive switching (RS), which shows a pinched-hysteresis test (figure. 1.3). A memristor can be defined as a two-terminal device, which has the capability of resistive switching (RS) behavior between two or more resistance states when an external excitation is applied to its terminal. Resistance in the low-resistance state (LRS) and

in the high-resistance state (HRS) is represented as R_{on} or R_{LRS} and as R_{off} or R_{HRS}, respectively, as illustrated in figure 1.3.

1.3 Memristive Finger Prints

Memristor is a state-dependent system that shows zero-crossing with pinched hysteresis loop [12]. The area of this pinched hysteresis loop decreases with the increase in the operating frequency. Figure 1.3 shows the fingerprints of a memristive system. Since the device possesses certain inertia so it cannot respond to fast variation in excitation waveform. Therefore, it settles to some equilibrium state, with decreased hysteresis loop area for higher sweep/ramp rates [12]. It explains pinched current-voltage (I-V) hysteresis, loop, as illustrated in figure 1.3, which is witnessed to be dependent on the bias sweep rate.

The "SET process" (V_{SET}) is defined when the device switch from a high resistance state (HRS) to a low resistance state (LRS) [13]. On the other hand, when the device turns back from LRS to HRS, it is considered as "RESET process" (V_{RESET}) [13].

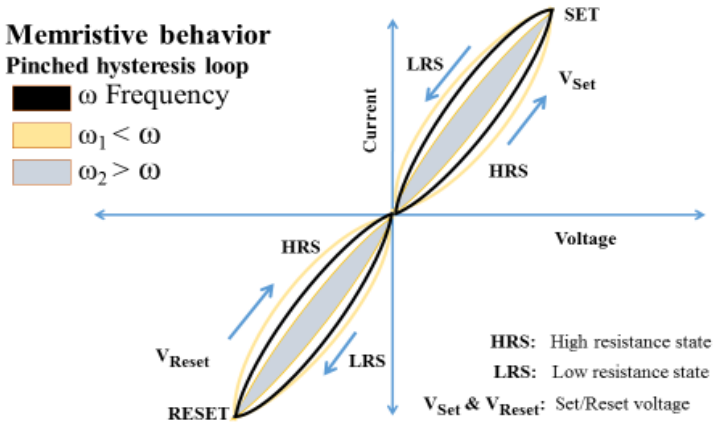

Figure 1.3: Resistive switching with memristive behavior exhibiting pinched-hysteresis.

1.4 Electroforming

Electroforming is defined as a process in which a dielectric is made electronically conductive upon application of a relatively high electric field [14]. It is commonly accepted that electroforming involves a defect-induced soft dielectric breakdown, which may include the processes of electrochemical reduction, heating, and field-driven bond rupturing [15].

Electroforming allows the formation of a conductive channel through the switching layer [16].

A strong electric field, which is applied across the switching material, initiates the electroforming by rupturing chemical bonds in the dielectric. This allows the formation of a conductive channel for the flow of vacancies towards cathode according to the thermochemical dielectric breakdown theory [15]. The polarity of the applied electric field sets the orientation of the conductive channel. Hence before initiating the RS in the device, an electrical-forming procedure is done to stimulate the pristine memory device to the high conductive state. Nonetheless, in this thesis work, we have aimed to fabricate forming-free resistive switching (RS) devices.

1.5 Modes of Resistive Switching

Resistive switching (RS) is directed by the underlying principle of non-volatile and reversible change of resistance upon the influence of electrical stimulus. The mode of RS devices can be classified as bipolar or unipolar**.** Bipolar switching (figure. 1.4) requires opposite voltage polarities for the SET and RESET processes, whereas nonpolar and unipolar switching has no such requirements [17]. Unipolar devices (figure. 1.4) are also termed as nonpolar when devices can be operated with both voltage polarities [17].

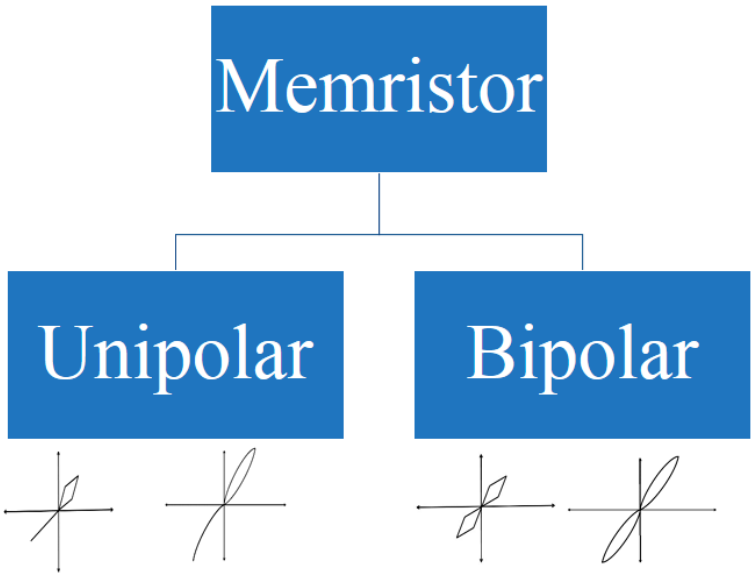

Figure 1.4: Modes of switching polarities.

1.6 RS Performance Parameters

1.6.1 Resistance Ratio

Resistance ratio is a measure of the range of a device to differentiate between two distinct states, i.e., HRS and LRS [18]. It is the ratio of HRS and LRS. A high resistance ratio is desirable to define the switching capability of an RS device as well as for multi-bit or multi-level storage where intermediate values of resistance can also be utilized.

1.6.2 Retention

Retention is the ability of a memory cell to retain a state over time [19]. A constant voltage pulse is applied, and the current is measured uninterruptedly for a specific time (thousand seconds or more) period after setting the system at either LRS or HRS [20]. The corresponding resistance state would indicate whether the memory cell has degraded or not with time.

1.6.3 Endurance

Endurance can be considered as the number of SET/RESET cycles that can be sustained by the device before the HRS and the LRS are no longer distinct [19]. To verify the stability and reproducibility of the RS, the voltage pulses have to be applied repetitively on the memory cell. Resistive memory requires high endurance (long-age) for practical applications as each cycle of transition from one state to another can accelerate the aging process of a device [21].

1.7 RS for Neuromorphic Applications

1.7.1 Synaptic Plasticity

Plasticity is the capability of the brain cells to change and familiarize themselves with a piece of new information. Synaptic plasticity represents the change that occurs at synapses when two neurons try to communicate with each other. The idea of synapses plasticity was first proposed by psychologist Donald Hebb [22].

The efficacy of neural communication is dependent on synaptic plasticity. The strength of this communication is affected by the volume of chat between neurons. Figure 1.5 shows the critical components of a neural

network, which involves neurons and synapse etc. The changes in synaptic strength, which occurs during neural communication, are referred to as synaptic plasticity. There are two types of synaptic plasticity:

1. Short-term plasticity

2. Long-term plasticity

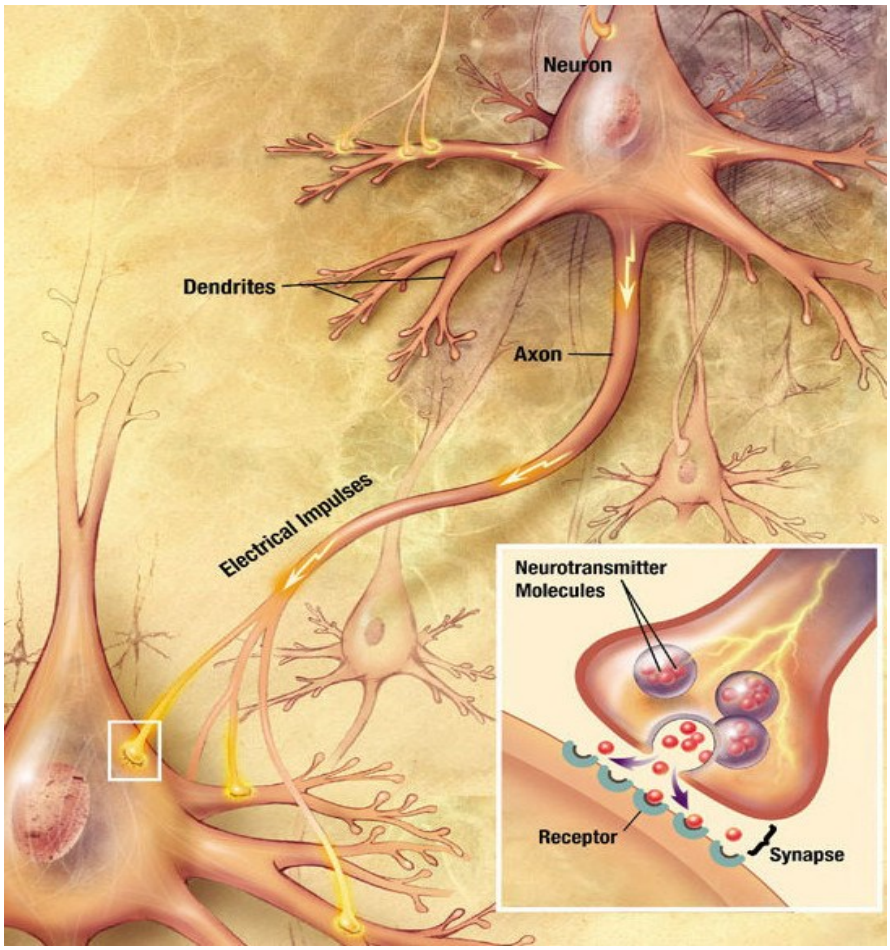

Figure 1.5: Key components in neural conversation. Credit: http://www.nia.nih.gov/alzheimers/publication/alzheimers-disease-unraveling-mystery/preface.

1.7.2 Short-Term Plasticity (STP)

It refers to rapid changes (increase and decrease) in synaptic strength that takes place on a sub-second timescale. It helps to determine how vital that neural connection is for the current conversation. The effect of these changes starts fading away as soon as the conversation ends.

1.7.3 Long-Term Plasticity (LTP)

Long-term synaptic plasticity persists anywhere from minutes to hours, days, or maybe years. It is considered to be the dominant model of brain storage. It defines how humans create and remember new memories.

1.8 Yttrium Oxide as Switching Material

RS devices based upon various oxides, including TiO_2 [4], CuO [23], NiO [24], TaO_x [25], and others containing regulated oxygen vacancies have been widely investigated in recent years. However, the exploration of yttria (Y_2O_3)-based RRAMs [26], [27] is an under-investigated area . Y_2O_3 has been studied thoroughly [1] as a gate oxide material as it is considered as a replacement of SiO_2 in thin-film transistor-based memory devices. SiO_2 thin films are highly unreliable because of the high density of pinholes [1] and larger tunneling currents [1], which results in reduced yields and low breakdown strength. High-dielectric constant (k) dielectric insulators such as yttria offer an attractive substitute of SiO_2 for ultra-large-scale integrated (ULSI) applications. Yttria exhibit excellent physical properties such as low lattice mismatch ($\boldsymbol{a_{Y_2O_3}}$ = 1.060 nm, $2\boldsymbol{a_{Si}}$ = 1.086 nm) with Si substrate [1], large band gap (~5.1 eV) [1], high dielectric constant (~10−18) [1] for thin film applications. However, the presence of unintended SiO_2 [28]–[31] layer found between Si substrates and Y_2O_3 is a major challenge in this direction.

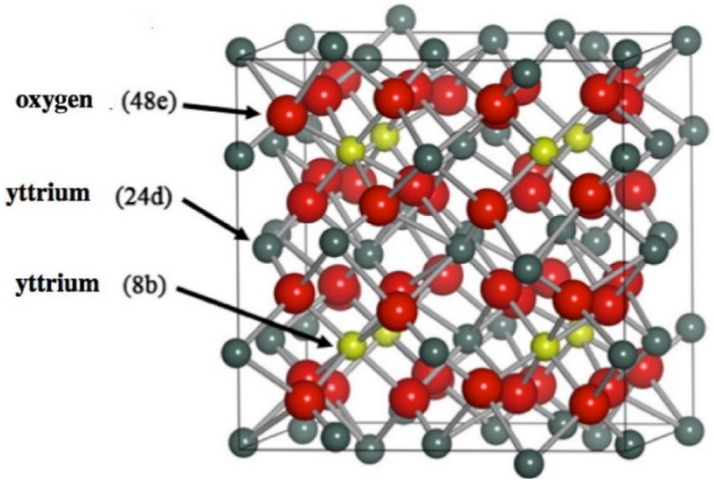

Figure 1.6: Structure of the cubic yttria. The lattice parameter is a_0 = 1.0604 nm [32].

1.9 Aim and Objective

The forming-free RS behavior is rare among general memristive devices. The device to device variation in parameters such as SET-voltage (V_{SET}), RESET-voltage (V_{REST}), and resistance ratio is a matter of concern for RRAMs. To the best of our knowledge, the fabrication of yttria based RRAM by dual ion beam sputtering (DIBS) system has not been studied to date. The main aim of this thesis is to realize Y_2O_3 based RS device for non-volatile memory applications using sputtering techniques and the study of neuromorphic behavior in the RS device. This task includes the following objectives:

(a) Exploration of the previous studies of different yttria based RS devices and understanding various design aspects of RS device, which corresponds to performance parameters.

(b) Fabrication of yttria based RS device with the help of DIBS as this sputtering method is a low-cost deposition technique, and it can be used for large-area fabrication.

(c) Study of the effect of deposition parameters (deposition temperature and oxygen partial pressure) on the RS of the device.

(d) Study of the Schottky interface on the conduction mechanism of yttria based RS device.

(e) Study of neuromorphic behavior of our RS devices.

1.10 Organization of the Thesis

The research in this thesis is focused on the realization of forming free high endurance yttria based RS devices using the DIBS system. The thesis is arranged as follows:

***Chapter* 2** illustrates the various instruments and tools which are used for the fabrication, characterization of RS device.

Chapter 3 discusses the design aspects of the experiment and fabrication conditions of our RS devices, which are used in this study.

Chapter 4 details the effect of deposition parameters on the electrical behavior of an RS device by utilizing various external electrical excitations. It also illustrates other characterization details concerning various aspects of RS device.

Chapter 5 illustrates the effect of the Schottky interface on the underlying conduction mechanism of our devices.

Chapter 6 describes the neuromorphic application of our RS device.

Chapter 7 presents the conclusion of the thesis and presents the challenges and future aspects in the field of RRAM.

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Chapter 2

Systems for Fabrication and Characterization of Yttrium Oxide-based Memristive System

In this chapter, the DIBS system (used for the deposition of thin films) and characterization techniques, which are used to investigate the yttria based memristive system, have been described in detail. Different characterization techniques are used to evaluate the structural, elemental, morphological, and electrical properties of the yttria switching layer. The crystal structure of the samples is characterized using X-Ray diffraction (XRD) system. The electrical properties of these devices are characterized by the current-voltage (I-V) measurement system (Keithley 4200A-SCS Parameter Analyzer). The quality of the material interface between the yttrium oxide and electrodes has been investigated by high-resolution transmission electron microscopy (HRTEM) measurement. The quality of the top surface of the yttrium oxide film is investigated by field emission scanning electron microscope (FESEM) images. These systems are discussed in detail in this chapter.

2.1 Growth Equipment

In this research work, the growth of Y_2O_3, Al, or *n*-Si thin films, and the fabrication of the yttria-based memristive system is performed by the Elettrorava-DIBS system. The DIBS system is explained in detail in the following section.

2.1.1 Dual Ion Beam Sputtering System

DIBS System is one of the most important physical vapor deposition (PVD) techniques for thin-film depositions under ultrahigh vacuum conditions [1]. DIBS system is equipped with a *radio-frequency* (RF) deposition ion beam source and a *direct-coupled* (DC) assist ion source, as shown in figure 2.1. The RF ion source is deployed to sputter materials from a target, which is fixed in a four target assembly. The assist ion source cleans the surface of the substrate prior to film deposition. It also hinders the island formation and removes the weak dangling bonds during thin film growth [2]. The

angle between the axis of the deposition ion source and the sputtering target is fixed at approximately 45° off normal. The angle between the assist ion source and the substrate is maintained at approximately 60°. DIBS system offers the following advantage with respect to other sputtering systems:

1. DIBS system produces high-quality thin films with reasonably better compositional stoichiometry, low surface roughness, and provides excellent adhesion even at room temperature [3].

The schematic of a deposition chamber of the DIBS system is shown in figure 2.1, while figure 2.2 shows the original assembly. The main components of this system include RF (deposition) ion source, assist ion source, a deposition chamber, load lock chamber, two vacuum turbopumps, different types of vacuum gauges, a substrate heater assembly, a water chiller and a controlling unit [2].

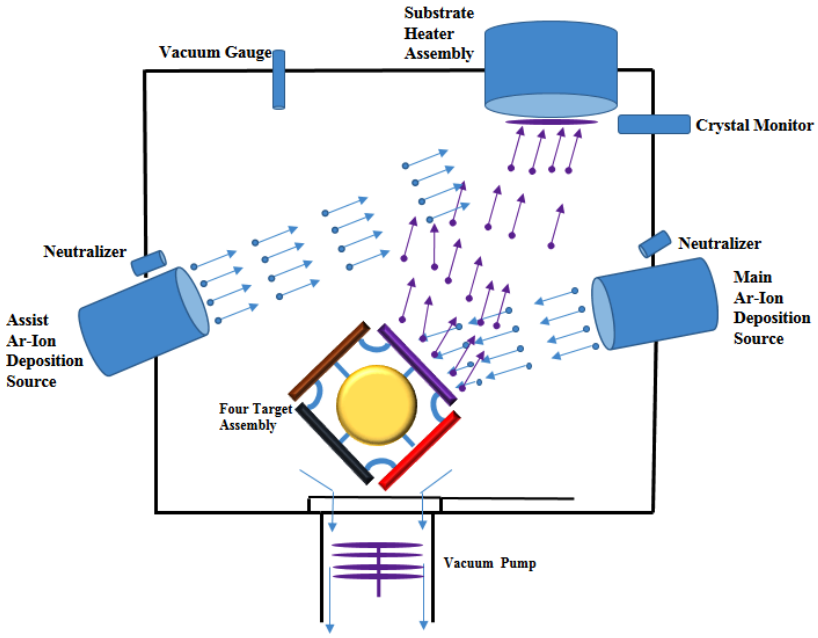

Figure 2.1: Schematic of the dual ion beam sputtering (DIBS) system.

In the DIBS system, both ion sources (made by Kaufman & Robinson) produce a cation ion beam, which is spatially well confined and mono-energetic [4]. Principally, RF ion source creates a plasma (mainly Ar gas), which consists of the ions accelerated with the help of grids. The deposition ion source consists of three key parts: the discharge chamber, grids, and neutralizer. Ions are produced inside the discharge chamber when a gas (generally Ar) is subjected to an RF field. This process starts when gas is sent into small isolated quartz or alumina chamber, which is surrounded by

an RF powered coil. The RF field excites outermost electrons of gas atoms until they gain enough energy to break away from gas atoms, which results in the plasma of cations and electrons; this process is referred to as "inductive coupling."

Figure 2.2: The photographic image of the DIBS system. Credit: Sophisticated instrumentation centre (SIC), IIT Indore. Manufactured and customized by ELETTRORAVA S.P.A.

These ions are then extracted in the form of a beam from the discharge chamber by subjecting the grids to various voltage biases. The deposition source usually consists of three-grids to extract ions.

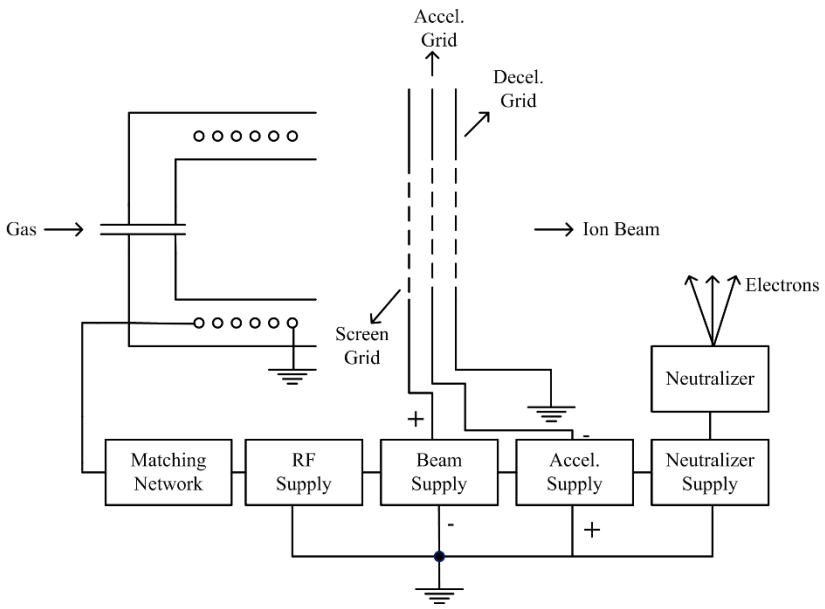

Figure 2.3: Block diagram of the ICP40 RF ion deposition source.

This arrangement reduces the chances of beam spread. The neutralizer (hollow cathode) is an electron source, which is used to neutralize the

positive ion beam after it has been extracted [4]. The schematic of the deposition ion source is given in figure 2.3. The assist ion source consists of an End-Hall 400 ion source module and a neutralizer. This system consists of three types of power supplies:

1. Keeper power supply
2. Emission power supply
3. Discharge power supply.

Keeper and emission power supplies are used for neutralizer. The discharge power supply is used to provide voltage and current to End-Hall 400 ion source module, which produces a positive ion beam. This type of low cost assist ion source assembly has some advantages such as broad ion-beam coverage, much larger ion-current capabilities, and excellent reliability. The larger ion-current capabilities of this ion source permits sufficient etch rates [2] even at low ion energies (less than or equal to 200 eV). Figure 2.4 shows the schematic diagram of the assist ion source assembly. The keeper power supply provides voltage and current to the hollow cathode neutralizer. This allows the thermionic emission of electrons [2] from the keeper plate by igniting and keeping the keeper plate hot. The emission power supply starts after the keeper power supply ignited the hollow cathode and then the emission power supply provides a negative voltage to the hollow cathode, which controls the electron beam. This electron beam neutralizes the beam of positive ions, which are emitted from the End-Hall 400 ion source. The deposition chamber of DIBS, in which growth processes are performed, is mostly made up of stainless steel as it is non-corrodible, non-magnetic, easy to weld and clean, highly malleable, and has excellent outgassing characteristics [2]. The chamber consists of a large number of ports for different functions and small viewing windows (Pyrex glass). The load lock chamber is a small chamber that allows the loading of the substrate into the deposition chamber without breaking the vacuum of the deposition chamber. This task is performed by a robotic arm that moves between the load lock chamber and the deposition chamber. A set of rotary and turbomolecular vacuum pumps are used for creating an ultra-high vacuum (inside the deposition chamber and load lock chamber) which is measured by different vacuum gauges. The substrate heater assembly

inside the main chamber is used to heat the substrate from room temperature up to 1000 °C.

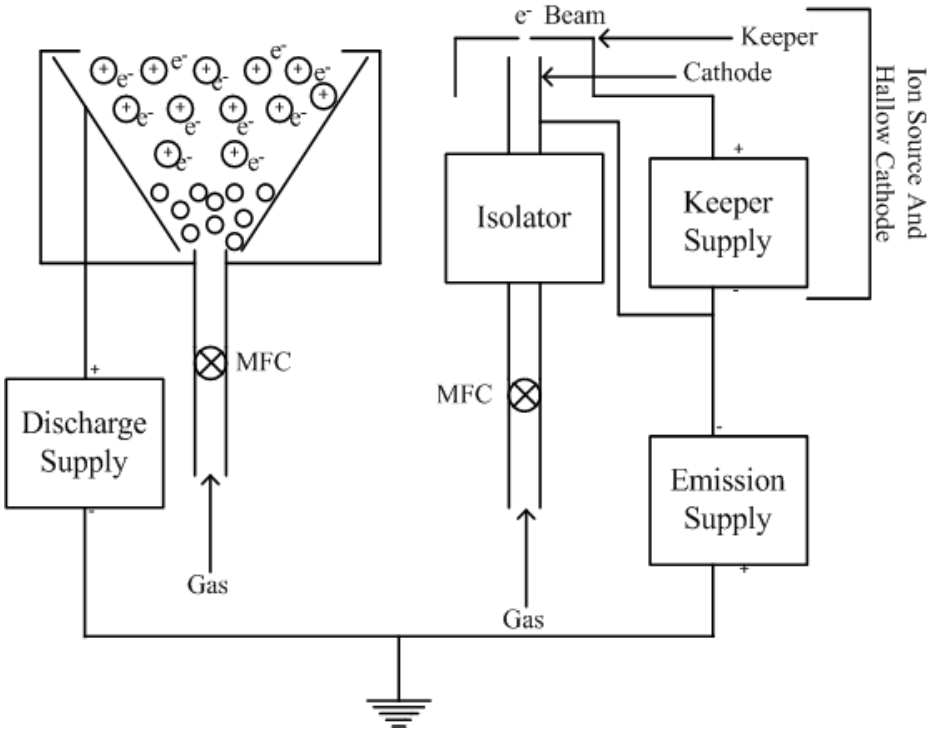

Figure 2.4: Block diagram of the EH400 assist ion source.

This heater assembly allows growth and in-situ annealing processes at elevated temperatures. The water chiller cools the pumps and reduces the temperature inside the deposition chamber and target assembly. DIBS system growth parameters such as deposition temperature, gas partial pressure, and RF power are controlled by a controlling unit [1], [2].

2.2 Characterization Techniques

The types of equipment, which are used for the characterization of thin films in this research work, is discussed in the following sections.

2.2.1 Current-Voltage (I-V) Measurement System

The Keithley 4200A-SCS Parameter Analyzer is a vital characterization tool to measure the current-voltage parameters. It is used to evaluate parameters like electrode area dependence of current, endurance, retention, and resistance ratio. For endurance and retention measurement, it is used in pulse mode. Figure. 2.5 shows the photographic images of the *I-V* measurement setup. The setup includes Everbeing cryogenic probe station

with the temperature range of 80 K to 350 K and a semiconductor parameter analyzer (4200A SCS).

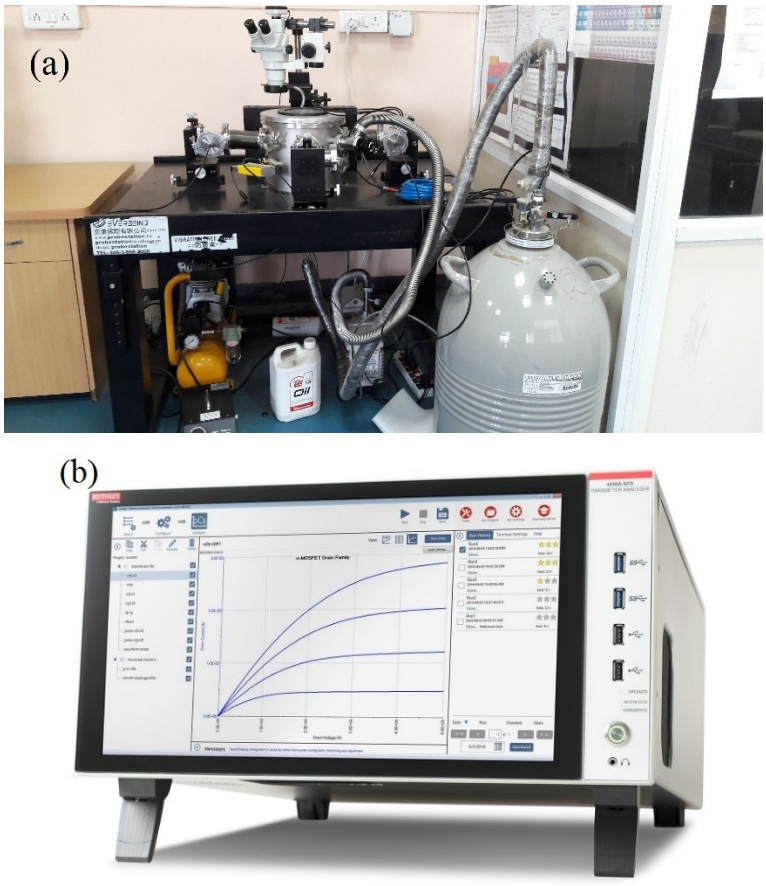

Figure 2.5: Photographs (a) probe station and (b) Keithley 4200A-SCS semiconductor parameter analyzer. Credit: Hybrid Nanodevice Research Group (HNRG) Lab, IIT indore.

Our setups are capable of measuring the thin-film samples of different sizes and shapes, but in our case, we have used mainly the samples of the area not more than 3.14 mm^2. The limitation of our setup is that we can only measure the I-V in the temperature range of 77 K to 450 K. The details of used current-voltage (I-V) protocols are given in the later chapters of this thesis.

2.2.2 X-Ray Diffraction Measurement

X-ray diffraction (XRD) is one of widely used technique which is quite useful in examining the crystallinity, phase, and analyze the stress and strain in any given sample [5]. The Concept of XRD is based on Bragg's

law and uses a collimated beam of X-Rays which incidents on a sample and diffracted by the crystalline phases in the sample:

$$n\lambda = 2d\ sin\theta \tag{2.1}$$

Where λ is the wavelength of the incident X-ray beam, d is the inter-plane separation of lattice between atomic planes in the crystalline phase, θ is the angle between atomic planes and the incident X-rays and n is an integer that represents the interference order.

The concept of Bragg diffraction works in electron diffraction processes because X-ray wavelengths are comparable with inter-atomic distances. These small wavelengths allow X-rays to be an excellent tool for measuring inter-atomic distances. The intensity of the X-rays, which are diffracted from lattice planes, is measured in terms of the diffraction angle 2θ. This diffraction pattern is unique for lattice planes; thus, it can be used to identify the sample crystal structure [5]. The XRD patterns show peak position with respect to 2θ and intensity of the diffracted beam, which provides the information about the crystal orientation and quantitative approximation of crystallinity.

In this research work, the crystal structure of Y_2O_3 thin films is characterized using Rigaku SmartLab; Automated Multipurpose X-ray diffractometer equipped with a copper target (Cu-Kα) to generate the incident X-rays of wavelength λ = 0.154178 nm for the diffraction measurement in Bragg Brentano configuration. The obtained experimental diffraction patterns of yttria are matched with powder diffraction file (PDF) Card No.: 00-025-1200 (cubic 'c') in order to identify phase information. The actual image of this XRD system is shown in figure 2.6.

The samples, which are used in this study for XRD measurement, are mainly square samples of size less than 2 cm^2.

Figure 2.6: Photographic image of Rigaku SmartLab, Automated Multipurpose X-ray diffractometer. Credit: Sophisticated instrumentation centre (SIC), IIT Indore.

2.2.3 Grazing Incidence X-ray Diffraction (GIXRD)

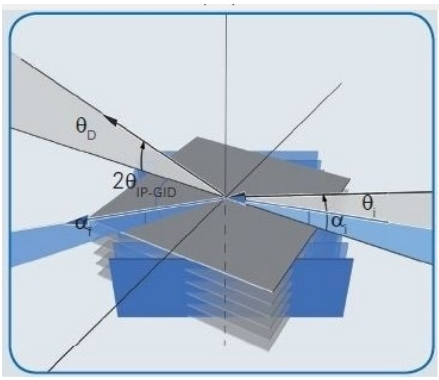

Figure 2.7: The diffraction geometry of grazing incidence. The beam is diffracted in the plane at the angle 2θ. Credit: https://www.azom.com/article.aspx?ArticleID=12666

XRD measurements of "thin" (<100 nm) films usually produce a week signal from the film and a strong interference signal from the substrate. One way to avoid the above problem is to increase the signal intensity from the film itself. GIXRD solves this problem by performing a 2θ scan with a fixed grazing angle of incidence. This fixed angle is chosen to be slightly higher than the critical angle in order to avoid the total internal reflection inside the material of thin film. This small incident angle of X-rays allows only a

swallow penetration of surface thus making measurements surface insensitive. This technique is useful in studying the surfaces and layers as it allows only limited wave penetration.

2.2.4 Field-Emission Scanning Electron Microscope (FESEM)

The scanning electron microscope (SEM) produces images of the surface of any sample by scanning that surface via a focused high energy electron beam. The interaction of these electrons with atoms present in the sample causes the emission of many secondary electrons that can provide information about the topographical features present on the surface and composition of the sample. In field emission scanning electron microscope (FESEM), primary electrons are produced by a field emission source under the influence of a very high electrical field. FESEM produces clearer, less electrostatically distorted images when compared with conventional SEM. These so-called primary electrons are focused via a electronic lenses to produce a narrow beam of electrons which is bombarded on the object in a zig-zag pattern. These collisions cause the emission of secondary electrons from the surface of the object. A detector detects these secondary electrons and produces an electronic signal. This signal is amplified and transformed into a video image.

Figure 2.8: Photograph of FESEM, Zeiss Supra 55. Credit: Sophisticated instrumentation centre (SIC), IIT Indore.

A FESEM can be used as a very high-resolution microscope, which can visualize the topographic details even below 100 nm scale on an object.
In this research work, the images of the top surface of Y_2O_3 film were taken by FESEM, Supra55 Zeiss. The actual image of this system is shown in figure 2.8.

2.2.5 High-Resolution Transmission Electron Microscopy

High-resolution transmission electron microscopy (HRTEM) is a specialized transmission electron microscope (TEM) that can be used for imaging the atomic structure of a sample. TEM uses a beam of electrons that passes through a very thin (<100 nm) sample. The interaction of these energetic electrons with the sample is used to form the image of the sample. TEM can provide morphological, compositional and crystallographic information of any sample. TEM has very high resolution than light microscopes as it uses electron as they have the smaller De Broglie wavelength. This high resolution allows instrument to capture very fine details such as a single column of atoms. TEM works in various operating modes, which include conventional imaging, scanning TEM imaging (STEM), diffraction, and spectroscopy. A TEM is composed of many modules; some of them are given as follows:

1. A Vacuum system for traveling of the electrons.

2. Electron emission source which uses thermionic or field emission for the generation of the electron stream into the vacuum.

3. A series of electromagnetic lenses that are made of a solenoid coil, nearly surrounded by ferromagnetic materials.

The electrons, which are emitted from a filament, pass through the multiple electromagnetic lenses. The speed of these electrons is directly related to the electron wavelength and determines the image resolution. The high-resolution transmission electron microscopy (HRTEM) uses an interference pattern to create a phase-contrast image; this interference pattern is created by the transmitted and the scattered beams. The captured image can have a very high resolution; it can detect a single unit cell of the crystal. HRTEM is used for investigating crystal structures and lattice

deficiencies, point defects, stacking faults, dislocations, grain boundaries, and defect in different kinds of materials on an atomic resolution [6].

In this research work, the quality of the Y_2O_3/Al or Y_2O_3/*n*-Si interface was studied using HRTEM. The photographic image of HRTEM is shown in figure 2.9.

Figure 2.9: Photographic image of the HRTEM system. Credit: https://www.jeol.co.jp/en/products/detail/JEM-2100.html

2.2.6 Conductive Atomic Force Microscopy (C-AFM)

Conductive atomic force microscopy (C-AFM) is a method that simultaneously processes the topography of a thin film as well as the electric current at the tip contact with the surface of the thin film. The topography is analyzed by sensing the change in the vibration of a cantilever by means of an optical system (a combination of laser and photodiode). The current, which is passing through the tip, measured using a current-to-voltage preamplifier setup as the current is passing through the cantilever may be as minor as pico-ampere. In C-AFM, during topographical measurement, a conductive cantilever scans the thin film sample surface in contact to produce a topographical map, and the change in electric current passing through the cantilever is measured simultaneously. During C-AFM, the sample is kept stationary on the

sample-holder by a conductive tape/paste. A Faraday cage surrounds the sample to prevent the perturbations caused by any external electrical noises.

In this research work, the quality of the Y_2O_3 thin film surface was studied using C-AFM. The schematic of the C-AFM is depicted in figure 2.10. The conduction mechanism of our device has been clarified using C-AFM. C-AFM is performed on the surface of the switching layer, and the results of measurements have been analyzed to understand the behavior of device with the bias applied.

In this research work, Shimadzu, SPM-9500J3 instrument with an Au coated Si_3N_4 probe has been used for C-AFM to study the morphology of the Y_2O_3 surface.

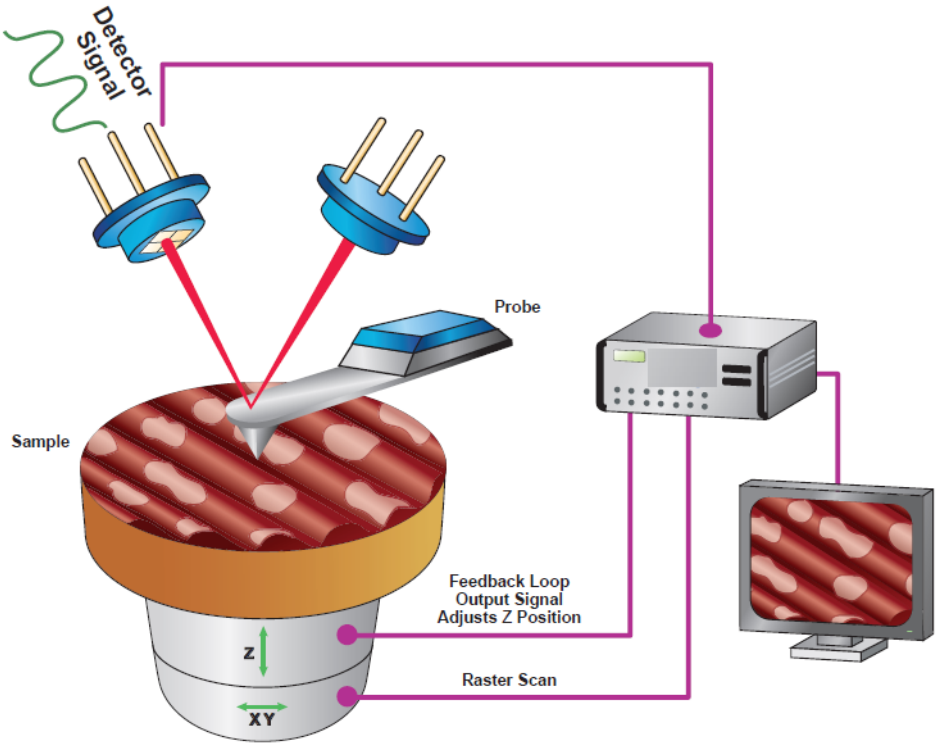

Figure. 2.10: Schematic representation of C-AFM. Credit: https://www.bruker.com/products/surface-and-dimensional-analysis/atomic-force-microscopes

2.3 References

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Chapter 3

Design and Fabrication of Yttria based Memristive Devices

3.1 Introduction

In 2008, Williams *et al.* [1] synthesized the memristive system for the first time. After that, many oxide materials (TiO_x [2], InGaZnO [3], ZnO [4], Ti/ZnO-NWs/ZnO-seed-layer/*p*-Si [5] and WO_x [6]) has been used to fabricate the memristive systems. There are very few attempts to study Y_2O_3 based memristive systems [7], [8]. Yttria has been studied as a gate oxide material in transistor-based applications [9]. Yttria exhibit excellent physical properties such as low lattice mismatch ($\boldsymbol{a_{Y_2O_3}}$ = 1.060 nm, $2\boldsymbol{a_{Si}}$ = 1.086 nm) with Si substrate [9], large bandgap (~5.1 eV) [9], high dielectric constant (~10−18) [9] for RRAM applications. In this chapter, the experimental steps, which are used in the study of the fabrication of yttria based memristive system, have been discussed. Since the DIBS system has been used for the first time in the fabrication of yttria based memristive system, we have designed a fabrication process flow (figure 3.1) to perform our study successfully. The steps of this process flow have been given below:

1. Deposition of the yttria switching layer on different substrate temperature at constant Argon (2 sccm) and oxygen (3 sccm) partial pressure (stage 1).
2. Appropriate devices (substrate temperature) will be selected on the basis of I-V measurements of the above devices (deposited in stage 1).
3. Deposition of the yttria switching layer on different Ar:O_2 partial pressure at constant substrate temperature (stage 2).
4. Appropriate devices (Ar:O_2 partial pressure) will be selected on the basis of the I-V measurement of the above devices (deposited in stage 2).
5. Deposition of yttria switching layer on different bottom electrodes (Al, *n*-Si, *p*-Si) at constant deposition temperature (chosen after stage 1) and constant Ar:O_2 (chosen after stage 2). (stage 3)

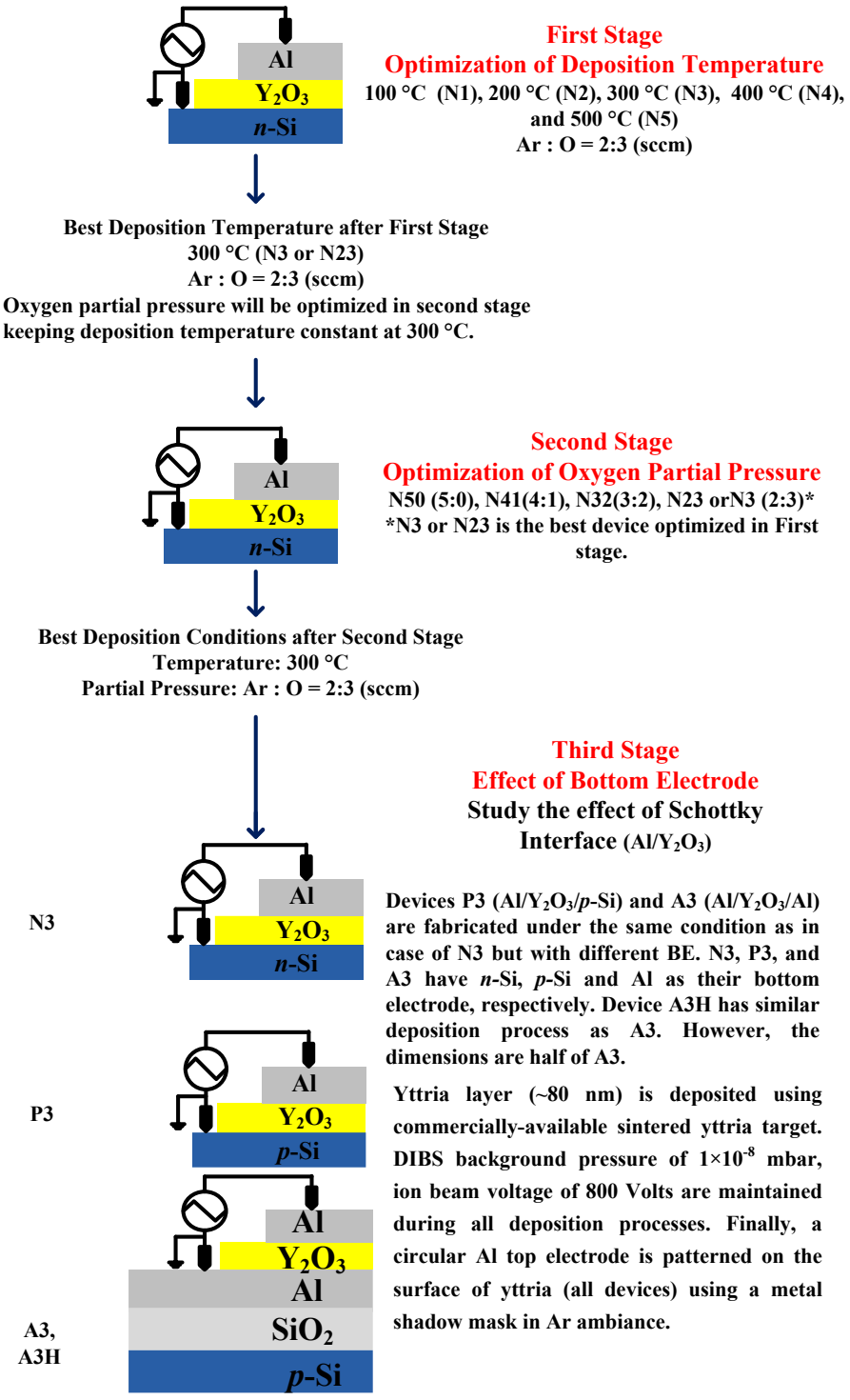


Figure 3.1: Schematic of Y_2O_3 based devices and stages of our experiment.

Surface contamination of silicon wafers is one of the most common problems in the semiconductor industry. Most commonly, silicon wafers become contaminated with organic particle contaminants as soon as they are exposed to the air. Strong electrostatic forces cause these organic

particle contaminants to bond on to the surface of the wafer. To effectively clean silicon wafers from organic particle contaminants, the following cleaning steps have been used in this study:

1. First, a wafer is put in trichloroethylene (C_2HCl_3) on sonicator for ultrasonic cleaning for 10 min, and then the wafer is rinsed with deionized (DI) water.
2. After the first step, the wafer is put in acetone ($(CH_3)_2CO$) on sonicator for ultrasonic cleaning for 10 min, then the wafer is rinsed with deionized (DI) water.
3. After the cleaning with acetone, the wafer is put in Isopropyl alcohol ($CH_3CHOHCH_3$) on sonicator for ultrasonic cleaning for 10 min. Then the wafer is rinsed with deionized (DI) water.

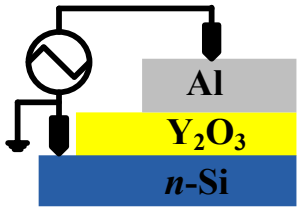
In this chapter, we will discuss other deposition conditions in detail; the measurement of characteristics of these devices will be discussed next chapters.

3.2 Optimization of Deposition Temperature

The DIBS system has been deployed to deposit yttria on *n*-type low-resistive (0.001-0.005 Ω cm) Si (100) substrate. In this stage, yttria (~80 nm) is deposited at different substrate temperatures of 100 °C - 500°C by the DIBS system, as shown in figure 3.2. The flow rate of Ar:O_2 is set at 2:3 (N23) during film deposition.

We have used the following protocol during deposition:

1) Native SiO_2 is etched out by assist ion source with the help of ion plasma (Ar^+) bombardment (10 min) at room temperature. 2) The substrate temperature is steadily increased up to the preferred temperature. 3) The primary deposition RF source is started at 200 V beam voltage. 4) After 1 min, O_2 is gradually introduced into the deposition chamber, and the ratio of Ar and O_2 has been changed slowly up to 2:3 sccm. 5) The ion beam voltage of the primary RF deposition source is increased up to 800 V beam voltage.



100 °C (N1), 200 °C (N2), 300 °C (N3), 400 °C (N4), and 500 °C (N5)
Ar : O = 2:3 (sccm)

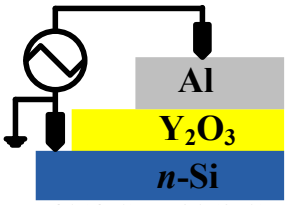
Figure 3.2: Schematic of devices (N1, N2, N3, N4, and N5) fabricated during optimization of deposition temperature. Circular top electrode (diameter = 1 mm).

After the above deposition steps, we have performed the current-voltage measurement of these devices. After the measurement, we have chosen those devices for further characterization, which have shown any kind of RS. A detailed discussion of the obtained results has been done in the next chapter. Deposition temperature, which is used to deposit that device considered as the best candidate for further optimization in partial pressure.

3.3 Optimization of Partial Pressure

After the optimization of deposition temperature, the DIBS system is deployed to deposit yttria on *n*-type low-resistive (0.001-0.005 Ω cm) Si (100) substrate for the optimization of partial pressure. At this stage, yttria (~80 nm) is deposited at a constant temperature of 300ºC (N3) by the DIBS system. The flow rate of Ar:O_2 is varied at 5:0 (N50), 4:1 (N41), 3:2 (N32), and 2:3 (N23) during film deposition.

We have used the following protocol during deposition:
1) Native SiO_2 is etched out by DC assist ion source with the help of ion plasma (Ar^+) bombardment (10 min) at room temperature. 2) The growth temperature is kept constant at the desired deposition temperature. 3) The primary deposition RF source is started at 200 V beam voltage. 4) After 1 min, O_2 is gradually introduced into the deposition chamber, and the flow rate of Ar and O_2 has been changed slowly up to the desired ratio. 5) The ion beam voltage of the primary RF source is increased up to 800 V beam voltage.



N50 (5:0), N41(4:1), N32(3:2), N23 orN3 (2:3)

Figure. 3.3: Schematic of devices 5:0 (N50), 4:1 (N41), 3:2 (N32), and 2:3 (N23) fabricated during optimization of partial pressure. Circular top electrode (diameter = 1 mm).

After the deposition, current-voltage measurement is performed for these devices. After the measurement, we have chosen the devices which have shown the best RS parameter. A detailed discussion of the obtained results has been done in the next chapter. Ar to O_2 partial pressure ratio, which is used to deposit a successful device, considered as the best candidate to study the effect of Schottky behaviour on memristive behaviour of yttria based devices.

3.4 Variation of Bottom Electrode

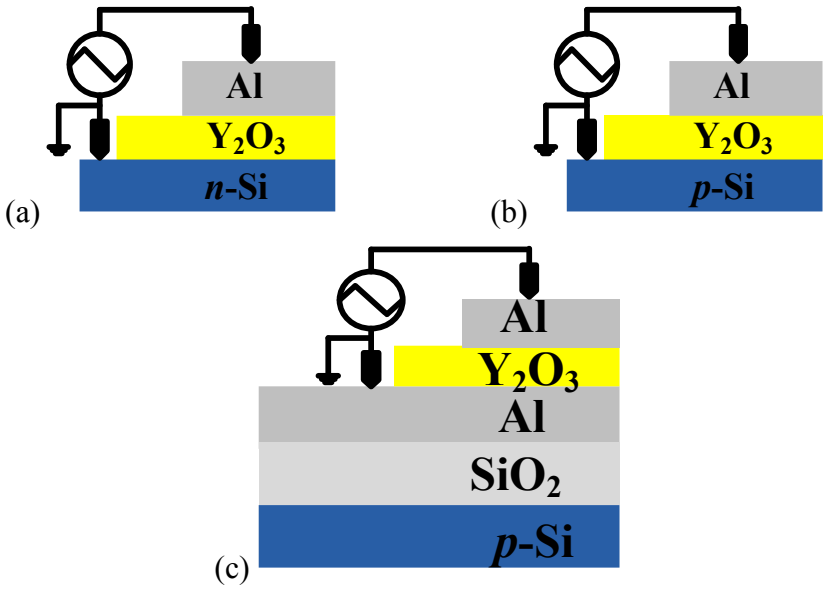


Figure 3.4: Variation of bottom electrode (a)N3 (b)P3 (c) A3. Circular top electrode (diameter = 1 mm).

After the optimization of DIBS parameters, three devices N3, P3, and A3, are fabricated at different bottom electrodes to understand the effect of the

interface on the mechanism of our devices. Devices N3, P3, and A3 have the same deposition conditions but have different bottom electrodes (BE). BE of N3 (*n*-Si), P3 (*p*-Si), and A3 (Al) are shown in figure 3.4. It is noteworthy that N3 has a single Schottky interface (Al/Y_2O_3) [27], whereas A3 has dual Schottky interfaces ($Al/Y_2O_3/Al$). The DIBS system is deployed to deposit yttria (~80 nm) for devices N3, A3, and P3 while the flow rate of oxygen and argon is maintained at 3 and 2 sccm, respectively, during deposition. An insulation layer of SiO_2 (thickness =250 nm) is deposited on Si for device A3. After that, Al bottom electrode (thickness = 150 nm) is sputtered on the insulation layer.

After this step, we have performed the current-voltage measurement of these devices to understand the effect of the Schottky interface and the mechanism of switching. A detailed discussion of obtained results has been done in a later chapter.

3.5 Conclusion

In this chapter, we have discussed the design of our experiment, which can prove our hypothesis of resistive switching in yttria based RRAMs. The deposition conditions, which are used in all three stages of our experiment, have been described in this chapter in detail. Apart from it, the schematic structures of all devices have also been presented here.

3.6 References

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Chapter 4

Effect of Deposition Parameters on Memristive Behavior of Yttria based Devices

4.1 Introduction

The RS behaviour of DIBS grown yttria based devices has been studied for the first time during this study. It is important to note that the DIBS system provides many control parameters such as deposition temperature, partial pressure, and ion beam voltage, etc. These parameters play a critical role in deciding the thin film properties such as resistivity, crystallinity, and surface roughness, etc. These properties of thin-film will affect the RS behaviour of our films. Therefore, we need to identify the optimized values of these deposition parameters, which can enhance the RS characteristics of the device. After each stage of deposition, we have performed current-voltage (I-V) measurement and all other pulse-mode measurements of these memory devices using Keithley 4200A semiconductor parametric analyzer at room temperature (RT) in order to know the optimized values of these parameters. I-V measurements of samples have been performed under triangular waveform voltage excitation (-5 V to 5 V, compliance current of 10 mA) for hysteresis loop analysis. After that, in order to understand the relation between crystallinity and switching characteristics, the X-ray diffraction (XRD) studies have been performed. We have studied the interface between the bottom electrode and yttria thin film by cross-sectional high-resolution transmission electron microscopy (HR-TEM).

In this chapter, firstly, the effect of deposition conditions on RS behaviour of our devices is explored. Then we have tried to find out the optimized value of these parameters, which will enhance the memristive behaviour of our devices.

4.2 Stage 1: Effect of Deposition Temperature

This stage will allow us to understand the effect of deposition temperature on the memristive behavior of our devices. Five types (N1 (100 °C), N2 (200 °C), N3 (300°C), N4 (400°C), and N5 (500°C)) of devices have been deposited at different deposition temperatures with Ar:O_2 flow rate of 2:3 sccm. The complete deposition procedure has been discussed in the previous chapter (section 3.2) for this stage.

4.2.1 X-Ray Diffraction (XRD) Study

Figure 4.1 (a) shows XRD patterns of DIBS grown yttria thin films prepared during deposition temperature optimization.

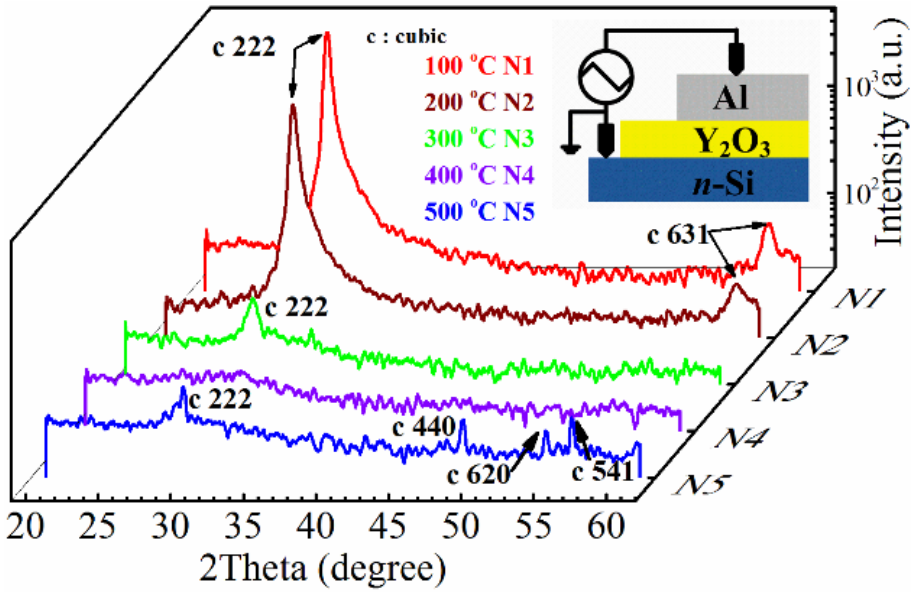


Figure 4.1: XRD Analysis for Y_2O_3 thin film deposited in devices N1, N2, N3, N4, and N5. All devices have the same structure, as shown in the inset.

It can be observed from table 4.1 that the crystallinity of thin-film reduces with an increase in deposition temperature. This pattern is the opposite of the general relation between crystallinity and deposition temperature. A similar phenomenon has also been observed in Ga-doped MgZnO [1], which is also deposited by DIBS. Here, it is worth paying attention to that a high ion beam voltage of 800 V is maintained during the deposition of yttria thin film. The ion beam voltage controls the kinetic energy of ions

in the DIBS system. The reason behind the reduction in the crystallinity of yttria thin film with an increase in the deposition temperature can be understood as follows: High beam voltage provides sufficient kinetic energy and surface mobility to atoms to occupy stable locations inside the yttria crystal lattice structure [2] even at lower deposition temperature. This provides stability and highly *c*-axis oriented structures with the improved crystalline quality of the film [2]. Whereas at higher deposition temperature, the high kinetic energy of atoms causes problems in the formation of yttria bonds and may cause re-sputtering of the deposited film. This process produces defects in the film and causes degradation in the crystallinity of film [2].

Table 4.1 XRD Results

Sample Name (Deposition Temperature)	2θ-Information (Phase) C-Cubic	Remarks
N1 (100°C)	~28.8° (c 222)	Highly Crystalline
N2 (200°C)	~28.8° (c 222)	Highly Crystalline
N3 (300°C)	~28.8° (c 222)	Short-range Amorphous
N4 (400°C)	No observable Peak	Amorphous
N5 (500°C)	~28.8° (c 222), ~49.4° (c 440), ~54.18° (c 620) and ~56.18° (c 541)	Polycrystalline

After this step, we have studied the SEM and HRTEM studies of these thin films in order to understand the surface topology of our films.

4.2.2 Yttria Surface Topology and Interface Study

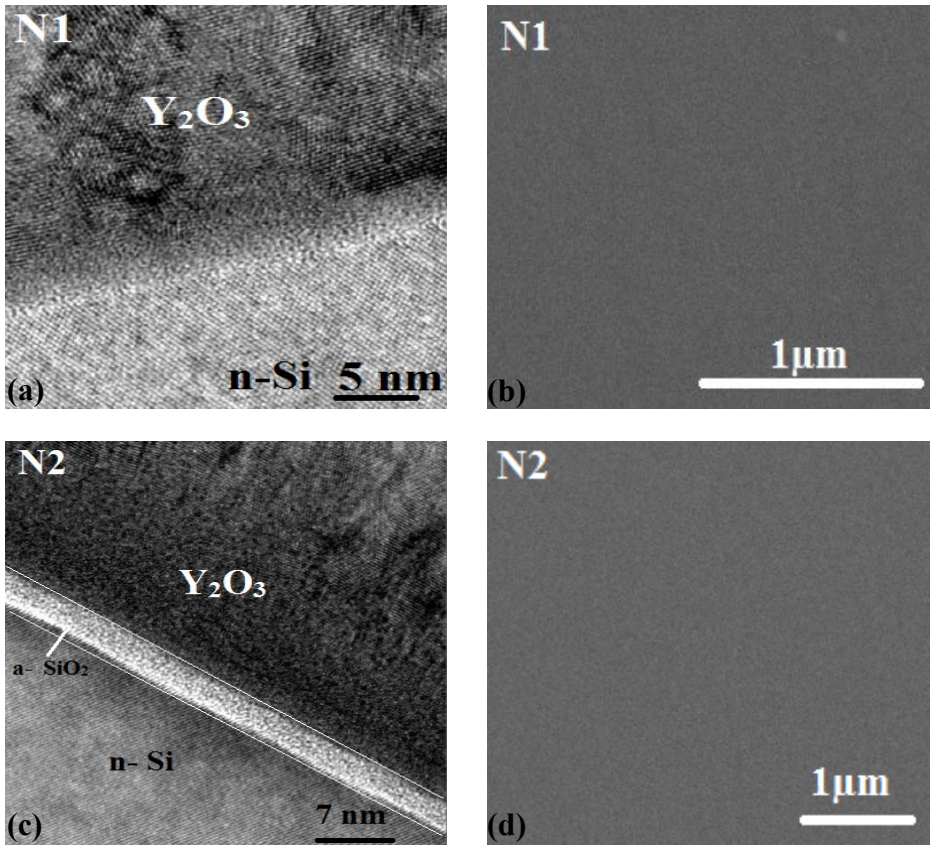
Field emission scanning electron microscope (FESEM) images of the top surface of yttria for all devices (N1, N2, N3, N4, and N5) have been performed in order to understand the role top surface variations on RS

behaviour of devices. High-resolution transmission electron microscopy (HRTEM) images have also been done to understand the effect of the Y_2O_3 and *n*-Si interface on the surface morphology of these devices.

Two correlation can be observed between deposition temperature, grain surface area, and interfacial SiO_2 layer (figure 4.2.1). These two correlations are given as:

1. It can be observed that the thickness of interfacial SiO_2 increases with the increases in deposition temperature. The thickness of amorphous SiO_2 layer for N1 (figure 4.2 (a)), N2 (figure 4.2 (c)), N3 (figure 4.2 (e)), N4 (figure 4.2 (g)) and N5 (figure 4.2 (i)) is ~0 nm, ~4 nm, ~6 nm, ~35 nm, and ~37 nm, respectively.

2. The grain surface area variations of the yttria surface increases as the thickness of amorphous SiO_2 layer and deposition temperature increases. SEM images of the N1 (figure 4.2 (b)), N2 (figure 4.2 (d)), N3 (figure 4.2 (f)), N4 (figure 4.2 (h)) and N5 (figure 4.2 (j)) clearly verify this fact.



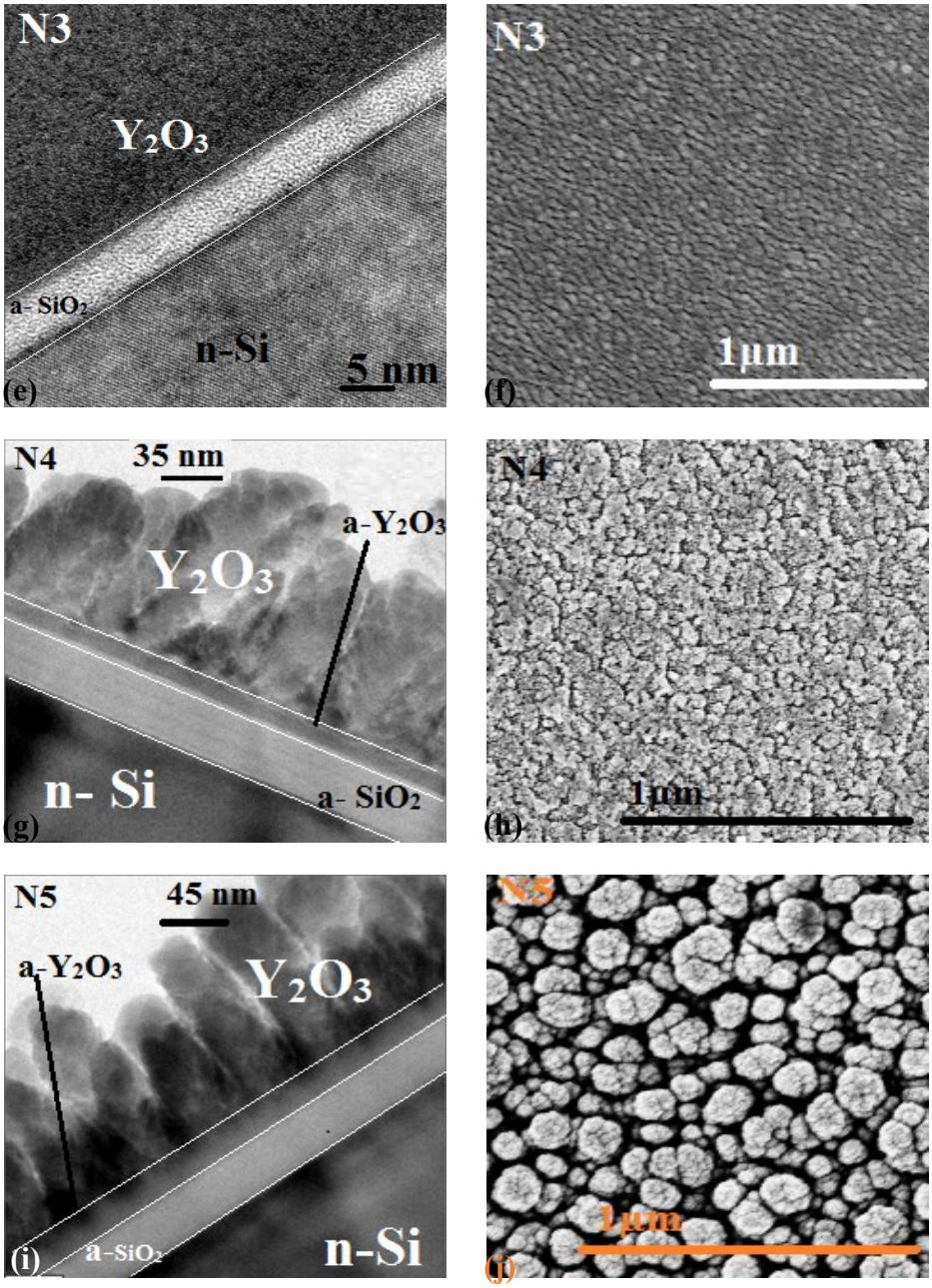


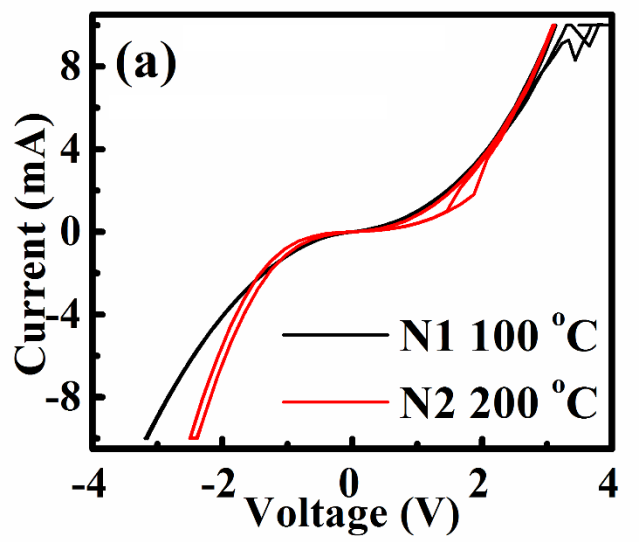
Figure 4.2: HRTEM images of the interface between Y_2O_3/ n-Si for (a) N1, (c) N2, (e) N3, (g) N4, and (i) N5. FESEM images of the top surface of yttria for (b) N1, (d) N2, (f) N3, (h) N4, and (j) N5.

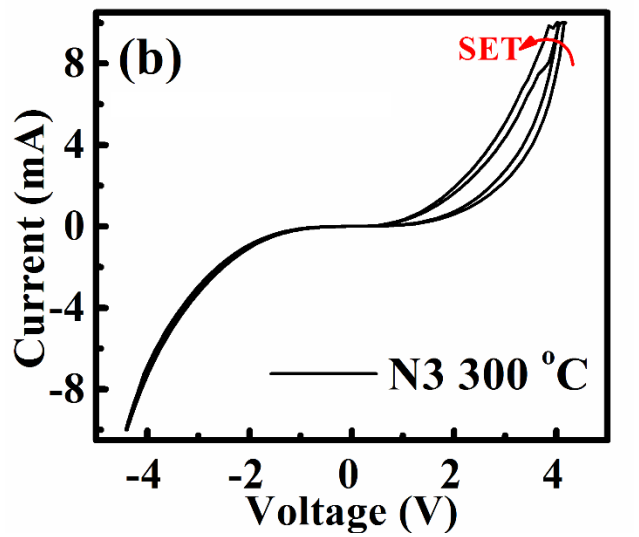
In the case of N1 and N2 formation of SiO_2 is negligible, and it can be observed that N1 and N2 have a very smooth top surface with no observable grain boundaries. This expected because of low lattice mismatch ($\boldsymbol{a_{Y_2O_3}}$ = 1.060 nm, $2\boldsymbol{a_{Si}}$ = 1.086 nm) between yttria and Si substrate [2], [3]. Apart from this, the formation of very thin amorphous yttria films (~20 nm for N4 and N5) can also be observed on top of the amorphous SiO_2, which is

followed by the growth of nano stalagmite of yttria in the lowest energy lattice plane.

4.2.3 Current-Voltage Measurements

A triangular voltage excitation is applied in order to study the I-V characteristics. The crystallinity of these devices is given in table 4.1. It is important to note that only amorphous ((N3, figure 4.3(b), N4, figure 4.3(c)), and polycrystalline devices (N5, figure 4.3(d)) show RS whereas highly crystalline device N1 and N2 do not show any RS. All of these devices (N3, N4, and N5) show a pinched hysteresis loop, which is a necessary condition for the memristance [3].





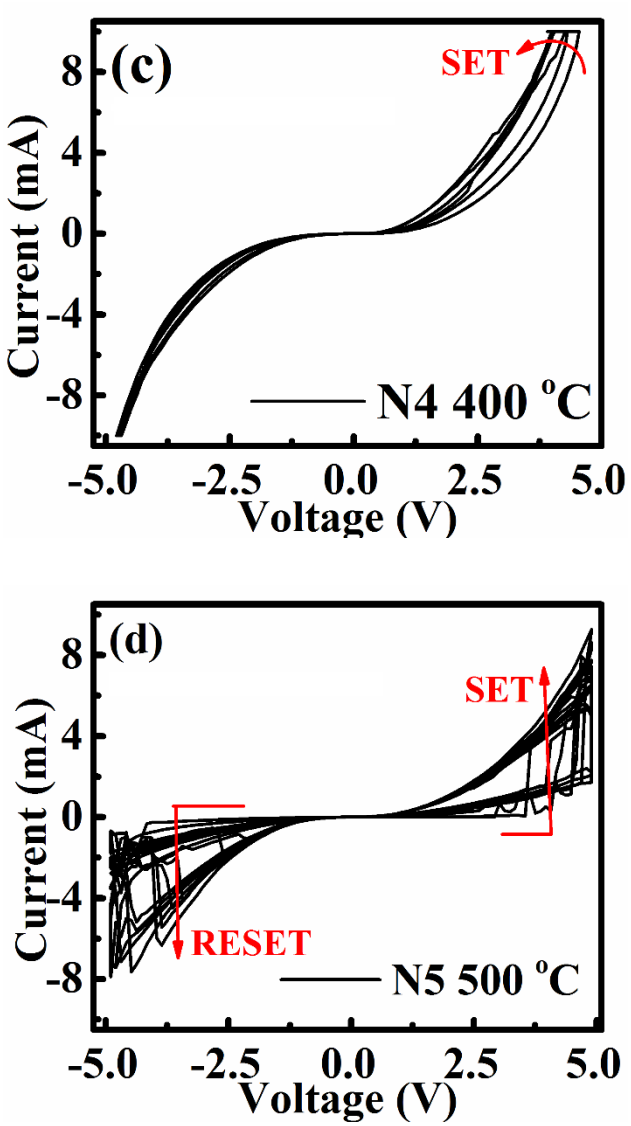
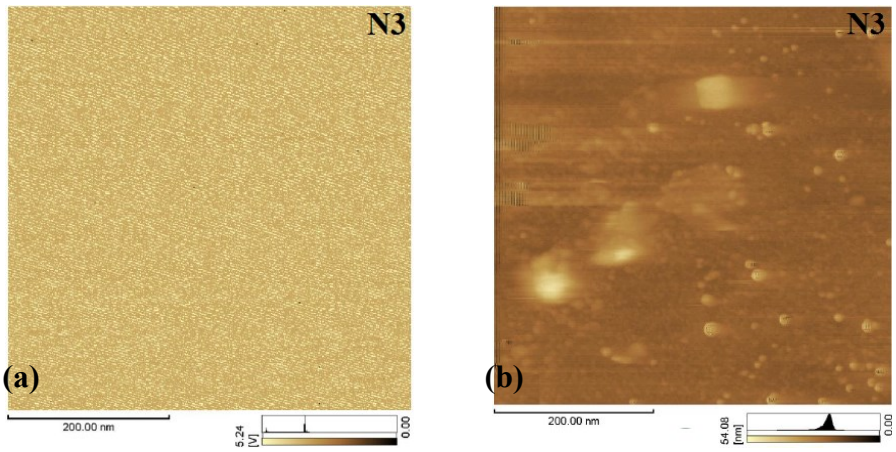


Figure 4.3: I-V characteristics of (a) N1 and N2 (b) N3 (c) N4 (d) N5.

Contrary to highly crystalline films (N1 and N2), amorphous (N3 and N4), and polycrystalline (N5) film contains a huge number of oxygen ions, oxygen vacancies, and defects. These ions, oxygen vacancies, and defects provide favorable circumstances for the generation of RS [4], [5]. These oxygen vacancies and ions play a crucial part in the mechanism of oxide RRAMs [6]. So it can be deduced that highly ordered crystalline structure of yttria thin films is counterproductive for the realization of reliable resistive switching devices [7].

4.2.4 Absence of Filamentary Switching

The RS behavior, which is demonstrated by N3,N4, and N5, maybe originated due to either filamentary switching (FS) [4] or interface-type switching [4]. The FS can be identified by the presence of filaments (low resistive regions) on the surface of the switching layer. Figure 4.4 (a), 4.4 (b), and 4.4 (e) show the current distribution (scan area: 500×500 nm^2, at 10V bias) on the surface of N3, N4, and N5 respectively. FS is highly improbable in our devices because C-AFM could not detect any significant change in current while scanning the surface at the 10 V bias. No high conductivity regions are detected on the surface of the thin film. This points out the absence of forming process which is a vital step for FS. Moreover, application of a small peak electric field of 0.5 MV/cm on our device (thickness ~100 nm) is not sufficient enough to start a forming process. The forming process occurs near breakdown in amorphous and microcrystalline dielectrics [2]. In oxide cells, forming causes the generation of oxygen vacancies, which in turn allows the creation of conducting filaments [2] . It should be noted that the rated current sensitivity of our C-AFM is of the order of pA (≥1pA), but external noises may not allow us the detection of such small currents. In our case, C-AFM instrument (sensing probe radius ~30 nm) could not detect any significant current. Due to these result it can be deduced that the current passing through our films is smaller than few pA. The roughness of N3, N4, and N5 has also been studied via AFM studies; it is also observed that the roughness of surface increases as we move from N3 to N5.



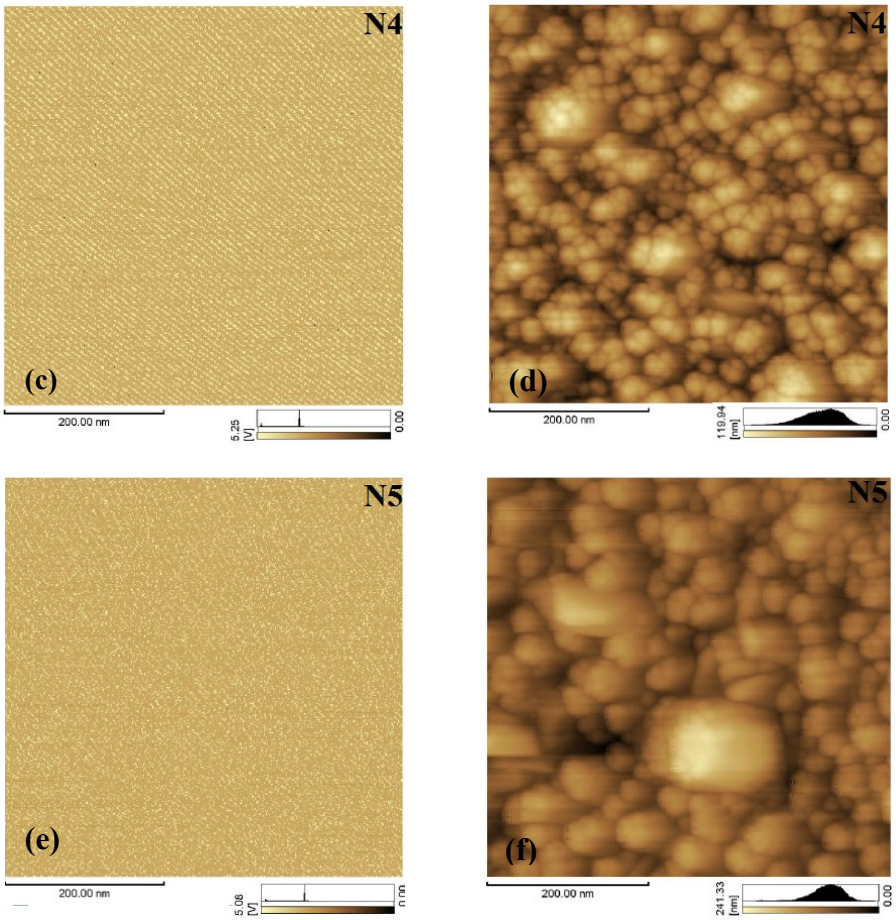


Figure 4.4: C-AFM shows the absence of high conductivity regions in the current distribution (500×500 nm^2) map of (a) N3 (c) N4 (e) N5 at 10 V. C-AFM image of surface morphology of (b) N3 (d) N4 (f) N5.

4.2.5 Variability Analysis in Current-Voltage Measurements

Statistical variability of parameters in any memory device plays a critical role in its acceptance as a technically viable device. Low statistical variability in device parameters is essential as it eases the design of other support systems such as memory controller. We have studied the variability in our device, which shows RS, in order to understand the correlation between morphological parameters with electrical parameters. This study will give us information about those morphological parameters which are needed to be controlled precisely in order to get low variability in devices. Figure 4.5 (a) shows mean voltages (M_v) and standard deviation (σ_v) of the set and reset voltages for devices N3, N4, and N5 as only these devices show RS. Figure 4.5 (b) shows mean (M_v) and standard deviation (σ_v) of

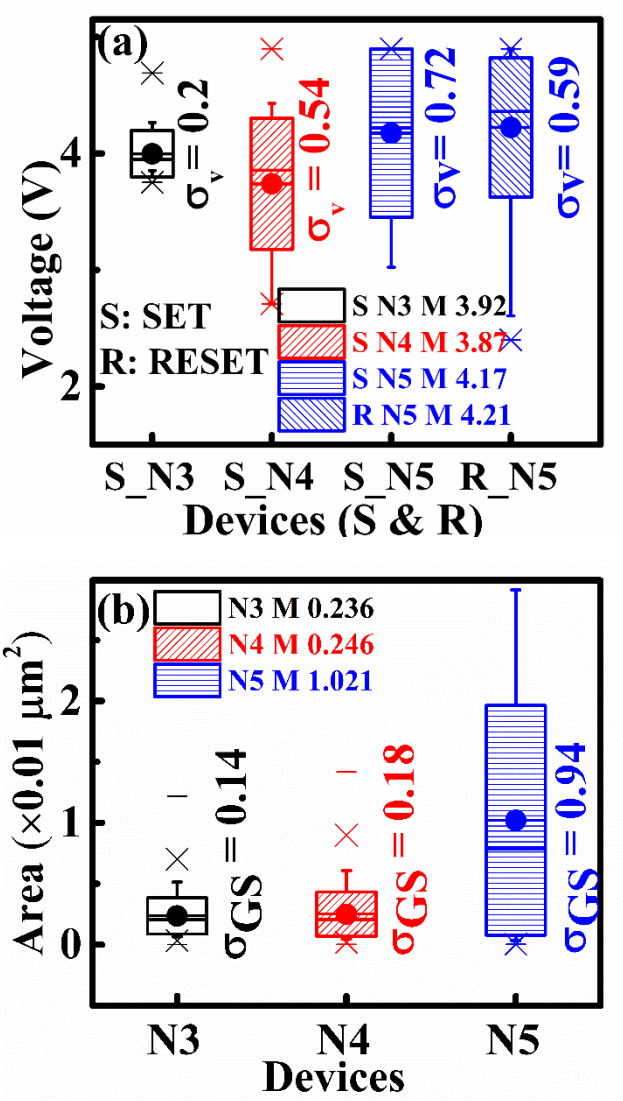


Figure 4.5: (a) Mean (M) and Standard deviation (σ) of the 'SET' and 'RESET' voltages. (b) Mean (M) and Standard deviation (σ) of the grain surface (GS) area.

the grain surface area for devices N3, N4, and N5. It can easily see that σ_v increases as we move towards devices (N3→N5) along with grain surface area variation and surface roughness. In order to quantify the top gain surface (GS) variations, we have used image processing techniques on FESEM image (section 4.2.2) of devices N3 (fig 4.2(f)), N4 (fig 4.2(h)) and N5 (fig 4.2(j)) using ImageJ software. Such FESEM image processing techniques were widely used for particle size measurements [8]. We have extracted the mean grain surface (GS) area (M_{GS}) and standard deviation (σ_{GS}) of the GS area in these devices. The variability in GS area (σ_{GS})

increases as the deposition temperature increases from 300 (N3) to 500 ^{o}C (N5) for yttria thin films.

The similar results have been reported (qualitatively) in the cases of ZrTiO [9] and PSCMO [10] through deductions from electrical characterizations only. It can be observed that as GS area deviation (σ_{GS}) (figure 4.5(b)) increases, the standard deviation of set-reset voltage (σ_V) (figure 4.5(a)) also increases. Grain boundaries (GBs) and grain surface (GS) area have an essential role in RS behavior [9], [11]–[13]. GBs are closely related to grain shape and size as it determines the GS area variation. The concentration of oxygen vacancies (O_v) is very high along the GBs, which allows leakage current flow through GBs [12], [14]. The variation in O_v will be closely related to grain boundary and grain surface variations. These oxygen vacancies and ions are supposed to play an essential role in the mechanism of oxide RS devices [6]. The change from unipolar switching (N3 (figure 4.3(b)) and N4 (figure 4.3(c))) to bipolar switching (N5, (figure 4.3(d))) can be observed very clearly. Das *et al* [2] have demonstrated that the change in switching modes takes place we move from a system of single Schottky barrier diode (SBD) to double SBD. However, this cannot be the case here as all of these devices have the same structure (*n*-Si/Y_2O_3/Al). Only the surface roughness of the yttria film is observed to vary in N3, N4, and N5. Here, it can be said this transformation take place due to the substantial film roughness. Pseudo-bipolar behavior of N5 can be arise because of huge statistical variability in grain surface area which may result in to the high surface roughness.

4.2.6 Endurance Measurements

We have performed a write (SET) and erase (RESET) endurance measurement for devices N3, N4, and N5 under pulse voltage excitation. The devices N3 and N4 (figure 4.6 (a)) do not show any degradation even after ~23000 switching cycles. However, N5 (figure 4.6 (b)) fails after only ~7000 cycles. This endurance failure of N5 may be associated with the reduction in effective thickness of the insulating Y_2O_3 due to nano stalagmite formation. The HRTEM of N5 (figure 4.2(i)) suggests that it has

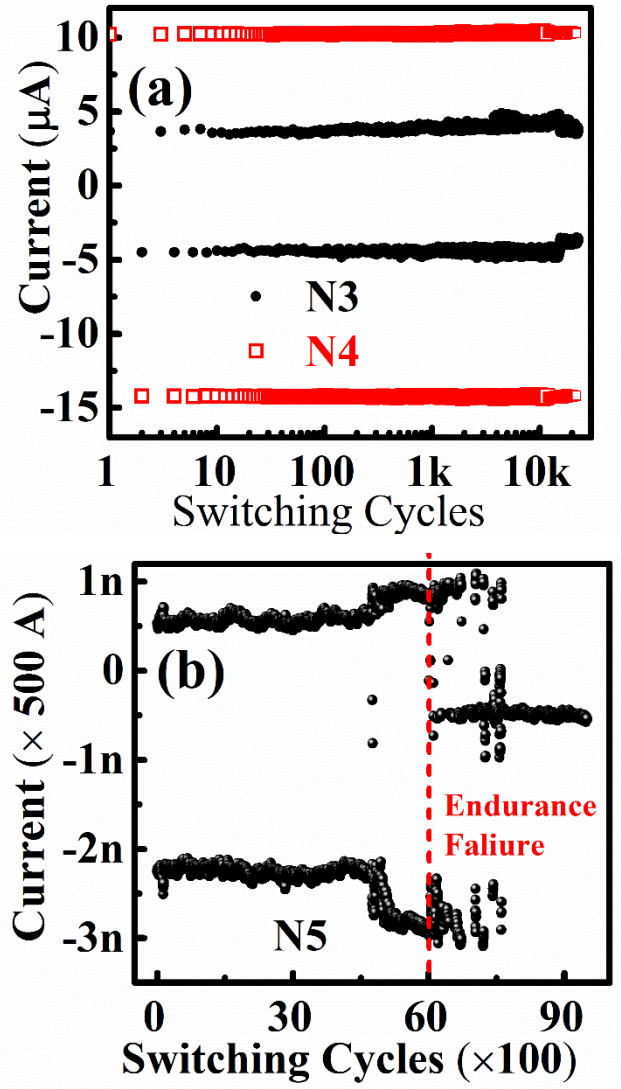


Figure 4.6: Endurance test of devices (a) N3 and N4, and (b) N5.

some stalagmite peaks. These peaks work as the point of high electrical stress in devices due to the high electric field. N5 device is subjected to very high electrical stresses in every cycle of pulses (during endurance measurement) at specific points, which accelerated the process of failure.

4.3 Stage 2: Effect of Partial Pressure

Partial pressure is another critical control parameter in our DIBS system, which can affect the RS behaviour of our devices. In our case, we can control Ar:O_2 flow rate (partial pressure), which in turn will control the oxygen vacancy concentration in our devices. After the optimization of deposition temperature (stage 1) for RS behaviour, we need to explore the

correct Ar:O_2 flow rate, which can further enhance the RS behaviour in DIBS grown yttria based devices. We have used the deposition procedure discussed in previous chapter (section 3.3) for this stage. We have deposited four more devices named as N50 (5:0), N41 (4:0), N32 (3:2), and N23 (2:3) at a constant deposition temperature of 300 ^{o}C. Measurements, which are discussed in last section (4.2), are also performed for these devices in a similar setup. Here it is important to note that device N23 is not new device it is same as N3 device which is discussed in previous section (4.2).

4.3.1 X-ray Diffraction (XRD) Study

Figure 4.7 shows XRD patterns of DIBS grown yttria thin films prepared during partial pressure optimization. It shows low-intensity peak c-222 for all types of samples. Here it is important to note that deposition temperature for all samples is 300 ^{o}C. It is claimed that the peaks, in figure 4.7, are of low intensity.

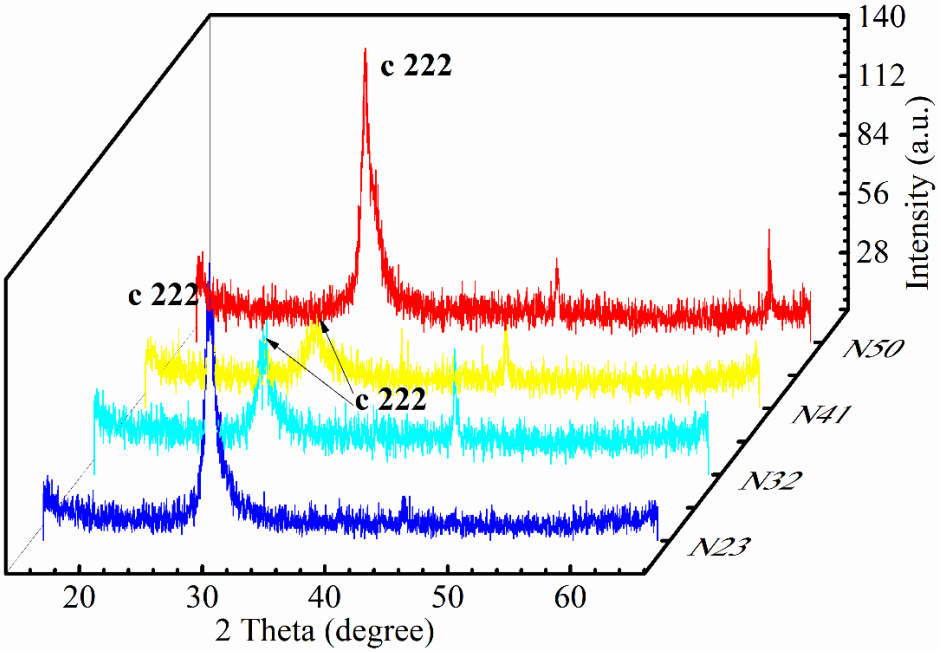


Figure 4.7: XRD patterns for yttria film used in devices N23, N32, N41, N50, and N5.

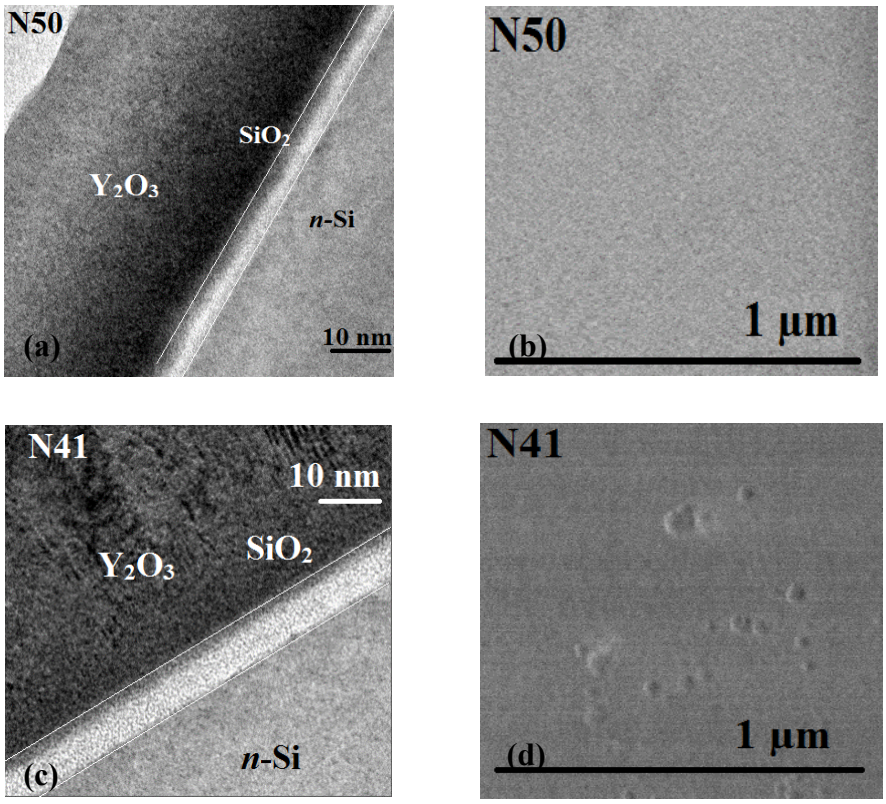
It becomes clear when we compare these XRD results with previous deposition temperature XRD results shown in the previous section (section

4.2, figure 4.1). These comparison hints that the sample crystallinity is mostly affected by deposition temperature, not by partial pressure as all of these devices are amorphous in nature. After this step, we have performed surface topographical and interfacial studies of these devices.

4.3.2 Yttria Surface Topology and Interface Study

High-resolution transmission electron microscopy (HRTEM) (figure 4.8) has also been done to understand the effect of the Y_2O_3 and *n*-Si interface on the surface morphology of these devices. FESEM images (figure 4.8) of the top surface of the yttria switching layer for all devices (N50, N41, N32, and N23) are used to show grain and grain boundaries.

Here, it can be observed that the thickness of the SiO_2 layer does not change very much with oxygen partial pressure.



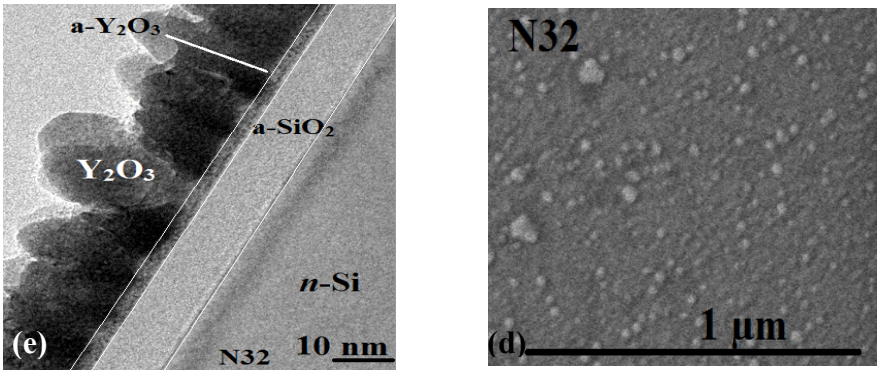


Figure 4.8: HRTEM images of the interface between Y_2O_3/n-Si for (a) N50, (c) N41, and (e) N32. FESEM images of the top surface of yttria for (b) N50, (d) N41, and (f) N32.

So it can be deduced that the thickness of the SiO_2 layer mainly depends on the deposition temperature. However, SEM images (figure 4.8(b), (d), and (f)) suggest that roughness of surface increases (very slowly) with an increase in oxygen partial pressure.

4.3.3 Current-Voltage Measurements

A triangular voltage excitation is applied in order to study the I-V characteristics of N50 (figure 4.9 (a)), N41 (figure 4.9 (b)), and N32 (figure 4.9 (c)). It is observed that N50 and N41 do not show any RS, whereas N32 shows RS for a small number of cycles (~4) initially, and subsequently, the RS behavior has disappeared. N50 (figure 4.9 (a)) device shows very high resistance in comparison to other devices such as N41 (figure 4.9 (b)), N32 (figure 4.9 (c)). Since N50 devices are grown in the absence of oxygen, thus yttria film is supposed to have the highest number of oxygen vacancies as compared to others grown in an oxygen-rich environment. It appears that such a massive number of oxygen vacancies actually hinder the movement of charge carriers and cause high resistance in the device. Devices N41 and N32 are comparatively more conductive than N50. However, these devices do not exhibit any RS.

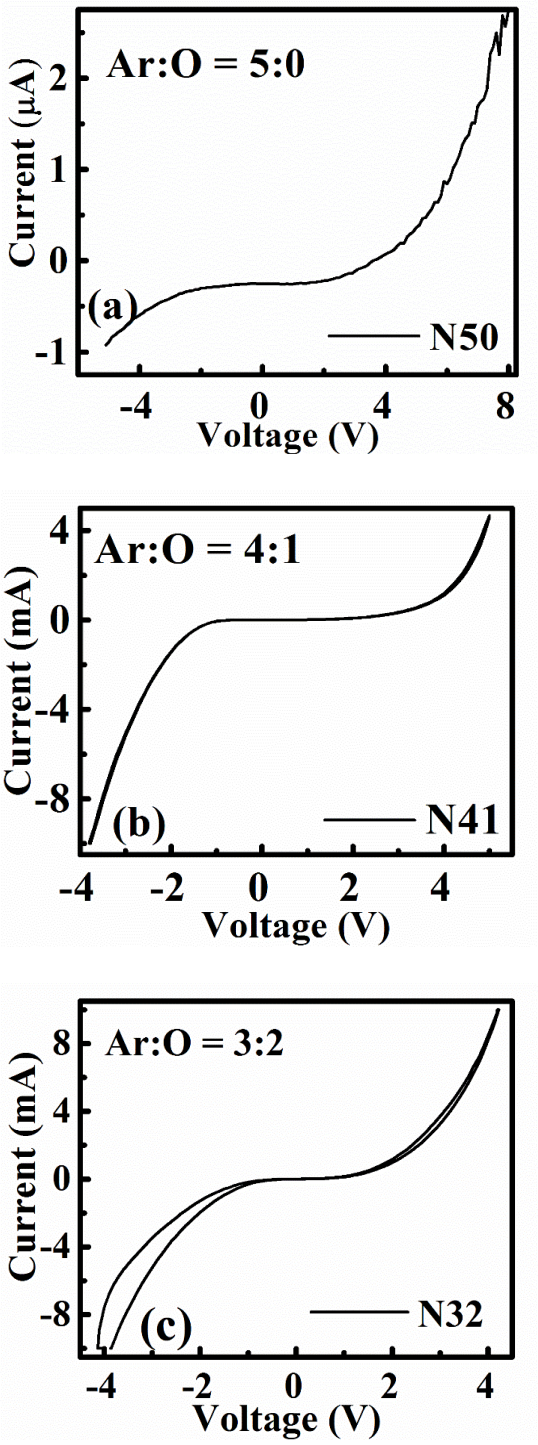


Figure 4.9: I-V characteristics of (a) N50 (b) N41 (c) N32.

4.4 Conclusion

In conclusion, it is found that the deposition temperature of 300°C and a mixture of Ar:O_2 with a ratio of 2:3, i.e., device N3 shows the best RS

characteristics. The amorphous yttria layer shows RS characteristics, while a highly crystalline yttria layer is not very useful for RS application. SiO_2 layer, present at yttria and Si interfaces, influences the roughness at the top surface of the yttria layer. As the thickness of the SiO_2 layer increases, the roughness of the yttria film also increases. As the level of surface roughness and thickness for the SiO_2 layer decreases, the endurance of the device improves. The irregularities at the top surface and bulk of the yttria layer are important for RS characteristics. But optimization of these irregularities is required in order to get the best result.

4.5 References

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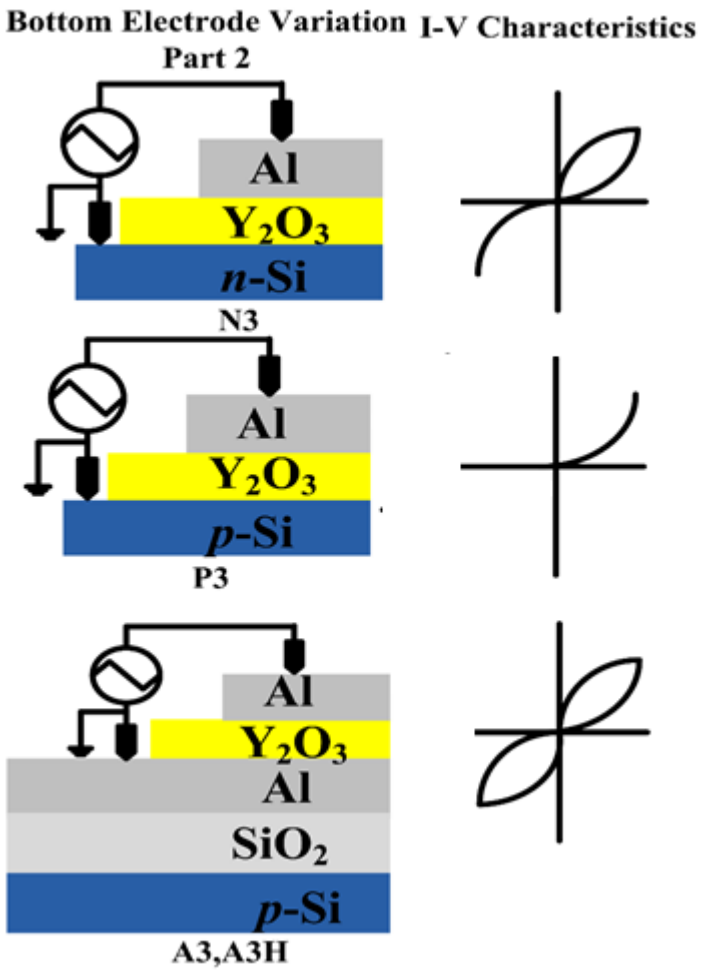
Chapter 5

Effect of Interface on Memristive Behavior of Yttria based Devices

5.1 Introduction

In the previous chapter (chapter 4), we have observed that devices such as N3, which is deposited at 300 ^{o}C and 2:3 (Ar:O_2) sccm flow rate, performs best in terms of overall performance. In this chapter, we will investigate the effect of interface on the performance of RS in Y_2O_3. This will be achieved by changing BE in N3 devices from *n*-Si into *p*-Si (P3) and Al (A3). This will allow us to understand the mechanism, which plays a significant role in the switching characteristics of the yttria based RS devices. The aim of thesis is not to minimize contact resistance to yttria and Si-wafer. Minimization of resistance will not be good idea as it will increase the current through device which will further increase the I^2R losses in our devices. Low resistive Si wafer provides a suitable basis for comparison between devices N3, P3, and A3. The effect of the Al interface on the performance of RS in Y_2O_3 can be isolated with the help of comparison with Si wafer. This will be achieved by changing the bottom electrode (BE) in N3 devices from n-Si into p-Si (P3) and Al (A3).

Four different types of devices (N3, P3, A3, and A3H) are fabricated by changing BE material, as shown in figure 5.1. Deposition temperature for the devices (N3, P3, A3, and A3H) is 300 ^{o}C and 2:3 (Ar:O_2) sccm flow rate. DIBS system is deployed for the deposition of all layers of every device according to the procedure, which is discussed in section 3.4 of chapter 3. Figure 5.1 shows the device structures along with their hypostatized I-V characteristics, which highlights the effect of variation in BE. After the deposition of devices, we have performed an I-V measurement and other pulse-mode measurements of these memory devices using Keithley 4200A semiconductor parametric analyzer at room temperature (RT).



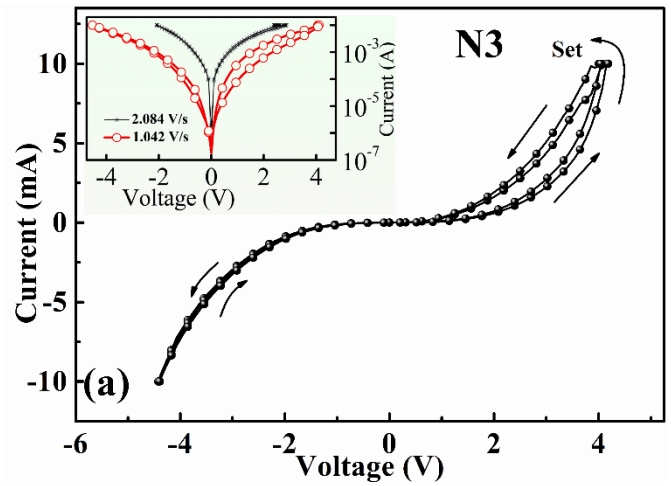
Device Name	Bottom Electrode	Y_2O_3 Thickness (nm)	Top Electrode Radius (mm)
N3	*n*-Si	100	2
P3	*p*-Si		
A3	Al		
A3H	Al	50	1

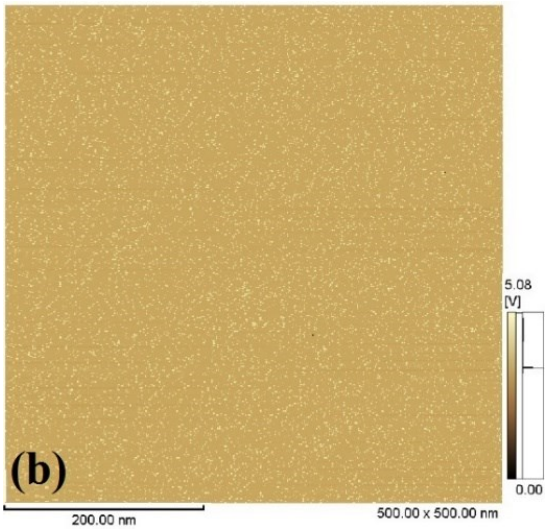
Figure 5.1: Device structures of N3, P3, A3, and A3H along with their hypostatized I-V characteristics.

5.2 Interface-type Switching

Figure 5.2 (a) shows the I-V characteristics of device N3. This device can be categorized as strictly unipolar as it shows a non-linear behavior (single-

valued function) in the third quadrant, and it shows a switching behavior in the first quadrant. This switching behavior may be caused by either filamentary switching (FS) [1] or interface-type switching [1]. The FS can be identified by the presence of filaments (low resistive regions) on the surface of the switching layer. Figure 5.2(b) and figure 5.2(c) show the current distribution (at ±10V bias) on the surface of the yttria thin film as measured by C-AFM. FS is highly improbable in our devices because C-AFM could not detect any significant change in the current while scanning the surface at the ±10 V bias. No distinct low resistive regions are observed on the surface (500×500 nm^2) of thin film. This indicates the absence of filaments [2]. It leaves only second type of mechanism, which is known as interface-type switching. The rectification orientation of I-V curves may be used for the identification of the interface that blocks the current.





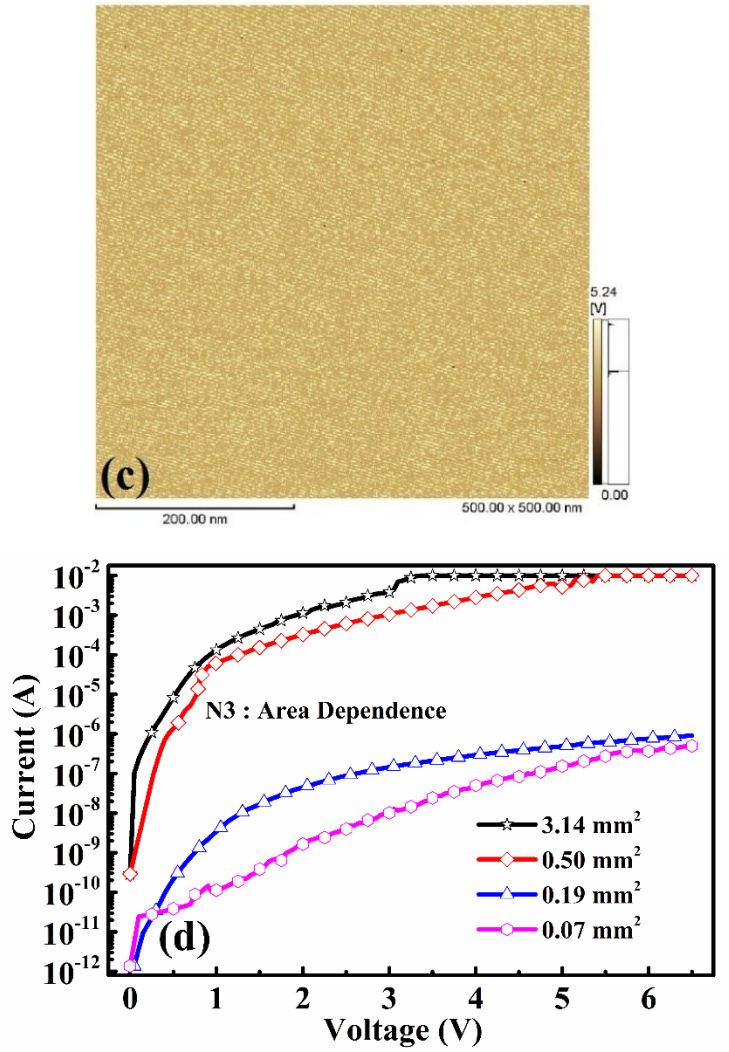


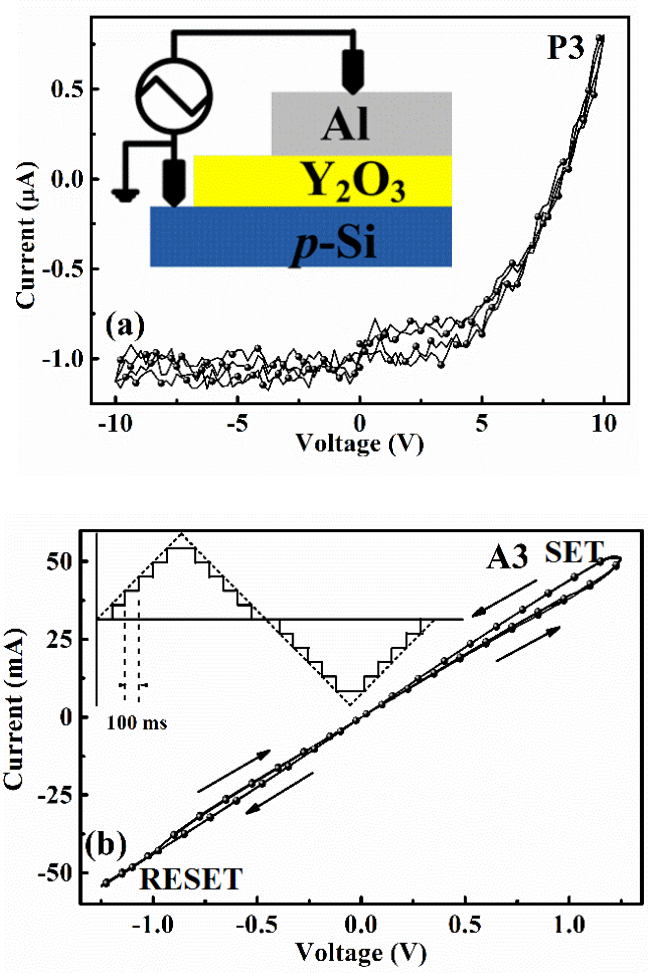
Figure 5.2: I-V characteristics of (a) N3. The inset in the figure shows the effect of sweep rate (1.042 V/s, 2.084 V/s) on the loop area. Current distribution (500×500 nm^2) map of the surface of N3 under (b) + 10 V bias and (c) -10 V bias. (d) Area dependence of current in N3.

This interface usually happens to be the switching interface between the metal electrode and the oxide. In general, it is observed that interface-type RS takes place in the cells which display rectifying I-V characteristics. It is assumed that the Schottky-like barrier plays a vital role in the occurrence of RS [3]–[5]. It appears that the Schottky interface between Al (top electrode) and Y_2O_3 [6] in N3 may be responsible for switching behavior (first quadrant), as another contact between yttria and *n*-Si forms is ohmic in nature. The current flowing through any Schottky interface should be proportional to the area of the interface [2]. The effect of this Schottky

interface on N3 can also be confirmed by figure 5.2(d), which shows that current in the N3 device depends on the area of top electrode.

5.3 Effect of Schottky Interface

In order to further understand the effect of the interface, Devices P3 (Al/Y_2O_3/***p*-Si**) and A3 (Al/Y_2O_3/**Al**) are fabricated with different bottom electrodes (BE) with respect to N3 (Al/Y_2O_3/***n*-Si**). N3, P3, and A3 have *n*-Si, *p*-Si, and Al as their bottom electrode, respectively. It is important to note that N3 has one Schottky interface between Al and Y_2O_3 [6], while A3 has two Schottky interfaces between Al and Y_2O_3.



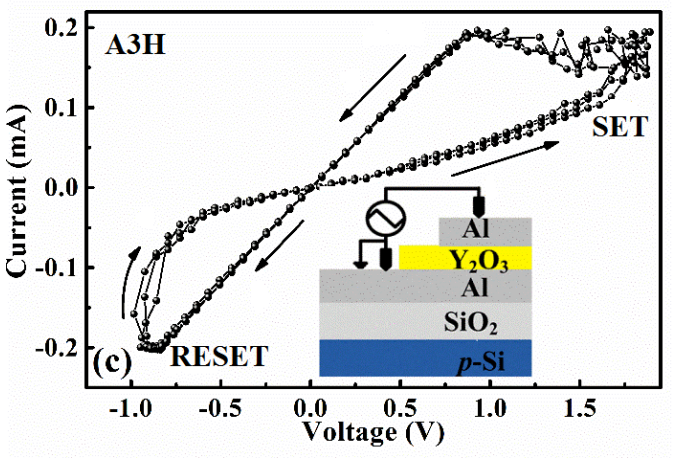


Figure 5.3: I-V characteristics of (a) P3 (b) A3 (c) A3H. The inset in figure (a) shows the device structure of P3. The inset in figure (b) shows the schematic of the corresponding applied triangular excitation. Inset in figure (c) shows the structure of A3H.

P3 (figure 5.3(a)) shows diode-like characteristics after forming. This characteristic may be originated due to *p*-*n* heterojunction between *p*-Si and *n*-yttria. However, no RS is shown by P3, which makes this device useless for our study. Device A3 (figure 5.3(b)) shows bipolar switching. The juxtaposition between N3 (Unipolar, figure 5.2(a)) and A3 (Bipolar, figure 5.3(b)) unmistakably suggests that the transformation from unipolar to bipolar RS is possible. This transformation can be achieved via moving from single Schottky junction (N3) to dual Schottky junctions (A3) based RS device. We have observed that the change in BE from *n*-Si (N3) to *p*-Si (P3) or Al (A3) can cause large changes in the shape and slope of I-V characteristics.

The resistance ratio of the A3 device is meager, so in order to increase the resistance ratio of A3, A3H is fabricated with half of the dimensions of A3. The overall current in A3H (figure 5.3(c)) decreases, and the resistance ratio increases with respect to A3.

The thickness of A3H is halved with respect to A3 because the memristance (state-dependent resistance [9]) of devices improves with a decrease in thickness of the device [9], [10]. In order to reduce the power consumption

of our device, we have reduced the area of the device as current in our device is proportional to the area of the top electrode of our device [3].

In general, as-grown oxide cells are highly insulating and do not exhibit RS. To create RS devices, electroforming (equivalent to a soft dielectric breakdown) is required by applying a large external bias in a controlled manner. This dielectric breakdown supplies thermal energy to the ions in an oxide cell [7]. This process typically results in the generation of oxygen vacancies, creating conducting filaments inside the oxide cells [7]. The occurrence of forming and its extent (measured by the increase in conductivity) depends on the insulator, on the electrodes, on the temperature and atmosphere during forming [8]. If RS is known to take place near a metal–oxide interface than the forming process does not seem to be required at first sight [1]. Indeed, Studies have reported that forming process is not necessary for some oxide thin films [3]–[9]. These cases are similar to our yttria based devices (N3, A3 and A3H) as RS in our devices originate due to interfacial phenomenon.

5.4 Mechanism of Dual Schottky Interface

In general, the Schottky interface plays a vital role in the existence of RS [3]–[5] in some devices, which consist of cells with rectifying I-V characteristics. We have used a Schottky barrier diode (SBD) model [3] to explain the behavior of our RS device. Here it is important to note that the SBD model captures only the main process of devices; however, the electrical transport mechanism is much more complicated in a real device.

Moreover, device A3H can be viewed as two SBDs connected serially in a back-to-back manner. The thermionic emission model [11] can be used to define the I-V characteristics in a single SBD. However, the Schottky barrier height in the thermionic emission (TE) model should be adjusted (decreased) due to the image force lowering (IFL) effect [3], [12], [13]. This reduction in Schottky barrier height ($q\Delta\emptyset_r$) due to IFL is given as follows:

$$q\Delta\emptyset_r = \begin{bmatrix} q\Delta\emptyset_{inital} = \frac{1}{4}\left[\frac{2q^7 N_D(\emptyset_r - V_r)}{\pi^2\epsilon^3}\right]^{1/4} & (-V_r < V_{th}) \\ q\Delta\emptyset_{threshold} = \left[\frac{2q^3 N_D(\emptyset_r - V_r)}{\epsilon}\right]^{1/2} * d_{th} & (-V_r > V_{th}) \end{bmatrix} \quad (1)$$

I_f and I_r, which flow through any SBD, can be given by equation (2) after incorporating the IFL effect into the thermionic emission model [3]:

$$I_f = A_E A^* T^2 exp\left(\frac{-q\emptyset_f}{k_B T}\right)\left[exp\left(\frac{-qV_f}{\alpha k_B T}\right) - 1\right]$$
$$I_r = -A_E A^* T^2 exp\left(\frac{-q\emptyset_r + q\Delta\emptyset_r}{k_B T}\right) \quad (2)$$

Table 5.1 describes the parameter used in equations 1 and 2. A3H has $I = I_f = -I_r$ and $V = V_f - V_r$. Here V is the voltage applied to the device, and I is the current through it.

Table 5.1 Description of parameters used in equation 1 and 2

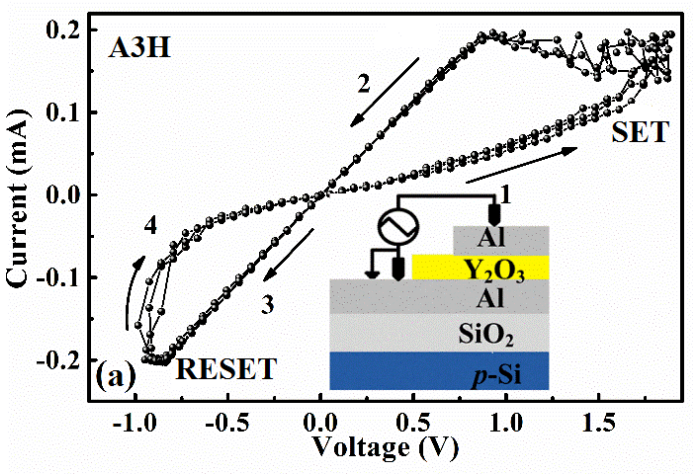
Parameters	Discription
V_r	Reverse bias voltage in SBD
N_D	Electron density near Fermi level
ϵ	Dielectric constant of the semiconductor
V_{th}	Reverse bias threshold voltage at which electrons can tunnel through Schottky barrier
d_{th}	Thickness of Schottky barrier at V>V_{th}
I_f	Forward current
I_r	Reverse current
V_f	Forward bias voltage
I	Total current
A_E	Area of the electrode
$q\emptyset_f$	Barrier height at V_f
$q\emptyset_r$	Barrier height at V_r
α	Ideality factor
q	Charge
T	Temperature
V	Applied voltage

The value of current, which is passing through the device, can be approximated by modifying equation (2) and given in table 5.2. The procedure of modification of equation (2) and finding transform coefficient (a and b) is described elsewhere [3].

Table 5.2 Current flow through double SBD device under different voltage ranges

Voltage range	Current	a	b
Low Voltage Range $V_f \ll V \approx -V_r < V_{th}$ $0 < V \leq 0.39$ IFL effect dominates in due to reverse bias.	$\ln(I) = a(\emptyset_r + V)^{1/4} + b$	$\frac{1}{4k_BT}\left[\frac{2q^7N_D}{\pi^2\epsilon^3}\right]^{1/4}$	$\ln(A_E A^* T^2 - \frac{q\emptyset_r}{k_BT})$
Middle Voltage Range $V_f \ll V \approx -V_r > V_{th}$ $0.39 \leq V \leq 1.09$ Tunneling current of reverse biased SBD	$\ln(I) = a(\emptyset_r + V)^{1/2} + b$	$\frac{d_{th}}{k_BT}\left[\frac{2q^3N_D}{\epsilon}\right]^{1/2}$	$\ln(A_E A^* T^2 - \frac{q\emptyset_r}{k_BT})$
High Voltage Range $V_f \ll V \approx -V_r > V_{th}$ $1.09 \leq V \leq 1.65$ Forward biased SBD controls the current	$\ln(I) = aV + b$	$\frac{q}{\alpha k_BT}$	$\ln(A_E A^* T^2 - \frac{q\emptyset_f}{k_BT})$

We have divided I-V characterticits of A3H (Figure 5.4 (a)) into four segments 1, 2, 3, and 4. We have observed a linear relationship of $ln(I)$ with $V^{1/4}$, $V^{1/2}$, and V in the ranges of V≤ 0.39 (figure 5.4(b)), 0.39 ≤ V≤ 1.09 (figure 5.4(c)), and 1.09 ≤V≤ 1.65 V (figure 5.4(d)) for segment 1 and 2. A similar analysis can be applied for segments 3 and 4.



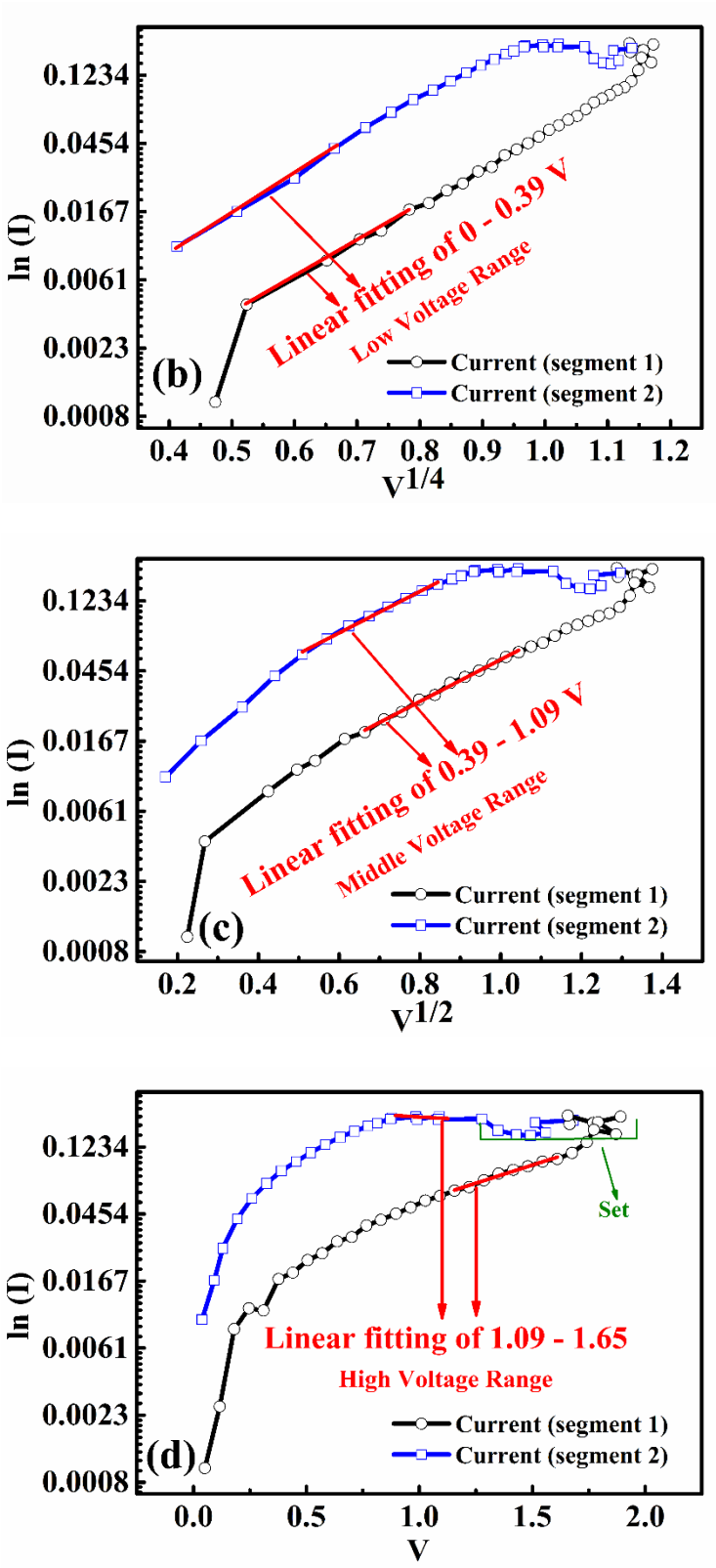
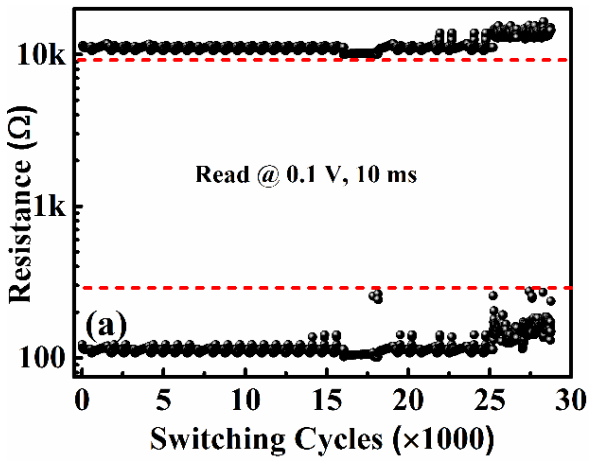


Figure 5.4: (a) I-V characteristics of A3H showing segments 1, 2, 3, and 4. The plots of segments 1 and 2, ln(I) versus (b) $V^{1/4}$ (c) $V^{1/2,}$ (d) V, respectively.

Device A3H presents a significant advantage on the current RRAM cell as it is a forming free and low-cost alternative because of the Al electrode. It is a known fact that forming causes deformation of electrodes [14]. It is noteworthy that devices N3, A3, and A3H do not require a high voltage forming process [15], which avoids the deformation of electrodes in these devices. The memristive systems will be used as memory cells in a crossbar structure [5], which will allow ultra high density for semiconductor memories. The simple structure of our devices simplifies the fabrication process while the DIBS system allows deposition of large number of device on single wafer. This allows a small reduction in cost and in manufacturing time for single unit of device [16].

5.5 Endurance and Retention Measurements

Endurance measurements (figure 5.5(a)) is done at a read voltage of 0.1 V for the A3H devices. These measurements indicate that the A3H is highly reliable and has reproducible RS characteristics. The device does not show significant degradation even after ~29000 switching cycles. Figure 5.5(b) shows the retention characteristics which is measured using a read voltage of 0.1 V.



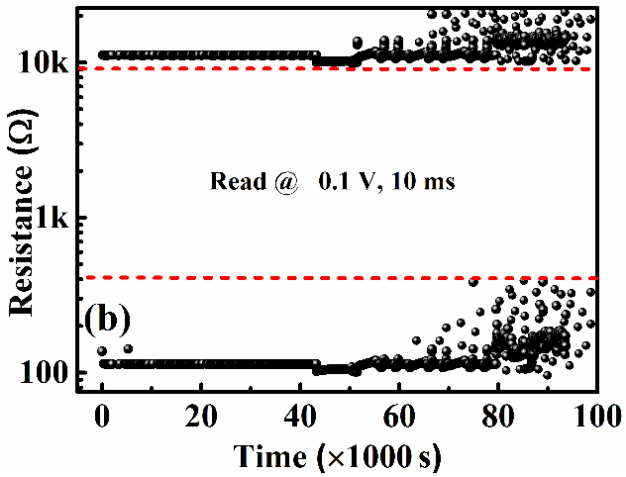
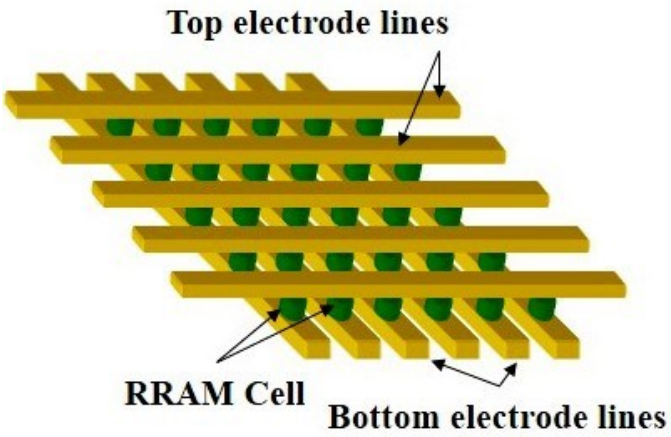


Figure 5.5: (a) Endurance tests of 29000 cycles for resistive switching. (b) Retention test for the 10^5 s. Read bias of 0.1 V for A3H.

5.6 Crossbar Array

A crossbar array (Al/Y_2O_3/Al) is fabricated in order to do a feasibility test of our DIBS grown devices. This study allowed us to understand the limitations of DIBS system weather; it is possible to scale up the system or not. The schematic of a typical crossbar structure is shown in figure 5.6 (a). Figure 5.6 (b) shows the image of yttria based crossbar structure, which is fabricated by the DIBS system. The crossbar is fabricated with the help of multiple metal shadow masks. The area of these rectangular devices varies from 200×500 μm^2 to 300×500 μm^2.



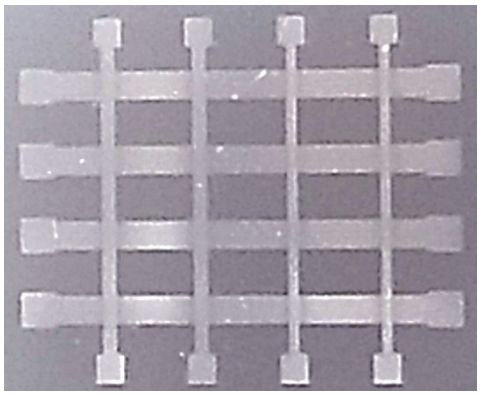
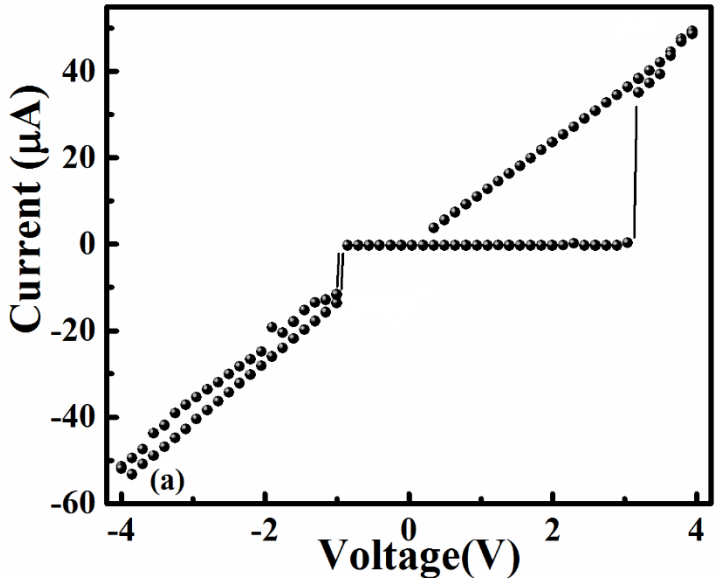


Figure. 5.6: (a) Schematic of a crossbar array. (b) Photographic image of our crossbar array, which is fabricated by DIBS.

Current-Voltage characteristics (figure 5.7 (a)) of these crossbar structure shows hudge reduction in the current (with respect to A3H) due to the smaller area of the top electrode. The value of resistance also improves up to ~300. However, high variability in the SET and RESET voltages can be observed in figure 5.7 (b).



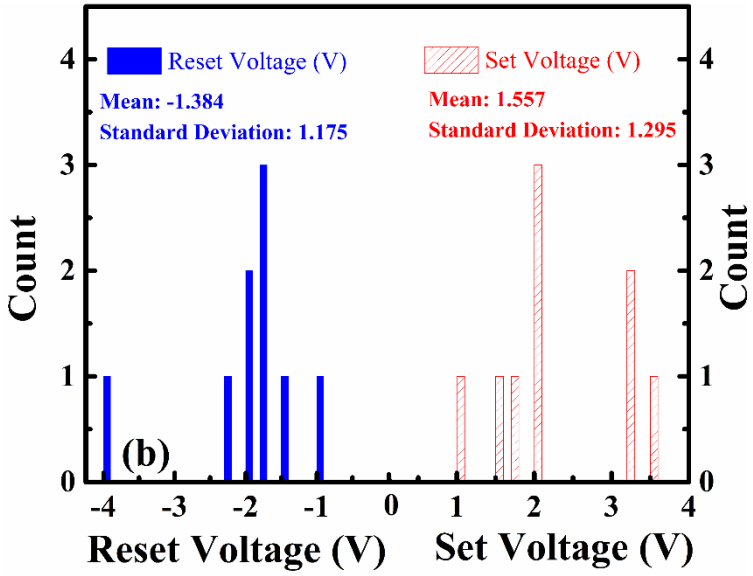


Figure 5.7: (a) Current-Voltage characteristics of one of the devices in the crossbar array. (b) Histogram of the 'SET' and 'RESET' voltages of different devices present in the crossbar array.

5.7 Conclusion

In conclusion, the Schottky interface between Al and yttria plays a vital role in the transformation from unipolar to bipolar characteristics. This transformation can be achieved by changing the BE from *n*-Si (N3) to Al (A3, A3H), i.e. moving from a single Schottky interface to a dual Schottky interface. These findings may be useful to advance research in double barrier memristive systems.

5.8 References

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Chapter 6

Synaptic Learning and Memory Functions in Yttria based Memristive System

6.1 Introduction

Synapses play a vital role in learning and memory, and it is considered as one of the underlying cellular units of a biological neural network [1], [2]. Figure 6.1 shows the chemical transmission of a nerve impulse at the synapse. Electrically, a synapse can be considered as a two-terminal device, and the synaptic weight can be dynamically altered using consecutive pulse excitations [3]. Imitation of the synaptic working will be a significant milestone toward the realization of hardwired artificial neural networks. It is proposed that memristors can emulate the synapse because both (memristors and synapse) have similar transmission characteristics [4]–[6]. In 2011, Chua [7] extended the theory of memristors to incorporate RRAMs. It is complicated to achieve a perfect equivalent of the natural synapse via a single electric device.

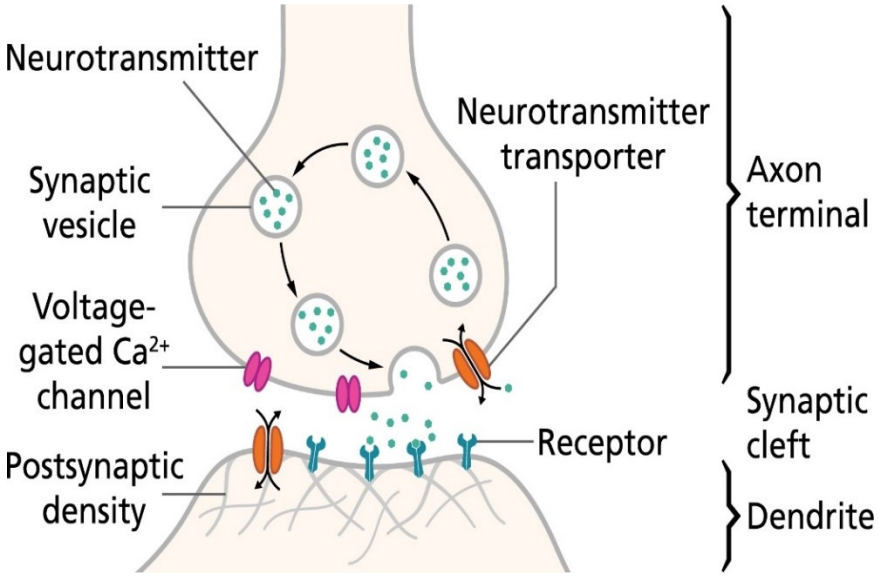


Figure 6.1: Chemical transmission of a nerve impulse at the synapse. Credit: https://qbi.uq.edu.au/brainbasics/brain/brainphysiology/action-potentials-and-synapses , University of Queensland, at 13 October 2019.

However, it is shown that some synaptic functions such as non-linear

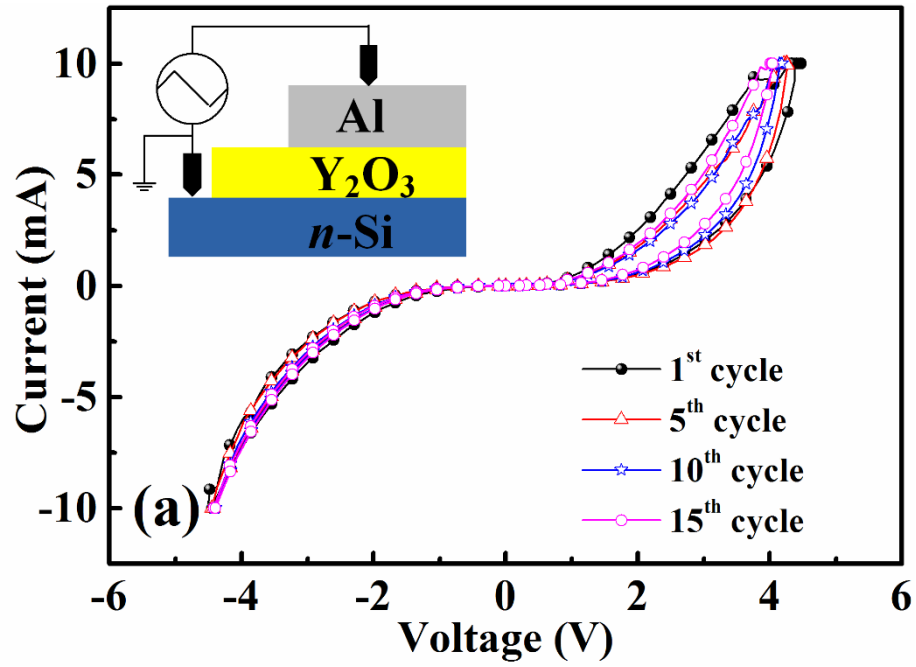
transmission characteristics, spike-timing-dependent plasticity (STDP), long-term potentiation (LTP), short-term plasticity (STP) and learning behavior (LB) can be achieved using a memristive device [8]–[10].

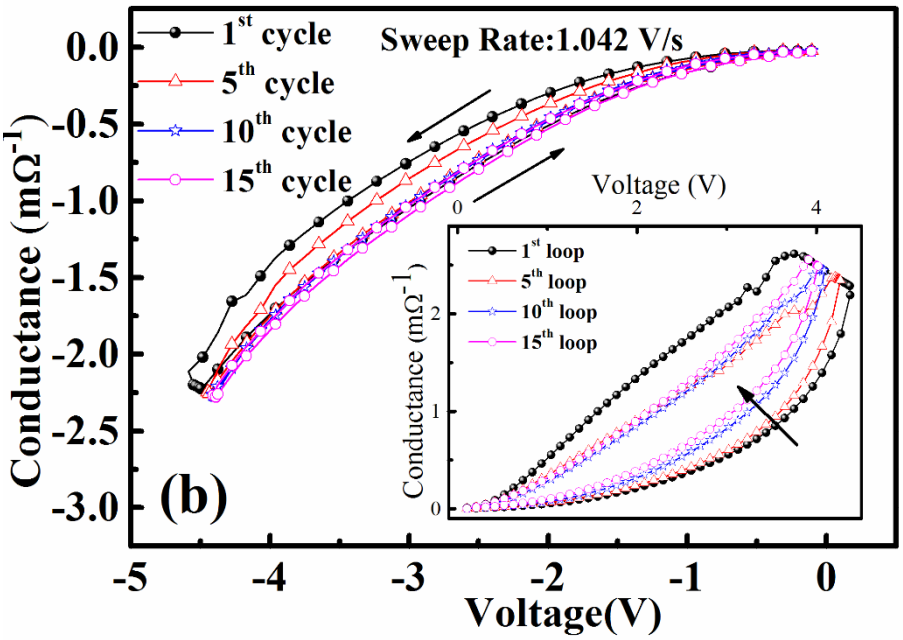
In this chapter, we have explored synaptic functions and learning behavior for a forming-free Al/Y_2O_3/*n*-Si structure grown by the DIBS technique. This device (N3) is grown under the deposition condition, which is discussed in chapter 3 (section 3.2). Metal-insulator-metal (MIM) structures, which show synaptic characteristics, may use one or more insulating layers (TiO_x [11], InGaZnO [8]). These insulator layers are sandwiched between two metal electrodes. As compared to the MIM structure, metal-insulator-semiconductor (MIS) structure such as device N3 provides a low-cost solution by removing the bottom metal electrode, isolation layer, an adhesion layer. Moreover, the flexibility of the amorphous yttria film allows memory devices to be bent into engineered sizes and shapes in practical applications [3].

6.2 Nonlinear Transmission Characteristics

We have observed a nonlinear I-V behavior (figure 6.2 (a)) in our device under a triangular voltage excitation (-5 to 5 V). This nonlinear behavior is one of the essential requirements to mimic the nonlinear behavior of synapses. We have also extracted the variation of device conductance (figure 6.2 (b)) with respect to applied excitation from figure 6.2 (a). Current flows from top to bottom electrode for positive half cycles (0→5 V) and flows in the opposite direction for the negative half cycle (-5→0 V). Figure 6.2 (c) demonstrates the logarithmic plot and linear fitting of the I-V curve for the positive (0→5→0V) and negative voltage (0→-5→0V) sweep regions. We have tested device for various conduction mechanisms such as ohmic conduction ($I \propto V$), space-charge-limited conduction (SCLC, $I \propto V^n$) (n~2) [12], [13], trap-assisted SCLC (TSCLC, $I \propto V^n$, n>2) [12], [13], Schottky emission ($\log(I) \propto V^{0.5}$) [14], and Poole-Frenkel conduction ($\log(I/V) \propto V^{0.5}$) [14]. However, trap-assisted SCLC (TSCLC, $I \propto V^n$, n>2) [12], [13], [15] is found to be the best fit for our device except for initial

low voltage region.





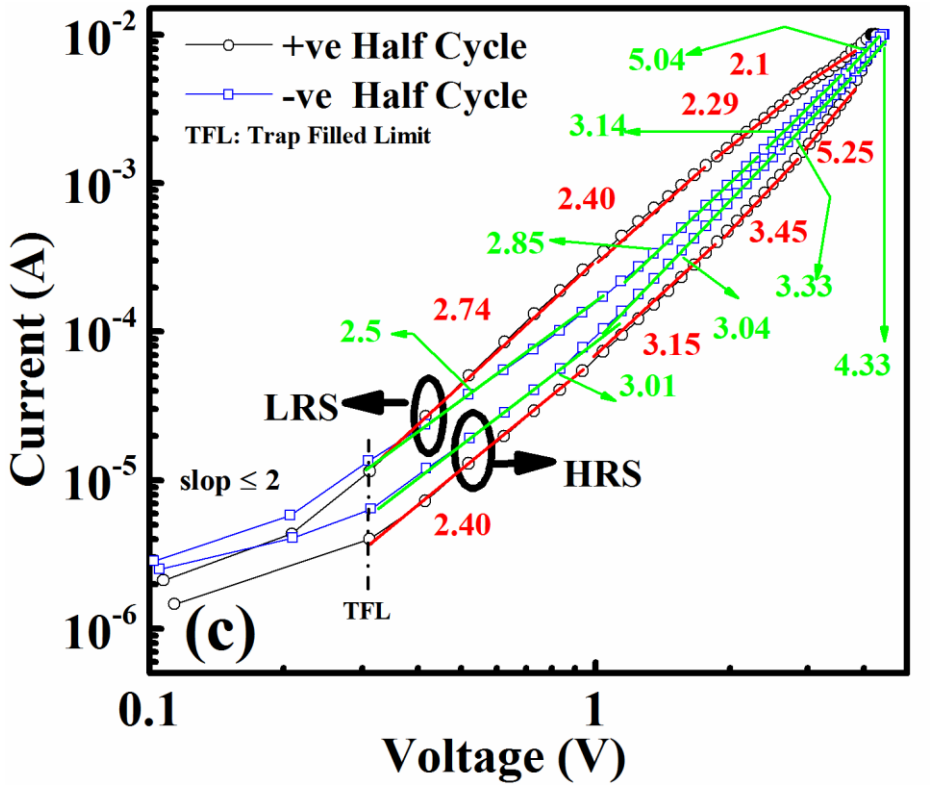


Figure 6.2: The nonlinear transmission characteristics of yttria memristor. (a) I-V characteristics of N3. The bottom inset shows the measurement configuration of N3. (b) Variation of device conductance for the negative half of voltage cycles. The inset shows the variation of conductance for the positive half of same voltage cycles. (c)Logarithmic plot and linear fitting of the I−V curve. Numbers represent slope of fitted lines for positive half cycle and negative half cycle in green and red color, respectively.

The low voltage region, where the slope is less than equal to 2, is called the trap-filled limit (TFL). The slope in this region depends on the total traps density and thickness of the sample, not on the distribution of traps [16], [17]. The current in our device is affected by shallow traps (slope >2), according to the low-exponent SCLC [14], [18].

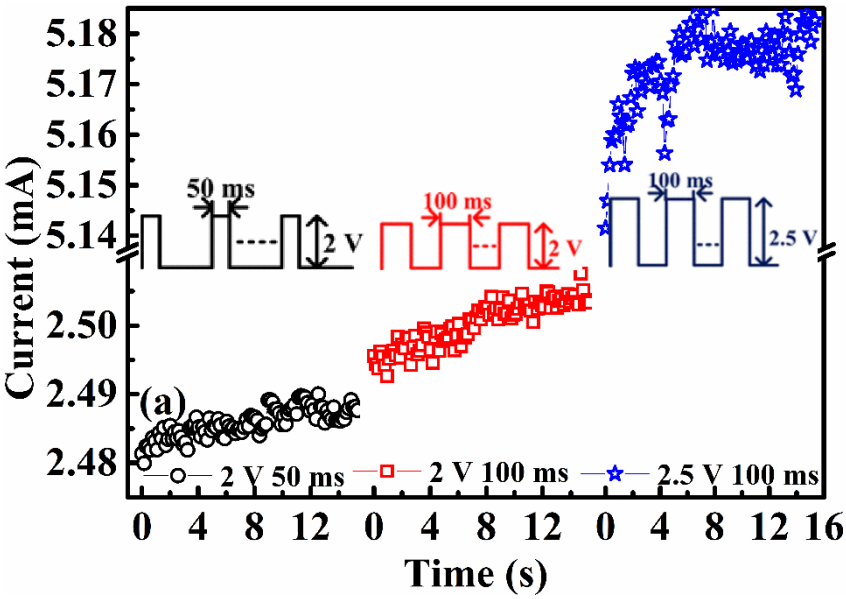
6.3 Synaptic Learning and Memory Functions

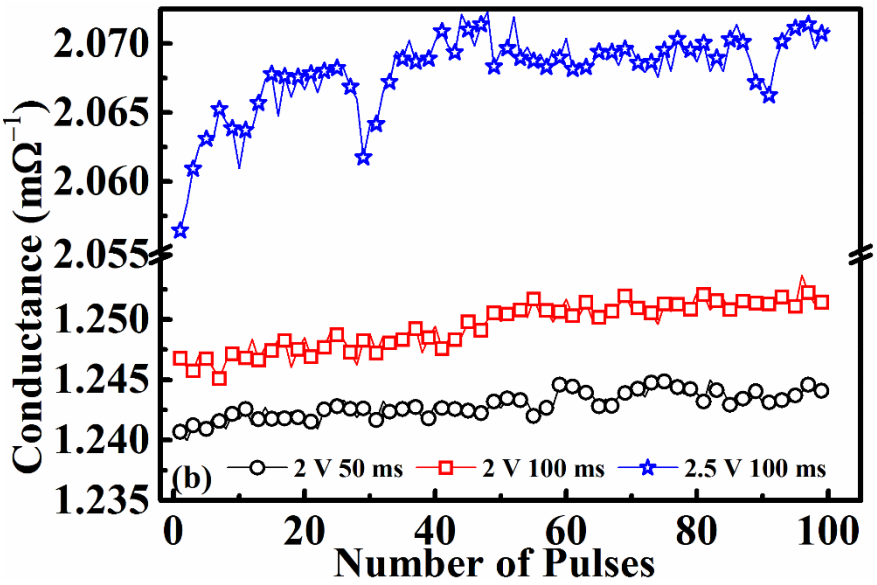
Synaptic behavior is heavily affected by stimulus intensity, sequence, and duration of the stimulus. Some memristor models suggest that the conductivity of memristive system can be tuned by duration, and sequence

of the applied excitation[19], [20]. We have studied the current response and change of conductance in our device by varying the different parameters of applied external stimulus. Here, it is important to note that we have treated device conductivity as synaptic weight in order to establish the equivalence with the synaptic behavior. We have applied three different kinds of pulse excitation with varying amplitudes and durations.

1. Pulse 'on time' variations: 2 V, 50 ms, and 2 V, 100 ms.
2. Pulse amplitude variations: 2V, 100ms and 2.5V, 100ms.

Figure 6.3 (a) shows the current response of the device when subjected to the above stimuli. Figure 6.3 (b) shows the conductivity variation of our device when it is subjected to the above pulse excitations. It is observed that a more significant change in the current and conductivity occurs when pulses of higher-amplitude and longer-duration are applied to our devices. Similar results have been obtained in amorphous InGaZnO based devices [8].





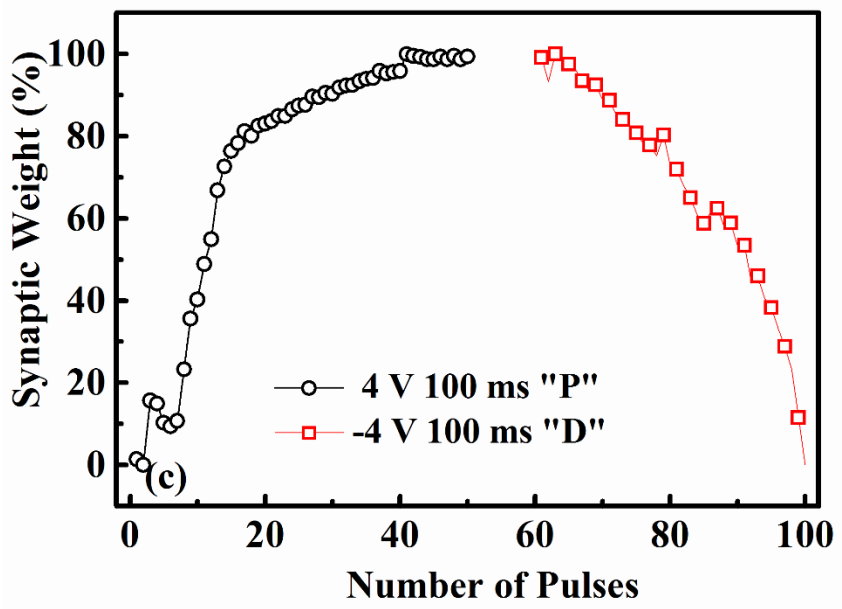


Figure 6.3: (a) Current with respect to applied voltage pulses of different amplitudes and time-durations. (b) Conductance with respect to applied voltage pulses of different amplitudes and time-durations. (c) Change in synaptic weight (device conductivity) under the influence of consecutive potentiating or depressing pulses.

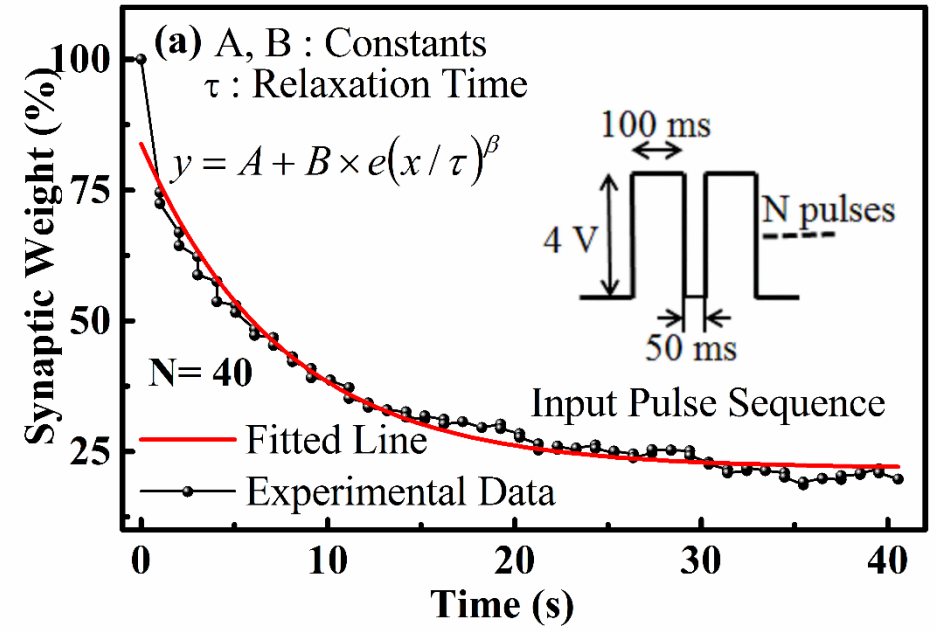
Some synapses show an excitatory and inhibitory response, which depends on the sequence of synaptic input pulses. To study the excitatory and inhibitory response of our device, we have applied the positive voltage and negative voltage pulses respectively. It is important to note that pulses of +4 V (-4 V) are applied to study excitatory (inhibitory) response with 'ON

time' of 100 ms. Firstly, device is subjected to a series of 50 positive/potentiating voltage pulses ("P process"), which is immediately followed by 40 negative/depressing pulses ("D process"). We can observe that conductivity of our device (figure 6.3 (c)) increases (decreases) by applying consecutive potentiating (depressing) voltage pulses. Such potentiation/depression of synaptic weight (device conductivity) through repeated voltage stimuli with varied pulse duration plays vital role in modulation of synaptic plasticity, which is similar to biological systems [3]. Similar modification of synaptic plasticity has been achieved in cultured hippocampal neurons of rats [1].

6.4 Transition in Synaptic Plasticity

Synaptic plasticity is one of the essential foundations of learning and memory. It is characterized by immensely inter-connected networks of synapses in the brain. There are two types of synaptic plasticity which are classified on the basis of memory retention [20]:

1. Long-term potentiation (LTP)
2. Short-term plasticity (STP)



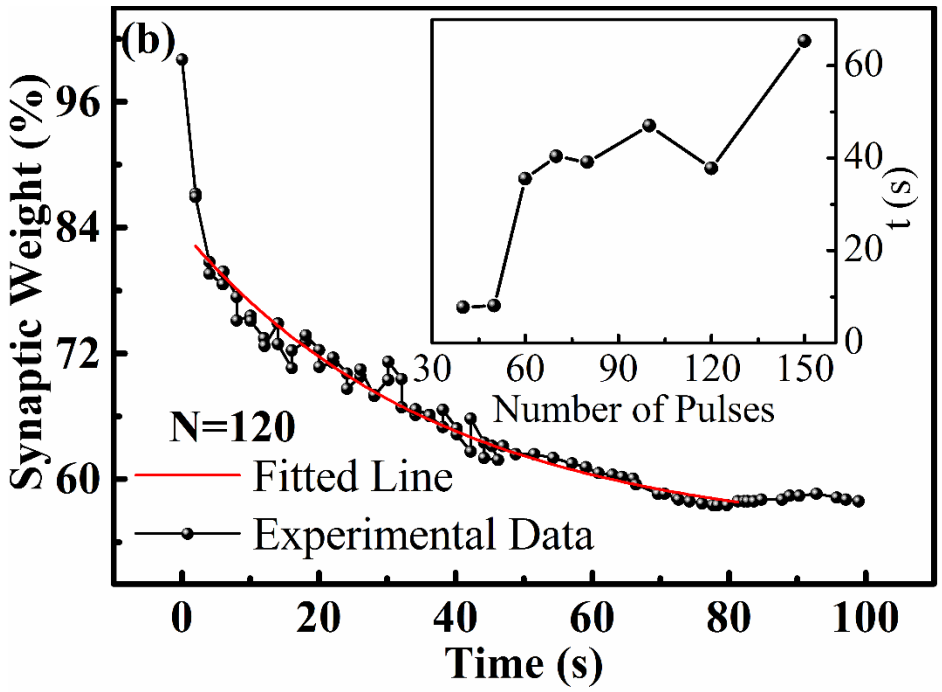


Figure 6.4: Repeated-stimulation-induced STP-to-LTP transition. Curves are obtained by stimulating the device using different numbers of input pulses, and reading pulse (amplitude 0.1 V, duration 10 ms) is applied just after the last stimulus. (a) Synaptic weight (SW) decay curve recorded after 40 identical pulses (shown by "N") and fitted curve according to the equation given in the inset. The inset shows the input pulse sequence. (b) SW decay curves recorded after N = 120 identical pulses, with inset showing the variation of relaxation time (τ) with the number of stimulation pulses, where τ is obtained from memory decay curves by fitting data.

These temporal characteristics are not isolated but inter-related to each other. STP is realized by temporal augmentation of a synaptic weight, which then rapidly decays to its original state. However, repetitive stimulation causes a permanent change in the connection to achieve LTP; shorter repetition intervals enable efficient LTP formation from fewer stimuli [20].

We have studied the STP to LTP transition by exposing our device to different numbers of stimulation pulses (but the same type). Precise mathematical function of memory loss which is shown in figure 6.4 (a) and 6.4 (b)) is still controversial [8], [18], [21]. We have used a modified stretched-exponential function $\boldsymbol{y = A + B \times exp^{(-x/\tau)^{\beta}}}$ to describe the

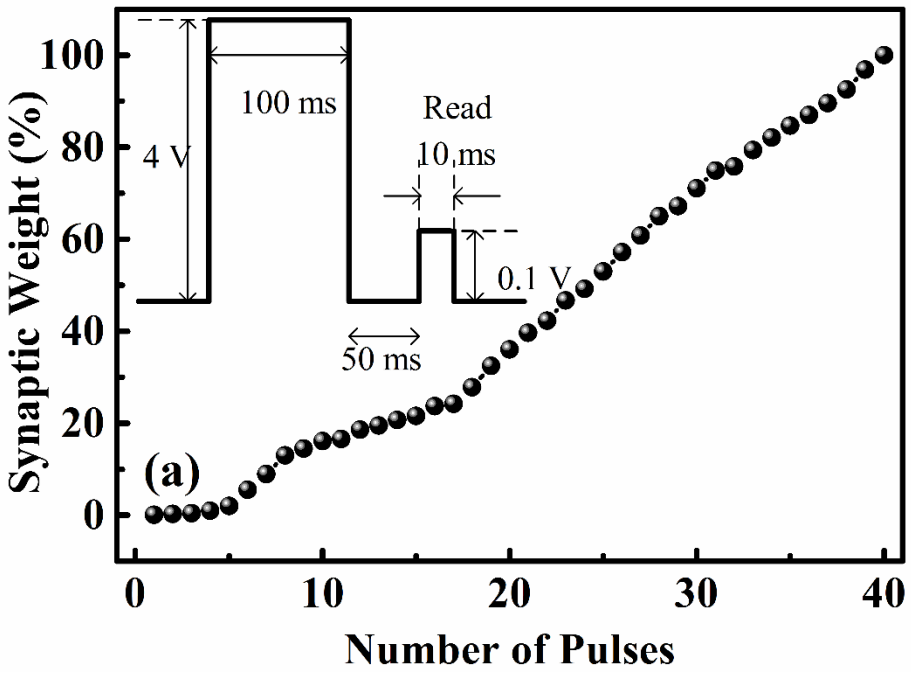
relaxation process of STP [18]. Constants of decay A and B depends on initial and on the final condition of the device, respectively. β is the stretch index ranging between 0 and 1. Relaxation time (τ) represents the decay rate after excitation is removed, and it is a constant for a given curve. Decay curves ((τ ~ 7.38 s) and (τ ~ 37.78 s)) for 40,120 stimulation pulses are shown in figure 6.4 (a) and 6.4 (b). Inset of figure 6.4 (b) shows that the relaxation time increases in proportion with the number of input pulses increase, which indicates a decreasing forgetting rate. This phenomenon can be considered as a signature of the STP-to-LTP transition, which is achieved due to repeated stimulations [8] [21], [20].

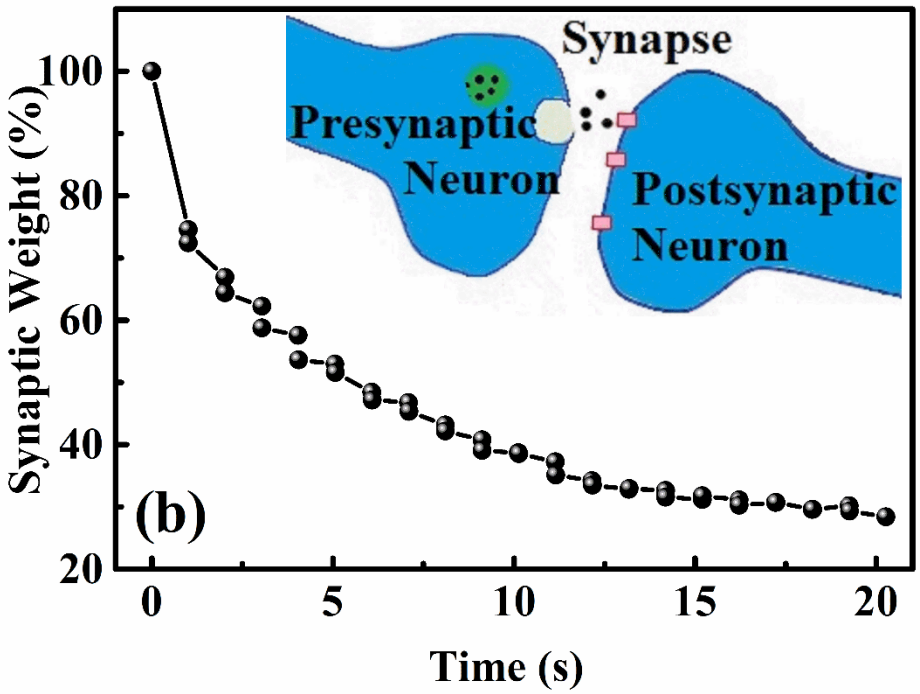
Sturman [22] has shown that the stretched exponential decay law (Kohlrausch law [23]),$\boldsymbol{B} \times \boldsymbol{exp}^{(-x/\tau)^{\beta}}$, originates from the simple and general geometric features of a random distribution of transport and trapping sites in the 3D space. The value of the variable stretching index β is determined by the localization radius of hopping electrons. One of the most known findings of this kind is the model of hierarchically constrained dynamics which implies triggering of slower relaxation processes after completion of faster ones [22]. The stretched exponential behavior originates from the wide distribution of activation energies and the associated wide range of relaxation times among different relaxation processes in a disordered system [21]. Thus, τ and β jointly account for the collective behavior of all possible relaxation processes for oxygen vacancis in the memristive system [21] after the application of faster input excitations.

6.5 Learning Behavior

We have studied the learning behavior (LB) in our device by using the procedure, which is described in this section. Figure 6.5 (a) shows that the synaptic weight (conductivity) of the device increases progressively with the number of pulses (the device is stimulated with 40 pulses). We have connected the device similar to a synapse between pre-synaptic and post-synaptic neurons (inset of figure 6.5 (b)) and used pulse excitation.

Repeated electrical activities can induce a persistent increase in synaptic efficacy in various parts of the nervous system [1].





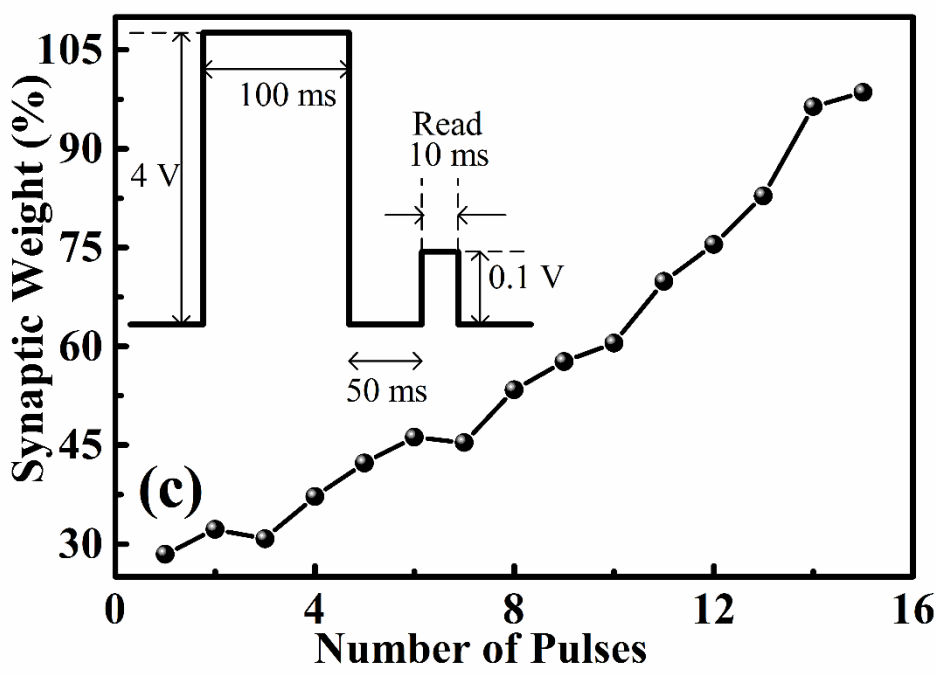


Figure 6.5: The "learning-behavior" of our device. (a) Increase in the synaptic weight with consecutive voltage pulse stimuli. The inset shows the input pulse sequence. (b) The relaxation process of STP with respect to time, and this is analogous to the human memory "forgetting process." Inset shows a schematic illustration of synapses. (c) The re-stimulation process shown by applying consecutive pulses after 22 s. The inset shows the input pulse sequence.

It is interesting to observe that a spontaneous decay happens in synaptic weight when the pulse excitation is removed ((figure 6.5 (b)). Initially, the synaptic weight of the device decays very rapidly than it gradually slows down. Twenty-second after the removal of pulse excitation, synaptic weight stabilizes at ~28% of its initial value. Such a variation trend is consistent with the "forgetting (or retention) curve" of human memory [8], [21]. When we perform re-stimulation process from previous state, it takes only 15 pulses to recover to ~100% of synaptic weight, as represented in figure 6.5 (c). This is relatively less than the number of pulses (40) required in the first learning process (figure 6.5 (a)). This complete process bears a striking similarity with the LB of synaptic systems. This LB allows re-learning of the forgotten information at a much faster rate. The above phenomenon, along with following observations cannot be fully understood

by the classic memristor model. Oxygen ions and vacancies play a significant part in the synaptic behavior of RRAMs [8], [11], [21]. An oxygen vacancy is a point defect, which is an object in thermodynamic equilibrium [24]. In other words, oxygen vacancies should always exist in any oxide at a finite temperature due to entropic disorder [24]. Amorphous yttria has oxygen ions and vacancies in large numbers [25]. These oxygen vacancies change the ionic charges of oxygen and yttrium in yttria lattice [26]. Such alterations lead to deviation in bond-length and bond-angle, which leads to unstable local structural disorders in amorphous yttrium oxide. A small amount of energy is required to destroy these unstable local structures and make oxygen ions to re-migrate [9], which may lead to the observation of such "learning behavior" in our memristor device.

6.6 Advantage of Yttria based Devices

Table 6.1 provides a comparative analysis of different deposition techniques that are deployed to fabricate a synaptic memory cell with different switching materials. Our device uses Al top contact and *n*-Si as bottom contact. Al and *n*-Si have lower cost as compared to Pt [11], [27], [8], Ti [8], [14], W [11], [21], TiW [9], Pd [21], [28] contacts. MIS structures, which are based on Si contact, allow easy integration of memristive systems with present Si-based semiconductor technology. Moreover, nearly all devices, which are shown in table 6.1, use multiple deposition techniques for different layers, whereas in our case, every layer (switching layer and metal electrode) of the device is deposited by a single deposition technique, *i.e.,* DIBS. The high voltage forming process [29] is not required in our pristine device to make it conducting due to abundant oxygen vacancies pre-existing in the yttria film. A forming-free cell as compared to a forming-necessary cell shows more stable resistive switching (RS) characteristics and also avoids destruction of electrodes [30].

RRAMs, which are based on Pt [8], [11], [27] electrodes generally suffer from switching degradation [31] and deformation of the junction due to the oxygen bubble formation at metal/semiconductor contact [31]. $Ge_2Sb_2Te_5$

(GST) is one of the most used material for high-speed phase-change memory (PCM) applications [10]. However, chalcogenide glass, such as GST has some drawbacks: (1) Te element is harmful to semiconductor techniques due to its volatilization and toxicity [32]. (2) chalcogenide glass also suffers from problems of thermal stability [32]. Amorphous InGaZnO [8] suffers from degradation under pulsed voltage stresses, which will be the primary mode of operation in synaptic RRAMs [33]. There are no such problems of volatilization, toxicity, thermal instability, and pulsed voltage stress with yttria based memristive device. LB, STP to LTP transitions, and relaxation processes of STP are shown by our device, whereas some of such behaviors have not been reported for HfO [34], ZnO [14], TiO_2 [11] and WO_x [28] based devices. Devices based on ZnO nanowires (NWs) [14] have a thickness in the order of μm, which makes it unsuitable for thin-film applications.

Table 6.1 Comparative analysis of different RS devices

Device structure	**Thickness (nm)**	**Temperature (˚C)**	**Reference**
Pt/Al/TiO_{2-x}/TiO_y/W	50 (TiO_{2-x}) 6 (TiO_y)	250 400 RT	[11]
Pt/Atomic Bridge (Ag)/Ag_2S/Ag	-	150	[27]
Pt/InGaZnO_{1-x} /InGaZnO_x/Pt/Ti/SiO_2/Si	80	RT	[8]
TiW/$Ge_2Sb_2Te_5$/TiW/SiO_2 /Si	150	200	[10]
Ti/ZnO-NWs/ZnO-seed-layer/p+-Si	2000 (NWs)+ 30 (seed-layer)	RT 90 RT	[14]
Pd/WO_x/W/SiO_2/Si	WO_x (50)+ W (60)	RT 400	[28]
TiN/HfO/Pt/Ti/SiO_2/Si	20	RT	[34]

		RT 600	
Al/Y_2O_3/*n*-Si	**80**	**300**	**Our work**

The simplicity of our MIS structure (Al/Y_2O_3/*n*-Si) is noteworthy with respect to other synaptic devices. Most devices use multiple switching layers [11], [27], [8],[14],[21], whereas our devices use one switching later, which means overall less time is required for manufacturing of the single-unit device. Our devices present a significant advantage on the current RRAM cell as it is a forming free and low-cost alternative because of Al electrode. It is a known fact that forming causes deformation of electrodes [30]. It is noteworthy that all of our devices (N3, A3, and A3H) do not require high voltage forming process [29] which avoids deformation of electrodes in these devices. The memristive systems will be used as memory cells in a crossbar structure [35], which will allow ultra high density for semiconductor memories. The simple structure of our devices simplifies the fabrication process while the DIBS system allows deposition of large number of device on single wafer. This allows a small reduction in cost and in manufacturing time for single unit of device [36].

6.7 Conclusion

In conclusion, some important synaptic functions, resembling learning/memory functions of biological systems, have been demonstrated in the amorphous yttria-based memristor fabricated by DIBS system, for the first time in the literature. It includes nonlinear transmission, LTP, STP, and STP to LTP transition. The interesting "learning behavior" characteristic, which is considered to be related to the unstable local structure in amorphous yttria, is also observed. The synaptic functions and plasticity are very complex in biological systems and require more detailed considerations of some other factors, such as device structure, the selection of material, and other dynamic mechanisms. We believe our work will be very useful for further research on neuromorphic computing to understand mechanisms and phenomena related to transmitting information in

neuroscience for the more precise realization of the synapse for an artificial neural network.

6.8 References

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Chapter 7

Conclusion and Future Scope

Semiconductor memories are an essential part of computing. Different computing systems require different abilities in the semiconductor memory according to desired applications. We need to find an optimum solution for our specific requirements. A new type of non-volatile memories (NVMs) are discovered during the last decade; these memories can be used as a synapse, which can allow mankind to build computers based on the brain. Many of these devices appear to be two-terminal devices with resistive switching capabilities, i.e., their resistance can be changed, and the devices can remember the new resistance. Such devices are called RRAM and may be considered as a subset of memristive systems. Memristor acts like tiny analog memories, and it is formed at the junctions of crossing electrodes separated by an appropriate material. RRAM promises to be a high-density, low-power consumption, low-cost, and fast-switching memories. However, it is quite early to say that it will be able to completely replace the current memory technology.

In this work, we have explored the yttria based RRAMs, which are fabricated by the DIBS system. DIBS system is noteworthy since it produces high-quality thin films with reasonably better compositional stoichiometry, small surface roughness and good adhesion to the substrate even for films grown at room temperature (RT). After the fabrication of devices, we have performed several experiments on devices such as current-voltage measurement, FESEM, TEM, XRD, and C-AFM. These experiments helped us to understand the mechanism and behavior of the device. We have also designed the experiment to understand the effect of the Schottky interface on the memristive device. We have achieved very good repeatable (~90 % , device to device) results in terms of endurance testing, but devices still show a very low (device to device) repeatability (~ 10 %) in retention characteristics. The yield of the device has been excellent

(~90%) with Si wafer bottom electrode, but as soon as we moved to metal (Al) bottom electrode, the yield dropped to a much lower percentage (~20 %). We did get some improvement after decreasing the thickness of Al bottom electrode; yield is improved by ~10 %. However, the Al bottom electrode yield does not move beyond ~30 %.

To the best of the author's knowledge, the fabrication of yttria based resistive memory device by DIBS system has not been reported to date. Therefore, the study of the switching characteristics of yttria and corresponding relation with electrical, optical, elemental, and structural properties is quite significant, when one seeks to realize yttria-based RRAM.

7.1 Conclusions

The primary outcomes of this thesis are summarized as follows:

1. The highly crystalline devices of yttria thin-film do not show any RS, whereas amorphous or polycrystalline devices show RS. This behavior is observed because of oxygen vacancies, and defects play a critical role in oxide-based RRAM. A highly crystalline yttria layer does not have enough defects to give birth to the RS behavior. Whereas amorphous yttria has a lot of defects that contribute to the oxygen vacancies and create conditions that are helpful in RS behavior.

2. The oxygen partial pressure does not play a significant role in deciding the crystallinity of the yttria thin film layer, whereas deposition temperature plays a critical role in deciding the crystallinity of thin film. Oxygen partial pressure plays very important in deciding the qualitative amount of oxygen vacancies in the thin film. The number of oxygen vacancies has to be optimized in order to maximize the resistance ratio.

3. We have found that the deposition temperature of 300 ºC and Ar:O of 2:3 sccm produce the best RS behavior with the least variability. The low variability in switching characteristics is essential as it eases the design process for other support systems.

4. The Schottky junction between Al and yttria plays a critical role in the shape and size of current-voltage characteristics and controls the polarity of switching behavior. When we move from a single Schottky junction device to a dual Schottky junction device, characteristics also shift from unipolar to bipolar.

5. We have also found that a layer of SiO_2 appears on the silicon wafer if deposition temperature is increased. This inherent amorphous layer of SiO_2 causes increases in the roughness of the yttria layer, which in turn increases the variability in switching voltage.

6. The roughness and lattice mismatch of the bottom electrode or layer play a significant role in the crystallinity of yttria layers, which are deposited on top of this bottom layer.

7. We can also change the ion beam voltage in the DIBS system. Ion beam voltage in a DIBS system is proportional to the kinetic energy of atoms that are bombarded on the substrate for deposition. However, in our case, we find ion beam voltage only affected the speed of the deposition of the film. It does not affect any RS behavior of thin film. However, this should not be generalized for other materials.

8. The thickness of the yttria film and area of the device plays a significant role in the RS behavior of our devices. It has been shown that a decrease in the thickness of yttria film actually improves the resistance ratio. The decrease in the area of electrode results in the decrease in overall current which reduces power consumption of device.

9. Crossbar arrays can be fabricated via the help of a metal shadow mask, but it restricts the top electrode width only up to 200 μm, as our DIBS system setup does not allow thickness to be lesser than 200 μm. We have confirmed this width-limit by testing with a metal shadow mask of an electrode width of up to 100 μm.

10. Some essential synaptic functions, resembling learning/memory functions of biological systems, have been demonstrated in the amorphous

yttria-based memristor. It includes nonlinear transmission, LTP, STP, and STP to LTP transition. The impressive "learning behavior" characteristic, which is considered to be originated due to the unstable local structures present in amorphous yttria, is also observed.

11. Oxygen ions and vacancies play a significant part in the synaptic behavior of RRAMs. Amorphous yttria has these ions and vacancies in large numbers. These oxygen vacancies change the ionic charges of oxygen and yttrium in the lattice of yttria. Such alterations lead to deviation in bond-length and bond-angle, which leads to unstable local structural disorders in amorphous yttrium oxide. A small amount of energy is required to destroy these unstable local structures and make oxygen ions to re-migrate, which may lead to "learning behavior" in our memristor device.

12. We have used a modified stretched-exponential function $\boldsymbol{y = A + B \times exp^{(-x/\tau)^{\beta}}}$ to describe the relaxation process of STP. Relaxation time (τ) represents the decay rate after excitation is removed, and it is a constant for a given curve. Decay curves for 40 ($\tau \sim 7.38$ s) and 120 ($\tau \sim 37.78$ s) stimulation pulses, which shows that the relaxation time increases in proportion with the number of input pulses increase, which indicates a decreasing forgetting rate.

13. The resistive switching in yttrium oxide memristive devices is interfacial. The variation in the electrode area will lead to variability in the different parameters at macroscopic levels. However, the effect of electrode area variation will depend on the type (nature) of the electrode, morphological variations on the interface at the microscopic level. These parameter variations, (set-reset voltage, resistance ratio, etc.), which are happening due to electrode area variations, will depend on inclusion or exclusion of these microscopic sites which produce variability.

7.2 Future Scope

We have realized a forming free high endurance yttrium oxide-based memristive system. The mechanism of this device is affected by the

interface between the oxide layer and electrode. The devices which do not use the smooth Si wafer as their bottom electrode seems to have more variability in current-voltage characteristics. It is observed that the crystallinity of yttria film plays very important role in origin of RS behavior in our device. The problem of variability arises when we move from lower deposition temperature to higher deposition temperatures as it causes to thicken unwanted SiO_2 layer. Another problem that was faced in our crossbar array is 'Sneak-path constraints.' Sneak-path constraints are common problems in crossbar array architecture; in our case, sneak path currents cause premature aging in our device. Future scope of our research is given below:

1. Improvement in the retention of memory cells by doping in Y_2O_3 or using bilayers in the switching layer.

2. Crossbar fabrication of Y_2O_3 based memory cells with the implementation of one selector-one resistor (1S1R) cells to tackle the sneak-path issue in cross-bar configuration.

3. Improvement is required in the roughness of the bottom electrode in order to improve the variability for devices that uses metal bottom electrodes.