

ON-CHIP CIRCUIT DESIGN TECHNIQUES FOR HIGH-SPEED SERIAL LINKS

Ph.D. Thesis

by

Mahesh Kumawat



**DISCIPLINE OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE
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ON-CHIP CIRCUIT DESIGN TECHNIQUES FOR HIGH-SPEED SERIAL LINKS

A THESIS

*thesis submitted in partial fulfillment of the
requirement for the award of the degree*

of

DOCTOR OF PHILOSOPHY

by

Mahesh Kumawat



**DISCIPLINE OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE
DECEMBER 2019**



INDIAN INSTITUTE OF TECHNOLOGY INDORE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **ON-CHIP CIRCUIT DESIGN TECHNIQUES FOR HIGH-SPEED SERIAL LINKS** in the partial fulfillment of the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY** and submitted in the **DISCIPLINE OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from July 2014 to December 2019 under the supervision of Dr. Santosh Kumar Vishvakarma, Associate Professor, Discipline of Electrical Engineering, Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Mahesh
21-Dec-19

Signature of the student with date
(MAHESH KUMAWAT)

This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

Santosh
4/12/19

Signature of Thesis Supervisor with date
(Dr. SANTOSH KUMAR VISHVAKARMA)

MAHESH KUMAWAT has successfully given his/her Ph.D. Oral Examination held on **18-May-2020**.

[Signature]

Signature of Chairperson (OEB)
Date: May 18, 2020

[Signature]

Signature of External Examiner
Date: May 28, 2020

Digitally signed by Dr. Sudeb Dasgupta
DN: cn=Dr. Sudeb Dasgupta, gn=Dr. Sudeb Dasgupta, c=US, United States, | =US, United States, o=IIT Roorkee, ou=ECE, e=sudeb.dasgupta@ece.iitr.ac.in
Reason: I am the author of this document
Location: IIT Roorkee
Date: 2020-05-28 12:33+05:30

[Signature]

Signature of Thesis Supervisor
Date: May 18, 2020

[Signature]
18.05.2020

Signature of PSPC Member #1
Date:

M. Shaikh
18-05-2020

Signature of PSPC Member #2
Date:

[Signature]

Signature of Convener, DPGC
Date: 18-05-2020

[Signature]
18/05/2020
Signature of Head of Discipline
Date:

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Dedicated
to
My Parents

ABSTRACT

Advances in semiconductor manufacturing allow higher degree of integration for application-specific integrated circuits (ASIC). The high transmission bandwidth requires an interface system to match the error-free transmission and communication need. The high speed computing and communication network advancement require scaling of silicon technology for higher number of component integration on small chip area and low power consumption.

Serial Link Transceivers is the crucial element in achieving high data transmission with I/O pin limitations in systems-on-chips (SoCs) and ASIC's. To match this high speed data computing requirements, power consumption and data recovery becomes key aspects. The focus of this thesis is on the circuit design of serial links using different methods of serialization.

A new serial link transceiver design is presented for high-speed synchronous transmission. The design consists of Wave Combining and driving unit at the transmitter end and the Decombiner at the receiver end. Wave combining and driving unit is responsible for combining the different serial data streams, and its driving over the transmission channel respectively. In contrast, a decombiner separates the information according to the clock signal. Continuous-Time Linear Equalizer (CTLE) taps help to limit the jitter tolerance up to 10% of the data received. The other commonly used serial link method is the asynchronous transmission. The asynchronous serial links are independent of a clock. The handshake protocols in asynchronous transmission method ensure valid data transmission. Furthermore, handshaking signals slow down the circuit, so the current mode logic blocks are used for faster transmission of the signal.

To help in asynchronous data serial link communication, an improved Current Mode Logic (CML) latch design is proposed. The Improved CML latch results in a boost in the output voltage swing, the delay model of latch is also proposed, based on the small-signal equivalent circuit analysis for the proposed latch. As an application of CML latch, asynchronous Wave-Pipelined Serial link is proposed. In designing of a serializer and deserializer is built using proposed CML Latch. The CML circuit operates at a higher data rate and low power consumption.

List of Publications

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1. **Mahesh Kumawat**, Abhishek Dalal, Mohit S. Choudhary , Ravi Kumar, Gaurav Singh and S. K. Vishvakarma, “Wave Combining Driver based Serial Data Link Transceiver Design for Multi-Standard Applications,” *Journal of Nanoelectronics and Optoelectronics*, vol 14, no. 5, pp. 675-679 (5) May 2019.
2. **Mahesh Kumawat**, Abhishek Kumar Upadhyay, Sanjay Sharma, Ravi Kumar , Gaurav Singh and S. K. Vishvakarma, “An Improved Current Mode Logic Latch for High-Speed Applications,” *International Journal of Communication System Wiley (Accepted)*
3. **Mahesh Kumawat**, Mohit S. Choudhary, Ravi Kumar , Gaurav Singh and S. K. Vishvakarma, "A Novel CML latch based Wave Pipelined Serial Link Transceiver for Low power application,” *Journal of Circuits, Systems and Computers, World Scientific. (Accepted)*
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LIST OF ABBREVIATIONS

ASIC	:	Application Specific Integrated Circuits
BSIM3v3	:	Berkeley Short-Channel IGFET Model
CML	:	Current Mode Logic
C-L	:	CML Latches
CMOS	:	Complementary Metal-Oxide Semiconductor
CTLE	:	Continuous Time Linear Equalizer
DC	:	Delay Control
DE	:	Delay Element
DETFE	:	Double Edge Triggered Flip-Flops
FF	:	Fast NMOS Fast PMOS
HDMI	:	High-Definition Multimedia Interface
IC's	:	Integrated Circuits
IGFET	:	Insulated-Gate Field-Effect Transistor
IoT	:	Internet of Thing
ISI	:	Inter-symbol interference
LEDR	:	Level Encoded Dual-Rail
LET-A	:	Long Term Evolution Advanced
MOS	:	Metal-Oxide Semiconductor
MUX	:	Multiplexer
NMOS	:	N-type Metal-Oxide Semiconductor
NoC	:	Network on Chip
PCIE	:	Peripheral Component Interconnect Express
PLL	:	Phase-Locked Loop
PMOS	:	P-type Metal-Oxide Semiconductor
PVT	:	Process Voltage Temperature
SATA	:	Serial Advanced Technology Attachment
SerDes	:	Serializer and De-serializer

SF	:	Slow NMOS Fast PMOS
SIPO	:	Serial-In-Parallel-Out
SoC	:	System on Chip
SS	:	Slow NMOS Slow PMOS
TT	:	Typical NMOS Typical PMOS
UHF	:	Ultra-High Frequency
USB	:	Universal Serial Bus
WP	:	Wave Pipeline
3G/4G/5G	:	Third/Fourth/Fifth Generation

Chapter 1

Introduction

1.1 Motivation

The era of the Internet of Things (IoT) and Big-Data, needs the significant amount of data generation and transmission through various hardware and software protocols. The IoT networks have enormous amount of information, from multiple connected devices. Such kind of data usage is increasing day by day therefore the interconnected devices of IoT network requires the standard protocol to work together for data handling. So, this kind of data can be utilized with any other network protocols [1][2].



Figure 1.1 Internet of Things and its Interconnected area [3]

Figure 1.1 shows the role of IoT network in our daily life, it covers every aspect connected to humans need i.e. healthcare, infrastructure, automation, energy etc. [3]. It uses various communication protocols to fulfill these requirements, which plays a significant role in wire line and wireless communication techniques [2]. For information transfer among multiple devices over the network, fast data transmission rate is required. The internet bandwidth requirement is boosted to match the needs of IoT systems. As IoT network uses machine to machine communication, it requires the large number of transmitter and receiver for real-time applications in this emerging field [4]. It requires deployment of sensors and controlling unit over the remote location, which helps in data sensing.

The data transfer growth rate in cellular networks is making milestone while working with IoT and Big Data. In mobile networks latest standards like Long Term Evolution Advanced (LTE-A) [5] also plays an essential part in IoT network. It helps in connecting the various IoT nodes and information sharing with data centres as shown in Figure 1.2 [6-7]. It captures the demand like high bandwidth, data rate, control etc.

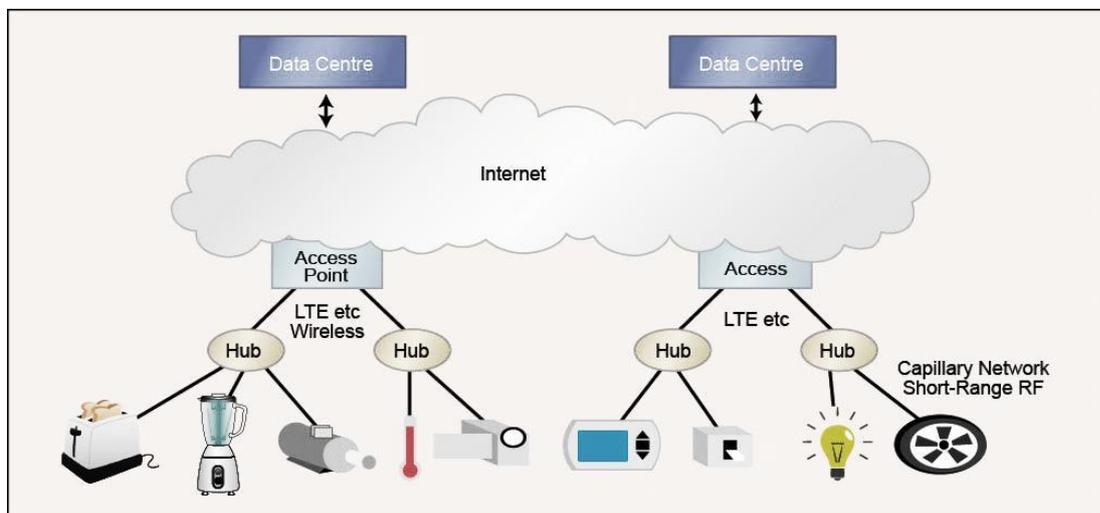


Figure 1.2 Role of LTE in Internet of Things [7]

In machine to machine communication, intermediate nodes are used to send data from sensor to network. Data processing through these intermediate nodes may reduce the cost of the system, but there are issues related to

topological or routing changes. The deployment of sensing devices in next generation communication standards like 4G/LTE-A or its advanced version demands communication efficiency, reliability and data security [8],[9]. To match with this surging demand of high-speed network, operators are turning towards the 4G networks, and boosting their connectivity, capacity, and speed [9].

As the numbers of I/O pins in Integrated Circuits (IC's) are increased, it results, the high-power dissipation, capacitive load, inter-symbol interference (ISI) and signal losses over the medium. [10-12]. These performance degradation issues make the condition worse for network-on-chip, routers and cross bar switches [11]. In addition, the scaling of MOS devices improves the performance of various circuit blocks, but the global interconnect does not exactly follow this same scaling improvement comparative to logic blocks due to low congestion communication infrastructure. As the chip sizes reduce day by day, it results in the complex design of high-speed links. Which needs the power optimization compared to the reduced area, and another major design issue is clock synchronization. The timing errors due to jitter and skew on the parallel bus makes the receiver synchronization crucial and limit the bandwidth [11-12].

In order to achieve connectivity and high speed in on-chip communication, one can choose parallel communication or serial link. Parallel data transmission requires parallel transmission lines which increases crosstalk as well as chip area. This parallel data transmission also generates routing congestion at receiver end which results in signal recovery problem. To overcome these issues of parallel transmission, the researchers find another promising solution for data transfer through the serial link [13].

Serial link transceivers have the advantage to achieve bandwidth requirement, small chip area and cost, which makes it a most promising solution. It finds its application in Serial Advanced Technology Attachment (SATA), Peripheral Component Interconnect Express (PCIe), High-Definition Multimedia Interface (HDMI), and Universal Serial Bus (USB) 3.0. A System on Chip (SoCs) widely used for multi-core communication such as Network on Chip (NoCs). Serial link transceiver has been designed using synchronous and

asynchronous method [14]. Synchronous transceiver uses the clock signal control for selection of various parallel signals. There are different types of clock selection, which is used to convert low-frequency data to high-frequency serialized data and then transmitted through the channel. At the receiver end, deserializer is used to recast the serialized data into the parallel signals. The asynchronous transceiver entirely controlled by the handshaking protocols instead of clock selection dependency. The serial link transceiver is used in different backplane communication circuits like equalizer, Analog to Digital Converters ADCs, and data converters. These circuits are desired to operate at high-speed logic, and this high-speed is difficult to achieve using conventional metal oxide semiconductor (MOS) based circuit design.

Additionally, circuit design using MOS offers different transition frequencies for NMOS and PMOS transistor which results into several design issues. The carrier's mobility in p-channel MOS transistor is low as compared to NMOS transistor, which can restrict the operating speed of the circuit. The PMOS device has an inferior unity gain frequency and cannot operate in the higher-frequency range; which may lead to degradation in high-speed performance [13–23].

The generation of the local oscillatory signal for frequency synthesis and modulation is typically implemented with phase-locked loop (PLL) based frequency synthesizer. The divider is a crucial element for high-frequency synthesizer as it operates at the higher frequency. Basically, two main architectures of the divider are widely used for high-frequency implementation. First one is the true signal phase clocked, while another is master-slave flip-flop based frequency divider [15-21]. It can be designed by CMOS rail to rail logic and current mode logic (CML). For low-frequency applications, CMOS logic is preferred owing to its simplicity, while CML is used for high-frequency applications because of its rapid switching speed, low power dissipation, and smaller output voltage swing [23–26].

This thesis is focused on the design and development of the circuit for the high-speed serial link transceivers with synchronous and asynchronous transmission method which can help the transceivers to achieve high data speed requirements. In addition, the current mode logic latch is discussed in

this thesis, and its time delay model is developed along with previously published latch.

1.2 Research Objectives

The circuit design techniques for both synchronous and asynchronous type high speed serial link transceivers are presented. The specific contributions made in this thesis for the serial link transceivers are as follows.

- Design of synchronous transceiver with the wave combiner and decombiner based Circuit block.
- Analysis and design of current mode logic latch with improved performance parameter. The delay model development of latch.
- Asynchronous serial link transceiver block design is with the improved current mode logic latch and the delay elements.

1.3 Thesis Organization

The chapters of this thesis, provides the background and related introductory information followed by the compilation of published research work. The thesis is organized as follows.

Chapter 1 describes the design requirement and challenges towards the present standards of IoT, Big data and the machine to machine communications. It shows the requirement and introduction about the serial link, various types of serializing methods.

Chapter 2 provides the brief discussion on high speed serial link blocks. This chapter also explains the requirement of continuous time linear equalizers and current mode logic circuits.

Chapter 3 is concerned with the wave combining driver based serial data link transceiver design for multi standard applications. In this chapter, new serial link transceiver design is presented, which is used to achieve high-speed transmission.

Chapter 4 incorporates an improved Current Mode Logic (CML) latch design that is proposed for high-frequency applications. The small signal

equivalent circuit based delay model is also developed for the analysis of proposed CML latch.

Chapter 5 discusses the high-speed asynchronous wave pipelined serializer and deserializer (SerDes) transceiver design implemented using (CML).

Chapter 6, all the contributions of the thesis are summarized in this chapter and the suggestions for future research possibilities are provided.

Chapter 2

Background and Related Work

2.1 Overview of Serial Link

The first thing, which needs to be understood before serial links, is the transition from parallel link communication to serial links in many applications. Because of parallel nature of transmission link, wide data buses are required to transmit the information. As every single data bit is transferred through single link, it requires its own conductors. It results in limited data transmission speeds less and large area [9], [27-28]. The higher performance systems are typically used in supercomputers or workstation.

In last two decades, the data transmission need is exponentially boosted. This demand creates major issue regarding cost and area in parallel link communication to achieve the data requirements. With serial link transmission we can avoid these major bottlenecks [28]. Serial link is the most promising solution and some of its interface like PCIe and SATA are used computer applications to match present scenario requirement because it addresses all the design specifications i.e. area, power, cost and data bandwidth. So after utilizing serial link method for data transmission over parallel method, immediate changes are seen in the form of cost and area[29].

Moreover, in serial link communication the data information is transmitted over a single line, which results in reduction of crosstalk and data skew. As crosstalk's and data skew are the major concerns of parallel line transmission [30]. It also helps in chip packaging due to its less area. In technology scaling, the Moore's law is also implemented on the serial link, which helps in proportional supply voltage reduction according to scaling of technology.

With all these advantages, serial links proven that as a favorable option to achieve the data transmission and efficiency [31].

Figure 2.1 shows the basic block diagram of a serial data link. It consists of a transmitter that modulates the digital input signal bits into the analog signal as per the clock pulse input, further transmitting it to the channel. Second one is Transmission channel, which is responsible for transmission of the data information from the transmitter to receiver. This transmission medium can be an optical fiber, copper wire or metal line. The other side of transmission channel is Receiver block, which samples the incoming signal and deserialize the transmitted bits according to the clock inputs [32-33].

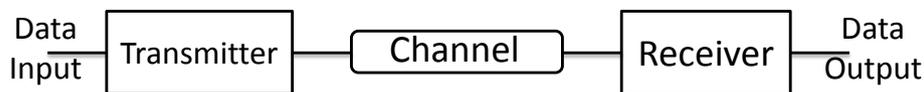
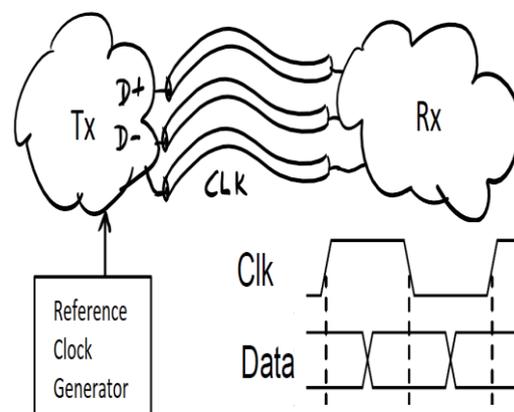
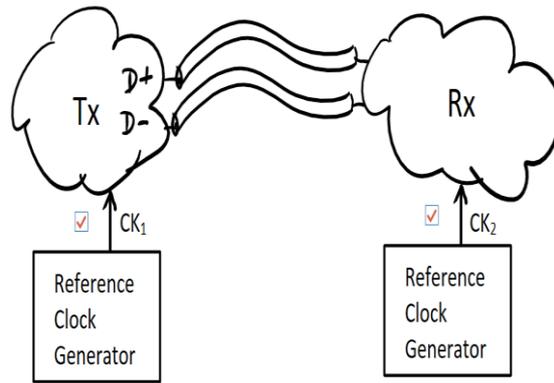


Figure 2.1 Block diagram of Serial Link

Figure 2.2 shows the basic types of Synchronous and Asynchronous Serial link. Synchronous Serial link transceiver uses the reference clock signal and serializes the data according to clock edges. The transmitted data from Tx is transferred to channel along with the clock, which helps receiver to recover the serialize bits by using clock and data recovery. Asynchronous type of serial link uses some standard band rates in transmission medium. Asynchronous method uses reference clock generator at both transmitter and receiver end for clock and data recovery [32-33].





(b)

Figure 2.2 Serial link type (a) synchronous (b) asynchronous

Now the typical implementation of synchronous Serial link, is shown in Figure 2.3. The explanations of transmitter and receiver are as follows.

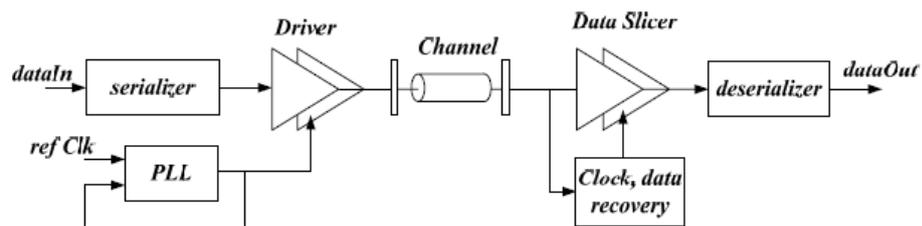


Figure 2.3 Serial Link Building Blocks

2.1.1 Transmitter

The transmitter consists of a serializer, output driver and the PLL. The output driver and serializer transmit data bits at maximum speed and consumes large amount of power at transmitter block. The PLL block is used to guide the data inputs to serialize as per the clock edges, it also matches the jitter requirement of the transmitter. These drivers are used at both the transmitting and receiver end of channel for amplification of signal [34]. The Output driver used in the transmitter portion must have some fixed output impedance matched with the transmission channel, independent from output swings and controllable with equalization methods. The conventional output

drivers are current mode logic (CML) based driver and Voltage mode drivers. Current mode logic drivers have all desirable features of driver to match the transmission channel requirement with only disadvantages found in large current consumption. Whereas the Voltage mode helps in energy efficient operations [35-36]

2.1.2 Receiver

The role of receiver is to recover the input data bits by sampling using recovered clock. In transmission channel, the information got attenuated and distorts due to noise and channel losses. For removal of these losses equalizers at both ends of the serial link can be used. There are different types of equalizers used in serial links; in Section 2.2 we will explain the equalization. Also, the recovered clock required to be aligned with the center half of received signal, so the proper voltage margin is maintained for higher as well as for lower voltage levels. After the proper equalization of signal the clock data recovery circuit is used. At receiver the clock is recovered from the received bit stream and used to sample the data. Afterwards, the system again needs to turn into a set of parallel data from received bit stream. The deserialization process is completed with the help of deserializer. It is fundamentally designed with flip-flop based shift registers or de-multiplexers [33-35].

2.2 Equalization

Furthermore, the important part of any data communication method is its proper recovery. As discussed in Section 2.1 that crosstalk and skew are the major issues that contribute in distortion and data information in the channel. In serial link equalization circuit is used for proper recovery of signal and to remove the distortion effects. The equalization circuit also helps to increase the bit error rate along with removal of closed nature of eye diagram. At the receiver end, it was repetitively sampled the signal and generates the eye which help the circuit designer to evaluate the effect of skew, noise and inter-symbol interference during transmission of signal. In the following Figure 2.4 an eye diagram is shown for the transition from 0 to 1 and 1 to 0.

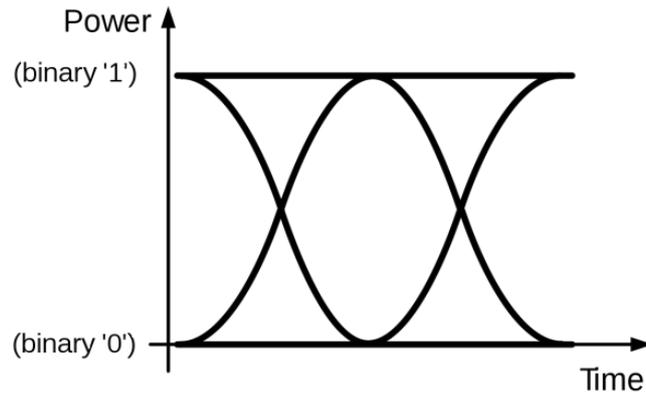
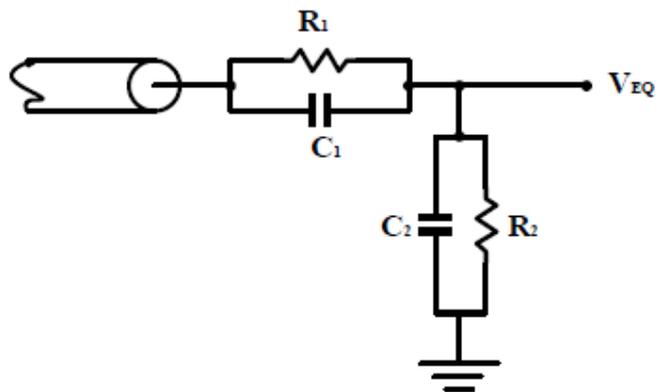


Figure 2.4 Eye Diagram

The interpretation of eye diagram is according to its Eye opening and closure nature. The height of eye (peak to peak supply) opening represents noise in the signal, whereas the eye width represents jitter effects and behavior of circuit architecture. For proper recovery of signals, presence of any inter-symbol interference responds in the form of eye closure [31]. To overcome the inter-symbol interference, equalizer circuits are used. Figure 2.5 (a) shows the passive continuous time linear equalizer used for removal of inter-symbol interference [37].



(a)

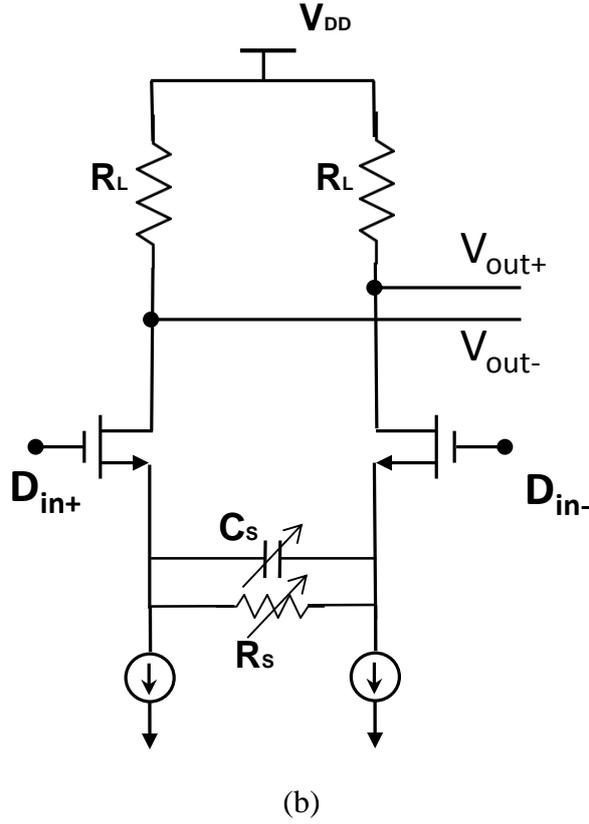


Figure 2.5 CTLE (a) Passive (b) Active

For the passive equalizer proposed by Hanumolu [37] the transfer function equation is as follows.

$$H(s) = \frac{R_2}{R_1 + R_2} \frac{1 + R_1 C_1 s}{1 + \frac{R_1 R_2}{R_1 + R_2} (C_1 + C_2) s} \quad (2.1)$$

The pole and the zero frequencies of the CTLE are as follows.

$$\omega_z = \frac{1}{R_1 C_1} \quad (2.2)$$

$$\omega_p = \frac{1}{\frac{R_1 R_2}{R_1 + R_2} (C_1 + C_2)} \quad (2.3)$$

The overall DC gain for the passive CTLE will depend on the values of resistors

$$DC \text{ Gain} = \frac{R_2}{R_1 + R_2} \quad (2.4)$$

By using this CTLE design at receiver in Serial link communication the equalizer adds gain to the high frequencies as per the pole and zero selection. So, if the pole value of the CTLE is larger than the pole of transmission channel, then the bandwidth of the equalized channel has increased.

The passive CTLE has limitation in the form of zero. In lossy channel single zero based CTLE is not sufficient to match with channel performances. It requires another zero addition to add additional +20dB/decade to match frequency range. The another form of linear equalizer is active CTLE as shown in Figure 2.5 (b) has advantage in gain and it can be designed easily and can be integrated with silicon. The additional zero is introduced in this design is achieved with the parallel combination of resistor and capacitor [37].

The transfer function of active CTLE is given by

$$H(s) = \frac{g_m}{C_L} \frac{s + \frac{1}{R_s C_s}}{1 + g_m \frac{R_s}{2} (s + \frac{1}{R_s C_s})(s + \frac{1}{R_L C_L})} \quad (2.5)$$

The pole and zeroes of active CTLE are as follows.

$$\omega_z = \frac{1}{R_s C_s} \quad (2.6)$$

$$\omega_{p1} = \frac{1}{R_L C_L} \quad (2.7)$$

$$\omega_{p2} = \frac{1 + g_m \frac{R_s}{2}}{R_s C_s} \quad (2.8)$$

For high frequency gain the pole value is selected higher than the zero frequency, and the peaking gain is also controlled using the selected frequencies ratio of pole and zero. The peaking gain value is as follows.

$$A = \frac{\omega_{p1}}{\omega_z} \frac{g_m R_L}{1 + g_m R_S/2} \quad (2.9)$$

This method of equalization helps to achieve the serial link to match the higher data transmission rate with proper height and width of eye diagram.

This differential pair type design also helps in the form of driver design in transceivers. Before transmitting the data information from transmitter, the driver is required with fixed output impedance to match the channel for signal integrity, independent from the effect of equalization without changing its output impedance and its control on output voltage swing. The differential pair design works with the current mode logic-based driver design, In this technique the output impedance is easy to match with channel and independent of output signal swings. Furthermore, to learn more we read many research papers to understand the research findings and gaps of published work in the field of high-speed serial link. The related work in serial links design is discussed as follows in section 2. 3.

2.3 Related Work

S. Safwat *et al.* [32] proposed a self-time signaling technique to multiplex data at the speed of 12Gbps with a clock frequency of 24GHz. The new three-level signaling scheme is introduced to extract data and clock at the receiver side. Serdes transceiver is tested on the lossy on-chip transmission line and shows 15mW power consumption. In [33] order to modify the same, self-timed design is published. This amendment removes the limitation on the minimum frequency found in previous technique. Data transmission is also improved up to the 16Gbps speed. A single-ended transmission line is used to solve routing congestion at the receiver side. They also showed switching threshold inverter techniques for correction of the signal at the receiver side. In Chapter 3 the work proposed is the combiner at the transmitter side and decombiner at receiver side along with the threshold inverters, this method maintains the two-level signaling.

Jaiswal *et.al.* [36] presented an on-chip asynchronous wave-pipelined CML SerDes, which uses delay element and MUX for bits propagation through the

serial link and new bits loaded via MUX. This SerDes implemented on 65nm technology resulting in total power consumption of 14.3mW and data rates of 12.67Gbps

Tadros *et al.*, [34] showed a differential self-timed three level signaling scheme, which uses half data rate frequency and achieves 24Gbps data transmission with 65nm technology. With the 12GHz input clock, it serializes the parallel 8 bits input of 3Gbps speed.

Mu-Shan Lin *et al.*, [38] presents a system of SerDes with 5Gbps Speed for Low power PCI Express. It occupies the area of $510\ \mu\text{m} * 710\ \mu\text{m}$ and, power consumption is 125mW with a supply voltage of 0.9 V at 40 nm technology. Asynchronous method of serialization is used by Bui Chinh Hien *et al.* in [39], In this technique, data is fed with the help of *load* signal through transmission gate, at this time *en_se* signal is LOW so that tri-state inverter are disabled which prevents data to propagate before it is properly loaded. After loading, the *load* signal goes LOW and *en_se* goes HIGH to propagate the data. Deserializer has same structure as of Serializer for timing reference and to prevent the jitters and data corruption. The circuit operates at 3.9Gbps speed with 2.44mW power consumption.

In [40], a clocked static CMOS/CML 16:1 Serializer is designed., by using 2:1 multiplexer to combine the input for serialization. Both CMOS and CML are used so that advantages of both can be utilized. The low speed branches are implemented using CMOS to reduce the static power loss and at high frequency stages CML is used. The circuit operates at 10Gbps speed with power 106mW. In [34] asynchronous CML SerDes is designed with the help of multiplexers, where all are designed in CML. *load* signal is used to control the flow of the data. Data is loaded from one of the inputs of multiplexer and propagated from other input. Serializer and Deserializer have same structure and control block for proper functioning. *Pilot* bit is used for all serialized 8 bit word so as to control signal can sense the bit and judge that the bit stream is arrived for deserialization. Thus, control block generates the signal to stop the transmission and parallel data can be available at the output pins.

In [24] an ultra-high speed CML latch is designed. This latch uses additional transistor so that current at one level of clock can be increased to reduce the error and thereby increasing the speed. Latch uses only one additional transistor at negative level of the clock so that tail current can be increased to gain speed. *Dobkin et al.* in [42] proposed wave pipelined bit-serial link with level encoded dual-rail (LEDR) asynchronous protocol to reduce per bit synchronization.

Chapter 3

Wave Combining Driver based Serial Data Link Transceiver Design for Multi Standard Applications

3.1 Introduction

The internet revolution increases the data traffic, the need to support this traffic requirement can be achieved with high bandwidth and equipment performance growth. Various devices have been a requirement to send and receive the information through internet. Previously the data inside the system is transmitted using parallel communication. Once data is transmitted from the transmitter, cable sizes required large area to carry the data and also crosstalk issues associated with multiple signal lines. Serial transmission was adopted as a solution that simplified data transmission protocols.

This chapter has presented a new serial link transceiver design, which is used to achieve high-speed data transmission requirements. The proposed design comprises of wave combining and driving unit at the transmitter end, and decombining at the receiver end. The continuous time linear equalizer (CTLE) helps to limit the jitter tolerance up to 10% of the data received. The simulation results with PVT corners show its compatibility with process corner variations. The wave combiner design may help to double the transmission speed of existing serial link standards like PCI, HDMI, USB, and SATA.

3.2 Proposed Transceiver Design

Figure 3.1 shows the proposed block diagram of synchronous transceiver design. At transmitter side two serializers are used for serializing of 8-bit parallel data as per the clocking sequences. The transmitter section includes the serialization blocks with wave combining and driving unit. Tcruche wave

combining unit generates combined bit sequence with driving capability so that it can be transferred over the transmission channel.

In the transmitter, oscillator is used to generate the operating frequency of 8GHz. Initially, 1GHz clock is used to select the data bit from the input of serializer, which helps to serialize data at the rate of 8Gbps, which is transferred through buffers after serialization. The wave combining unit combines these serialized streams and drives it to the transmission channel with the help of clock signal. We have used the single dispersion-less transmission line as a transmission channel to transmit the data with its length of 3mm. At the receiver, differential pair based active equalizer is selected to equalize the signal from noise and distortion, afterwards de-combiner is used to separate the data streams into data stream 1 and data stream 2, and then de-serializer recast the serial data into parallel.

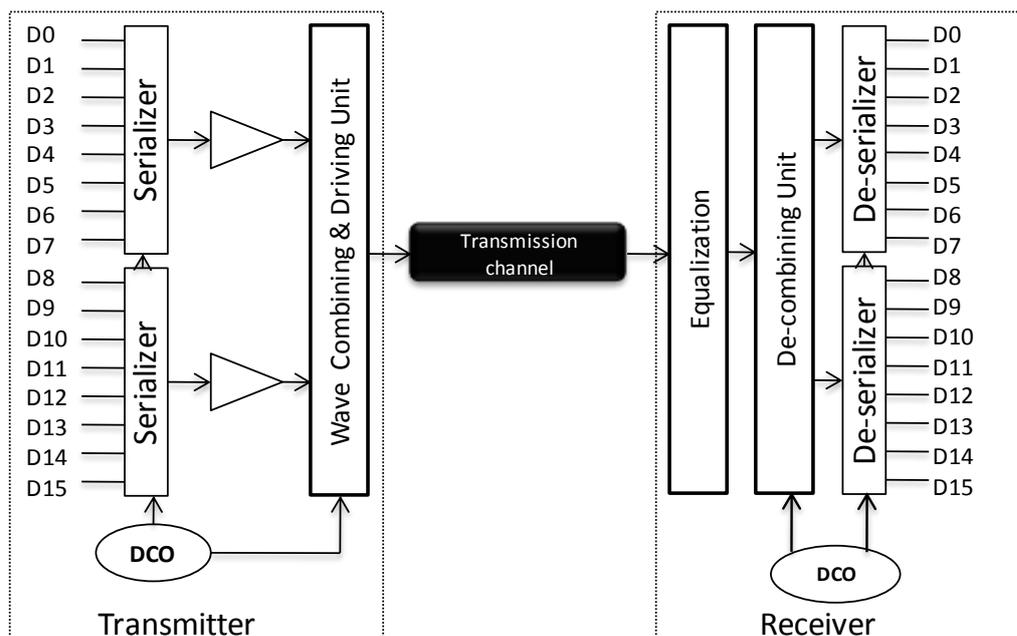
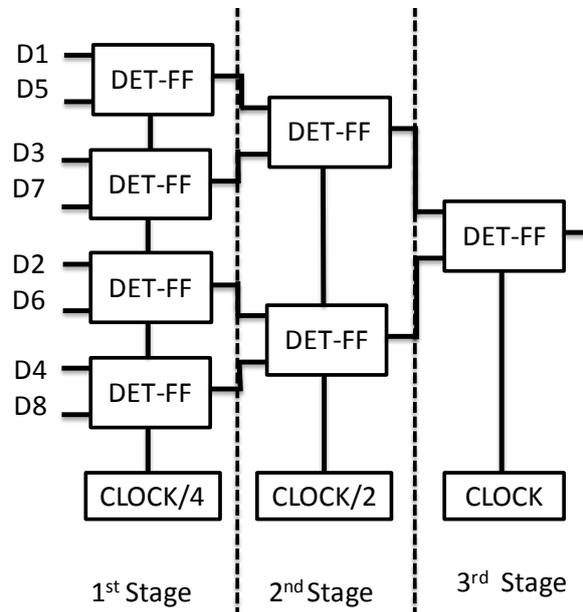


Figure 3.1 Block diagram of proposed SerDes with proposed wave combiner and de-combiner

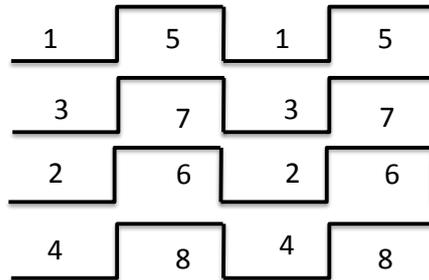
3.2.1 Serializer Design

The serializer design shown in Figure 3.2, consists of the combination of double edge triggered flip-flops (DETFF) for serializing the data [32]. The DETFFs are the basic cell for the serialization block, which select the data

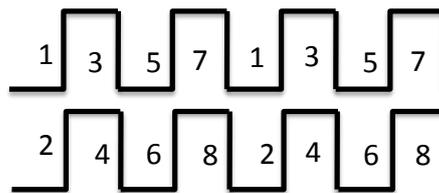
according to the positive and negative edges of the clock cycles. These DETFFs were designed using transmission gate logic which help in the form of speed enhancement and less power requirement over CMOS.



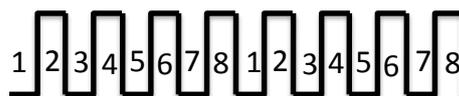
(a) Serializer design



(b) First stage clock



(c) Second stage clock



(d) Third stage clock

Figure 3.2 Serializer design with stage wise serialization

In Figure 3.2 (b) different clock supply has been applied at every stage. It helps to choose data bit according to the positive and negative edges of clock signal. So, at the transmitter end we received data according to the serializer data bits.

After the first stage of clock signal, where the clock signal is one fourth of the main clock, the data is serialized in the following pattern as shown in Figure 3.2(b). These serialized data is now applied to the second stage DETFF, which allows and serializes the data in the form of odd and even bits according to its clock/2 signal as shown in Figure 3.2(c). Finally, the last stage uses same phenomenon to serialize all 8 bit data into one serialized data which is shown in Figure 3.2 (d)

3.2.2 Deserializer Design

The Deserializer is designed using serial-in-parallel-out shift register (SIPO) as shown in Figure 3.3. This SIPO architecture divides the bit stream according to the clock signal. In this design we use half clock rate frequency, which is used at input serialization blocks. It helps to distinguish bit streams according to the positive and negative edges of the clock and parallel data is received using the D-flip-flops.

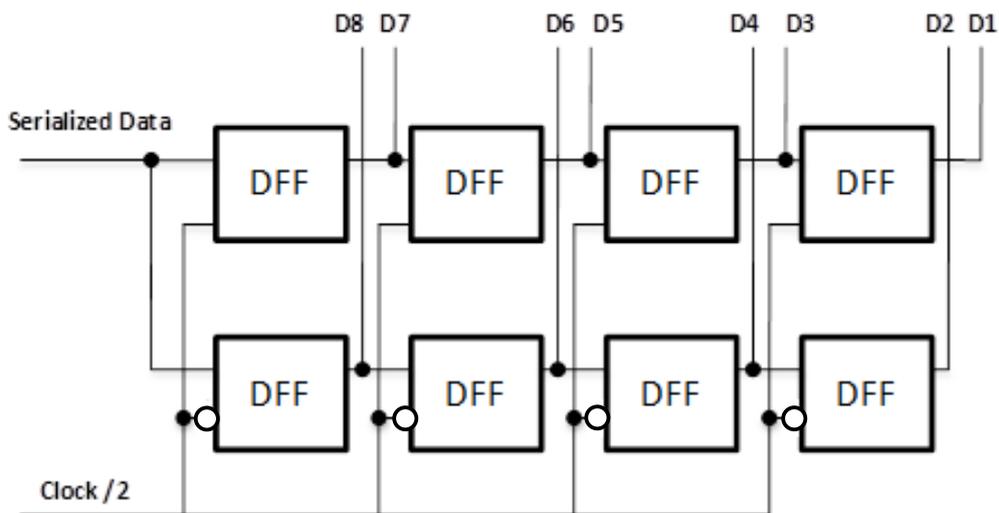
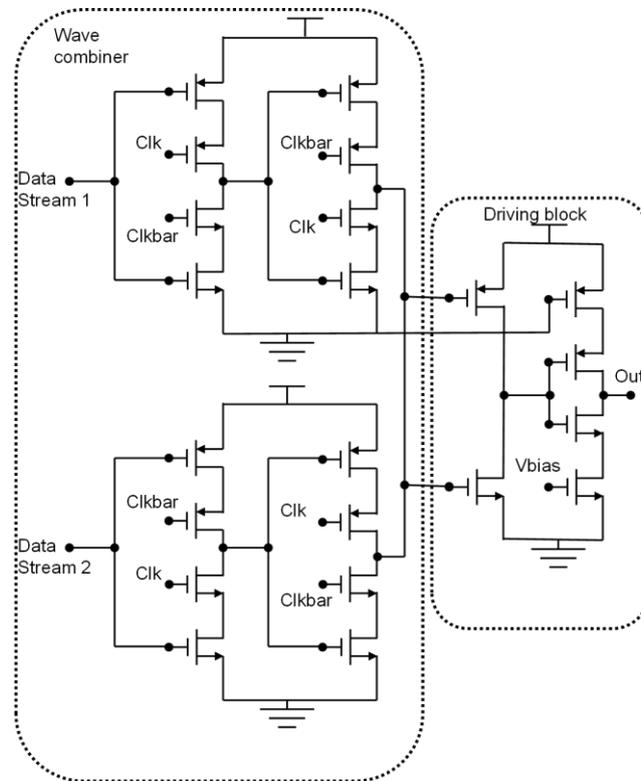


Figure 3.3 Deserializer design with outputs.

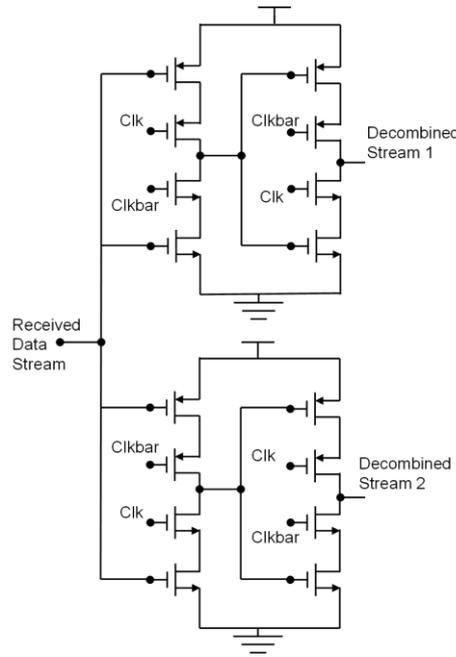
3.3 Wave Combiner and Decombiner

The proposed wave combining and driving unit, which is shown in Figure 3.4(a), has two blocks. The first one is used for selection of the information while second one is used to drive it through the transmission channel. In the first block, two different data streams are applied as input.

The combination of data takes place by positive and negative edge triggering of clock input signal (clk). The input clock and its complement (clkbar) are used for data stream selection according to rising and falling edge of clock signal. Data stream 2 is selected during rising edge of the clock signal, while the data stream 1 is selected during falling edge so that the output does not have any information overlapping after the wave combination. For the combination of data streams, 8GHz clock frequency is used as a clock signal. At the driving stage of wave combiner, the combined data is boosted to maintain the logic level “high” and “low” with the help of bias voltage signal and then it is fed to the transmission channel.



(a)



(b)

Figure 3.4 (a) Wave combiner and driving unit design (b) Decombiner design

A single ended dispersion-less transmission line with ground termination is used to match with proposed model, instead of the differential transmission line because it reduces the routing area and power dissipation. The dispersion-less model helped us concerning non-dependency on the frequency of results. In this transmission line model inductance and capacitance makes the characteristics impedance of transmission line frequency independent. So, the output propagation in this transmission is dispersion-less.

After the data transmitted over this transmission line, at receiver side CTLE is used to reduce jitters incorporated during transmission in channel. We used differential pair based active CTLE which need differential signaling, So CMOS to CML (current mode logic) blocks are used which helps CTLE for equalization on receiving data streams. The equalizer taps are used to maintain the offset voltage level of collecting the data at receiver end. Moreover, the decombining uses the single input data streams after equalization. For single-ended input, we used CML to CMOS converter after equalizer, which is required to send the data to wave decombining.

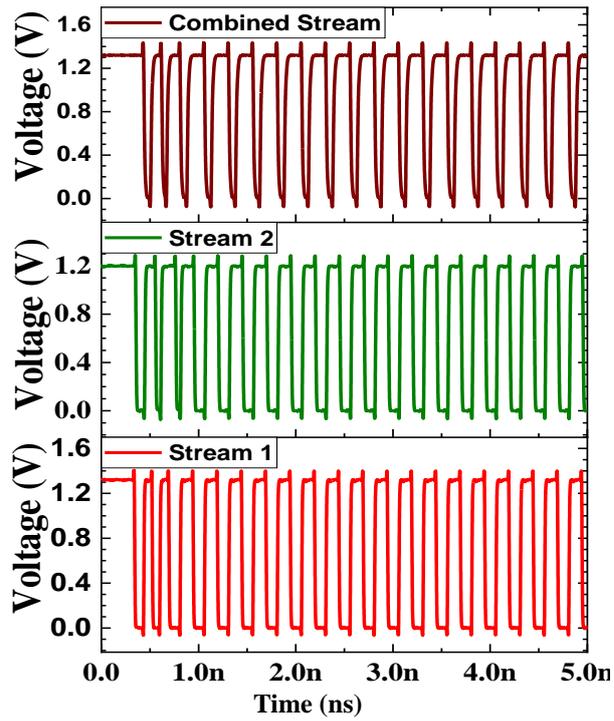
The Wave de-combining stage uses the same approach as the wave combiner unit of edge triggering and divides the received data into two separate streams. As shown in Figure 3.4 (b), according to the positive and negative edges of clock signal it generates the data stream 1 and data stream 2 respectively. For proper recovery of data streams the clock rate of decombining and combining block should be the same. Therefore, signal of same clock frequency i.e. 8GHz has been chosen at the decombining end. The separated two different data streams are then forwarded to deserializer which convert data stream into bits.

3.4 Results and Discussion

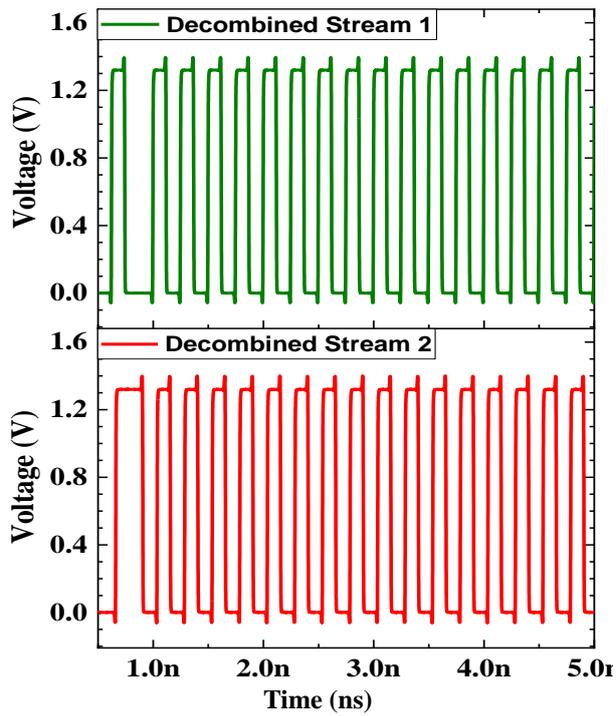
The Synchronous SerDes transceiver is designed with 65nm standard CMOS technology and 1.2V voltage supply. Each serializer block serializes data with 8Gbps, whereas wave combiner results in 16Gbps after combining two separate bit streams. The transceiver also boosted the voltage levels of transmitting signal. Simulation result waveforms of wave combiner and de-combiner at room temperature are shown in Figure 3.5. 16Gbps speed achieved with very low power consumption at each stage. Table 3.1 shows the power consumption of various blocks under PVT corners. The circuit simulated with temperature variation from -45°C to 125°C and voltage variation from 1.08V to 1.32V. Table 3.2 compares this work with [30-32]. Use of transmission gate instead of CMOS reduces the power consumption at the different stages.

TABLE 3.1 POWER CONSUMPTION OF BLOCKS ASSOCIATED WITH DESIGN

Blocks	Average Power Consumption (mW) in different process corner		
	TT	SS	FF
Serializer	57.8	39.4	64.24
Wave-Combiner & Driver	4.16	2.3	4.3
Equalization block	15	5.56	29.84
Decombiner	5.71	4	7.3
Buffers	10	4.69	11.6



(a)



(b)

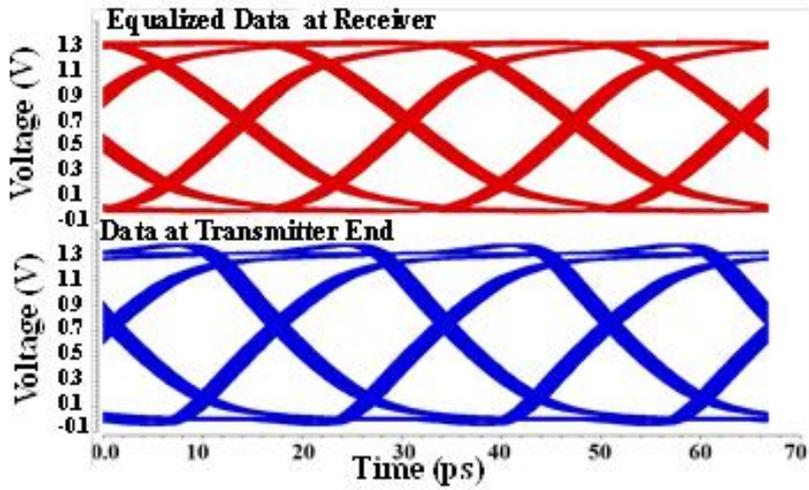
Figure 3.5 Simulation waveform (a) Transmitter end (b) Receiver end

TABLE 3.2 COMPARATIVE ANALYSIS WITH PREVIOUS WORK

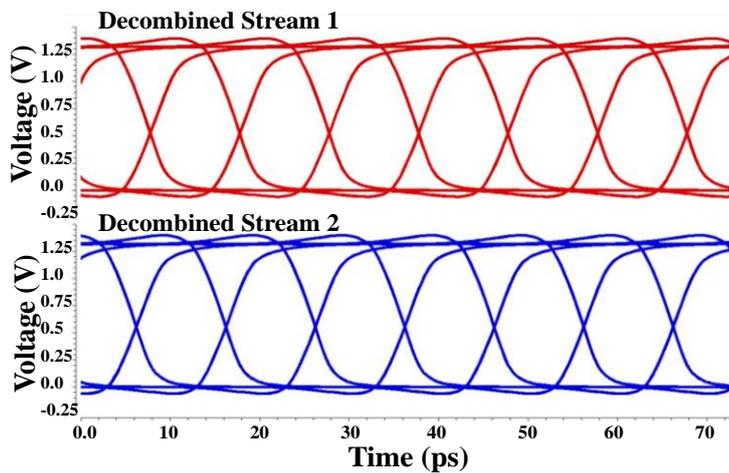
	Our Work	Safwat <i>et.al.</i> [32]	Hussein <i>et.al.</i> [33]	Tadros <i>et.al.</i> [34]	Duvvuri <i>et.al.</i> [42]
Tech.	65nm 1.2 V	65nm 1.2 V	65nm 1.2 V	65nm 1.2 V	65nm 1.1 V
Data Rate (Gbps)	16	12	16	24	15
TL	3mm	3mm	3mm	5mm	7.5 in FR4
Freq. (GHz)	8	24	16	12	---
Notes	2 level	3 level	3 level	3 level	---

Eye diagram of combined data at transmitter and receiver is shown in Figure 3.6 (a), which shows the proper transmission of information. Eye diagram of decombined bit stream 1 and 2 are shown in Figure 3.6 (b). It shows proper eye opening of the signal, which depicts in a proper recovery of an input signal at the receiver end. Due to edge triggering at wave de-combiner unit around 10% jitter window occurred in output stream 2, which shows more occurrence of “0” signal compared with “1”. The vertical eye opening of output signal is 0.9V and horizontal eye opening is 10ps.

For perfect matching of output with respect to input signal, voltage swing required to be as large as possible. In [30], due to three levels signaling the voltage swing is limited to 500mV, which results in input and output voltage swing is around 500-600mV for speed of 12Gbps and its eye diagram of output, showing eye crossing of around 75% due to noise and other pulse symmetry issue. As per the eye diagram in [40], the serializer eye diagram shows 1V peak to peak output swing.



(a)



(b)

Figure 3.6 Eye diagram (a) transmitter and receiver Section (b) Eye diagram of decombined signal.

In proposed wave combiner design, eye diagram shows the voltage swing of around 0.9V eye opening on transmitter and receiver end. I have worked on two level signaling in wave combiner design and it shows vertical eye opening of 0.9V at transmitter and receiver. The eye diagram of decombined data streams have also shown with vertical eye opening of 1.1V peak to peak and horizontal eye crossing at 0.5V after decombination.

3.5 Conclusion

In this chapter, the synchronous serial link design is discussed with the help of a proposed wave combiner and decombiner. The proposed model is responsible for the combination of different data streams into a single data stream. This design also helps with efficient transmission capability of high-speed serial links. It uses a binary tree approach for designing wave combiner and decombiner with half clock rate structure. It uses a low-frequency signal to transmit a high-speed signal compared to literature. Furthermore, the other type of serial link technique, i.e., asynchronous serial links, uses the current mode logic-based circuit for the fast operation because of its swift current switching method at differential pair transistors and its output swings.

Chapter 4

An Improved Current Mode Logic Latch for High Speed Applications

4.1 Introduction

In analog circuit design, current mode logic circuits are essential element. Differential pair of CML circuit helps with current steering and produce the differential outputs, the output signals are complement to each other. The main difference in CML is its output voltage swing, the output complement each other by smaller voltage swing, which results in fast switching operation. The limitation with the CML is its power consumption, but it is tolerable for achieving high speed operation.

Numerous Current Mode Logic (CML) architectures are discussed along with an improved Current Mode Logic (CML) latch design. For an asynchronous transceiver, the improved CML latch is designed to boost the output voltage swing. A frequency divider for operating frequency of 16GHz is also proposed using the same improved CML latch based design. Next, the delay model is also developed based on small signal equivalent circuit for the analysis of proposed latch. The output voltage behavior of the proposed latch is analyzed using 180nm standard CMOS technology.

4.2 CML Latch

The Conventional CML latch is shown in Figure 4.1. It works in two different modes: tracking mode and latch mode. In the tracking mode, transistor pair of M_1 and M_2 senses the information and the regenerative pair M_3 and M_4 stores that information accordingly. These modes are dependent on the clock signal. When V_{clk+} is high, transistor M_5 operates in tracking mode, while M_1 and M_2 transistors sense the input data variation. In this mode of operation tail current I_0 is taken to transistor M_5 , and allows output to track the input signal, at this

time cross-coupled regenerative transistors stores the data [26]. When input clock signal $V_{\text{clk-}}$ is high, it enables the latch mode of the circuit to store the data through the cross-coupled transistors M_3 and M_4 , while current I_0 flows through M_6 to feed the input signal V_{in} [23–26]. The output voltage levels are defined as V_{DD} and $(V_{\text{DD}} - RI_0)$ respectively and is independent of the input common mode voltage level [44]. For large output swing common voltage required to be increased, but it should not be greater than input clock common mode level. In conventional CML latch fixed tail current source supplies fixed bias current, so the transistors always work in saturation region. So, the CML topology is used which exhibits higher operating speed [24].

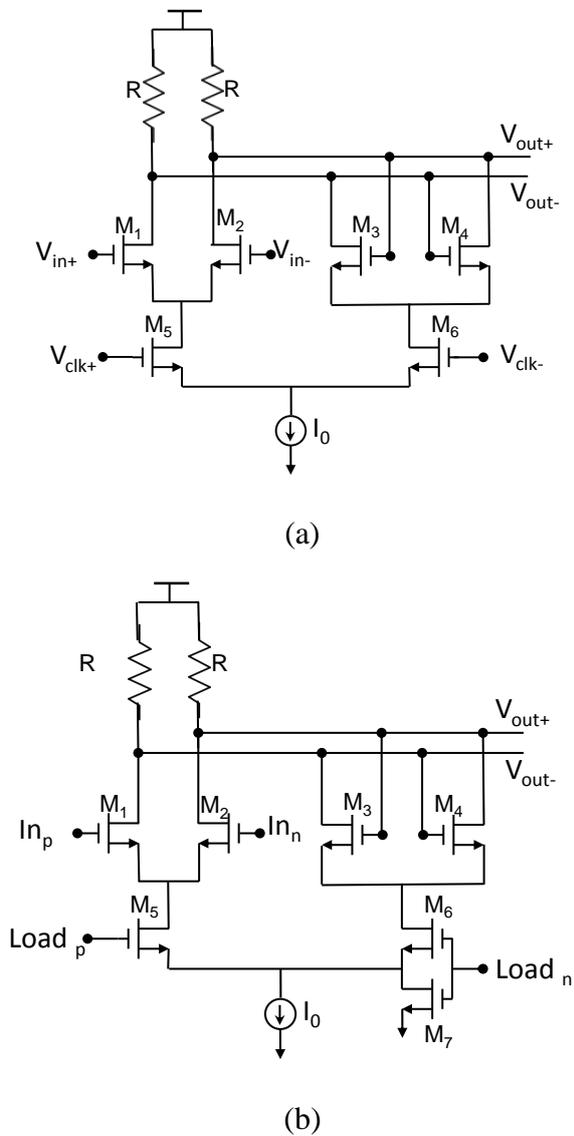


Figure 4.1 (a) Conventional CML Latch (b) Modified CML Latch of Ref. [24]

In higher frequency range ($> 7GHz$), the conventional latch has some functional failures for limited gain in latching branch [44], so different architectures are proposed to improve its gain under high frequency [22],[45]. In a conventional latch, during tracking operation, M_1 and M_2 transistor's capacitance increases which degrades the small signal gain for proper tracking operation. The conventional CML latch consists of only one single tail current source for both modes of operation. The main limitation of this latch is that for ultra-high speed data rates, the parasitic of the input transistors degrade the performance during the tracking operation. Therefore, the tail current needs to be high to achieve significant linearity but on another side in latch mode, large bias current is not required. Therefore, the modification in the conventional latch is proposed [22] by designing distinct tail current branches for the latch and track mode of operation controlled by the reference voltage, which makes the new latch suitable to work on high-frequency operations.

This modified CML latch introduces additional tail current source so that both tracking and latching mode use distinct current, which makes the new latch suitable to work in high-frequency operations. When clock signal V_{clk+} is high, the entire tail current flows through tracking branch. The additional transistors M_7 and M_8 controlled by V_{ref} allow tracking of input signal V_{in} . In latch mode, the tracking branch is disabled so the latch pair permits the stored logic to output.

Another modification in the CML latch is proposed by Zhang *et. al.* [24] by boosting the tail current during latch mode. An additional NMOS transistor is introduced in latch branch which is controlled by V_{clk-} signal. During tracking mode, the latch works as a conventional latch design while the additional transistor is in the off state, so the total current flow in track mode is I_0 . In latching mode, the additional NMOS transistor is turned on, therefore increased total current flows through latching branch is equal to $I(I_0) + I(\text{NMOS transistor})$. It results in higher gain under higher frequency.

4.3 Delay Model

Propagation delay is one of the most important parameters of any sequential or combinational logic design. We have developed a propagation delay model of

CML latch introduced by Zhang *et. al.*[24]. The delay model for already developed CML latch design [24] is shown in Figure 4.2. The circuit is divided into three parts. The delay τ_A is calculated for the Output node (V_{out+}) with reference to the input signal V_{in} and the delay τ_B is associated with the output node (V_{out-}) with reference to the input signal V_{in} . The third delay (τ_C) originates due to V_{clk+} .

For Output node (V_{out+})

$$\tau_A = R_{eq,A}C_{eq,A} \quad (4.1)$$

Where $R_{eq,A}$ is the equivalent resistance, and $C_{eq,A}$ is the equivalent capacitance of Figure 4.2 (a), is given as,

$$R_{eq,A} = \frac{1}{(2G_{m1,2} \parallel G_{m5})} \quad (4.2)$$

While,

$$C_{eq,A} = C_{gs5} + C_{gd5} + 2C_{gs1,2} + 2C_{gb1,2} \quad (4.3)$$

For Output node (V_{out-})

$$\tau_B = R_{eq,B}C_{eq,B} \quad (4.4)$$

Where $R_{eq,B}$ is the equivalent resistance, $C_{eq,B}$ is the equivalent capacitance of Figure 4.2 (b), is given as,

$$R_{eq,B} \cong R_D \quad (4.5)$$

While,

$$C_{eq,B} = 2C_{gd1,3} + C_{gs3,4} + 2C_{db1,3} + C_{RD} + C_L \quad (4.6)$$

the third time constant is due to input clock signal V_{clk+} and output node.

$$\tau_C = R_{eq,C}C_{eq,c} \quad (4.7)$$

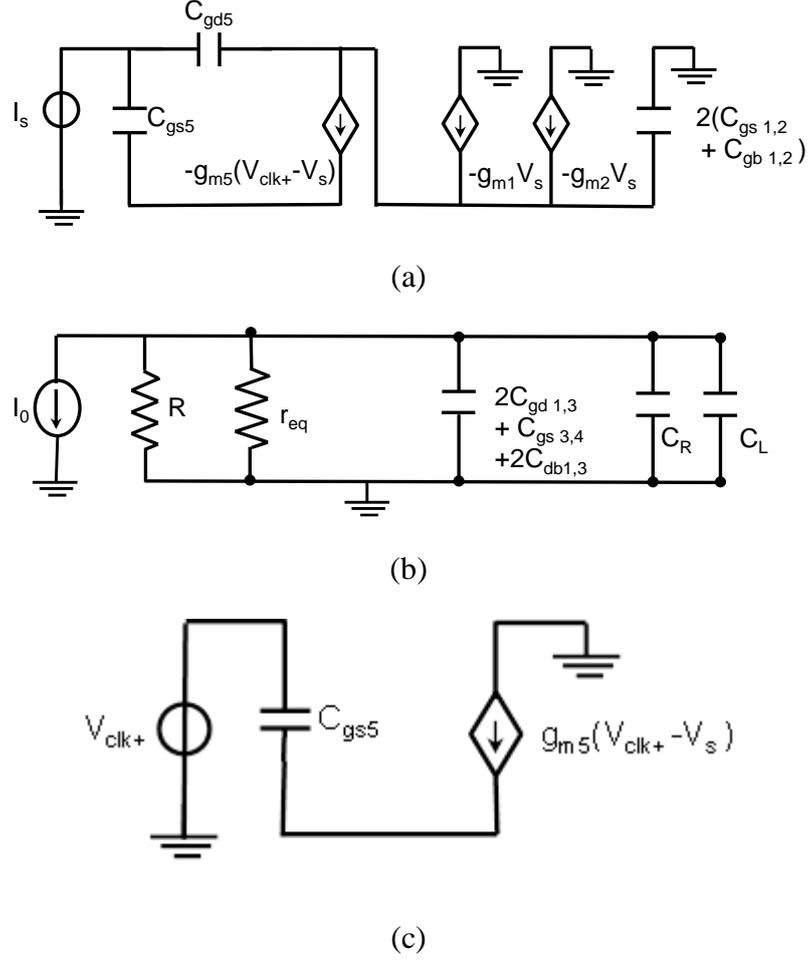


Figure 4.2 Equivalent circuit model for delay for (a) τ_A (b) τ_B (c) τ_c

where,

$$R_{eq,A} = \frac{1}{G_{m5}} \quad (4.8)$$

and

$$C_{eq,c} = C_{gs5} \quad (4.9)$$

4.4 Proposed CML Design

The proposed CML latch is shown in Figure 4.3, in which we introduce additional transistor to provide current flow in track mode transition. In both operations, the transistor pair combination of M_5 - M_8 and M_6 - M_7 is controlled by the differential clock signal. When V_{clk+} signal is high, the transistors M_5 - M_8 are turned on and allow tail current to flow in tracking mode. In latch mode, transistor pair M_6 - M_7 helps to flow tail current in

regenerative transistor pair. These additional transistors M_7 and M_8 result in high gain as well as improved circuit suitability for high frequency and low power applications.

The propagation delay model of the proposed CML latch is discussed in this section. Delay model is shown by considering the output signal according to the clock (V_{clk}) [18], [45–47]. In our proposed model of CML latch, equivalent propagation delay model is shown in Figure 4.4. Propagation delay model is also split into three parts similar to time constants of [24].

For Output node (V_{out+})

$$\tau_A = R_{eq,A} C_{eq,A} \quad (4.10)$$

Where

$$R_{eq,A} = \frac{1}{(G_{m1} + G_{m2})} \quad (4.11)$$

and

$$C_{eq,A} = C_{gs5,6} + C_{gd5} + 2(C_{gs1,2} + C_{gb1,2}) \quad (4.12)$$

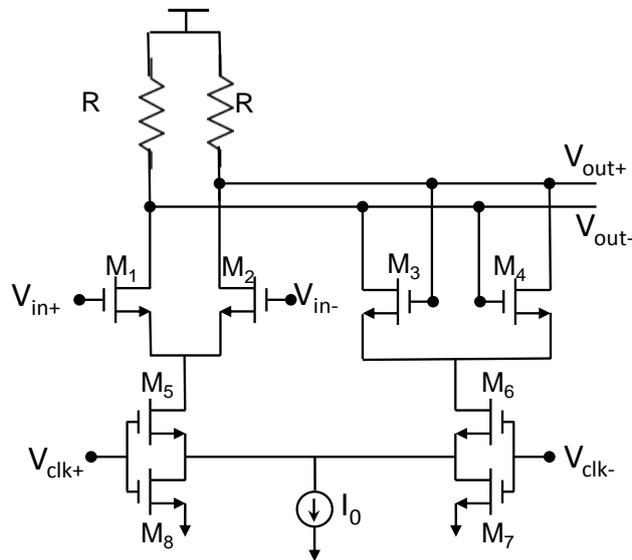
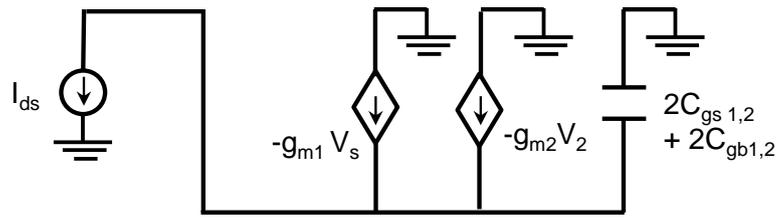
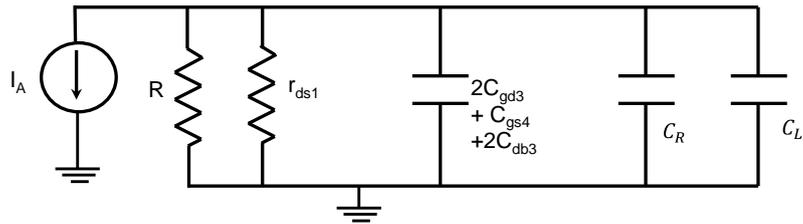


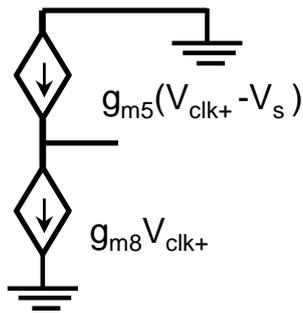
Figure 4.3 Proposed CML Latch



(a)



(b)



(c)

Figure 4.4 Proposed CML latch Equivalent circuit model for delay for (a) τ_A
(b) τ_B (c) τ_C

For Output node (V_{out-})

$$\tau_B = R_{eq,B} C_{eq,B} \quad (4.13)$$

where,

$$R_{eq,B} \cong R_D \quad (4.14)$$

and

$$C_{eq,B} = 2C_{gd1,3} + C_{gs3,4} + 2C_{db1,3} + C_{RD} + C_L \quad (4.15)$$

The third time constant in our proposed design is due to the input clock signal (V_{clk+}), which is also connected through additional transistor M_8 , which will affect the time constant and the output node.

The third time constant

$$\tau_C = R_{eq,C} C_{eq,c} \quad (4.16)$$

where,

$$R_{eq,c} = \frac{(G_{m5} + G_{m8})}{(G_{m5}G_{m8})} \quad (4.17)$$

and

$$C_{eq,c} = 2C_{gb5,8} + 2C_{gs5,8} \quad (4.18)$$

This proposed design is having slightly higher time constant τ_C compared to reported work by [22].

4.5 Static Model and Transistor Sizing

The proposed CML latch is designed using resistive load, the static model derived in [14] and [16] by modeling their load transistors by an equivalent resistance R_P . By BSIM3v3 model, the linear resistance computed is as follows

$$R_P = \frac{R_{int}}{1 - \frac{(R_{DSW} \cdot 1.10^{-06})/W_P}{R_{int}}} \quad (4.19)$$

Where, R_{DSW} = Empirical model parameter

W_P = Channel width of load transistor and

R_{int} = Intrinsic resistance of the PMOS transistor in linear region

However, we have used resistive load structure, the linear resistance model of PMOS transistor is not applied in the proposed design.

One more essential parameter for design is Output Voltage Swing. With reference to [9], the voltage swing should be lower than the twice of threshold voltage (V_{Th}), to ensure that the transistor $M_{1,2,3,4}$ shown in Figure 4.3 should operate in saturation region. The voltage swing equation determined by [16] is

$$V_{swing} = R_p I_{ss} \quad (4.20)$$

The small signal voltage gain A_v and noise margin NM of the CML will be computed according to the method outlined by [26].

$$A_v = \frac{V_{swing}}{2} \sqrt{2\mu_{eff,n} C_{ox} \frac{W_n}{L_n} \frac{1}{I_{ss}}} \quad (4.21)$$

$$NM = \frac{V_{swing}}{2} \left[1 - \frac{\sqrt{2}}{A_v} \right] \quad (4.22)$$

Where $\mu_{eff,n}$, W_n , L_n are the effective electron mobility and the width and length of the transistor pair M_1 - M_2 and M_3 - M_4 .

The sizing of the transistor is determined by the small signal voltage gain and the noise margin. As we have used the resistive load in our design so the maximum current, I_{max} for the design will be as follows.

$$I_{max} = \frac{V_{swing}}{R_{load}} \quad (4.23)$$

The transistors ($M_{5,6}$) work as conventional latches for the track and latch mode operation. For maintaining the voltage swing, the aspect ratio of the additional transistors M_7 and M_8 , in current source section is maintained in a manner such that the total voltage swing does not cross the twice of threshold voltage level.

With reference to [24], in the latching operation, the transistor M_7 turns on and the current flows through the latching branch equals to $I(I_0) + I(M_7)$, which is larger than the conventional CML latch. To match the voltage swing condition the total current should not exceed larger than I_{max} . Therefore,

following criteria for current source should be followed in tracking and latching operations

$$I_{max} \leq I_0 + I(M_7) \quad (4.24)$$

The M_7 & M_8 Transistors have the same aspect ratio and the width of the transistors can be increased to an extent such that maximum current matches the Voltage swing condition.

In this design the aspect ratio of $M_{1,2,3,4}$ is chosen to be same, whereas the transistors $M_{5,6}$ are chosen as double aspect ratio to handle the worst case current of transistor pair M_1 - M_2 and M_3 - M_4 . The additional transistors M_7 and M_8 are used with higher aspect ratio to maintain and provide path for I_{max} if it exceeds I_{bias} by a very large amount.

4.6 Results and Discussion

The circuit is designed using 180nm standard CMOS technology with 1.2V power supply. The layout of the proposed design is as shown in Figure 4.5. The post-layout simulations were carried using Spectre simulator. Some of the output wave forms of the proposed latch is as shown in Figure 4.6. The performance of the CML latch is checked at 1.25GHz frequency and shown in Figure 4.6. In tracking and latching operation the output offset voltage range is increased. In output waveform, received voltage range is between 0.1V to 0.3V for “logic low” and between 0.9V to 1.15V for “logic high”. The additional transistors used in tail branch helped to increase overall current in both operations of CML latch. This technique has the merit of improved offset voltage window as compared to conventional and previously published works.

Comparative analysis of the maximum operational frequency of proposed latch and previously reported CML latch is shown in Table 4.1. The proposed design can work with a gigabit frequency range of 16GHz with the maximum power dissipation of 0.280mW.

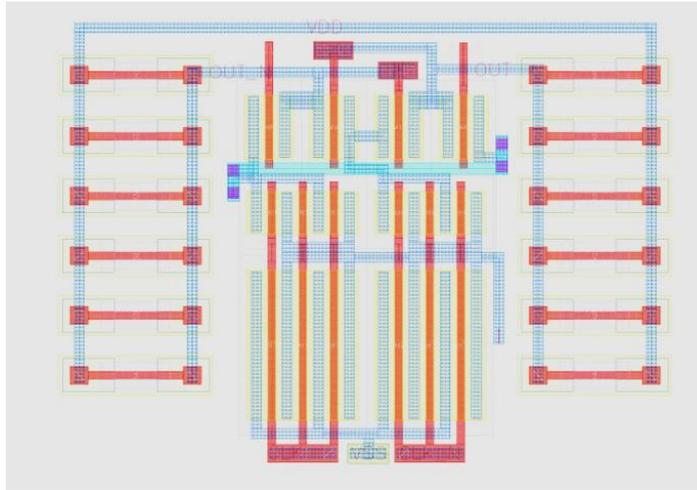


Figure 4.5 Layout of CML Latch

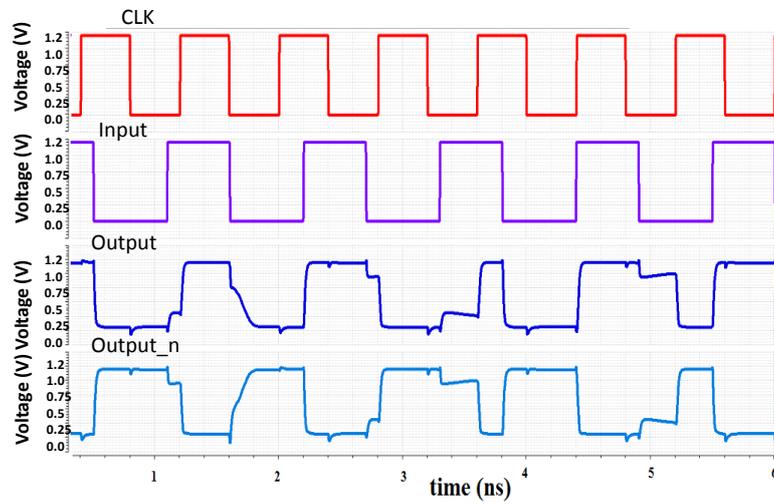
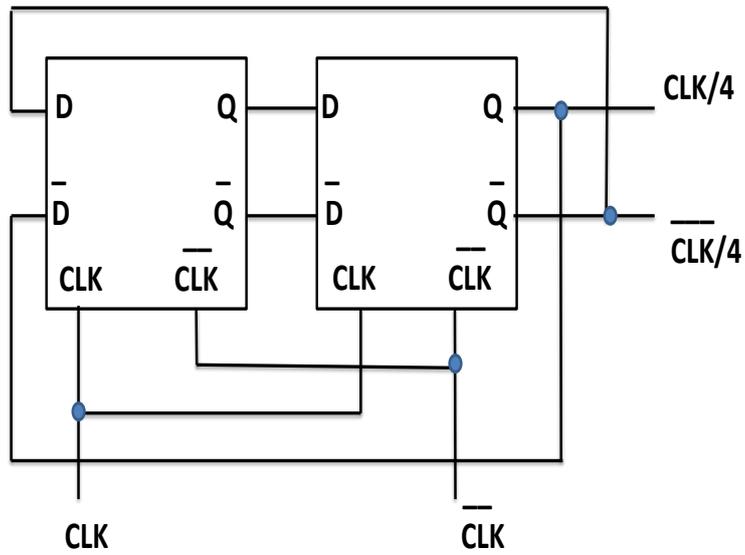


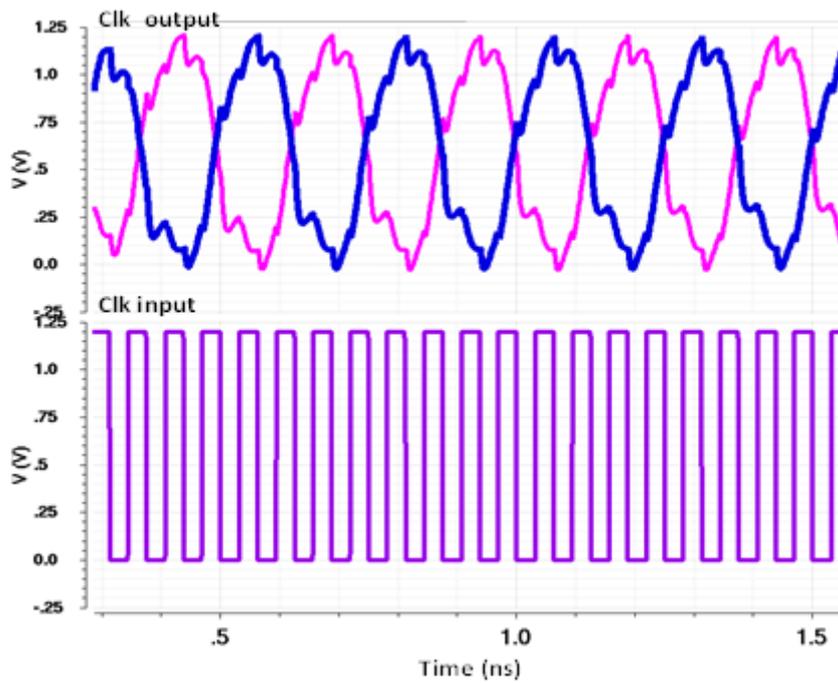
Figure 4.6 Proposed CML latch output at 1.25 GHz

Table 4.1 Comparative analysis with previous work

Latch Structure	Performances				
	Tech. (nm)	Power @ 1.25GHz (mW)	Maximum Frequency (GHz)	No. of Devices	Extra bias voltage
Conventional	180	0.180	8.5	9	No
Heydari <i>et al</i> [22]	180	0.262	14.3	14	Yes
Zhang <i>et al</i> [24]	130	0.182	15.2	10	No
This work	180	0.280	16	11	No



(a)



(b)

Figure 4.7 (a) Frequency divider (b) Post layout simulation of frequency divider.

As CML latches are widely used in a variety of circuits, one flip-flop based frequency divider circuit has been designed to verify its performance. In Figure 4.7 (a) two D flip-flops based frequency divider circuit is presented and the functionality of this frequency divider is with the supply voltage of 1.2 V. It divides the input frequency of 16 GHz into the divide-by-four ratios. The output voltage swing variation of the frequency divider is around 0.6 V.

4.7 Conclusion

The need of Current mode logic for high speed circuits is discussed in this chapter. The delay model and transistor sizing of proposed CML latch is also defined. These type of CML latches are very useful for the asynchronous type serial link transceivers. The next chapter describes the asynchronous wave pipelined transceiver using improved CML Latch.

Chapter 5

A Novel CML Latch Based Wave-Pipelined Asynchronous SerDes Transceiver for Low Power Application

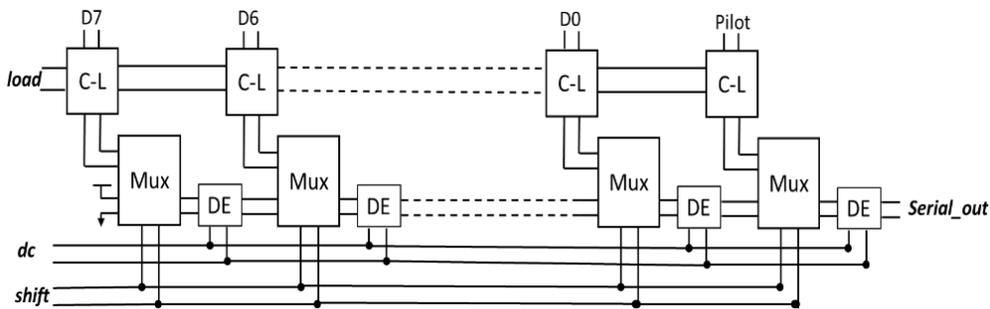
5.1 Introduction

In the present technology development billions of transistors are fabricated on a single chip, which improves the performance of circuits in terms of high data transmission speed and power consumption. This requirement of data transmission speed is achieved with the help of high-speed Transceivers. In this chapter, a high-speed asynchronous wave pipelined Serializer and Deserializer (SerDes) transceiver implemented using current mode logic (CML) has been presented. This asynchronous transceiver circuit does not require a clock and therefore it saves the large amount of power which is consumed in the PLL and frequency synthesizer circuits. Furthermore, the proposed design is built using CML which saves more power. CML circuit can be operated at relatively higher speed as compared to CMOS circuits which helps circuit in higher data rate applications. In spite of using conventional CML latch, a novel CML latch is proposed in our design to increase the speed. The circuit is implemented in standard CMOS 65nm technology. The total power consumed by the Serializer and Deserializer is 9.32mW, which is very less as compared to published related works. The proposed asynchronous SerDes transceiver operates at 18.1Gbps data transmission rate with low power dissipation.

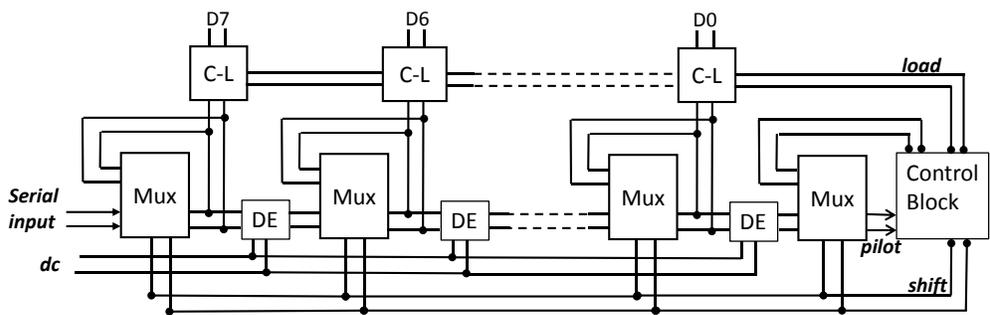
5.2 Proposed Serializer and Deserializer

The proposed asynchronous SerDes is designed using CML logic. Figure 5.1(a) shows the Serializer, in which load, delay control (dc) and shift are the

handshaking signals for serialization. Serializer circuit contains CML multiplexer, CML Latches (C-L) and Delay Element blocks. CML latches are controlled by the load signal, whereas the multiplexers are controlled using shift signal. CML latch inputs are connected to the $D7 \dots D0$ and *Pilot* for loading of parallel data and multiplexers are used to propagate received parallel data. To send the parallel data to the Serializer, load signal is kept high, which sends input data to input of the delay element (DE) through multiplexer. All delay elements are selected according to the state of dc signal and transfer the data to multiplexers. Multiplexers transfer the bit received from delay element depending on shift signal. At the end the serialized output is received along with one pilot bit. After arrival of Pilot bit at control block data transmission is stopped and loading of next bit stream at Serializer is initiated.



(a)



(b)

Figure 5.1 Asynchronous Transceiver (a) Serializer (b) Deserializer

The controlling in CML latch is maintained by load signal, whenever the load signal is high it transfers the parallel data to multiplexer blocks. The multiplexers

are controlled with shift signal. They are Shift signal turn ON The multiplexers are connected in such a manner that they are turned ON whenever the shift signal goes LOW. The load and shift signals are always turn ON their respective connected blocks. The load and shift signal always in opposite state to each other for proper transmission of data. Therefore, when load signal is HIGH, it turns ON the vertical CML latch to load parallel data and shift signal's LOW state to enable the multiplexer for data transmission.

Proposed asynchronous deserializer design is shown in Figure 5.1(b). It has same structure as of Serializer with same timing references to avoid jitter and noise. Serialized bit stream with prefix pilot bit received at Deserializer is passed through multiplexers, since delay control (dc) is wiped of all the data from Deserializer before bit stream enters Deserializer, thus all the mux will have zero at their input before the serial stream enters. When dc signal is low, data stream propagates through all multiplexer latches with pilot bit at starting. When pilot bit reaches to control block, it generates signal to stop the received signal and turns ON the CML latch. Since, the CML latches are turned OFF, they will maintain the respective bits at the input of CML latch and these latches pass the data information to the output.

5.3 CML latch and other building blocks

It's very challenging for a CMOS based circuit to be operated at MOS Device's transition frequency. Gigabit communication needs high speed signal in transceiver and should be abandoned to use PMOS devices. CMOS circuit's limitation to work in gigahertz high frequency makes Current mode logic (CML) most promising. CML circuits can work for high speed applications with low output swing. For the proposed asynchronous SerDes transceiver, CML latch is the basic building block [18-23].

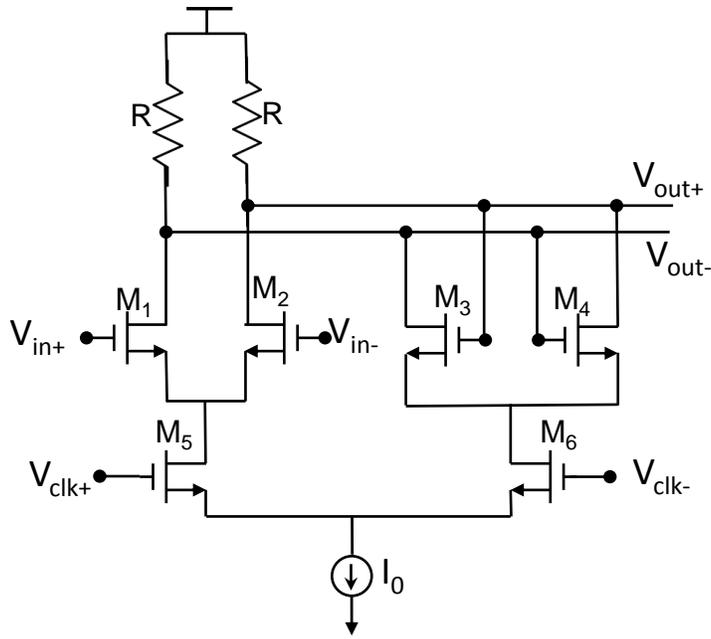


Figure 5.2 Conventional CML Latch

A conventional current mode logic latch works in a sample and hold stage. The conventional latch is shown in Figure 5.2. During sample stage, transistors M_1 , M_2 , & M_5 are operated, and for hold stage transistor M_3 , M_4 & M_6 are operated. Clock signal connected with M_5 & M_6 decides the stage of the latch. Sample stage works when V_{clk+} is HIGH, and hold stage works for HIGH V_{clk-} . Sink current I_0 is used to maintain the voltage swing of the CML output in high frequency conditions. For the limited gain of the conventional latch it is difficult to operate it in ultra-high frequency (UHF) application (>10 GHz) [22], therefore a new CML latch has been introduced with improved tail current Figure 5.3.

In proposed CML latch an additional parallel path for current flow has been introduced for sample and hold stages of operation. Clock signal V_{clk+} is HIGH during sample stage operation which turns ON the transistors M_5 - M_8 and allows more current to flow in additional tail branch. For the hold stage operation transistor pair M_6 - M_7 operates and the tail current flows through this regenerative pair transistor. These transistors produce high gain and stability for high speed application. The other advantage of this proposed design is its output offset

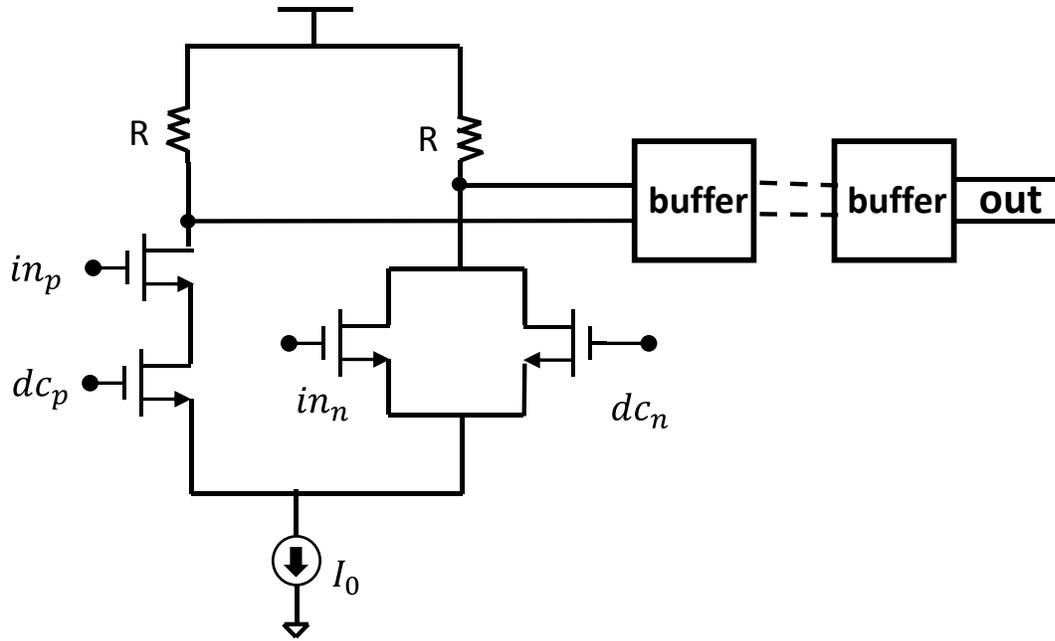


Figure 5.4 Delay Element (DE)

Control block is an important part of asynchronous CML SerDes. In asynchronous circuit, the data rate is bounded by the delay signal due to non-availability of clock signal. For this reason, the control block must switch the handshaking signal for proper data recovery. The proposed control block generates two handshaking signals, i.e. “shift” and “load” for proper functioning of Deserializer. Jaiswal *et. al.* [36] presented control block with fast propagation and optimum driving capabilities for control signal as shown in Figure 5.5. It consists *Pilot* hold circuit and buffer chain blocks to generate the handshaking signals. For fast switching of signal the multiplexers need to react as fast as possible, so parallel buffer chain blocks are used to generate multiple outputs. To overcome the voltage swing issue of propagating signal, larger current signal is employed in buffer chain.

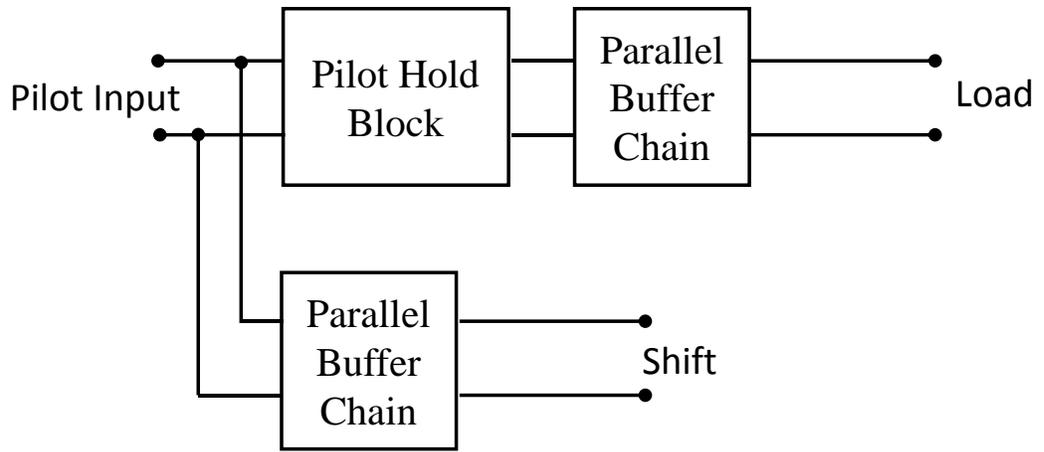


Figure 5.5 Control Block

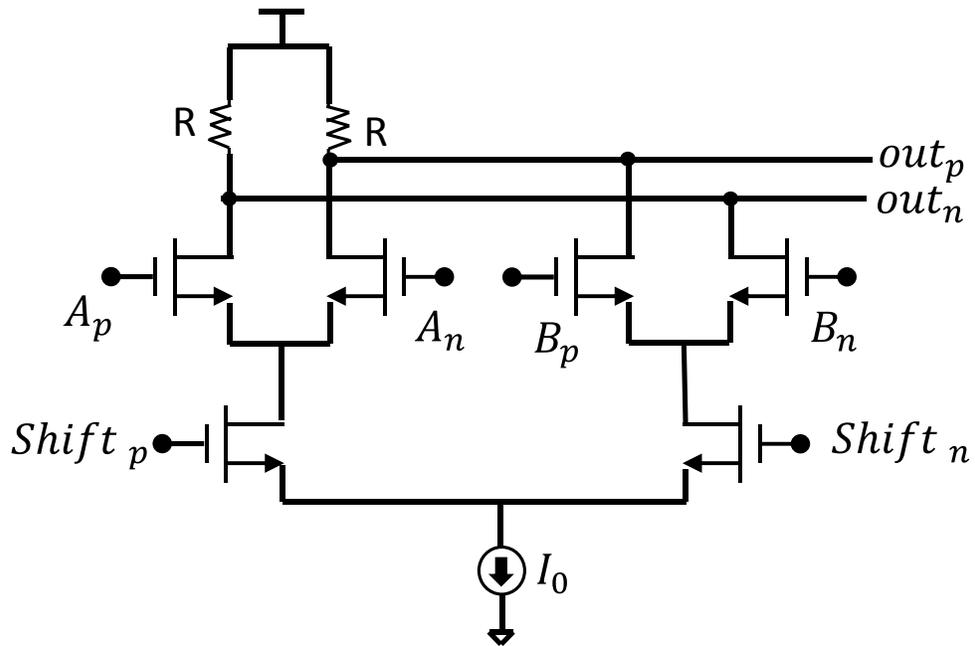


Figure 5.6 CML Mux

The CML multiplexer, as shown in Figure 5.6, works with select signals S_p & S_n and it is controlled by the shift signal. Initially, the shift signal is set to “1” such that all serialized bits inserted in Deserializer and the pilot bit is received at the control block. Control block then generates the shift= “0” to hold the information at each multiplexer and load = “1” to receive the deserialized data bits. The shift and load signals are opposite in nature. For logic”1”, shift signal turns OFF the propagation whereas load signal turns ON the CML latches and

opposite is true for logic “0”. Modified CML latch works with larger voltage swing, so at the output we get data bit with larger voltage swing without applying higher sink current. CML buffer and CML inverter are the important circuits used in buffer chain and delay element of control block. These buffers and inverters have the identical structures as shown in Figure 5.7. The basic difference between buffer and inverter is their output selection. The output of CML buffer is taken in inverted manner as compared to CML inverter.

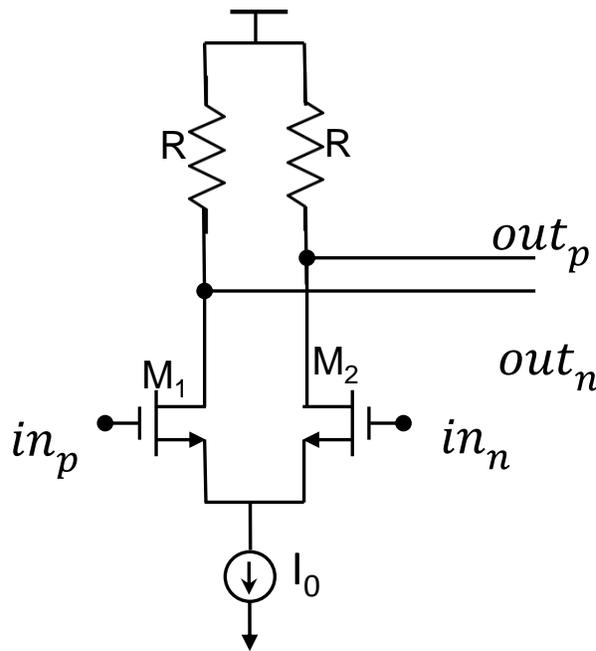


Figure 5.7 CML Inverter

As shown in Figure 5.1, the Serializer and Deserializer circuit blocks are controlled by the same *load* signal and *shift* signal. Therefore, loading of the parallel data at the Serializer and taking out of the parallel data at Deserializer takes place at the same time.

Before starting of data transmission switching on of the start-up circuit is required. The initialization circuit as shown in Figure 5.8 [36] is placed with the control block input to make the system in reset condition. The circuit consists of an NMOS transistor along with a resistance and a capacitance. When the circuit is

switched on, this NMOS capacitors generates an active HIGH and an active LOW signal for a small duration of time so that the circuit starts correctly.

Since the SerDes transceiver using current mode logic, therefore the input which is in CMOS logic should be first converted to CML. This study has used differential CML inverter as CMOS to CML converter to achieve such requirements. In this circuit, we have applied CMOS signal to the InP of CML converter and inverted CMOS signal to the InN of CML converter. After completion of receiving the information at the receiver end, to ensure that the output is compatible with CMOS signal, a CML to CMOS converter is used. As shown in Figure 5.9, CML to CMOS converter is designed using a push-pull output Operational amplifier with regenerative inverter blocks.

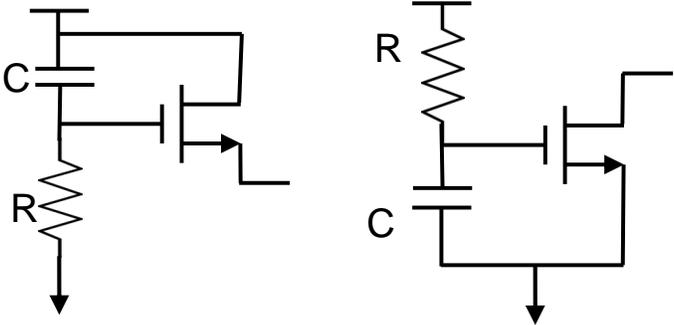


Figure 5.8 Initial state circuits

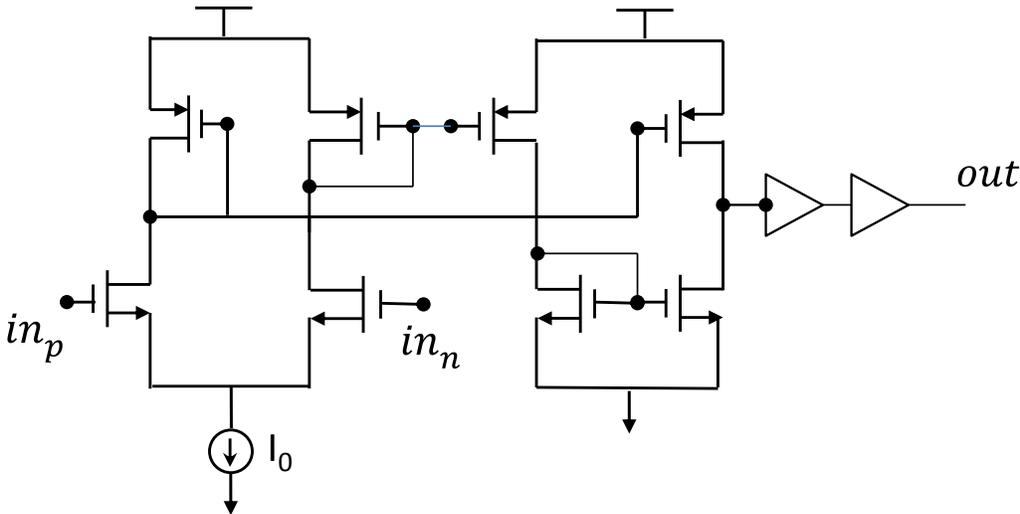


Figure 5.9 CML to CMOS Converter

5.4 Results

In this section, the modified CML latch circuit is compared with the conventional CML latch and it shows the larger output voltage swing as shown in Figure 5.10. Conventional latch shows the 0.4V output swing and works between 0.7V to 1.1V and the modified latch has 0.9V output voltage swing and works between 0.2V to 1.1V supply range. Results are captured while applying input voltage swing from 0 to 1.2V.

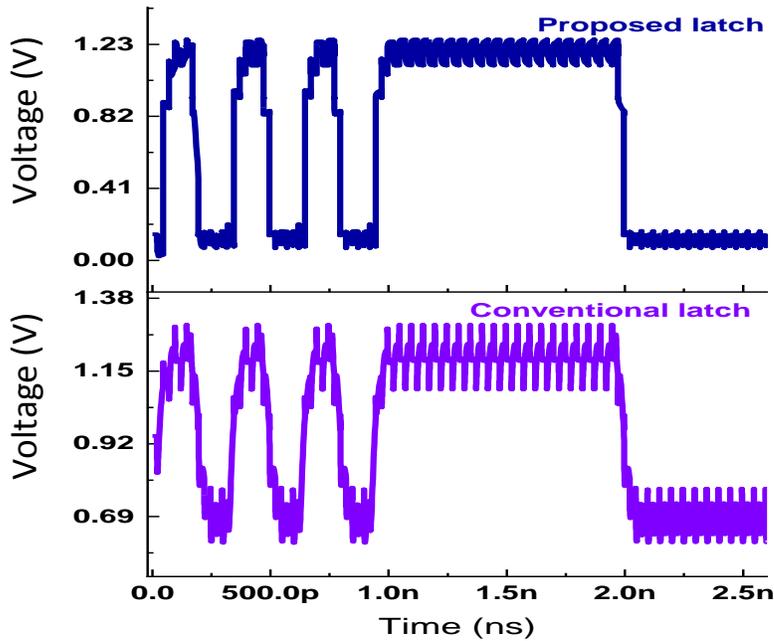


Figure 5.10 CML latch Output waveform (a) Proposed latch (b) Conventional latch

The novel CML latch based asynchronous SerDes transceiver is designed in previous work. PVT corners simulations are also performed to ensure the stable operation of the transceiver. The circuit is designed and simulated using Spectre with standard 65nm CMOS technology. Serialized bit stream (for the input 10101010) is shown in the Figure 5.11. As this circuit is implemented using CML logic, final serialized bit having voltage swing between 0.6 to 1.2V. The first upper waveform in the figure shows the differential *shift* signal, which is responsible for transmission of serial information. The bottom waveform shows the complete serialized output for the input 10101010. All other outputs of

multiplexers are shown in between second to ninth waveform. The Figure 5.12 shows output of Deserializer with the voltage swing between 0.7 to 1.18V.

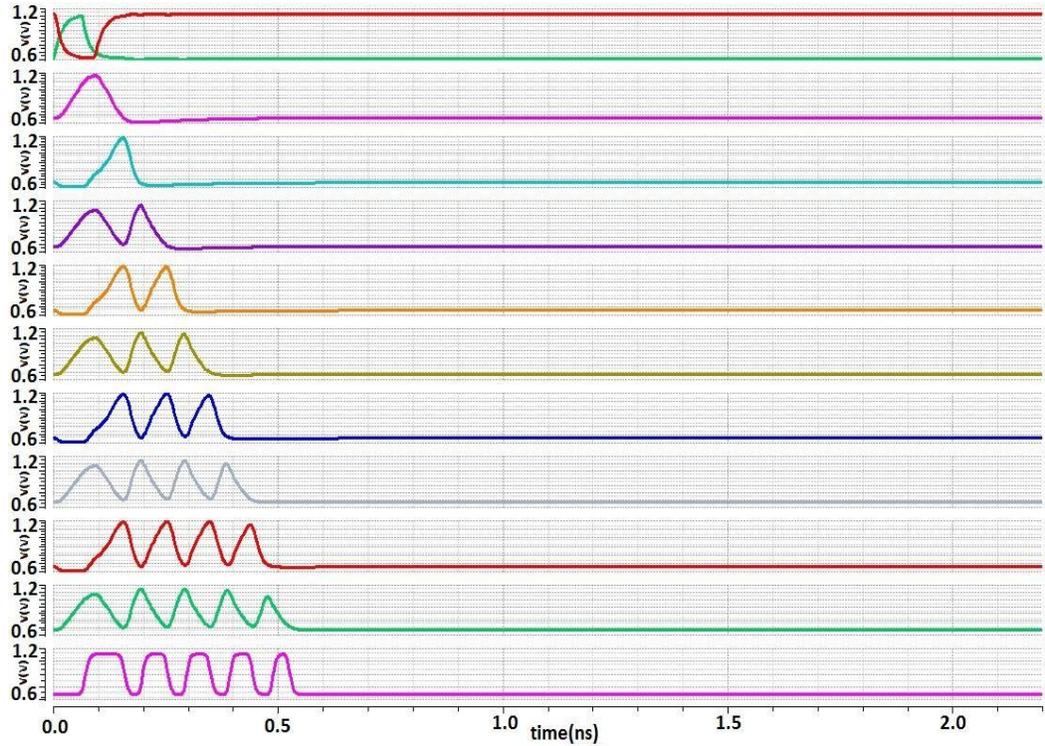


Figure 5.11 Serializer output for the input bits 10101010

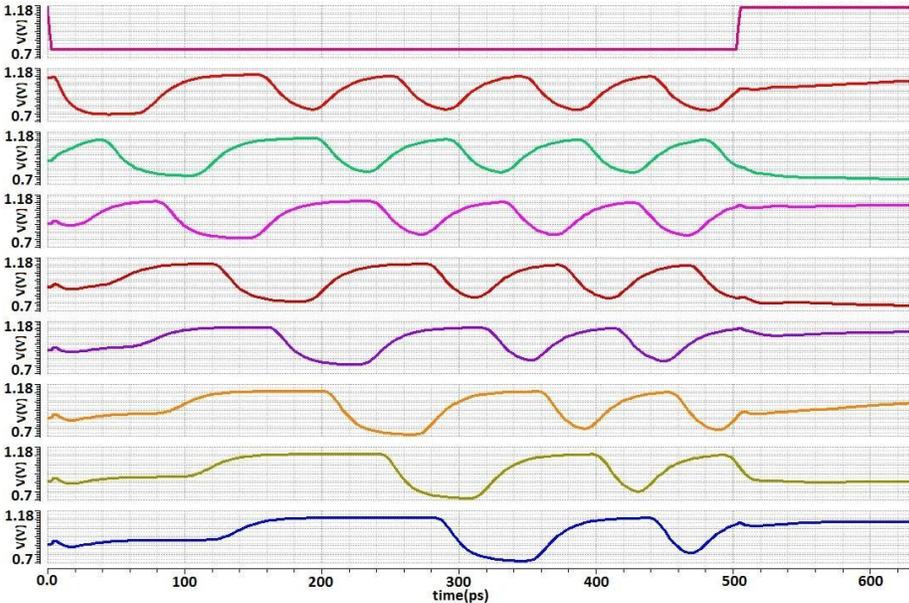


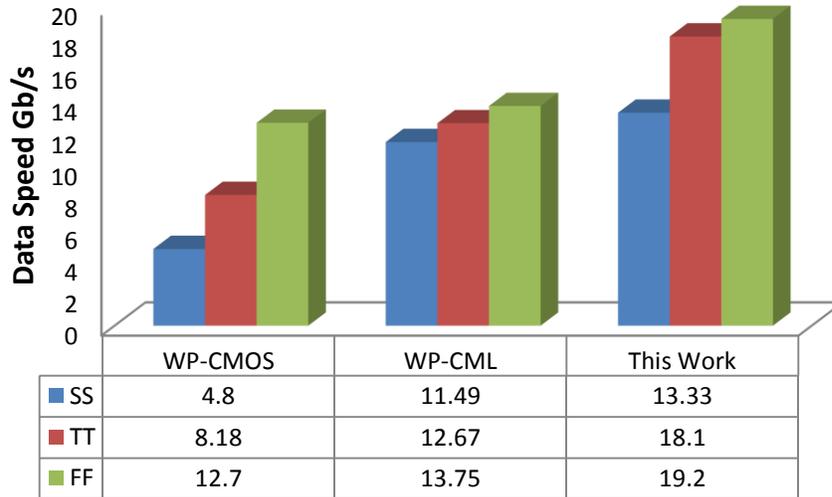
Figure 5. 12 Deserialized output for the bits 10101010

The asynchronous CML based SerDes gives a bit width of 55.24ps, corresponding to the data rate of 18.1Gbps. The proposed circuit has dynamic power consumption of 9.32mW. The comparison of proposed design with literature is given in the Table 5.1.

Table 5.1 Comparison of SerDes Architectures

Architecture	Technology(nm)	Speed (Gbps)	Power (mW)
CMOS-CML [40]	45/65	10	10/106
Self-timed [32]	65	12	15.5
Self-timed [33]	65	16	18.1
WP-CML [36]	65	12.67	14.3
This work	65	18.1	9.32

Table 5.2 PVT corner of various SerDes transceiver



Process Corner analysis is also compared with other published results. For SS process corner, 1.08V supply voltage and 125⁰C temperature is selected, while for

FF corner 1.32V supply voltage and -45°C temperature is chosen. For TT corner, 1.2V supply voltage is chosen at room temperature. Table 5.2 shows that, the proposed design works with higher data transmission rate in different process corner conditions.

As compared to WP-CML, it shows the 42.8% higher data transmission rate in typical conditions. In SS corner conditions the proposed design is also better than WP-CMOS and WP-CML techniques. In FF PVT Corner the proposed technique has shown 39% improvement from WP-CML and 50% from WP-CMOS. Hence, the proposed SerDes design can work better in different corner conditions.

Chapter 6

Conclusions and Future Works

6.1 Conclusions

In this thesis, all the proposed design techniques simulations are carried out using Cadence and Mentor graphics tools.

The wave combining and de-combining block based SerDes transceiver link is designed and analysed. It helps in connecting the separate input streams and its levelled transmission with proper driving capabilities. The two-level signalling improves the signal bits communication and signal recovery at receiver. Single-ended transmission line used in the transmission of the signal, which shows 10% jitter at output de-serialized stream. Further, the CTLE maintains the 400mV signal offset window by that output signal readily recovered at the receiver end.

Additionally, the thesis also shows the improved on-chip low voltage, high-speed CML latch designed using 180nm standard CMOS technology with a 1.2V supply. The delay model of the proposed latch and reported design has been developed and presented. The overall time constant of the proposed circuit is described and compared with the reported latch structure. The performance of the proposed latch design is checked for power dissipation and offset swing at the 1.25GHz clock frequency. The Output voltage swing range of this design is 0.6 V, which is higher than the conventional latch. Hence, the proposed design has the advantage to work with a large tail current condition in both tracking and latching mode of operation. Additionally, this design provides an output voltage swing of around 0.6V.

Furthermore, the thesis reports a new wave pipelined technique for asynchronous serial link transmission. With the help of Improved CML latch design the high-

speed serial link is presented, which results in improved voltage swing, reduction of error and speed boosting. This design also has advantages in the form of reduced power dissipation, when compared to other structures. In this design approach we achieved 18.1Gbps data transmission speed with low dynamic power dissipation of 9.32mW in 65nm technology. Comparative analysis with different process corner was also verified with the proposed design and it was found that it works between 13.33Gbps to 19.1Gbps in different corner conditions with low power dissipation and is suitable for the higher data transmission rate.

6.2 Future works

The research vision of this thesis is to design circuit blocks for high speed serial links. CML based latch design is proposed and simulation-based results are studied. The design is verified using some example for frequency divider and asynchronous based transceiver links, it helps this thesis to propose half circuit architecture-based wave combiner and decombiner approach for synchronous type of high speed serial links. This thesis deals with different serial link circuit blocks design with external clock signals, therefore, for future work is to complete SerDes with PLL design.

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