DESIGN OPTIMIZATION OF DOUBLE GATE JUNCTIONLESS MOSFET FOR ENHANCED SHORT CHANNEL IMMUNITY

Ph.D. Thesis

By

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DISCIPLINE OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

NOVEMBER 2019

DESIGN OPTIMIZATION OF DOUBLE GATE JUNCTIONLESS MOSFET FOR ENHANCED SHORT CHANNEL IMMUNITY

A THESIS

Submitted in partial fulfillment of the
requirements for the award of the degree
of
DOCTOR OF PHILOSOPHY

by

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DISCIPLINE OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE
NOVEMBER 2019

INDIAN INSTITUTE OF TECHNOLOGY INDORE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **DESIGN OPTIMIZATION OF DOUBLE GATE JUNCTIONLESS MOSFET FOR ENHANCED SHORT CHANNEL IMMUNITY** in the partial fulfillment of the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY** and submitted in the **DISCIPLINE OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from December 2015 to November 2019 under the supervision of Dr. Abhinav Kranti, Professor, Discipline of Electrical Engineering, Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

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This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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Date: May 22, 2020

ACKNOWLEDGEMENTS

Foremost, I would like to express my sincere gratitude to my Ph.D. thesis supervisor, Prof. Abhinav Kranti, for providing me an opportunity to join his research group at IIT Indore. I am deeply grateful for his guidance, motivation, positive criticism, and feedback towards my Ph.D. work. His support and effort have made me accomplish the research objectives in this thesis.

I sincerely thank my PSPC members, Dr. Prabhat Kumar Upadhyay, and Dr. Bhupesh Kumar Lad, for their insightful remarks on the Ph.D. work from various perspectives.

I gratefully acknowledge IIT Indore for providing me the necessary infrastructures and research facilities. I am thankful to all the faculty members of the Discipline of Electrical Engineering for their kind support during my Ph.D. work. I greatly appreciate all the staff members of IIT Indore for their generous help concerning academics and accommodations.

I express my sincere gratitude to the Ministry of Electronics and Information Technology (MeitY), Government of India, for providing fellowship grant under Visvesvaraya Ph.D. scheme for Electronics and IT. This thesis is an outcome of the research and development work undertaken in the project under the Visvesvaraya Ph.D. scheme of MeitY, being implemented by Digital India Corporation. I would also like to acknowledge Council of Scientific and Industrial Research (CSIR) for providing the international travel grant to present my research paper.

I am deeply grateful to my colleagues Bhuvaneshwari, Manish and Nupur for their kind support and motivation during the research work. I would also like to extend my gratitude towards other colleagues Praveen, Hasan, Sandeep, Mukta, Saurabh, Pranjal, Siddharth, Khushboo and Pranay for their kind co-operation and healthy working environment in the research lab.

I would like to express my heartfelt gratitude to my friend Abhishek for motivating me to pursue my career in research. A special thanks to my friend Lichchhavi for her homely care and pleasant stay at IIT Indore. I cannot forget to thank my other friends Shweta, Krishnendu, Pooja, Kalyani, Sujata, Komal, Anjali, Anubha, Nishant, Uday and Biswajit for their friendship and co-operation at IIT Indore.

I would like to express my deepest gratitude to my family members: my father Mr. Vinod Jaiswal, mother Mrs. Sandhya Jaiswal, younger sister Ritika and younger brother Vibhor, for their unconditional love, encouragement and support during the Ph.D. work. I am also heartily

grateful to my cousins Niharika and Abhijeet for their timely help and care during paper presentations related to the Ph.D. work.

At last, I am wholeheartedly grateful to Almighty God for giving me skills, strength and faith for this crucial phase of my life.

Nivedita Jaiswal

Dedicated to my family

ABSTRACT OF THE DISSERTATION

Design Optimization of Double Gate Junctionless MOSFET for Enhanced Short Channel Immunity

The semiconductor industry has continuously been involved in the development and production of digital Integrated Circuits (ICs) for High Performance (HP) and Low Power (LP)/Ultra Low Power (ULP) logic applications. Due to the very different nature of constraints, LP compatible devices widely differ from the HP transistor architectures. The prime goal of LP technology is to trade-off speed performance for low standby power or low off-current (I_{OFF}). A scaled-down transistor possessing ideal subthreshold swing (S) and a low value of Drain Induced Barrier Lowering (DIBL) is desirable for LP technology. However, due to the downscaling of the gate length (L_g), the undesirable Short-Channel Effects (SCEs) are observed in the characteristics of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). SCEs cause a reduction in threshold voltage (V_{th}) with decreasing L_g (i.e. threshold voltage roll-off, dV_{th}) and increasing V_{ds} (i.e. DIBL), as well as degradation in S. A feasible solution to alleviate SCEs is to enhance electrostatic control over the channel region through multiple gates in a transistor. Multi-gate Junctionless (JL) transistors can be potential alternatives to conventional MOSFET for downscaling owing to the absence of traditional *pn* junctions, relaxed fabrication processes and thermal budgets, efficient control over the channel by multiple gates, and enhanced immunity towards SCEs. Literature has shown the potential of heavily doped (10^{19} cm^{-3}) JL MOSFET over conventional MOSFET for LP logic technology than for HP logic technology applications. A moderately doped JL MOSFET (10^{18} cm^{-3} to 5×10^{18} cm^{-3}) can further improve LP performance, reduce parameter variability and relax gate workfunction requirement. Dedicated optimizations of underlap regions and sidewall spacers in JL FETs are essential for LP technologies. Recently, JL MOSFET with innovative Shell Doping Profile (SDP) has experimentally demonstrated improved S, higher I_{ON}/I_{OFF} ratio, and lower parameter sensitivity than uniformly doped JL transistors, thus indicating favorable prospects for downscaling and LP technology.

In conventional JL transistors, due to the identical dopant type (preferably high doping) throughout the semiconductor film, the extension of depletion regions outside the gated portion can take place in the off-state. Consequently, effective channel length (L_{eff}) becomes longer than L_g. An elongated L_{eff} in the subthreshold operating regime can suppress SCEs in these transistors and has the potential for LP technology while enabling downscaling. This unique and inherent property of JL transistors exists in mostly all JL architectures, whether traditional structures [11],

modified structures with Gate-Source/Drain (G-S/D) underlap, or novel JL FET with SDP. However, the value of L_{eff} in the subthreshold regime varies in different topologies. The thesis provides comprehensive and dedicated approaches to estimate as well as suppress SCEs in various Double Gate (DG) JL architectures (DG JL with G-S/D underlap and SDP), by adequately capturing L_{eff} in the subthreshold regime. The thesis also identifies critical design parameters that can be optimized for superior short channel performance, thereby providing optimally designed DG JL transistor for LP subthreshold logic applications.

A five-region semi-analytical model for subthreshold channel potential is developed to adequately capture L_{eff} for symmetric mode-operated DG JL MOSFET at any gate-underlap length. The five-region model can be adapted into three or four regions depending upon the lateral extent of depletion into the G-S/D underlap. The transfer characteristics obtained from approximate analytical solutions for subthreshold drain current (I_{ds}) are utilized to extract the parameters indicating SCEs (dV_{th}, DIBL and S). The developed model results reasonably agree with simulation data. The thesis presents that channel doping and underlap length are two critical parameters that affect SCEs. An optimally long underlap along with moderate doping (10^{18} cm^{-3}) can be used as an advantage to improve SCEs at sub-50 nm gate lengths.

The thesis develops a semi-analytical model to estimate SCEs for independent gate-operated asymmetric DG structure with G-S/D underlap. The model considers non-identical values for front and back gate workfunctions and oxide thicknesses, and S/D underlap lengths. The modeled I_{ds}, V_{th}, and S adequately agree with the simulation data. The thesis highlights the role of back gate bias (V_{bg}), channel doping (N_d) and underlap length (L_{un}) to improve the device performance through optimization of off-current (I_{OFF}), V_{th} and S. Results propose an optimum choice of negative V_{bg} together with moderate N_d and sufficiently long L_{un} for short channel asymmetric DG JL device. The generalized model formalism in the subthreshold regime can be utilized to optimize the self-aligned DG JL device for LP subthreshold logic applications.

The thesis also presents a semi-analytical model for estimating L_{eff}-dependent SCEs in DG JL MOSFET with SDP (referred to as Core-Shell (CS) DG JL MOSFET). The developed model reasonably captures the channel potential and SCEs in CS DG JL MOSFETs for varying L_g, core thickness (T_{core}), shell doping (N_d) and biases. The modeled V_{th}, DIBL and S, derived from the transfer characteristics, are in good agreement with the simulation results. The thesis investigates the impact of N_d and T_{core} on the short channel performance of the CS DG JL MOSFET. Results suggest that the moderate N_d – narrow T_{core} pair can be preferred over high N_d – wide T_{core} for similar SCEs but at reduced V_{th} sensitivity.

LIST OF PUBLICATIONS

A. Peer-reviewed Journals:

1. **Nivedita Jaiswal** and Abhinav Kranti, "A Model for Gate-Underlap Dependent Short Channel Effects in Junctionless Transistor," **IEEE Transaction on Electron Devices**, vol. 65, no. 3, pp. 881-887, Mar. 2018.
2. **Nivedita Jaiswal** and Abhinav Kranti, "Modeling Short-Channel Effects in Asymmetric Junctionless MOSFETs With Underlap," **IEEE Transactions on Electron Devices**, vol. 65, no. 9, pp. 3669-3675, Sep. 2018.
3. **Nivedita Jaiswal** and Abhinav Kranti, "Modeling Short-Channel Effects in Core-Shell Junctionless MOSFET," **IEEE Transactions on Electron Devices**, vol. 66, no. 1, pp. 292-299, Jan. 2019.

B. Proceedings in International Conferences:

1. **Nivedita Jaiswal** and Abhinav Kranti, "Influence of Gate-Source/Drain Underlap on Performance of Junctionless Transistor," **In Abstract of 6th International Symposium on Integrated Functionalities (ISIF 2017)**, New Delhi, India, Dec. 2017, p. 126.
2. **Nivedita Jaiswal** and Abhinav Kranti, "Scalability and V_{th} Sensitivity Assessment of Core-Shell Junctionless MOSFET," **In Extended Abstract of International Conference on Solid State Devices and Materials (SSDM 2019)**, Nagoya, Japan, Sep. 2019, pp. 653-654.

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NOMENCLATURE

Symbols	Description	Units
a, b	*Arbitrary integration limits*	-
$a_0, b_0, c_0,$	*Coefficients in parabolic potential approximation*	*V*
$a_1, b_1, c_1,$	*Coefficients in parabolic potential approximation*	*V/nm*
$a_1, b_1, c_1,$	*Coefficients in parabolic potential approximation*	V/nm^2
A_1, A_2	*Coefficients in generic solution for Region-I*	*V*
B_1, B_2	*Coefficients in generic solution for Region-IV*	*V*
C_1, C_2	*Coefficients in generic solution for Region-V*	*V*
C_{ob}	*Back gate oxide capacitance per unit area*	F/cm^2
C_{of}	*Front gate oxide capacitance per unit area*	F/cm^2
C_{ox}	*Gate oxide capacitance per unit area*	F/cm^2
d	*Shell depth (or) thickness of shell region*	*nm*
D_1, D_2	*Coefficients in generic solution for top shell potential along the y-direction*	*V*
d_D	*Lateral extension of depletion regions beyond the gate edges into the drain side*	*nm*
d_{Dmax}	*Maximum allowable d_D under long channel approximation*	*nm*
d_S	*Lateral extension of depletion regions beyond the gate edges into the source side*	*nm*
d_{Smax}	*Maximum allowable d_S under long channel approximation*	*nm*
dV_{th}	*Threshold voltage roll-off*	*mV*
E_1	*Coefficient in generic solution for core potential along the y-direction*	*unitless*
E_2	*Coefficient in generic solution for core potential along the y-direction*	*nm*
E_c	*Conduction band energy*	*eV*
E_D	*Electric field at $x = L_g + d_D$*	*V/cm*
E_{De}	*Electric field at $x = L_g + L_{De}$*	*V/cm*
$E_{f,s}$	*Electron Fermi-level at the source end*	*eV*
E_g	*Bandgap energy of Si*	*eV*

E_i	*Intrinsic Fermi-level energy*	*eV*
E_{ref}	*Reference energy*	*eV*
E_S	*Electric field at x = -d_S*	*V/cm*
E_{Se}	*Electric field at x = -L_{Se}*	*V/cm*
E_v	*Valence band energy*	*eV*
E_y	*Vertical component of electric field*	*MV/cm*
f	*Operating frequency*	*Hz*
F_1, F_2	*Coefficients in generic solution for bottom shell potential along the y-direction*	*V*
F_I, F_{II}, F_{III},	*Notations used to represent integrals along the x-direction in subthreshold drain current expression*	*unitless*
g, h	*Notations used in general solution for channel potential*	*V*
G_I, G_{II}, G_{III}	*Notations used to represent integrals along the y-direction in subthreshold drain current expression*	*nm*
$H(z)$	*Arbitrary function dependent on variable 'z'*	-
i	*Notations used to indicate regions I, II or III*	-
$I_{ds,th}$	*Drain current corresponding to threshold voltage*	*μA*
I_{OFF}	*Off-current*	*nA*
I_{ON}	*On-current*	*mA*
j	*Notations used to indicate regions II and III*	-
k	*Boltzmann's constant*	*J/K*
k_1	*Notation used in equations for calculating L_{Se} and L_{De}*	*nm^{-1}*
k_2	*Notation used in equations for calculating L_{Se} and L_{De}*	*unitless*
k_{3s}, k_{3d}, k_4	*Notations used in equations for calculating L_{Se} and L_{De}*	*nm*
k_{5s}, k_{5d}	*Notations used in equations for calculating L_{Se} and L_{De}*	*nm^2*
k_a, k_c	*Notations used in transcendental equations in d_S and d_D*	*V/nm^2*
k_b, k_e, k_g	*Notations used in transcendental equations in d_S and d_D*	*V/nm*
k_d, k_f, k_{h1}, k_{h2}	*Notations used in transcendental equations in d_S and d_D*	*V*
L_{eff}	*Effective channel length*	*nm*
L_D	*Gate-to-drain underlap length*	*nm*
L_{De}	*Lateral drain extension at the centre of the undoped core*	*nm*
L_{Dext}	*Undoped drain underlap length*	*nm*
L_g	*Gate length*	*nm*
$L_{g,L}$	*Gate length for long channel device*	*nm*

$L_{g,S}$	*Gate length for short channel device*	*nm*
L_S	*Gate-to-source underlap length*	*nm*
L_{Se}	*Lateral source extension at the centre of the undoped core*	*nm*
L_{Sext}	*Undoped source underlap length*	*nm*
L_{un}	*Gate-source/drain underlap length*	*nm*
N_a	*Acceptor-type doping concentration*	cm^{-3}
N_C	*Effective density of states for electrons conduction band*	cm^{-3}
N_0	*Core doping*	cm^{-3}
N_d	*Donor-type doping concentration (or) shell doping*	cm^{-3}
n_e	*Electron concentration*	cm^{-3}
N_{eq}	*Equivalent core doping seen by the gate in central core region*	cm^{-3}
n_i	*Intrinsic carrier concentration in Si*	cm^{-3}
n_{i0}	*Intrinsic carrier concentration in Si core region*	cm^{-3}
n_{id}	*Intrinsic carrier concentration in Si top/bottom shell region*	cm^{-3}
N_{sd}	*Source/Drain donor-type doping*	cm^{-3}
N_V	*Effective density of states for holes in valence band*	cm^{-3}
q	*Electronic charge*	*C*
S	*Subthreshold swing*	*mV/dec*
S_1	*Subthreshold swing for low drain bias case*	*mV/dec*
S_2	*Subthreshold swing for high drain bias case*	*mV/dec*
S_L	*Subthreshold swing for long channel device*	*mV/dec*
S_S	*Subthreshold swing for short channel device*	*mV/dec*
T	*Temperature*	*K*
T_{box}	*Buried gate oxide thickness*	*nm*
T_{core}	*Thickness of core region*	*nm*
T_{ox}	*Gate oxide thickness*	*nm*
T_{oxb}	*Back gate oxide thickness*	*nm*
T_{oxf}	*Front gate oxide thickness*	*nm*
T_{si}	*Si film thickness*	*nm*
V_{bg}	*Back gate voltage*	*V*
V_{biD}	*Built-in potential corresponding to channel doping* N_d	*V*
$V_{bi,eff}$	*Effective built-in potential*	*V*
V_{biSD}	*Built-in potential corresponding to S/D doping* N_{sd}	*V*
V_D	*Potential at* $x = L_g + d_D$	*V*

V_{De}	*Potential at* $x = L_g + L_{De}$	*V*
V_{ds1}	*Low drain bias*	*V*
V_{ds2}	*High drain bias*	*V*
V_f	*Electron quasi-Fermi potential*	*V*
V_{FB}	*Flatband voltage with respect to Fermi level of bulk silicon*	*V*
V_{fb}	*Flatband voltage of gate with respect to intrinsic silicon*	*V*
$V_{fb,bg}$	*Flatband voltage of back gate with respect to intrinsic silicon*	*V*
$V_{fb,fg}$	*Flatband voltage of front gate with respect to intrinsic silicon*	*V*
V_{fg}	*Front gate voltage*	*V*
V_{gs}	*Gate voltage/bias*	*V*
V_S	*Potential at* $x = -d_S$	*V*
V_{Se}	*Potential at* $x = -L_{Se}$	*V*
V_T	*Thermal voltage*	*mV*
V_{th}	*Threshold voltage*	*V*
V_{th1}	*Threshold voltage for low drain bias case*	*V*
V_{th2}	*Threshold voltage for high drain bias case*	*V*
$V_{th,L}$	*Threshold voltage for long channel device*	*V*
$V_{th,S}$	*Threshold voltage for short channel device*	*V*
W_g	*Gate (channel) width*	*µm*
x	*Lateral direction*	-
y	*Vertical direction*	-
y_m	*Position of subthreshold conduction along y-direction*	*nm*
β	*Reciprocal of thermal voltage,* V_T	V^{-1}
Δ	*Spacing between n+1 samples in trapezoidal rule*	-
ΔS	*Degradation in subthreshold swing*	*mV/dec*
ΔV_{bi}	*Change in built-in potential between* V_{biSD} *and* V_{biD}	*mV*
ε_{ox}	*Permittivity of gate oxide*	*F/cm*
ε_{si}	*Permittivity of silicon*	*F/cm*
κ	*Dielectric constant*	*unitless*
λ_D	*Extrinsic Debye length*	*nm*
λ_{Dd}	*Extrinsic Debye length in shell region*	*nm*
λ_{D0}	*Extrinsic Debye length in core region*	*nm*
λ_N	*Natural length*	*nm*
λ_γ	*Natural length at any location* $y = \gamma$	*nm*

μ_n	*Mobility of electrons*	$cm^2/V\text{-}s$
μ_{nd}	*Electron mobility in shell region*	$cm^2/V\text{-}s$
μ_{n0}	*Electron mobility in core region*	$cm^2/V\text{-}s$
η_S, η_D	*Notations used in general solution for channel potential*	V
φ_{bg}	*Back gate metal workfunction*	V
φ_{fg}	*Front gate metal workfunction*	V
φ_g	*Gate metal workfunction*	eV
ϕ_{bg}	*Effective back gate voltage*	V
ϕ_{fg}	*Effective front gate voltage*	V
ϕ_{gs}	*Effective gate voltage*	V
χ_{si}	*Electron affinity's in Si*	eV
ψ, Φ	*Electrostatic potential*	V
ψ_b	*Back surface potential*	V
ψ_C	*Central potential*	V
ψ_f	*Front surface potential*	V
ψ_{Long}	*Long channel central potential*	V
$\psi_{Long,\gamma}$	*Long channel central potential at any location* $y = \gamma$	V
ψ_m	*Channel potential at* $y = y_m$	V
ψ_S	*Surface potential*	V
ψ_γ	*Channel potential at any location* $y = \gamma$	V

ACRONYMS

Abbreviation	Description
1D	*One-dimensional*
2D	*Two-dimensional*
3D	*Three-dimensional*
BTBT	*Band-to-Band Tunneling*
CB	*Conduction Band*
CMOS	*Complementary Metal Oxide Semiconductor*
CS	*Core-Shell*
CRV	*Contact Resistivity Variability*
CSG	*Cylindrical Surrounding Gate*
DG	*Double Gate*
DIBL	*Drain Induced Barrier Lowering*
Eq.	*Equation*
FET	*Field-Effect Transistor*
Fig.	*Figure*
G-S/D	*Gate-Source/Drain*
GAA	*Gate-All-Around*
HfO_2	*Hafnium oxide*
HP	*High Performance*
HVM	*High Volume Manufacturing*
IC	*Integrated Circuit*
IoT	*Internet-of-things*
IM	*Inversion Mode*
JL	*Junctionless*
LP	*Low Power*
MOSFET	*Metal Oxide Semiconductor Field-Effect Transistor*
mM	*more Moore*
n	*Donor-type*
NMOS	*n-type MOSFET*
NW	*Nanowire*

p	*Acceptor-type*
PE(s)	*Poisson's Equation(s)*
PMOS	*p-type MOSFET*
PPAC	*Performance, Power, Area and Cost*
QCE	*Quantum Confinement Effect*
RDFs	*Random Dopant Fluctuations*
S/D	*Source/Drain*
SDP	*Shell Doping Profile*
SCEs	*Short Channel Effects*
SDEs	*Source/Drain Extensions*
SG	*Single Gate*
SiGe	*Silicon-Germanium*
Si	*Silicon*
SiO_2	*Silicon dioxide*
SoC	*System-on-Chip*
SOI	*Silicon-on-Insulator*
SP	*Standard Performance/Power*
TCAD	*Technology Computer Aided Design*
TG	*Triple Gate or Tri-gate*
ULP	*Ultra Low Power*
VB	*Valence Band*
WFV	*Workfunction Variability*

Chapter 1

Introduction

1.1 MOTIVATION

The progressions in semiconductor industry are contributed by the farsighted vision of Gordon E. Moore, who projected that the transistors' density in an Integrated Circuit (IC) doubles every two years, which was later revised to 18 months [1], [2]. Since 1965, the famous 'Moore's law' has motivated the semiconductor industry to achieve smaller, denser and cheaper chips with higher computing performance, lower power, improved reliability and enhanced functionalities every couple of years [3]-[5]. Moore's law has also guided the semiconductor industry to define future goals for research and development of semiconductor devices [5]. The ever-shrinking of transistor dimensions has continued to transform the technology for over half-a-century extending from smartphones to supercomputers [3], [4]. Dennard's constant field scaling theory, proposed in 1974 [6], provided necessary assistance to fulfill criteria laid down by Moore's law until the early 2000s [7], [8]. Traditionally, downscaling has been adequate to obtain efficient ICs in terms of density, power, speed, functionality, etc., but is no longer viable in sub-50nm regimes due to the technological challenges in transistor scaling, interconnection, lithography, and circuit and memory designs [9]-[11]. In the present scenario, it is becoming increasingly challenging to keep pace with Moore's scaling projection. Thus, the semiconductor industry is in search of 'more Moore' technologies [12]-[15].

1.1.1 More Moore

Instead of relying on the inherent benefits achieved by dimensional scaling, more Moore (mM) focuses on the advanced Complementary

Metal-Oxide-Semiconductor (CMOS) techniques [5], [13], [14]. mM solutions attempt to aggressively push the fundamental IC scaling limits at a reduced cost per transistor for the next-generation technologies [13], [14]. The applications involving efficient computing, extensive memory usage and enormous or instant data handling impose goals for mM technologies, such as mobile applications, Internet-of-things (IoT), big-data applications, high-performance computing, etc. [13]. To sustain mM scaling, logic and memory technologies must meet the Performance, Power, Area and Cost (PPAC) requirements in every 2-3 years for each node scaling [13].

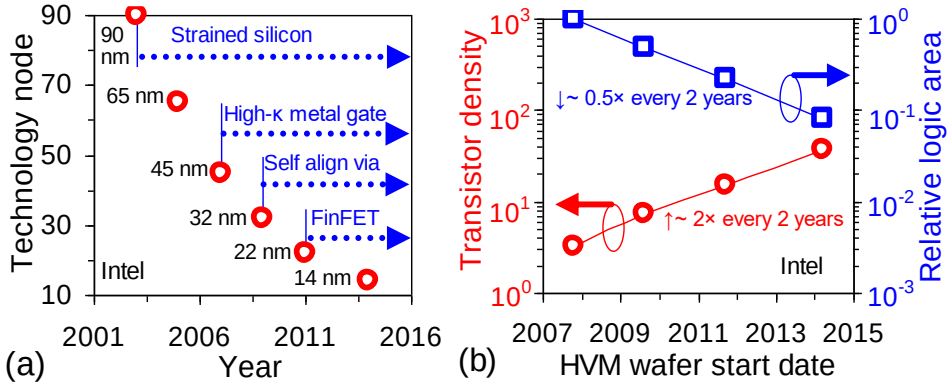

Fig. 1.1 (a) Intel transistor chronological innovations over six generations facilitating Moore's scaling [15]-[16]. **(b)** Scaling trends for Intel logic technologies showing High Volume Manufacturing (HMV) wafer start date-wise improvement in logic transistor density (MTr/mm^2) [16] and relative logic area [15]. Data source: Intel (Bohr and Young, 2017 [15], and Bohr, 2018 [16]).

mM technologies involve the introduction of innovative structures, novel materials and new physical effects in CMOS platform [12]-[16]. The viable options for mM technologies at device architectural levels are multigate transistor (e.g. Fin Field-Effect Transistor (FET)), strained silicon, high-κ gate oxide (e.g. HfO_2), channel materials beyond silicon (e.g. SiGe, germanium, III-V materials, graphene), novel device topologies (e.g. junctionless transistor, tunnel FET) and beyond [12]-[16]. Fig. 1.1(a) summarizes the transistor innovations by Intel over the six generations to continue Moore's scaling via mM solutions after the saturation of

traditional scaling in the early 2000s [15], [16]. The transistor innovations have led to almost 0.5 times improvement in the logic area scaling and approximately 2 times increment in the logic transistor density (MTr/mm^2) in every two years [15], [16] (Fig. 1.1(b)). The scaling trends have also resulted in improved transistor performance, lower cost per transistor and reduced active power (by lowering the dynamic capacitance) [15], [16].

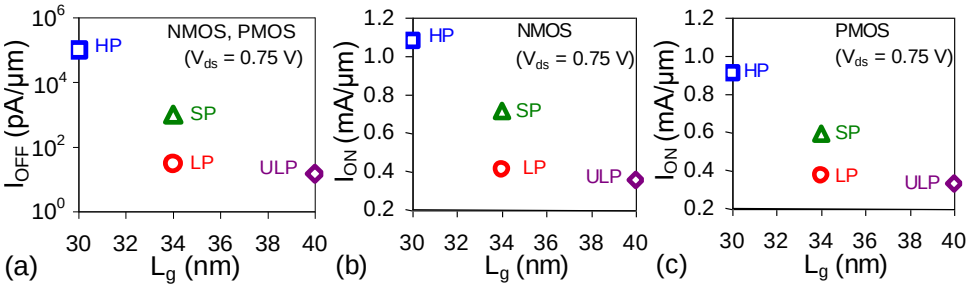

Fig. 1.2 Typical attributes of 22nm non-planar tri-gate transistor optimized for various logic technologies: **(a)** NMOS and PMOS off-current (I_{OFF}) **(b)** NMOS on-current (I_{ON}), and **(c)** PMOS on-current (I_{ON}). Data source: Intel (Jan *et al.*, 2012 [17]).

1.1.2 Low Power Logic Technology

The semiconductor industry has continuously been involved in the development and production of digital ICs for both low power and high speed logic technology applications. Fig. 1.2(a)-(c) compares 22nm System-on-Chip (SoC) non-planar tri-gate transistors (both NMOS and PMOS) optimized for Ultra-Low Power (ULP), Low Power (LP), Standard Performance/Power (SP) and High Performance (HP) logic technologies in terms of gate length (L_g), I_{OFF} and I_{ON} [17]. The off- and on-currents are evaluated at a supply (or drain) voltage (V_{ds}) of 0.75 V. Due to the different nature of constraints; LP transistors widely differ from the HP transistors [17]. In particular, the performance of portable devices is constrained by battery usage, and hence, demands low power technology innovations [13]. The prime goal of LP technology is to trade-off speed performance for low standby power or low I_{OFF} [13]. A scaled-down transistor possessing ideal subthreshold swing and a low value of drain induced barrier lowering is desirable for LP technology [17]. At the same I_{ON} and a fixed operating frequency, an improved subthreshold swing can

provide a better I_{ON}/I_{OFF} ratio at relatively low V_{ds} [18]. A feasible solution to achieve the same is to have enhanced electrostatic channel controllability through multiple gates in a transistor [19]-[22].

1.2 BASIC BACKGROUND

This section discusses a few essential topics before stating the objective and scope of the thesis. The section thereby facilitates a better understanding of the research work presented in this thesis.

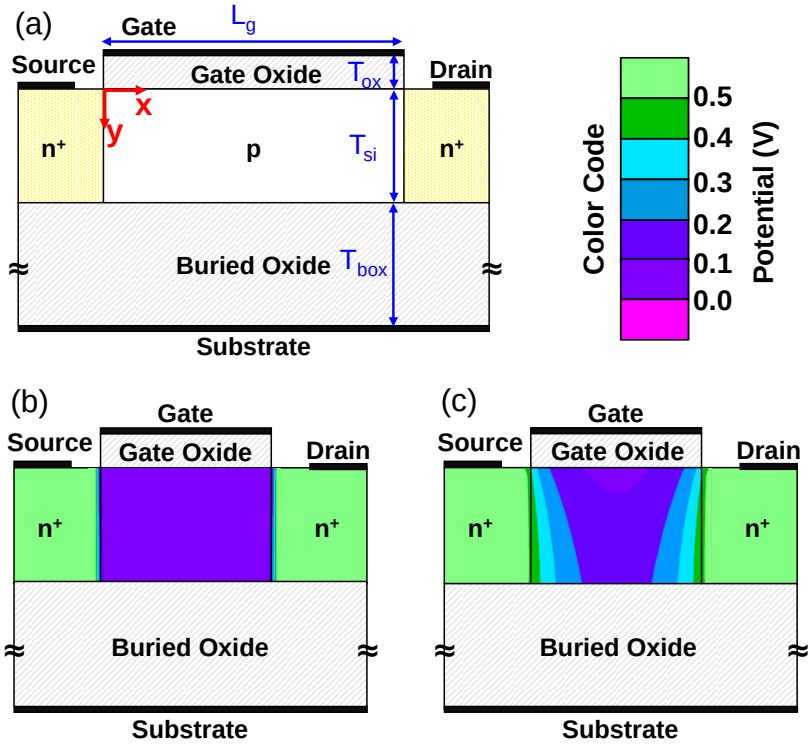

Fig. 1.3 (a) Simplified schematic diagram of *n*-channel Single Gate (SG) Silicon-on-Insulator (SOI) MOSFET [21], [23], [24]. Illustration of short channel effects using two-dimensional potential contours in the channel region for **(b)** long channel (L_g = 500 nm) and **(c)** short channel (L_g = 50 nm) devices. In Fig. 1.3(b),(c), each color corresponds to a certain potential range, as indicated by the above color codes. The simulations have been carried out through Atlas TCAD tool [25].

1.2.1 Short Channel Effects

Short Channel Effects (SCEs) are the undesirable behavior observed in the characteristics of Metal-Oxide-Semiconductor Field-Effect Transistor

(MOSFET) due to a reduction in the gate length, i.e. for short channel devices [26]-[28]. Fig. 1.3(a) depicts a simplified schematic view of *n*-channel SG SOI MOSFET [21], [23], [24]. To understand SCEs, two-dimensional (2D) potential contours are presented in Fig. 1.3(b) and Fig. 1.3(c) under zero applied biases (V_{gs} = V_{ds} = 0 V) condition for long (L_g = 500 nm) and short (L_g = 50 nm) channel MOSFETs, respectively. Other device parameters are channel doping (*p*-type) of 10^{16} cm^{-3}, source/drain doping (*n*-type) of 10^{20} cm^{-3}, gate oxide thickness (T_{ox}) of 2 nm, silicon film thickness (T_{si}) of 10 nm, buried oxide thickness (T_{box}) of 300 nm and midgap value (4.72 eV) of gate workfunction.

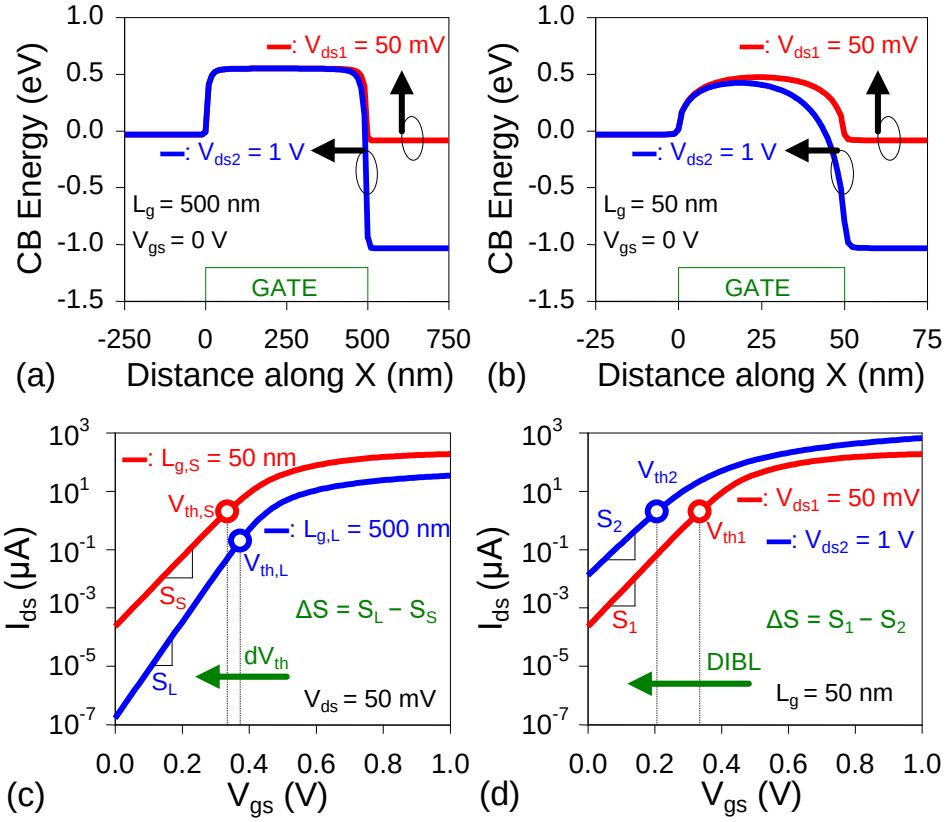

Fig. 1.4 Variations of Conduction Band (CB) energy along the lateral (*x*-) direction with drain bias for **(a)** long channel and **(b)** short channel MOSFETs. Comparison of transfer (I_{ds}-V_{gs}) characteristics: **(c)** long channel ($L_{g,L}$) versus short channel ($L_{g,S}$) cases and **(d)** low drain bias (V_{ds1}) versus high drain bias (V_{ds2}) cases.

In long channel devices, source and drain regions are distant from each other such that their electric fields have negligible effects over the channel

potential underneath the gate. The electrostatics is mostly controlled by the gate and is one-dimensional (1D) (i.e. varying mainly along the vertical (*y*-direction) [26]. The variation of potential in the *y*-direction for the long channel case in Fig. 1.3(b) is not significantly observed due to the choice of identical scale in Fig. 1.3(b),(c). However, due to the proximity of source and drain regions at shorter gate lengths, their electric fields interfere with the gate electric field and compete for the depletion charge in the channel [21], [22]. The lateral encroachment of source and drain electric fields deteriorates control of the gate over the channel. The potential distribution becomes 2D, rather than 1D (in Fig. 1.3(c)), having significant variations in vertical as well as lateral directions [26].

Fig. 1.4(a)-(b) compares the off-state (V_{gs} = 0 V) energy barrier seen by the electrons for low (V_{ds} = 50 mV) and high (V_{ds} = 1 V) drain biases for long and short channel cases, respectively. In the long channel case, the channel electrostatics is controlled by the gate field, and therefore, the energy band is flat in most of the channel (Fig. 1.4(a)). Only the near ends of the channel (adjacent to source/drain regions) are affected by the source and drain electric fields. The energy barrier height remains unaffected even if the drain field strengthens with increasing drain bias (when V_{ds} changes from 50 mV to 1 V). However, for a short channel case (Fig. 1.4 (b)), the intervention of source and drain electric fields against the gate field causes the barrier height to lower, as compared to the long channel case. The energy barrier lowering heightened when the drain-channel junction is more reverse biased (i.e. V_{ds} rises from 50 mV to 1 V).

SCEs can be observed in the device characteristics through a reduction in threshold voltage and degradation of subthreshold swing [21], [22], [26]-[28], as indicated in Fig. 1.4(c),(d):

i) **Reduction in threshold voltage [21], [22], [26]-[28]:** Threshold voltage (V_{th}) signifies the gate voltage at which significant drain current flows through the transistor, and the device is considered to be turned on [27], [28]. In Fig. 1.4(c),(d), V_{th} is usually extracted from I_{ds}-V_{gs} curve of the transistor using the constant current method [29]. In a long channel device, V_{th} is independent of the gate length. While in a

short channel device, the lowered energy barrier causes easy injection of carriers (electrons in *n*-channel MOSFET) from source to drain [26]-[28]. This barrier lowering tends to raise the subthreshold current, thereby forcing transistor to turn-on at a relatively low gate bias, and hence, at reduced threshold voltage. The reduction in V_{th} with decreasing L_g (relative to long channel case) is known as the 'threshold voltage roll-off (dV_{th})' [26], [27], as elucidated in Fig. 1.4(c). The reduction in V_{th} heightened when a high drain bias is applied, and the effect is termed as 'Drain Induced Barrier Lowering (DIBL)' [26]-[28], as illustrated in Fig. 1.4(d). The short channel threshold voltage is a function of gate length as well as drain bias.

ii) **Degradation in the subthreshold swing [21], [22], [26]-[28]:** Subthreshold swing (S), or inverse subthreshold slope or simply subthreshold slope, is defined as the gate voltage required for changing the drain current by a decade, below threshold [22], [26]. Subthreshold swing is a direct indication of gate controllability over the channel region. It has a minimum limit of 2.3 times the thermal voltage (~60 mV/dec at room temperature) under perfect gate-channel electrostatic coupling (ideal case) [22], [26]. In a long channel device, the subthreshold drain current varies exponentially with the gate bias and is independent of drain bias (provided V_{ds} > few times the thermal voltage) [28]. While in short channel devices, the gate does not solely control the channel electrostatics, and hence, a degraded S value (> 60 mV/dec) is usually achieved [26], [28]. In short channel MOSFET, subthreshold swing increases with both decreasing gate length and increasing drain bias [28], as depicted in Fig. 1.4(c),(d) by ΔS.

1.2.2 Junctionless Transistor

State-of-art transistors have reached to such dimensions where the formations of *pn* junctions with doping concentration gradients changing within a few nanometers are necessary. The need for ultra-sharp *pn* junctions imposes severe limitations on fabrication processes and thermal budgets. In 2009, Colinge *et al.* [30] experimentally demonstrated a new multi-gate nanowire transistor architecture named as the 'Junctionless'

(JL) transistor. They were shown to exhibit full CMOS functionality without radically altering the CMOS process technology [30], [31]. Fundamentally, a JL transistor is a gated resistor without any junctions [31]. Unlike conventional inversion-mode (IM) devices (in Fig. 1.5(a)), JL MOSFET (in Fig. 1.5(b)) possesses identical doping types and concentrations in the gated, source and drain regions. Since the doping gradients between the channel and source/drain regions are non-existent, no diffusion can take place.

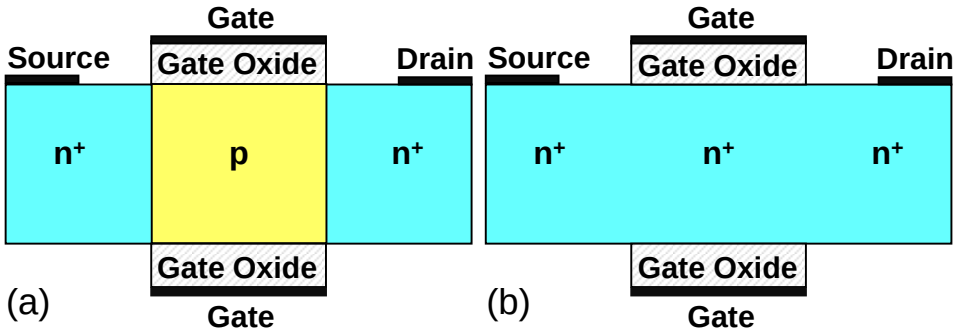

Fig. 1.5 Schematic diagram showing longitudinal cross-sectional view of **(a)** conventional inversion mode (n^+-p-n^+) MOSFET [21] and **(b)** junctionless (n^+-n^+-n^+) transistors [31], elucidating difference in doping profile across the semiconductor film.

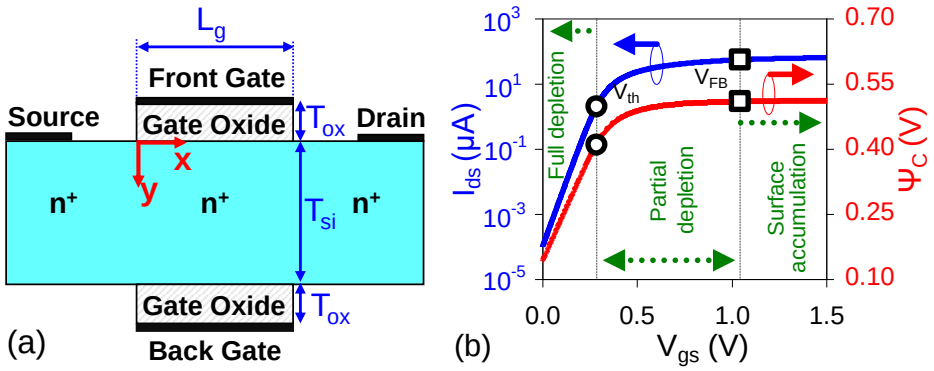

Fig. 1.6 (a) Schematic view of n-channel double gate JL MOSFET. **(b)** Typical variations of drain current (I_{ds}) and central potential (ψ_C) extracted at $x = L_g/2$, $y = T_{si}/2$ with gate bias at V_{ds} = 50 mV, marked with threshold (symbol: ○) and flatband (symbol: □) voltages. Device parameters: L_g = 50 nm, T_{ox} = 2 nm, T_{si} = 10 nm, N_d (n^+) = 10^{19} cm^{-3} and p+ polysilicon gate.

The key considerations to be taken care while fabricating a JL transistor [31] are as follows:

a) **Appropriate selection of gate metal workfunction [31]:** Due to identical doping type across the semiconductor film, JL MOSFET behaves as a normally-on device. A high (low) value of gate workfunction for *n*-channel (*p*-channel) JL device is needed to turn off the device and to obtain positive (negative) values of the threshold voltage.

b) **Narrow and thin semiconductor film [31]:** A sufficiently narrow and thin semiconductor film should be utilized such that the gate electric field can fully deplete the majority carriers from the channel.

c) **Heavy doping [31]:** To supply significant drive current in the on-state of the device, the semiconductor film is preferred to be heavily doped.

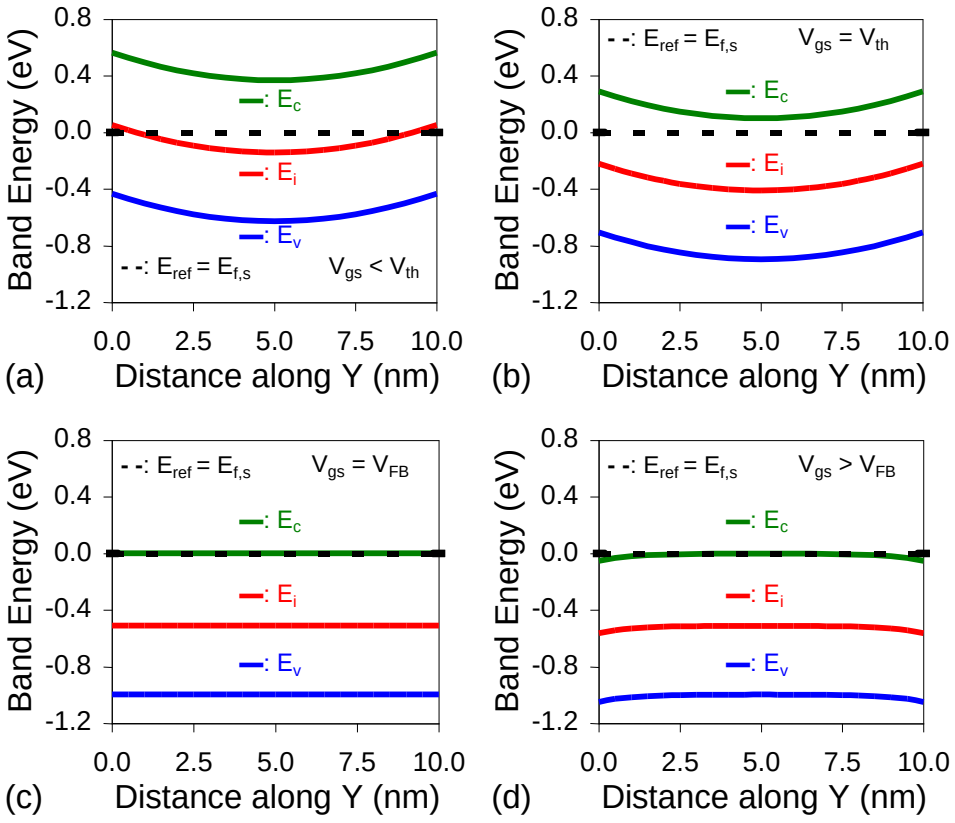

Fig. 1.7 Energy band diagrams extracted along the semiconductor film at mid-gate position ($x = L_g/2$), illustrating typical conduction mechanism in an *n*-channel DG JL MOSFET for **(a)** V_{gs} = 0 V (< V_{th}), **(b)** V_{gs} = 0.285 V (= V_{th}), **(c)** V_{gs} = 1.04 V (= V_{FB}) and **(d)** V_{gs} = 1.5 V (> V_{FB}). Device parameters are the same, as mentioned in Fig. 1.6.

Fig. 1.6(b) presents drain current (I_{ds})-gate voltage (V_{gs}) and central potential (ψ_C)-V_{gs} characteristics of an *n*-channel Double Gate (DG) JL MOSFET, as shown in Fig. 1.6(a), marked with V_{th} and flatband voltage (V_{FB}). Here, V_{th} and V_{FB} are extracted using the transfer curve through constant current [29] and transconductance change (i.e. the derivative of transconductance with respect to gate voltage) [32] methods, respectively. To demonstrate the typical conduction mechanism in JL transistor, the energy bands are extracted along the vertical direction inside the semiconductor film at different V_{gs}, as shown in Fig. 1.7(a)-(d). The notations E_v, E_i and E_c, denote Valence Band (VB), intrinsic Fermi level and CB energies, respectively. All the energy levels are with reference to the electron Fermi-level at the source end ($E_{f,s}$), fixed at ground potential.

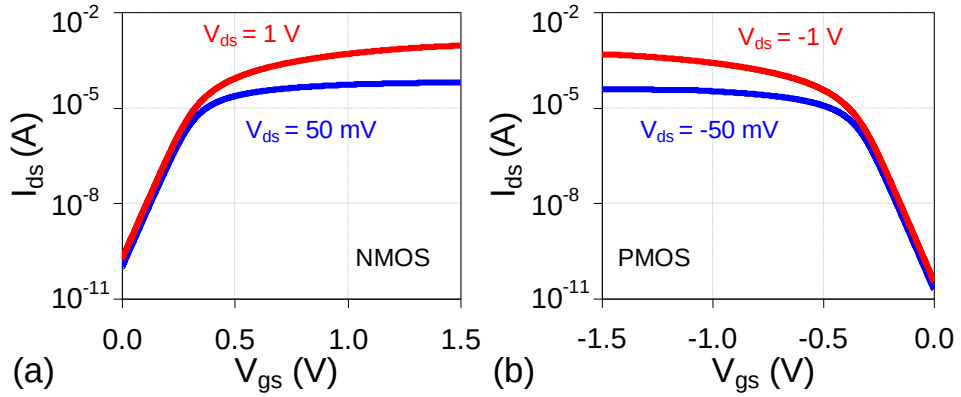

Fig. 1.8 Transfer characteristics of **(a)** NMOS and **(b)** PMOS DG JL transistors for V_{ds} of 50 mV and 1 V. Device specification: L_g = 50 nm, T_{ox} = 2 nm, T_{si} = 10 nm, T_{ox} = 2 nm, N_d (n^+) = 10^{19} cm^{-3}, N_a (p^+) = 10^{19} cm^{-3} , and p^+ (n^+) polysilicon gates for NMOS (PMOS).

In the subthreshold region (Fig. 1.7(a)), due to the gate workfunction induced high electric field, the semiconductor film is fully depleted of carriers (electrons in *n*-channel JL device), and the Fermi-level lies close to the intrinsic level. As V_{gs} rises, a neutral portion forms in the bulk of the device (away from the surface) between source and drain regions, and central potential increases. It can be noticed from the proximity of the conduction band to Fermi-level at the center than at the surface. The formation of the neutral channel leads to a significant flow of current through the transistor from drain to source, indicating V_{th} (Fig. 1.7(b)). The

device operates in a partially depleted mode for V_{gs} lying between V_{th} and V_{FB}. When V_{gs} reaches V_{FB}, the entire silicon film becomes neutral, and JL transistor behaves as a resistor. The electric field normal to the flow of drain current becomes zero, as interpreted by flat energy bands in Fig. 1.7(c). Also, the magnitude of carrier concentration in the semiconductor film reaches value equivalent to the channel doping, and ψ_C saturates. On further increase in V_{gs} beyond V_{FB}, the surface accumulation takes place at the semiconductor-oxide interface, as observed in Fig. 1.7(d) by slight downward bending of the conduction band away from the Fermi-level.

JL transistors offer various inherent benefits such as full CMOS functionality (illustrated in Fig. 1.8(a)-(b)), compatibility with present CMOS fabrication processes, lower thermal budget, relaxed expensive annealing techniques, easy fabrication of devices with shorter channels, less mobility degradation by transverse fields in the on-state, and enhanced immunity towards SCEs [30], [31], [33], [34]. However, conventional JL devices with high doping suffer from several drawbacks too, such as mobility degradation due to impurity scattering [35], [36] and reduced current drive due to increased source and drain series resistance [37], [38] when operated at higher gate overdrive, poor turning off capabilities for thicker semiconductor film or higher doping levels [30], [39], off-state Band-to-Band Tunneling (BTBT) [40], and enhanced sensitivity of device characteristics towards temperature [35], device parameter variations [41]-[43] and Random Dopant Fluctuations (RDFs) [43]-[46].

Since the advent of JL transistors, various researchers across the globe have extensively analyzed these devices for scalability [47], [48], low power logic technology [42], [49], high performance logic application [50], [51], analog/RF application [35], [52], transient behavior [39], [53], cryogenic operation [54]-[57], high temperature functionality [35], [36], [58], steep switching [59], [60], sensors [61]-[64], static [65], [66] and dynamic random access [67] memories, noise performance [68], [69], and parameter variability [35], [41]-[46].

1.2.3 Numerical Simulation using TCAD Tools

Numerical simulations using Technology Computer-Aided Design (TCAD) tools help to develop, comprehend and optimize the semiconductor devices, circuits and processes. The tools also aid in reliable predictions of next-generation devices, new circuit designs and novel process techniques [70], [71]. All the device numerical simulations reported in the thesis have been carried out using Atlas TCAD 2D device simulator by Silvaco, Inc. [25]. Atlas provides a detailed understanding of the underlying physical phenomena and mechanisms associated with a semiconductor device or structure. It also facilitates reliable predictions of the device's electrical characteristics. Appropriate physical models are incorporated in the simulator to capture the underlying physics of semiconductor devices [25].

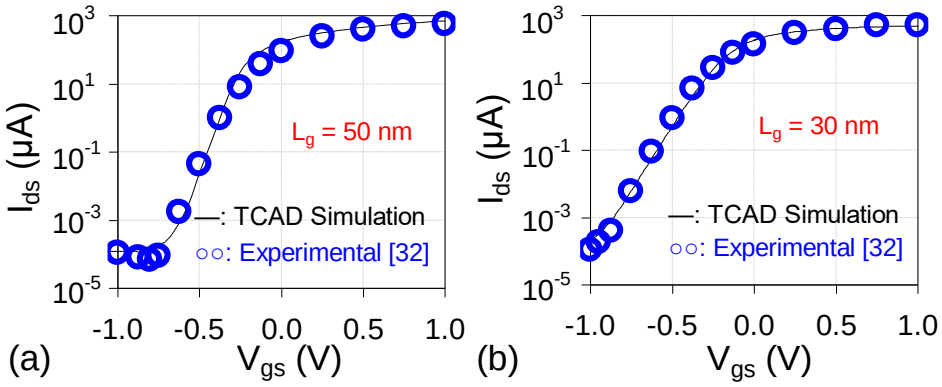

Fig. 1.9 Comparison of transfer characteristics obtained from simulation against published experimental data [32] for gate lengths of (a) L_g = 50 nm, and (b) L_g = 30 nm. Symbols indicate experimental data and solid lines show the numerical simulation data.

Before proceeding with the numerical simulation concerning the research work in the thesis, the physical model parameters have been calibrated with published experimental data [32]. Fig. 1.9 compares the transfer characteristics obtained from numerical simulation (denoted by solid lines) and published experimental data [32] (represented by symbols) for SG JL SOI MOSFET. The device parameters are gate lengths of 50 nm and 30 nm, effective oxide thickness of 1.2 nm, silicon film thickness of 9 nm, buried oxide thickness of 145 nm, body doping (*n*-type) of 10^{19} cm^{-3}.

Physical modules such as Boltzmann's carrier statistics, concentration- and field-dependent mobility, bandgap narrowing generation/recombination, and models are used in the simulation. The simulated data agree well with the experimental data [32].

1.2.4 Semiconductor Device Modeling

Device modeling, concerning the semiconductor industry, aims to capture mathematically the physical and electrical behavior of semiconductor devices, mostly MOSFETs [72]-[76]. The device models can be broadly categorized as either physical device models or equivalent circuit models [74], [75].

i) **Physical device models [74], [75]:** These models allow understanding the underlying physical phenomena involved (e.g., carrier transport), obtaining the non-measurable quantities (e.g., field distribution) and characterizing the physical parameter (e.g., mobility) related to the device. They also describe the electrical behavior at the terminals of the device (for instance, current-voltage characteristics, capacitance-voltage relation, etc.) in all the operating regimes. The model involves defining the geometry, materials, dimensions, doping distribution and carrier transport mechanism. Since these models provide detailed and accurate insights into the device operation and physics, and hence, are commonly used in commercial device numerical simulators.

ii) **Equivalent circuit models [74], [75]:** These models comprise interconnected electrical elements to replicate the electrical behavior at the terminals of the semiconductor structure. The model depends on the device characteristics where each circuit element is represented by its equivalent physical model. Due to their compact and fast computational nature, these models are widely preferred in circuit simulators.

Although the physical device models are highly accurate, these models are data and computationally intensive and are not suitable for the fast

device and large circuit simulations. Following approaches are adopted to simplify a purely physical device model [74]-[76] into compact models:

a) **Analytical models [74]-[76]:** These models rely on device physics and popularly utilized in circuit simulators. They contain closed-form solutions for physical quantities (e.g., surface potential, charge density) that are valid to the specific operating regime(s) only. Due to complex MOSFET behavior, it may not always be possible to obtain a compact and continuous closed-form analytical model that is applicable throughout the operating region.
b) **Empirical models [74]-[76]:** These models are based on curve fittings (e.g., polynomial or a cubic spline function). There are adjustable parameters, such as coefficients, exponents, etc., that are available to fit the device characteristics and seldom have any physical significance. A purely empirical model is generally not preferred for circuit simulators and is often accompanied by analytical models to describe complex physical phenomena.
c) **Lookup table models [74]-[76]:** These models consist of tables containing values of a physical or electrical quantity (e.g., mobility or drain current) for a large number of combinations of another quantity (e.g., doping or gate bias). These values can be derived from numerical simulations or experimental measurements. The simulator then 'looks up' and select the appropriate values from the table rather than evaluating them. These models are time-saving but require a massive set of data and interpolation functions between the values to be stored for high accuracy.

The developed models reported in the subsequent chapters of the present thesis are semi-analytical physical models. Most of the expressions involved in the proposed models have closed-form solutions, except for some equations that require numerical computations to determine the values for the unknowns.

1.3 REVIEW OF THE PAST WORK

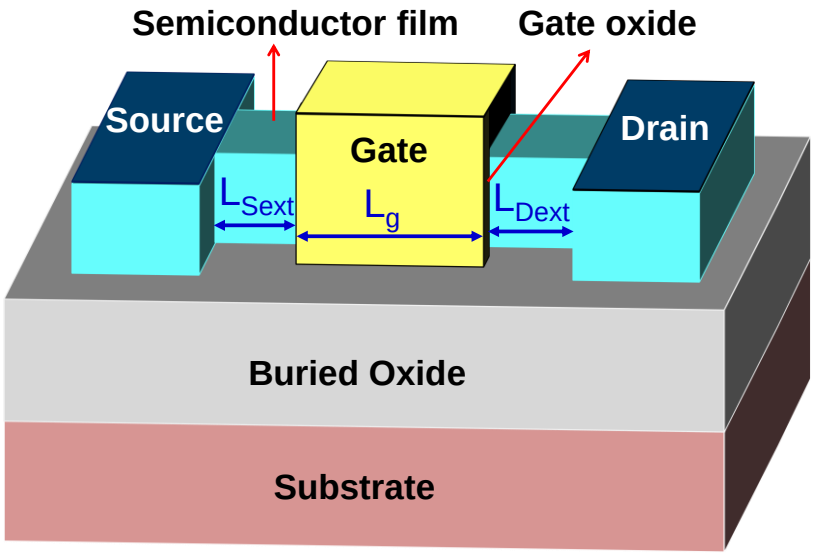

Fig. 1.10 Three-dimensional (3D) schematic representation of undoped IM SOI FinFET indicating the source and drain underlap of lengths, L_{Sext} and L_{Dext}, respectively [77], [78].

1.3.1 Optimization of Undoped Nanoscale FinFETs utilizing Gate-Source/Drain Underlap

Due to technological limitations in nanoscale IM FinFETs with an undoped body, there is likely to exist portions of Source/Drain Extensions (SDEs) adjacent to the gate edges that are also intrinsic (without any dopants), as indicated by L_{Sext} and L_{Dext} in Fig. 1.10 [77], [78]. Fossum *et al.* [77] suggested that to optimize the DG CMOS circuits when gate length reduces below 25 nm; such gate-source/drain underlap portions could be favorable. The length up to which the gate electric field modulates the conductivity of SDEs is termed as the effective channel length (L_{eff}) [77], [79]. In the gate underlap structure (Fig. 1.10), L_{eff} is bias-dependent; it is longer than gate length in the subthreshold region (or weak inversion region), whereas approaches the gate length in the strong inversion regime [77], [79], i.e.

- In subthreshold region: $L_{eff} \approx L_g + L_{Sext} + L_{Dext}$
- In the above threshold region: $L_{eff} \approx L_g$

L_{eff} is the most crucial parameter that determines the channel current and SCEs. A longer L_{eff} results in better immunity towards SCEs, but smaller values for drain current. Both underlap length as well as SDEs doping profile can be optimized to tune the performance of MOSFETs in terms of SCEs [77], [80], on-current [77], [79], [81]-[83], Source/Drain (S/D) series resistance [79], power consumption [81], [83], delay [82], [83], gate capacitance [79], [81]-[83] and leakage current [79], [83].

1.3.2 Feasibility of JL Transistors for LP and ULP Logic Applications

Based on the working of JL transistors, it is envisaged that JL transistors are expected to be more suitable for ultra-low-voltage applications where the supply (or drain) voltage is maintained less or equal to the threshold voltage (i.e. in the subthreshold), or for applications where the gate bias is restricted to 100 mV-200 mV above the threshold voltage. Under such operating conditions, the current in JL transistors is expected to flow through the center of the film i.e. bulk of the device where the electric field is minimum [30], [31]. The drain current reduction due to transverse field-induced mobility degradation [33], [84] as well as source/drain series resistance [38], [85] effects may not be severe. Hence, loss of drivability can be compensated with an increase in the on-to-off current ratio (an essential metric for LP/ULP logic application [17]). Previous studies [42], [49], [50] have shown the potential of JL MOSFET ($\sim 10^{19}$ cm^{-3}) over conventional IM MOSFET for LP subthreshold logic technology applications [42], [49] than for HP logic technology applications [50]. Dedicated optimizations of channel doping, underlap region (length and doping profile) and sidewall spacer (thickness and material) are essential in JL devices for LP and ULP technologies [49].

Historically, the semiconductor industry is driven by ITRS projections that do not cater to the subthreshold logic applications and are primarily focused on high performance or low power applications (both for above threshold operation) [13]. However, due to the reduced capacitance and lower supply voltage, digital subthreshold circuits are projected to

consume less power than their above threshold counterpart at a particular frequency of operation [81], [82]. A few years ago, Parihar *et al.* [42], [49], demonstrated that for an identical I_{OFF}, JL device with longer effective channel length can significantly improve ULP performance metric (on-current, on-to-off current ratio, intrinsic delay, etc.) and can be a prospect for subthreshold logic operation. Moreover, a moderately doped JL MOSFET (10^{18} cm^{-3} to 5×10^{18} cm^{-3}) can further improve ULP performance, reduce parameter variability and relax gate workfunction requirement to near midgap values [38] over a heavily doped (~10^{19} cm^{-3}) JL MOSFET, and is the most suitable for ULP subthreshold logic applications [38].

1.3.3 Analytical Modeling of JL Transistors

To capture the geometrical, physical and electrical aspects of the JL transistor in different operating regimes, numerous (pure/quasi-/semi-) analytical models have been proposed by the researchers worldwide. The list of analytical models for JL transistors available in the literature is exhaustive, and it is not possible to cover every model in the present thesis. Therefore, Table 1.1 reviews some selected analytical models for JL transistors [86]-[122].

Table 1.1 Summary of few existing analytical models for JL transistors available in the literature [86]-[122]

Author(s)	**Salient Features**
Duarte *et al.*, 2011 [86], [87], 2012 [88], [89]	• Bulk [86] and full-range [87] drain current model for planar DG JL MOSFET • Full-range drain current model for cylindrical nanowire (NW) [88] JL FET • Estimation of electron density under quantum confinement effects in the subthreshold region through a compact model for DG JL FET [89] • Analytical expression for V_{th} shift due to quantum confinement effects [89]

	• Valid for long channel devices [86]-[89]
Sallese *et al.*, 2011 [90]	• Charge-based modeling of DG JL MOSFET • Valid for long channel device in all operating regions (linear to saturation and deep depletion to accumulation)
Trevisoli *et al.*, 2011 [91], 2012 [92]	• V_{th} model for long channel JL rectangular NW transistor using 2D Poisson's equation [91] • Temperature influence on V_{th} considering incomplete ionization of dopants [91] • Drain current model using the surface potential for short channel Triple Gate (TG) JL NW FET [92] • Evaluates gate capacitance, transconductance, and output conductance [92]
Gnani *et al.*, 2011 [93], 2012 [94]	• Modeling of long channel mobile charge density, surface potential and drain current for JL NW FET (cylindrical geometry) [93] and JL ultrathin-body SOI FET [94]
Chiang, 2012 [95], [96]	• Scaling theory and threshold voltage model for DG [95] and Cylindrical Surrounding Gate (CSG) [96] topologies • Valid for short channel JL MOSFETs
Gnudi *et al.*, 2013 [97]	• 2D semi-analytical model for potential considering S/D depletion extensions • Fully analytical model for drain current • Valid for short channel JL DG FET under subthreshold operation
Woo *et al.*, 2013 [98]	• Analytical model for JL DG MOSFET with localized interface charges
Jin *et al.*, 2013 [99], [100]	• Subthreshold drain current [99] and continuous drain current [100] models for symmetric and asymmetric DG JL MOSFETs

Lime *et al.*, 2013 [101], 2014 [102], 2017 [103]	• Compact models for drain current characteristics of long channel DG [101], long [102] and short channel [103] cylindrical Gate-All-Around (GAA) JL MOSFETs
Jazaeri *et al.*, 2013 [104], 2014 [105]	• Trans-capacitance modeling in long channel JL symmetric DG [104] and GAA NW FETs [105]
Moldovan *et al.*, 2014 [106]	• Compact model for total charges and intrinsic capacitance characteristics of long channel cylindrical GAA JL MOSFETs
Baruah *et al.*, 2014 [107], 2016 [108]	• Electrostatic potential model for DG JL transistor with dual gate materials and vacuum as spacer material adjacent to both sides of the gate [107] • Surface potential based full range (depletion to accumulation) drain current model for DG JL transistor, without any fitting parameter [108]
Holtij *et al.*, 2014 [109], 2015 [110]	• 2D potential and V_{th} models for JL accumulation mode DG MOSFETs, introducing conformal mapping technique and effective built-in potential [109] • Valid for long and short channel devices, and all operating regions • Extended model for 3D TG NW JL device including quantization effects [110]
Hur *et al.*, 2015 [111]	• General potential model for tied/untied JL FETs with symmetric and asymmetric DG structures • Analytical V_{th} expression derived from a new definition (i.e., the gate voltage at which the sum of front and back gate induced depletion widths equals the semiconductor film thickness)
Kumari *et al.*, 2015 [112]	• Model for DG JL FET accounting the influence of outer fringing field from the gate electrode to the S/D regions

Ávila-Herrera *et al*., 2015 [113], 2016 [114]	• Charge-based compact model for short channel DG [113] and TG JL NW [114] transistors • Includes mobility degradation, channel length modulation, drain saturation voltage, series resistance, and velocity saturation
Xiao *et al*., 2016 [115], [116]	• Compact drain current model for short channel JL CSG [115] and DG [116] FET including dynamic channel boundary effect
Singh *et al*., 2016 [117], 2017 [118]	• Analytical modeling of threshold voltage in DG JL MOSFETs having vertical Gaussian-like doping profile [117] and dielectric pockets [118] • Evanescent mode analysis [117], [118] to find the solution for 2D Poisson's equations considering S/D depletion effect [118]
Oproglidis *et al.* 2017 [119]	• Analytical charge-based compact drain current model for TG JL MOSFETs including SCEs, series resistance, saturation velocity overshoot, and mobility degradation effects.
Shin *et al*., 2017 [120]	• Analytical subthreshold model for JL DG FETs using Fourier series and Green's function • Hot-carrier effects and random dopant fluctuations are modeled using localized trap charges and macroscopic analysis
Gola *et al*., 2018 [121]	• V_{th} model for TG JL FET including substrate bias and S/D depletion effects
Shalchain *et al*., 2018 [122]	• Charge-based modeling of quantum confined ultra-thin JL DG FET • Valid for linear to saturation as well as deep depletion to accumulation regions

1.4 RESEARCH PROBLEM AND OBJECTIVES

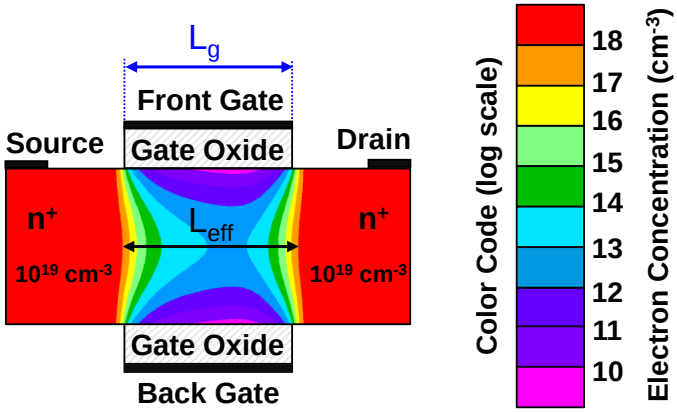

Fig. 1.11 2D contour of electron concentration elucidating longer L_{eff} than L_g in JL MOSFET under off-state (V_{gs} = 0 V) [123]. Device specifications are identical to those mentioned in Fig. 1.6. The numbers written for each color code boundary corresponds to the powers of 10.

1.4.1 Problem Formulation

As discussed earlier in subsection 1.2.2, the semiconductor film of a traditional JL transistor is (heavily) doped with identical dopant type and concentrations, and does not have *pn* junctions [30], [31]. In such cases, the gate electric field in the off-state not only modulates (deplete) the region underneath the gate, but also some portions adjacent to the gate edges. As a result, an elongated L_{eff} [77] in comparison to L_g is obtained in the off-state [123], as illustrated in Fig. 1.11. A relatively long L_{eff} in the off-state than L_g can significantly improve the performance of these devices at shorter gate lengths. The increase in L_{eff} becomes prominent for lower channel doping and has shown to be advantageous for ULP subthreshold logic applications while enabling downscaling [42], [123]. This unique and inherent property of JL transistors exists in mostly all JL architectures, whether traditional structures (i.e. uniformly doped gate, source and drain regions [30], [31]), modified structures with underlap [49] or novel JL structures with shell doping profile [124]-[127]. However, the value of L_{eff} in the subthreshold regime varies in different JL device topologies. For instance, if the source and drain regions are counter doped [34] till the edge of the gate, then L_{eff} is most likely equal to the gate length

(L_g) [95], [96]. However, if a device is designed such that source/drain doping is maintained away from the gate edge (primarily for ultra-low-power applications) [49], known as the underlap length [34], [49], then L_{eff} may become longer than L_g. Typically, L_{eff} depends on the lateral extension of depletion region beyond the gate edges into the S/D regions [123], which in turn depends on device parameters [97], [116], gate and drain biases [97], [116], geometry [97], [115], [116], [118] as well as underlap length [49]. Therefore, a model that can accurately capture the potential distribution accounting the lateral extension of S/D depletion regions for various conditions is indispensable to analyze and optimize JL architecture for ULP logic applications. Table 1.2 summarizes the key findings from some selected models available in the literature that have evaluated L_{eff}-dependent SCEs assuming either abrupt S/D boundaries [95], [96], or dynamic S/D boundaries [97], [109], [117] at the gate edges.

Table 1.2 Key findings of some existing models for short-channel JL MOSFETs

Methodology	**Limitation**
Chiang [95], [96] proposed scaling theory and evaluated dV_{th}, S and DIBL for DG [95] and CSG [96] JL MOSFETs assuming L_{eff} equals to L_g.	The model is applicable only when S/D regions are counter doped till the gate edges, i.e. when no underlap is present.
Holtij *et al.* [109] presented a compact model for short channel JL DG MOSFET incorporating the voltage drop across the S/D depletion regions beyond the gated region. The model used new device- and bias-dependent boundary conditions at the gate edges called the effective built-in voltage, which was computed by eliminating the	Though the approach allows an accurate evaluation of potential underneath the gate, it does not give any information about the potential variations in the S/D depletion region (beyond the gate edges). The determination of lateral extent of S/D depletion regions is essential for an accurate estimation of L_{eff}.

voltage drop across the S/D depletion region from the built-in potential developed at the S/D neutral regions.	
Gnudi *et al.* [97] developed a 2D potential model for DG JL FET considering lateral extensions of S/D depletion using 1D Poisson's equation outside the gated portion. Subthreshold drain current, dV_{th}, S and DIBL was also estimated.	The model is valid only if the maximum S/D depletion region extension is less than the underlap length. Due to the application-specific requirements for device characteristics [17], a ULP device is likely to be different from an HP device. The model may not be able to estimate L_{eff} for shorter underlap length than S/D depletion extension, especially at lower channel doping.
Xiao *et al.* [115] modeled 2D potential for CSG JL MOSFET, assuming S/D depletion regions similar to [97].	The model does not account for underlap length dependence on the lateral extent of S/D depletion regions.

The thesis identifies a missing aspect of existing analytical models and aims to capture underlap-dependent modulation of the lateral extension of S/D depletion regions, and hence, SCEs in JL devices. Furthermore, due to 2D distribution of potential outside the gated portion of a JL device with shell doping profile [124], [125], the existing 1D modeling approaches in [97], [115], cannot be directly applied beyond the gate edges in such a structure. Thus, it is essential to formulate a new methodology that can effectively predict channel potential while capturing essential device physics in the novel JL device with a shell doping profile.

1.4.2 Thesis Objectives

To explore and utilize the capabilities of nanoscale JL transistors by device and circuit designers for ULP subthreshold logic technology, the development of a generic yet simplified analytical model to evaluate the L_{eff}-dependent SCEs is essential. Thus, the prime objective of the research work presented in the thesis is to model SCEs in DG JL architectures (DG JL with gate underlap and shell doping profile), by adequately capturing the modulation of electrostatic potential by the gate field outside the gated regions in the subthreshold regime. The thesis also aims to propose guidelines for optimized JL transistor suitable for ULP subthreshold logic technology applications. Certain features are expected from the developed model, as listed below:

a) Analytical: The model should be fully or partially analytical. The empirical or fitting should be seldom used to preserve the physical significance of the model parameters.

b) Physical: The model must aid in providing insights into the device physics and operation.

c) Valid: To effectively predict SCEs, the model must be valid in the subthreshold operating regime.

d) Accurate: The model should predict the device behavior within a permissible error range (~10% - 15%).

e) Wide coverage: The models should be applicable for wide variations in parameter (e.g., underlap lengths, independent gate bias, etc.).

1.5 ORGANIZATION OF THE THESIS

The thesis presents detailed approaches to model SCEs in self-aligned DG JL transistors with underlap and shell doping profile. Semi-analytical models are developed to capture electrostatic channel potential efficiently in the subthreshold regime. The modeling approach involves solutions of 2D Poisson's equations using parabolic potential approximations in the vertical direction [119]-[123]. The one-dimensional channel potential along the lateral direction, governing the subthreshold conduction, is obtained considering S/D depletion extensions outside the gated portion.

Suitable device-dependent boundary and continuity conditions are used while solving the region-wise Poisson's equations. The subthreshold drain current is then derived from the channel potential at the different gate and drain biases, and V_{th} and S are extracted from I_{ds}-V_{gs} characteristics. At last, the parameters indicating SCEs are estimated, and the optimal device is proposed. The developed model results are validated with TCAD simulation results. A substantial portion of the thesis is dedicated to the detailed discussion of the modeled results to comprehend the device physics, as well as to propose design guidelines aiding device and circuit engineers.

Chapter 1 describes the motivation behind the identification of the research area selected for the present thesis. Starting from the aggressively pushing of the fundamental scaling limits of MOSFET through mM technology to the constraints faced by LP logic technology, this chapter covers the fundamental concepts necessary to follow the discussion in the rest of the thesis. The chapter also reviews the existing work available in the literature concerning LP JL transistors and the analytical modeling of JL transistors. At last, a brief description of each chapter is included.

Chapter 2 presents a semi-analytical model for an *n*-channel DG JL MOSFET under symmetric mode operation to estimate gate-underlap dependent SCEs. The model presented in this chapter primarily predicts the electrostatic channel potential by evaluating the S/D depletion region extensions as functions of underlap length, gate workfunction, channel doping and gate and drain biases. A detailed analysis is carried out to identify the additional design spaces offered by channel doping and underlap length to optimize the JL transistor with suppressed SCEs.

Chapter 3 discusses the modeling of SCEs in independent gate operation of self-aligned DG JL transistor, considering asymmetric gate workfunctions and oxides thicknesses, and S/D depletion extensions into non-identical S/D underlap. The chapter reports on the SCEs, dynamic nature of threshold voltage and design guidelines in an independently operated asymmetric DG JL MOSFET with underlaps.

Chapter 4 deals with a semi-analytical model for determining channel potential and SCEs in DG JL MOSFET with shell doping profile, i.e., core-shell JL MOSFET. The core-shell architecture has three regions in vertical (top shell, core and bottom shell) as well as in lateral (source extension, gated and drain extension regions) directions. Therefore, separate formalisms are carried out for each region to predict the potential distribution utilizing the equivalent doping, the effective built-in voltage at the S/D neutral regions and appropriate boundary/continuity conditions. This chapter discusses the effects of shell depth and shell doping on the SCEs and presents subsequent design guidelines for core-shell JL transistor, in particular suitable for subthreshold logic applications.

Chapter 5 summarizes the conclusion drawn from the research work presented in the thesis. It also mentions the scope for future work

Appendix-A offers the supplement reading material in assistance to the approximated solutions for integrals related to drain current in chapter 2, and the effective built-in potential at S/D neutral regions in chapter 4.

References enlist the cited references used in the present thesis.

Chapter 2

Modeling the Dependence of Short Channel Effects on Gate-Source/Drain Underlap Regions in Junctionless Transistor

2.1 INTRODUCTION

Multi-gate JL transistors can provide new pathways to extend the downscaling limits imposed by conventional MOSFETs. The key attributes of these transistors include the absence of traditional *pn* junctions, relaxed fabrication processes and thermal budgets, efficient control over the channel by multiple gates, and enhanced immunity towards SCEs [30]-[34]. Interestingly, due to the identical dopant types (preferably high doping) in the source, drain and gated regions, the extension of depletion regions outside the gated portion can take place in the off-state [123]. Consequently, L_{eff} becomes longer than the actual L_{g}. An elongated L_{eff} can suppress SCEs in JL transistors and have shown applications for LP technology [42], [49]. The optimization of Gate-Source/Drain (G-S/D) underlap regions has been favorable for achieving superior subthreshold characteristics in undoped IM DG MOSFETs [77]-[83]. A similar idea can be used to control SCEs in JL transistors. Such G-S/D underlap JL structures can be more suitable for ULP subthreshold logic applications where the main focus is to minimize the off-current and static power dissipation [17], [42], [49], [81], [132]-[134].

Several analytical models [95], [99], [111], [135], [136] have been proposed in the literature for short channel DG JL transistors that have approximated the S/D boundaries to be abrupt. They have ignored the potential drop across the laterally extended depletion regions outside the

gated portion. This assumption is expected to work efficiently when the length of S/D depletion extensions is negligibly small as compared to the gate length. However, for JL devices with shorter gate length and moderate doping levels, the lateral extension of depletion regions significantly contributes to the effective channel length [97], [115], [123]. As a result, the assumption may no longer be valid and may introduce a certain degree of error in estimating the channel potential and short channel performance of these devices [97], [115]. Recently, few reported models for DG JL transistors [109], [113] have attempted to incorporate these depletion region extensions by introducing an appropriate device-dependent effective built-in voltage at the gate boundaries. Furthermore, some latest models for DG JL devices [97], [116], [118] have considered these S/D depletion effects through dynamic S/D boundaries at the gate edges. However, these reported models are limited to the cases when the maximum extent of the depletion region permitted by the device is much less than the SDE lengths.

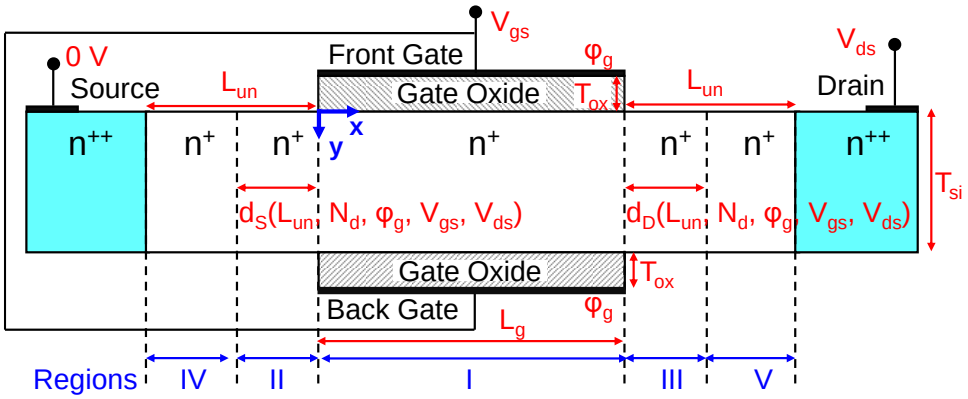

Fig. 2.1 Schematic view of *n*-channel DG JL transistor displaying I-V regions examined for the model development under symmetric mode operation, i.e. same values of G-S/D underlap lengths (L_{un}), gate biases (V_{gs}), gate workfunctions (φ_g), and gate oxide thicknesses (T_{ox}).

In practice, the additional S/D implantation is carried out away from the gated region in the JL transistor to reduce access resistance and contact formation [32], [34], [51]. The underlap length determines the distance between the gate edge and the additionally implanted S/D portion of the SDE regions [79], [137]. The lateral depletion region extension towards

S/D sides in JL devices depends on device specifications [97], [116], geometry [97], [115], [118], and underlap region [49]. Consequently, both the depletion extension length and underlap length can be different from each other, and must be considered while modeling SCEs in JL transistors. This chapter presents a five-region model to estimate and alleviate SCEs in symmetric DG JL transistor, considering different possible sets of depletion extension and underlap lengths.

2.2 MODEL DEVELOPMENT

In this section, a semi-analytical model has been developed for a symmetric mode operated DG JL MOSFET (as shown in Fig. 2.1) in the subthreshold regime to estimate gate-underlap dependent SCEs. In the n^{++}-n^{+} JL architecture, the same type of doping switches from typically a concentration of ~10^{20} cm^{-3} to a concentration of 10^{19} cm^{-3}-10^{18} cm^{-3}, and hence, doping gradient may not be very significant. To maintain simplicity in the model, abrupt doping transitions from n^{++} S/D to n^{+} underlap region is assumed, which is quite reasonable due to ~1.5 to 2 decades [32], [34] of transition in the doping levels from n^{++} S/D to n^{+} underlap region. As depicted in Fig. 2.1, the silicon film is split into five separate regions (I-V). Region-I covers the gated portion extending from $x = 0$ to $x = L_g$. Region-II and region-III define the portions covered by the laterally extended depletion region (outside the gated portion) towards the source and drain sides of lengths d_S and d_D, i.e. $-d_S \leq x \leq 0$ and $L_g \leq x \leq L_g + d_D$, respectively. For the cases, when L_{un} is longer than d_S and d_D, region-IV and region-V are included between heavily doped (n^{++}) neutral S/D region and extended depleted region at the source and drain sides, i.e. $-L_{un} \leq x \leq -d_S$ and $(L_g + d_D) \leq x \leq (L_g + L_{un})$, respectively. The channel potential is referenced to the electron quasi-Fermi potential at the source end.

2.2.1 Gated Portion (Region-I)

The potential distribution $\psi_I(x, y)$ in region-I is considered to be governed by 2D Poisson's equation under full depletion approximation (i.e. considering the contribution of channel doping (N_d) only while

neglecting mobile charge carriers related terms) in the subthreshold operating regime [99], as given below:

$$\frac{\partial^2 \psi_I(x,y)}{\partial x^2} + \frac{\partial^2 \psi_I(x,y)}{\partial y^2} = \frac{-qN_d}{\varepsilon_{si}} \tag{2.1}$$

where ε_{si} is the permittivity of Si and q is the electronic charge. $\psi_I(x, y)$ can be approximated as a generic parabolic function in the vertical (y-) direction [128] with arbitrary coefficients $a_0(x)$, $a_1(x)$ and $a_2(x)$ as

$$\psi_I(x,y) = a_0(x) + a_1(x)y + a_2(x)y^2 \tag{2.2}$$

Following vertical boundary conditions in (2.3)-(2.5) are utilized to obtain the expressions for the above coefficients:

a) Potential at the (symmetric) front and back surfaces, $\psi_S(x)$

$$\psi_I(x, y=0) = \psi_I(x, y=T_{si}) = \psi_S(x) \tag{2.3}$$

b) Electric field at the front and back surfaces, as decided by the effective gate voltage, ϕ_{gs} (= $V_{gs} - V_{fb}$), and gate oxide capacitance per unit area, C_{ox} (= ε_{ox}/T_{ox})

$$\left.\frac{\partial \psi_I(x,y)}{\partial y}\right|_{y=0} = \frac{C_{ox}(\psi_S(x) - \phi_{gs})}{\varepsilon_{si}} \tag{2.4}$$

$$\left.\frac{\partial \psi_I(x,y)}{\partial y}\right|_{y=T_{si}} = \frac{C_{ox}(\phi_{gs} - \psi_S(x))}{\varepsilon_{si}} \tag{2.5}$$

where ε_{ox} is the permittivity of gate oxide (in this case, silicon dioxide (SiO_2)), and V_{fb} (= $\varphi_g - \chi_{si} - E_g/2 - (kT/2)\cdot\ln(N_C/N_V)$) is the gate flatband voltage relative to intrinsic Si [97], [138], [139], χ_{si} is the electron's affinity in Si, E_g is the bandgap energy of Si, T is the temperature, k is the Boltzmann's constant, and N_C and N_V are the effective density of states for electrons and holes in CB and VB, respectively. Subsequently, $\psi_I(x, y)$ in (2.2) can be rewritten as

$$\psi_I(x,y) = \psi_S(x) + \frac{C_{ox}(\psi_S(x) - \phi_{gs})}{\varepsilon_{si}} y - \frac{C_{ox}(\psi_S(x) - \phi_{gs})}{\varepsilon_{si} T_{si}} y^2 \tag{2.6}$$

It has been well-established by Suzuki *et al.*, in [130] that the location of subthreshold current lies where the gate electric field coupling is the weakest inside the semiconductor film. Thus, the potential at $y = T_{si}/2$, i.e. central potential ($\psi_C(x)$), governs the subthreshold conduction for

symmetric DG JL MOSFET. Also, the conduction channel is located at the centre for DG JL topology (the bulk of the device in the JL architecture [30]-[31]). Adopting the approach described in [130] reduces (2.1) into a 2nd order differential equation in $\psi_C(x)$,

$$\frac{d^2\psi_C(x)}{dx^2} = \frac{\psi_C(x) - \psi_{Long}}{\lambda_N^2} \tag{2.7}$$

where λ_N indicates the natural length that characterizes SCEs and ψ_{Long} signifies the long channel central potential, and are represented by

$$\psi_{Long} = \frac{qN_d}{\varepsilon_{si}}\lambda_N^2 + \phi_{gs} \tag{2.8}$$

$$\lambda_N = \sqrt{\frac{\varepsilon_{si}T_{si}}{2C_{ox}}\left(1 + \frac{C_{ox}T_{si}}{4\varepsilon_{si}}\right)} \tag{2.9}$$

The generalized solution for (2.7) can be written by

$$\psi_I\left(x, \frac{T_{si}}{2}\right) = A_1 \exp\left(\frac{x}{\lambda_N}\right) + A_2 \exp\left(\frac{-x}{\lambda_N}\right) + \psi_{Long} \tag{2.10}$$

The boundary conditions at $x = 0$ and $x = L_g$ determine the values of unknown coefficients A_1 and A_2 in (2.10).

2.2.2 Depleted Portion of S/D Underlap Region (Region II/III)

The x-dependent 1D Poisson's equation under depletion approximation [97], [140] can be utilized to obtain the potential distribution $\psi_{II}(x)$ and $\psi_{III}(x)$ in regions II and III, respectively, as mentioned below:

$$\frac{d^2\psi_{II}(x)}{dx^2} = \frac{-qN_d}{\varepsilon_{si}} \tag{2.11}$$

$$\frac{d^2\psi_{III}(x)}{dx^2} = \frac{-qN_d}{\varepsilon_{si}} \tag{2.12}$$

As a first-order approximation, the potential variations along the y-direction are ignored in the S/D underlap regions, considering (i) negligible effect of the outer fringing fields from the gate electrode [97], [140], and (ii) no gate overlap over the S/D regions [141]. These assumptions provide an effective way to analytically model the lateral S/D depletion extensions and have shown to work efficiently for planar DG

[97], [116], as well as CSG [115] JL topologies in the subthreshold region. For region-II, twice integration of (2.11) within limits from $-d_S$ to x gives

$$\psi_{II}(x) = V_S - E_S(x + d_S) - \frac{qN_d}{2\varepsilon_{si}}(x + d_S)^2 \tag{2.13}$$

where E_S and V_S indicates the electric field and potential, respectively, at $x = -d_S$. Similarly for region-III, twice integration of (2.12) within limits from x to $L_g + d_D$ results

$$\psi_{III}(x) = V_D - E_D(x - L_g - d_D) - \frac{qN_d}{2\varepsilon_{si}}(x - L_g - d_D)^2 \tag{2.14}$$

where E_D and V_D denotes the electric field and potential, respectively, at $x = L_g + d_D$. The values for E_S, E_D, V_S, and V_D are estimated using the lateral boundary conditions in the subsequent sections of the chapter.

2.2.3 Non-depleted Portion of Underlap Region (Region IV/V)

As realized in Fig. 2.1, abrupt doping transitions from (n^{++}) heavily doped region to the (n^{+}) underlap region exist at the edges $x = -L_{un}$ and $x = L_g + L_{un}$ of regions IV and V, respectively. Whenever the doping concentration changes abruptly at a very short scale length, the energy bands do not respond immediately due to the thermal diffusion of mobile carriers [138]. The difference in doping causes thermal diffusion of electrons from n^{++} into n^{+} regions. This creates a space charge portion in region-IV that is predominantly governed by the transition of electrons (i.e., negatively space charge regions). Equivalently, the potential takes distances of the order of Debye length to respond to the abrupt change in doping [138]. Under such situations, 1D Poisson's equation along x-direction considering the contribution of both doping and electron concentration can be used to describe $\psi_{IV}(x)$ and $\psi_V(x)$, respectively,

$$\frac{d^2\psi_{IV}(x)}{dx^2} = \frac{-q}{\varepsilon_{si}}\left(N_d - n_i \exp\left(\frac{\psi_{IV}(x) - V_f(x)}{V_T}\right)\right) \tag{2.15}$$

$$\frac{d^2\psi_{V}(x)}{dx^2} = \frac{-q}{\varepsilon_{si}}\left(N_d - n_i \exp\left(\frac{\psi_{V}(x) - V_f(x)}{V_T}\right)\right) \tag{2.16}$$

where V_T ($= kT/q$) is the thermal voltage, $V_f(x)$ is electron quasi-Fermi potential, and n_i is intrinsic carrier concentration in Si. Note that the

depletion approximation cannot be applied to region-IV/V, due to the presence of significant electron concentration as compared to the doping concentration. Revising (2.15) and (2.16) using built-in potential (V_{biD}) relative to channel doping (N_d), i.e., $V_{biD} = V_T \ln(N_d/n_i)$ yields

$$\frac{d^2\psi_{IV}(x)}{dx^2} = \frac{-qN_d}{\varepsilon_{si}}\left(1-\exp\left(\frac{\psi_{IV}(x)-V_{biD}-V_f(x)}{V_T}\right)\right) \quad (2.17)$$

$$\frac{d^2\psi_{V}(x)}{dx^2} = \frac{-qN_d}{\varepsilon_{si}}\left(1-\exp\left(\frac{\psi_{V}(x)-V_{biD}-V_f(x)}{V_T}\right)\right) \quad (2.18)$$

Firstly, assume that $V_f(x)$ near the S/D ends is independent of x, and approximate $V_f(x)$ to zero (since the source electrode is grounded) and V_{ds} at the source and drain sides, respectively [142]. Secondly, expand the exponential term in (2.17) and (2.18) and discard second- and higher-order terms in the series. Subsequently, (2.17) and (2.18) can be approximated to a 2nd order differential equation in x, as written below:

$$\frac{d^2\psi_{IV}(x)}{dx^2} = \frac{\psi_{IV}(x)-V_{biD}}{\lambda_D^2} \quad (2.19)$$

$$\frac{d^2\psi_{V}(x)}{dx^2} = \frac{\psi_{V}(x)-V_{biD}-V_{ds}}{\lambda_D^2} \quad (2.20)$$

where $\lambda_D = (\varepsilon_{si}V_T/qN_d)^{1/2}$ is the extrinsic Debye length [138]. The general solution for (2.19) and (2.20) can be given as

$$\psi_{IV}(x) = B_1\exp\left(\frac{x+L_{un}}{\lambda_D}\right) + B_2\exp\left(\frac{-(x+L_{un})}{\lambda_D}\right) + V_{biD} \quad (2.21)$$

$$\psi_{V}(x) = C_1\exp\left(\frac{x-L_g-L_{un}}{\lambda_D}\right) + C_2\exp\left(\frac{-(x-L_g-L_{un})}{\lambda_D}\right) + V_{biD} + V_{ds} \quad (2.22)$$

The above unknown coefficients B_1, B_2, C_1 and C_2 are evaluated using boundary conditions in the later sections of the chapter.

2.2.4 Boundary and Continuity Conditions

The expressions for unknown coefficients in (2.10), (2.13), (2.14), (2.21), and (2.22) are obtained by ensuring continuity of potential and its first-order derivative at different edges. Appropriate lateral boundary and continuity conditions are selected to ascertain the various possibilities

observed from numerical simulations as well as those reported in the literature [97], [99], [116], [140].

a) The portions beyond regions I-V exhibit n^{++} S/D neutral regions with a doping concentration of N_{sd}. The potential boundaries of these regions are assumed to be:

$$\psi_{IV}\left(-L_{un}\right)=V_{biSD} \quad \text{and} \quad \psi_{V}\left(L_g+L_{un}\right)=V_{biSD}+V_{ds} \tag{2.23}$$

where V_{biSD} (= $V_T\, ln(N_{sd}/n_i)$) denotes the built-in potential at S/D ends.

b) For simplicity, the influence of gate fields on the region IV/V for S/D underlap lengths shorter than the respective maximum value of S/D depletion length achievable by the device is ignored. In other words, the electrons diffusion from n^{++} to n^{+} regions merely decides the electrostatics in these regions. This assumption can be translated into the equivalent potential boundaries as:

$$\psi_{IV}\left(\infty\right)=V_{biD} \quad \text{and} \quad \psi_{V}\left(-\infty\right)=V_{biD}+V_{ds} \tag{2.24}$$

c) Numerical simulations depict that for shorter L_{un} compared to the maximum depletion length allowed by the device, the electric field distributions in the negatively developed space charge region and depleted region (i.e., regions II/III and IV/V, respectively) overlap with each other. In contrast, for sufficiently longer L_{un}, the above two electric fields are well separated from one another. In either of these cases, continuity in the potentials and its first-order derivative remains intact at the interfaces of regions II-IV and III-V. Accordingly, the following boundary conditions are utilized:

$$\psi_{II}\left(-d_S\right)=\psi_{IV}\left(-d_S\right), \quad \psi_{III}\left(L_g+d_D\right)=\psi_{V}\left(L_g+d_D\right) \tag{2.25a}$$

$$\left.\frac{d\psi_{II}(x)}{dx}\right|_{x=-d_S}=\left.\frac{d\psi_{IV}(x)}{dx}\right|_{x=-d_S}, \quad \left.\frac{d\psi_{III}(x)}{dx}\right|_{x=L_g+d_D}=\left.\frac{d\psi_{V}(x)}{dx}\right|_{x=L_g+d_D} \tag{2.25b}$$

d) The continuity in the potentials and its first-order derivative persist at the gate edges [97], [116],

$$\psi_{I}\left(0,T_{si}/2\right)=\psi_{II}\left(0\right), \quad \psi_{I}\left(L_g,T_{si}/2\right)=\psi_{III}\left(L_g\right) \tag{2.26a}$$

$$\left.\frac{d\psi_{I}(x,T_{si}/2)}{dx}\right|_{x=0}=\left.\frac{d\psi_{II}(x)}{dx}\right|_{x=0}, \quad \left.\frac{d\psi_{I}(x,T_{si}/2)}{dx}\right|_{x=L_g}=\left.\frac{d\psi_{III}(x)}{dx}\right|_{x=L_g} \tag{2.26b}$$

Few observations can be made from the choice of above boundary and continuity conditions in (2.23)-(2.26). First, in the absence of S/D underlap (i.e. L_{un} = 0 nm), the additionally implanted (n^{++}) S/D region lies adjacent to the gated regions. Since the gate fields cannot penetrate the S/D portion with high doping, the S/D depletion lengths reduce to zero (i.e. $d_S = d_D = 0$ nm). The potential boundary conditions at $x = 0$ and $x = L_g$ transform to well-established values of V_{biSD} and ($V_{biSD} + V_{ds}$), respectively [99]. Second, when L_{un} exceeds the respective depletion lengths (d_S or d_D) by a few times λ_D, it can be noticed from (2.21), (2.22) and (2.25) that the potential and its first-order derivative at region II-IV boundary approach V_{biD} and 0 V/cm, respectively; whereas ($V_{biD} + V_{ds}$) and 0 V/cm at region III-V interface, respectively. Consequently, these boundary conditions result in the same expressions for the potential distribution in the S/D depleted extensions in [97], [116]. Mohammadi *et al*., [140] have also used the similar boundary conditions for predicting junction depletion lengths beyond the gate edges in DG tunnel FETs.

2.3 ESTIMATION OF GATE-UNDERLAP DEPENDENT DEVICE CHARACTERISTICS

2.3.1 Electrostatic Channel Potential Distribution

After solving (2.10), (2.13), (2.14), (2.21), and (2.22) using boundary conditions in (2.23)-(2.26), the following expressions in (2.27) are derived for the coefficients

$$A_1 = \frac{-g\exp\left(-L_g/\lambda_N\right)+h}{2\sinh\left(L_g/\lambda_N\right)},\ A_2 = \frac{g\exp\left(L_g/\lambda_N\right)-h}{2\sinh\left(L_g/\lambda_N\right)} \qquad (2.27a)$$

$$V_S = V_{biD} + \Delta V_{bi}\exp\left(\frac{d_S - L_{un}}{\lambda_D}\right),\quad E_S = \frac{\Delta V_{bi}}{\lambda_D}\exp\left(\frac{d_S - L_{un}}{\lambda_D}\right) \qquad (2.27b)$$

$$V_D = V_{biD} + V_{ds} + \Delta V_{bi}\exp\left(\frac{d_D - L_{un}}{\lambda_D}\right),\ E_D = \frac{-\Delta V_{bi}}{\lambda_D}\exp\left(\frac{d_D - L_{un}}{\lambda_D}\right) \qquad (2.27c)$$

$$B_1 = 0,\ B_2 = \Delta V_{bi}, C_1 = \Delta V_{bi} \text{ and } C_2 = 0 \qquad (2.27d)$$

where $\Delta V_{bi} = V_{biSD} - V_{biD}$, $g = V_S - \psi_{Long} - E_S d_S - \left(q N_d / 2\varepsilon_{si}\right) d_S^{\,2}$ and

$$h = V_D - \psi_{Long} + E_D d_D - \left(q N_d / 2\varepsilon_{si}\right) d_D{}^2$$

The system of equations in unknown quantities d_S and d_D are obtained by applying continuity conditions (2.26b), as given in (2.28) and (2.29), respectively. Since these equations involve transcendental functions, hence, their values are estimated numerically.

$$\begin{aligned} &k_a\, d_S{}^2 + k_b\, d_S + k_c\, d_D{}^2 + k_d \exp\left(d_S/\lambda_D\right) + k_e d_S \exp\left(d_S/\lambda_D\right) \\ &+ k_f \exp\left(d_D/\lambda_D\right) + k_g d_D \exp\left(d_D/\lambda_D\right) + k_{h1} = 0 \end{aligned} \tag{2.28}$$

$$\begin{aligned} &k_a\, d_D{}^2 + k_b\, d_D + k_c\, d_S{}^2 + k_d \exp\left(d_D/\lambda_D\right) + k_e d_D \exp\left(d_D/\lambda_D\right) \\ &+ k_f \exp\left(d_S/\lambda_D\right) + k_g d_S \exp\left(d_S/\lambda_D\right) + k_{h2} = 0 \end{aligned} \tag{2.29}$$

where,

$$k_a = \frac{-qN_d}{2\,\varepsilon_{si}} \cosh\left(L_g/\lambda_\gamma\right),\ k_b = \frac{-qN_d\lambda_\gamma}{\varepsilon_{si}} \sinh\left(L_g/\lambda_\gamma\right),\ k_c = \frac{-qN_d}{2\,\varepsilon_{si}},$$

$$k_d = \Delta V_{bi}\left(\cosh\left(L_g/\lambda_\gamma\right) - \left(\lambda_N/\lambda_D\right)\sinh\left(L_g/\lambda_\gamma\right)\right)\exp\left(-L_{un}/\lambda_D\right),$$

$$k_e = \left(-\Delta V_{bi}/\lambda_D\right)\cosh\left(L_g/\lambda_\gamma\right)\exp\left(-L_{un}/\lambda_D\right),$$

$$k_f = \left(-\Delta V_{bi}/\lambda_D\right)\exp\left(-L_{un}/\lambda_D\right),\ k_g = -\Delta V_{bi}\exp\left(-L_{un}/\lambda_D\right),$$

$$k_{h1} = \left(V_{biD} - \psi_{Long}\right)\cosh\left(L_g/\lambda_\gamma\right) - \left(V_{biD} + V_{ds} - \psi_{Long}\right),$$

$$k_{h2} = \left(\left(V_{biD} + V_{ds} - \psi_{Long}\right)\cosh\left(L_g/\lambda_\gamma\right) - \left(V_{biD} - \psi_{Long}\right)\right)$$

Moreover under the long channel approximation (i.e. $L_g >> \lambda_N$), the maximum allowable S/D depletion length (for $L_{un} >> d_S$, d_D) can be obtained using following expressions for d_{Smax} and d_{Dmax}, respectively:

$$d_{S\max} = \sqrt{\lambda_N^2 + \left(2\varepsilon_{si}/qN_d\right)\cdot\left(V_{biD} - \psi_{Long}\right)} - \lambda_N \tag{2.30}$$

$$d_{D\max} = \sqrt{\lambda_N^2 + \left(2\varepsilon_{si}/qN_d\right)\cdot\left(V_{biD} + V_{ds} - \psi_{Long}\right)} - \lambda_N \tag{2.31}$$

2.3.2 Peculiar Cases and Modifications

Note that the value of d_S or d_D exceeding L_{un} is not physically feasible, and must range between 0 and L_{un} values. If d_S or d_D value exceeds L_{un} from the procedure mentioned above in subsection 2.3.1, then set $d_S = L_{un}$ or $d_D = L_{un}$, and exclude respective region-IV or region-V from the developed model. The coefficients A_1, A_2, V_S and V_D are evaluated using the same expressions mentioned in (2.27). However, to satisfy the

boundary condition in (2.26b), E_S and E_D must be computed through (2.30) and (2.31), respectively.

$$E_S = \frac{\left\{\lambda_N \sinh\left(L_g/\lambda_N\right) + d_D \cosh\left(L_g/\lambda_N\right)\right\}\eta_s - d_D\,\eta_d}{\left\{\left(d_S + d_D\right)\left(\lambda_N/2\right)\right\}\sinh\left(2L_g/\lambda_N\right) + \left(\lambda_N^2 + d_S\,d_D\right)\left\{\sinh\left(L_g/\lambda_N\right)\right\}^2}$$

(2.32)

$$E_D = \frac{-d_S\,\eta_s + \left\{\lambda_N \sinh\left(L_g/\lambda_N\right) + d_S \cosh\left(L_g/\lambda_N\right)\right\}\eta_d}{\left\{\left(d_S + d_D\right)\left(\lambda_N/2\right)\right\}\sinh\left(2L_g/\lambda_N\right) + \left(\lambda_N^2 + d_S\,d_D\right)\left\{\sinh\left(L_g/\lambda_N\right)\right\}^2} \quad (2.33)$$

where

$$\eta_s = \left(V_S - \psi_{Long} - \left(q\,N_d/2\varepsilon_{si}\right){d_S}^2\right)\cosh\left(L_g/\lambda_N\right) - \left(V_D - \psi_{Long} - \left(q\,N_d/2\varepsilon_{si}\right){d_D}^2\right) - \left(q\,N_d/\varepsilon_{si}\right)d_S\lambda_N \sinh\left(L_g/\lambda_N\right)$$

$$\eta_d = -\left(V_D - \psi_{Long} - \left(q\,N_d/2\varepsilon_{si}\right){d_D}^2\right)\cosh\left(L_g/\lambda_N\right) + \left(V_S - \psi_{Long} - \left(q\,N_d/2\varepsilon_{si}\right){d_S}^2\right) + \left(q\,N_d/\varepsilon_{si}\right)d_D\lambda_N \sinh\left(L_g/\lambda_N\right)$$

2.3.3 Subthreshold Drain Current

The subthreshold drain-to-source current in an *n*-channel MOSFET is predominantly constituted by the flow of electrons from source to drain. This electron current can be estimated by solving the current continuity equation in the *x*-direction while assuming a constant quasi-Fermi potential for electrons in the *y*-direction [138], [143]. The subthreshold current is then derived using the Pao and Sah's double integral [143] as:

$$I_{ds} = \frac{k\,T\,W_g\,\mu_n\,n_i\left(1 - \exp\left(-\beta V_{ds}\right)\right)}{\left[\int_{-d_S}^{0}\frac{dx}{\int_0^{T_{si}}\exp\left(\beta\psi_{II}(x)\right)dy} + \int_{0}^{L_g}\frac{dx}{\int_0^{T_{si}}\exp\left(\beta\psi_{I}(x,y)\right)dy} + \int_{L_g}^{L_g+d_D}\frac{dx}{\int_0^{T_{si}}\exp\left(\beta\psi_{III}(x)\right)dy}\right]} \quad (2.34)$$

where $\beta = 1/V_T$, μ_n is the mobility of electrons and W_g is the gate (channel) width. Eq. (2.34) is derived assuming that the hole current as well as the generation and recombination current are negligible in the device [138]. An analytical expression for I_{ds} is given in (2.35) using piecewise approximations [144] to avoid numerical computation involved in (2.34)

$$I_{ds} \approx \frac{k T W_g \mu_n n_i \left(1-\exp\left(-\beta V_{ds}\right)\right)}{\left(F_{II} + F_I + F_{III}\right)} \tag{2.35}$$

where

$$F_I = \int_0^{L_g} \frac{dx}{G_I(x)} \approx \frac{L_g}{6}\left[\frac{1}{2\,G_I(0)} + \sum_{m=1}^{5} \frac{1}{G_I\left(\frac{mL_g}{6}\right)} + \frac{1}{2\,G_I\left(L_g\right)}\right]$$

$$F_{II} = \int_{-d_S}^{0} \frac{dx}{G_{II}(x)} \approx \frac{d_S}{4}\left[\frac{1}{2\,G_{II}(0)} + \sum_{m=1}^{3} \frac{1}{G_{II}\left(\frac{-md_S}{4}\right)} + \frac{1}{2\,G_{II}\left(-d_S\right)}\right]$$

$$F_{III} = \int_{L_g}^{L_g+d_D} \frac{dx}{G_{III}(x)} \approx \frac{d_D}{4}\left[\frac{1}{2\,G_{III}\left(L_g\right)} + \sum_{m=1}^{3} \frac{1}{G_{III}\left(L_g + \left(\frac{md_D}{4}\right)\right)} + \frac{1}{2\,G_{III}\left(L_g + d_D\right)}\right]$$

$$G_I(x) = \int_0^{T_{si}} \exp\left(\beta\psi_I(x,y)\right)dy$$

$$\approx \left(T_{si}/4\right) \times \left[\exp\left(\beta\psi_S(x)\right) + \exp\left(\beta\psi_C(x)\right) + 2\exp\left(\beta\psi_I\left(x, T_{si}/4\right)\right)\right]$$

$$G_{II}(x) = \int_0^{T_{si}} \exp\left(\beta\psi_{II}(x)\right)dy = T_{si}\exp\left(\beta\psi_{II}(x)\right)$$

$$G_{III}(x) = \int_0^{T_{si}} \exp\left(\beta\psi_{III}(x)\right)dy = T_{si}\exp\left(\beta\psi_{III}(x)\right)$$

The section A.1 of appendix-A at the end of this thesis can be referred for more details on the above approximations for the integrals.

2.3.4 Estimation of Short Channel Effects

As discussed in chapter 1, SCEs can be primarily observed in the device transfer characteristics through three parameters, namely DIBL, dV_{th} and degradation in S, and can be evaluated as follows:

i) DIBL is measured by the reduction in V_{th} with a rise in V_{ds} [95], [109]

$$DIBL = V_{th}\left(V_{ds} = few\,mV\right) - V_{th}\left(V_{ds}\right) \tag{2.36}$$

ii) dV_{th} is estimated by a decrease in V_{th} for a reduction in L_g with

respect to long channel V_{th} [95]

$$dV_{th} = V_{th}(Long\,channel) - V_{th}(L_g) \tag{2.37}$$

iii) An increase in S occurs for short channel devices, where S can be evaluated using [22]

$$S = \partial V_{gs} / \partial(\log(I_{ds})) \tag{2.38}$$

2.4 RESULTS AND MODEL VERIFICATION

Following device parameters are kept fixed for DG JL MOSFET throughout the analysis in this chapter: T_{ox} = 2 nm, T_{si} = 10 nm, N_{sd} = 5×10^{20} cm^{-3} and W_g = 1 µm. The developed model is mainly investigated for N_d varying from 10^{18} cm^{-3} to 10^{19} cm^{-3}. The developed model results are verified with results derived from Atlas device simulator [37]. In all the subsequent figures of this chapter, solid lines show developed model results, whereas symbols denote TCAD simulation data.

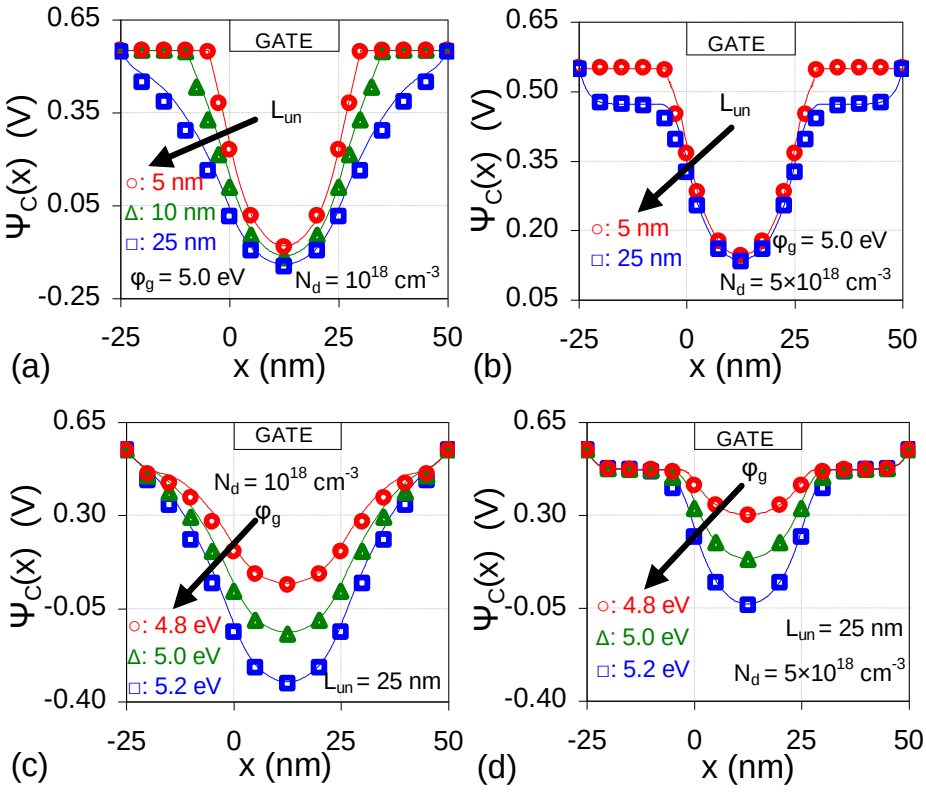

Fig. 2.2 Variation in central potential along the x-direction for varying L_{un} and φ_g with L_g = 25 nm, V_{gs} = V_{ds} = 0 V, and **(a)**, **(c)** N_d = 10^{18} cm^{-3} and **(b)**, **(d)** N_d = 5×10^{18} cm^{-3}. Solid lines represent the developed model results and symbols denote TCAD simulation data.

2.4.1 Simulation Details

To capture the essential physical phenomena occurring in the device, modules have been included in the device simulations such as Auger and Shockley-Read-Hall models for carrier recombination, Boltzmann's carrier statistics, concentration-dependent mobility [97], and doping-dependent bandgap narrowing model [25]. For the device thickness above ~7 nm, Quantum Confinement Effect (QCE) does not have a significant effect over the electron concentration profile (normal to the current flow direction) [33], [41], [89], [145]. Hence, QCE is not considered in the present analysis, and the model is expected to be valid for $T_{si} \geq 7$ nm.

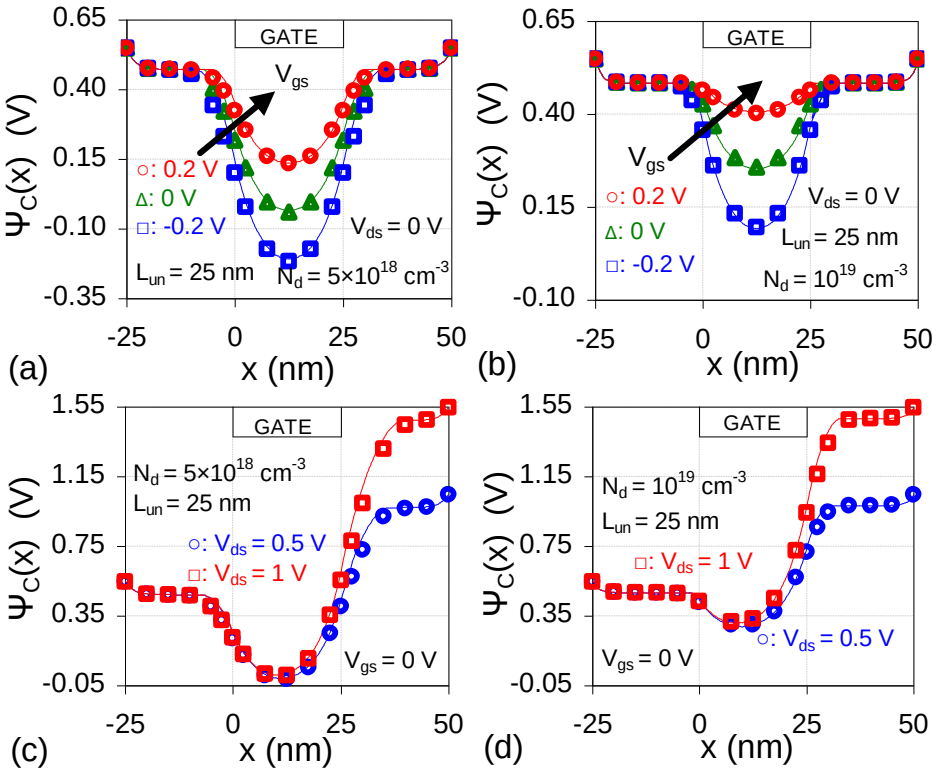

Fig. 2.3 Dependence of $\psi_C(x)$ along the x-direction on varying V_{gs} and V_{ds} at L_g = 25 nm, φ_g = 5.2 eV and **(a)**, **(c)** N_d = 5×10^{18} cm^{-3} and **(b)**, **(d)** N_d = 10^{19} cm^{-3}. Lines denote model results and symbols show simulation data.

2.4.2 Preliminary Model Verification

Fig. 2.2(a)-(d) demonstrates that the model results agree well with simulation to predict the dependence of L_{un}, φ_g and N_d on the central potential, $\psi_C(x)$. Fig. 2.2(a)-(b) shows that L_{un} limits the extent of the

depletion region outside the gated portion by restricting the penetration of gate fields through heavily doped S/D regions. Fig. 2.2(c)-(d) presents that a relatively low minimum channel potential and slightly longer depletion region extension lengths are achieved for higher φ_g (at a constant N_d value). Moreover, for fixed φ_g and L_{un}, the extent of lateral extension is prominent for lower doping levels (i.e. for $N_d = 10^{18}$ cm^{-3} than $N_d = 5\times10^{18}$ cm^{-3}) due to ease in the gate field penetration for lower doping.

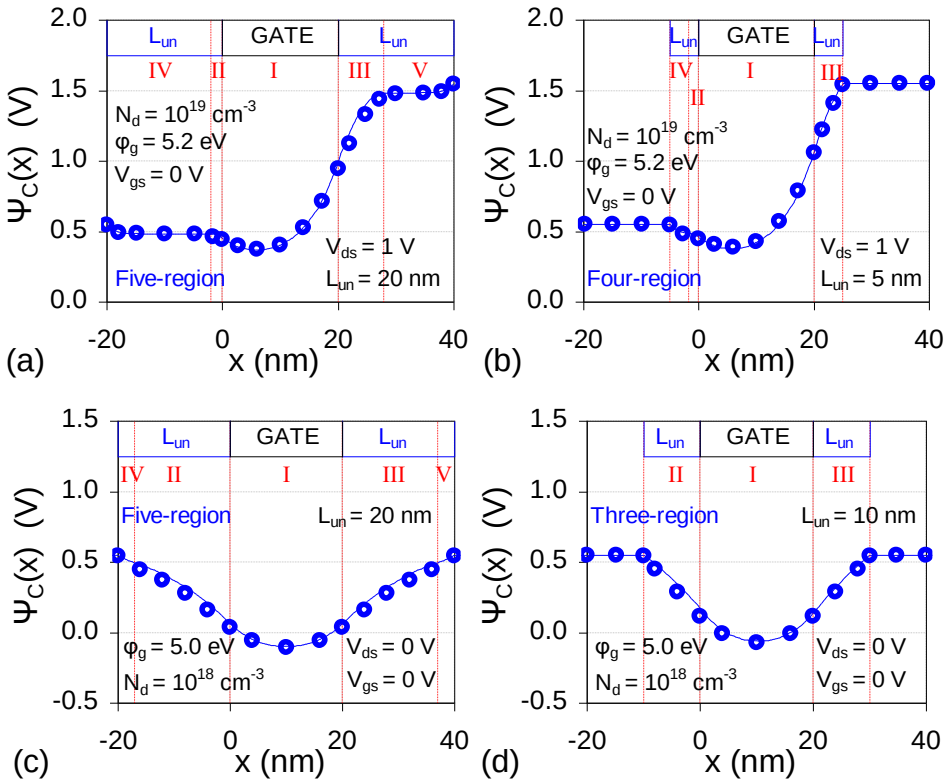

Fig. 2.4 Plots of $\psi_C(x)$ illustrating possible peculiar cases captured by the developed model at L_g = 20 nm and V_{gs} = 0 V for different (N_d, L_{un}, V_{ds}) combinations: **(a)** (10^{19} cm^{-3}, 20 nm, 1 V), **(b)** (10^{19} cm^{-3}, 5 nm, 1 V), **(c)** (10^{18} cm^{-3}, 20 nm, 0 V), and **(d)** (10^{18} cm^{-3}, 10 nm, 0 V). Lines denote model results and symbols show simulation data.

Next, the dependence of central potential on V_{gs} and V_{ds} is analyzed in Fig. 2.3(a)-(d) and $\psi_C(x)$ estimated by the model matches the simulation results. The plots in Fig. 2.3(a)-(b) signifies that the channel potential increases for rising V_{gs}, thereby forcing the device to approach the threshold. Also, it can be noticed in Fig. 2.3(c)-(d) that owing to the increased reverse-biased drain-channel junction with increasing V_{ds}, the

drain depletion region becomes longer than its source counterpart, which otherwise is identical at V_{ds} = 0 V (in Fig. 2.3(a)-(b)).

Fig. 2.4(a)-(d) displays the wide applicability of the developed five-region model in estimating the channel potential variations for possible peculiar cases at L_g = 20 nm. As depicted in Fig. 2.4(a)-(b), the five regions for L_{un} = 20 nm modifies to four regions (without region-V) for L_{un} = 5 nm, indicating fully depleted drain underlap region for $N_d = 10^{19}$ cm^{-3} at V_{ds} = 1 V. Also, when L_{un} is varied from 20 nm to 10 nm for $N_d = 10^{18}$ cm^{-3} in Fig. 2.4(c)-(d), five regions transform into three regions at zero biases condition, signifying $d_S = d_D$ = 10 nm for L_{un} = 10 nm case. It is emphasized here that the developed model predicts inherently the same potential profile in the subthreshold region as estimated by previously reported model in [97], [116], provided $L_{un} >> d_S$ and d_D. Nevertheless, the developed five-region model offers additional features to estimate the channel potential profile at any S/D underlap length.

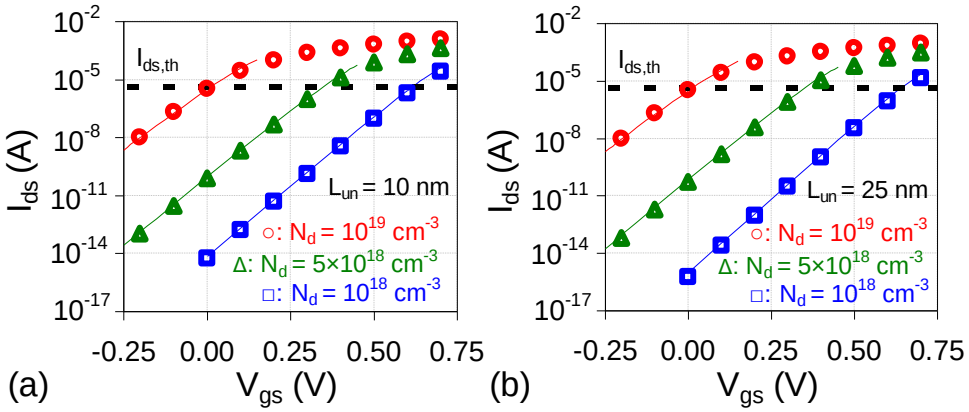

Fig. 2.5 I_{ds}-V_{gs} characteristics for three N_d values with **(a)** L_{un} = 10 nm and **(b)** L_{un} = 25 nm. Other parameters: L_g = 25 nm, V_{ds} = 1 V and φ_g = 5.1 eV. Lines denote model results and symbols show simulation data.

2.4.3 Short Channel Effects

Since the prime motive of the developed model is to capture the dependence of the S/D underlap region on SCEs, hence, the model is analyzed only in the subthreshold operating region. Fig. 2.5(a)-(b) depicts I_{ds}-V_{gs} characteristics for L_{un} = 10 nm and 25 nm at different N_d, where $I_{ds,th}$

indicates the drain current corresponding to $V_{gs} = V_{th}$. The modeled drain current agrees well with simulated subthreshold drain current.

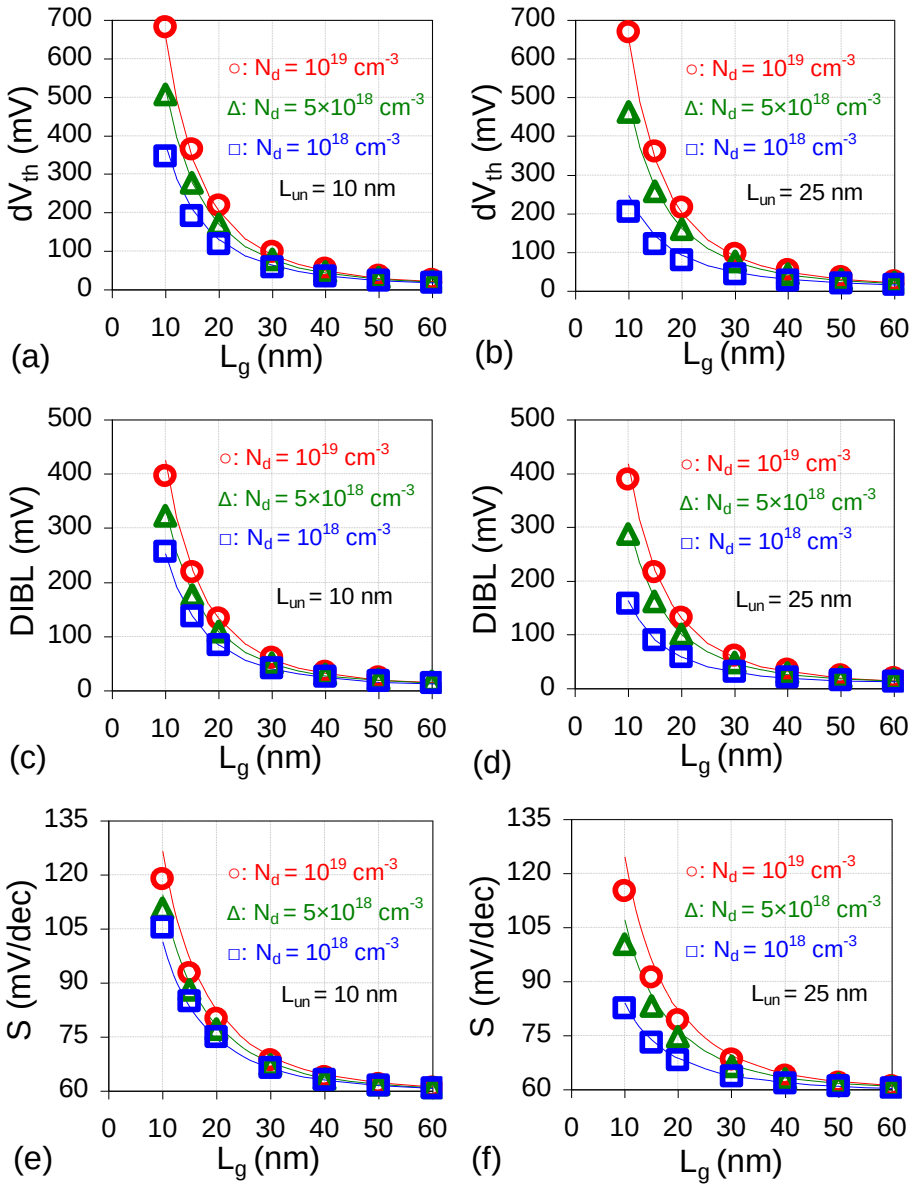

Fig. 2.6 Plot of SCEs with L_g for φ_g = 5.1 eV at V_{ds} = 1 V: **(a)** dV_{th}, **(c)** DIBL and **(e)** S for L_{un} = 10 nm, and **(b)** dV_{th}, **(d)** DIBL and **(f)** S for L_{un} = 25 nm. Lines denote model results and symbols show simulation data.

Fig. 2.6(a)-(d) investigates SCEs for varying gate lengths, L_{un} = 10 nm and 25 nm, and three N_d values at V_{ds} = 1 V. The modeled dV_{th}, DIBL and S reasonably match the simulations. Here, dV_{th} and DIBL is computed relative to V_{th} for L_g = 100 nm, and V_{th} at V_{ds} = 50 mV, respectively. While SCEs remain unaltered by increasing L_{un} from 10 nm to 25 nm for N_d = 10^{19} cm^{-3}, an alleviated SCEs are observed for L_{un} = 25 nm than L_{un} = 10

nm for N_d = 5×10^{18} cm^{-3} and 10^{18} cm^{-3}. Lower doping (e.g., 10^{18} cm^{-3}) along with longer underlap (e.g., L_{un} = 25 nm) can be chosen to suppress SCEs at shorter L_g. The improved immunity towards SCEs for N_d = 10^{18} cm^{-3} is mainly due to better gate controllability and relatively easy gate field penetration into the underlap region at lower channel doping.

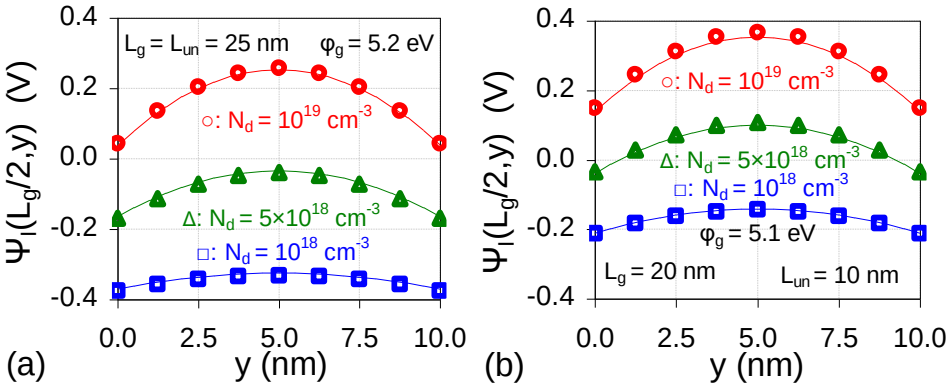

Fig. 2.7 Channel potential along the *y*-direction at mid-gate position elucidating doping-dependent channel spreading at V_{gs} = V_{ds} = 0V for **(a)** L_g = L_{un} = 25 nm, and **(b)** L_g = 20 nm and L_{un} = 10 nm. Lines show model results and symbols denote simulation data.

Certainly decreasing N_d to 10^{18} cm^{-3} offers suppressed SCEs, but the device no longer operates in JL mode (i.e. dominant bulk conduction) rather in accumulation mode (spread-out channel in the subthreshold region), as presented in Fig. 2.7(a)-(b). A moderately doped device can offer better subthreshold I_{ON} for a fixed I_{OFF} (due to improved S) and can be a prospect for ULP subthreshold logic operation [42], [49]. Moreover, lowering the channel doping can relax the constraints on gate workfunction [49] as well as minimize the sensitivity of the device characteristics (such as V_{th}, I_{ON}, I_{OFF} and S) due to parameter variations [41], [42] and random dopant fluctuations [46]. Hence, N_d scaling is suggested to be an optimal solution to suppress SCEs while enhancing low power performance metrics for the subthreshold logic application.

Next, to examine the variations in SCEs with L_{un}, DIBL and S are estimated at V_{ds} of 0.5 V and 1 V for L_g = 25 nm, as shown in Fig. 2.8(a)-(d). Modeled results reasonably agree with simulation data. Results suggest that increasing L_{un} can reduce DIBL and S by permitting a longer

d_S and d_D, and hence a longer L_{eff}. However, the combination of φ_g and N_d limits the maximum allowable depletion length extension for long enough L_{un}. Further increment in L_{un} does not alter the depletion length or the minimum channel potential, and hence, short channel performance remains unchanged. SCEs further degrade by increasing V_{ds}.

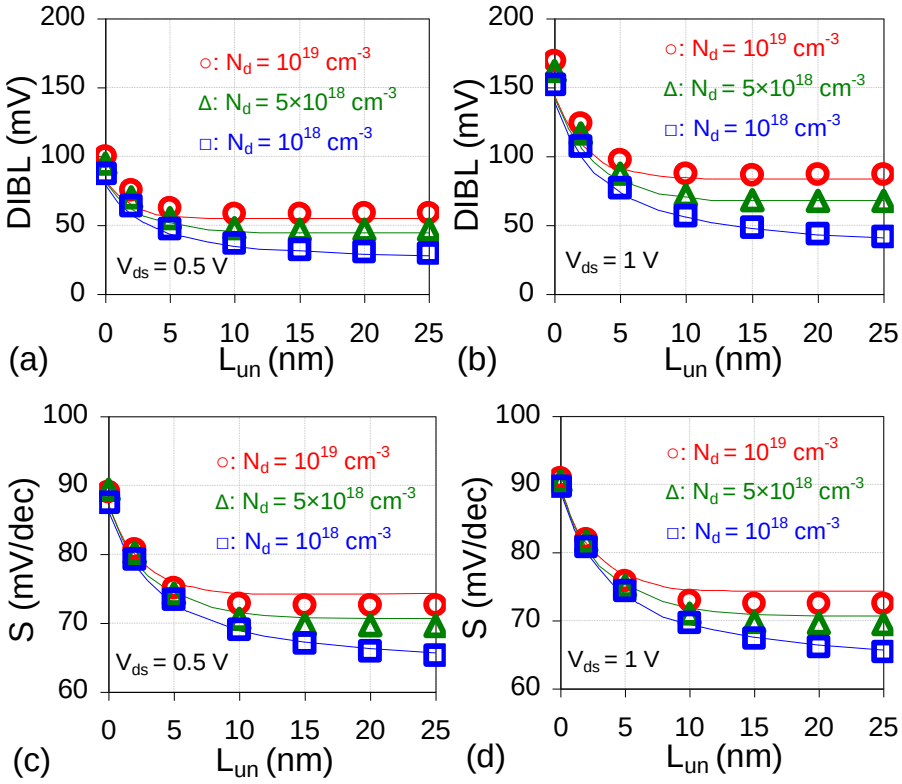

Fig. 2.8 Underlap-dependent short channel behavior for L_g = 25 nm and φ_g = 5.1 eV: **(a)** DIBL and **(b)** S at V_{ds} = 0.5 V, and **(c)** DIBL and **(d)** S at V_{ds} = 1 V. Lines denote model results and symbols show simulation data.

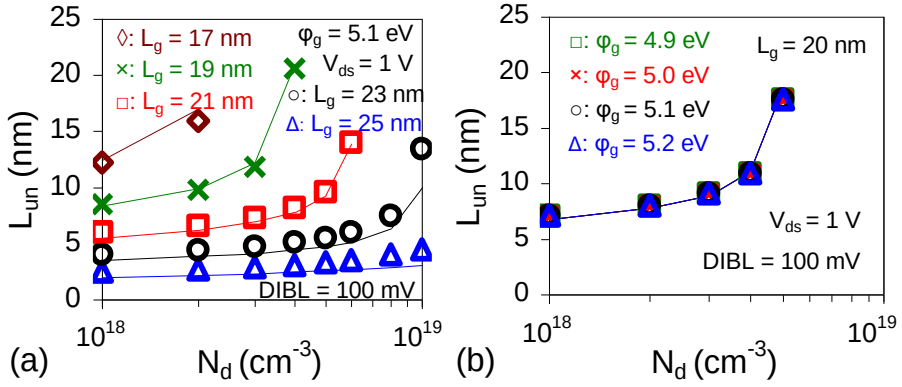

Fig. 2.9 Plot depicting the minimum values of L_{un} required for attaining DIBL = 100 mV at V_{ds} = 1 V as a function of N_d for various **(a)** L_g and **(b)** φ_g. Lines show model results and symbols denote simulation data.

Fig. 2.9(a) shows that a longer L_{un} is necessary to attain the same value of DIBL (= 100 mV at V_{ds} = 1 V) for (i) higher N_d at a constant L_g, and (ii) shorter L_g at a fixed N_d value. On the other hand, Fig. 2.9(a) suggests the doping-dependent minimum L_{un} value required for a fixed DIBL at a given L_g remains unaltered by a change in φ_g (from 4.9 eV to 5.2 eV). This behavior is observed due to approximately identical V_{th} shift for both V_{ds} = 1 V and 50 mV with changing φ_g, thereby maintaining a constant DIBL at each φ_g value.

2.5 CONCLUSION

This chapter has provided a detailed methodology to model and alleviate SCEs in symmetric mode operated DG JL MOSFETs utilizing the gate-underlap regions. The presented five-region semi-analytical model can adequately capture electrostatic channel potential at any gate-underlap length and have shown good agreement with simulation data. A simplified analytical solution for subthreshold drain current can be utilized to evaluate threshold voltage, subthreshold swing and SCEs related parameters. The developed model results have shown acceptable agreement with simulation for predicting SCEs for varying underlap length, gate workfunction, channel doping, gate length and drain biases. The results obtained from TCAD simulation and developed model suggest that channel doping together with underlap region decide the short channel performance of DG JL transistor, whereas SCEs remain unaffected by gate workfunction. An optimally long underlap length along with moderate doping (10^{18} cm^{-3}) can be advantageous to improve SCEs at sub-50 nm gate lengths.

Chapter 3

A Generic Model to Optimize Short Channel Self-Aligned Asymmetric Double Gate Junctionless Transistor with Gate-Underlap

3.1 INTRODUCTION

SCEs are one of the most critical issues faced by the miniaturization of transistors to sub-50 nm scale that severely degrade their subthreshold characteristics [10], [21], [22], thereby making them unsuitable for LP/ULP logic technology applications [17]. Utilizing G-S/D underlap along with a multi-gate structure has been a feasible solution for controlled SCEs [77], [79], [137] as well as enhanced ULP performance metrics [42], [49], [81] in both IM and JL transistors. The previous chapter has presented that an optimum choice of G-S/D underlap lengths and moderate channel doping can significantly improve SCEs in a multi-gate device such as symmetric DG JL MOSFET [146]. A DG MOSFET also provides additional flexibility to alter its performance through asymmetric mode operation [131], [147]-[151]. Over the years, structural asymmetries (non-identical front and back gate workfunctions and oxide thicknesses) and independent gate operation (front and back bias asymmetry) have been widely exploited to tune V_{th} [131], [147], to improve S and I_{OFF} [147]-[149] and to enhance performance [150], [151] of IM DG MOSFETs.

Due to the prominent bulk conduction mechanism (below flatband), the effect of independent gate operation can be significant in JL devices than the surface conducting IM devices [152]. An independent back bias can be applied to deplete the channel region and to obtain positive values for V_{th} in heavily-doped JL MOSFET [32]. As symmetric DG JL

MOSFETs with underlap has provided better prospects for subthreshold logic applications [49], [146], hence, it is equally important to investigate an asymmetric DG JL with underlap for LP subthreshold logic technology.

Few popular models [99], [111], [153] that are available in the literature has analyzed the DG JL transistor under asymmetric mode operation. Hur *et al*., [111] have derived V_{th} expression from a generic potential model for DG JL MOSFET with an asymmetric gate structure under tied/untied modes. Jin *et al*., [99] have reported an analytical drain current model for JL DG transistor having asymmetric gate oxide thicknesses and gate biases. Jazaeri *et al*., [153] have combined two virtual symmetric JL FETs to model charges in the asymmetric operation of JL DG FETs. These models may be adequate to analyze the DG JL device under gate structural and bias asymmetries. However, they cannot be directly employed for asymmetric DG JL with G-S/D underlap structure due to assumed abrupt S/D boundaries at the gate edges. Therefore, the present chapter focuses on modeling SCEs in independent gate operated DG JL MOSFET, considering the lateral extension of S/D depletion region into G-S/D underlap. The model also includes the differences in front and back gate workfunctions and oxides thicknesses, and S/D underlap lengths to account for possible structural asymmetries.

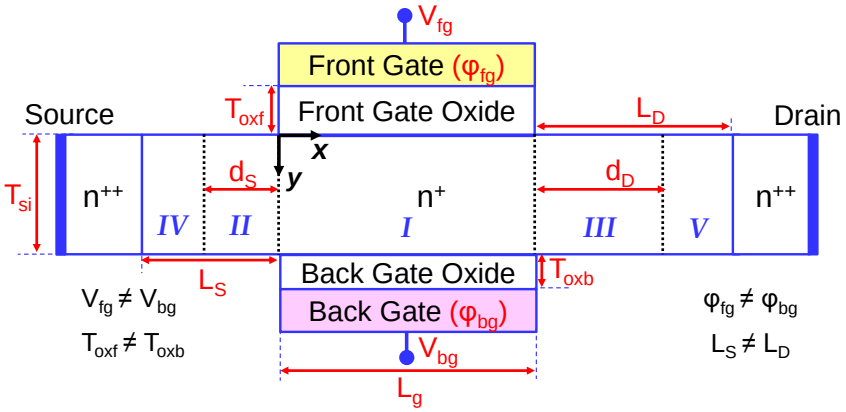

Fig. 3.1 Schematic view of a self-aligned *n*-channel DG JL transistor displaying I-V regions examined for the model derivation under asymmetric mode operation, i.e. different values of G-S/D underlap lengths ($L_S \neq L_D$), and front and back gate biases ($V_{fg} \neq V_{bg}$), oxide thicknesses ($T_{oxf} \neq T_{oxb}$) and workfunctions ($\varphi_{fg} \neq \varphi_{bg}$).

3.2 MODEL DERIVATION CONSIDERING BIAS AND STRUCTURAL ASYMMETRIES

For the model derivation in the subthreshold regime, the silicon film is separated into five regions (I-V), as shown in Fig. 3.1. Region-I defines the gated portion extending from $x = 0$ to $x = L_g$. Regions II and III consist of laterally extended depletion portions beyond region-I till $x = -d_S$ and $x = L_g+d_D$ into the source and drain underlap, respectively. At last, regions IV and V cover the undepleted portion of the source and drain underlap of non-identical lengths L_S and L_D, respectively. The modeling approach adopted in this chapter is similar to those followed in chapter 2 for symmetric DG JL MOSFET (i.e. a special case of asymmetric DG JL MOSFET). Nonetheless, there exists following two major differences:

i. The expressions for various coefficients depend on both structural and bias asymmetries and are quite different from the symmetric case.
ii. The location of subthreshold conduction is predefined to exist at the centre of the film, (i.e. $y = T_{si}/2$) in the symmetric case. While in the asymmetric case, subthreshold conduction need not necessarily take place at the centre, instead is determined by the asymmetries involved.

3.2.1 Gated Portion (Region-I)

The SCEs governing 2D Poisson's equation, as mentioned in (2.1) of chapter 2 for symmetric DG JL case, decides the potential distribution $\psi_I(x, y)$ in the asymmetric case as well. Subsequently, a generic parabolic function in the y-direction approximates the potential distribution in the region-I, as given in (2.2). However, the expressions for the coefficients $a_0(x)$, $a_1(x)$ and $a_2(x)$ are relatively different from the symmetric case. Following boundary conditions are used to determine the values for the above coefficients:

c) Potential at the front surface, $\psi_f(x)$:

$$\psi_I(x, y = 0) = \psi_f(x) \tag{3.1}$$

d) Potential at the back surface, $\psi_b(x)$:

$$\psi_I(x, y = T_{si}) = \psi_b(x) \tag{3.2}$$

e) Electric field at the front surface, as decided by the effective front gate voltage, ϕ_{fg} (= V_{fg} – $V_{fb,fg}$), and front gate oxide capacitance per unit area, C_{of} (= ε_{ox}/T_{oxf})

$$\left.\frac{\partial \psi_I(x,y)}{\partial y}\right|_{y=0} = \frac{C_{of}\left(\psi_f(x)-\phi_{fg}\right)}{\varepsilon_{si}} \tag{3.3}$$

f) Electric field at the back surface, as determined by the effective back gate voltage, ϕ_{bg} (= V_{bg} – $V_{fb,bg}$), and back gate oxide capacitance per unit area, C_{ob} (= ε_{ox}/T_{oxb})

$$\left.\frac{\partial \psi_I(x,y)}{\partial y}\right|_{y=T_{si}} = \frac{C_{ob}\left(\phi_{bg}-\psi_b(x)\right)}{\varepsilon_{si}} \tag{3.4}$$

where $V_{fb,fg}$ and $V_{fb,bg}$ is the front and back gate flatband voltages relative to intrinsic Si, and is dependent on the front (φ_{fg}) and back (φ_{bg}) gate metal workfunctions, respectively. On evaluating the coefficients from (3.1)-(3.4) and putting them back into (2.2) yields,

$$\psi_I(x,y) = \psi_f(x) + \frac{C_{of}\left(\psi_f(x)-\phi_{fg}\right)}{\varepsilon_{si}}y - \frac{\left(\varepsilon_{si}C_{of}+T_{si}C_{of}C_{ob}\right)\left(\psi_f(x)-\phi_{fg}\right)+\varepsilon_{si}C_{ob}\left(\psi_f(x)-\phi_{bg}\right)}{\varepsilon_{si}T_{si}\left(2\varepsilon_{si}+T_{si}C_{ob}\right)}y^2 \tag{3.5}$$

Adopting a similar method as discussed in [130], [131], $\psi_I(x,y)$ can be rewritten in terms of $\psi_\gamma(x)$ (= $\psi_I(x, y = \gamma)$) at any arbitrary location $y = \gamma$ inside the semiconductor film as:

$$\begin{aligned}\psi_I(x,y) = &\left[\frac{\left(2\varepsilon_{si}T_{si}+T_{si}^2C_{ob}\right)\left(\varepsilon_{si}+C_{of}y\right)-\left\{\varepsilon_{si}\left(C_{of}+C_{ob}\right)+T_{si}C_{of}C_{ob}\right\}y^2}{\left(2\varepsilon_{si}T_{si}+T_{si}^2C_{ob}\right)\left(\varepsilon_{si}+C_{of}\gamma\right)-\left\{\varepsilon_{si}\left(C_{of}+C_{ob}\right)+T_{si}C_{of}C_{ob}\right\}\gamma^2}\right]\\ &\times\left[\phi_\gamma(x)+\frac{C_{of}\phi_{fg}}{\varepsilon_{si}}\gamma-\frac{\left(\varepsilon_{si}C_{of}+T_{si}C_{of}C_{ob}\right)\phi_{fg}+\varepsilon_{si}C_{ob}\phi_{bg}}{\varepsilon_{si}T_{si}\left(2\varepsilon_{si}+T_{si}C_{ob}\right)}\gamma^2\right]\\ &-\left[\frac{C_{of}\phi_{fg}}{\varepsilon_{si}}y-\frac{\left(\varepsilon_{si}C_{of}+T_{si}C_{of}C_{ob}\right)\phi_{fg}+\varepsilon_{si}C_{ob}\phi_{bg}}{\varepsilon_{si}T_{si}\left(2\varepsilon_{si}+T_{si}C_{ob}\right)}y^2\right]\end{aligned} \tag{3.6}$$

On replacing $\psi_I(x,y)$ from (2.1) using (3.6), and on putting $y = \gamma$, a 2nd order differential equation in $\psi_\gamma(x)$ is obtained as,

$$\frac{\partial^2\psi_\gamma(x)}{\partial x^2}-\frac{\left\{\psi_\gamma(x)-\psi_{Long,\gamma}\right\}}{\lambda_\gamma^2}=0 \tag{3.7}$$

with the generic solution (having boundary condition dependent unknown coefficients A_1 and A_2) as given below:

$$\psi_I(x, y=\gamma)=\psi_\gamma(x)=A_1\exp\left(\frac{x}{\lambda_\gamma}\right)+A_2\exp\left(\frac{-x}{\lambda_\gamma}\right)+\psi_{Long,\gamma} \quad (3.8)$$

where

$$\lambda_\gamma=\sqrt{\frac{\left(2\varepsilon_{si}T_{si}+T_{si}^2C_{ob}\right)\left(\varepsilon_{si}+C_{of}\gamma\right)-\left\{\varepsilon_{si}\left(C_{of}+C_{ob}\right)+T_{si}C_{of}C_{ob}\right\}\gamma^2}{2\left\{\varepsilon_{si}\left(C_{of}+C_{ob}\right)+T_{si}C_{of}C_{ob}\right\}}} \quad (3.9)$$

$$\psi_{Long,\gamma}=\frac{qN_d\lambda_\gamma^{\,2}}{\varepsilon_{si}}+\phi_{fg}-\frac{\left(\phi_{fg}-\phi_{bg}\right)\left(\varepsilon_{si}C_{ob}+C_{of}C_{ob}\gamma\right)}{\varepsilon_{si}\left(C_{of}+C_{ob}\right)+T_{si}C_{of}C_{ob}} \quad (3.10)$$

In the above expressions, λ_γ and $\psi_{\mathrm{Long},\gamma}$ denotes the characteristic length and long channel potential for asymmetric DG JL MOSFET, respectively, assuming channel conduction is taking place at any arbitrary location $y = \gamma$.

3.2.2 Depleted Portions of G-S/D Underlap (Region II/III)

In regions II and III, 1D Poisson's equation in (2.11) and (2.12) are utilized to derive the potential distributions $\psi_{\mathrm{II}}(x)$ and $\psi_{\mathrm{III}}(x)$, with general solutions identical to (2.13) and (2.14) as written below:

$$\psi_{II}(x)=V_S-E_S\left(x+d_S\right)-\frac{qN_d}{2\varepsilon_{si}}\cdot\left(x+d_S\right)^2 \quad (3.11)$$

$$\psi_{III}(x)=V_D-E_D\left(x-L_g-d_D\right)-\frac{qN_d}{2\varepsilon_{si}}\cdot\left(x-L_g-d_D\right)^2 \quad (3.12)$$

The expressions for E_{S}, E_{D}, V_{S}, and V_{D} are estimated using the lateral boundary conditions at $x = -d_{\mathrm{S}}$ and $x = L_{\mathrm{g}} + d_{\mathrm{D}}$ assuming bias/structural asymmetries in the subsequent section of the chapter.

3.2.3 Non-Depleted Portions of G-S/D Underlap (Region IV/V)

The approximate solutions for potential in these regions are obtained by following the approach similar to the symmetric case in chapter 2:

$$\psi_{IV}(x)=B_1\exp\left(\frac{x+L_S}{\lambda_D}\right)+B_2\exp\left(\frac{-\left(x+L_S\right)}{\lambda_D}\right)+V_{biD} \quad (3.13)$$

$$\psi_V(x)=C_1\exp\left(\frac{x-L_g-L_D}{\lambda_D}\right)+C_2\exp\left(\frac{-\left(x-L_g-L_D\right)}{\lambda_D}\right)+V_{biD}+V_{ds} \quad (3.14)$$

It can be noticed that (3.13) and (3.14) is a function of non-identical S/D underlap length, L_S and L_D, respectively. The values for unknown coefficients B_1, B_2, C_1 and C_2 also depend on the boundary conditions under structural/bias asymmetry.

3.2.4 Channel Potential Distribution

Following boundary and continuity conditions in (3.15) are used to determine the expressions for coefficients in (3.8) and (3.11)-(3.14).

$$\psi_I(0,\gamma)=\psi_{II}(0),\ \psi_I(L_g,\gamma)=\psi_{III}(L_g) \tag{3.15a}$$

$$\left.\frac{d\psi_I(x,\gamma)}{dx}\right|_{x=0}=\left.\frac{d\psi_{II}(x)}{dx}\right|_{x=0},\ \left.\frac{d\psi_I(x,\gamma)}{dx}\right|_{x=L_g}=\left.\frac{d\psi_{III}(x)}{dx}\right|_{x=L_g} \tag{3.15b}$$

$$\psi_{IV}(\infty)=V_{biD},\ \psi_{IV}(-L_S)=V_{biSD} \tag{3.15c}$$

$$\psi_V(-\infty)=V_{biD}+V_{ds},\ \psi_V(L_g+L_D)=V_{biSD}+V_{ds} \tag{3.15d}$$

$$\psi_{II}(-d_S)=\psi_{IV}(-d_S),\ \psi_{III}(L_g+d_D)=\psi_V(L_g+d_D) \tag{3.15e}$$

$$\left.\frac{d\psi_{II}(x)}{dx}\right|_{x=-d_S}=\left.\frac{d\psi_{IV}(x)}{dx}\right|_{x=-d_S},\ \left.\frac{d\psi_{III}(x)}{dx}\right|_{x=L_g+d_D}=\left.\frac{d\psi_V(x)}{dx}\right|_{x=L_g+d_D} \tag{3.15f}$$

Subsequently, the entire 1D channel potential from ($x = -L_S$) to ($x = L_g + L_D$) at $y = \gamma$ is obtained by using following expressions:

$$A_1=\frac{-g\ \exp(-L_g/\lambda_\gamma)+h}{2\sinh(L_g/\lambda_\gamma)},\quad A_2=\frac{g\ \exp(L_g/\lambda_\gamma)-h}{2\sinh(L_g/\lambda_\gamma)} \tag{3.16a}$$

$$V_S=V_{biD}+\Delta V_{bi}\exp\left(\frac{d_S-L_S}{\lambda_D}\right),\ E_S=\frac{\Delta V_{bi}}{\lambda_D}\exp\left(\frac{d_S-L_S}{\lambda_D}\right) \tag{3.16b}$$

$$V_D=V_{biD}+V_{ds}+\Delta V_{bi}\exp\left(\frac{d_D-L_D}{\lambda_D}\right),\ E_D=\frac{-\Delta V_{bi}}{\lambda_D}\exp\left(\frac{d_D-L_D}{\lambda_D}\right) \tag{3.16c}$$

$$B_1=0,\ B_2=\Delta V_{bi},\ C_1=\Delta V_{bi}\ \text{and}\ C_2=0 \tag{3.16d}$$

where $g = V_S-\psi_{Long,\gamma}-E_S d_S-(qN_d/2\varepsilon_{si})d_S^{\,2}$ $\Delta V_{bi}=V_{biSD}-V_{biD}$ and $h=V_D-\psi_{Long,\gamma}+E_D d_D-(qN_d/2\varepsilon_{si})d_D^{\,2}$

The values of d_S and d_D are obtained by simultaneously solving (3.17) and (3.18) numerically:

$$k_a d_S^{\,2} + k_b d_S + k_c d_D^{\,2} + \left(k_d + k_e d_S\right) \exp\left(\left(d_S - L_S\right)/\lambda_D\right) + \left(k_f + k_g d_D\right) \exp\left(\left(d_D - L_D\right)/\lambda_D\right) + k_{h1} = 0 \quad (3.17)$$

$$k_a d_D^{\,2} + k_b d_D + k_c d_S^{\,2} + \left(k_d + k_e d_D\right) \exp\left(\left(d_D - L_D\right)/\lambda_D\right) + \left(k_f + k_g d_S\right) \exp\left(\left(d_S - L_S\right)/\lambda_D\right) + k_{h2} = 0 \quad (3.18)$$

where,

$$k_a = \frac{-qN_d}{2\varepsilon_{si}} \cosh\left(L_g/\lambda_\gamma\right),\ k_b = \frac{-qN_d\lambda_\gamma}{\varepsilon_{si}} \sinh\left(L_g/\lambda_\gamma\right),\ k_c = \frac{-qN_d}{2\varepsilon_{si}},$$

$$k_d = \Delta V_{bi}\left(\cosh\left(\frac{L_g}{\lambda_\gamma}\right) - \frac{\lambda_N}{\lambda_D}\sinh\left(\frac{L_g}{\lambda_\gamma}\right)\right),\ k_e = \frac{-\Delta V_{bi}}{\lambda_D}\cosh\left(\frac{L_g}{\lambda_\gamma}\right),\ k_f = \frac{\Delta V_{bi}}{\lambda_D},$$

$$k_g = -\Delta V_{bi},\ k_{h1} = \left(\left(V_{biD} - \psi_{Long,\gamma}\right)\cosh\left(L_g/\lambda_\gamma\right) - \left(V_{biD} + V_{ds} - \psi_{Long,\gamma}\right)\right),$$

$$k_{h2} = \left(\left(V_{biD} + V_{ds} - \psi_{Long,\gamma}\right)\cosh\left(L_g/\lambda_\gamma\right) - \left(V_{biD} - \psi_{Long,\gamma}\right)\right)$$

3.2.5 Position of Subthreshold Conduction

Suzuki *et al.*, [130] have demonstrated that the maximum potential along the semiconductor indicates the position from where the subthreshold current flows and is mostly affected by the gate length variations. Thus, by computing $\partial\psi_I(x, y)/\partial y = 0$ at $x = L_g/2$ and $y = y_m$ results in an approximate position of the subthreshold conduction (y_m), as given below:

$$y_m \approx \frac{T_{si} C_{of} \left(2\varepsilon_{si} + T_{si} C_{ob}\right)\left(\psi_f\left(L_g/2\right) - \phi_{fg}\right)}{2\left[\left(\varepsilon_{si} C_{of} + T_{si} C_{of} C_{ob}\right)\left(\psi_f\left(L_g/2\right) - \phi_{fg}\right) + \varepsilon_{si} C_{ob}\left(\psi_f\left(L_g/2\right) - \phi_{bg}\right)\right]} \quad (3.19)$$

3.2.6 Exceptional Cases and Modifications

Two special cases must be treated appropriately to achieve a physics-based model, as discussed below:

i) The feasible range of y_m is [0, T_{si}]. If y_m obtains from (3.19) lies outside the silicon film boundaries, then y_m must be assigned with the nearest boundary (0 or T_{si}).

ii) Similar to one discussed in subsection 2.3.2, the feasible range of d_S and d_D is [0, L_S] and [0, L_D], respectively, in the subthreshold region. If ($d_S > L_S$) or ($d_D > L_D$) for any device specification or bias

condition, then set ($d_S = L_S$) or ($d_D = L_D$) and remove corresponding region-IV or region-V from the developed model. The coefficients A_1, A_2, V_S and V_D are calculated using (3.16). But, E_S and E_D must be computed using similar expressions, as mentioned in (2.30) and (2.31), respectively, at $y = \gamma$.

3.2.7 Subthreshold Drain Current

A similar procedure is adopted to evaluate the subthreshold drain current as discussed in previous chapter subsection 2.3.3,

$$I_{ds} = \frac{k T W_g \mu_n n_i \left(1 - \exp\left(-\beta V_{ds}\right)\right)}{\left[\int_{-d_S}^{0} \frac{dx}{G_{II}(x)} + \int_{0}^{L_g} \frac{dx}{G_I(x)} + \int_{L_g}^{L_g + d_D} \frac{dx}{G_{III}(x)}\right]} \tag{3.20}$$

where

$$G_I(x) = \int_0^{T_{si}} \exp\left(\beta \psi_I(x, y)\right) dy = \int_0^{T_{si}} \exp\left(\beta\left(a_0(x) + a_1(x)\, y + a_2(x)\, y^2\right)\right) dy$$

$$= \sqrt{\frac{-\pi}{4\,\beta a_2(x)}}\, \exp\left(a_0(x) - \frac{\beta\left(a_1(x)\right)^2}{4\, a_2(x)}\right)\left[erf\left(\frac{a_1(x)}{2\sqrt{-a_2(x)/\beta}}\right) - erf\left(\frac{a_1(x) + 2a_2(x)\, T_{si}}{2\sqrt{-a_2(x)/\beta}}\right)\right]$$

$$G_{II}(x) = \int_0^{T_{si}} \exp\left(\beta \psi_{II}(x)\right) dy = T_{si} \exp\left(\beta \psi_{II}(x)\right)$$

$$G_{III}(x) = \int_0^{T_{si}} \exp\left(\beta \psi_{III}(x)\right) dy = T_{si} \exp\left(\beta \psi_{III}(x)\right)$$

$$a_0(x) = \psi_f(x), \;\; a_1(x) = \left(C_{of} / \varepsilon_{si}\right)\left(\psi_f(x) - \phi_{fg}\right) \quad \text{and}$$

$$a_2(x) = -\frac{\left(\varepsilon_{si} C_{of} + T_{si} C_{of} C_{ob}\right)\left(\psi_f(x) - \phi_{fg}\right) + \varepsilon_{si} C_{ob}\left(\psi_f(x) - \phi_{bg}\right)}{\varepsilon_{si} T_{si}\left(2\varepsilon_{si} + T_{si} C_{ob}\right)}$$

The above coefficients (a_0, a_1 and a_2) are rewritten in terms of $\psi_m(x)$ (= $\psi_I(x, y_m)$), where $\psi_f(x)$ (= $\psi_I(x, 0)$) is replaced by the following expression

$$\psi_f(x) = \left[1 + \frac{C_{of}}{\varepsilon_{si}} y_m - \left\{\frac{\varepsilon_{si}\left(C_{of} + C_{ob}\right) + T_{si} C_{of} C_{ob}}{\varepsilon_{si} T_{si}\left(2\varepsilon_{si} + T_{si} C_{ob}\right)}\right\} y_m^2\right]^{-1}$$

$$\times \left[\psi_m(x) + \frac{C_{of}\, \phi_{fg}}{\varepsilon_{si}} y_m - \frac{\left(\varepsilon_{si} C_{of} + T_{si} C_{of} C_{ob}\right)\phi_{fg} + \varepsilon_{si} C_{ob}\, \phi_{bg}}{\varepsilon_{si} T_{si}\left(2\varepsilon_{si} + T_{si} C_{ob}\right)} y_m^2\right] \tag{3.21}$$

3.3 RESULTS AND MODEL VALIDATION

The developed model results (denoted by solid lines in the subsequent figures) are verified with results derived from Silvaco Atlas device simulator (marked by symbols) [25]. Simulation details are the same as described in the earlier subsection 2.4.1 of chapter 2. The following device parameters are chosen for the analysis of asymmetric DG JL MOSFET: T_{si} = 10 nm, $N_{sd} = 10^{20}$ cm^{-3}, W_g = 1 µm, L_g and N_d varies from 10 nm to 100 nm and 10^{18} cm^{-3} to 2×10^{19} cm^{-3}, respectively. Also, the values for T_{oxf} (and T_{oxb}), φ_{fg} (and φ_{bg}), and L_S (and L_D) ranges from 1 nm to 2 nm, 4.8 eV to 5.2 eV and 0 nm to 20 nm, respectively.

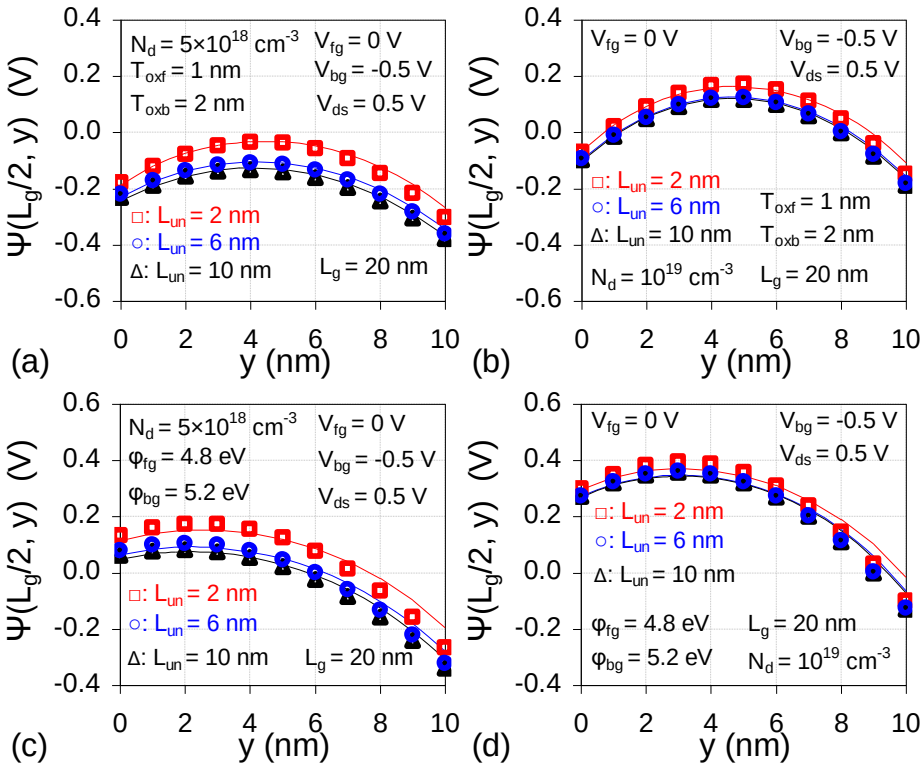

Fig. 3.2 Variation of electrostatic potential along the *y*-direction at $x = L_g/2$ with identical S/D underlap length L_{un} (= L_S = L_D) for **(a)**, **(b)** $T_{oxf} \neq T_{oxb}$ and φ_g (= φ_{fg} = φ_{bg}) = 5.1 eV, and **(c)**, **(d)** $\varphi_{fg} \neq \varphi_{bg}$ and T_{ox} (= T_{oxf} = T_{oxb}) = 2 nm. In figure parts **(a)**, **(c)** $N_d = 5\times10^{18}$ cm^{-3} and **(b)**, **(d)** $N_d = 10^{19}$ cm^{-3}. Lines show model results and symbols denote simulation data.

3.3.1 Electrostatic Potential Profiles under Asymmetries

Fig. 3.2(a)-(d) captures the effect of identical S/D underlap length (L_{un})

and channel doping on the electrostatic potential under gate workfunction ($\varphi_{fg} \neq \varphi_{bg}$) and oxide ($T_{oxf} \neq T_{oxb}$) asymmetries. The developed model results agree well with the simulation data. For a fixed N_d and L_{un}, the y_m shift (relative to the centre of the film) is larger for asymmetric workfunction than the asymmetric oxide thickness case. For a constant N_d but relatively long L_{un}, a lower channel potential is achieved owing to a greater depletion of the channel region by the gate fields. Also, a profound difference in potential with L_{un} is observed for lower doping.

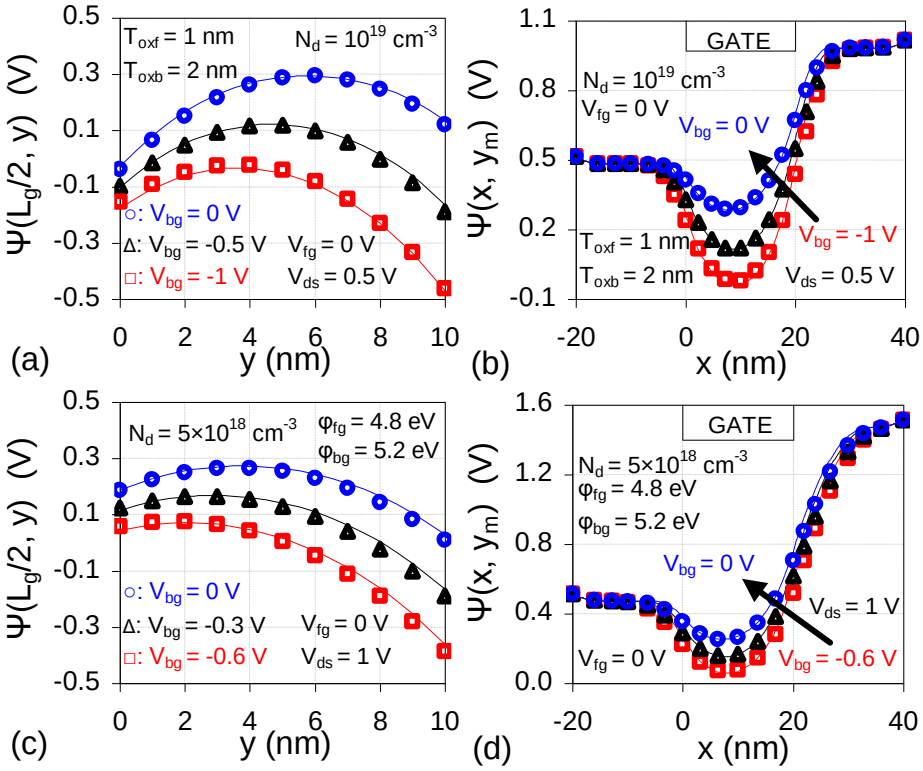

Fig. 3.3 Dependence of electrostatic potential **(a), (c)** along the *y*-direction at $x = L_g/2$, and **(b), (d)** along the *x*-direction at $y = y_m$ on V_{bg} for **(a)**, **(b)** $N_d = 10^{19}$ cm^{-3}, $T_{oxf} \neq T_{oxb}$ and $\varphi_g = 5.1$ eV, and **(c)**, **(d)** $N_d = 5\times10^{18}$ cm^{-3}, $\varphi_{fg} \neq \varphi_{bg}$ and $T_{ox} = 2$ nm. Other parameters: $L_g = L_{un} = 20$ nm and $T_{si} = 10$ nm. Lines show model results and symbols denote simulation data.

Next, Fig. 3.3(a)-(d) plots the modeled electrostatic potential under independent gate operation for $T_{oxf} \neq T_{oxb}$ and $\varphi_{fg} \neq \varphi_{bg}$ cases, which shows good agreement with the simulation. Results present that a more negative back gate bias causes the electrons to deplete more from the channel region, and hence, the channel potential decreases. The effect of negative

V_{bg} is more significant at the maximum potential at $y = y_m$ (in the vicinity of the centre of the film) than at the front surface, in Fig. 3.3(a),(c). The closer y_m is to the back surface, the more prominent variations in $\psi_m(x)$ with V_{bg} is obtained, as can be observed in Fig. 3.3(b),(d). Nonetheless, a more negative V_{bg} forces y_m to shift towards the front surface (or away from the back surface), as clearly observed in Fig. 3.3(a).

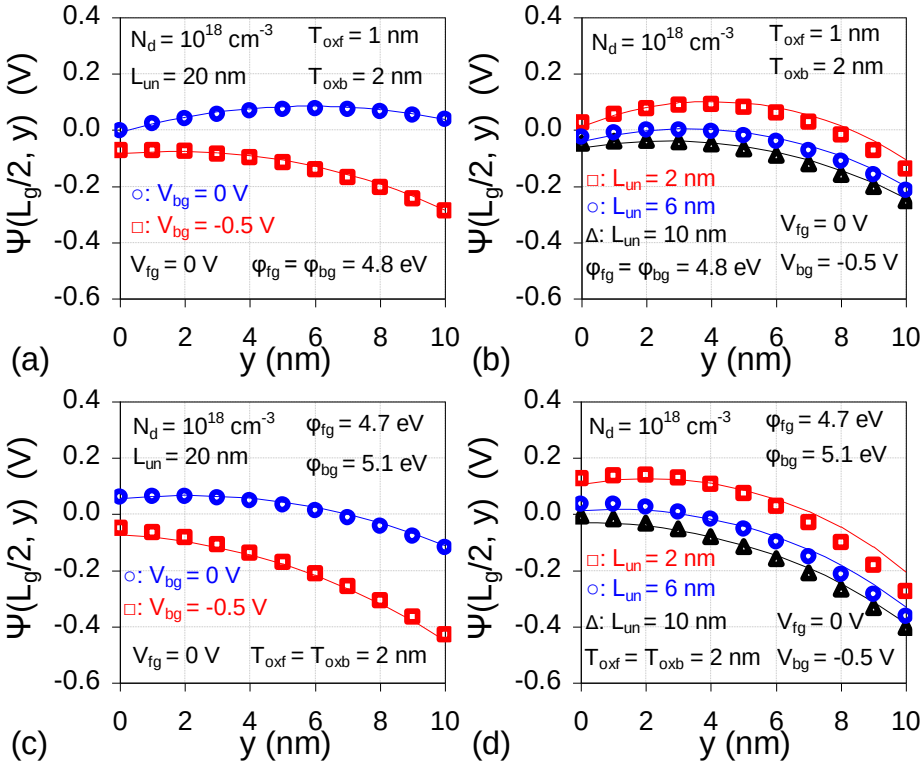

Fig. 3.4 Dependence of electrostatic potential along the y-direction at $x = L_g/2$ on **(a), (c)**, V_{bg} and varying and **(b), (d)** L_{un} for $N_d = 10^{18}$ cm^{-3} **(a), (b)**, $T_{oxf} \neq T_{oxb}$ and $\varphi_g = 4.8$ eV, and **(c), (d)** $\varphi_{fg} \neq \varphi_{bg}$ and $T_{ox} = 2$ nm. Other parameters: $L_g = 20$ nm and $T_{si} = 10$ nm. Lines show model results and symbols denote simulation data.

Moreover, Fig. 3.4(a)-(d) verifies the electrostatic potential variations for $N_d = 10^{18}$ cm^{-3}, which agree well with the simulation for oxide and workfunction asymmetries. The electrostatic potential is also validated under asymmetric underlap length ($L_S \neq L_D$) in Fig. 3.5(a)-(b). The lateral extent of source and drain depletion region increases for respective longer L_S and L_D, and is well captured by the developed model.

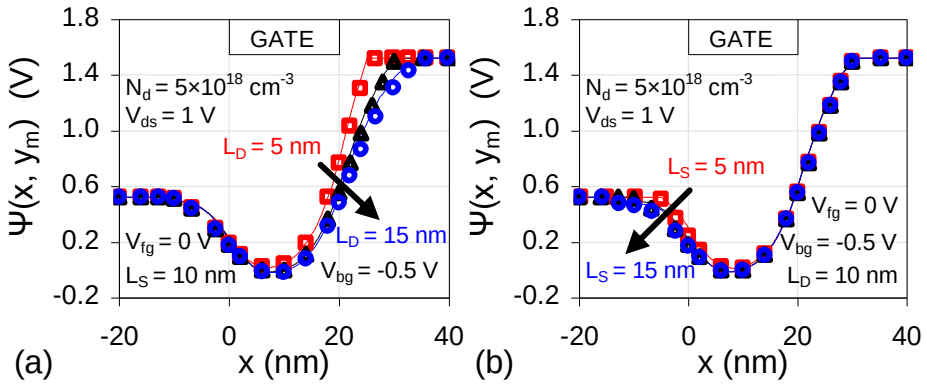

Fig. 3.5 Variation of electrostatic potential along the *y*-direction at $x = L_g/2$ with **(a)** varying L_D but fixed L_S, and **(b)** varying L_S but fixed L_D. Other parameters: L_g = 20 nm, T_{ox} = 2 nm and φ_g = 5.1 eV. Lines indicate model results and symbols represent simulation data.

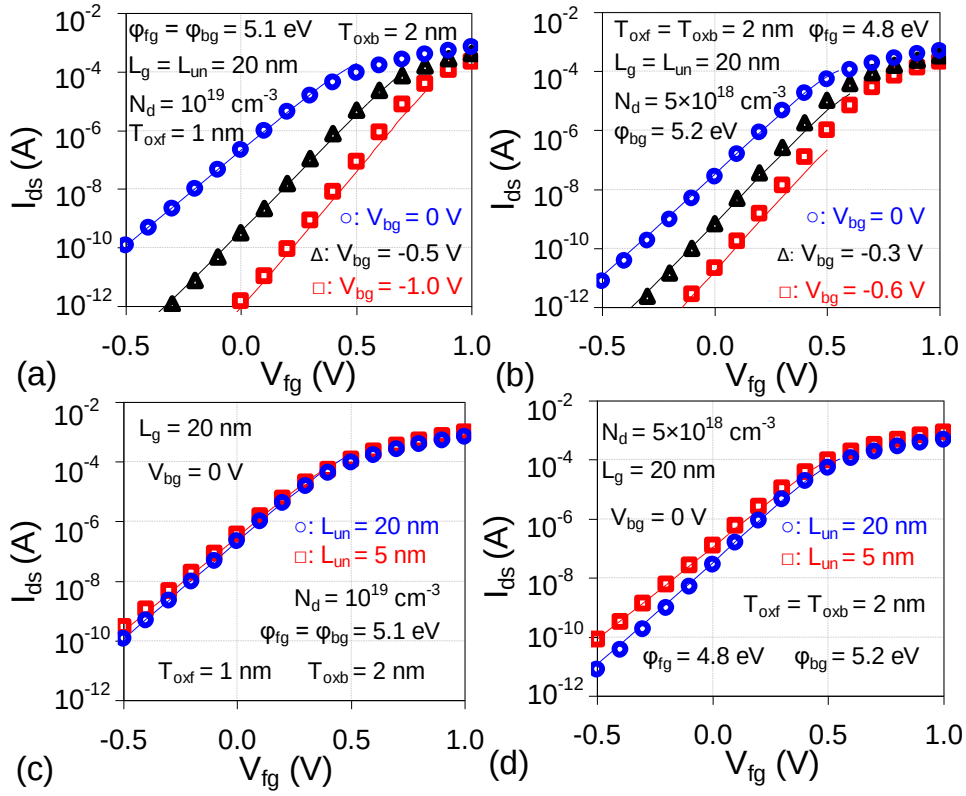

Fig. 3.6 Subthreshold drain current versus front gate bias characteristics at V_{ds} = 1 V for varying **(a)**, **(b)** V_{bg} and **(c)**, **(d)** L_{un} values. In figure parts **(a),** **(c)** $T_{oxf} \neq T_{oxb}$ and $N_d = 10^{19}$ cm^{-3}, and **(b)**, **(d)** $\varphi_{fg} \neq \varphi_{bg}$ and $N_d = 5\times10^{18}$ cm^{-3}. Lines indicate model results and symbols represent simulation data.

3.3.2 Short Channel Effects

Fig. 3.6(a)-(d) presents I_{ds}-V_{fg} characteristics for various V_{bg} and L_{un}

under structural asymmetries in gate oxide thickness and workfunction. The developed model results show good agreement with simulations. It can be observed from Fig. 3.6(a)-(b) that applying a negative back gate bias significantly suppresses I_{OFF} in an *n*-channel DG JL device. Moreover, increasing L_{un} also results in improved I_{OFF} values, particularly for relatively low values of doping (in Fig. 3.6(c)-(d)).

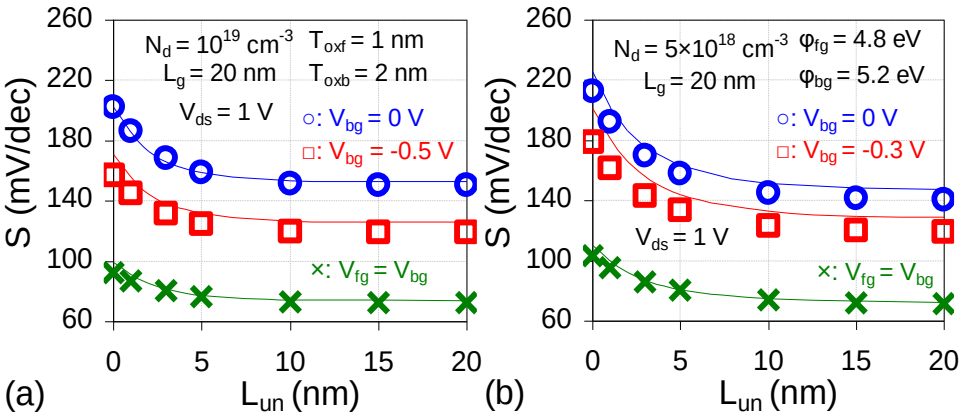

Fig. 3.7 Comparison of subthreshold swings for independently driven (V_{bg} have fixed bias value) and simultaneously driven (V_{fg} = V_{bg}) gate operation, and for different L_{un} under gate asymmetries: **(a)** $T_{oxf} \neq T_{oxb}$ and φ_g = 5.1 eV, and **(b)** $\varphi_{fg} \neq \varphi_{bg}$ and T_{ox} = 2 nm. Lines indicate model results and symbols represent simulation data.

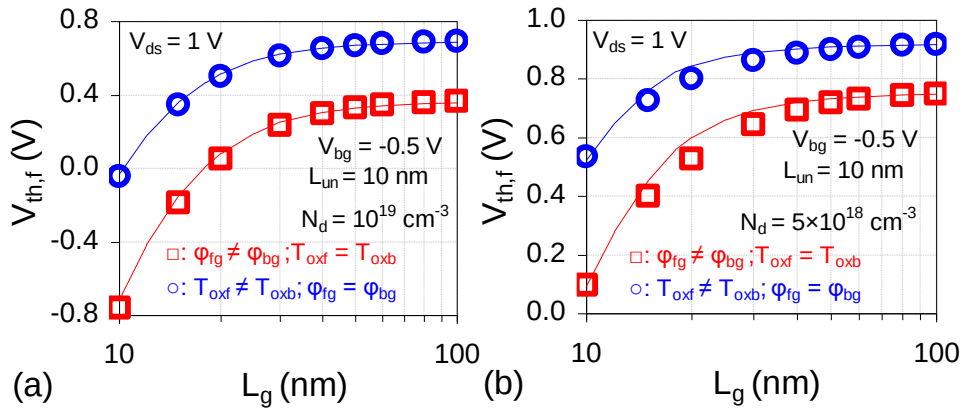

Fig. 3.8 Plot of front gate threshold voltage as a function of L_g for **(a)** N_d = 10^{19} cm^{-3} and **(b)** N_d = 5×10^{18} cm^{-3} with gate asymmetries. Lines denote model results and symbols mark simulation data.

Next, Fig. 3.7(a)-(b) plots the dependence of S on L_{un} for independently and simultaneously driven gate operations. With increasing

L_{un} values, S improves for both asymmetric ($V_{fg} \neq V_{bg}$) as well as symmetric gate bias ($V_{fg} = V_{bg}$) conditions. Also, S improves for a more negative V_{bg} value owing to a shift in the position of subthreshold conduction closer to the front surface, thereby increasing front gate controllability over the channel. However, asymmetric gate bias (V_{bg}: fixed) case possesses deteriorated S than $V_{fg} = V_{bg}$ condition due to single (front) gate control over the channel in the former case, while the channel is simultaneously controlled by both front and back gates in the latter case.

Fig. 3.8(a)-(b) depicts the variations in front gate threshold voltage ($V_{th,f}$) for various L_g. The subscript '*f*' is added explicitly to indicate that for DG MOSFET with independently-driven gates, the front gate is utilized as a driving gate, whereas the back gate is used as a control gate to tune the threshold voltage of the transistor [131]. The modeled $V_{th,f}$ roll-off with L_g reasonably agrees with the simulation for asymmetric gate workfunction (φ_{fg} = 4.8 eV, φ_{bg} = 5.2 eV; $T_{oxf} = T_{oxb}$ = 2 nm) and gate oxide (T_{oxf} = 1 nm, T_{oxb} = 2 nm; $\varphi_{fg} = \varphi_{bg}$ = 5.1 eV). The increase in $V_{th,f}$ roll-off ascertains increased SCEs with shorter L_g. Also, for same range of L_g, $V_{th,f}$ roll-off reduces considerably from $N_d = 10^{19}$ cm^{-3} (in Fig. 3.8(a)) to $N_d = 5\times10^{18}$ cm^{-3} (in Fig. 3.8(b)).

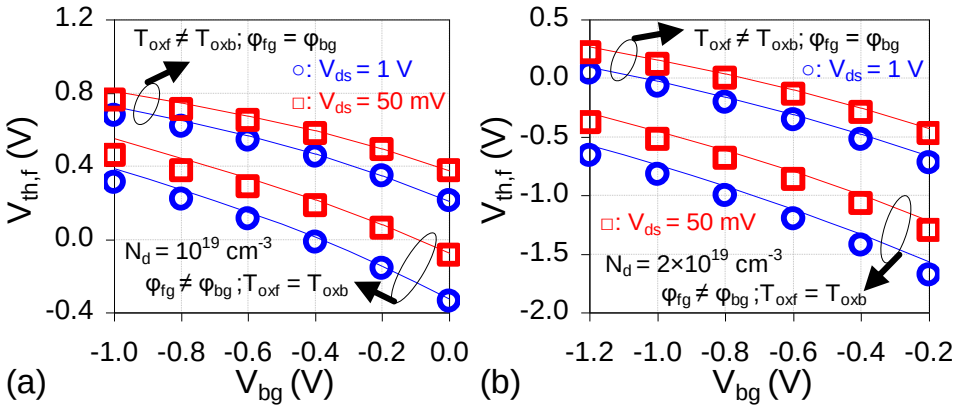

Fig. 3.9 Plot of $V_{th,f}$ versus V_{bg} at $L_g = L_{un}$ = 20 nm, V_{ds} = 50 mV and 1 V for **(a)** $N_d = 10^{19}$ cm^{-3} and **(b)** $N_d = 2\times10^{19}$ cm^{-3} with gate asymmetries. Lines denote model results and symbols indicate simulation data.

3.3.3 Dynamic Aspect of Threshold Voltage

Fig. 3.9(a)-(b) captures the dynamic aspect of $V_{th,f}$ by altering V_{bg} for

$N_d = 10^{19}$ cm^{-3} and 2×10^{19} cm^{-3} under asymmetric gate workfunction (φ_{fg} = 4.8 eV, φ_{bg} = 5.2 eV; $T_{oxf} = T_{oxb}$ = 2 nm) and gate oxide thickness (T_{oxf} = 1 nm, T_{oxb} = 2 nm; $\varphi_{fg} = \varphi_{bg}$ = 5.1 eV). A larger positive $V_{th,f}$ is achieved by reducing V_{bg} to a more negative value. Also, a marginal decrease in the $V_{th,f}$ difference between V_{ds} = 1 V and V_{ds} = 50 mV reflects on the improvement in the front gate controllability for negative V_{bg}. It is emphasized here that the developed model is expected to be valid in the subthreshold operating region and does not incorporate holes build-up at the back surface for sufficiently negative V_{bg}. Since the prime objective of the model is to predict SCEs in asymmetric DG JL devices with underlap, and hence, the inclusion of inversion at the back surface is treated as outside the scope of the present thesis.

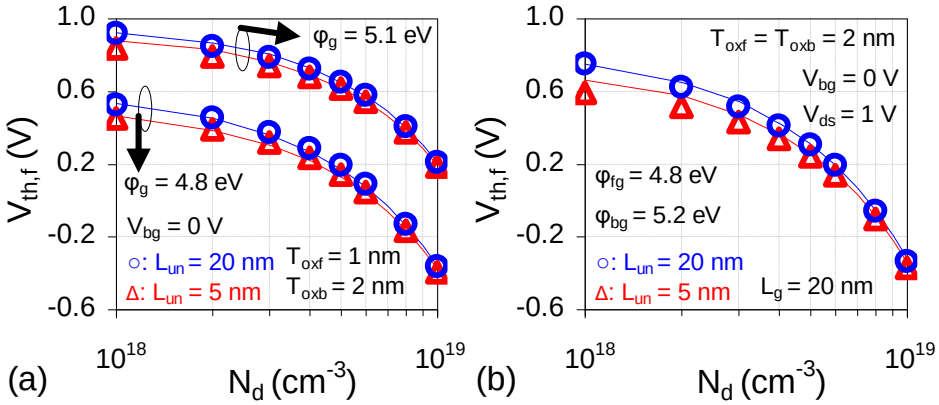

Fig. 3.10 Plot of $V_{th,f}$ as a function of N_d at V_{ds} = 1 V for L_{un} = 5 nm and 20 nm, **(a)** $T_{oxf} \neq T_{oxb}$, φ_g = 5.1 eV and φ_g = 4.8 eV, and **(b)** $\varphi_{fg} \neq \varphi_{bg}$ and T_{ox} = 2 nm. Lines denote model results and symbols indicate simulation data.

In addition to back gate bias, L_{un} and N_d can also be altered to tune $V_{th,f}$, as shown in Fig. 3.10(a)-(b) for non-identical gate oxide thicknesses and workfunctions. $V_{th,f}$ reaches positive values for lower N_d, and the improvement in $V_{th,f}$ by increasing L_{un} is significant for lower doping. Alternatively, at same V_{bg} and L_{un}, identical values of $V_{th,f}$ (e.g. $V_{th,f} \approx 0.2$ V) can be obtained for either moderate φ_g - moderate N_d (4.8 eV - 5×10^{18} cm^{-3}) or high φ_g - high N_d (5.1 eV - 10^{19} cm^{-3}) pair, as elucidated in Fig. 3.10(a). Similarly, for $N_d = 6\times10^{18}$ cm^{-3}, choosing L_{un} = 20 nm than L_{un} = 5 nm at V_{bg} = 0 V also yields $V_{th,f} \approx 0.2$ V, as noticed in Fig. 3.10(b).

3.4 CONCLUSION

The chapter has investigated a generic model for estimating channel potential and SCEs in self-aligned DG JL transistor for independent gate operation while incorporating asymmetries in gate workfunctions, oxide thicknesses and S/D underlap lengths. The modeled results are in good agreement with the simulated data in the subthreshold region. The analysis has shown that an independent gate operation in DG JL transistor can offer wide flexibility to enhance the device performance through optimization of I_{OFF}, S and $V_{th,f}$. Apart from V_{bg}, the developed model proposes that N_d and L_{un} can also provide added flexibility to improve device performance further. Results suggest that the choice of appropriate V_{bg} together with moderate N_d and sufficiently longer L_{un} can be optimum for asymmetric DG JL device (specific to LP subthreshold logic technology).

Chapter 4

Modeling-based Optimization of Short Channel Effects in Core-Shell Junctionless Transistor

4.1 INTRODUCTION

Despite the various inherent benefits of heavy (uniform) doping in conventional JL devices [30]-[34], these transistors suffer from detrimental effects that can be unfavorable for downscaling and LP applications. These adverse effects include off-state BTBT [40], [154], RDFs [43]-[46], mobility degradations due to impurity scattering [35], [36], fin width variations [41], [42], and limits on the choice of gate workfunction for obtaining appropriate threshold voltage [31], [49]. Recently, an innovative JL transistor possessing Shell Doping Profile (SDP) [124], [125] has experimentally demonstrated improved *S*, higher I_{ON}/I_{OFF} ratio, and lower sensitivity towards RDFs and fin-width variations than uniformly doped JL transistors [124]-[127]. These devices have also shown to offer suppressed off-state BTBT current [155] and higher mobility values [156], thus indicating favorable prospects for downscaling and LP technology.

The uniform doping profile across the channel region in a conventional JL transistor assist the gate electric field to modulate the channel potential laterally beyond the gated portion in the subthreshold region [97], [115], [123], [157]. On the other hand, JL transistor with SDP (termed as Core-Shell (CS) JL transistor) consists of near-surface heavily doped shell regions separated by central undoped or lightly doped core region [124]-[127], [155], [156]. In addition to the gate field-induced modulation of channel potential (outside the gated portion), the diffusion of carriers takes

place along the lateral as well as vertical directions in such a device [127]. Consequently, 2D distribution of channel potential in the S/D extension regions is achieved, and the existing methodologies for conventional JL MOSFETs [97], [116], [146], [157] cannot be directly utilized to model subthreshold channel potential in these devices. In this chapter, the channel potential and SCEs in CS DG JL MOSFET is estimated through a semi-analytical model developed by evaluating region-wise 2D Poisson's equations in the subthreshold operating regime.

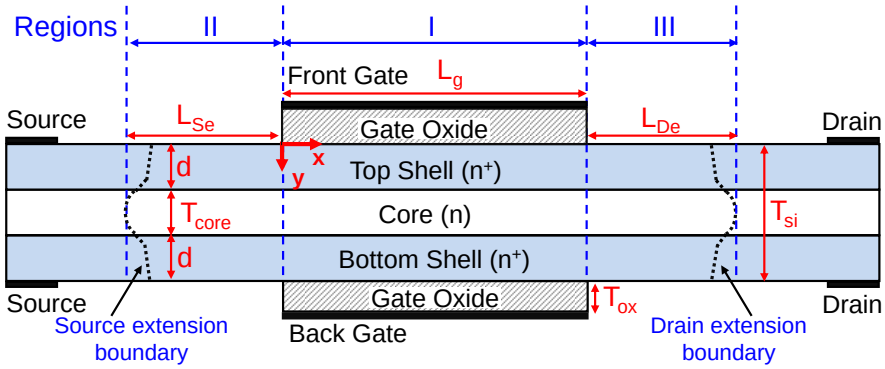

Fig. 4.1 Schematic view of *n*-channel CS DG JL MOSFET.

4.2 REGION-WISE MODELING ASSUMPTIONS

An *n*-channel (symmetric) CS DG JL MOSFET is analyzed for model derivation in the subthreshold operating regime, as shown in Fig. 4.1. The silicon film of thickness T_{si} is vertically sliced into three parts namely top shell, core and bottom shell having corresponding region boundaries as $[0 \leq y \leq (T_{si} - T_{core})/2]$, $[(T_{si} - T_{core})/2 \leq y \leq (T_{si} + T_{core})/2]$ and $[(T_{si} + T_{core})/2 \leq y \leq T_{si}]$. The doping transition between the shell and core portions is assumed to be abrupt such that $d = (T_{si} - T_{core})/2$, where d is the shell depth and T_{core} is the core thickness. The shell portions are heavily doped with doping concentration N_d, whereas the core part is left undoped (or lightly doped) having doping concentration N_0. Also, the channel region is laterally split into three portions namely gated (region-I), source extension (region-II) and drain extension (region-III) portions, having region boundaries as $[0 \leq x \leq L_g]$, $[-L_{Se} \leq x \leq 0]$ and $[L_g \leq x \leq L_g + L_{De}]$, respectively. Here, L_{Se} and L_{De} denote lengths of the source and drain

extension regions at the centre of the Si film. The S/D extension regions include the portions outside the gated region up to which the modulation of channel potential due to the gate field occurs.

Throughout this chapter, Boltzmann's carrier statistics are utilized because the analyzed shell doping ($N_d \leq 2\times10^{19}$ cm^{-3}) is relatively low than N_C [90]. Doping-dependent bandgap narrowing effect is accounted through an increase in intrinsic carrier concentration in the shell (n_{id}) as compared to the core (n_{i0}) [25]. Also, the doping-dependent mobility enhancement in the core than shell region is considered through concentration-dependent electron mobility in core and shell regions, indicated by μ_{nd} and μ_{n0}, respectively, where $\mu_{n0} > \mu_{nd}$ [25], [126], [127]. As a first-order approximation, QCE is neglected in the model development, thereby limiting the validity of the developed model for $T_{si} \geq 7$ nm [81], [122].

4.3 MODEL DERIVATION

In the subthreshold regime, TCAD simulation of CS DG JL MOSFET confirms that the electron concentration in the shell region is significantly less than N_d in all regions (I-III). In contrast, the electron concentration is much greater than N_0 in regions II and III of the core portion. Consequently, region-wise 2D Poisson's equations are utilized to obtain the channel potential distributions, as given below:

i) Top Shell Portion: Assuming depletion approximation [99],

$$\frac{\partial^2\psi_{i,st}(x,y)}{\partial x^2}+\frac{\partial^2\psi_{i,st}(x,y)}{\partial y^2}=\frac{-qN_d}{\varepsilon_{si}} \tag{4.1}$$

ii) Core Portion: Considering electron concentration and doping [99],

$$\frac{\partial^2\psi_{i,cr}(x,y)}{\partial x^2}+\frac{\partial^2\psi_{i,cr}(x,y)}{\partial y^2}=\frac{-q}{\varepsilon_{si}}\left[N_0-n_{i0}e^{\beta\left(\psi_{i,cr}(x,y)-V_f(x,y)\right)}\right] \tag{4.2}$$

iii) Bottom Shell Portion: Assuming depletion approximation [99],

$$\frac{\partial^2\psi_{i,sb}(x,y)}{\partial x^2}+\frac{\partial^2\psi_{i,sb}(x,y)}{\partial y^2}=\frac{-qN_d}{\varepsilon_{si}} \tag{4.3}$$

where *i* indicates regions I, II or III. It is rather difficult to obtain complete yet analytical solutions for (4.1)-(4.3), and hence, appropriate region-wise

approximations are utilized to develop a simplified analytical model to predict the channel potential distribution in the Si film.

4.3.1 Parabolic Potential Approximation

The potential distribution in the shell and core regions is approximated by distinct region-wise parabolic potential approximations along the *y*-direction [130], as given below:

$$\psi_{i,st}(x,y) = a_{i0}(x) + a_{i1}(x)\cdot y + a_{i2}(x)\cdot y^2 \tag{4.4}$$

$$\psi_{i,cr}(x,y) = b_{i0}(x) + b_{i1}(x)\cdot(y - T_{si}/2) + b_{i2}(x)\cdot(y - T_{si}/2)^2 \tag{4.5}$$

$$\psi_{i,sb}(x,y) = c_{i0}(x) + c_{i1}(x)\cdot(y - T_{si}) + c_{i2}(x)\cdot(y - T_{si})^2 \tag{4.6}$$

The *x*-dependent coefficients in (4.4)-(4.6) are evaluated using appropriate boundary conditions in each region (I-III), as mentioned below:

a) Potentials at the front and back surfaces, ($\psi_{Si}(x)$) in regions I-III,

$$\psi_{i,st}(x,0) = \psi_{i,sb}(x,T_{si}) = \psi_{Si}(x) \tag{4.7}$$

b) Potential at the centre, ($\psi_{Ci}(x)$) in regions I-III,

$$\psi_{i,cr}(x,T_{si}/2) = \psi_{Ci}(x) \tag{4.8}$$

c) In region-I, electric field at the front and back surfaces,

$$\left.\frac{\partial\psi_{I,st}(x,y)}{\partial y}\right|_{y=0} = \left.\frac{-\partial\psi_{I,sb}(x,y)}{\partial y}\right|_{y=T_{si}} = \frac{C_{ox}\left(\psi_{Si}(x) - \phi_{gs}\right)}{\varepsilon_{si}} \tag{4.9a}$$

While in regions II and III, assuming the negligible effect of outer fringing fields from the gate electrode [80], [141], electric field at the front and back surfaces can be approximated as,

$$\left.\partial\psi_{j,st}(x,y)/\partial y\right|_{y=0} = -\left.\partial\psi_{j,sb}(x,y)/\partial y\right|_{y=T_{si}} \cong 0 \tag{4.9b}$$

where the notation *j* indicates region-II or region-III only.

d) In regions I-III, the potential and vertical component of the electric field are continuous at both top and bottom shell-core interfaces,

$$\psi_{i,st}(x,(T_{si} - T_{core})/2) = \psi_{i,cr}(x,(T_{si} - T_{core})/2) \tag{4.10a}$$

$$\psi_{i,cr}(x,(T_{si} + T_{core})/2) = \psi_{i,sb}(x,(T_{si} + T_{core})/2) \tag{4.10b}$$

$$\left.\frac{\partial\psi_{i,st}(x,y)}{\partial y}\right|_{y=(T_{si}-T_{core})/2} = \left.\frac{\partial\psi_{i,cr}(x,y)}{\partial y}\right|_{y=(T_{si}-T_{core})/2} \tag{4.10c}$$

$$\left.\frac{\partial \psi_{i,cr}(x,y)}{\partial y}\right|_{y=(T_{si}+T_{core})/2} = \left.\frac{\partial \psi_{i,sb}(x,y)}{\partial y}\right|_{y=(T_{si}+T_{core})/2} \tag{4.10d}$$

As already discussed in chapter 2 that for symmetric DG topology, the weakest gate coupling exists at the centre of the film. Hence, the central potential (i.e. at $y = T_{si}/2$) decides the subthreshold conduction. The subsequent subsections determine the expressions for central potential in the core region for regions I-III in the subthreshold regime.

4.3.2 Gated Portion (Region-I)

The gated portion of the film is depleted of mobile carriers in the subthreshold regime, and hence, the electron concentration term is neglected in (4.2) while estimating the channel potential. On evaluating (4.4)-(4.6) using suitable conditions from (4.7)-(4.10) gives,

$$\psi_{I,st}(x,y) = \psi_{S1}(x) + \frac{C_{ox}\left(\psi_{S1}(x)-\phi_{gs}\right)}{\varepsilon_{si}} y + \frac{4\varepsilon_{si}\left(\psi_{C1}(x)-\psi_{S1}(x)\right)-C_{ox}\left(\psi_{S1}(x)-\phi_{gs}\right)\left(2T_{si}-T_{core}\right)}{\varepsilon_{si}T_{si}\left(T_{si}-T_{core}\right)} y^2 \tag{4.11}$$

$$\psi_{I,cr}(x,y) = \psi_{C1}(x) - \frac{4\varepsilon_{si}\left(\psi_{C1}(x)-\psi_{S1}(x)\right)-C_{ox}\left(\psi_{S1}(x)-\phi_{gs}\right)\left(T_{si}-T_{core}\right)}{\varepsilon_{si}T_{si}T_{core}}\left(y-\frac{T_{si}}{2}\right)^2 \tag{4.12}$$

$$\psi_{I,sb}(x,y) = \psi_{S1}(x) - \frac{C_{ox}\left(\psi_{S1}(x)-\phi_{gs}\right)}{\varepsilon_{si}}\left(y-T_{si}\right) + \frac{4\varepsilon_{si}\left(\psi_{C1}(x)-\psi_{S1}(x)\right)-C_{ox}\left(\psi_{S1}(x)-\phi_{gs}\right)\left(2T_{si}-T_{core}\right)}{\varepsilon_{si}T_{si}\left(T_{si}-T_{core}\right)}\left(y-T_{si}\right)^2 \tag{4.13}$$

To express (4.11)-(4.13) as a function of $\psi_{C1}(x)$ only, $\psi_{S1}(x)$ needs to be rewritten in terms of $\psi_{C1}(x)$. On simultaneously solving (4.1) and (4.2) at $y = d$ (= $(T_{si} - T_{core})/2$) using (4.11) and (4.12), respectively, yields

$$\psi_{S1}(x) = \frac{8\varepsilon_{si}\psi_{C1}(x) + 2C_{ox}T_{si}\phi_{gs} + q\left(N_d - N_0\right)T_{core}\left(T_{si}-T_{core}\right)}{2\left(4\varepsilon_{si}+C_{ox}T_{si}\right)} \tag{4.14}$$

Next, on substituting (4.14) into (4.12) and evaluating (4.2) at $y = T_{si}/2$ using (4.12) gives an x-dependent 2nd order differential equation in $\psi_{C1}(x)$:

$$\frac{d^2\psi_{C1}(x)}{dx^2} - \frac{\{\psi_{C1}(x) - \psi_{Long}\}}{\lambda_N{}^2} = 0 \tag{4.15}$$

where ψ_{Long} and λ_{N} are the long channel central potential and natural length for CS DG JL transistor, respectively, as given below:

$$\psi_{Long} = \phi_{gs} + \frac{q\left(N_d T_{si} + \left(N_0 - N_d\right) T_{core}\right)}{2C_{ox}} + \frac{q\left(N_d \left(T_{si} - T_{core}\right)^2 + N_0 \left(2T_{si} - T_{core}\right) T_{core}\right)}{8\varepsilon_{si}} \tag{4.16a}$$

or, $$\psi_{Long} = \phi_g + \frac{qN_d(2d) + qN_0\left(T_{si} - 2d\right)}{2C_{ox}} + \frac{qN_d\left(4d^2\right) + qN_0\left(T_{si}^2 - 4d^2\right)}{8\varepsilon_{si}} \tag{4.16b}$$

$$\lambda_N = \sqrt{\left(4\varepsilon_{si}T_{si} + C_{ox}T_{si}{}^2\right)/8C_{ox}} \tag{4.17}$$

The generalized solution for (4.15) can be given by

$$\psi_{C1}(x) = \psi_{I,cr}\left(x, y = T_{si}/2\right) = A_1 \exp\left(x/\lambda_N\right) + A_2 \exp\left(-x/\lambda_N\right) + \psi_{Long} \tag{4.18}$$

Following two observations can be made from the above expressions:

i) The derived λ_{N} for JL with SDP in (4.17) is identical to λ_{N} for uniformly doped JL in (2.9).

ii) When the shell depth equals half the film thickness, i.e. $d = T_{\text{si}}/2$, CS JL MOSFET behaves as a conventional uniformly N_{d}-doped JL MOSFET (without any core (undoped) region, i.e. $T_{\text{core}} = 0$, in Fig. 4.1). For instance, when $T_{\text{core}} = 0$, ψ_{Long} for JL with SDP in (4.16a) becomes identical to ψ_{Long} for uniformly doped JL in (2.8).

4.3.3 Source and Drain Extension Portions (Regions II and III)

In regions II and III, the potential distribution is obtained by evaluating the x-dependent coefficients in (4.4)-(4.6) by choosing appropriate conditions from (4.7)-(4.10), as follows:

$$\psi_{j,st}(x, y) = \psi_{Sj}(x) + \frac{4\left(\psi_{Cj}(x) - \psi_{Sj}(x)\right)}{T_{si}\left(T_{si} - T_{core}\right)} y^2 \tag{4.19}$$

$$\psi_{j,cr}(x, y) = \psi_{Cj}(x) - \frac{4\left(\psi_{Cj}(x) - \psi_{Sj}(x)\right)}{T_{si}T_{core}}\left(y - \frac{T_{si}}{2}\right)^2 \tag{4.20}$$

$$\psi_{j,cr}(x,y)=\psi_{Cj}(x)-\frac{4\left(\psi_{Cj}(x)-\psi_{Sj}(x)\right)}{T_{si}T_{core}}\left(y-\frac{T_{si}}{2}\right)^2 \quad (4.21)$$

Now, rewriting $\psi_{Sj}(x)$ in terms of $\psi_{Cj}(x)$ by simultaneously computing (4.1) and (4.2) at $y = d$ having potential $\psi_{Dj}(x)$ using (4.19) and (4.20), as

$$\psi_{Sj}(x)=\psi_{Cj}(x)+\frac{qT_{core}\left(T_{si}-T_{core}\right)}{8\varepsilon_{si}}\left[\left(N_d-N_0\right)+n_{i0}e^{\beta\left(\psi_{Dj}(x)-V_f(x,d)\right)}\right] \quad (4.22)$$

On substituting (4.22) into (4.20) and then simplifying (4.2) using (4.22) at $y = (T_{si}/2)$ yield a non-linear 2nd order differential equation as:

$$\begin{aligned}\frac{d^2\psi_{Cj}(x)}{dx^2}=&\frac{-q}{\varepsilon_{si}}\left(N_d-\left(N_d-N_0\right)\frac{T_{core}}{T_{si}}\right)\\&+\frac{qn_{i0}}{\varepsilon_{si}}\left[e^{\beta\left(\psi_{Cj}(x)-V_f(x)\right)}-\left(\frac{T_{si}-T_{core}}{T_{si}}\right)e^{\beta\left(\psi_{Dj}(x)-V_f(x,d)\right)}\right]\end{aligned} \quad (4.23)$$

Due to the complicated non-linear behavior of (4.23) as well as complex core-shell structure, it is difficult to derive analytical solutions for $\psi_{Cj}(x)$ from the above equation in regions II and III. To resolve this issue, the following assumption is considered. It can be observed that (4.23) closely resembles the 1D Poisson's equation [90] in which the first and second terms on the right-hand side of (4.23) depends on doping concentration and electron concentration, respectively. In the subthreshold regime, TCAD simulation ascertains that at $y = T_{si}/2$, the magnitude of the first term is more significant than the second term in region II/III. Hence, the second term can be neglected in (4.23). Consequently, a 2nd order differential equation is obtained as

$$\frac{d^2\psi_{Cj}(x)}{dx^2}=\frac{-q}{\varepsilon_{si}}\left(N_d-\left(N_d-N_0\right)\frac{T_{core}}{T_{si}}\right)=\frac{-qN_{eq}}{\varepsilon_{si}} \quad (4.24)$$

whose generic solutions for regions II and III can be written below as:

$$\psi_{C2}(x)=\psi_{II,cr}(x,y=T_{si}/2)=V_{Se}-E_{Se}\left(x+L_{Se}\right)-\frac{qN_{eq}}{2\varepsilon_{si}}\left(x+L_{Se}\right)^2 \quad (4.25)$$

$$\psi_{C3}(x)=\psi_{III,cr}(x,y=T_{si}/2)=V_{De}-E_{De}\left(x-L_g-L_{De}\right)-\frac{qN_{eq}}{2\varepsilon_{si}}\left(x-L_g-L_{De}\right)^2 \quad (4.26)$$

where $N_{eq} = (N_d - (N_d - N_0)T_{core}/T_{si})$ denotes an equivalent doping concentration at the central core region ($> N_0$). Here, E_{Se} and V_{Se} indicate

the electric field and potential, respectively, at $x = -L_{Se}$, and E_{De} and V_{De} denote the electric field and potential, respectively, at $x = L_g + L_{De}$.

4.3.4 Complete Solution for Central Channel Potential

Following boundary/continuity conditions along the lateral directions are utilized to estimate the values for unknown coefficients A_1, A_2, V_{Se}, E_{Se}, L_{Se}, V_{De}, E_{De} and L_{De} in (4.18), (4.25) and (4.26):

a) Potential developed at the outer edges of regions II and III,

$$\psi_{C2}(-L_{Se}) = V_{bi,eff} \quad \text{and} \quad \psi_{C3}(L_g + L_{De}) = V_{bi,eff} + V_{ds} \tag{4.27}$$

where $V_{bi,eff}$ signifies effective built-in voltage developed at the neutral S/D ends. The section A.2 of appendix-A at the end of this thesis presents more details on $V_{bi,eff}$.

b) Lateral component of the electric field is zero at the outer edges of regions II and III,

$$\left.\frac{d\psi_{C2}(x)}{dx}\right|_{x=-L_{Se}} = 0 \quad \text{and} \quad \left.\frac{d\psi_{C3}(x)}{dx}\right|_{x=L_g+L_{De}} = 0 \tag{4.28}$$

c) Potential and lateral component of the electric field are continuous at the gate edges,

$$\psi_{C1}(0) = \psi_{C2}(0), \quad \psi_{C1}(L_g) = \psi_{C3}(L_g) \tag{4.29a}$$

$$\left.\frac{d\psi_{C1}(x)}{dx}\right|_{x=0} = \left.\frac{d\psi_{C2}(x)}{dx}\right|_{x=0} \quad \text{and} \quad \left.\frac{d\psi_{C1}(x)}{dx}\right|_{x=L_g} = \left.\frac{d\psi_{C3}(x)}{dx}\right|_{x=L_g} \tag{4.29b}$$

After simplifying (4.18), (4.25) and (4.26) using (4.27)-(4.29), the complete solution for central channel potential ($\psi_C(x)$) along the x-direction [$-L_{Se} \le x \le (L_g + L_{De})$] is given by:

$$\psi_{C1}(x) = \frac{g\sinh\left((L_g - x)/\lambda_N\right) + h\sinh(x/\lambda_N)}{\sinh(L_g/\lambda_N)} + \psi_{Long} \tag{4.30a}$$

$$\psi_{C2}(x) = V_{bi,eff} - \frac{q N_{eq}}{2\varepsilon_{si}}(x + L_{Se})^2 \tag{4.30b}$$

$$\psi_{C3}(x) = V_{bi,eff} + V_{ds} - \frac{q N_{eq}}{2\varepsilon_{si}}(x - L_g - L_{De})^2 \tag{4.30c}$$

Also, (4.31) and (4.32) are computed to determine the values of L_{Se} and L_{De} as expressed below:

$$\left(k_1 L_{Se}^2 + k_2 L_{Se} + k_{3s}\right)^2 = -k_2 L_{Se}^2 + k_4 L_{Se} + k_{5s} \tag{4.31}$$

$$\left(k_1 L_{De}^2 + k_2 L_{De} + k_{3d}\right)^2 = -k_2 L_{De}^2 + k_4 L_{De} + k_{5d} \tag{4.32}$$

where

$$g = V_{bi,eff} - \psi_{Long} - \frac{q N_{eq}}{2\varepsilon_{si}} L_{Se}{}^2,\ h = V_{bi,eff} + V_{ds} - \psi_{Long} - \frac{q N_{eq}}{2\varepsilon_{si}} L_{De}{}^2,$$
$$q_d = 2\varepsilon_{si}/q N_{eq},\ k_1 = -\sinh\left(L_g/\lambda_N\right)/2\lambda_N,\ k_2 = -\cosh\left(L_g/\lambda_N\right),$$
$$k_{3s} = -q_d k_1\left(V_{bi,eff} - \psi_{Long}\right),\ k_{3d} = -q_d k_1\left(V_{bi,eff} + V_{ds} - \psi_{Long}\right),$$
$$k_4 = 2\lambda_N \sinh\left(L_g/\lambda_N\right),\ k_{5s} = q_d\left\{\left(V_{bi,eff} + V_{ds} - \psi_{Long}\right) + \left(V_{bi,eff} - \psi_{Long}\right)k_2\right\},$$
$$k_{5d} = q_d\left\{\left(V_{bi,eff} - \psi_{Long}\right) + \left(V_{bi,eff} + V_{ds} - \psi_{Long}\right)k_2\right\}$$

4.3.5 Electron Concentration

The electron concentration (n_e) can be obtained from the potential distribution in the shell and core regions as [143]:

$$n_{ei,st}(x,y) = n_{id}\exp\left\{\beta\left(\psi_{i,st}(x,y) - V_f(x,y)\right)\right\} \tag{4.33a}$$

$$n_{ei,cr}(x,y) = n_{i0}\exp\left\{\beta\left(\psi_{i,cr}(x,y) - V_f(x,y)\right)\right\} \tag{4.33b}$$

$$n_{ei,sb}(x,y) = n_{id}\exp\left\{\beta\left(\psi_{i,sb}(x,y) - V_f(x,y)\right)\right\} \tag{4.33c}$$

4.3.6 Subthreshold Drain Current

Simulation confirms that the quasi-Fermi potential is weakly dependent on *y*, and hence, is assumed to be invariant along the *y*-direction for current calculations. Subsequently, utilizing the Pao and Sah's double integral (as already discussed in chapter 2), the subthreshold drain current in a core-shell architecture can be evaluated as:

$$I_{ds} = \frac{kTW_g\left(1 - \exp\left(-\beta V_{ds}\right)\right)}{\left[\int_{-L_{Se}}^{0}\frac{dx}{G_{II}(x)} + \int_{0}^{L_g}\frac{dx}{G_I(x)} + \int_{L_g}^{L_g+L_{De}}\frac{dx}{G_{III}(x)}\right]} \tag{4.34}$$

where

$$G_i(x) = \mu_{nd}\, n_{id}\int_{0}^{(T_{si}-T_{core})/2}\exp\left(\beta\psi_{i,st}(x,y)\right)dy + \mu_{n0}\, n_{i0}\int_{(T_{si}-T_{core})/2}^{(T_{si}+T_{core})/2}\exp\left(\beta\psi_{i,cr}(x,y)\right)dy$$
$$+ \mu_{nd}\, n_{id}\int_{(T_{si}+T_{core})/2}^{T_{si}}\exp\left(\beta\psi_{i,sb}(x,y)\right)dy$$

4.4 RESULTS AND MODEL VALIDATION

Following device parameters are chosen to investigate CS DG JL MOSFET in this chapter: T_{ox} = 1 nm, T_{si} = 10 nm and 15 nm, V_{ds} = 0 V, 0.5 V and 1 V, N_0 = 10^{15} cm^{-3} (undoped), φ_g = 5 eV and W_g = 1 µm. The developed model is examined for varying N_d, T_{core}, L_g that ranges from 5×10^{18} cm^{-3} to 2×10^{19} cm^{-3}, 0 to T_{si}, and 10 nm to 100 nm, respectively. The developed model results (indicated by solid lines in the subsequent figures) are validated with results derived from Atlas device simulator (marked by symbols) [25]. Simulation details are the same as previously discussed in subsection 2.4.1 of chapter 2.

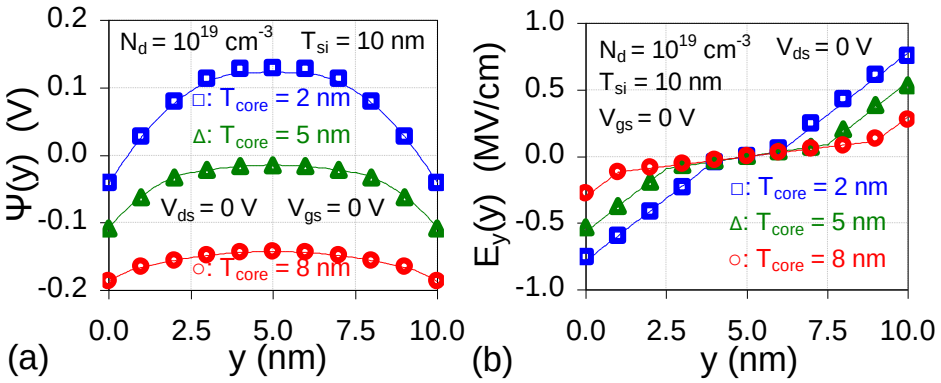

Fig. 4.2 Dependence of **(a)** potential and **(b)** vertical component of the electric field (E_y) along the y-direction at $x = L_g/2$ on varying T_{core} for L_g = 10 nm. Symbols mark TCAD simulation data and lines denote model results.

4.4.1 Preliminary Model Validation

Fig. 4.2(a) validates the choice of region-wise parabolic potential approximation in shell and core regions in (4.4)-(4.6). Also, Fig. 4.2(a)-(b) ascertains that the potential and E_y as derived from the developed model are continuous at both top and bottom shell-core interfaces (in (4.10)), and well satisfy the TCAD simulations for various T_{core} and N_d = 10^{19} cm^{-3}. Furthermore, the modeled electron concentration matches the simulated n_e for different T_{core} at V_{ds} = 0, as shown in Fig. 4.3(a)-(d). A wider T_{core} enables easier depletion of electrons from the channel, as observed by ~5 orders decrease in n_e at $y = T_{si}/2$ from T_{core} = 2 nm to T_{core} = 8 nm in Fig.

4.3(a)-(b). Another observation in Fig. 4.3(a) is the remarkable increase (~3 orders than N_0) in n_e values at the neutral S/D ends (far away from the gated portion) due to electrons diffusion from the shell ($N_d = 10^{19}$ cm^{-3}) to core ($N_0 = 10^{15}$ cm^{-3}) regions.

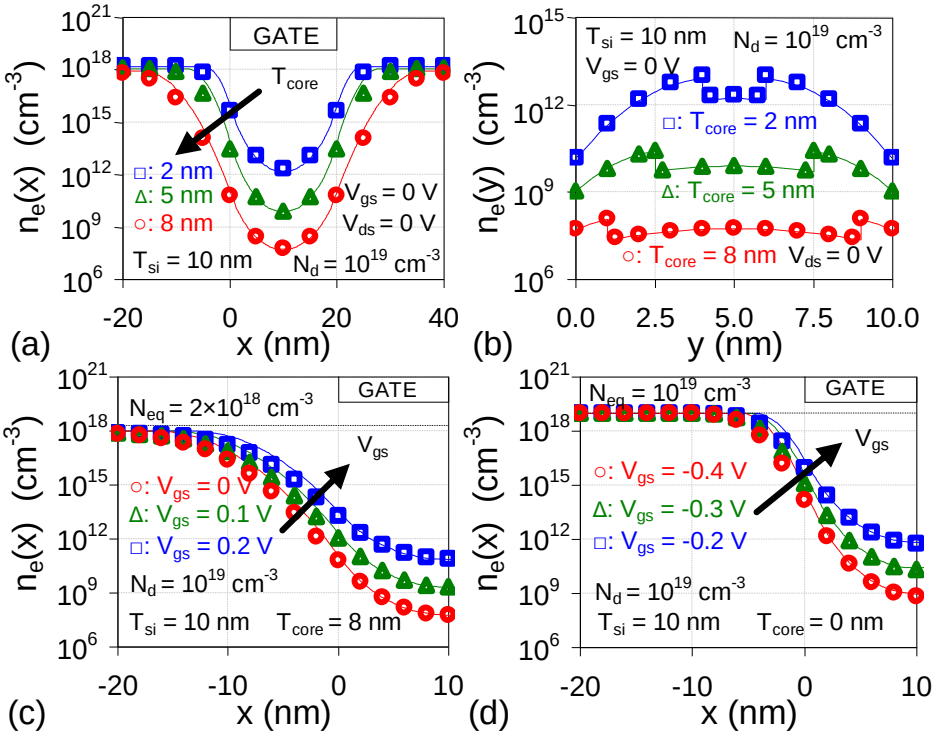

Fig. 4.3 Plot of electron concentration **(a)** along the x-direction at $y = T_{si}/2$ and **(b)** along the y-direction at $x = L_g/2$ for various T_{core} and L_g = 20 nm. Enlarged view of part **(a)** illustrating n_e with varying V_{gs} for **(c)** CS (T_{core} = 8 nm) and **(d)** conventional (T_{core} = 0 nm) DG JL topologies in the subthreshold region. Symbols depict simulation data and lines denote model results.

Next, Fig. 4.3(c) demonstrates the validity of N_{eq} used in (4.24) to approximate the central potential in regions II and III of CS DG JL topology. Also, Fig. 4.3(d) is added to illustrate that at T_{core} = 0 nm, N_{eq} equals $N_d = 10^{19}$ cm^{-3}, and the expressions in regions II and III in (4.30b)-(4.30c) transforms to those reported in the literature for uniformly N_d-doped conventional DG JL device [97], [116], [146], [157]. The relation (4.24) is analogous to 1D Poisson's equation under depletion approximation used for evaluating S/D depletion region extensions in conventional DG JL MOSFET. Hence, the subthreshold characteristics of

the CS DG JL device can be determined by device parameter-dependent N_{eq} instead of N_0 and electron concentration at the central core region.

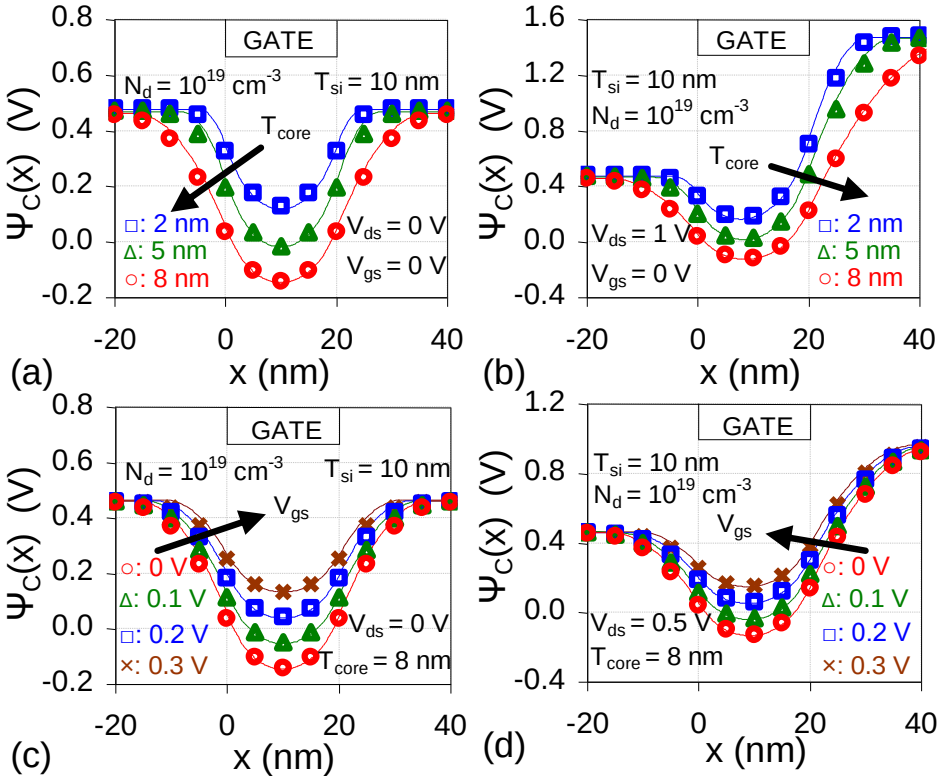

Fig. 4.4 Dependence of central potential along the *x*-direction at $y = T_{si}/2$ and L_g = 20 nm on **(a), (b)** various T_{core} for $V_{gs} = V_{ds}$ = 0 V, and **(c), (d)** different V_{gs} for T_{core} = 8 nm. In figure part **(b)** V_{ds} = 1 V and **(d)** V_{ds} = 0.5 V. Symbols mark simulation data and lines denote model results.

Fig. 4.4(a)-(d) shows the variations of central potential with T_{core}, V_{gs} and V_{ds}, and developed model results agree well with the TCAD simulations. With increasing T_{core} (or equivalently decreasing d), the number of dopants that screen the gate field penetration into the channel region decreases. As a result, longer L_{Se} and L_{De}, and a lower channel potential are achieved at a wider T_{core}, as shown in Fig. 4.4(a)-(b). The rise in V_{gs} from 0 V (subthreshold) towards positive values (threshold) in Fig. 4.4(c)-(d) for T_{core} = 8 nm causes the channel potential to increase, and hence, contribute to turning on of the device. On the other hand, with rising V_{ds}, the channel-drain junction is more reverse-biased and L_{De} becomes greater than L_{Se} (in Fig. 4.4(b),(d)). While at V_{ds} = 0V, identical values of L_{De} and L_{Se} are achieved, as shown in Fig. 4.4(a),(c).

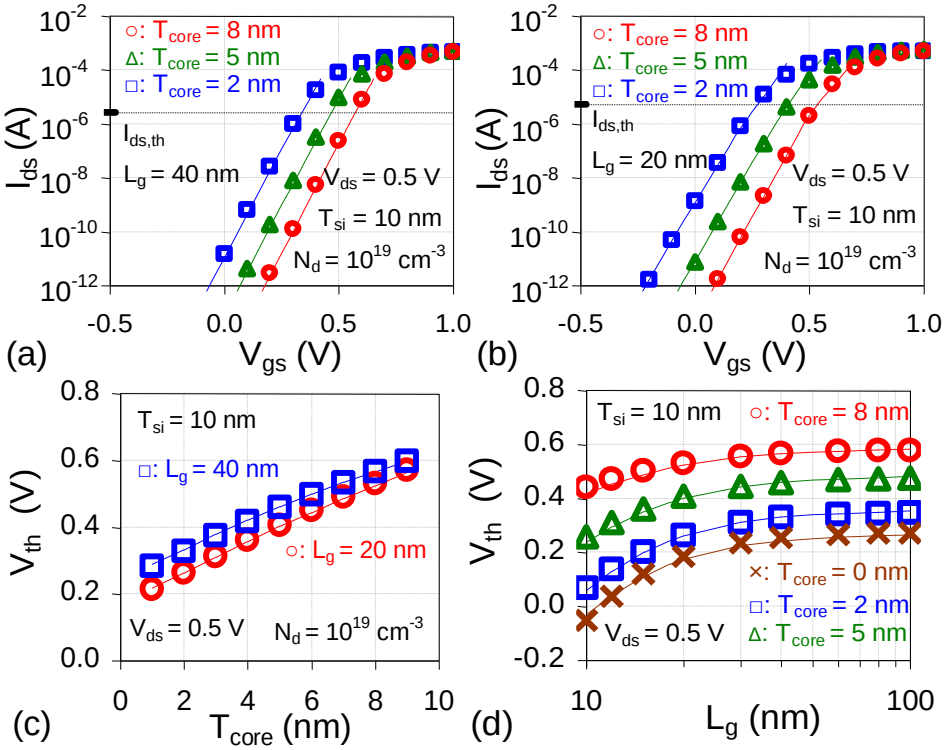

Fig. 4.5 Transfer characteristics at different T_{core} for **(a)** L_g = 40 nm and **(b)** L_g = 20 nm. Plot of V_{th} versus **(c)** T_{core} and **(d)** L_g. Symbols mark simulation data and lines denote model results.

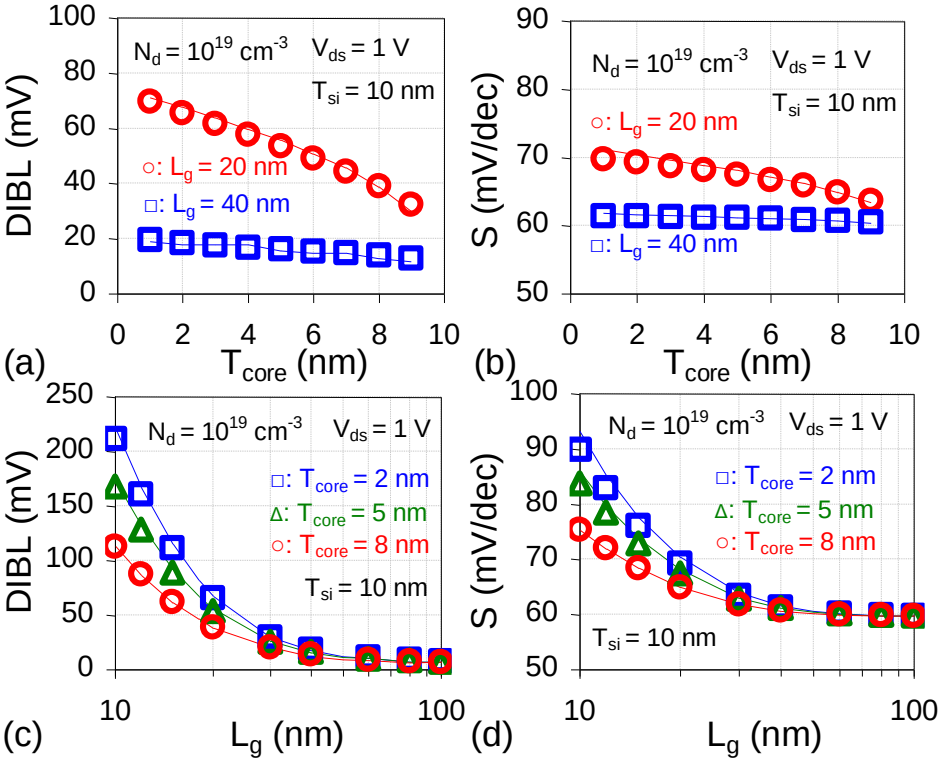

Fig. 4.6 Effect of T_{core} and L_g variations on **(a)**, **(c)** DIBL and **(b)**, **(d)** *S*. Symbols mark simulation data and lines denote model results.

4.4.2 Short Channel Effects

This section examines the effect of T_{core}, L_g and N_d on V_{th} and SCEs that are extracted from the subthreshold I_{ds}-V_{gs} curve of the CS DG JL device, similar to one shown in Fig. 4.5(a)-(b) for different L_g and T_{core}. As presented in Fig. 4.5(c), V_{th} increases with widening T_{core} values owing to the easier depletion of electrons from the channel in the subthreshold regime. Furthermore, Fig. 4.5(d) depicts that V_{th} roll-off with L_g suppresses by widening T_{core}. Also, DIBL (Fig. 4.6(a), (c)) and S (Fig. 4.6(b), (d)) improve with increasing T_{core} values, indicating superior gate controllability over the channel at a wider T_{core}. The improvement in SCEs for wider T_{core} is remarkable at shorter L_g (in Fig. 4.6(a)-(d)).

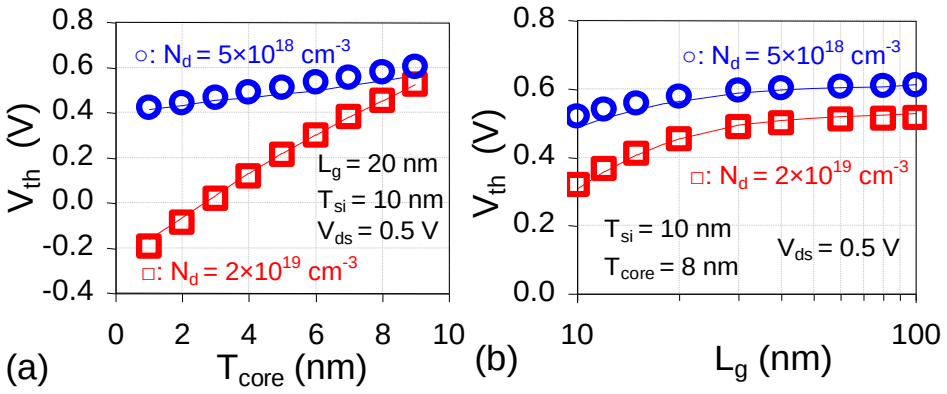

Fig. 4.7 Variation of V_{th} with varying **(a)** T_{core} and **(b)** L_g for N_d = 5×10^{18} cm^{-3} and 2×10^{19} cm^{-3}. Symbols mark simulation data and lines show model results.

Another key parameter that decides V_{th} and SCEs in CS DG JL MOSFETs is shell doping, as illustrated in Fig. 4.7(a)-(b) and 4.8(a)-(d). As observed in Fig. 4.5(c)-(d) and 4.7(a)-(b) that appropriate (positive) values of V_{th} can also be achieved by decreasing N_d values for fixed T_{core}, even at shorter L_g. With lowering N_d, the number of shell dopants that screen the gate field penetration into the channel reduces, and hence, the gate controllability over the channel enhances. The rate of change of V_{th} with respect to T_{core} is higher for N_d = 2×10^{19} cm^{-3} than N_d = 5×10^{18} cm^{-3}, indicating a relatively high V_{th} sensitivity in CS DG JL device having heavily-doped shell than its moderately-doped counterpart. For fixed T_{core} and L_g, N_d = 5×10^{18} cm^{-3} offers suppressed V_{th} roll-off (Fig. 4.7(b)), DIBL

(Fig. 4.8(a),(c)) and S (Fig. 4.8(b),(d)) than $N_d = 2\times10^{19}$ cm^{-3}, and hence, alleviated SCEs.

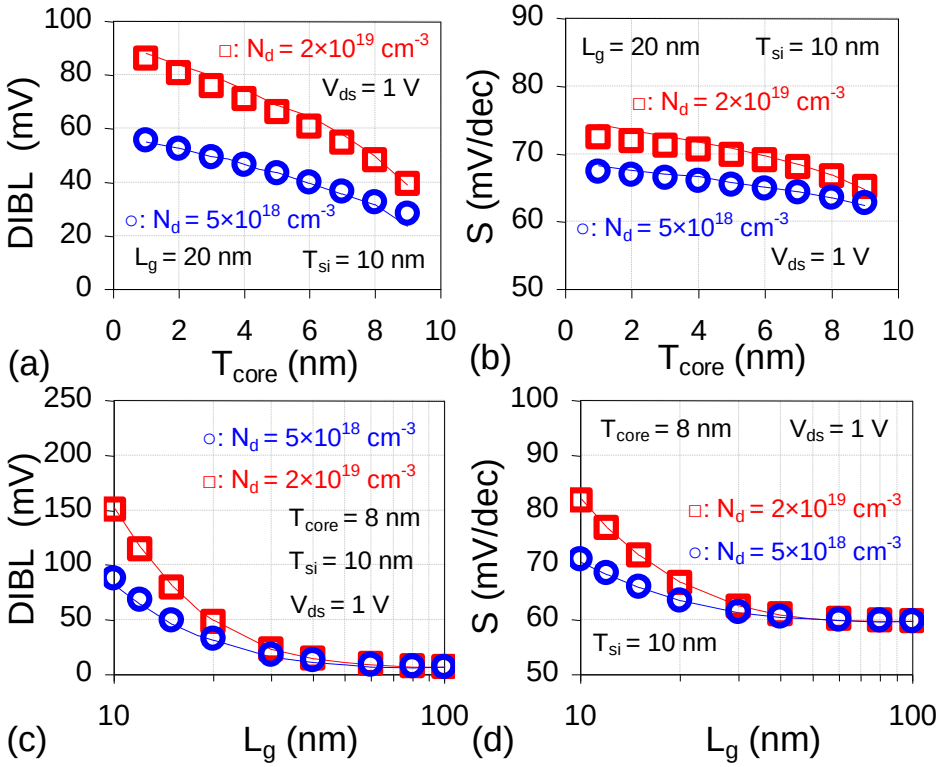

Fig. 4.8 Effect of T_{core} and L_g variations on **(a)**, **(c)** DIBL and **(b)**, **(d)** S for $N_d = 5\times10^{18}$ cm^{-3} and 2×10^{19} cm^{-3}. Symbols mark simulation data and lines denote model results.

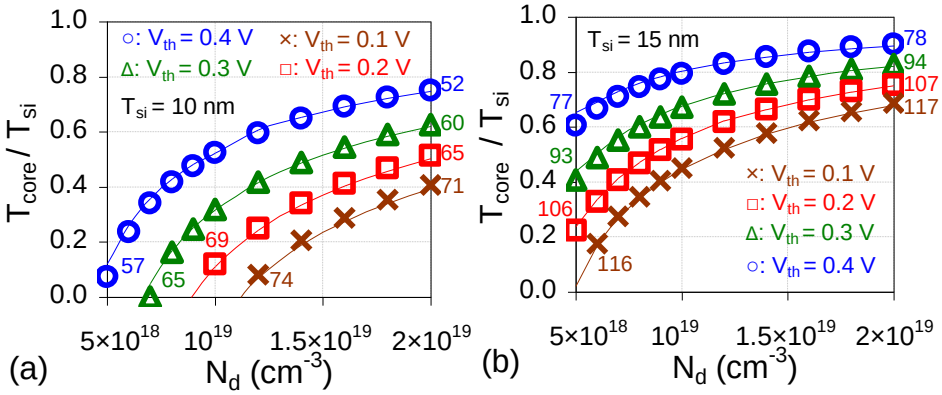

Fig. 4.9 Plot of T_{core}/T_{si} versus N_d for fixed values of V_{th} at V_{ds} = 1 V, L_g = 20 nm, and **(a)** T_{si} = 10 nm and **(b)** T_{si} = 15 nm. Symbols mark simulation data and lines denote model results.

4.4.3 Design Guidelines

At last, Fig. 4.9(a)-(b) plots the relation between T_{core}/T_{si} and N_d to

obtain fixed values for V_{th} with respective DIBL range written against each curve. It can be observed that for a given V_{th}, the marginal difference in DIBL values exists at two extremes of N_d ranges, i.e. between 5×10^{18} cm^{-3} and 2×10^{19} cm^{-3}. The degradation in DIBL at higher N_d is compensated by wider T_{core}, whereas moderate N_d recovers poor DIBL performance at narrow T_{core} values. Results show that both high N_d – wide T_{core} and moderate N_d – narrow T_{core} pairs can result in identical values of V_{th} and similar values of DIBL, and hence, offers a broader design window for device optimization.

4.5 CONCLUSION

The chapter has presented a semi-analytical subthreshold model to reasonably capture the channel potential and SCEs in CS DG JL MOSFETs for varying L_g, T_{core}, N_d and biases. The model is based on the solutions of 2D Poisson's equations in gated as well as S/D extension portions using appropriate region-wise approximations, and boundary and continuity conditions. The developed model presents core thickness and shell doping as the two key parameters to optimize the short channel performance of CS DG JL MOSFETs. Results suggest that the moderate N_d - narrow T_{core} pair can be preferred over high N_d - wide T_{core} for similar SCEs but reduced V_{th} sensitivity. Such design guidelines can be useful to optimize DG JL device with SDP to simultaneously ensure fabrication feasibility as well as efficient LP/ULP performance.

Chapter 5

Conclusion and Future Work

5.1 CONCLUSION

JL transistors can be promising alternatives to replace conventional MOSFETs for the next generation of technology innovation [12]-[15]. These transistors eliminate the need for ultra-sharp *pn* junction formation. Their key attributes include relaxed fabrication processes requirements, enhanced short channel immunity and extended downscaling limits than conventional transistors [30], [31]. Since LP/ULP logic technology demands transistors that exhibit superior control over subthreshold characteristics and improved SCEs [17], JL MOSFETs show capabilities for LP/ULP technologies rather than for HP logic applications [49], [50].

Owing to the identical doping type and concentration throughout the semiconductor film, an elongated L_{eff} than L_g in the off-state for JL device reflects on the superior short channel performance of the device in comparison to the conventional MOSFETs at identical L_g [34], [123]. However, the value of L_{eff} in the subthreshold regime depends on lateral S/D depletion extensions, which varies with different JL device topologies. The thesis has developed semi-analytical models to predict SCEs in self-aligned DG JL FETs considering these lateral SDEs. The architectures that have been analyzed are: **(i)** simultaneously-driven symmetric DG structure with identical S/D underlap lengths, **(ii)** independent gate-operated asymmetric DG structure with non-identical S/D underlap lengths, and **(iii)** (symmetric) DG JL transistor with SDP. The developed 2D models have adequately captured the dependence of device parameters and biases on SCEs in DG JL MOSFETs. The main contributions of the research work presented in this thesis are summarized as follows:

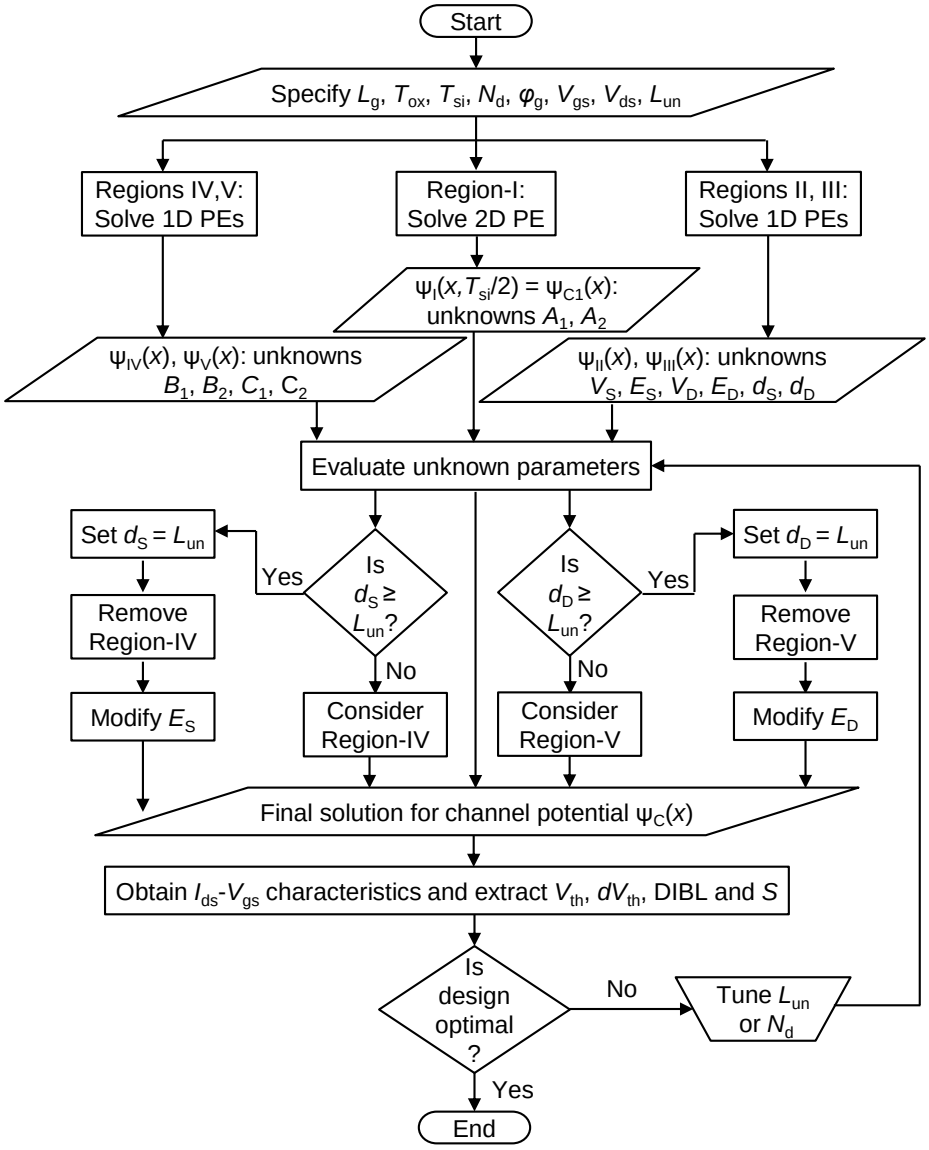

Fig. 5.1 Flowchart summarizing the modeling approach followed for the design optimization of DG JL under the symmetric mode operation. The abbreviation PE(s) denotes Poisson's equation(s).

1. Modeling the Dependence of SCEs on G-S/D Underlap Regions in JL Transistor

The developed five-region model for channel potential in the subthreshold regime has facilitated the estimation of G-S/D underlap-dependent SCEs in *n*-channel DG JL MOSFET under the symmetric mode operation (i.e., simultaneously driven front and back gates with identical values of gate oxide thicknesses and workfunctions, and G-S/D underlap lengths). Fig. 5.1 summarizes the entire modeling flow adopted for the

optimization of symmetric DG JL MOSFET with controlled SCEs. The developed model can be applied for any underlap length, and hence, has a generic formulation. The five regions can be transformed into four or three regions depending upon the extent of depletion into the gate underlap. Approximate analytical solutions of subthreshold drain current can be utilized to obtain the device transfer characteristics, thereby to extract V_{th}, S and SCEs related parameters. The developed model results reasonably agree with the simulation data. Analyses have shown that L_{un} and N_d are two key parameters that can be tuned to control SCEs in these devices. Lowering N_d allows easy penetration of the gate electric field, leading to longer d_S and d_D, and better electrostatic control of gate over the channel region. Also, L_{un} limits the extent of depletion region beyond the gate edges as the gate field cannot penetrate the heavily doped S/D regions. With increasing L_{un}, SCEs improve until the maximum depletion extension lengths allowed by the device parameters are achieved. Thus, the choice of sufficiently long L_{un} and moderate N_d can prove beneficial to suppress SCEs in these devices at shorter gate lengths.

2. A Generic Model to Optimize Short Channel Self-Aligned Asymmetric DG JL Transistor with Gate-Underlap

The thesis has presented a generic model formulation to predict SCEs in a self-aligned *n*-channel DG JL transistor with gate underlap under the asymmetric mode operation, as depicted in Fig. 5.2. Independent gate operation (i.e., asymmetries in gate biases) along with structural asymmetries in gate workfunctions, gate oxide thicknesses and G-S/D underlap lengths have been incorporated during the model development. The locations of subthreshold conduction, channel potential, drain current and SCEs indicating parameters have been evaluated for both bias and structural asymmetries in the subthreshold regime. The developed model results satisfy well with the numerical simulations. Results have shown that tuning V_{bg} can be advantageous in optimizing V_{th}, S and I_{off} in independent gate operated DG JL transistor. Moreover, N_d and L_{un} can offer additional design spaces to tune the performance of these devices. Results suggest that the choice of appropriate V_{bg} together with moderate

N_d and sufficiently longer L_{un} can be optimum for asymmetric DG JL device (specific to LP subthreshold logic technology).

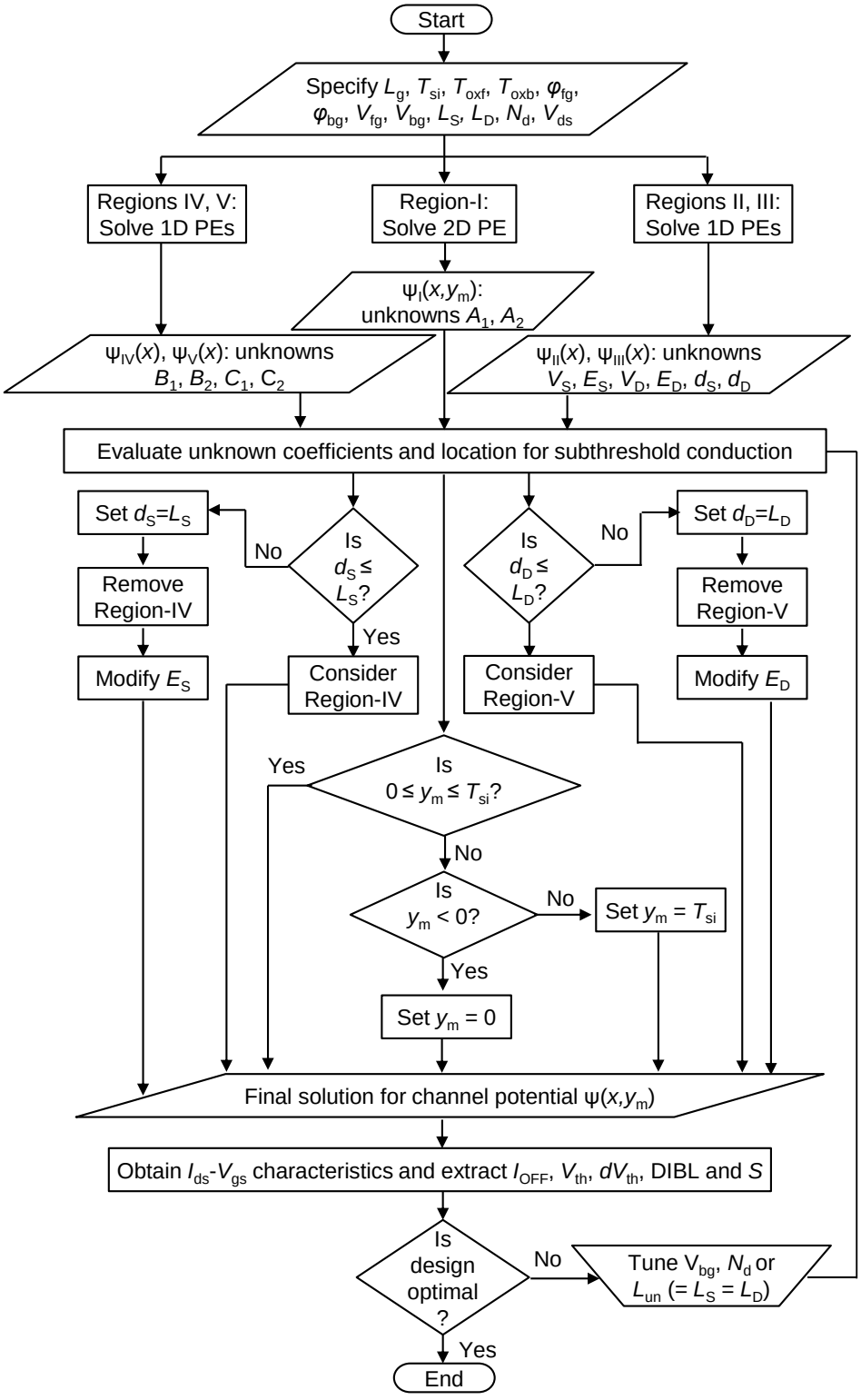

Fig. 5.2 Flowchart depicting generic model formulation for an optimally designed asymmetric DG JL MOSFET for LP subthreshold logic application. PE(s) indicates Poisson's equation(s).

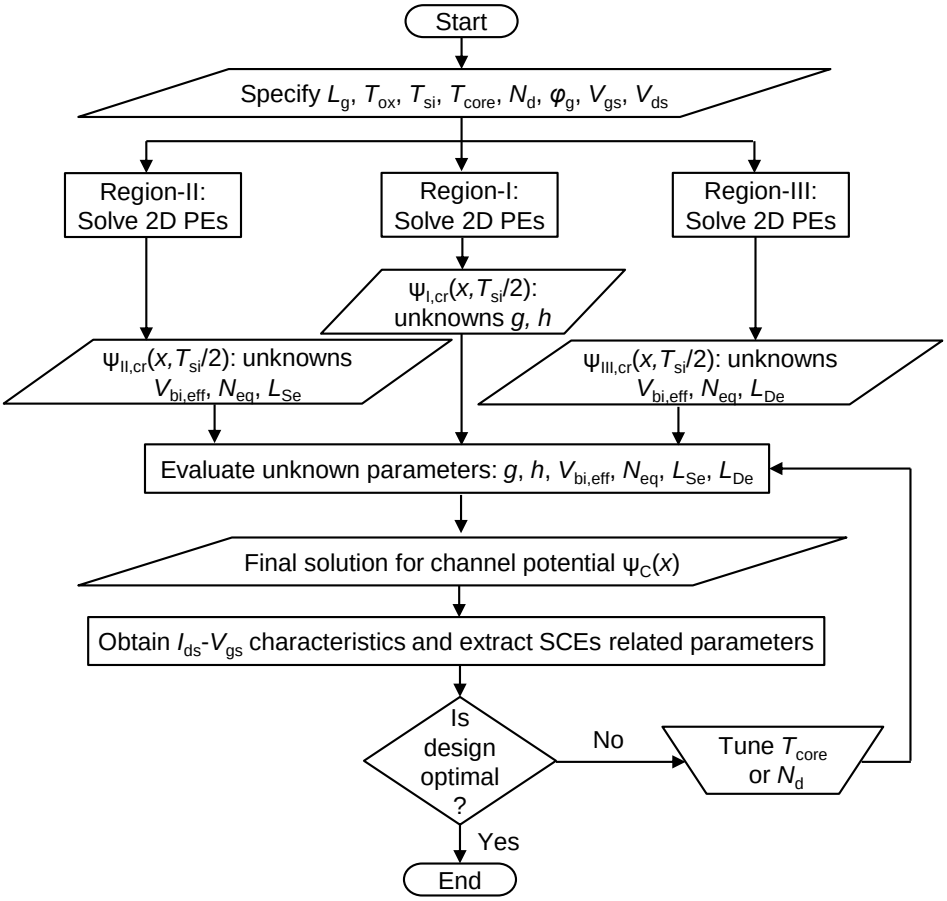

Fig. 5.3 Flowchart showing the modeling scheme followed to optimize CS DG JL MOSFET with suppressed SCEs. PEs represents Poisson's equations.

3. Modeling-based Optimization of SCEs in Core-Shell JL Transistor

The semi-analytical modeling approach has facilitated the prediction and suppression of SCEs in *n*-channel CS DG JL MOSFETs through the solution of 2D Poisson's equations with appropriate boundary and continuity conditions across the three regions, as shown in Fig. 5.3. The modeled channel potential governing subthreshold conduction, subthreshold drain current and SCEs related parameters are in good agreement with TCAD simulations. The developed model has shown that shell doping and core thickness (otherwise shell depth) are two crucial parameters that needs to be tuned for optimal device performance. Analysis has shown that SCEs can be alleviated by a thicker T_{core} as well as moderate N_d. The widening of T_{core} or lowering of N_d leads to a lower minimum potential and longer L_{Se} and L_{De}, due to reduced screening of

gate electric field by relatively less number of dopants. For low power applications, choice of a narrow T_{core} - moderate N_d can be preferred over wide T_{core} - high N_d to achieve almost similar short channel performance but at reduced sensitivity of V_{th} and SCEs on T_{core}.

The research work presented in the thesis has provided comprehensive and dedicated approaches to estimate and suppress SCEs in various DG JL MOSFET architectures for LP/ULP applications. The proposed guidelines can be beneficial for the design optimization of nanoscale JL devices for ULP/LP subthreshold logic technology applications while enabling downscaling.

5.2 SCOPE FOR FUTURE WORK

This thesis has presented semi-analytical modeling-based design guidelines to optimize nanoscale DG JL transistors with suppressed SCEs, which can be suitable for subthreshold logic applications. The thesis has aimed to adequately capture the essential device physics of the analyzed DG JL topologies in the subthreshold regime. However, there are few uncovered attributes in the present thesis that needs to be incorporated in the model development, and hence, are stated in the scope for future work.

5.2.1 Incorporation of QCE in Core-Shell JL MOSFETs

Literature [89], [145] has presented that the shift in threshold voltage due to 2D QCEs is significant for T_{si} roughly less than 7 nm in both JL as well as IM transistors. Unlike conventional IM transistor, since the majority charge carriers are mainly confined at the centre of the film in JL transistors, a lower threshold voltage shift between classical and quantum regimes is observed in these devices [89]. Also, for thick T_{si} and fixed classical V_{th}, QCE reduces with decreasing N_d of JL device [89]. Therefore, 2D QCE arising due to semiconductor film thickness and channel doping are expected to have minimal effect on V_{th} and SCEs in JL transistors. In the present thesis work, as a first-order approximation, 2D QCE is not considered during the model development. The developed models are expected to be valid for $T_{si} \geq 7$ nm.

However, QCE cannot be ignored while estimating V_{th} and SCEs for ultra-thin JL transistors. Few analytical models [89], [122], [158] have been proposed in the literature that includes QCE in the ultra-thin conventional heavily doped JL transistors. The incorporation of QCE in core-shell DG JL transistors can be interesting as well as challenging. For more accurate estimation of V_{th} and SCEs in CS JL transistor, the understanding and incorporation of QCE in the analytical model are essential. The quantum correction factor can be added along with classical threshold voltage to accurately predict the device behavior under significant influence of 2D QCE.

5.2.2 Modeling SCEs in Core-Shell JL Transistors including Non-abrupt Doping Gradient

In the present thesis, the doping profile transition between core and shell regions are assumed to be abrupt (i.e., the slope of 0 nm/dec) for simplicity. However, in practical CS JL devices, doping steepness of about 0.8 nm/dec is achieved due to various thermal processes involved during the fabrication of such devices [124], [125]. Variations in V_{th}, S, and I_{OFF} have been observed with non-steep doping gradients [127]. Therefore, to capture the physical behavior of a more practical CS JL device, it is crucial to incorporate the effect of doping gradient in V_{th} and SCEs related parameters. The developed model can be extended to include the influence of non-abrupt doping gradient through the shift in minimum channel potential and lateral S/D extensions of the CS JL device.

5.2.3 Process-induced Variability Analysis in the Subthreshold Characteristics of JL MOSFETs

For efficient LP/ULP logic performance of a digital IC, the device subthreshold characteristics should not severely change from one transistor to another inside an IC. However, several process-induced variability such as RDFs [159]-[161], gate metal Workfunction Variability (WFV) [162], [163], Contact Resistivity Variability (CRV) [164], [165], fin-width variations [41], etc., can affect the device characteristics across the chip.

Both simulation and model-based studies have demonstrated that the conventional JL transistor suffers from severe process-induced variations than the conventional IM transistor [43], [44], [166]. Consequently, to propose variability immune optimal design for LP/ULP logic applications, it is equally important to consider these process-induced phenomena while modeling the subthreshold characteristics for JL devices with G-S/D underlap and SDP.

APPENDIX-A

A.1 APPROXIMATING NUMERICAL INTEGRALS

The trapezoidal rule is used to compute the integration of any arbitrary function $H(z)$ within the limits of z from a to b [144], as expressed below:

$$\int_a^b H(z)dz = \Delta\left[\frac{H(a)}{2} + H(a+\Delta) + H(a+2\Delta)\ldots H(a+(n-1)\Delta) + \frac{H(b)}{2}\right] \tag{A1}$$

where Δ (= $(b - a)/n$)) determines the spacing between (n + 1) equally spaced samples from a and b (including a and b, where $b > a$).

Considering the curvatures of channel potential along the x- and y-directions in the subthreshold operating regime, a simple trapezoidal rule is sufficient to efficiently evaluate the integrations in (2.34) of chapter 2. In region-I, the first part of the integral along the y-direction in (2.34) is computed using general relation in (A1) and $\Delta = T_{si}/4$, as written below:

$$\int_0^{T_{si}} \exp\{\beta\psi_I(x,y)\}dy \approx \frac{T_{si}}{4}\left[\begin{array}{r}\exp\{\beta\psi_S(x)\} + \exp\{\beta\psi_C(x)\} \\ + 2\exp\left\{\beta\psi_I\left(x, \frac{T_{si}}{2}\right)\right\}\end{array}\right] \tag{A2}$$

In chapter 2, to adequately compute the second part of the integrals along the x-direction in regions I, II and III, Δ is chosen to be $L_g/6$, $d_S/4$, and $d_D/4$, respectively. The approximate solutions of integrals are already mentioned in (2.35). To further enhance the accuracy in computing the integrals, closely spaced samples (i.e., a relatively low value of Δ) along the x- and y-directions can be used.

A.2 EFFECTIVE BUILT-IN VOLTAGE

A.2.1 Determination of Effective Built-in Voltage

Far away from the gate edges (precisely beyond the S/D extension boundaries), the electrostatic potential distribution is solely governed by the thermal diffusion of electrons from the heavily doped shell to the

undoped core, rather remains unaffected by the gate electric fields [138]. Therefore, the potential distribution is independent of *x*-direction, but possesses *y*-direction dependence, as depicted in Fig. A.1. A constant potential equals to the effective built-in voltage appears at the end of the S/D boundaries in the centre of the undoped core, i.e. $\psi_{cr}(-L_{Se}, T_{si}/2) = V_{bi,eff}$ and $\psi_{cr}(L_g+L_{De}, T_{si}/2) = V_{bi,eff}$ (provided $V_{ds} = 0$).

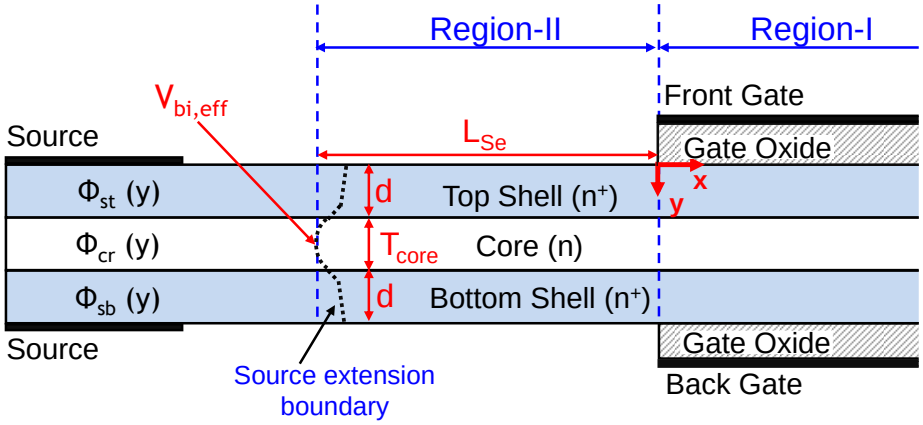

Fig. A.1 Schematic illustration of effective built-in potential at the end of the source extension boundary of a CS DG JL MOSFET. $V_{bi,eff}$ on the drain side is identical to the source side (not shown in Fig. A.1).

In contrast to N_d-dependent built-in voltage for uniformly doped JL devices [97], [116], the built-in potential for a CS JL transistor depends on additional device parameters (N_d, N_0, T_{si} and T_{core}) and differs at various *y* positions (along the Si film thickness). A 1D Poisson's equation in the *y*-direction can be solved to obtain the $V_{bi,eff}$ as:

a) **Top Shell Portion:** $\{0 \le y \le (T_{si} - T_{core})/2\}$

$$\frac{d^2\Phi_{st}(y)}{dy^2} = \frac{-q}{\varepsilon_{si}}\left[N_d - n_{id}\exp\left(\beta\Phi_{st}(y)\right)\right] \qquad \text{(A3)}$$

b) **Core Portion:** $\{(T_{si} - T_{core})/2 \le y \le (T_{si} + T_{core})/2\}$

$$\frac{d^2\Phi_{cr}(y)}{dy^2} = \frac{q}{\varepsilon_{si}}\left[n_{i0}\exp\left(\beta\Phi_{cr}(y)\right)\right] \qquad \text{(A4)}$$

c) **Bottom Shell Portion:** $\{(T_{si} + T_{core})/2 \le y \le T_{si}\}$

$$\frac{d^2\Phi_{sb}(y)}{dy^2} = \frac{-q}{\varepsilon_{si}}\left[N_d - n_{id}\exp\left(\beta\Phi_{sb}(y)\right)\right] \qquad \text{(A5)}$$

On solving (A3) and (A5) using the analytical approach described in

subsection 2.2.3 of chapter 2, approximate solutions for shell potential, $\Phi_{st}(y)$ and $\Phi_{sb}(y)$, are obtained. Also, the integration of (A4) provides the exact solution for core potential, $\Phi_{cr}(y)$. The general solutions obtained are then expressed by:

$$\Phi_{st}(y) = D_1 \exp(y/\lambda_{Dd}) + D_2 \exp(-y/\lambda_{Dd}) + V_{bi} \tag{A6}$$

$$\Phi_{cr}(y) = V_T \ln\left\{E_1 \sec^2\left\{\sqrt{E_1/2\lambda_{D0}{}^2}\,(y - T_{si}/2 - E_2)\right\}\right\} \tag{A7}$$

$$\Phi_{sb}(y) = F_1 \exp((y - T_{si})/\lambda_{Dd}) + F_2 \exp(-(y - T_{si})/\lambda_{Dd}) + V_{bi} \tag{A8}$$

where $\lambda_{Dd} = (\varepsilon_{si}V_T/qN_d)^{1/2}$ and $\lambda_{D0} = (\varepsilon_{si}V_T/qn_{i0})^{1/2}$ denote the extrinsic and intrinsic Debye lengths in shell and core regions, respectively. The values for the unknown coefficients (D_1, D_2, E_1, E_2, F_1 and F_2) are determined using the following boundary conditions:

a) Assuming ohmic contacts between S/D metal electrode and semiconductor, the front and back surface are maintained at a constant potential, V_{bi} (= $V_T \ln(N_d/n_{id})$) [25]

$$\Phi_{st}(y = 0) = \Phi_{st}(y = T_{si}) = V_{bi} \tag{A9}$$

b) Potentials and the vertical component of the electric field is continuous at top/bottom shell-core interfaces,

$$\Phi_{st}(y = (T_{si} - T_{core})/2) = \Phi_{cr}(y = (T_{si} - T_{core})/2) \tag{A10a}$$

$$\Phi_{cr}(y = (T_{si} + T_{core})/2) = \Phi_{sb}(y = (T_{si} + T_{core})/2) \tag{A10b}$$

$$d\Phi_{st}(y)/dy\big|_{y=(T_{si}-T_{core})/2} = d\Phi_{cr}(y)/dy\big|_{y=(T_{si}-T_{core})/2} \tag{A10c}$$

$$d\Phi_{st}(y)/dy\big|_{y=(T_{si}+T_{core})/2} = d\Phi_{sb}(y)/dy_{\,y=(T_{si}+T_{core})/2} \tag{A10d}$$

The simplified solutions for (A6)-(A8) are obtained using (A9)-(A10) as:

$$\Phi_{st}(y) = 2D_1 \sinh(y/\lambda_{Dd}) + V_{bi} \tag{A11}$$

$$\Phi_{cr}(y) = V_T \ln\left\{E_1 \sec^2\left\{\sqrt{E_1/2\lambda_{D0}{}^2}\,(y - T_{si}/2)\right\}\right\} \tag{A12}$$

$$\Phi_{sb}(y) = 2D_1 \sinh((T_{si} - y)/\lambda_{Dd}) + V_{bi} \tag{A13}$$

The coefficients D_1 and E_1 are evaluated by simultaneously solving the transcendental expressions derived using the condition (A10) at $y = d = (T_{si} - T_{core})/2$, as follows:

$$D_1 \sinh(d/\lambda_{Dd}) + V_{bi} = V_T \ln\left\{E_1 \sec^2\left\{\left(\sqrt{E_1/2\lambda_{D0}{}^2}\right)(-T_{core}/2)\right\}\right\} \tag{A14}$$

$$\frac{2D_1}{\lambda_{Dd}}\cosh\left(\frac{d}{\lambda_{Dd}}\right)=\frac{V_T\sqrt{2E_1}}{\lambda_{D0}}\tan\left\{\frac{\sqrt{E_1/2}}{\lambda_{D0}}\left(\frac{-T_{core}}{2}\right)\right\} \qquad \text{(A15)}$$

At last, on evaluating (A12) at $y = T_{si}/2$ yields $V_{bi,eff}$ at the centre of the film in the undoped region is obtained by, as written below:

$$V_{bi,eff}=\Phi_{cr}\left(T_{si}/2\right)=V_T\ln\left(E_1\right) \qquad \text{(A16)}$$

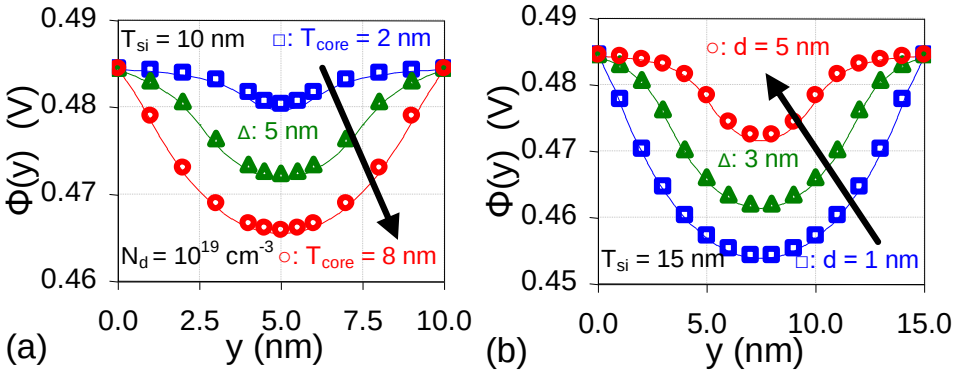

Fig. A.2 Dependence of electrostatic potential underneath S/D electrode **(a)** on different T_{core} values for T_{si} = 10 nm, and **(b)** on varying d values for T_{si} = 15 nm with $N_d = 10^{19}$ cm^{-3}. It is emphasized that $d = (T_{si} - T_{core})/2$. Symbols show simulation data and solid lines represent model results.

A.2.2 Model Validation for Effective Built-in Voltage

Fig. A.2(a)-(b) ensures the validity of the approximate solution used in (A6) and (A8) as well as the various conditions mentioned in (A9) and (A10) for estimating $V_{bi,eff}$. The model results are indicated by solid lines, whereas the simulation data are denoted by symbols. The model expressions are in good agreement to the simulated data for T_{si} = 10 nm (Fig. A.2(a)) and T_{si} = 15 nm (Fig. A.2(b)). The potential underneath the electrode region ($\Phi(y)$) decreases with increasing T_{core}, or equivalently decreasing d values. With decreasing shell depth (or widening core thickness), the number of electrons available for thermal diffusion from n^+ shell to the undoped core decreases. As a result, a lesser number of electrons (i.e. lower potential) are achieved underneath the S/D electrode under the equilibrium state.

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