# Design and Fabrication of MgZnO/CdZnO Heterostructures for HFET Application

Ph.D. Thesis

By Md ARIF KHAN



# DISCIPLINE OF ELECTRICAL ENGINEERING INDIAN INSTITUTE OF TECHNOLOGY INDORE Oct. 2019

# Design and Fabrication of MgZnO/CdZnO Heterostructures for HFET Application

## A THESIS

Submitted in partial fulfillment of the requirements for the award of the degree of DOCTOR OF PHILOSOPHY

> *by* **Md ARIF KHAN**



# DISCIPLINE OF ELECTRICAL ENGINEERING INDIAN INSTITUTE OF TECHNOLOGY INDORE Oct. 2019



# INDIAN INSTITUTE OF TECHNOLOGY INDORE

## **CANDIDATE'S DECLARATION**

I hereby certify that the work which is being presented in the thesis entitled **Design and Fabrication of MgZnO/CdZnO Heterostructures for HFET Application**, in the partial fulfillment of the requirements for the award of the degree of **Doctor of Philosophy** and submitted in the **Discipline of Electrical Engineering, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from June, 2015 to October, 2019 under the supervisions of Dr. **Shaibal Mukherjee**, Associate Professor, Electrical Engineering, IIT Indore, **Prof. Abhinav Kranti**, Professor, Electrical Engineering, IIT Indore, and **Dr. Ajay Agarwal**, Sr. Principal Scientist, Coordinator, Smart Sensors Area, and Head of Nano Biosensors Group at CSIR-Central Electronics Engineering Research Institute, Pilani.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

28/5/2020

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This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

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Signature of Head of Discipline Date:

### ACKNOWLEDGEMENTS

There are many people who have made important contributions to this dissertation. It would be impossible to list everyone who had contributed to this work, or to completely enlist the extent of the contributions for those who are mentioned.

First of all, I would like to express my deep sense of gratitude to my supervisor **Dr. Shaibal Mukherjee** and co-supervisors **Prof. Abhinav Kranti** and **Dr. Ajay Agarwal** for their outstanding mentorship and support that they have provided over the past four years. They were always accessible and have been a constant source of advice to keep my project headed toward its main goal. Dr. Mukherjee played an influential role in developing my research skills and personality. I benefited immensely from his vast technical expertise and insight, he could not even realize how much I have learned from him.

I am extremely grateful to my doctoral committee members **Dr. Swadesh Kumar Sahoo** and **Dr. Prabhat Kumar Upadhyay** for giving me valuable advice on my research and kindly going through my dissertation. My sincere appreciation to **Dr. Mukul Gupta** of UGC-DAE consortium for scientific research, in providing magnetron sputtering facilities for metal deposition. Furthermore, I would like to acknowledge the support from **Mr. Tomohiko Yamakami** of the Technical Division, Faculty of Engineering, Shinshu University for TEM imaging. I would also like to thank the in-charge cleanroom facilities at CSIR-CEERI, Pilani for providing the facilities and **Mr. Supriyo Das**, Technical Officer, for the assistance in Lithography.

I would like to thank **Dr. Pradeep Mathur**, Director, IIT Indore for providing the essential experimental facilities and financial support in attending international conferences. I want to acknowledge the support provided by sophisticated instrumentation center (SIC) at IIT Indore, for performing SEM, EDX and XRD measurements. I would like to thank my fellow group members including **Dr. Vishnu Awasthi, Dr. Pankaj Sharma, Dr. Rohit Singh, Dr. Aaryashree, Dr. Vivek Garg, Dr. Brajendra Singh Sengar, Dr.**  Amitesh Kumar, Ritesh Bhardwaj, Mangal Das, Biswajit Mandal, Gaurav Siddharth, Pawan Kumar, Sanjay Kumar, Ruchi Singh, Chandrabhan Patel, Mayank Dubey, Kumari Jyoti and others for their valuable support and co-operation during this research work.

Last, but far from least, I must thank my parents, my wife, and my sister who have supported me in all of my academic accomplishments. I owe a lot to them.

Md Arif Khan

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Dedicated to my Papaji, Mummyji, my wife Rumman, and my sister Ruby

## LIST OF PUBLICATIONS

#### A: Publications from PhD thesis work

#### A1. In refereed journals

- Md Arif Khan, Pawan Kumar, Mangal Das, Myo Than Htay, Ajay Agarwal, and Shaibal Mukherjee, "Drain Current Optimization in DIBS-grown MgZnO/CdZnO HFET", IEEE Transactions on Electron Devices, Accepted, April 2020. Impact Factor (2.704).
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#### A4. Patents

 A method of fabricating high two dimensional electron gas density yielding zinc oxide heterostructures
 Inventors: Shaibal Mukherjee, Abhinav Kranti, Md Arif Khan and Rohit Singh

Patent No. 201721010866, March 27, 2017 (Status: Published)

#### **B:** Other publications during PhD

#### **B1.** In refereed journals

- Pawan Kumar, Md Arif Khan, Gaurav Siddharth, Sanjay Kumar, Ruchi Singh, and Shaibal Mukherjee, "*Electron scattering analysis in 2DEG in* sputtering-grown MgZnO/ZnO heterostructure", Journal of Physics D: Applied Physics, vol. 53, no. 12, p. 125108, December 2019. Impact Factor (2.829).
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- 6. Rohit Singh, Pankaj Sharma, **Md Arif Khan**, Vivek Garg, Vishnu Awasthi, Abhinav Kranti, and Shaibal Mukherjee, "*Investigation of barrier*

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#### **B4.** Patent

1. *A method of fabricating high two dimensional electron gas density yielding zinc oxide heterostructures* 

Inventors: Shaibal Mukherjee, Abhinav Kranti, Md Arif Khan and Rohit Singh

Patent No. 201721010866, March 27, 2017 (Status: Published)

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# ACRONYMS

2DEG	Two Dimensional Electron Gas
2DHG	Two Dimensional Hole Gas
2DES	Two Dimensional Energy States
C-V	Capacitance-Voltage
CdO	Cadmium Oxide
DIBS	Dual Ion Beam Sputtering
DPC	Deposition Chamber
EDX	Energy Dispersive X-Ray
eV	Electron Volt
FESEM	Field Emission Scanning Electron Microscopy
FWHM	Full Width at Half Maximum
GaN	Gallium Nitride
HFET	Heterojunction Field Effect Transistor
HRTEM	High Resolution Transmission Electron Microscopy
I-V	Current-Voltage
MgO	Magnesium Oxide
MZO	Magnesium Zinc Oxide/Zinc Oxide Heterostructure
МСО	Magnesium Zinc Oxide/Cadmium Zinc Oxide
	Heterostructures
SBH	Schottky Barrier Height
XRD	X-Ray Diffraction
ZnO	Zinc Oxide

# NOMENCLATURE

а, с	Lattice constant	
$\mathcal{E}_{0}$	Dielectric constant	
$E_g$	Energy gap	
λ	Wavelength	
$\mu_n$	Electron mobility	
$\mu_p$	Hole mobility	
ρ <sub>c</sub>	Specific resistivity	
$V_H$	Hall Voltage	
$P_{\mathrm{SP}}$	Spontaneous polarization	
$P_{\mathrm{PZ}}$	Piezoelectric polarization	
V <sub>OFF</sub>	Threshold voltage	
q	Elementary charge	
$R_s$	Sheet resistance	

## ABSTRACT

# Design and Fabrication of MgZnO/CdZnO Heterostructure for HFET Application

by

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This work explores dual ion beam sputtering (DIBS)-grown heterostructure of Magnesium Zinc Oxide and Cadmium Zinc Oxide (MgZnO/CdZnO) for the possibility of achieving high two-dimensional electron gas (2DEG) density  $(n_s)$  and eventually high values of drain current  $(I_d)$  in order to develop a low-cost large-area-electronics compatible heterostructure field effect transistor (HFET). The heterostructure MgZnO/CdZnO proposed and exploited in this work is a functional solution to circumvent the limitations presented by the heterostructures of MgZnO/ZnO, Beryllium Zinc Oxide and Zinc Oxide (BeZnO/ZnO), and BeMgZnO/ZnO towards achieving high values of  $n_{\rm s}$ . The long-pending challenge with popular Mg<sub>x</sub>Zn<sub>1-x</sub>O/ZnO heterostructure system is the occurrence of phase segregation at high Mg content (x > 0.35) in barrier layer, which limits this heterostructure from achieving high values of  $n_{\rm s}$ . To circumvent this limitation,  $Be_yMg_xZn_{1-x-y}O$  as the barrier layer was proposed in the literature that yielded  $n_s$  comparable to that achieved in the case of Mg<sub>0.6</sub>Zn<sub>0.4</sub>O/ZnO heterostructure by utilizing y = 0.2 and x = 0.26. While, BeMgZnO enhances  $n_s$  in ZnO-based heterostructures for lower Mg content, Be2+ ions leave the substitutional lattice sites when annealed at 400 °C and above. The ohmic contact formation for HFET demands metal contacts at the source and drain regions to be annealed at  $\geq$  800 °C, which

imposes a limitation for utilizing BeMgZnO or BeZnO in the barrier layer. Alloying Cadmium Oxide (CdO) in the buffer ZnO layer reduces the spontaneous polarization of the buffer layer and increase conduction band offset at the barrier-buffer interface. Both these phenomena add up to a possibility of significant enhancement in  $n_s$  in MgZnO/CdZnO heterostructure over MgZnO/ZnO heterostructure at lower Mg content in the barrier layer.

In addition, reports of sputtered ZnO heterostructures yielding 2DEG are available in the literature, while Gallium Nitride (GaN) heterostructures are generally fabricated using costly epitaxial growth mechanisms such as molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD). It can be pointed out that MBE is incompatible with large-area fabrication of electronic devices and systems and MOCVD needs extreme control of multiple growth parameters alongside the precise selection of precursors. Sputtering process, on the other hand, is a userfriendly, cost-effective, and large-area compatible growth technique. Amongst various sputtering techniques, DIBS is notable for producing high-quality thin films with reasonably superior compositional stoichiometry and uniformity as well as better film adhesion over a larger substrate surface area. DIBS-grown MgZnO/ZnO heterostructures have been reported to induce 2DEG with conductance, a product of 2DEG density and carrier mobility, comparable to that in GaN-based heterostructure and higher than that in Gallium Arsenide (GaAs)-based heterostructures.

Therefore, this work explores the possibility of achieving high  $n_s$  and drain current ( $I_d$ ) characteristics for low-cost large-area-electronics compatible DIBS-grown MgZnO/CdZnO heterostructure for HFET application.

To achieve this objective, first a physics-based analytical model is developed to estimate the enhancement in  $n_s$  MgZnO/CdZnO heterostructure can provide over MgZnO/ZnO heterostructure at similar barrier layer thickness and Mg content in barrier layer. Utilizing the developed analytical model, it was demonstrated that up to ~25× higher  $n_s$  values can be achieved in MgZnO/CdZnO as compared to that in MgZnO/ZnO heterostructure at lower Mg composition of 0.10 in barrier layer for same barrier layer thickness. It was shown that a lower spontaneous polarization in buffer layer due to more electronegative Cd and higher lattice constant of CdZnO which introduces tensile piezoelectric strain in the barrier layer, favorably add up, and increase polarization difference at barrier-buffer interface which eventually enhances  $n_{\rm s}$ . This analytical model demonstrated new opportunities to effectively utilize buffer layer properties to significantly improve  $n_{\rm s}$  (~4 × 10<sup>13</sup> cm<sup>-2</sup>) in ZnO heterostructures.

After analytically establishing possibility of achieving higher  $n_s$  in MgZnO/CdZnO heterostructure over MgZnO/ZnO heterostructure, the predictions of analytical model were confirmed experimentally by DIBSgrown MgZnO/CdZnO heterostructure. In the experimental report significantly high (~6×)  $n_s$  in MgZnO/CdZnO heterostructure was achieved as compared to that in MgZnO/ZnO, at lower Mg ( $\leq 0.15$ ) compositions in barrier MgZnO layer, with both heterostructures grown by dual ion beam sputtering (DIBS) technique. Buffer CdZnO and barrier MgZnO layers were probed separately to investigate carrier density in defect prone sputtered layers prior to development of MgZnO/CdZnO heterostructure. The MgZnO/CdZnO heterostructure was than characterized by capacitance-voltage (C-V) measurement and temperaturedependent Hall measurement to confirm the presence of quantum confined carrier density at barrier-buffer interface. The results from C-V measurement and temperature-dependent Hall measurement suggested that the enhancement in carrier densities in the MgZnO/CdZnO heterostructure over individual MgZnO and CdZnO thin films was probably due to the formation of two-dimensional electron gas (2-DEG).

Further after establishing high values of  $n_s$  in DIBS-grown MgZnO/CdZnO heterostructure, another analytical model was developed to estimate  $I_d$ characteristics in polycrystalline MgZnO/ZnO and MgZnO/CdZnO-based HFET. The developed model utilized ionized interface states density ( $Q_i$ ) and its interrelationship with the barrier layer thickness (d), Mg content (x), and electron mobility ( $\mu$ ) to account for the interface defects and their variations with electrical and physical parameters of polycrystalline heterointerface. The results achieved in this study suggested that the saturation drain current ( $I_{dsat}$ ) in MgZnO/CdZnO HFET can be comparable to that in MgZnO/ZnO HFET when  $Q_i$  enhancement is considered along with the reduction in  $\mu$ . This work extensively explored major relationships of  $Q_i$ , which governs  $I_d$  in HFETs, with d and x to convincingly postulate that the experimental  $I_d$  in polycrystalline MgZnO/ZnO and MgZnO/CdZnO-based HFETs could be a combination of the two extreme cases of  $Q_i$  dependent and independent on d and x.

After the analytical study of polycrystalline MgZnO/CdZnO-based HFET, a DIBS-grown MgZnO/CdZnO-based gateless HFET was fabricated by photolithography. Prior to development of MgZnO/CdZnO-based HFET, the conductance  $(n_s \times \mu)$  of MgZnO/CdZnO heterostructure was enhanced over MgZnO/ZnO heterostructure by introduction of a 30 nm yttria (Y<sub>2</sub>O<sub>3</sub>) spacer layer. Introduction of a crystalline Y<sub>2</sub>O<sub>3</sub> significantly enhanced the crystallinity of the buffer layer CdZnO and reduced the interface roughness at the heterojunction of MgZnO/CdZnO heterostructure. Further, transmission line measurement (TLM) technique was utilized to ascertain metal combination and annealing conditions to attain least specific contact resistivity ( $\rho_c$ ) for developing source and drain metal contacts. The results suggested that introduction of yttria spacer layer improved the overall conductance of MgZnO/CdZnO up to  $3.5 \times 10^{15}$  V<sup>-1</sup>s<sup>-1</sup> as compared to  $9 \times$ 10<sup>14</sup> V<sup>-1</sup>s<sup>-1</sup> in non-yttria spacer based MgZnO/CdZnO. After all these optimizations, the drain current-drain voltage ( $I_d$ - $V_d$ ) characteristic of the as as-developed yttria spacer based MgZnO/CdZnO HFET showed high drain current value (~400 mA/mm).

The study presented in this work, hence, establishes DIBS-grown MgZnO/CdZnO heterostructure as a viable option for low cost HFETs necessary for fabrication of large scale HFET based power and sensor devices.

## **Chapter 1**

### Introduction

Heterostructure field effect transistor (HFET) is a device that incorporates quantum-confinement of charge carriers, called two-dimensional electron gas (2DEG), at the heterojunction interface. This quantum confinement of channel reduces ionized impurity scattering of the channel carriers and hence, enhances the electron mobility and transconductance in HFETs over the traditional metal oxide semiconductor field effect transistors (MOSFETs). Some of the extremely demanding field of applications for HFETs are satellite and compact radar transceivers, low-noise amplifiers, 4G/5G communication modules [1, 2], and bio-chemical sensors etc. [3].

Gallium Arsenide (GaAs), Gallium Nitride (GaN) and other group III-V compounds are the common material systems used for the fabrication of HFETs. Recently, Zinc Oxide (ZnO), one of the group II-VI compounds, is being extensively probed for cost-effective HFET fabrication, due to reports of 2DEG in ZnO-based heterostructures [4]. ZnO has wide energy bandgap (3.4 eV), high electron saturation velocity ( $3 \times 10^7$  cm/s), lowcost native substrates, and low-temperature growth capability, making the material system a suitable candidate for HFET applications [5]. A comparison of various parameters for developing an HFET by ZnO-based heterostructure with existing GaN and GaAs based heterostructure is presented in Table 1.1. It is interesting to note that, while the contemporary GaN-based HFETs have substantial command over the present high-power transistor market, ZnO-based HFETs can provide cost-effective alternative due to the following reasons:

- (i) The cost of native substrates of ZnO (2-inch diameter and 0.5-mm thick), is nearly half as compared to that of similar dimension GaN substrates. [5-7]
- (ii) Reports of sputtered ZnO heterostructures yielding 2DEG are available in the literature [8, 9], while GaN heterostructures are generally fabricated using costly epitaxial growth mechanisms such as molecular beam epitaxy (MBE) and metal-organic chemical

vapor deposition (MOCVD). It can be pointed out that MBE is incompatible with large-area fabrication of electronic devices and MOCVD needs extreme control of multiple growth parameters alongside the precise selection of precursors [10]. Sputtering process, on the other hand, is a user-friendly, cost-effective, and large-area compatible growth technique.

#### Table 1.1

## COMPARISON OF VARIOUS PARAMETERS ESSENTIAL FOR HFET FABRICATION OF GaN, GaAs AND ZnO-BASED HETEROSTRUCTURES

Properties	Al <sub>x</sub> Ga <sub>1-x</sub> As/ GaAs	Al <sub>x</sub> Ga <sub>1-x</sub> N/ GaN	Mg <sub>x</sub> Zn <sub>1-x</sub> O/ ZnO
Saturation velocity (cm/s)	1×10 <sup>7</sup> [11]	2×10 <sup>7</sup> [11]	3×10 <sup>7</sup> [12]
Lattice mismatch x=0.1-0.4	0.014-0.056 [13]	(-0.148)-(-0.6) [14]	0.096-0.38 [14]
Density of 2DEG (cm <sup>-2</sup> )	$\sim 10^{11} - 10^{12} [15]$	~10 <sup>12</sup> -10 <sup>13</sup> [11]	~10 <sup>12</sup> -10 <sup>13</sup> [8]
Conduction band offset $x=0.1-0.4$	0.078-0.315 [13]	0.127-0.549 [14]	0.182-0.763 [14]
Breakdown field (V/cm)	4×10 <sup>5</sup> [11]	2×10 <sup>6</sup> [11]	8×10 <sup>5</sup> [8]
Energy bandgap (eV)	1.4 [11]	3.4 [11]	3.4 [12]
Native substrate cost (INR)	1× [16]	4× [6]	2× [7]
Electron mobility (at 300 K) (cm <sup>2</sup> /Vs)	~5 ×10 <sup>3</sup> [17]	~5-10 ×10 <sup>2</sup> [18]	~1-3 ×10 <sup>2</sup> [19]

Amongst various sputtering techniques, dual ion beam sputtering (DIBS) is notable for producing high-quality thin films with reasonably superior compositional stoichiometry and uniformity as well as better film adhesion over a larger substrate surface area [20]. DIBS-grown heterostructures with Magnesium Oxide (MgO) alloyed ZnO (MgZnO) as barrier layer and ZnO as buffer layer, have been reported to induce 2DEG with conductance, a

product of 2DEG density and carrier mobility, comparable to that in GaNbased heterostructures and higher than that in GaAs-based heterostructures [9].

As DIBS-grown ZnO-based heterostructures have significant potential to produce low-cost HFETs, thus it is imperative to study and analyse all possible ZnO-based heterostructures for HFET applications. The significant factor to analyse these heterostructures is their ability to yield significantly large 2DEG density  $(n_s)$ , which is majorly dependent upon the net polarization difference ( $\sigma_{net}$ ) and conduction band offset ( $\Delta E_c$ ) at the barrier-buffer interface in the HFET structure. The long-pending challenge with popular  $Mg_xZn_{1-x}O/ZnO$  heterostructure system is the occurrence of phase segregation at high Mg content (x > 0.35) in barrier layer, which limits this heterostructure from achieving high values of  $\sigma_{net}$  and  $\Delta E_c$ , subsequently to reach high values for  $n_s$  [21]. To circumvent this limitation, Beryllium Oxide was alloyed with MgZnO (Be<sub>v</sub>Mg<sub>x</sub>Zn<sub>1-x-v</sub>O) as the barrier layer has been proposed in the literature [22]. 2DEG density achieved by utilizing y = 0.2 and x = 0.26, has been found to be comparable to that achieved in the case of Mg<sub>0.6</sub>Zn<sub>0.4</sub>O/ZnO heterostructure [22]. While, BeMgZnO enhances  $n_s$  in ZnO-based heterostructures for lower Mg content,  $Be^{2+}$  ions leave the substitutional lattice sites when annealed at 400 °C and above [23]. The ohmic contact formation for HFET demands metal contacts at the source and drain regions to be annealed at  $\geq 800$  °C, which imposes the limitation for utilizing BeMgZnO or BeZnO in the barrier layer.

A possible solution to circumvent these limitations is to alloy Cadmium Oxide (CdO) in the buffer ZnO layer (CdZnO), resulting in MgZnO/CdZnO heterostructure. This would reduce the spontaneous polarization of the buffer layer (increasing  $\sigma_{net}$ ), due to higher electronegativity value of Cd over Zn [24] and increase  $\Delta E_c$ , due to lower band gap of CdZnO [25]. Both these phenomena favorably add up to a possibility of significant enhancement in  $n_s$  in MgZnO/CdZnO heterostructure with lower Mg content in the barrier layer. Therefore, this work explores the possibility of achieving high  $n_s$  and drain current ( $I_d$ ) characteristics for low-cost large-area-electronics compatible DIBS-grown MgZnO/CdZnO heterostructures for HFET applications.

The primary objective of this research work is to realize 2DEG density in MgZnO/CdZnO heterostructure using DIBS system and lithographically develop source and drain contacts on as-grown MgZnO/CdZnO heterostructure for HFET application. To achieve this objective in this thesis, initially, an analytical model is developed for the estimation of  $n_s$  in case of replacing ZnO buffer layer by CdZnO in the traditional MgZnO/ZnO heterostructure. Thereafter, MgZnO, CdZnO and MgZnO/CdZnO films are grown by DIBS for investigating formation of 2DEG in MgZnO/CdZnO heterostructures. Temperature dependent Hall measurement and C-V measurement were carried out to confirm the presence of quantum-confined  $n_s$ . Further, an analytical model is developed to estimate I<sub>d</sub> in polycrystalline MgZnO/ZnO and MgZnO/CdZnO-based HFETs. Subsequently, a gateless-MgZnO/CdZnO-based HFET is fabricated using lithography, after the optimization of the source and drain metal contact combination and annealing conditions.

This chapter summarizes the background of this work, significant parameters for the formation of 2DEG, material properties of alloys of ZnO, MgZnO and CdZnO in specific, the advantages MgZnO/CdZnO heterostructure provides over MgZnO/ZnO heterostructure towards  $n_s$  and subsequently, towards HFET application.

#### 1.1 Background

In 1979, Mimura *et al.* demonstrated first ever HFET made out of GaAs material system, which was eventually commercialized by 1985 [17, 26]. This HFET was promising to high-power high-frequency applications due to its higher bandgap (1.4 eV) and electron mobility (~5000 cm<sup>2</sup>/Vs) compared to Si MOSFETs with 1.1 eV bandgap and 1400 cm<sup>2</sup>/Vs. In 1993, Khan *et al.* demonstrated GaN material system-based HFET, which has higher bandgap (3.4 eV), higher breakdown voltage (2 MV/cm) and higher electron saturation velocities (2 ×  $10^7$  cm/s) as compared to GaAs [18].

However, lack in availability of native substrates of GaN adds to its fabrication cost, which is unfavorable to large-scale fabrication of HFETs.

ZnO provides an inexpensive and competitive material system compared to GaN. HFETs fabricated by ZnO material system have potential to sustain high radio frequency (RF) power owing to its wide bandgap (3.4 eV), high breakdown field (0.8 MV/cm), large conduction band offset, and high saturation velocity  $(3 \times 10^7 \text{ cm/s})$  [12, 14]. The first time demonstration of 2DEG in MgZnO/ZnO heterostructure (with  $n_s = 6 \times 10^{12}$  cm<sup>-2</sup> and  $\mu = 130$ cm<sup>2</sup>/Vs ) was published in 2004 [27] and first MgZnO/ZnO-based HFET  $(n_{\rm s} = 1.2 \times 10^{13} \text{ cm}^{-2} \text{ and } \mu = 170 \text{ cm}^2/\text{Vs})$  is demonstrated by Koike *et al.* using MBE in 2005 [19]. In 2006, Tampo et al. [28] improved the electron mobility of same heterostructure grown by MBE by growing Zn polar ZnO buffer layer, from ~100 to 250 cm<sup>2</sup>/Vs, with  $n_s$  maintained ~1×10<sup>13</sup> cm<sup>-2</sup>. In 2010, first time demonstration of 2DEG in sputtered deposited MgZnO/ZnO heterostructure was reported by Chin et al. [8]. In 2018, Singh et al. reported formation of 2DEG in DIBS grown MgZnO/ZnO heterostructure [9]. The presented literature survey suggests, ZnO based heterostructures have been reliably grown by various growth techniques with consistency in the  $n_s$  and  $\mu$  values, and therefore, have been used in fabrication of HFET [29-31] and are being extensively probed for further HFET applications. Further, as sputtering process is a cost-effective and large-area compatible growth technique, this opened up the possibility of fabrication of low-cost HFETs.

While, MgZnO/ZnO heterostructure has shown to induce high twodimensional electron gas (2DEG) sheet density ( $n_s$ ) (~ 10<sup>13</sup> cm<sup>-2</sup>) at room temperature by Tampo *et al.* [32], the Mg composition required to achieve such high  $n_s$  has been as high as 0.6 in barrier layer MgZnO, which is difficult to fabricate without the occurrence of phase separation [33]. This implies that for lower Mg composition in barrier layer, higher 2DEG density is very difficult to achieve in MgZnO/ZnO heterostructure. Ding *et al.* has proposed Be<sub>y</sub>Mg<sub>x</sub>Zn<sub>1-x-y</sub>O as the barrier layer to circumvent this limitation and has achieved 2DEG density comparable to that achieved in the case of Mg<sub>0.6</sub>Zn<sub>0.4</sub>O/ZnO heterostructure achieved by utilizing y = 0.2 and x = 0.26 [22]. Benharrats *et al.* have shown that 2DEG can be increased further with the use of CdZnO/ZnO heterostructure [34]. Although the use of CdZnO/ZnO, BeZnO/ZnO, or BeMgZnO/ZnO heterostructures are beneficial for enhancing 2DEG density compared to that in MgZnO/ZnO, the main drawback of all these structures is that the polarization in ZnO buffer does not change significantly. Therefore, any improvement in 2DEG density is solely governed by the change in the polarization in barrier layer. A possible option to circumvent this limitation proposed in this work is to alloy CdO in the buffer layer, which would result in MgZnO/CdZnO heterostructure, instead of MgZnO/ZnO or CdZnO/ZnO. This provides an opportunity to modulate the barrier as well as buffer layer polarization components towards enhanced  $n_{\rm s}$ , which otherwise has been restricted to barrier layer only. Therefore, this work explores the possibility of achieving high 2DEG density in low-cost large-area-electronics compatible DIBS grown MgZnO/CdZnO heterostructure towards eventual fabrication of HFET.

# 1.2 Material Parameters for Two Dimensional Electron Gas (2DEG)1.2.1 Heterostructure: Band Gap Discontinuity

A heterostructure is formed when two different materials are stacked over one another keeping their individual properties intact. In case of presence of a large band gap difference at the interface of such heterostructures, an energy discontinuity is created in the energy band spectrum at the interface. For centrally band aligned heterostructures with either material being undoped or *n*-type doped, the energy discontinuity makes the energy band to bend in the formation of a notch in the conduction band and a valley in the valence band at the interface, both of which are formed in the lower band gap material. Fig. 1.1 visualizes a band diagram of before and after the junction formation in heterostructure materials that yield such band gap discontinuity. In case the notch formation in the conduction band lies below fermi energy level, the energy states lying below fermi energy level have the potential to accommodate electrons free from the influence of the lattice atoms of either materials, forming a quantum potential well. Such energy states are called two-dimensional energy states (2DES) as they can accommodate two-dimensional electron gas (2DEG). Therefore, this notch's depth defines the ability of the heterostructure to accommodate 2DEG. The notch's depth is defined by the conduction band discontinuity ( $\Delta Ec$ ) or the conduction band offset, which in turn is dependent upon the difference in the band gap of two materials known as bandgap discontinuity ( $\Delta Eg$ ).

Considering the case of ZnO based heterostructure with MgZnO being the high band gap material (barrier layer) and ZnO being the low band gap material (buffer layer). The content of magnesium in the barrier layer defines the bandgap of MgZnO. In case of MgZnO/ZnO heterostructure,  $\Delta Ec$  is calculated as  $\Delta Ec = 0.9 \times \Delta Eg$  [14].



Fig. 1.1: Schematic Energy Band diagram, drawn under the Anderson's rule [35] with ideal assumption of no chemical reaction between the two interacting layers, of 2DEG yielding heterostructure under thermodynamic equilibrium condition, with Schottky contact at barrier surface with barrier height  $\phi_b$ . Here,  $E_c$  is conduction band minimum,  $E_F$  is Fermi energy level,  $E_V$  is valence band maximum.

#### **1.2.2 Polarization in Heterostructures**

In compound materials with asymmetric lattice structures with covalent bonding like GaN, and GaAs, or with borderline iconicity between covalent and ionic like that in ZnO, the electronegativity of different elements in the lattice creates a dipole like electron cloud distribution at every bonding pair. The vector summation, of all such dipoles over the unit lattice structure, provides a net local dipole that creates a long-range polarization in the compound in absence of an external electric field, called spontaneous polarization ( $P_{sp}$ ). When such lattices are mechanically stretched or compressed, the relative position of the lattice elements is altered. This change in displacement between two polarities of the dipole moment at the bonding pairs alters the polarization of the compound. Such mechanical stress induced polarization is called piezoelectric polarization ( $P_{zp}$ ).

In case of a heterostructure with polarization in both layers, a polarization difference can be formed at the interface of such heterostructures if polarization in either of the layers exceeds the polarization of the other layer. This creates an imbalance in the net electric neutrality of such heterostructure stack. This net polarization difference at the interface of the heterostructure induces an electric field capable of sweeping free charges of opposite polarities present in the heterostructure. These free charges are accumulated at the interface of the heterostructure under the electrostatic attraction of the net polarization difference present at the interface. As the opposite polarity free charge carriers are accumulated near the interface, they neutralize the net polarization difference and therefore reduces the electric field to zero. These free charge carriers accumulated at the interface can be holes or electrons depending upon the polarity (positive or negative) of the net polarization difference that is formed at the interface of the heterostructure stack, as shown in Fig.1.2. The polarity of polarization of the material at the interface is generally dependent upon the growth face of the crystal.

In case of ZnO-based devices, the direction of  $P_{sp}$  depends on the growth face of the crystal (Zn or O at the surface). As the ZnO buffer layer is generally thick (~1 µm) [8, 36], it is strain relaxed and hence  $P_{zp}$  component is not significant in ZnO buffer. However, the MgZnO barrier layer being very thin is always strained. Hence, in addition to  $P_{sp}$ , barrier MgZnO layer also possess  $P_{zp}$ . For an MgZnO/ZnO heterostructure, a net polarization difference charge is developed at the interface, the polarity of which depends on the face of the growth of the crystal. In case there is a positive charge polarization difference at the interface of the MgZnO/ZnO heterostructure, it is compensated by the equal negative charge (free electrons swept by electric field). As these electrons accumulate at the interface under the electrostatic force of positive net polarization difference, due to the presence of conduction band notch below fermi energy level at the MgZnO/ZnO heterojunction, a 2DEG is formed close to the interface.



Fig. 1.2: Polarization charge in 2DEG yielding heterostructure, (a) Charge polarization in individual materials,  $\sigma_{barrier}$  and  $\sigma_{buffer}$  in barrier and buffer layers is the sum of both spontaneous and piezoelectric polarization in individual layers, (b) Total sum of all the polarization results in a net positive charge at the interface ( $\sigma_{net}$ ).

# 1.3 CdZnO and MgZnO: Alloys of ZnO

### **1.3.1 Structural Properties**



Fig. 1.3: Schematic representation of thermodynamically stable lattice structures of ZnO, MgO and CdO with phase segregation limits of  $Mg_xZn_{1-x}O$  and  $Cd_xZn_{1-x}O$ .

Among the two lattice structures of ZnO, hexagonal wurtzite [37] and cubic zincblende [38], wurtzite structure is the most thermodynamically stable structure of ZnO at ambient conditions. This is due to its iconicity that falls at the verge of the covalent and ionic materials. At room temperature (RT) the hexagonal wurtzite ZnO has lattice parameters a =3.25 Å and c = 5.20 Å [39]. In contrast, MgO and CdO are thermodynamically stable in rocksalt structure with lattice parameter a =4.216 Å and 4.689 Å, respectively. As shown in Fig. 1.3, alloying MgO and CdO above ~35 at. % in ZnO leads to phase segregation in MgZnO and CdZnO [21, 40]. The alloying of MgO and CdO in ZnO increases the lattice constant a of the alloyed Mg<sub>x</sub>Zn<sub>1-x</sub>O (a = 3.248 Å (at x = 0.05) to 3.261 Å (at x = 0.3) [41, 42] and Cd<sub>x</sub>Zn<sub>1-x</sub>O (a = 3.271 Å (at x = 0.05) to 3.378 Å (at x = 0.3)) [34, 41]. Since, the lattice parameter *a* of CdZnO increases at a higher rate compared to that of MgZnO, the straining of MgZnO barrier layer is tensile for MgZnO/CdZnO heterostructure as opposed to the compressive straining in MgZnO/ZnO heterostructure. This phenomenon increases the net polarization in the MgZnO barrier layer as the  $P_{zp}$  due to tensile straining adds up with the orientation of the  $P_{sp}$  of the MgZnO layer, as shown in Fig. 1.4. This in turn increases net polarization difference and subsequently the 2DEG density at the MgZnO/CdZnO heterointerface compared to that in MgZnO/ZnO heterostructure.


Fig. 1.4: The schematic representation of (a) MgZnO/ZnO lattice structure with compressive straining of MgZnO layer resulting in  $P_{zp}$  directed opposite to that of  $P_{sp}$ , (b) MgZnO/CdZnO lattice structure with tensile straining of MgZnO layer resulting in  $P_{zp}$  aligning in the direction of  $P_{sp}$ .

## **1.3.2 Electrical Properties**



Fig. 1.5: Energy bandgaps, and lattice constants of ZnO, MgO and CdO compounds.

ZnO is recognized amongst the large bandgap materials with a direct band gap of ~3.4 eV at room temperature [11]. This make it suitable for high frequency and high power applications. The bandgap of ZnO can be tuned by alloying it with MgO and CdO. As shown in Fig. 1.5, alloying MgO in ZnO increases the energy bandgap ( $E_g$ ) of resulting Mg<sub>x</sub>Zn<sub>1-x</sub>O alloy (3.37 + 2.145x) [43] and alloying CdO in ZnO reduces the energy bandgap of resulting Cd<sub>x</sub>Zn<sub>1-x</sub>O (3.37 - 2.28x + 0.95x<sup>2</sup>) [25]. As  $\Delta E_c$  is directly proportional to the difference in the energy bandgaps of barrier and buffer layers, CdZnO in buffer layer provides ability to increase the  $\Delta E_c$  value after attaining the maximum limit of Mg content without induction of phase segregation in barrier layer MgZnO. For the initial review of the advantages of utilizing CdZnO as a Buffer layer, we have utilized the work of Park *et*  *al.* [44], which suggested that in MgZnO/Cd<sub>x</sub>Zn<sub>1-x</sub>O heterostructure, as we increase *x* from 0 to 0.2, the quantum well (QW) depth increases due to decrease in energy band gap of CdZnO. Hence, we can assume as we alloy ZnO with CdO, the conduction band offset between MgZnO and CdZnO increases. In their work, Park *et al.* analysed the band structures and wave functions for the CdZnO/MgZnO QW structures by solving the Schrödinger equation for electrons and the 3 × 3 Hamiltonian for holes [45]. As increase in  $\Delta E_c$  is directly proportional to increase in  $n_s$ , MgZnO/CdZnO heterostructure shows promise of achieving higher  $n_s$  values compared to that in MgZnO/ZnO heterostructure.

The thermal conductivity and dielectric constant of ZnO are 0.6 Wcm<sup>-1</sup> [46] and 8.75 [43], respectively. The thermal conductance of the material characterizes the ease with which heat can be dissipated by the material. This is a crucial parameter as undissipated heat in the device degrades the stability and performance of the electronic device. In addition, the dielectric constant defines the capacitive loading capability of the transistor made of that material and affects the device terminal impedances [47]. The dielectric constant of wide bandgap semiconductors is approximately 20% lower than the traditional semiconductors, allowing 20% area increase for similar order impedance. An increased device area allows for higher current carrying capacity and therefore higher RF power. Comparing the dielectric constant of ZnO with GaN (8.9) [48] and GaAs (12.46) [49], ZnO has a lower value which makes ZnO and its alloys more suitable for RF applications.

Various electrical properties of ternary oxides like MgZnO and CdZnO can be computed by interpolation using Vegard's law given by the formula [50],

$$P(A_x Z n_{1-x} 0) = x P(A0) + (1-x)P(Zn0) + bx(1-x)$$
(1.1)

where A is alloying element Mg or Cd, P(x) represents the electrical property to be interpolated and b represents the bowing parameter which has to be experimentally determined for accurate interpolation.

## 1.4 Challenges in Development of MgZnO/CdZnO HFET

As MgZnO/CdZnO heterostructure-based HFET is not available in literature, fabrication of it is an unchartered territory. The roadmap to its fabrication is inspired from MgZnO/ZnO based HFET, however, sputtering-based ZnO based HFET is not found in literature. This creates opportunities and challenges unknown in prior literature. The major expected challenges in the fabrication of MgZnO/CdZnO-based HFET are as follows:

- (i) Realization of 2DEG in DIBS grown MgZnO/CdZnO heterostructure.
- (ii) Achieving higher conductance in DIBS grown MgZnO/CdZnO heterostructure compared to that in MgZnO/ZnO heterostructure.
- (iii) Selection of source and drain contact materials and fabrication of low contact resistance providing source and drain contacts on wide bandgap MgZnO top surface.

## 1.5 Aim and Objectives

The main aim of this thesis is to explore analytically and then realize 2DEG in MgZnO/CdZnO heterostructure towards HFET using DIBS as it is low-cost, large-area fabrication compatible. Steps involved in order to achieve the above objectives are as follows:

- (a) Development of a physics-based analytical model for the estimation of 2DEG density in MgZnO/CdZnO heterostructure and analyze the impact of CdZnO as buffer layer over traditional MgZnO/ZnO heterostructure.
- (b) Validation of the developed analytical model with the published experimental data in the literature.
- (c) Realization of 2DEG in MgZnO/CdZnO heterostructure by DIBS after optimizing growth conditions.

- (d) Validation of analytically predicted enhancement of 2DEG in MgZnO/CdZnO over MgZnO/ZnO for lower Mg content in MgZnO barrier layer.
- (e) Development of analytical model to estimate *I*<sub>d</sub> in polycrystalline MgZnO/ZnO and MgZnO/CdZnO HFETs.
- (f) Utilization of ionized interface states density as a crucial empirical parameter to define  $I_d$  in polycrystalline MgZnO/ZnO and MgZnO/CdZnO HFETs.
- (g) Optimization of the MgZnO/CdZnO heterostructure to achieve enhanced conductance over MgZnO/ZnO heterostructure.
- (h) Selection of the source and drain contact material combination based upon transmission line measurement (TLM) technique and optimization of annealing conditions to achieve least contact resistance.
- (i) Development of source and drain contacts by lithography process to develop DIBS grown MgZnO/CdZnO-based gateless HFET with high drain current density.

#### **1.6 Organization of the thesis**

The research in this thesis has focused on the realization of 2DEG in MgZnO/ZnO heterostructures using sputtering for HEMT. The thesis is organized as follows:

*Chapter 2* describes the deposition and characterization techniques utilized for probing DIBS gown MgZnO/CdZnO heterostructures and its HFET. The used systems are DIBS system, X-Ray Diffraction, Variable-anglevariable wavelength Spectroscopic Ellipsometry, Four Probe Hall, I-V, and C-V Measurements, Energy dispersive X-Ray Spectroscopy, and High-Resolution Transmission Electron Microscopy, Photolithography,.

*Chapter 3* provide a physics based analytical model for the estimation of 2DEG density in ZnO capped and bilayer MgZnO/CdZnO heterostructures. Factors largely affecting the 2DEG density are Mg composition in MgZnO layer, barrier and cap layer thicknesses; were examined in detail. The

purpose is to analyse the effect on 2DEG density of MgZnO/ZnO heterostructure by replacing the buffer ZnO by CdZnO.

*Chapter 4* describes the realization of 2DEG in MgZnO/CdZnO heterostructures and validation of the analytical prediction that higher 2DEG (~6 times) can be achieved in MgZnO/CdZnO heterostructure for lower Mg content in barrier layer (< 0.15) as compared to similar dimensions and Mg content in MgZnO/ZnO heterostructure.

*Chapter 5* details an analytical model to estimate the drain current  $(I_d)$  in polycrystalline MgZnO/ZnO and MgZnO/CdZnO HFETs.

*Chapter 6* describes the fabrication of linear transmission line measurement (TLM) contacts for contact resistance optimization, these optimized metal contacts are used to fabricate source and drain contacts on top of DIBS grown MgZnO/CdZnO heterostructures using lift-off process for transistor application.

*Chapter* **7** draws conclusions from the thesis and proposes the scope for future works for continuation of the research.

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# Chapter 2

# Experimental Tools and Characterization Techniques for Development of MgZnO/CdZnO-based HFET

In this chapter, growth and characterization techniques utilized to experimentally achieve 2DEG yielding MgZnO/CdZnO heterostructure are briefly discussed. In addition, the experimental tools to develop HFET from as-grown MgZnO/CdZnO heterostructure is also detailed. To develop an HFET out of an entirely new material combination of MgZnO/CdZnO, an extensive analytical study was performed before starting the experimental fabrication and characterization of the as-developed device. After analytically arriving at the conclusion that utilizing MgZnO/CdZnO could yield higher two-dimensional electron gas (2DEG) as compared to that in MgZnO/ZnO, the MgZnO/CdZnO heterostructure was fabricated using Dual Ion Beam Sputtering (DIBS) system. The as-grown MgZnO/CdZnO heterostructure was characterized for structural and stoichiometric conformation and thereafter 2DEG was ascertained by electrical characterizations. The crystal structure of the samples was characterized using X-Ray diffraction (XRD) system. Hall, current-voltage (I-V), and capacitance-voltage (C-V) measurement characterized the electrical properties of these heterostructures. The atomic composition of the samples for the presence of different elements was investigated by energy dispersive X-Ray (EDX). Further, the quality of the material interface of MgZnO/ZnO was investigated by high-resolution transmission electron microscopy (HRTEM) measurement. After establishing the presence of 2DEG in MgZnO/CdZnO heterostructure by aforementioned characterizations, lithography was utilized to develop gateless-HFET on as-grown MgZnO/CdZnO heterostructures. To attain this, first metal combinations were analyzed by transmission line measurement (TLM) study to achieve least ohmic contact resistance for the formation of source and drain contacts. The least contact providing metal combination was than grown as part of three-step lithography to pattern and develop source and drain contacts.

# 2.1 Experimental and Characterization Setup for 2DEG yielding MgZnO/CdZnO

This section describes in detail the growth technique, and characterization facilities utilized to fabricate 2DEG yielding MgZnO/CdZnO heterostructure by DIBS.

#### 2.1.1 Thin Film and Heterostructure Growth by DIBS

Prior to the deposition of MgZnO, CdZnO and MgZnO/CdZnO physical layers by DIBS, silicon (Si) wafers were cleaned by simple degreasing process [1]. These wafers are than loaded in the load-lock chamber (LLC) of the DIBS. The wafers are transferred into the main deposition chamber (DPC) at the substrate holder position by a robotic arm.

The DIBS is a very efficient physical vapor deposition technique for oxide materials' thin film deposition in ultrahigh vacuum conditions [2]. DIBS system has two ion beam sources as shown in the schematic of Fig. 2.1. The primary deposition is done by *radio-frequency* (RF) deposition ion beam source that sputters materials from a target fixed in a four target assembly onto the intended substrate. The *direct-coupled* assist ion source pre-sputters the substrate surface prior to film deposition and also hinders island formation by removing weak dangling bonds during the actual sputtering process [3]. A few other unique features of the DIBS system are high-quality growth with reduced surface roughness, increased growth uniformity on a larger substrate area and in-situ substrate pre-cleaning before growth.

The growth conditions were optimized for individual MgZnO and CdZnO. Utilizing the optimized growth conditions, 250 nm MgZnO and CdZnO thin films were deposited onto *p*-Si wafer to ascertain the uniformity of characteristics, prior to deposition of 30 nm MgZnO over 250 nm CdZnO onto a 3" Si wafer.



Fig. 2.1: Schematic illustration of deposition of MgZnO, CdZnO and MgZnO/CdZnO heterostructure on three Si wafers by DIBS system.



Fig. 2.2: The actual image of DIBS System.

The background pressure inside the deposition chamber was maintained at  $10^{-8}$  mbar. The heater assembly above the deposition chamber that is used to heat the sample was kept at 300 °C during the growth of the thin films and heterostructure. The water chiller was deployed to remove heat from the deposition chamber, target assembly, and vacuum pumps. DIBS system growth parameters, i.e., deposition temperature, gas pressure, gas

composition and RF power are controlled by the parameter controlling unit of the DIBS system [2, 3].

#### **2.1.2 Characterization Techniques**

The equipment used for the characterization of thin films and heterostructures in this research work are demonstrated briefly in the following sections.

### 2.1.2.1 X-Ray Diffraction Measurement

In this work, the crystallinity, phase, strain, and preferred orientation of Mg<sub>x</sub>Zn<sub>1-x</sub>O (x = 0.05, 0.15, 0.2 and 0.3) and CdZnO thin films were examined using Rigaku SmartLab, Automated Multipurpose X-Ray Diffractometer equipped with a copper target (Cu-K $\alpha$ ) to generate the incident X-Rays of wavelength  $\lambda = 0.154178$  nm for the diffraction measurement in Bragg Brentano configuration. The photographic image of this XRD system is shown in Fig. 2.3.

A collimated beam of X-Rays is incident on the as-grown MgZnO and CdZnO thin film samples and diffracted by the crystalline phases in the samples according to Bragg's law such that:

$$n\lambda = 2d\,\sin\theta \tag{2.1}$$

where  $\lambda$  is the wavelength of the incident X-Ray beam, *d* is the inter-plane separation of lattice between atomic planes in the crystalline phase,  $\theta$  is the angle between atomic planes and the incident X-Rays beam and *n* is an integer that represents the interference order.

The intensity of the diffracted X-Rays is measured as a function of the diffraction angle  $2\theta$ . The diffraction pattern thus obtained is used to identify the sample's crystal orientation [4].



*Fig. 2.3: Photograph of Rigaku SmartLab, Automated Multipurpose X-Ray Diffractometer.* 

## 2.1.2.2 Energy-dispersive X-Ray spectroscopy



Fig. 2.4: Image of EDX, Zeiss Supra 55.

The atomic composition of different elements in Mg<sub>x</sub>Zn<sub>1-x</sub>O (x = 0.05, 0.15, 0.2 and 0.3) and Cd<sub>0.15</sub>Zn<sub>0.85</sub>O was characterized using energy dispersive X-Ray (EDX, Zeiss Supra 55). The image of the utilized EDX system is shown in Fig. 2.4. EDX is a chemical microanalysis technique used in conjunction with scanning electron microscopy (SEM). The EDX

technique detects X-Rays emitted from the sample during the bombardment of an electron beam to detect the elemental composition of the samples. The samples were scanned at multiple 1  $\mu$ m<sup>2</sup> area locations to achieve a reliable average composition of various elements present in the sample. The spectrum of X-Ray energy versus counts is evaluated to determine the elemental composition of the sampled area. Quantitative results can be derived from the relative X-Ray counts at the characteristic energy levels for the sample constituents [5].

# 2.1.2.3 Variable Angle Variable Wavelength Spectroscopic Ellipsometry Measurement System

In this work, M-2000D J. A. Woollam Variable Angle Variable Wavelength Spectroscopic Ellipsometer was utilized to determine the thickness of MgZnO, CdZnO thin films to achieve average rate of growth under various growth conditions. In this Ellipsometer, the measurements can be performed at various angles with respect to the plane of the sample and at various wavelength range of 200-1000 nm. The photographic image of Variable Angle Variable Wavelength Spectroscopic Ellipsometer is shown in Fig. 2.5.

Ellipsometry technique measures a change in polarization as light reflects or transmits from a material structure [6]. The polarization change is represented as an amplitude ratio,  $\Psi$ , and the phase difference,  $\Delta$ . The measured response depends on optical properties and thickness of individual materials. Thus, ellipsometry is primarily used to determine film thickness and optical constants. However, it can also be utilized to estimate the composition, crystallinity, roughness, doping concentration, and other material properties associated with a change in optical response [6].

Each sample was measured multiple times for light incident at different locations of the samples to determine the uniformity of thickness and optical characteristics of each sample. The absorption coefficient obtained from the fitting of the  $\Psi$  and  $\Delta$  vs varying incident wavelengths is utilized to determine the optical bandgap of the samples. The transmission

coefficient is provided by the Ellipsometer given the film and sample overall is significantly transparent. This transmission coefficient directly provides the energy bandgap of the grown film, given the bare substrates transmission coefficient has been measured prior to the deposition of the film.

The primary components of the ellipsometry system are a light source, polarization generator, sample, polarization analyzer, and detector [7]. The polarization generator and analyzer are constructed of optical components that manipulate the polarization: polarizers, compensators, and phase modulators.



*Fig. 2.5: Photographic image of Variable Angle Variable Wavelength Spectroscopic Ellipsometry system.* 

## 2.1.2.4 High-Resolution Transmission Electron Microscopy

In this work, the quality of MgZnO/CdZnO, MgZnO/CdZnO/SiO<sub>2</sub> and MgZnO/CdZnO/Y<sub>2</sub>O<sub>3</sub> interfaces were observed using high-resolution transmission electron microscopy (HRTEM). All TEM and SAED images in this Thesis work were captured by Mr Tomohiko Yamakami and provided by Dr. Myo Than Htay of the Technical Division, Faculty of Engineering, Shinshu University. The photographic image of HRTEM is shown in Fig. 2.6.



Fig. 2.6: Photographic image representation of HRTEM.

TEM is a technique that utilizes the interaction of energetic electrons with the sample to provide morphological, compositional and crystallographic information of the samples. The electron emitted from the filament are modulated through multiple electromagnetic lenses before contacting the screen where the electrons are converted into luminescence, and a very high-resolution image of the analyzed sample is obtained. The resolution of image is directly related to the speed of electrons which determines the wavelength. A modern TEM is composed of an illumination system, a condenser lens system, an objective lens system, a magnification system, and the data recording system. Finally, a set of intermediate lenses that magnify this image and projects them on a phosphorous screen or a charge coupled device (CCD). TEM can be used in imaging and diffraction mode [8].

HRTEM utilizes both the transmitted and the scattered beams to create an interference image. It is a phase contrast image and the resolution of the image can becomes as small as the unit cell of the crystal. It is utilized for the characterization of point defects, stacking faults, dislocations, grain boundaries, and surface and interface structures [8].

#### 2.1.2.5 Hall Measurement System

The electrical transport properties, such as, carriers concentration, electrical resistivity, and the mobility of carriers, of the MgZnO, CdZnO thin films and MgZnO/CdZnO heterostructures were characterized by Hall Effect measurements using the Van der Pauw configuration. The experimental setup used for Hall Effect measurement is shown in Fig. 2.7. Here, square samples of 1 cm  $\times$  1 cm are soldered with Indium (In) contacts at four corners in the configuration shown in Fig. 2.8. These samples are then mounted onto the sample holder and are sourced current by Keithley 2612 A source meter. The magnetic field density (B) in the electromagnets are controlled by constant current supply and B is measured by digital Gauss meter. For our experiment B is set at ~0.5 Tesla. The amount of current sourced by Keithley source meter and read-back of Hall voltage were performed using a software interface namely Lab Tracer. A small current (-50  $\mu$ A to 50  $\mu$ A) was swept across two terminals and voltage was read back from remnant terminals.



Fig. 2.7: Photographic image of Hall measurement setup used to attain electrical properties of MgZnO, CdZnO thin films and MgZnO/CdZnO heterostructure.

At equilibrium, the voltage that appears at the semiconductor edges is called Hall voltage ( $V_{\rm H}$ ). From  $V_{\rm H}$ , sheet carrier concentration ( $n_{\rm s}$ ) of the semiconductor is determined by [4]

$$n_S = \frac{IB}{q|V_H|} \tag{2.1}$$

where I is the current flowing in the semiconductor, B is the applied magnetic field and q is the elementary charge.



Fig. 2.8: Schematic of In contacts placed on MgZnO/CdZnO heterostructure for Hall measurement.

The Hall mobility of the samples was measured with the help of  $n_s$  and sheet resistance ( $R_s$ ) and is given by the relation

$$\mu = \frac{1}{q n_s R_s} \tag{2.2}$$

## 2.1.2.6 I-V and C-V Measurement system

The current-voltage (*I-V*) measurement was used to identify ohmic and Schottky metal contacts on the as-grown MgZnO/CdZnO heterostructure. The Schottky contact is than utilized to attain depth based carrier density profile of the MgZnO/CdZnO heterostructure by capacitance-voltage (*C*-V) measurement. In addition, the *I-V* measurements were utilized in determining resistance in ohmic contacts, details of which are discussed in later sections.

Fig. 2.9 and 2.10 shows the photographic images of equipments used for I-V and C-V measurement. Fig. 2.9 shows the probe station setup that includes Everbeing cryogenic probe station with the measurement temperature range of 77 K to 350 K, with probing-tip resolution up to 10

 $\mu$ m. Fig. 2.10(a) and (b) shows the photographic images of two source meters Keithley 2612A and 4200 A, resepectively, used for *I-V* and *C-V* measurements.



Fig. 2.9: Photographs of probe station used for I-V and C-V measurements



*Fig. 2.10: Images of (a) Keithley 2612A and (b) Keithley 4200A semiconductor parameter analyzer.* 

## 2.2 Experimental Setup for MgZnO/CdZnO-based HFET

After confirmation of presence of 2DEG in as-grown MgZnO/CdZnO heterostructure the heterostructures were utilized to develop DIBS grown MgZnO/CdZnO-based HFET. Lithography was utilized to develop source and drain contacts in a four level lithography process. Prior to developing source and drain contacts the ohmic contact was optimized for least contact resistance. The tools and techniques utilized to attain DIBS grown MgZnO/CdZnO gateless-HFET is discussed in this section.

## 2.2.1 Lithography

Lithography in semiconductor manufacturing is the process of transferring intended geometric features from a lithography mask onto the surface of the substrate. Different lithography techniques such as photolithography, UV-lithography, and e-Beam lithography use optical radiation, UV radiation, and e-Beam radiation, respectively, to image the lithography mask on the sample surface using photoresist (PR) layers. The steps involved in the photolithographic process are wafer cleaning; moisture baking; photoresist application; soft baking; mask alignment; exposure and development; and hard-baking.

# 2.2.1.1 Wafer Cleaning, Moisture Baking, and Photoresist Application

In wafer cleaning, the wafers are chemically cleaned using trichloroethylene (TCE), acetone and isopropanol (IPA), to remove particulate matter on the surface as well as any traces of organic, ionic, and metallic impurities utilizing degreasing process. After cleaning, the wafers are moisture baked at 120 °C for 45 minutes to evaporate traces of water. After moisture baking, the photoresist is coated on the desired surface of the wafer using Spin Coating process. The thickness of the PR coat on the wafer is determined by two parameters, i) viscosity of the PR and ii)

rotational speed of the spin coater. In this work, a positive photoresist S-1818 was utilized at 1000 rpm spin coating speed for 60 seconds to attain 3  $\mu$ m thickness.

#### 2.2.1.2 Soft Baking

Soft baking is the step during which almost all of the solvents are removed from the photoresist coating. In this work, the optimized soft baking recipe is 120 °C for 30 minutes. Soft baking is a very crucial for photo-imaging. The photoresist coatings is made photosensitive after soft baking. Excess soft baking will degrade the photosensitivity of resists by either reducing the developer solubility or by destroying parts of the sensitizer. Lack of sufficient soft baking will prevent light from reaching the sensitizer.

#### 2.2.1.3 Lithography Masks

The lithography masks are designed using L-Edit software and then developed on a glass plate using cobalt chrome. Fig. 2.11 shows the L-Edit image of the designed masks. There are two types of mask light field and dark field mask. In light field mask, the UV light is passing through the entire mask except for the desired image to be replicated on the wafer. Whereas in dark field mask the UV light passes only through the desired image printed on the mask and rest of the portion is opaque. In this work, the mask for active area formation is a light field mask, and remaining masks are dark field masks.



Fig. 2.11: The L-Edit image of the mask in which green color mask is for active area formation, the red one is for insulator pad formation, the gray one is for source and drain contact fabrication.

#### 2.2.1.4 Mask Alignment; Exposure and Development

A photomask is a square glass plate patterned with an emulsion of the metal film on one side. The mask is aligned with the wafer to transfer the pattern onto the wafer surface. In this work, three level of lithography is used and hence, each mask after the first needed to be aligned with the previous pattern. Once the mask has been accurately aligned with the alignment markers of the previous pattern on the wafer's surface, the photoresist is exposed through the pattern on the mask with high-intensity ultraviolet light. In this work, the optimized recipe of exposure is 30 seconds of UV light exposure.

Further, the UV-exposed patterned wafers are dipped in the developer CD-26 to dissolve the softened PR. The optimized recipe for the developing used in this work is 25 seconds dip and hold and then 25 seconds rinse the wafers in the developer solution followed by rinsing in de-ionized (DI) water for 1 minute.

#### 2.2.1.5 Hard Baking

Hard-baking is the final step in the photolithographic process. The optimized recipe for this work is hard-baking for 120 °C for 30 minutes. This step is necessary in order to harden the photoresist and improve adhesion of the photoresist to the wafer surface.

## 2.2.2 Lift-off Process

In this work, linear transmission line measurement (TLM), source, and drain contact formation is performed utilizing lift-off process.

In lift-off a complimentary image of the desired pattern is patterned upon PR covered wafer using a dark field mask. After the development, the exposed area is developed to form trenches in the PR coat. The metal layer to be developed is then deposited over the PR coated wafer with trenches. The metal layer fills the trenches in the PR and gets deposited over the PR on the rest of the area of wafer.

After the metal layers have been deposited, the wafer is immersed in acetone to dissolve the PR layer. Once the PR is dissolved, the metal layer over PR gets 'lifted off', leaving behind the metal layer deposited only in the trenches developed by lithography. Fig. 2.12 shows the complete process flow of the lift-off process.



Fig. 2.12: The complete process flow of the lift-off process.

In this work, all the metal deposited wafers were kept in acetone for 15 hours and then agitated in ultra-sonicator for 2 min and then 1 min break.

# 2.2.3 Lithography Process for Transmission Line Measurement

In this work, linear transmission line measurement (TLM) technique is utilized to measure contact resistance of the ohmic contacts to be developed as source and drain contacts. The dark field TLM masked shown in Fig. 2.13(a) is utilized to pattern 3  $\mu$ m thick positive PR on MgZnO/CdZnO heterostructure grown wafers. The patterned wafers are than developed and hard baked prior to growth of metal layers. After deposition of metal layers, the wafers are immersed in acetone for 15 hours and then agitated in ultrasonicated. The metal contacts remain on the surface of the wafer form linear

TLM configuration, as shown in Fig. 2.13(b), and is utilized to measure the contact resistance.



Fig. 2.13: (a) The TLM mask designed in L-Edit and the photographic image of the developed mask. (b) The schematic of the developed TLM on the heterostructure grown wafer.

# 2.2.4 Lithography Process for Transistor Fabrication

## 2.2.4.1 Active Area Formation

MgZnO/CdZnO heterostructure grown on Y<sub>2</sub>O<sub>3</sub> is coated with positive PR of 3  $\mu$ m after wafer cleaning, moisture baking. A light field mask is used to pattern the coated PR by UV exposure in rectangular geometry of 1030  $\mu$ m × 300  $\mu$ m. After developing and hard baking the wafers are immersed in extremely diluted HCl (5 ml HCl in 200 ml DI water) for an optimized time of 50 second to etch the exposed heterostructure from the wafers. The etched wafers are than immersed in acetone for removing the hard baked PR from the active region islands.



*Fig. 2.14: The schematic of the bright field mask and developed active layer island.* 

### 2.2.4.2 Mesa Isolation Formation

After active island formation a 400 nm thick layer of SiO<sub>2</sub> is deposited all over the wafer with active region islands after cleaning the wafers and moisture baking them. The wafers deposited with SiO<sub>2</sub> are coated with 3  $\mu$ m positive PR. A dark field mask is used to pattern 1020  $\mu$ m × 290  $\mu$ m trenches, over the active island regions, in the positive PR by UV exposure and developing them in the developer. The developed wafers are than hard baked. Further the exposed SiO<sub>2</sub> in the hard baked wafers is etched out by dry reactive ion etching (DRIE) for an optimized time of 11 minute. This step exposes the active region out of SiO<sub>2</sub>. Hereafter, the wafers are rinsed in acetone to remove the hard baked PR.



Fig. 2.15: The schematic of the dark field mask used to develop the  $SiO_2$  mesa isolation and the developed mesa isolated active layer island.

## 2.2.4.3 Source and Drain Formation

The wafers with the mesa isolated active regions are coated with 3  $\mu$ m positive PR after cleaning and moisture baking. A dark field mask with dimension of the contact overlapping with active region of 500 × 200  $\mu$ m<sup>2</sup> and contact pads of 500 × 500  $\mu$ m<sup>2</sup> is utilized to pattern source and drain trenches in the PR by UV exposure and development. A metal combination of 10 nm Ti, 120 nm Al, 30 nm Ni and 50 nm Au is deposited over the developed wafers after hard baking. These wafers are than placed in Acetone for 15 hour period for lift-off prior to agitating them in ultrasonicator.



Fig. 2.16: The schematic of the dark field source-drain mask and the developed source and drain contacts.

## 2.3 References

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# Chapter 3

# Analytical Modelling for Estimation of 2DEG Density in MgZnO/CdZnO Heterostructures

# **3.1 Introduction**

Zinc oxide (ZnO) has emerged as an attractive option for optoelectronics, sensors and actuators, owing to higher exciton binding energy (60 meV) and large direct energy band gap (3.37 eV) [1-3]. ZnO has a lower growth temperature along with the availability of large area ZnO substrates at relatively low cost [4, 5]. ZnO is also being explored as a viable option for heterostructure field effect transistor (HFET) application due to strong polarization fields in MgZnO/ZnO heterostructure [6, 7] which has shown to induce high two-dimensional electron gas (2DEG) sheet density  $(n_s)$  (~ 10<sup>13</sup> cm<sup>-2</sup>) at room temperature by Tampo *et al.* [7] at Mg composition as high as 0.6 in barrier layer MgZnO, which is difficult to fabricate without the occurrence of phase separation [8-10]. Also, for Mg composition of 0.37 in barrier layer, 2DEG density saturates in  $10^{12}$  order for increasing barrier layer thickness. This implies that for lower Mg composition in barrier layer, 2DEG density of 10<sup>13</sup> order is very difficult to achieve in MgZnO/ZnO heterostructure. Benharrats et al. have shown that 2DEG can be increased further with the use of CdZnO/ZnO heterostructure [11]. Although the use of CdZnO/ZnO heterostructure is beneficial for enhancing 2DEG density compared to that in MgZnO/ZnO, the main drawback of either structure is that the polarization in ZnO buffer does not change significantly. Therefore, any improvement in 2DEG density is solely governed by the change in the polarization in barrier layer. A possible option to circumvent this limitation is to alloy Cd in the buffer layer which would result in MgZnO/CdZnO heterostructure, instead of MgZnO/ZnO or CdZnO/ZnO.

In this work a physics based theoretical estimation shows that the use of MgZnO/CdZnO heterostructure would result in high 2DEG density (>  $10^{13}$ 

cm<sup>-2</sup>), for lower Mg composition in barrier layer ( $\leq 0.3$ ). This is due to high degree of polarization in MgZnO/CdZnO heterostructure which effectively result in upto 25 times enhanced 2DEG density, for 0.1 Mg composition in barrier layer and 30 nm barrier layer thickness, as compared to that in MgZnO/ZnO. Also, as the 2DEG density saturates at lower barrier layer thickness in MgZnO/CdZnO, even for 0.15 Mg composition in barrier layer, low barrier layer thickness (< 15 nm) can be utilized to achieve very high 2DEG density. Good quality MgZnO/CdZnO and ZnO/CdZnO junctions fully compatible with the fabrication process have been demonstrated for opto-electronics application, such as light emitting diodes [12-14].

## **3.2 2DEG Density Model Development**

In this work, we investigate the effect of alloying Cd in ZnO buffer layer on 2DEG density in structures I and II, as shown in Fig. 3.1(a) - (b), through a physics-based analytical model. Structure I in Fig. 1(a) comprises of ZnO cap layer ( $t_2$ ), barrier layer Mg<sub>x</sub>Zn<sub>1-x</sub>O ( $t_1$ ) and a buffer layer Cd<sub>y</sub>Zn<sub>1-y</sub>O. Fig. 1(b) represents heterostructure without a cap layer (structure II). The energy band diagram of structure I is shown in Fig. 3.1(a).



Fig. 3.1. (a) Schematic diagram of MgxZn1-xO/CdyZn1-yO structure I with ZnO Cap Layer and corresponding energy band diagram, showing potential offset ( $\Delta V$ ) and electric-field ( $\xi$ ) in each layer and conduction band offset at each interface ( $\Delta E_c$ ). (b) Schematic diagram of bilayer heterostructure, structure II.

To obtain an analytical model for 2DEG sheet charge density, selfconsistent Poisson's equation is solved at each interface of structure I. The electric field ( $\xi_1$ ) in barrier layer is related to electric field ( $\xi_2$ ) in cap layer to satisfy the dielectric boundary condition, and is given as

$$\xi_1 = \xi_2 + \frac{q\sigma_{net_2}}{\epsilon} \tag{1}$$

where,  $\sigma_{net_2}(=\sigma_3-\sigma_2)$  is the net polarization sheet charge densities at ZnO/Mg<sub>x</sub>Zn<sub>1-x</sub>O interface,  $\sigma_2$  and  $\sigma_3$  are the net polarization charge in barrier and cap layer, respectively, q is the charge of electron and  $\epsilon$  is the permittivity of all layers, which has been considered constant for the simplification of the model. Net polarization charge in barrier and cap layer is comprised of spontaneous ( $P_{sp}$ ) and piezoelectric ( $P_{zp}$ ) components. Here, the piezoelectric component in barrier layer is calculated as [15]:

$$P_{zp} = 2\left(\frac{a_s - a_0}{a_0}\right) \left(E_{31} - \frac{E_{33}C_{13}}{C_{33}}\right)$$
(2)

where,  $a_s$  and  $a_0$  are the *a*-lattice constants of the buffer (or substrate) layer and the barrier (or deposited) layer, respectively,  $E_{31}$  (- 0.55 - 0.23*x*), and  $E_{33}$  (1.24 - 1.10*x*) are the Piezoelectric coefficients and  $C_{13}$  (84 + 4*x*), and  $C_{33}$  (176 - 9*x* + 55*x*<sup>2</sup>) are the Elastic stiffness coefficients of the Mg<sub>x</sub>Zn<sub>1-x</sub>O barrier layer [16]. This P<sub>zp</sub> component is than added to the spontaneous polarization (P<sub>sp</sub>) of barrier layer to give total polarization of the barrier layer. Further, from the energy band diagram, electric field ( $\xi_1$ ) can also be expressed as

$$\xi_1 = \frac{\phi_b - \xi_2 t_2 + \Delta E_{C,net} + E_f}{t_1}$$
(3)

where,  $\phi_b$  is the bare surface barrier height,  $E_f$  is the Fermi energy level with respect to the bottom of the conduction band at the barrier-buffer interface and  $\Delta E_{C,net} (= \Delta E_{C,2} - \Delta E_{C,1})$  is the net conduction band offset,  $\Delta E_{C,2}$  and  $\Delta E_{C,1}$  are conduction band offsets at cap-barrier, and barrier-buffer interface, respectively. Conduction band offset at either interface is maintained at 0.9 times the difference of band gaps ( $\Delta E_g$ ) [5, 17]. Also, as the thickness of net charge developed at barrier-buffer interface is very small compared to the cross sectional area of the interface, the electric field at barrier-buffer interface ( $\xi_1$ ) is given as

$$\xi_1 = \frac{qn_s - q\sigma_{net_1}}{\epsilon} \tag{4}$$

where,  $\sigma_{net_1} = \sigma_2 - \sigma_1$  is the net polarization charge difference at barrierbuffer interface and  $\sigma_1$  is the polarization charge density in buffer layer. Solving (3) and (4),  $n_s$  can be obtained as

$$n_{s} = \frac{\epsilon}{q(t_{1}+t_{2})} \Big[ V_{g} - \phi_{b} - \Delta E_{C,net} - E_{f} \\ - \frac{q}{\epsilon} \Big( \sigma_{net_{2}} t_{2} + \sigma_{net_{1}} (t_{1}+t_{2}) \Big) \Big]$$
(5)

where,  $V_g$  is the gate voltage. Equation (5) can be reduced to a more compact expression as

$$n_s = \frac{\epsilon}{qt} \left[ V_g - V_{OFF} - E_f \right] \tag{6}$$

where,  $t (= t_1 + t_2)$  is the total thickness of layers over buffer layer.  $V_{OFF}$  is the threshold voltage and is given as

$$V_{OFF} = \phi_b + \Delta E_{C,net} + \frac{q}{\epsilon} \Big( \sigma_{net_2}(t_2) + \sigma_{net_1}(t_1 + t_2) \Big)$$
(7)

The solution of Schrodinger's equation for a triangular potential well gives  $n_s$  as [18]
$$n_s = DV_t \ln\left[exp\left(\frac{E_f - E_0}{V_t}\right) + 1\right]$$
(8)

where  $D = 1.17 \times 10^{18} \text{ m}^{-2} \text{V}^{-1}$  is the two dimensional density of states [18] and  $V_t$  (= kT / q) is the thermal voltage where k is Boltzmann's constant, and T is absolute temperature.  $E_0$  is the position of first sub-band in the triangular potential well. Solving (6) and (8) for all cases of  $V_g$ ,  $n_s$  is given as [19]

$$n_{s} = \frac{C_{g}V_{g0}}{q} \frac{V_{g0} + V_{t} \left[1 - \ln(\beta V_{gon})\right] - \frac{\gamma_{0}}{3} \left(\frac{C_{g}V_{g0}}{q}\right)^{2/3}}{V_{g0} \left(1 + \frac{V_{t}}{V_{god}}\right) + \frac{2\gamma_{0}}{3} \left(\frac{C_{g}V_{g0}}{q}\right)^{2/3}}$$
(9)

where  $C_g = \epsilon / (t_1 + t_2)$ ,  $\beta = C_g / (qDV_t)$ ,  $V_{g0} = V_g - V_{OFF}$ , and  $V_{gon}$  and  $V_{god}$ are functions of  $V_{go}$  given by the interpolation expression [19]

$$V_{g0x} = V_{g0} \alpha_x / \sqrt{V_{g0}^2 + \alpha_x^2}$$
(10)

where  $\alpha_n = e / \beta$ ,  $\alpha_d = 1 / \beta$ , and e is Euler's number. Equation (5) can be reduced for a more simplified bilayer heterostructure i.e. structure II by substituting  $t_2$  and  $\Delta E_{C,2}$  as zero. Accordingly,  $V_{OFF}$  in (5) and (6) will be modified for a bilayer structure. The  $V_{OFF}$  for structure II when substituted in (9), gives an expression for  $n_s$  in bilayer heterostructure. The model for structure II, when solved for Mg<sub>x</sub>Zn<sub>1-x</sub>O/ZnO heterostructure compares favorably with published experimental results [7], as shown in Fig. 3.2(a). The parameters for Cd<sub>y</sub>Zn<sub>1-y</sub>O are obtained from the linear combination between the parameters of CdO and ZnO [11]. Energy band gap ( $E_g$ ) of Cd<sub>y</sub>Zn<sub>1-y</sub>O can be obtained as  $E_g(y) = 3.37 - 2.28y + 0.95y^2$  [20]. The spontaneous polarization constants for ZnO and CdO used in the calculation are -0.057 [21] and -0.15 C/m<sup>2</sup>[11], respectively, while that for Mg<sub>x</sub>Zn<sub>1-x</sub>O is -0.057–0.066x C/m<sup>2</sup> [21, 22].

#### 3.3 Results and Discussion

Fig. 3.2(a) shows the variation of 2DEG density at barrier-buffer interface in structure II, as shown in Fig. 1(b), with different atomic composition of Mg (*x*) in barrier layer and Cd (*y*) in buffer layer. Substituting *x* (or *y*) = 0, structure II can be reduced into ZnO/Cd<sub>y</sub>Zn<sub>1-y</sub>O (or Mg<sub>x</sub>Zn<sub>1-x</sub>O/ZnO). From Fig. 3.2(a) the following are evident from the graph.



Fig. 3.2 (a) Variation of 2DEG density in  $Mg_xZn_{1-x}O/Cd_yZn_{1-y}O$  with varying atomic composition of Mg(x) in barrier or Cd(y) in buffer. (b) Change in different polarization components in barrier layer with different atomic composition of x and y. (c) Effect of varying barrier layer thickness for structure I and II at different Cd composition (y) in buffer on  $n_s$ . (d) Effect of addition of a cap layer for varying Mg composition in barrier layer for structure I and II.

(i) Cadmium composition of 0.15 in buffer layer increases 2DEG density 5 times as compared to that in Mg<sub>x</sub>Zn<sub>1-x</sub>O/ZnO at x = 0.3. This is attributed to introduction of more electronegative Cd (1.7) [23] in ZnO, which leads to lesser attraction of electron cloud by oxygen atoms in sp3 covalent bonds

and result in decreased spontaneous polarization in buffer layer. Also, the lattice constant of Cd<sub>0.15</sub>Zn<sub>0.85</sub>O (a = 3.314 Å) [11, 24] is larger than that of Mg<sub>x</sub>Zn<sub>1-x</sub>O (a = 3.248 Å (at x = 0.05) to 3.261 Å (at x = 0.3)) [24, 25]. This implies that the piezoelectric polarization in barrier layer is tensile, and more importantly, adds up favorably with spontaneous polarization of barrier layer, which increases  $\sigma_{net_1}$ . As  $n_s$  has direct proportionality with  $\sigma_{net_1}$ , 2DEG density also increases with addition of Cd in buffer layer.

(ii) 2DEG density for Mg<sub>0.15</sub>Zn<sub>0.85</sub>O/Cd<sub>y</sub>Zn<sub>1-y</sub>O is nearly half of that for Mg<sub>x</sub>Zn<sub>1-x</sub>O/Cd<sub>0.15</sub>Zn<sub>0.85</sub>O at *y* and *x* being 0.05 in respective structures. This is because, 0.05 Cd composition in buffer layer will have higher spontaneous polarization than 0.15 Cd, as higher content of Cd will induce a reduction of spontaneous polarization. Also, the lattice constant of buffer CdZnO will be smaller (a = 3.271 Å) in former case than for latter (a = 3.314 Å) resulting in lesser piezoelectric induced strain in barrier layer, and hence, lesser polarization difference at the barrier-buffer interface.

(iii) The variation in Mg composition (x) in barrier layer seems to have negligible effect on 2DEG density as compared to the variation of Cd composition (y) in buffer layer. As for y = 0.3,  $n_s$  is nearly twice that of  $Mg_xZn_{1-x}O/Cd_{0.15}Zn_{0.85}O$  at x = 0.3. The reason for this observation is the variation in spontaneous and piezoelectric components with varying x and y, as shown in Fig. 3.2(b). As the difference between lattice constant (a) of  $Mg_xZn_{1-x}O$  and  $Cd_{0.15}Zn_{0.85}O$  decreases for increasing x, the tensile strain in barrier layer decreases, and thus,  $P_{zp}$  decreases with x in barrier layer. The net polarization in barrier layer remains nearly constant as  $P_{sp}$  in barrier layer increases with x and  $P_{zp}$  decreases with x, as shown in Fig. 3.2(b). As buffer layer Cd composition remains constant, net polarization in buffer layer is constant, and hence,  $n_s$  remains nearly constant in Mg<sub>x</sub>Zn<sub>1-</sub>  $_xO/Cd_{0.15}Zn_{0.85}O$ , as shown in Fig. 3.2(a). An increase of  $n_s$  in  $Mg_{0.15}Zn_{0.85}O/Cd_yZn_{1-y}O$  with increase in y, is due to linear increase in lattice constant of Cd<sub>y</sub>Zn<sub>1-y</sub>O (a = 3.271 Å (at y = 0.05) to 3.378 Å (at y =0.3)) and decrease in  $P_{sp}$  in buffer layer. This increases the tensile  $P_{zp}$  in

barrier layer and  $\sigma_{net_1}$ , as shown in Fig. 3.2(b). Thus,  $n_s$  increases linearly with increasing Cd composition in buffer layer.

It is evident from Fig. 3.2(a) that for a 30 nm barrier layer Mg<sub>0.10</sub>Zn<sub>0.9</sub>-<sub>0</sub>O/Cd<sub>0.15</sub>Zn<sub>0.85</sub>O and Mg<sub>0.15</sub>Zn<sub>0.85</sub>O/Cd<sub>0.10</sub>Zn<sub>0.90</sub>O results in ~25 times and ~20 times higher  $n_s$  than that in Mg<sub>0.10</sub>Zn<sub>0.90</sub>O/ZnO with same barrier layer thickness. Also, for barrier layer Mg composition as low as 0.05, MgZnO/CdZnO heterostructure with 0.15 Cd in buffer layer yield 2 × 10<sup>13</sup> cm<sup>-2</sup> 2DEG density, while MgZnO/ZnO heterostructure for same Mg composition and barrier layer thickness induces no 2DEG density. Also, Mg<sub>0.15</sub>Zn<sub>0.85</sub>O/Cd<sub>0.30</sub>Zn<sub>0.70</sub>O and Mg<sub>0.30</sub>Zn<sub>0.70</sub>O/Cd<sub>0.15</sub>Zn<sub>0.85</sub>O has ~9 times and ~5 times enhanced  $n_s$  over Mg<sub>0.30</sub>Zn<sub>0.70</sub>O/ZnO. As the MgZnO shows phase segregation above 0.35 Mg [9] and CdZnO shows preferential wurtzite phase below 0.30 Cd [26], lower alloy composition in buffer and barrier layer ensures better crystallinity of both layers.

Fig. 3.2(c) shows the variation of  $n_s$  with increasing barrier layer thickness for structure I and II. The results for the variation of  $n_s$  with barrier layer thickness of structure II are in good agreement with published experimental results [17] for MgZnO/ZnO heterostructure. It is observed that an addition of 0.05 Cd in buffer ZnO layer enhances  $n_s$  by ~6 times and 0.15 Cd improves  $n_s$  by ~13 times as compared to that for Mg<sub>0.15</sub>Zn<sub>0.85</sub>O/ZnO with 30 nm barrier layer thickness. This shows alloying of buffer ZnO with Cd can give rise to significantly enhanced 2DEG density. As can be seen in the graph,  $n_s$  increases for lower barrier layer thickness and saturates for higher thickness for all heterostructures. For structure II, a well-known reason in literature for this observation is the presence of surface donor-like states [27]. As the surface donor-like states provide the electrons in the conduction band of the barrier layer, the electric field  $(\xi_1)$  created by the net polarization difference  $\sigma_{net_1}$ , as given in (4), sweeps them into buffer layer, where they accumulate under columbic attraction of net positive polarization difference  $\sigma_{net_1}$  and bend the buffer conduction band below fermi energy level at barrier-buffer interface, and hence, forms a 2DEG. As  $n_s$  tends to approach  $\sigma_{net_1}[17]$ , electric field  $(\xi_1)$  reduces and tends toward zero, and thus,  $n_s$  approaches saturation for higher barrier layer thickness. It is worth noticing that initially electric field  $(\xi_1)$  is directly proportional to  $\sigma_{net_1}$ . Hence, the  $n_s$  for lower thickness of barrier layer is dependent on  $\sigma_{net_1}$ , as a stronger  $\xi_1$  can attract electrons from shallow donor states and thus,  $\sigma_{net_1}$  dictates the minimum thickness of barrier layer to form 2DEG.



Fig. 3.3. 2DEG density is plotted against VOFF for varying barrier layer alloy composition x in  $Mg_xZn_{1-x}O/Cd_yZn_{1-y}O$  at y=0 (red color) and 0.05 (blue color), with 10 nm cap layer (structure I) depicted by filled symbols and without cap layer (structure II) denoted by empty symbols and is compared to bilayer  $Al_xGa_{1-x}N/GaN$  (black color). All structures are simulated for x varying from 0.01 to 0.3, and the values for  $n_s$  obtained for every x in every structure is plotted against the corresponding values of obtained V<sub>OFF</sub>.

In Fig. 3.2(c), it is also observed that an addition of a 10 nm ZnO cap layer reduces  $n_s$ . An addition of cap layer, with net polarization  $\sigma_3$  smaller than net polarization of barrier layer  $\sigma_2$ , induces a net negative polarization difference at cap-barrier interface ( $\sigma_{net_2}$ ). This reduces the electric field  $\xi_1$  in barrier layer [27], which in turn affects the threshold thickness of barrier layer and also the saturation of  $n_s$  will be attained at lower values. It is also

noticed that even with the addition of 10 nm cap layer, addition of 0.05 and 0.15 Cd in buffer ZnO increases  $n_s$  by ~4 and ~9 times, respectively, compared to that in same barrier layer thickness and Mg composition MgZnO/ZnO heterostructure. 2DEG density in Mg0.15Zn0.85O/CdyZn1-yO for y = 0.05 and 0.15 saturates at ~9 × 10<sup>12</sup> cm<sup>-2</sup> and ~2 × 10<sup>13</sup> cm<sup>-2</sup>, respectively, for 15 nm of barrier layer thickness. For same Mg composition in barrier layer and barrier layer thickness, MgZnO/ZnO yields  $n_s \sim 1 \times 10^{12}$  cm<sup>-2</sup>, as shown in Fig. 2(c). This suggests that a considerably lower barrier layer thickness can be utilized along with lower Mg composition in barrier layer to achieve very high 2DEG density by alloying Cd in buffer layer ZnO. Alternately, it seems very difficult to increase barrier layer thickness and Mg composition of MgZnO/ZnO to achieve comparable levels of  $n_s$  as exhibited by MgZnO/CdZnO heterostructure. Fig. 3.2(d) shows the effect of addition of a cap layer for varying Mg composition (x) in a 30 nm barrier layer for all heterostructures. It is observed that addition of cap layer reduces  $n_s$  for all heterostructure combinations. This plot suggests that ZnO/Mg<sub>0.3</sub>Zn<sub>0.7</sub>O/Cd<sub>0.15</sub>Zn<sub>0.85</sub>O gives ~3 times and ZnO/Mg<sub>0.3</sub>Zn<sub>0.7</sub>O/Cd<sub>0.05</sub>Zn<sub>0.95</sub>O provides ~2 times higher  $n_s$ than that for  $Mg_{0.3}Zn_{0.7}O/ZnO$ .

Fig. 3.3 shows the dependence of 2DEG density on  $V_{OFF}$  in Mg<sub>x</sub>Zn<sub>1</sub>- $_xO/Cd_yZn_{1-y}O$  (at y = 0 and 0.05), for x varying from 0.01 to 0.3 and 15 nm barrier layer thickness, with and without ZnO cap layer. The graph also shows 2DEG density in Al<sub>x</sub>Ga<sub>1-x</sub>N/GaN [28] for the same variation of x and equal barrier layer thickness. This graph can be used to obtain a trade-off between  $n_{\rm s}$  and  $V_{\rm OFF}$ , by adjusting the barrier layer alloy composition x. It is noteworthy that for same barrier layer thickness and variation in barrier alloy composition, MgZnO/ZnO can achieve a higher 2DEG density compared to AlGaN/GaN, with a marginal increase in VOFF. Alloying Cd in buffer ZnO increases 2DEG density 3.5 times for Mg0.3Zn0.7O/Cd0.05Zn0.95O compared to Al0.3Ga0.7N/GaN, in practical VoFF limits [29]. Also, an addition of 10 nm ZnO cap layer achieves 2 times higher  $n_s$  than Al<sub>0.3</sub>Ga<sub>0.7</sub>N/GaN for Mg<sub>0.3</sub>Zn<sub>0.7</sub>O/Cd<sub>0.05</sub>Zn<sub>0.95</sub>O and 1.5 times higher than  $Mg_{0.3}Zn_{0.7}O/ZnO$ .

An electrostatically stable ZnO surface is necessary for predicting 2DEG density in ZnO based heterostructures. The clear understanding of physical mechanisms defining effects of various external growth parameters such as oxygen partial pressure during growth [30], and hydrogen adsorbed at the surface of ZnO [31], on conductivity of ZnO, are still ambiguous [32, 33] and very complex to model analytically. In their work, Delagebeaudeuf et al., [18] made provision of interface charge  $(Q_i)$  term in the equation of 2DEG density, to take into account of such effects which might be formed due to the different growth parameters preventing the formation of perfectly electrostatically stable surface. These interface charges  $(Q_i)$  turned out to be negligible for the present model when compared with experimental results of Tampo et al., [7], wherein MgZnO/ZnO heterostructure was fabricated using Molecular Beam Epitaxy (MBE). It is important to note that Tampo et al., did not report any adverse observation related to the electrostatic stability of the surface in the experimental data for the 2DEG sheet density [7]. We have carried out a comparison study with electrostatically stable ZnO surface for all heterostructures. Thus, the manuscript stresses the need to consider buffer layer engineering as an important factor to improve the 2DEG density.

In general, the value of 2DEG mobility depends on factors governing the growth conditions, and as reported in the literature, growth with Molecular Beam Epitaxy (MBE) has shown higher 2DEG mobility values [7] of 310 cm<sup>2</sup>/Vsec in comparison to 40 cm<sup>2</sup>/Vsec when grown by rf sputtering [34]. In contrast, the value of 2DEG sheet charge density by rf sputtering is nearly an order higher (~10<sup>14</sup> cm<sup>-2</sup>) [34] than that achieved by MBE. The scattering mechanisms governing the 2DEG mobility are acoustic deformation potential, piezoelectric, polar optic phonon, alloy disorder, interface roughness, dislocation and remote modulation doping [35]. Although, the development of an analytical model for various mobility components as mentioned above is beyond the scope of this work, it is expected that a higher 2DEG concentration along with a higher electron effective mass (*m*\*) in MgZnO/CdZnO heterostructure is expected to yield lower mobility values in comparison to MgZnO/ZnO heterostructure. The

main thrust of this work is to consider buffer layer engineering as a viable option for increasing the 2DEG sheet charge density in ZnO heterostructures.

# **3.4 Conclusion**

An in-depth analysis of modulating the net polarization by buffer layer engineering has been presented in this work. The work shows the need to efficiently utilize the properties of buffer CdZnO layer to enhance 2DEG density in MgZnO/CdZnO heterostructure, which seems to be limited when focusing only on the barrier layer. By alloying the buffer ZnO with Cd, the polarization of buffer layer is modulated, which effectively enhances the net polarization difference at barrier-buffer interface. Also, addition of Cd in buffer increases the buffer lattice constant such that the compressive strain in barrier layer MgZnO prior to addition of Cd in buffer becomes tensile, thus increasing the net polarization in barrier layer. Both these effects favorably add-up to a significant enhancement in 2DEG density, for same compositional variations in barrier MgZnO layer.

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# **Chapter 4**

# Experimental Confirmation of 2DEG in MgZnO/CdZnO Heterostructure

# **4.1 Introduction**

In our previous work [1], we have theoretically estimated higher  $n_s$  at lower Mg compositions in barrier layer, for epitaxially grown MgZnO/CdZnO as compared to that in MgZnO/ZnO. This chapter presents an experimental confirmation of the theoretically expected enhancement in 2DEG density (n<sub>s</sub>) by replacing ZnO buffer layer by CdZnO in MgZnO/ZnO heterostructure, at lower Mg compositions ( $x \le 0.15$ ) in barrier layer. As the method of growth in this work is DIBS the increase in  $n_s$  is compared to experimentally available  $n_s$  in sputtered MgZnO/ZnO heterostructures. A probable reason for enhanced  $n_s$  in sputtered heterostructures has been assumed to be the high carrier densities in individual barrier and buffer layers, due to defect prone growth in sputtering. Therefore, the individual MgZnO and CdZnO layers are probed for their carrier densities. The trend of carrier concentration with varying Mg composition in separately grown MgZnO is completely opposite to that observed in MgZnO/CdZnO heterostructure, which suggests a probable charge carrier confinement at barrier-buffer interface. The depth dependent carrier profile measured by capacitance-voltage (C-V) measurement, confirms confined carrier density at the hetero-interface. The temperature-dependent Hall measurement further establishes that the enhanced carrier concentration in the as-grown heterostructure is not due to the thermally excited bulk electrons as  $n_s$ remains nearly constant with varying measurement temperature from 5 to 300 K. The resultant  $n_s$  in the as-grown heterostructure, is one of the highest  $n_{\rm s}$  reported in ZnO [2], GaN [3] or GaAs [4] based heterostructures and it possesses potential for applications in HFETs, thin film transistors (TFTs) and transparent thin film transistors (TTFTs).

#### **4.2 Experimental Details**

A 250 nm Cd<sub>0.15</sub>Zn<sub>0.85</sub>O buffer layer, thickness measured by average deposition rate, is deposited onto p-Si (100) substrate by DIBS system at Ar: $O_2 = 2:3$  and 300 °C, with beam voltage of 800 V, ion beam power of 44 W, and  $2.43 \times 10^{-4}$  mbar working pressure inside the DIBS chamber. The 30 nm Mg<sub>x</sub>Zn<sub>1-x</sub>O barrier layer (x = 0.05, 0.15, 0.2, 0.3) is deposited on top of Cd<sub>0.15</sub>Zn<sub>0.85</sub>O buffer under same growth conditions. The barrier and buffer layers are deposited using commercially available MgZnO and CdZnO sputtering targets [5]. Prior to film deposition, in order to remove organic contaminants and native oxide, Si substrate is thoroughly cleaned, details of which are described in our previous work [6]. To perform Hall measurement, four In metal ohmic contacts, in Van der Pauw configuration, are soldered at 400 °C on the top of MgZnO. To perform C-V characterization, a 100-nm thick and 0.5 mm<sup>2</sup> Pt layer is grown on 30 nm thick MgZnO layer (x = 0.3) in bilayer heterostructure, by sputtering a Pt target at room temperature using RF-magnetron sputtering and an In metal ohmic contact is soldered at 400 °C at a lateral distance of 1 mm.

#### 4.3 Results and Discussion

Fig. 4.1(a) shows X-ray diffraction (XRD) patterns of Mg<sub>x</sub>Zn<sub>1-x</sub>O and Cd<sub>0.15</sub>Zn<sub>0.85</sub>O samples, as obtained using Rigaku Smart Lab system with Cu-K $\alpha$  radiation (1.54 Å). The XRD results suggest the wurtzite structure formation in all grown films that are highly oriented in *c*-axis crystallographic direction on *p*-Si (100) substrate. It is observed that, in 250 nm thick Mg<sub>x</sub>Zn<sub>1-x</sub>O, the (002) diffraction peaks are shifted towards higher 2- $\theta$  compared to the diffraction peak of 250 nm thick Cd<sub>0.15</sub>Zn<sub>0.85</sub>O. A probable cause for this effect is a smaller lattice constant of Mg<sub>x</sub>Zn<sub>1-x</sub>O [7] due to smaller Mg<sup>2+</sup> ionic radii (0.57 Å) [8], as compared to that for Cd<sub>0.15</sub>Zn<sub>0.85</sub>O [7, 9] with Cd<sup>2+</sup> ionic radii of 0.78 Å [8]. In addition, with Mg content increase ( $\geq$  0.20) in Mg<sub>x</sub>Zn<sub>1-x</sub>O, the intensity increases for secondary wurtzite phase (100) diffraction peak.



Fig. 4.1: (a) XRD patterns for separately grown  $Mg_xZn_{1-x}O$  and  $Cd_{0.15}Zn_{0.85}O$ . (b) Sheet carrier density in DIBS grown  $Mg_xZn_{1-x}O$  against atomic compositions as determined by EDX. Inset show schematic of films on Si substrate. (c) Tauc's plot from transmission coefficients of  $Mg_xZn_{1-x}O$  showing corresponding energy band gap.

Fig. 4.1(b) shows  $n_s$  evaluated from Hall measurement system in Van der Pauw configuration, utilizing Keithley source meter (model 2612A), in 250 nm thick Mg<sub>x</sub>Zn<sub>1-x</sub>O for different Mg contents. The possible composition error ranges, as shown in fig. 1(b), are the average composition scattering, as evaluated by energy dispersive X-ray spectroscopy (EDX, Oxford Instruments). The average deviation in composition is assessed from multiple measurements on different locations of the same sample and different samples with same chemical composition and thickness grown under similar conditions. Similarly, y-error bar depicts the average deviation in  $n_s$ , as provided by Hall measurements. The fitting curve represents the trend of mean  $n_s$  at mean composition values in Mg<sub>x</sub>Zn<sub>1-x</sub>O films. It is observed that, with Mg content increasing,  $n_s$  decreases from ~2×10<sup>13</sup> to ~6×10<sup>11</sup> cm<sup>-2</sup>. This is consistent with the reported trend in  $n_s$ , as found in the literature [10]. The mean value of  $n_s$  for 250 nm thick  $Cd_{0.15}Zn_{0.85}O$  is  $6.12 \times 10^{12}$  cm<sup>-2</sup> (not shown). A conductive *p*-Si is utilized as the substrate for the Hall measurements due to the formation of depletion region between *n*-CdZnO and *p*-Si with cut-in bias of 2-3 V, while all read back voltages in Hall measurement remain within 10-15 mV.

Fig. 4.1(c) shows the Tauc's plot of  $Mg_xZn_{1-x}O$  films grown on glass substrates. The red shift in energy band gap ( $E_g$ ) with increasing Mg content suggests increasing  $E_g$  in  $Mg_xZn_{1-x}O$  films. The red shift in  $E_g$  supports the  $n_s$  trend for  $Mg_xZn_{1-x}O$  with increasing x value. As  $E_g$  increases, the number of free electrons available in conduction band reduces when measured at the same temperature.



Fig. 4.2: (a) Sheet carrier density in DIBS grown  $Mg_xZn_{1-x}O/Cd_{0.15}Zn_{0.85}O$ heterostructure. Inset shows the schematic of bilayer heterostructure used for Hall measurement. (b) C-V determined carrier density in the sample A and B of  $Mg_{0.3}Zn_{0.7}O/Cd_{0.15}Zn_{0.85}O$  for 30 nm barrier layer thickness at 300 K. Inset shows the schematic of bilayer heterostructure used for C-V

measurement. (c) Temperature dependent Hall measurement of  $Mg_{0.3}Zn_{0.7}O/Cd_{0.15}Zn_{0.85}O$  with temperature varying from 5 to 300 K. (d) Comparative plots of  $n_s$  vs Mg composition in ZnO based bilayer heterostructures grown by MBE, RF-sputtering, DIBS and theoretically predicted  $n_s$  in MgZnO/Cd\_{0.15}Zn\_{0.85}O.

Fig. 4.2(a) shows  $n_s$  measured in as-grown Mg<sub>x</sub>Zn<sub>1-x</sub>O/Cd<sub>0.15</sub>Zn<sub>0.85</sub>O heterostructures. Here, the mean  $n_s$  values increase with increasing Mg content in barrier layer, from 2.4×10<sup>14</sup> at x=0.05 to 2.8×10<sup>14</sup> cm<sup>-2</sup> at x=0.30. This trend is in contrast with the trend of measured  $n_s$  in 250 nm Mg<sub>x</sub>Zn<sub>1-x</sub>O with increasing Mg content. In addition, the  $n_s$  observed in heterostructures is ~10<sup>1</sup>-10<sup>3</sup> orders higher than that in the individual Mg<sub>x</sub>Zn<sub>1-x</sub>O and Cd<sub>0.15</sub>Zn<sub>0.85</sub>O films. It is noteworthy that the buffer layer is grown on a single 3" *p*-Si (100) wafer at constant growth condition. This reduces the probability of variation in  $n_s$  in buffer layer. Even if a deviation in  $n_s$  at various spatial locations is considered, ~10<sup>2</sup> order of increase in  $n_s$  cannot be justified, especially when two samples of 10 × 10 mm<sup>2</sup> area from different spatial location on the buffer grown wafer are probed and both have resulted in coherent values of  $n_s$ .

Furthermore, the addition of Mg<sub>x</sub>Zn<sub>1-x</sub>O barrier layer should have had a negative effect on the values of  $n_s$  in the heterostructure as the value of  $n_s$  in Mg<sub>x</sub>Zn<sub>1-x</sub>O films decreased by ~10<sup>2</sup> orders with increasing *x*. Therefore, a probable explanation for this trend observed in Fig. 4.2(a) is the carrier confinement in two-dimensional (2-D) potential well at barrier-buffer heterointerface, along the lines of MgZnO/ZnO system [2, 11]. A linear increase in the  $n_s$  values with increasing Mg contents can be attributed to enhancement in spontaneous polarization in barrier layer.

To probe carrier concentration at various depths from surface, the *C-V* measurements are performed with a Pt Schottky contact and an In contact. The carrier density at various depths from the barrier layer surface, as calculated from *C-V* measurements at 300 K, in two similar samples (A and B) of Mg<sub>0.3</sub>Zn<sub>0.7</sub>O/Cd<sub>0.15</sub>Zn<sub>0.85</sub>O, grown in same conditions, with 30 nm barrier layer is shown in Fig. 2(b). It is observed that at ~30 nm from the

barrier layer surface the carrier density rises to  $\sim 10^{20}$  cm<sup>-3</sup> and then drastically decreases to  $\sim 10^{18}$  cm<sup>-3</sup>. Similar observation have been reported in MgZnO/ZnO [11] heterostructures to prove confinement of carriers at barrier-buffer heterointerface.

Fig. 4.2(c) shows temperature-dependent  $n_s$  and mobility of Mg<sub>0.3</sub>Zn<sub>0.7</sub>O/Cd<sub>0.15</sub>Zn<sub>0.85</sub>O, measured by temperature-dependent Hall measurement. The y-error bars represents measurement deviations. Insignificant variation of  $n_s$  with temperature, for 5 to 300 K, indicates that the dominant carriers are not resulting from the thermal activation of bulk and confirms presence of quantum confined carriers. In addition, as-grown sample shows a temperature independent carrier mobility, which is related to surface roughness scattering of quantum confined carriers at heterointerface [2]. The surface roughness values as measured at different spatial locations by ellipsometry, of CdZnO buffer layer is ~ 30-40 nm. The improvement of the surface smoothness would be essential to achieve higher mobility.

An order of magnitude lower value of carrier mobility in MgZnO/CdZnO compared to that in MgZnO/ZnO, in general, depends on various scattering mechanisms governing the mobility. These are acoustic deformation potential, piezoelectric, polar optic phonon, alloy disorder, interface roughness, dislocation, and remote modulation doping [11]. All scattering mechanisms have a non-linear and differential relationship with confined carrier density, thus, an extensive study of all scattering components will be necessary to assess which scattering components dominate the carrier mobility in the grown heterostructure, which is, beyond the scope of the presented study.

However, from the equations presented in [12], an approximation can be made about the significance of each scattering component. Since, Interface roughness and dislocation scattering are majorly governed by the growth parameters, hence, the temperature independent nature of mobility is almost similar in MgZnO/ZnO [13] and MgZnO/CdZnO, both grown by sputtering under same growth conditions. The piezoelectric scattering will

change as piezoelectric polarization experienced by MgZnO barrier layer significantly changes with buffer layer changing from ZnO to CdZnO [1]. As the value of  $n_s$  is enhanced in MgZnO/CdZnO than that in MgZnO/ZnO, and the enhanced carriers are probably the confined carriers, the optical phonon scattering component will also change. As a ternary CdZnO is replacing the buffer layer ZnO, it is expected to increase alloy disorder and hence increase the alloy disorder scattering. Therefore, the piezoelectric, optical phonon, and alloy disorder scattering could be the probable reasons for an order of magnitude lower mobility in MgZnO/CdZnO compared to that in sputtered MgZnO/ZnO.

Fig. 4.2(d) shows theoretically predicted variation of  $n_s$  in epitaxial MgZnO/Cd<sub>0.15</sub>Zn<sub>0.85</sub>O and epitaxial MgZnO/ZnO with Mg composition, as per the analytical model presented in [1]. Here, the term epitaxial represent that the heterostructure considered for analytical estimation was defect-free and its estimated  $n_s$  values agreed with the experimental  $n_s$  values of epitaxial grown heterostructure. In addition, it shows  $n_s$  variation in RF-sputtering [2], DIBS-grown [13] MgZnO/ZnO system, and in our present reported work. From the graph, it is observed that the increase in  $n_s$  in MgZnO/Cd<sub>0.15</sub>Zn<sub>0.85</sub>O with Mg composition for both DIBS-grown and theoretically predicted epitaxial is subtle, whereas, the increase in  $n_s$  in MgZnO/ZnO for both sputtering and epitaxial is comparatively significant.

In Fig. 4.2(d), it can be observed that sputtering grown MgZnO/ZnO heterostructures yield consistently an order higher value of  $n_s$  [2, 14] as compared to that in molecular beam epitaxy (MBE) grown heterostructures [11]. As can be seen at x=0.30, the sputtered MgZnO/ZnO heterostructure yields ~20×  $n_s$  compared to that in epitaxially grown heterostructure. A similar one order of magnitude enhancement in  $n_s$  value is reported in case of as-grown MgZnO/Cd<sub>0.15</sub>Zn<sub>0.85</sub>O heterostructure over theoretically predicted  $n_s$  value for epitaxial grown structures. In the literature, this has been attributed to higher defect density resulted from sputtering growth [2]. The attribution, of high  $n_s$  in sputtering grown heterostructure over epitaxial heterostructure, to high defect density is verified by simulation in the work

of Singh *et al.* [15]. In their work [15], the defect prone sputtering growth has been linked to the formation of trap states, which manifest themselves as interface charges responsible for increased  $n_s$  in sputtered heterostructure. Additionally, it is observed that replacing the buffer layer ZnO with Cd<sub>0.15</sub>Zn<sub>0.85</sub>O in the sputtered heterostructure, ~6× and ~3× enhancement in  $n_s$  is reached at x=0.05 and 0.30, respectively. This enhanced  $n_s$  value by alloying CdO in buffer ZnO is attributed to decreased spontaneous polarization of buffer layer and the larger lateral lattice constant (*a*) of Cd<sub>0.15</sub>Zn<sub>0.85</sub>O than Mg<sub>x</sub>Zn<sub>1-x</sub>O (for x = 0.05 - 0.3), increasing the net polarization difference at barrier-buffer interface, thus enhancing confined carrier density [1].

# **4.4 Conclusion**

In conclusion, this work shows that by using CdZnO buffer layer very high  $n_{\rm s}$  (~10<sup>14</sup> cm<sup>-2</sup>) for low Mg compositions ( $x \le 0.15$ ) in barrier layer, can be obtained in an otherwise MgZnO/ZnO heterostructure. Temperature-dependent Hall and *C-V* measurements confirmed the presence of carrier confinement at barrier-buffer interface. Moreover, the achieved  $n_{\rm s}$  in presented heterostructure system is one of the highest reported  $n_{\rm s}$  values in ZnO or GaN based heterostructures. Therefore, DIBS grown CdZnO buffer based heterostructures can have potential applications in HFETs, TFTs, and TTFTs.

# 4.5 References

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# Chapter 5

# Analytical Investigation of Drain Current in Polycrystalline MgZnO/CdZnO HFET

## **5.1 Introduction**

The MgZnO/ZnO (MZO) heterostructure has been successfully utilized to fabricate HFET by Sasa *et al.* using molecular beam epitaxy (MBE) [1] and Cheng *et al.* [2] using radio-frequency (RF) sputtering. In addition, in our previous work [3], we have shown that the dual ion beam sputtering (DIBS)-grown ZnO-based heterostructure with Cd alloyed buffer layer provides significant enhancement (~ 6×) in 2DEG density ( $n_s$ ) as compared to DIBS and radio frequency (RF)-sputtering grown MZO heterostructures. However, no analytical study was found in the literature to estimate the drain current analysis MgZnO/CdZnO (MCO) and MZO-based HFETs grown by growth techniques such as DIBS and other polycrystalline deposition techniques.

In this work, an analytical model has been developed and utilized to comprehensively estimate the drain current performance of MZO-based HFET and the impact of replacing the buffer layer by CdZnO. The model utilizes ionized interface state density ( $Q_i$ ) as an empirical parameter to take into consideration the non-idealities of the heterointerface grown by DIBS and other polycrystalline film deposition techniques [3, 4]. As the role of  $Q_i$  in the formation of 2DEG density in MZO heterostructure has been established in the polycrystalline heterostructures [5], the inclusion of  $Q_i$  for estimation of  $I_d$  performance in MZO-based HFET becomes essential to accurately predict the transfer and output characteristics experimentally reported in the literature [1, 6]. An exhaustive study of the drain current ( $I_d$ ) in MZO and MCO-based HFET is performed, with inclusion of various interrelationships of  $Q_i$  with electron mobility ( $\mu$ ), thickness of barrier layer (d) and Mg content in barrier layer (x).

The results suggest that a linear modulation of  $Q_i$  with respect to applied gate voltage ( $V_g$ ) is essential for achieving acceptable agreement with the experimentally obtained drain current ( $I_d$ ) in MZO HFET, as reported in the literature [6]. Moreover, the results suggest that the consideration of interrelationship of  $Q_i$  with  $\mu$ , d and x, drastically changes the values of  $I_d$ with a constant values of drain voltage ( $V_d$ ) and  $V_g$ , as compared to the corresponding cases in which  $Q_i$  is independent of  $\mu$ , d and x in both MZO and MCO-based HFETs. The developed model and the presented study are significant to analyze and optimize MZO and MCO-based HFETs grown by low-cost, large area electronics compatible polycrystalline growth techniques.

## **5.2 Model Development**

Fig. 5.1(a) shows the schematic of MgZnO/ZnO or MgZnO/CdZnO-based HFET, assuming the channel is confined below the gate contact. The source  $(R_s)$  and drain  $(R_d)$  contact resistances are assumed to be up to the edges of the channel. The developed analytical model utilizes the material-growth non-idealities, in the form of ionized interface states, near the barrier-buffer interface, as shown in Fig. 5.1(b), as an empirical parameter to modify the threshold voltage  $(V_{OFF})$  in the general equation of  $n_s$ , which is given as:

$$n_{\rm s}(x) = \frac{\epsilon}{qd} (V_g - V_{OFF} - V(x) - E_f) \tag{1}$$



*Fig. 5.1: (a) Schematic of device structure. (b) Conduction energy band diagram with the interface non-idealities.* 

where,  $E_f$  is the Fermi energy level with respect to the bottom of the conduction band at the barrier–buffer interface, d is the thickness of barrier layer, q is the electron charge,  $\epsilon$  is the permittivity of MgZnO,  $V_g$  is the gate voltage, V(x) is the applied voltage on  $n_s$  along x-axis. For polycrystalline heterojunction,  $V_{OFF}$  is given by [7, 8]:

$$V_{OFF} = \phi_b + \Delta E_C + \frac{q}{\epsilon} (\sigma_1 d) + \frac{qd}{\epsilon} Q_i$$
(2)

where,  $\phi_b$  (5.81 $x^2$  - 3.12x + 1.12) [18] is the barrier height of Mg<sub>x</sub>Zn<sub>1-x</sub>O barrier layer surface,  $\Delta E_c$  is conduction band offset and is equal to 0.9 times the band gap difference at the heterointerface,  $\sigma_1$  is the net polarization difference at barrier-buffer interface, it is calculated as described in [16, 18], and  $Q_i$  is the ionized interface state density, as can be seen in Fig. 1 (b).

From the work of Dasgupta *et al*, [9]  $E_f$  can be approximated in a polynomial form as:

$$E_f = k_1 + k_2 \sqrt{n_s(x)} + k_3 n_s$$
(3)

where,  $k_1$ ,  $k_2$ , and  $k_3$  are parametric constants. To attain values of  $k_1$ ,  $k_2$ , and  $k_3$  values of  $n_s$  independent of  $E_f$  are derived by (4), [11] at three values of  $V_g$  (-1, 0 and 1 V), for d = 30 nm and Mg content (*x*) of 30 at.%.

$$n_{s} = \frac{C_{g}V_{g0}}{q} \frac{V_{g0} + V_{t} \left[1 - \ln(\beta V_{gon})\right] - \frac{\gamma_{0}}{3} \left(\frac{C_{g}V_{g0}}{q}\right)^{2/3}}{V_{g0} \left(1 + \frac{V_{t}}{V_{god}}\right) + \frac{2\gamma_{0}}{3} \left(\frac{C_{g}V_{g0}}{q}\right)^{2/3}}$$
(4)

where  $C_g = \epsilon/d$ , in which  $\epsilon$  is the permittivity of layers (8.75 $\epsilon_0$ ),  $\beta = C_g / (qDV_t)$ , where,  $D = 1.17 \times 10^{18} \text{ m}^{-2} \text{V}^{-1}$  is the two dimensional density of states [7],  $V_t$  (= kT / q) is the thermal voltage where k is Boltzmann's constant, T is absolute temperature (300 K), q is the electron charge,  $V_{g0} =$ 

 $V_{g}$  -  $V_{OFF}$ , and  $V_{gon}$  and  $V_{god}$  are functions of  $V_{go}$  given by the interpolation expression (5) [10]

$$V_{gox} = V_{g0} \alpha_x / \sqrt{V_{g0}^2 + \alpha_x^2}$$
 (5)

where  $\alpha_n = e / \beta$ ,  $\alpha_d = 1 / \beta$ , and e is Euler's number. The evaluated values for  $n_s$  at  $V_g$  (= -1, 0, 1 V) are utilized to obtain the corresponding values of  $E_{f.}$  ( $E_f = V_{g0} - \frac{n_s q d}{\epsilon}$ ), where,  $V_{g0} = V_g - V_{OFF}$ . The derived values of  $n_s$  and  $E_f$ at three values of  $V_g$ , are further utilized to linearly solve (3) to attain the values of  $k_1 = -0.1107$  eV,  $k_2 = 1.6466 \times 10^{-9}$  eV·m, and  $k_3 = 1.0039 \times 10^{-18}$ <sup>18</sup> eV·m<sup>2</sup>. Now, from equations (1) and (3),  $n_s$  can be given as:

$$n_{s} = \left(\frac{-k_{2} + \sqrt{k_{2}^{2} + 4k_{4}(V_{G1} - V(x))}}{2k_{4}}\right)^{2}$$
(6)

where,  $V_{G1} = V_g - V_{OFF} - k_1$  and  $k_4 = k_3 + \frac{qd}{\epsilon}$ . Now using approximate binomial expansion of equation (6),  $n_s$  can be expressed as:

$$n_s = A + BV(x) \tag{7}$$

where,  $A = \frac{V_{G_1}}{k_4} + \frac{2}{\gamma k_4} (1 - \sqrt{1 + \gamma V_{G_1}})$  and  $B = \frac{1}{k_4} (\frac{1}{\sqrt{1 + \gamma V_{G_1}}} - 1)$ , where  $\gamma = \frac{4k_4}{k_2^2}$ .

The current density (J) in the channel of MZO HFET can be expressed as:

$$J = \sigma \xi \tag{8}$$

where,  $\sigma$  is conductivity and  $\xi$  is the applied electric field and is given by  $\xi = \frac{dV(x)}{dx}.$ 

From equation (8), drain current  $(I_d)$  can be written as:

$$I_{\rm d} = q n_s W \nu_d \tag{9}$$

where, W is the channel width, and  $v_d$  is the drift velocity and is given as:

$$\nu_{d} = \begin{cases} \frac{\mu\xi}{1 + \frac{\xi}{2\xi_{c}}} & \text{for } \xi < \xi_{c} \\ \nu_{sat} & \text{for } \xi \ge \xi_{c} \end{cases}$$
(10)

where,  $\mu$  is the electron mobility,  $v_{sat}$  is the electron saturation velocity  $(1 \times 10^6 \text{ cm/s})$  [1] and  $\xi_c$  is the saturation electric field and is given by  $\xi_c = \frac{v_{sat}}{\mu}$ .

#### Table 5.1

# PARAMETERS OF Mg<sub>x</sub>Zn<sub>1-x</sub>O and Cd<sub>y</sub>Zn<sub>1-y</sub>O AT ROOM TEMPERATURE

Parameters	$Mg_xZn_{1-x}O[18]$	Cd <sub>y</sub> Zn <sub>1-y</sub> O [16]
Lattice constant	0.325 + 0.0016x +	$0.325 \pm 0.143x + 0.147x^2$
(a) (nm)	$0.0109x^2$	$0.323 \pm 0.143$ y $-0.147$ y
Spontaneous Polarization $(P_{sp})$ (C/m <sup>2</sup> )	- 0.057 - 0.066x	- 0.15y -0.057(1-y)
Energy Bandgap ( <i>E</i> g) (eV)	3.37 + 2.145x	$3.37 - 2.28y + 0.95y^2$

Now, for calculation of the linear region of the output characteristics of MZO and MCO based HFETs,  $I_d$  can be derived by substituting (10) in (9) for  $\xi < \xi_c$  and integrating the equation from source end of the channel (x = 0) to drain end of the channel (x = L), as:

$$\int_{x=0}^{x=L} I_d dx = q \mu W \int_{V_{x=0}}^{V_{x=L}} n_s \, dV - \frac{I_d}{2E_c} \int_{V_{x=0}}^{V_{x=L}} dV \tag{11}$$

Now solving (11) at potential boundary conditions at the edge of the channel ( $V_{(x=0)} = I_d R_s$  and  $V_{(x=L)} = V_d - I_d R_d$ ) with expression of  $n_s$  from (7),  $I_d$  can be expressed as:

$$I_d = \frac{-b + \sqrt{b^2 - 4ac}}{2a}$$
(12)

where  $a = -(R_d + R_s) - \lambda(R_d^2 - R_s^2)$ ,  $b = 2\xi_c L + V_d + 2\lambda(A(R_d + R_s) + BV_dR_d)$ ,  $c = -\lambda V_d(2A + BV_d)$  and  $\lambda = Wqv_{sat}$ .

In addition, for calculating the saturation region of the output characteristics of MZO- and MCO-based HFETs,  $I_d$  (I<sub>dsat</sub>) can be calculated by substituting  $\nu_d$  for  $\xi \ge \xi_c$  from (10) in (9) as:

$$I_{\rm dsat} = \lambda (A + BV_{\rm dsat}) \tag{13}$$

By solving (12) at  $V_d = V_{dsat}$  and (13), we attain  $V_{dsat}$  as:

$$V_{dsat} = \frac{-\beta + \sqrt{\beta^2 - 4\alpha\chi}}{2\alpha} \tag{14}$$

here, for small values of  $\alpha$ ,  $\beta$ , and  $\chi$  a simplified root is given as:

$$V_{dsat} = \frac{-\chi}{\beta} \tag{15}$$

where,  $\chi = 2A(\xi_c L + \lambda A(R_d + R_s))$  and  $\beta = 2B(\xi_c L + \lambda AR_d) - A$ .

The derived analytical expression is solved in MATLAB environment to attain  $I_d$  values in polycrystalline ZnO based HFETs. The material parameters of MgZnO, ZnO and CdZnO are derived from our previous analytical works [8, 11] and presented in Table 5.1. The  $Q_i$  values are derived empirically to fit the experimental  $n_s$  and  $I_d$  values.

## 5.3 Results and Discussion



Fig. 5.2: (a) Variation of  $I_d$  with  $V_g$  in MZO-based HFET for  $Q_i = 0$ , with a constant value of  $Q_i$  and with  $Q_i$  linearly varying with  $V_g$ . (b) Graphical representation of ionized  $Q_i$  modulation with applied  $V_g$ . (c) Output characteristics of MZO-based HFET with different values of  $V_g$  (-1, 0, and 1 V) for constant  $Q_i$  and linearly modulated  $Q_i$ .

Fig. 5.2(a) shows the transfer DC characteristics of MZO-based HFET for 2 nm barrier layer thickness, 1  $\mu$ m channel length, 50  $\mu$ m channel width at constant 4 V drain voltage, with  $n_s = 1.4 \times 10^{11}$  cm<sup>-2</sup>, and  $\mu = 240$  cm<sup>2</sup>/V.s [6] at  $V_g = 0$  V and other parameter values for calculation of  $I_d$  are derived from our previous reports [8, 11]. It is observed that for  $Q_i = 0$ ,  $V_{OFF}$  starts very close to 0 V and by considering constant value of  $Q_i$  (~ 7.3 × 10<sup>17</sup> cm<sup>-3</sup>),  $V_{OFF}$  shifts close to -3 V, with the  $I_d$  variation with  $V_g$  maintaining similar slope as for  $Q_i = 0$  case.  $V_{OFF} \approx 0$  V for  $Q_i = 0$  case is indicative of very low barrier layer thickness, in this case 2 nm, which is barely higher than

the critical thickness limit of the barrier layer to form the 2DEG channel [11]. In addition, the shift in  $V_{\text{OFF}}$  and  $I_d$  by introducing a constant value of  $Q_i$  can be attributed to the increase in 2DEG density [5], and therefore, an additional demand of reverse potential to deplete the enhanced channel to turn the device off [11]. It is also observed in Fig. 5.2(a), that neither  $Q_i = 0$  nor constant  $Q_i$  case matches with the experimentally obtained results of the transfer characteristics. A satisfactory agreement with the experimental results [6] is achieved by considering a linear modulation of  $Q_i$  with  $V_g$  (~( $7.3 \times 10^{17} + 5.5 \times 10^{17} \times V_g$ ) cm<sup>-3</sup>), extracted empirically. In one of our group's previous work [12], an experimental C-V study of Au/MgZnO presented that the interface states density in MgZnO decreases with increasing  $E_c$ - $E_{ss}$ , here,  $E_c$  is the conduction band minimum, and  $E_{ss}$  is the energy level of the interface states. Further,  $E_c$ - $E_{ss}$  is calculated utilizing below given equation:

$$E_c - E_{SS} = q(\phi_e - V) \tag{16}$$

Where, q is charge of electron,  $\phi_e$  is the effective barrier height, which is constant for a given measurement temperature, and V is the applied bias voltage. As q and  $\phi_e$  are constant, for a given measurement temperature, increasing applied bias V, decreases  $E_c$ - $E_{ss}$ , therefore an increase in  $N_{ss}$  with decreasing  $E_c$ - $E_{ss}$  can be inferred as increase of  $N_{ss}$  with increasing V. A similar result and explicit increase in  $N_{ss}$  with V is present in the study of Turut *et al* [13]. This is consistent with the available reports in the literature presenting an increase in  $Q_i$  at the heterojunction interface with an increased applied potential [13, 14]. Based on these experimental results, it was postulated that increase in interface defect density with applied bias can be generalized, and hence, an increase in  $Q_i$  with increase in applied  $V_g$ was utilized in the proposed drain current model. The non-linearity in the experimental as well as modeled  $I_d$ - $V_g$  characteristics towards higher  $V_g$ , in the linearly modulated  $Q_i$  case, arises due to the fact that  $V_{dsat}$  increases beyond 4 V, for higher  $V_g$  values.

Fig. 5.2(b) presents a graphical representation of the ionization of interface states with a rise in the value of  $V_g$  ( $V_g > 0$ ) and neutralization of interface

states for declining  $V_g$  ( $V_g < 0$ ). This representation takes into account the non-idealities of the interface grown by DIBS and other polycrystalline growth techniques [4], which manifests themselves as traps and defects near the interface creating interface states, which act as donors. Electrons in these trap states can be mobilized by an applied external electric field, which is provided by  $V_g$  and as  $V_g > 0$  is applied, these electrons in trap defect states shifts towards the upper surface of barrier under electrostatic force on these electrons, leaving these trap defect states ionized positively. Similarly, under  $V_g < 0$ , these trap electrons are repelled from the barrier surface towards the interface, neutralizing the trap defects near the interface. These donor interface states are neutral below  $E_F$  and when ionized act as unbalanced positive charge [7, 14].

Fig. 5.2(c) presents analytically obtained output characteristics of Mg<sub>0.3</sub>Zn<sub>0.7</sub>O/ZnO-based HFET for  $n_s = 8.5 \times 10^{12}$  cm<sup>-2</sup>,  $\mu = 165$  cm<sup>2</sup>/V.s [1], at  $V_g = 0$  V, d = 1.5 nm, L = 2  $\mu$ m, and W = 50  $\mu$ m at different  $V_g$  values (-1, 0 and 1 V). It is observed from Fig. 2(c) that a constant value of  $Q_i$  satisfies the drain current model only for  $V_g = 0$  V case, however, does not accommodate the model when there is a change in the value of  $V_g$ . In Fig. 5.2(c),  $I_d - V_d$  characteristics agree with the experimental results [1] only when a linearly modulated  $Q_i$  is considered with  $V_g$ .





Fig. 5.3: (a) Output characteristics of MCO-I and MCO-II HFETs for  $\mu = 100\%$  and 10% that of the electron mobility in MZO HFET. (b) Variation in the  $I_d$  values of MCO-I HFET for considering the relation between  $Q_i$  and  $\mu$ . (c) Variation in the  $I_d$  values of MZO and MCO (at Cd = 5, 10 and 15 at. %) based HFETs at different L values, while maintaining W, d and x as constant.

Fig. 5.3(a) shows the output characteristics of MZO HFET in comparison to the similar HFET with ZnO buffer layer replaced by Cd<sub>0.15</sub>Zn<sub>0.85</sub>O (MCO-I) and Cd<sub>0.05</sub>Zn<sub>0.95</sub>O (MCO-II), at constant W = 50  $\mu$ m, L = 1  $\mu$ m, and d = 2 nm, plotted for  $V_g = 0$  V. The output characteristics of MCO-I and MCO-II HFETs are analyzed for  $\mu = 100\%$  and 10% of the electron mobility value in MZO. The value  $\mu = 100\%$  assumes the value of  $\mu$  in MCO is equivalent to that observed in MZO heterostructure with same dand x, which considers an ideal condition that a similar order of mobility could be maintained both in MCO and MZO. Similarly, the value  $\mu = 10\%$ assumes the value of  $\mu$  in MCO one order lower than that found in MZO heterostructure with same d and x, as observed in [3]. It is observed from Fig. 5.3(a) that, in ideal assumption case of  $\mu = 100\%$ , the value of  $I_{dsat}$  in MCO-I and MCO-II HFETs are ~50% and ~20%, respectively, higher than that in MZO HFET. However, for  $\mu = 10\%$ , the  $I_{dsat}$  reduces by ~77% and ~81% in MCO-I and MCO-II HFET, respectively. It should be noted here that in the analysis of Fig. 5.3(a), the reduction in  $\mu$  has been assumed to be independent of the change in  $Q_i$ , and all output characteristics have been analyzed at constant  $Q_i$  value obtained for MZO HFET at  $V_g = 0$  V. These

observations suggest that ideal MCO HFETs could provide significant advantage over MZO HFETs, even with a Cd content as low as 5 at.% in buffer ZnO. However, a practical MCO interface tend to have lower electron mobility as compared to that in MZO and hence, the output performance of MCO HFETs may be lower than MZO HFETs.

The analysis in Fig. 5.3(a), while takes into account the impact of reduced  $\mu$  due to a ternary alloy in buffer, it does not consider a probable rise in defects and in turn increase in  $Q_i$  due to such introduction of a ternary alloy in the buffer [15]. A more accurate comparison is depicted in Fig. 5.3(b), which takes into account the probability of change in  $Q_i$  with a reduced electron mobility. Fig. 5.3(b) shows the output characteristics of MCO-I for  $\mu = 100\%$  and 10% of that in MZO, with a 160% increase in  $Q_i$  value from that acquired in MZO case (100%  $Q_i$ ) for  $V_g = 0$  V, in  $\mu = 10\%$  case. This 160% increase in  $Q_i$  has been calculated from the analytical expression of  $n_{\rm s}$  required to fit the experimental values of  $n_{\rm s}$  in MZO and MCO heterostructures grown by DIBS [3, 11, 16]. It is observed in Fig. 5.3(b) that for  $\mu = 10\%$ , considering experimental  $n_s$  for MCO-I,  $I_{dsat}$  enhances by ~22% over the 100%  $Q_i$  case. This is consistent with the fact that a reduced mobility could be imparted to the interface roughness, dislocation and alloy disorder scattering due to growth, lattice and interface defects, which are major contributors to the formation of interface trap defects, which provides increased  $Q_i$  [7, 17]. Henceforth, these results suggest that even with polycrystalline growth leading to larger  $Q_i$  and lower mobility, MCO HFETs could provide comparable DC performance to MZO HFETs.

Fig. 5.3(c) shows the variation of  $I_d$  in MZO- and MCO- (for Cd = 5, 10, and 15 at.%) based HFETs for varying L, while keeping W = 50  $\mu$ m, d = 2 nm and x = 0.3 in the HFET structures, at  $V_d = 4$  V and  $V_g = 0$  V. It is observed that  $I_d$  in the MCO HFETs with same  $Q_i$  (100%  $Q_i$ ) and  $\mu$  (100%  $\mu$ ) values as MZO structures, reduce with approximately the same slope (-0.0108 mA/ $\mu$ m) as that of MZO (-0.0103 mA/ $\mu$ m) for all the cases of Cd composition. The reduction in  $I_d$  with increasing L is due to direct proportionality of  $I_d$  with W/L ratio; and the ratio reduces with increasing

L in Fig. 5.3(c) as W is kept constant. Additionally, with an increase in Cd content in the buffer layer, the  $I_d$  values shift higher than those in MZO HFET. This is consistent with the fact that given constant  $Q_i$ , with increasing Cd content in the buffer layer,  $n_s$  in MCO heterostructure will increase proportionally to the increase in Cd content [8]. Further, Fig. 5.3(c) shows the variation of  $I_d$  in MCO-based HFETs at same Cd content in buffer layer, for  $\mu = 10\%$  and  $+160\% Q_i$  values, by broken lines, presenting lower  $I_d$  values as compared to those in MZO-based HFET. Interestingly, the slope of change in  $I_d$  with L in this case is much less steeper (-0.0024 mA/ $\mu$ m) than that in the case of 100%  $Q_i$  and 100%  $\mu$  values in MCO. This is probably due the significant rise in the value of  $Q_i$ , which overshadows the impact of lowering W/L ratio in the considered case. Here, it must be noticed that depending upon the growth quality of the polycrystalline barrier-buffer interface in ZnO-based HFET, the slope of  $I_d$  with respect to L could significantly alter for specific values of L.

In the prior literature, pertaining to oxide-semiconductor interface, it is well established that lower barrier oxide thickness (d) creates more interface defects compared to thicker barrier oxide layers [18]. Thus, this inverse proportionality relationship between  $Q_i$  and d is modelled in the equations of  $n_s$  (equation 1 above) in MZO and MCO-I HFETs. Fig. 5.4(a) shows  $I_d$ values in MZO and MCO-I ( $\mu = 100\%$  with 100%  $Q_i$  and  $\mu = 10\%$  with +160%  $Q_i$ ) HFETs with varying d, considering two scenarios: (i)  $Q_i = (Q_{i,j})$  $v_{g=1 V}/d$ , where  $Q_{i, V_{g=1 V}}$  is the empirical value of  $Q_i$  derived for  $V_g = 1 V$ in MZO and MCO HFETs; (ii)  $Q_i = (Q_{i, Vg = 1 V})$ . Here,  $Q_{i, Vg = 1 V}$  in MCO-I HFET for  $\mu = 10\%$  includes the +160% enhancement in  $Q_i$  values from  $Q_i$ derived for MZO. It is observed that, in all HFETs, considering  $Q_i$  inversely proportional to d,  $I_d$  is almost independent of d in polycrystalline ZnO heterostructure based HFETs. This observation could be possibly due to an increase in  $n_{\rm s}$  and decrease in  $Q_{\rm i}$  with the corresponding rise in d occurring simultaneously. However, it is noteworthy that the relative variation of values of  $n_s$  and  $Q_i$  at different values of d, could significantly alter the slope of  $I_d$  with respect to d, depending upon the quality of polycrystalline heterostructure at respective value of d.



Fig. 5.4: (a)  $I_d$  values in MZO and MCO-I ( $\mu = 100\%$  with 100%  $Q_i$  and 10% with +160%  $Q_i$ ) HFETs with varying barrier layer thickness, considering constant  $Q_i$  and thickness dependence of  $Q_i$ . (b) Mg content dependency of  $I_d$  in MZO and MCO-I ( $\mu = 100\%$  with 100%  $Q_i$  and 10% with +160%  $Q_i$ ) HFETs for constant  $Q_i$  and its dependence on Mg content in barrier layer.

However, considering the variation in  $Q_i$  with *d* negligible ( $Q_{i, Vg=1V}$ ), it is observed  $I_d$  rises with the increase in *d* in all HFETs and saturates towards higher *d*. This observation mimics the relation of  $n_s$  and *d*, reported in the prior literature [11, 19], which suggests, in case of constant  $Q_i$ ,  $I_d$  is dependent upon the variation of 2DEG in the heterostructure. Results in Fig. 5.4(a) are based upon the two extreme assumptions of inverse proportionality of  $Q_i$  with *d* and complete independence of  $Q_i$  on *d*, which exhausts all possible effects of interface defects upon  $I_d$  in MZO and MCO HFETs relating to varying barrier layer thickness. Therefore, the experimental relationship of  $I_d$  with *d* in polycrystalline MZO and MCO HFETs could be a combination of the two extreme cases, as presented in Fig. 5.4(a).

In addition to thickness dependence of  $Q_i$ , Mg content in barrier layer has also been identified as a cause for variation in  $Q_i$ . As lower Mg content in the barrier layer has lower lattice mismatch with the buffer layer, the straining in barrier layer is less and hence lower defects are formed at the barrier-buffer interface as compared to those in the barrier layer with higher Mg content [20]. For higher Mg contents in the barrier layer, the variation in  $Q_i$  is not significant [5]. However, to comprehend all possible case scenario, this work considers: (i) a linear dependence of  $Q_i$  on Mg content in the barrier layer depicted as  $Q_i = (Q_{i, Vg = 1 V}) \times x$ ; (ii)  $Q_i$  completely independent of Mg content depicted as  $Q_i = (Q_{i, Vg = 1 V})$ . Fig. 5.4(b) shows Mg content dependence of  $I_d$  in MZO and MCO-I ( $\mu = 100\%$  with 100%  $Q_i$  and  $\mu = 10\%$  with +160%  $Q_i$ ) HFETs with d = 2 nm,  $V_g = 1$  V,  $V_d = 5$  V,  $L = 1 \mu m$  and  $W = 50 \mu m$ . It is observed that, for constant  $Q_i$  case,  $I_d$  values are weakly related to Mg content. The approximately independent variation of  $I_d$  with Mg content is similar to the variation of 2DEG density with Mg content in sputtering grown MZO heterostructure [5].

For the linear dependence case of  $Q_i$  on x, the linear increase in  $I_d$  with rising x is due to channel enhancement with more ionized positive interface states at the interface coupled with an increase in  $\sigma_1$ . Here, the experimental  $I_d$  values for different x in the barrier layer can turn up as an amalgamation of the two assumed cases in both MZO- and MCO-HFETs, depending upon the growth quality of polycrystalline heterostructure for specific value of xin barrier layer.

# **5.4 Conclusion**

An in-depth analysis of DC characteristics in polycrystalline MZO and MCO HFETs has been presented. This work conclusively presents significant role of  $Q_i$  in ascertaining the  $I_d$  values in polycrystalline ZnObased HFETs. The replacement of CdZnO, with a relatively lower  $\mu$ , in the place of ZnO in the buffer layer is observed to lower the  $I_{dsat}$  value in ZnObased HFET. However, considering the enhancement in  $Q_i$  for corresponding decrease in  $\mu$ , the overall reduction of  $I_{dsat}$  in MCO HFET is negligible. This work has extensively explored major relationships of  $Q_i$ , which governs  $I_d$  in HFETs, with d and x to convincingly postulate that the experimental  $I_d$  in polycrystalline MZO and MCO-based HFETs could be an amalgamation of the two extreme cases of  $Q_i$  dependent and independent on d and x. The present study is significant in the development and
optimization of ZnO-based low-cost, large-area-growth compatible HFETs.

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## Chapter 6

# Drain Current Optimization in DIBS Grown MgZnO/CdZnO Heterostructure based HFET

## **6.1 Introduction**

In one of our previous works [1], we have theoretically estimated higher  $n_s$  at lower Mg compositions ( $x \le 0.3$ ) in barrier layer, for epitaxial grown MgZnO/CdZnO (MCO) as compared to that in MgZnO/ZnO (MZO). In another work [2], we experimentally confirmed higher  $n_s$  (~6×) in sputtered MCO than that in similarly grown MZO and analytically estimated epitaxial MCO heterostructure. The drawback observed in DIBS grown MCO heterostructure was one order lower electron mobility ( $\mu \approx 3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ) [2] compared to sputtered MZO heterostructure (~30 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>) [3, 4], at barrier layer thickness ( $t_b = 30 \text{ nm}$ ) and x = 0.3, which restricted its conductance ( $n_s \times \mu$ ) to be utilized in HFET application.

This chapter attempts to establish DIBS grown MCO heterostructure as a viable HFET material alongside the MBE grown MZO, due to the largearea growth capability and therefore, cost-effectiveness of sputtering system. Experimentally depositing a thick (> 0.6  $\mu$ m) CdZnO was found challenging, and a thick CdZnO was essential to get unstrained buffer layer. In ZnO such limitations were not encountered and buffer layers as thick as 1  $\mu$ m were deposited easily. With strained CdZnO buffer (~400 nm), we were able to achieve high  $n_s$  in MgZnO/CdZnO (~6×) compared to that in MgZnO/ZnO with thick buffer (1  $\mu$ m thick) [2]. The only drawback that persisted was drop in electron mobility in MgZnO/CdZnO heterostructure due to very high interface roughness (~10-20 nm), which was missing in the MgZnO/ZnO heterostructure due to unstrained thick ZnO buffer. It was observed that MgZnO/ZnO heterostructure with a 1  $\mu$ m thick buffer ZnO layer has a better crystallinity (from Selected Area Electron Diffraction (SAED) patterns) than that of MgZnO/CdZnO with ~400 nm CdZnO buffer. Since interface roughness leads to higher scattering of channel electrons and thereby reduces electron mobility [5], a low crystallinity of CdZnO buffer was assumed to be the reason for a lower electron mobility in MgZnO/CdZnO heterostructure as compared to that of MgZnO/ZnO, grown similarly. Therefore, to improve the crystallinity and in turn enhance the electron mobility of MgZnO/CdZnO heterostructure with the thickness limitation of CdZnO, a 30 nm Y<sub>2</sub>O<sub>3</sub> (Yttria) was introduced, optimized for cubic crystallinity elsewhere [6], as spacer layer between p-Si substrate and CdZnO buffer. This has shown to improve the crystallinity of the 400 nm thick CdZnO buffer layer significantly along with better demarcation of MgZnO/CdZnO heterointerface. The improvement in crystallinity and interface has shown to enhance the  $\mu$  (~20 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>) by nearly one order in DIBS grown Yttria spacer based MCO (MCO-II) compared to that in the non-Yttria spacer based MCO (MCO-I) (~3 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>). In addition negligible reduction is found in  $n_s$  (~1.8 × 10<sup>14</sup> cm<sup>-2</sup>) in MCO-II than that in MCO-I (~2.8 × 10<sup>14</sup> cm<sup>-2</sup>) at  $t_{\rm b} = 50$  nm and x = 0.3. Therefore, MCO-II shows an improved overall  $n_s \times \mu$  than that in sputtered MZO and MCO-I. As MZO heterostructure can be fabricated with a thick (~1  $\mu$ m) ZnO buffer layer with a good degree of crystallinity, an introduction of Yttria under ZnO buffer was not considered in this work, however, it could be studied in future works of this study.

Further, three metal combinations; (i) Au/Ni/Al/Ti, (ii) Au/Al/Ti, and (iii) Au/Ti, were studied by Transmission Line Measurement (TLM) technique to attain the metal combination and annealing conditions for least contact resistance ohmic contact on MgZnO surface. The optimized least contact resistance providing metal combination is patterned onto SiO<sub>2</sub> mesa isolated MCO-II based active region pads to form Source and Drain contacts in a Gateless HFET configuration. The developed Gateless DIBS grown MCO-II based HFET has presented drain currents as high as ~400 mA/mm, one of the highest ever reported in a ZnO based HFET. The results suggest that DIBS grown MCO-II based HFET could provide a cost-

effective large-area electronics compatible solution for HFET based sensor applications [7, 8].



## **6.2 Experimental Details**

Fig. 6.1: (a) Image of the TLM dark field mask. (b) Schematic of TLM metal bars on MCO heterostructure with different d values. (c) Schematic of three metal combinations I, II, and III used for contact resistance study on MCO heterostructure. (d) Optical profilometer images of developed metal combination bars.

Three heterostructures were deposited by DIBS, namely; (i) 50 nm Mg<sub>0.3</sub>Zn<sub>0.7</sub>O barrier layer on 1  $\mu$ m ZnO buffer layer over *p*-Si substrate

(MZO), (ii) 50 nm Mg<sub>0.3</sub>Zn<sub>0.7</sub>O on 400 nm Cd<sub>0.15</sub>Zn<sub>0.85</sub>O over *p*-Si substrate (MCO-I), and (iii) 50 nm Mg<sub>0.3</sub>Zn<sub>0.7</sub>O on 400 nm Cd<sub>0.15</sub>Zn<sub>0.85</sub>O over 30 nm Y<sub>2</sub>O<sub>3</sub> deposited p-Si (MCO-II). The thickness of layers were measured by the average deposition rate, and were deposited by DIBS system at Ar:O<sub>2</sub> = 2:3 and 300 °C (100 °C for Y<sub>2</sub>O<sub>3</sub>), with beam voltage of 800 V, ion beam power of 44 W, and  $2.43 \times 10^{-4}$  mbar working pressure inside the DIBS chamber. The barrier and buffer layers are deposited using commercially available MgZnO and CdZnO sputtering targets [9]. Prior to film deposition, in order to remove organic contaminants and native oxide, Si substrate is thoroughly cleaned, details of which are described in our previous work [10]. The deposited heterostructures were examined for sheet carrier concentration (*n*<sub>s</sub>) and electron mobility ( $\mu$ ) by Hall measurement using four In metal ohmic contacts, soldered in Van der Pauw configuration at 400 °C on the top of MgZnO.

Further, a Transmission Line Measurement (TLM) dark field mask, as shown in Fig. 6.1(a), was used to pattern e-beam evaporated metal combinations by lift-off process to develop rectangular ( $20 \ \mu m \times 200 \ \mu m$ ) bars spaced at linearly increasing distance (*d*) (20, 100, 200, 400, 800, 1000, 1200, 1400 and 1600  $\mu$ m), as shown in Fig. 6.1(b). The three combinations of metal contacts deposited are as shown in Fig. 6.1(c); (i) 40 nm Au on top of 20 nm Ni, over 120 nm Al, and over 10 nm Ti, (structure I), (ii) structure I without 20 nm Ni (structure II), and (iii) structure II without 120 nm Al (structure III). The developed TLM contacts were observed using Zeta 3D optical profiler, as shown in Fig. 6.1(d). Total resistance (*R*<sub>t</sub>) between every pair of linearly spaced metal contact bar was measured using Keithley 4200SCS Semiconductor Parameter Analyzer (SPA) and Everbeing probe station.

In addition, 3" diameter wafer of as-grown MCO-II heterostructure was patterned into active region islands using bright field mask and wet chemical etching, as shown in Fig. 6.2(a) along with optical profiled image of as-developed active region pad. Further, mesa-isolation between the active region pads was created by depositing SiO<sub>2</sub> using PECVD, patterned

by dark field mask and etched by Reactive Ion Etching (RIE) from the active region pads, as shown in Fig. 6.2(b) along with optical profiled image of active region pad opened out of SiO<sub>2</sub> while rest of the area is covered in photoresist. Hereafter, structure I was e-beam evaporated on mesa isolated active pads, and patterned using dark field source-drain mask to achieve source and drain contacts by lift-off process, as shown in Fig. 6.2(c) along with the optical profiled image of as-developed source drain contacts.



Fig. 6.2: (a) Schematics of the bright field active region mask and developed active region (left) along with optical profilometer image of the developed active region (right). (b) Schematics of the dark field  $SiO_2$  mesa isolation mask and developed  $SiO_2$  mesa isolation (left) along with optical profilometer image of the active region RIE etched out of  $SiO_2$  (right). (c)

Schematics of the dark field Source-Drain mask and developed Source and Drain contacts (left) along with optical profilometer image of the developed gateless HFET (right).

## 6.3 Results and Discussion





Fig. 6.3: HR-TEM images of (a) MZO, (b) MCO-I, and (c) MCO-II heterostructures grown by DIBS under same growth conditions. The inset in all images shows SAED patterns of the respective heterostructures. (all TEM and SAED images were captured by Mr Tomohiko Yamakami and provided by Dr. Myo Than Htay of the Technical Division, Faculty of Engineering, Shinshu University) (d) Box plots for conductivity figure of merit ( $n_s \times \mu$ ) in MZO, MCO-I and MCO-II heterostructures.

Fig. 6.3(a), (b), and (c) show High Resolution-Transmission Electron Microscopy (HR-TEM) images of the MZO, MCO-I and MCO-II heterostructure. It is observed from the HR-TEM images that distinct MgZnO/ZnO and MgZnO/CdZnO interfaces are visible in MZO and MCO-II heterostructures in Fig. 6.3(a) and (c). However, in Fig. 6.3(b) the MgZnO/CdZnO heterointerface is not distinctly defined. The distinct demarcation of MgZnO/CdZnO interface in MCO-II against that in MCO-I can be attributed to the introduction of crystalline  $Y_2O_3$  as a spacer layer in MCO-II, which improves the lattice matching of the substrate and buffer CdZnO layer. In addition, the inset images in Fig. 6.3(a), (b), and (c) shows Selected Area Electron Diffraction (SAED) patterns in as-grown MZO, MCO-I and MCO-II heterostructures, respectively. The SAED patterns of MZO and MCO-II show a nearly crystalline lattice pattern of the grown heterostructures, which can be attributed to the pattern observed in the [1 2  $\overline{1}$  0] axis of the wurtzite crystal [3], as opposed to the definitive polycrystalline circular ring pattern in MCO-I. The SAED patterns confirm the improvement in the crystallinity of the MCO-II heterostructure by introduction of 30 nm  $Y_2O_3$ . It is interesting that while 1  $\mu$ m ZnO is crystalline on p-Si, 400 nm CdZnO is polycrystalline on the same substrate. This is probably due to the unrelaxed strain in the CdZnO thin film opposed to the completely strain relaxed 1  $\mu$ m ZnO layer. A crystalline Y<sub>2</sub>O<sub>3</sub> has shown to decrease the dislocation density of growth planes in the CdZnO film, as can be seen in Fig. 3(c), and therefore, 400 nm CdZnO is strain relaxed and highly crystalline in MCO-II heterostructure.

Fig. 6.3(d) shows box plots of conductivity figure of merit ( $n_s \times \mu$ ) in MZO, MCO-I and MCO-II, for the as grown heterostructures sampled multiple times for  $n_s$  and  $\mu$ . It is observed in Fig. 6.3(d) that the mean  $n_s$  ( $< n_s >$ ) is higher in MCO-I ( $2.8 \times 10^{14} \text{ cm}^{-2}$ ) than those in MZO ( $9.2 \times 10^{13} \text{ cm}^{-2}$ ) and MCO-II ( $1.76 \times 10^{14} \text{ cm}^{-2}$ ). This is probably due to higher defect density in a polycrystalline MCO-I heterostructure compared to more crystalline MZO and MCO-II heterostructures. It has been established in prior literature [11] that higher defect states in terms of interface charges contribute towards higher  $n_s$ . In addition, the average  $\mu$  ( $< \mu >$ ) is approximately an order lower in MCO-I ( $3.1 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ ) compared to those in MZO ( $28.3 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ ) and MCO-II ( $19.9 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ ). This observation can probably be attributed to the higher dislocation density of growth planes and interface roughness [12] of MCO-I heterostructure, as visible in Fig. 3(b).



Fig. 6.4: (a) Total resistance ( $R_t$ ) obtained between individual pairs of I, II, and III metal combinations TLM contact bars on MgZnO surface spaced at linearly increasing distance d. (b) Specific contact resitivity in I, II, and III metal combinations annealed in  $N_2$  ambience for 30 s at different annealing temperatures.

It is interesting to note in Fig. 6.3(d), that the  $n_s \times \mu$  product in MCO-II is higher than both MZO and MCO-I. This is probably due to the enhancement in  $\mu$  in MCO-II due to reduced interface roughness and dislocation density, in addition to a high  $n_s$  value compared to that in MZO. In addition, the high conductivity in MCO-II is achieved for less than half buffer layer thickness (400 nm) compared to that in MZO (1  $\mu$ m), by introduction of a mere 30 nm Yttria layer, therefore making MCO-II, a costeffective and better performing heterostructure amongst the three heterostructures discussed.

Fig. 6.4(a) shows R<sub>t</sub> between two contact bars spaced at linearly increasing d values for non-annealed I, II and III contact combinations developed by TLM on MCO-II heterostructure. The inset in Fig. 6.4(a) shows the intersection of R<sub>t</sub> curve with zero d value. The specific contact resistivity ( $\rho_c$ ) values of contact combination I, II and III are 9.2 × 10<sup>-4</sup>  $\Omega$ -cm<sup>2</sup>, 3.1 × 10<sup>-3</sup>  $\Omega$ -cm<sup>2</sup>, and 7.7 × 10<sup>-3</sup>  $\Omega$ -cm<sup>2</sup>, respectively. The least  $\rho_c$  in contact I is

generally attributed to the Ni layer preventing Au diffusion through Al and Ti that can degrade the ohmic nature of the contact [13].

Fig. 6.4(b) shows  $\rho_c$  values in contact combinations I, II, and III annealed at different annealing temperatures in N<sub>2</sub> ambience for 30 s. The  $\rho_c$  for I varies from 6.1 × 10<sup>-4</sup>  $\Omega$ -cm<sup>2</sup> at 400 °C annealing to 1.9 × 10<sup>-4</sup>  $\Omega$ -cm<sup>2</sup> at 800 °C annealing. Similar trends in I, II, and III metal contacts were observed in prior literature [14] on GaN. Table 6.1 presents comparison of  $\rho_c$  for metal contact combinations I, II, and III on GaN surface and MgZnO surface (our work). The higher values of  $\rho_c$  for contact combinations I, II, and III, on MgZnO surface against that on GaN surface can probably be attributed to monolayer metal-oxide formation at MgZnO-Ti interface.

#### Table 6.1

## COMPARISON OF $\rho_c$ OF CONTACTS I, II, AND III ON MgZnO AND GaN BASED HETEROSTRUCTURES ANNEALED AT 800 °C

Contact Surface	Ι	II	III	
	$(\Omega$ -cm <sup>2</sup> )	$(\Omega$ -cm <sup>2</sup> )	$(\Omega$ -cm <sup>2</sup> )	
MgZnO	<b>1.9</b> × 10 <sup>-4</sup>	<b>4.8</b> × 10 <sup>-4</sup>	1.8× 10 <sup>-3</sup>	
(Our Work)				
GaN [14]	$1.6 \times 10^{-4}$	$3.8 \times 10^{-4}$	0.14	

Fig. 6.5(a) shows drain current ( $I_d$ ) with varying drain voltage ( $V_d$ ) in three similar samples (A, B and C) of non-annealed Drain and Source contacts, 200  $\mu$ m in width (W), developed on MCO-II heterostructures, with 50 nm barrier layer thickness (t<sub>b</sub>), 30 at.% Mg content in barrier layer and 10  $\mu$ m separation between Source and Drain contacts (D). The three samples have shown significantly coherent  $I_d$ . It is observed that the linear part of  $I_d$  ( $V_d$ < 8 V) in all three samples A, B, and C, is not perfectly ohmic. This could probably be due to the formation of TiO<sub>x</sub> monolayer at the MgZnO and Ti interface [15]. Fig. 6.5(b) shows  $I_d$ - $V_d$  characteristics in as developed gateless MCO-II based HFET for contacts annealed in N<sub>2</sub> environment for 30 s at different annealing temperatures (500, 600, 700 and 800 °C). It is observed that the saturation drain current improves ~2.5 times at 8 V, for samples annealed at 800 °C than that those annealed at 500 °C.



Fig. 6.5: (a) Drain current vs Drain voltage in three similarly developed Gateless DIBS grown MCO-II based HFET samples A, B, and C. (b) Drain current vs Drain voltage in as-developed Gateless DIBS grown MCO-II based HFET at different annealing temperatures annealed in N2 ambience for 30 s. (c) Comparison of Drain current in our developed DIBS grown MCO-II based HFET with MBE grown AlGaN/GaN and MgZnO/ZnO based HFET, for measurements at  $V_g = 0$  V.

In addition, the linear region of  $I_d$  curves improve significantly for annealed samples compared to non-annealed samples (shown in Fig. 6.5(a)). All these observations can probably be attributed to the diffusion of Al through In to the surface of barrier MgZnO layer with increasing annealing temperatures, therefore reducing the contact resistance of Source and Drain contacts [14]. In addition, the parasitic impedance at Ti-MgZnO interface also reduces due to diffusion of Al contact, therefore flattening the saturation curve with increasing annealing temperature.

Fig. 6.5(c) shows comparison of  $I_d$  value achieved in our 800 °C annealed gateless MCO-II HFET with 0 V gate voltage ( $V_g$ )  $I_d$ - $V_d$  curves of AlGaN/GaN [16] and molecular beam epitaxially (MBE) developed MgZnO/ZnO [17] based HFETs. The high values of  $I_d$  in  $I_d$ - $V_d$  curves establish MCO-II as a viable option for HFET development alongside with the accepted and existing MgZnO/ZnO and AlGaN/GaN heterostructures. However, due to non-availability of experimental results of MBE grown MgZnO/ZnO (D = 3  $\mu$ m and t<sub>b</sub> = 2 nm) and AlGaN/GaN (D = 5  $\mu$ m and t<sub>b</sub> = 40 nm) for MCO-II similar values of D (= 10  $\mu$ m) and t<sub>b</sub> (= 50 nm), an estimation of performance improvement in MCO-II based HFET in comparison with MBE developed MgZnO/ZnO and AlGaN/GaN based HFET cannot be ascertained by  $I_d$ - $V_d$  curves.

#### Table 6.2

## COMPARISON OF THIN FILM TRANSISTOR (TFT) PERFORMANCE PARAMETERS OF DEVELOPED MCO-II-BASED GATELESS TRANSISTOR WITH THE STATE-OF-THE ART TFTs

Material System	Growth Technique	Substrate	μ (cm <sup>2</sup> /Vs)	V <sub>th</sub> (V)	$I_{on}(A)/I_{off}(A)$	Reference
Mg <sub>0.3</sub> Zn <sub>0.7</sub> O/ Cd <sub>0.15</sub> Zn <sub>0.85</sub> O /Y <sub>2</sub> O <sub>3</sub>	DIBS	Silicon	19.9		8×10 <sup>-2</sup> /	This work
$ZrO_2/In_2O_3$	Spin- coating	Glass	5.82	0.57	9×10 <sup>-5</sup> / 3×10 <sup>-7</sup>	[18]
Al <sub>2</sub> O <sub>3</sub> /IGZO*	ALD	Glass	10.4	0.6	10 <sup>-4</sup> / 10 <sup>-13</sup>	[19]
Al <sub>2</sub> O <sub>3</sub> / Mg <sub>0.2</sub> Zn <sub>0.8</sub> O /ZnO	RF- Sputtering	Glass	84.22	-0.55	4×10 <sup>-4</sup> / 1×10 <sup>-9</sup>	[20]
Al <sub>2</sub> O <sub>3</sub> / IGZO	Spin- coating	PI**	5.41	0.65	10 <sup>-5</sup> / 10 <sup>-11</sup>	[21]

\*IGZO- Indium Gallium Zinc Oxide

\*\*PI-Polyimide

Further, a comparative analysis is of the developed gateless HFET is performed against the state-of-the art thin film transistor (TFT) parameters

in Table 6.2. As the developed device lacks gate contact, threshold voltage  $(V_{th})$  and off-state drain current  $(I_{off})$  is not yet available for the developed device. It is interesting to note that the as-developed MCO-II-based HFET shows highest on-state drain current  $(I_{on})$  in comparison to any other TFT yet reported, which gives ample margin to attain very high Ion/Ioff ratio for the developed MCO-II-based HFET.

The I<sub>d</sub> values attained in MCO-II Gateless HFET in this work are significant as utilizing DIBS asserts much lower fabrication cost due to large area electronics compatibility compared to MBE. In addition, the use of abundant low cost large area ZnO substrates [22, 23] will further drop the unit device price of DIBS grown MCO-II based HFET. From large-area electronics and low-cost of fabrication perspective, compatibility of proposed structure with glass and polymer substrate is of utmost significance. As all the layers in the proposed heterostructure are grown at low temperatures (Y<sub>2</sub>O<sub>3</sub>- 100 °C, CdZnO- 300 °C, and MgZnO- 300 °C), the heterostructure is compatible with Glass (Softening point- 700 °C, and Melting point- ~1000°C for Soda Lime Glass) substrate, and high temperature (growth temperature  $\geq 300$  °C) polymer substrates, along with Si and Sapphire substrate. Since, CdZnO buffer layer does not see the mechanical substrate in our proposed heterostructure, the optimization of crystallinity of Y<sub>2</sub>O<sub>3</sub> on any given substrate will ensure the consistency of the electrical performance parameters of the proposed structure. Further, reports of MgZnO/ZnO heterostructure based FET on Si [24], glass [20], and sapphire [25] substrate exists in literature. Therefore, this work provides a cost-effective large-area electronics compatible alternative to the existing MBE grown ZnO and GaN based HFETs. This is significant to develop low cost high conductance large-scale utilization HFET based devices such as biosensor, and water pollutant sensors, etc.

## **6.4 Conclusion**

In conclusion, this work shows that by using a 30 nm Yttria spacer layer, the conductivity figure of merit of DIBS grown MgZnO/CdZnO heterostructure can be improved over similarly grown MgZnO/ZnO heterostructure for half the buffer layer thickness (400 nm in MCO against 1  $\mu$ m in MZO). Further, Au/Ni/Al/Ti shows the least contact resistance on MgZnO barrier layer surface, annealed in N<sub>2</sub> ambience for 30 s. Further, utilizing the contact resistivity optimized Au/Ni/Al/Ti metal combination as Source and Drain contacts; a Gateless HFET is fabricated upon conductivity enhanced MCO-II heterostructure. High drain currents (~ 400 mA/mm) were achieved in the DIBS grown MCO-II based HEFT, which presents the possibility of developing cost-effective large-scale ZnO based HFET for high conductance sensor applications.

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## Chapter 7

## **Conclusion and Future Scope**

In conclusion, this work has successfully demonstrated the utilization of DIBS-grown MgZnO/CdZnO heterostructure towards development of lowcost HFETs. As this material combination was never explored prior to this work towards HFET application, the challenge faced during this work were to come up with innovative solutions, in analytical modelling and experimental structural design. This work therefore, started with the development of an analytical model for  $n_s$  in MgZnO/CdZnO heterostructure. It was designed to estimate the enhancement in  $n_s$ achievable by utilizing CdZnO as buffer layer instead of ZnO buffer layer. The electronegativity of Cd element and ionic radii of Cd<sup>2+</sup> changed the polarization and the lattice constants of the otherwise ZnO buffer layer towards significant enhancement in  $n_s$  in MgZnO/CdZnO heterostructure over MgZnO/ZnO heterostructure. This analytical enhancement of  $n_s$  in MgZnO/CdZnO over MgZnO/ZnO was than confirmed in an experimental work by growing MgZnO/CdZnO heterostructure by DIBS and comparing the  $n_s$  values to that in DIBS-grown MgZnO/ZnO heterostructure. A high value of  $n_s$  in MgZnO/CdZnO heterostructure was achieved (~6×), as compared with that in MgZnO/ZnO, at lower Mg ( $\leq 0.15$ ) compositions in barrier MgZnO layer. Upon the realization of high  $n_s$  in DIBS-grown MgZnO/CdZnO heterostructure, another analytical model was developed to estimate I<sub>d</sub> characteristics in polycrystalline MgZnO/CdZnO-based HFET. This model utilized ionized interface state density  $(Q_i)$  as an empirical parameter to account for the defect prone interface in a polycrystalline growth based heterointerface. The model presented that for polycrystalline MgZnO/CdZnO-based HFET even with one order lower electron mobility, the  $I_d$  values can be comparable to that achievable in polycrystalline MgZnO/ZnO-based HFET. After this analytical estimation of  $I_d$  in polycrystalline MgZnO/CdZnO-based HFET, the conductance ( $n_s$  $\times \mu$ ) of DIBS-grown MgZnO/CdZnO was enhanced by the introduction of 30 nm yttria (Y<sub>2</sub>O<sub>3</sub>) as a spacer layer over the Si substrate. The introduction of yttria improved the overall conductance of MgZnO/CdZnO up to  $3.5 \times 10^{15}$  V<sup>-1</sup>s<sup>-1</sup> as compared to  $9 \times 10^{14}$  V<sup>-1</sup>s<sup>-1</sup> in non-yttria spacer based MgZnO/CdZnO. This conductance enhanced yttria spacer based MgZnO/CdZnO was utilized to fabricate gateless HFET by developing source and drain contacts in a three-step lithography process. Prior to the development of source and drain contacts, TLM technique was utilized to ascertain the metal combination and annealing condition to achieve least specific contact resistivity on the MgZnO barrier layer surface. The *I*<sub>d</sub> in as-developed gateless MgZnO/CdZnO HFET was ~400 mA/mm, which is the highest *I*<sub>d</sub> value ever reported in ZnO based HFET. This study therefore conclusively establishes MgZnO/CdZnO heterostructure as a low-cost alternative for HFET development towards high-power and sensor devices.

## 7.1 Conclusions

The main outcomes of this thesis are summarized as follows:

- (i) A physics-based analytical model has been developed and utilized to show the need of efficiently utilizing the properties of buffer CdZnO layer to enhance  $n_s$  in MgZnO/CdZnO heterostructure, which was limited only to the barrier layer to enhance  $n_s$ . By alloying the buffer ZnO with Cd, the polarization of buffer layer was modulated to effectively enhance the net polarization difference at barrier-buffer interface. Also, addition of Cd in buffer increases the buffer lattice constant such that the compressive strain in barrier layer MgZnO prior to addition of Cd in buffer becomes tensile, thus increasing the net polarization in barrier layer. Both these effects favorably add-up to a significant enhancement in 2DEG density, for same compositional variations in barrier MgZnO layer.
- (ii) An experimental confirmation has been presented of the theoretically expected enhancement in  $n_s$  by replacing ZnO

buffer layer by CdZnO in MgZnO/ZnO heterostructure, at lower Mg compositions ( $x \le 0.15$ ) in barrier layer. Temperaturedependent Hall and *C-V* measurements confirmed the presence of carrier confinement at barrier-buffer interface. This work presented high  $n_s$  (~10<sup>14</sup> cm<sup>-2</sup>) for low Mg compositions ( $x \le$ 0.15) in barrier layer, in DIBS-grown MgZnO/CdZnO heterostructure. This was ~6× higher than the  $n_s$  obtained in DIBS-grown MgZnO/ZnO heterostructure for same Mg content in barrier layer and barrier layer thickness. The  $n_s$  achieved in the presented heterostructure system is one of the highest reported  $n_s$  values in ZnO or GaN based heterostructures.

- (iii) An in-depth analysis of  $I_d$  characteristics in polycrystalline MgZnO/ZnO and MgZnO/CdZnO HFETs has been presented. This work has conclusively presented significant role of  $Q_i$  in ascertaining the I<sub>d</sub> values in polycrystalline ZnO-based HFETs. Considering MgZnO/CdZnO heterostructure with one order lower  $\mu$ , as compared to that in MgZnO/ZnO heterostructure, the saturation drain current (Idsat) in MgZnO/CdZnO HFET is significantly low. However, considering the enhancement in  $Q_i$ for corresponding decrease in  $\mu$ , the overall reduction of  $I_{dsat}$  in MgZnO/CdZnO HFET becomes negligible as compared to that in MgZnO/ZnO HFET. This work has extensively explored major relationships of  $Q_i$ , which governs  $I_d$  in HFETs, with barrier layer thickness (d) and Mg content in barier layer (x) to convincingly postulate that the experimental  $I_d$  in polycrystalline MgZnO/ZnO and MgZnO/CdZnO-based HFETs could be an amalgamation of the two extreme cases of  $Q_i$  dependent and independent of d and x.
- (iv) In the last work of this thesis, it was shown that by utilizing a 30 nm yttria spacer layer, the conductance of DIBS grown MgZnO/CdZnO heterostructure can be improved over similarly grown MgZnO/ZnO heterostructure for half the buffer layer thickness (400 nm in MgZNO/CdZnO against 1  $\mu$ m in

MgZnO/ZnO). Further, Au/Ni/Al/Ti presented the least contact resistance on MgZnO barrier layer surface, annealed at 800 °C in N<sub>2</sub> ambience for 30 s. Utilizing the contact resistivity optimized Au/Ni/Al/Ti metal combination as source and drain contacts, a Gateless HFET was fabricated upon yttria spacer based MgZnO/CdZnO heterostructure using photolithography. High drain currents (~ 400 mA/mm) were achieved in the DIBS grown MgZnO/CdZnO-based gateless HFET, which presents the possibility of developing cost-effective large-scale MgZnO/CdZnO-based HFET for high power and sensor applications.

## 7.2 Future Scope

Although, an extensive work on the design and fabrication of MgZnO/CdZnO heterostructure has been described in this thesis, there are still some future challenges that needs to be tackled before establishing this heterostructure into a widely accepted HFET alternative. Few of the suggested future works are listed below:

- (i) Investigations of rectifying contact for gate formation needs to be pursued.
- (ii) Various high- $\kappa$  dielectrics needs to be investigated for achieving least leakage current and at the same time better control over the channel.
- (iii) The developed gateless and gated MgZnO/CdZnO-based HFETs can be specialized for power and sensing device applications.