Silicon Based Nanophotonic Device with Electric Control for Optical Switching

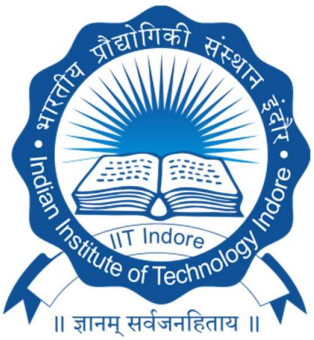
Ph.D. Thesis

By

LALIT SINGH

Under the Supervision of

Dr. Mukesh Kumar



DISCIPLINE OF ELECTRICAL ENGINEERING

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July 2020

Silicon Based Nanophotonic Device with Electric Control for Optical Switching

A THESIS

Submitted in partial fulfillment of the

requirements for the award of the degree

of

DOCTOR OF PHILOSOPHY

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"Silicon Based Nanophotonic Device with Electric Control for Optical Switching,"** in the partial fulfillment of the requirements for the award of the degree of **Doctor of Philosophy** and submitted in the **Discipline of Electrical Engineering, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from **March, 2016** to **July, 2020** under the supervisions of **Dr. Mukesh Kumar**, Associate Professor, Electrical Engineering, IIT Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Lalit Singh 07/08/2020

Signature of the student with date

(Lalit Singh)

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

7/08/2020

Signature of Thesis Supervisor with date

(Dr. MUKESH KUMAR)

LALIT SINGH has successfully given his Ph.D. Oral Examination held on **19th January 2021**

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Lalit Singh

Dedicated to

My Dear Mother & Father

List of Publication

A1. Published in journals for PhD work:

1. L. Singh, S. Jain and M. Kumar, "Electrically Writable Silicon Nanophotonic Resistive Memory with Inherent Stochasticity," **Optics Letters**, Vol. 44 (16) pp. 4020-4023, 2019. **(IF 3.866)**

2. L. Singh, S. Tidke and M. Kumar, "Guiding and controlling light at nanoscale in field effect transistor," **Applied Physics B,** Vol. 125 (6) pp.4-7, June 2019. **(IF 1.769)**

3. L. Singh, T. Sharma and M. Kumar, "Controlled Hybridization of Plasmonic and Optical Modes for Low-Loss Nano-Scale Optical Confinement with Ultralow Dispersion," **IEEE Journal of Quantum Electronics**, vol. 54, no. 2, pp. 1-5, April 2018. **(IF 2.753)**

4. L. Singh, Sulabh, S. Rajput, V. Kaushik, R. Mishra and M. Kumar, "Light Assisted Electro-Metallization in Resistive Switch with Optical Accessibility," **Journal of Lightwave Technology,** under review, 2020. **(IF 4.162)**

B1. Other publication in journals during PhD:

1. Sulabh, L. Singh, S. Jain and M. Kumar, “Nanophotonic Device based on Fano Resonance in Engineered Slot Waveguide for Optical Detection of Hepatitis B” revision submitted **IEEE Sensors Journal,** 2020**. (IF 3.076)**

2. Sulabh, V. Kaushik, L. Singh, S. Rajput and M. Kumar, “Nanophotonic Waveguide based on Engineered Horizontal-

vertical Slots for Polarization Independent Bio-chemical Sensing," (Accepted) 2021**(IF 2.2)**

3. V. Kaushik, S Rajput, Sulabh, S. Jain, L. Singh, and M. Kumar, "Efficient Sub-bandgap Photodetection via Two-dimensional Electron Gas in ZnO Based Heterojunction," **Journal of Lightwave Technology,** (Accepted) 2020**. (IF 4.162)**

4. S. Jain**,** Sulabh, S. Rajput, L. Singh, P. Tiwari, A. Shrivastava, and M. Kumar, "Thermally stable optical filtering using silicon-based comb-like asymmetric grating for sensing applications," **IEEE Sensors Journal**, vol.20(7) pp.3529-3535, 2020. **(IF 3.076)**

5. S. Sulabh, L. Singh, S. Jain and M. Kumar, "Optical Slot Waveguide with Grating-loaded Cladding of Silicon and Titanium Dioxide for Label-free Bio-sensing," **IEEE Sensors Journal,** Vol. 19(15) pp. 6126-6133,2019. **(IF 3.076)**

6. T. Sharma, L. Singh, and M. Kumar, "Nanophotonic Ultra-short Coupler Based on Hybrid Plasmonic Waveguide with Lateral Subwavelength Grating", **IEEE Transactions on Nanotechnology,** 15, 6 pp. 931-935,2016. **(IF 2.292)**

A2. Published in proceedings for PhD work:

1. L. Singh, P. Babu, Sulabh, S. Rajput and M. Kumar, "Optical Resistive Switch with High Extinction Ratio Using Plasmonic Amplification," Conference on Laser and Electro-Optics **CLEO-PR-2020**, Sydney, Australia, 2020.

2. L. Singh, R. D. Mishra, S. Rajput S. Jain and M. Kumar, "Enhanced Optical Readout in Resistive Memory Through Plasmonic Amplification," **ECIO-2020**, Paris, France, June 2020.

3. L. Singh, S. Jain, Sulabh and M. Kumar, “Loss Compensation in Hybrid Plasmonic Waveguide by Controlled Electron Injection,” **ICOL-2019** (International Conference on Optics and Electro-Optics), Instruments R&D Establishment, Dehradun, Uttar Pradesh India, 19 Oct 2019 - 22 Oct 2019.

4. L. Singh and M. Kumar, "Silicon Assisted Plasmonic Waveguide with Constant Group Delay and Flattened Dispersion Over Broadband," **Photonics 2018** - The International Conference on Fibre Optics and Photonics 12th to 15th December 2018.

5. L. Singh, M. Kumar, “Graphene based Electrically Tunable Hybrid Plasmonic-photonic Waveguide with Low loss and Nano-scale Optical Confinement,” The 2nd Edition of the European Graphene Forum **(EGF)**-2016.

B2. Other publication in proceedings during PhD:

1. S. Rajput, P. Babu, V. Kaushik, L. Singh, S. Jain and M. Kumar, “High Extinction Ratio in Silicon-ITO Heterojunction based Optical Modulator,” Conference on Laser and Electro-Optics **CLEO-PR-2020**, Sydney, Australia, 2020.

2. S. Jain, L. Singh, S. Rajput and M. Kumar,” Low Group Index Optical Slot Structure for Efficient Optical Modulation”, **CLEO-2020**, San-Jose, California, USA, 2020.

3. S. Jain, L. Singh, S. Rajput and M. Kumar,” Waveguide Engineering in Optical Slot Structure for Efficient Optical Modulation”, **ICOL-2019**, DRDO, Dehradun, 2019.

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ACRONYMS

MOS	*Metal Oxide Semiconductor*
MIM	*Metal Insulator Metal*
MIS	*Metal Insulator Semiconductor*
IPE	*Internal Photoemission*
SPP	*Surface Plasmon Polariton*
PIC	*Photonic Integrated Circuit*
SOI	*Silicon on Insulator*
DI	*De-Ionized*
HPW	*Hybrid Plasmonic Waveguide*
NIR	*Near Infra-Red*
I-V	*Current-Voltage*
FESEM	*Field Emission Scanning Electron Microscopy*
NVM	*Non-Volatile Memory*
VM	*Volatile Memory*
RRAM	*Resistive Random-Access Memory*
CB	*Conduction Bridge*
EDX	*Energy Dispersive X-ray Spectroscopic*
UV	*Ultraviolet*
ECM	*Electro-Chemical Metallization*
VCM	*Valency Change Memory*
HRS	*Limit of Detection*
DC	*Direct Current*
LRS	*Low Resistance State*

eV	*Electron Volt*
CMOS	*Complementary Metal Oxide Semiconductor*
Ag	*Silver*
Au	*Gold*
APTMS	*(3-Aminopropyl) Trimethoxy Silane*
FEM	*Finite Element Method*
SEM	*Scanning Electron Microscopy*
TEM	*Tunneling Electron Microscopy*
Si	*Silicon*
SiO_2	*Silicon Dioxide*
TiO_2	*Titanium Dioxide*
ZnO	*Zinc Oxide*
ITO	*Indium Tin Oxide*
VCCS	*Voltage Controlled Current Source*
FET	*Field Effect Transistor*
MOSFET	*Metal Oxide Field Effect Transistor*
TFET	*Tunneling Field Effect Transistor*
EO	*Electro Optic*
FDE	*Finite Difference Eigenmode (FDE) solver*

NOMENCLATURE

ε	*Dielectric Constant*
E_a	*Activation Energy*
m_o	*Electron Mass*
λ	*Wavelength*
$h\nu$	*Photon Energy*
Φ_B	*Potential Barrier*
E_{vac}	*Vacuum level Energy*
E_c	*Conduction Band Energy*
E_v	*Valance Band Energy*
E_g	*Energy Band gap*
E_F	*Fermi Level Energy*
n_e	*Electron Density*

ABSTRACT

Silicon Based Nanophotonic Device with Electric Control for Optical Switching

by

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Indian Institute of Technology Indore

Supervisor: Dr. Mukesh Kumar

Information processing at optical frequencies has its advantages, especially in terms of bandwidth. Photonic devices are rapidly emerging as saviors to meet bandwidth requirements in communication networks and high-speed computing. Compact photonics at real nanoscales can be the key to realize optical interconnects. The recent advances in the area of nanofabrication have given the ability to control the structure and properties of the devices to the desired levels. The miniaturization of the photonics devices is ideally limited by the diffraction limit of light which has been addressed with the proposal of novel guiding mechanisms. The coupling of light with collective oscillations of free electrons at a metal-dielectric interface is a potential candidate for nanoscale optical confinement beyond the diffraction limit. Such plasmonic waveguide with surface plasmon polariton (SPP) modes suffers from large metallic losses which limit its use in practical devices. Leaky mode confinement in a high refractive index layer underneath the HP confinement layer can further reduce the losses and can control propagation characteristics of the hybrid plasmonic waveguide for nanoscale devices. The large light-matter interaction can be harnessed for the application in electrical control of optical signals.

A silicon-based nanophotonic hybrid plasmonic waveguide is designed, fabricated, and characterized. An 11-nm thick SiO_2 on

silicon with gold as top layer provides us an optical-confinement at the nanoscale with an effective mode area of $\lambda^2/200$ an acceptably low loss of 7 dB/cm. The role high index layer (silicon) is analyzed. The grating is introduced in the silicon layer which provides us an ultra-low dispersion of 10 pico-sec^2/m and it passes through zero-dispersion value many times over a broad range of wavelength. The proposed work can be useful in realizing photonic platform at nanoscales for a variety of on-chip functionalities including high data rate optical interconnects which require low dispersion at nanoscales.

To electrically control the light in the proposed hybrid plasmonic waveguide, the field-effect transistor is proposed. The charge carrier dynamics along with the plasma dispersion effect in the silicon channel, through voltages applied on the gate and source-drain, results in the optical phase modulation in MOSFET and tunnel FET (TFET). A phase shift of π radian at a length of 1.2 mm and 0.21 mm is obtained in MOSFET and TFET, respectively. The proposed concept has the potential to enable the multifunctionality of the mature field-effect transistors.

To further improve the electrical control at nanoscale we consider the combination of the strength of the resistive switch with that of the photonics which has resulted in an interesting optical switching element. A nanophotonic resistive switch based on silicon is designed, fabricated, and characterized. The proposed electrically writable resistive switch with optical readout capability is demonstrated. An optical hysteresis curve with 10 dB of extinction ratio is obtained for a 1550-nm wavelength of light. The top electrode (metal Au) is chosen such that the conduction bridge formation uses both electrochemical metallization and valency change mechanism. The device showed a good self-rectifying ratio which enables it for realization in fabrication with multi-layer stacking. The optical readout is less error-prone compare to electrical readout and large bandwidth operation. The proposed device shows an inherent stochastic property where the set (writing) voltage reduces in each set-reset cycle, which

can be used for optical readout of synaptic weight for neuromorphic computations.

On the analysis of the device, it is observed that the optical extinction ratio can be improved by increasing the metal diffusion in the active layer. An improved extinction ratio of 16 dB is demonstrated by using silver as the top electrode and highly doped p-Si in the bottom electrode. The titanium oxide is used as the controlling layer sandwiched between these two highly conducting electrodes. The top metal electrode material is chosen such that it has low ionization energy, low electronegativity, and support SPP propagation with low optical loss. The SET voltage of the device is improved from 10 V to 4 V by application of blue pump light. The pump light increases the photogenerated charges which in turn increases the leakage current. The scheme helps in avoiding undesirable overshoot of current hence improving device life span. The electroforming of the conduction bridge at lower voltages reduces the overall power consumption of the device.

Chapter 1

Introduction to Integrated Nanophotonics

1.1 Integrated photonics

The demand for increasing high-speed data and computational power, with an increase in the curiosity and population of humans, pushes us to make better devices [1]–[4]. The 5G technology, the IoT devices, all automation, the virtual reality, and the AI robots, these are the few examples of new technologies that need fetching and processing a large amount of data in real-time. With the current semiconductor electronic technology, these demands can be fulfilled up to some extent. The cloud and storage, the prediction of environmental behaviour, solving the electrochemistry for new drug discovery, for all these applications high-speed transmission and processing of the data is crucial [3], [5]. The optical fibres, optical interconnects, and nanophotonic devices are saviours devices for such problems [6], [7]. These devices are large and bulky and do not fit the demand for high integration on a single chip. The advancement in the photonics leads to a new branch i.e. Nanophotonic. This leads to the study of controlling and guiding light beyond its diffraction limitation [8]. These advancements gave the speed a new dimension leading to devices with THz bandwidth of operation with low energy consumption and high density of integration on a single chip [9], [10].

Nowadays, the speed of data centers and high-speed internet purely relies on optical interconnects. The integration of these photonic devices on-chip makes the per-bit data storage and processing much cheaper and faster. To meet the continuously increasing demand of these data centers, need continuous cooling as the electronics component produces a large amount of heat, leading to a decrease in the performance and increasing the cost per bit data processing [11], [12]. On the contrary, if the maximum parts are replaced with photonic

devices speed, reliability, and the cost per bit could have been improved. Figure 1.1 shows the various components of the photonic integrated chip [13]–[15]. To conclude, the integration of photonic devices on a single chip with electronics is one of the possible solutions to meet our demand for low power consumption high-speed transmission and processing of the data [16], [17].

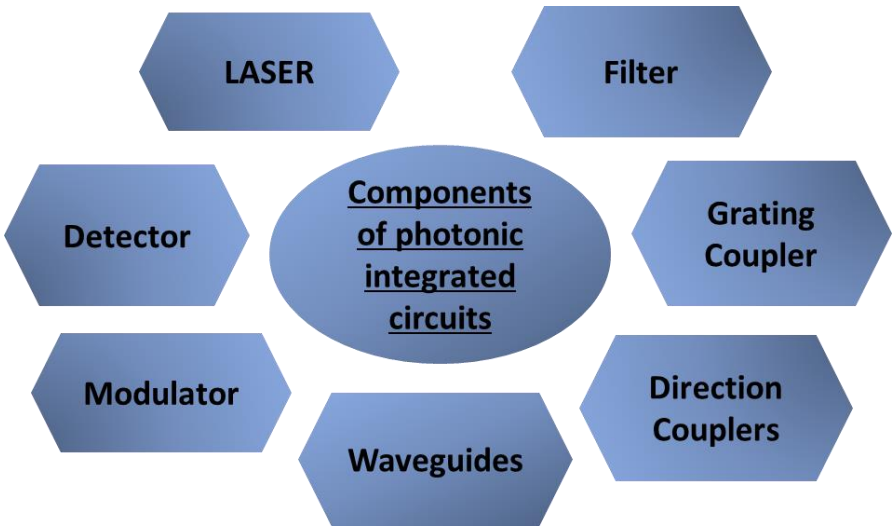


Figure 1.1 Image showing the main components of integrated photonic circuits.

1.2 Nanophotonic devices and applications

The photonic devices have already proven its importance in technology in the present scenario. The squeezing of the light beyond the half dimensions of its wavelength is still of vital importance [18]. Material and design engineering have able us to overcome these problems. The plasmons, slot waveguide, and photonic crystals are the few waveguides engineered device technologies along with the use of two-dimensional materials such as graphene and MoS_2 enable us to have devices much smaller than the dimensions of wavelength [19]. These devices still suffer from fundamental hurdles of propagation losses and crosstalk due to leakage across the nano dimension device. These hurdles are still hot topics of interest among researchers and

scientists. In these nanophotonic devices, the light-matter interaction is large. The larger the interaction, easy it is to control and make better functional devices with high efficacy. The devices like optical switches interconnects [20], modulators, polarization controllers [21], and memory [22], [23] devices are the few examples of such controlling and manipulating of the light using nanophotonic devices.

1.2.1 Nanophotonic waveguides

The guiding and controlling of the light beyond the diffraction limit is crucial to make the photonic devices comparable to the size of modern on-chip electronic counterparts. To overcome this hurdle various techniques were proposed by the researcher. The three basic waveguiding techniques i.e. Slot waveguide, photonic crystals, and plasmonic waveguide has shown tremendous potential in solving the diffraction limit problem. In this section, these three waveguiding techniques will be discussed followed by some few important waveguiding and controlling examples.

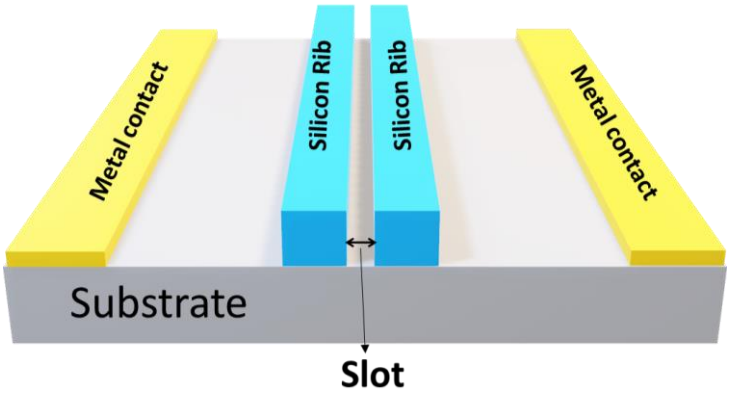


Figure 1.2 Silicon nanophotonic slot waveguide with metal contact has an application in optical modulation and detection.

Slot waveguide: The researchers have worked with various electro-optic materials to achieve high-speed changes in a light signal using the external electric field. The materials used for electro-optic

materials were not compatible with silicon. In 2004 Almeida et al. invented a way to confine light on SOI in a small gap between two ribs of silicon waveguide [24], shown in Figure 1.2. This type of structure results in partial confinement of light inside the gap. It experiences a large electric field in slot even with small voltage is applied across the two-silicon rib [25], [26]. The third benefit for such a structure is compatible with present silicon technology.

The slot waveguide has also shown its advantage in the application for optical sensing. The 70% of light in the slot waveguide interacts with the analyte surround it, which gives large interaction of analyte and light resulting in better sensing. On the contrary, a single rib waveguide allows only 20% of light interaction with the analyte [27], [28]. The strong light analyte interaction leads to large optical sensitivity, which motivated the researchers to work on optical sensing. To enhance the characteristics of the optical modulation, researchers started using other materials with slot waveguide on SOI wafers. Slot waveguide confines the high intensity of the light in a very narrow region. Infiltration of the slot region with electrooptic materials will leads to high-speed phase change modulators using Pockels effects [29]. This waveguide can further be used in Mach-Zehnder interferometers and ring resonators for intensity modulators [29]–[31]. The waveguide has an application in optical photodetection also. The tight confinement, small footprint, and high electric field inside the slot area make it better for use in nanophotonic modulators and sensing devices.

Photonic crystals: The periodical arrangement of material optical nanostructure that allows or stop a certain band of frequency is called photonic crystal. Yablonovich [32] and John [33] proposed a one-dimensional period structure which is an optical analogy to semiconductor bands. In 1997 [34] authors proposed these phenomena with a name photonic crystal in which the atoms of the material are arranged such that they allow or forbid a certain block of frequencies. These types of structures were future being investigated and researchers came up with an idea that we create a certain type of defect

in the crystal structure we can use it as a bandpass filter with tighter control over the optical frequencies [34], [35].

The photonic crystal can be one, two, or three-dimensional, as shown in Figure 1.3, depending upon the direction of periodicity. The one-dimensional crystals can be made by depositing an alternate layer of two or more materials. The two-dimensional photonic crystals can be fabricated using optical lithography and material deposition or by creating holes in a slab of material using anodization or FIB. The fabrication of three-dimensional crystals is a bit tricky; the researchers have reported the 3-D crystal using 3-D printers, some have used multiple layers of the 2-D photonic crystals deposited one over the other. The complications and the difficulties in the fabrication of these crystals made them less popular than the other nanophotonic devices. The one and two-dimensional nanophotonic crystals are the famous ones among the three. They are easy to fabricate comparatively and have a better controlling environment. These photonic structures can confine an extremely high field of intensity in the nanostructured device. They have proven to be amazingly effective in the application of biosensing and optical modulations.

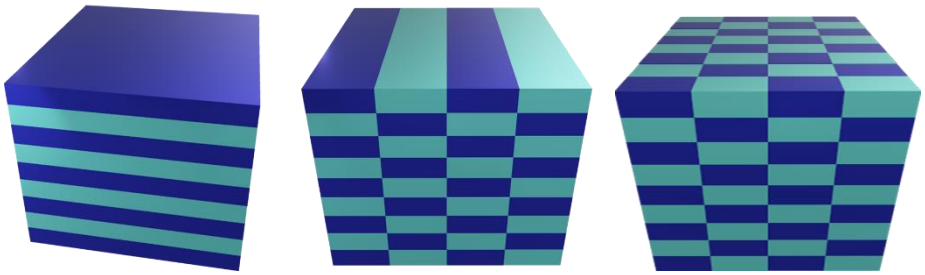


Figure 1.3Photonic crystal for nanophotonic waveguiding and optical applications.

Using the electro-optic materials with these periodically arrange nanostructures have proven its benefit in the field of sensing and optical modulation. It has been observed that the periodicity in the waveguide helps in slowing down the light with a great extent. These devices can be used in optical delay lines and memory devices. Despite

being difficult to fabricate these devices have proven its capability to be used in the filed for optical interconnects, optical data manipulation, delay lines, optical memory, bio-sensing using light, etc.

Plasmonic waveguide: Among various nanophotonic devices the most popular one is the plasmonic waveguide. Surface plasmons are the free-electron gasses on the surface of the metal. The incident electromagnetic wave over the surface plasmons can excite them which then start oscillating in sync with the incident electromagnetic wave, called surface plasmon polariton (SPP) [12], [36]. The SPP exists at the interface of metal and dielectric, where the real part of permittivity of metal should be negative and positive for dielectric material for the wavelength of the incident light. It also preferable that the magnitude of the real part of the permittivity of metal should be larger than the real part of dielectric permittivity. These SPP can be used to propagate the light signal along the waveguide. Using the plasmonic waveguide we can confine light or electromagnetic field much below the diffraction limitation, even in dimensions as small as few nanometres.

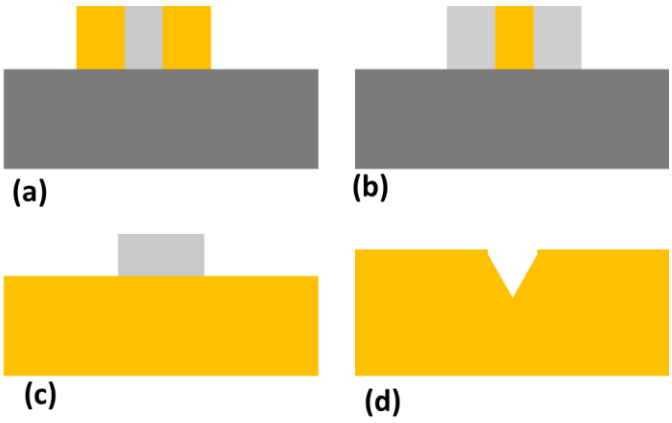


Figure 1.4 Various configuration of plasmonic waveguide (a) MIM (b) IMI (c) dielectric-loaded plasmonic waveguide (d) V grove MIM

Plasmonic waveguide usually suffers from large ohmic losses. To overcome this, researchers came up with various schemes such as MIM metal-insulator-metal, MIS metal insulator semiconductor, V grove MIM, IMI, etc., shown in Figure 1.4. The noble metals Au, Ag,

and Cu have shown a significant low loss in operating at NIR wavelengths. This scheme has a direct relation between material property and incident light which makes it easy to control and manipulate. These properties made plasmonic waveguide a better candidate for the on-chip nanophotonic device in the application of optical modulation and photodetection. Large light-matter interaction of plasmonic waveguide also made it eligible for the sensing application. To overcome various losses in the plasmonic waveguide researchers in 2007 proposed a hybrid device where the plasmonic losses are compensated by coupling the modes [37] i.e. optical mode and plasmonic mode resulting in hybrid plasmonic mode. Which is discussed in the subsequent sections of in this chapter.

Design application: Till now in this chapter we have discussed how to confine light in nano regimes. For practical use, it requires having couplers for coupling the light from the source to on-chip nanophotonic waveguides. To use optical phase modulators for a practical application like switches, intensity modulator, and sensing, the MZI (Figure 1.5) and ring resonators (Figure 1.6) can be used using above mentioned waveguiding mechanism. In this section, we will discuss these structures in brief.

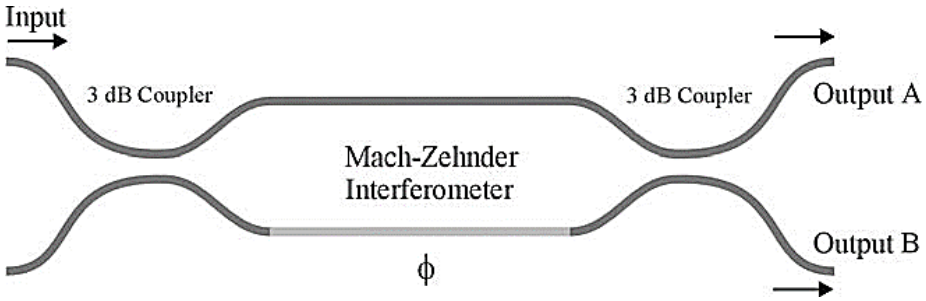


Figure 1.5 Basic MZI for the application in intensity modulators and optical interconnects.

The couplers are used as the interface for the light to couple from a light source to on-chip nanophotonic devices. The butt coupler, grating coupler, and inverted wedge coupler and parallel waveguides, etc are the few examples of such couplers. The butt coupled

waveguides are easy to use and fabricate, but large coupling losses occur due to alignment issues. The grating couplers use the subwavelength grating period. By changing the grating period and duty cycle the light can be coupled at a desirable angle. Coupling losses are small in grating couplers comparing to butt coupled waveguides as well as easy to align. Similar to these couplers, the inverted wedge couplers use butt coupling style where coupler width decreases from large to small near the waveguide which couples the light. Light can also be a couple if a waveguide is kept in the proximity with another waveguide with proper beat length.

The ring resonators use a parallel coupling waveguide to couple light from a straight waveguide to a circular shaped waveguide. The gap between the ring and the interaction length is kept such that the desired frequency can be coupled in the ring for further use. Mach-Zehnder Interferometer MZI splits the input light into two equal parts and combines them at the out. Based on the processing at the one branch of the waveguide, the phase difference results in the different intensity at the out of the waveguide.

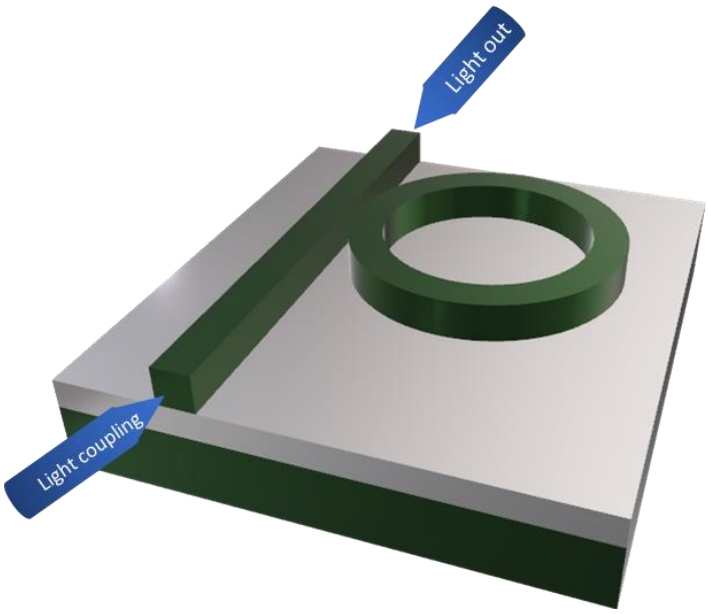


Figure 1.6 Image describing a basic structure for ring resonator.

1.2.2 Applications of nanophotonic waveguides

This section introduces the important applications of nanophotonic devices. In nanophotonic devices, the light or electromagnetic wave acts as an information carrier. The guiding and manipulation of light results in many practical applications such as optical modulator, photodetector, add-drop filter, beam steering devices, optical interconnects, optical memory, delay line, and biosensor, etc.

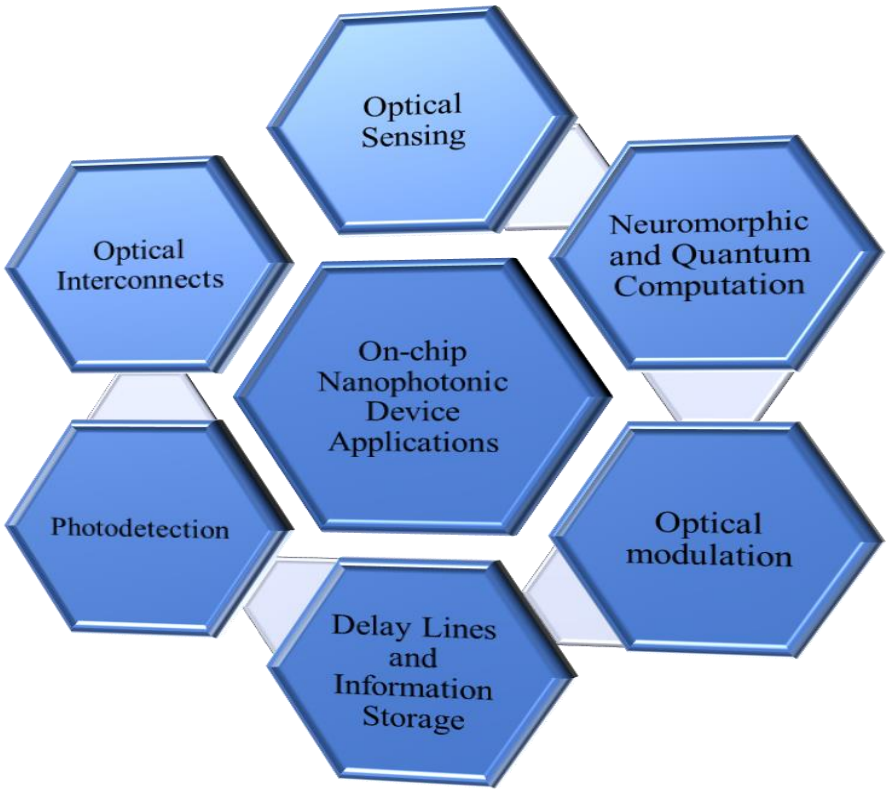


Figure 1.7 Application of on-chip nanophotonic devices.

For utilizing light as the information carrier for on-chip communication, it must be modulated, slow down, and stored. Various applications are shown in Figure 1.7. For the modulation of the light various techniques are involved. Based upon their physics involved they can be classified in electro-optic modulators, intensity modulators,

Pockels effect, electro-absorption modulators, liquid crystal modulators, phase modulators, acousto-optic modulators [38]. By changing the effective refractive index of the material in which light is guided the light can be modulated. In an acoustic-optics sound, a sound wave is used to change the amplitude or frequency or the direction of the guided optical wave. The liquid crystal modulators can be found in displays and for the pulse shapers. Among all these the electro-optic modulators are mostly used for the application in on-chip devices. These are the most energy-efficient and fast compared to other schemes. Electro-optic modulation uses the Pockels effect by changing the refractive index of the nonlinear crystal on the application of the external electric field. The material like lithium niobate (LiNbO3), lithium tantalate (LiTaO3) and ammonium dihydrogen phosphate (ADP) are few of the example that uses this effect. For CMOS compatibility Silicon is the choice of material, but to negligible nonlinear effect, the Pockels effect cannot be used in silicon-based devices. The plasma dispersion effect is used to modulate light in silicon like material [39], [40]. The effect uses the fact that on the application of the external electric filed the charge carriers i.e. holes and electrons displaces in bulk which leads to a change in the refractive index of the material.

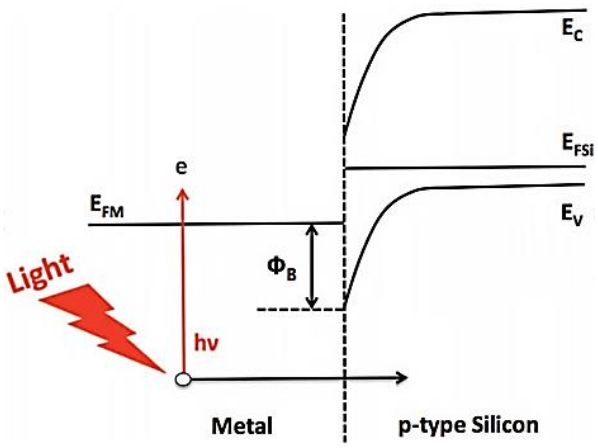


Figure 1.8 Energy band diagram of Schottky Junction explain photodetection in Silicon using Internal Photoemission.

To record the modulated optical signal photodetectors are required. Silicon provides an excellent platform for the monolithically integrated device on the same substrate [41]. Silicon is considered as one of the best choices for optical transmission, unfortunately, it has been neglected due to its bandgap of 1.12 eV [42]. It cannot detect the wavelength above 1.1 μm. A tremendous exploration has been done to use silicon in the NIR wavelength range. The internal photoemission (IPE) technique is one of the possible solutions for photodetection in Silicon [43], [44]. A Schottky junction is one of the devices used for the IPE based detection in Silicon, Figure 1.8. For NIR the most used materials are in with a combination of Silicon are Ge and III-V semiconductors [45]–[47].

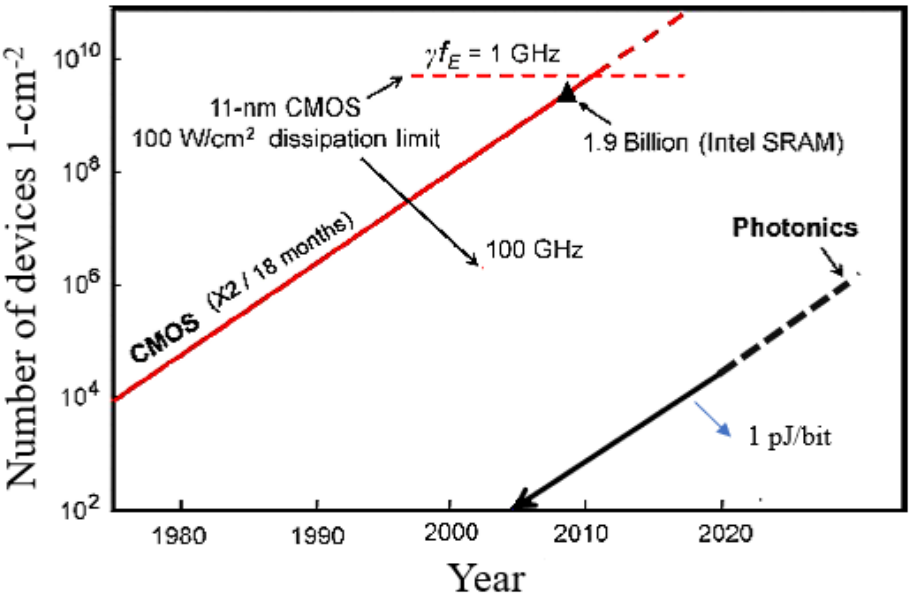


Figure 1.9 Increasing trend of number of CMOS and photonic devices per unit on chip area. Adapted from [48]

1.3 Recent trends

Photonic integrated circuits have gained tremendous attention and demand from tech companies because of their large bandwidth and low energy consumption. Making CMOS compatible integrated

photonic components is a hot topic among the researchers. The optical on-chip devices have compactness with high bandwidth of operation with high phase stability. These characteristics make them appealing for application in quantum computing. For the data centers and supercomputers, the optical interconnects are the key element in controlling the data transfer between two units. Figure 1.9 shows the trend of increasing number of CMOS and photonic devices per year on per unit chip area.

To achieve this high-density integration on a monolithic silicon chip, the major concern for scientists and researchers is diffraction limitation. Plasmonic devices, slots, photonic crystals, and material engineering has overcome this limitation. The following are the examples of state of art application using silicon nanophotonics. The smallest optical phases modulator with only 350-nm in footprint area and 56 MZI [49] were used to make programable CPU [50], Figure 1.10.

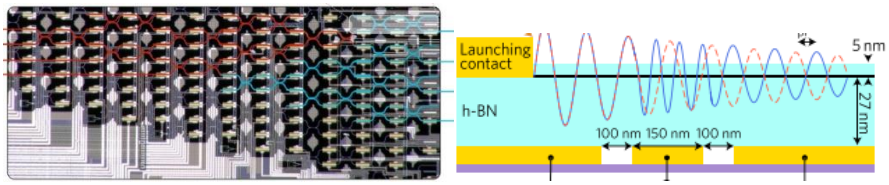


Figure 1.10 (a) 56 –MZI configuration programmable CPU [49] *(b) Smallest optical Phase modulator* [50].

1.4 Organization of the thesis

The thesis is organized in seven chapters starting with an introduction to integrated nanophotonics and literature survey, four major chapters consisting of the original research work followed by the conclusion and the future scope.

Chapter 2. Silicon-based nanophotonic waveguides and their applications: The second chapter covers the conceptual review of

nanophotonic devices including hybrid plasmonic waveguide, its application in modulation, and switches. It also discusses the important contributions in the area of nanophotonic devices for applications in resistive switching with optical readout and photodetection.

Chapter 3. Design, fabrication, and analysis of hybrid plasmonic waveguide: In this chapter, the proposed nanophotonic waveguide based on the concept of hybridization of plasmonic and photonic modes (Hybrid plasmonic waveguide) is designed and fabricated. The role of the high-index layer of silicon to control vertical and lateral confinement is studied. The wavelength 1550-nm is confined in an only 10-nm thick layer of low index material with an acceptably low loss of 7 dB/cm in a 350-nm wide waveguide with a mode character of 0.5. The chapter also discusses the role of introducing grating in the high index layer for ultra-low dispersion which also crosses ‘zero-dispersion’ many times over a broad range of wavelengths.

Chapter 4. Guiding and controlling light at the nanoscale in field-effect transistor: The chapter proposes a field-effect transistor-based device to control light in Hybrid Plasmonic Waveguide (proposed in the last chapter). Metal-oxide-semiconductor field-effect transistor and tunnel field-effect transistor are used to create a plasma dispersion effect, which in turn modulates the light in nanoconfinement with a very small mode area of $\lambda^2/100$. A π-phase shift is achieved at a length of 204 μm. All the waveguiding characteristics along with phase and intensity modulation are analyzed.

Chapter 5. Electrically writable silicon nanophotonic resistive switch: This chapter focusses on the design, fabrication, and characterization silicon-based nanophotonic resistive switch. To improve the control over the nanoconfined light (1550 nm) in a hybrid plasmonic waveguide, the mechanism of resistive switching is used. A clear optical extinction ratio of 10-dB is achieved, with a low power

consumption of 0.15pJ for one cycle. The transport mechanisms governing each resistance state are studied and discussed. The metal diffusion and formation/deformation of the conduction bridge is experimentally analyzed.

Chapter 6. Light assisted electro-metallization in resistive switch device with optical accessibility: This chapter presents material-analysis and device fabrication for nanophotonic resistive memory. The conduction mechanism involved in the resistive switching effect is also studied to provide an optically assisted nonvolatile resistive memory device. The three-layered device has shown a large hysteresis current loop in the presence of a blue wavelength of visible light at lower voltages. The SET voltage decreases from 10 V to 4 V on the application of visible light. The electrical resistive state of the device is read out at 1550-nm of wavelength.

Chapter 7. Conclusion & Future scope: In this chapter, all the contributions are summarized, and the relevant future scope of the work is briefly discussed.

Chapter 2

Silicon Based Nanophotonic Waveguides and their Applications

2.1 Importance of silicon nanophotonics

The silicon nanophotonic has gained huge attention in the last few years primarily because of its two benefits, first is compatibility with complementary metal-oxide-semiconductor (CMOS) and mature silicon foundries. Silicon gives us the benefit of high-density monolithic integration on-chip. Due to its high refractive index silicon is widely used to make passive photonic devices. It has strong optical confinement which enhances the Kerr nonlinear process. The mature Si technology enables the low-cost manufacturing of the device and easy to realize device design. The silicon photonics has been used as stimulated Raman scattering for gain in lasers and amplifiers, for nonlinear mixing for optical parametric amplification (OPA) [51]. Silicon has an indirect bandgap but still [52], [53] has shown silicon can be used as light sources with Erbium-doped, photonic crystal cavity with large Q and small V. These properties have shown application in spectroscopy and single-molecule detection. It has also shown application with biological spectroscopy using waveguide coupling interferometer, biomolecule bind on the Si waveguide resonator, and by wavelength shift in the resonant frequency. Silicon photonics is the primary application for solar cell applications for increasing the efficiency of solar cells [54]. The new era with silicon photonics is in quantum optics has been started [35] for quantum computations. But Si photonics have few challenges such as it has no Pockels effect hence difficult to modulate but plasma dispersion can be used instead, it has an indirect bandgap but by doping and using nanowires lasing can be achieved, and also due to diffraction

limitations photonic devices has a large footprint on a silicon-chip platform which can be overcome using plasmonic physics [8], [12], [36], [55], [56].

2.2 Plasmonic waveguides

The dimensions of the photonic waveguides are limited by the diffraction limit of the light. For rectangular silicon rib waveguide dimensions are limited with a width of 450 nm and a height of 220 nm for the 1550 nm of wavelength. This footprint is quiet a large compare to recent nanotechnology. To guide the light beyond this limit surface plasmons polariton can be used. Plasmons are the bunch of free charge carriers at the interface of the metal. These plasmons can be coupled with the electromagnetic wave that is incident on it and starts resonating with the same momentum and wavelength as that of the light. This property of the plasmons can be harness in the nanophotonic waveguiding where light is coupled in a few nanometres wide waveguide. In the subsequent section of this chapter, we will discuss plasmonic waveguide, SPP, and various losses in the plasmonic waveguides. Further, the discussion will continue with how these losses are compensated. The section of the thesis also thesis how large light-matter interaction can be used for controlling light at the nanoscale.

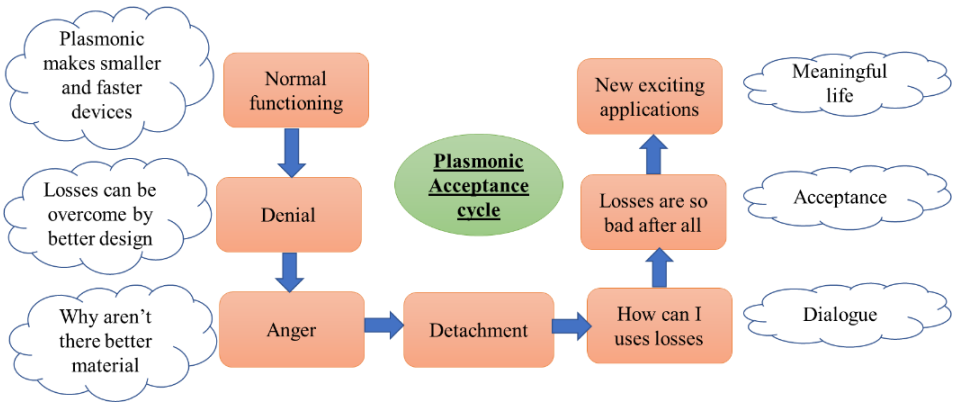


Figure 2.1 The figure shows the acceptance of plasmonic in the field of research, adapted from [54]

2.2.1 Surface plasmon polariton

The study of plasmonics deals with the generation, control, detection and plasmons as information carriers. Plasmons are the collection of charge carriers with quanta energy of $\hbar\omega_{p,}$ where ω_p is the plasma frequency and $\hbar$ is the Planck's constant. The plasma frequency is the effect on the plasmons characteristics on the application of an external electric field given by

$$\omega_p = \left(\frac{n_e\, e^2}{m_e\, \varepsilon_o}\right)^{\frac{1}{2}} \tag{2.1}$$

Where e is the electrons electric charge, m_e is the effective mass and n_e id electrons density. The carrier density of metal is usually 10^{22} cm^{-3} and for highly doped semiconductor is 10^{19} cm^{-3}. These high density of electrons acts as plasmons which oscillate at plasma frequency $\omega_{p,}$ typically for metal its value is 10^{15} Hz. At the interface of metal and dielectric, the interaction between plasmons and photons results in surface plasmon polariton (SPP), Figure 2.2. The surface plasmon polariton SPP can bound the light in a few nanometres at the surface of the metal interface [57]. This can be utilized to reduce the size of the photonic device up to much extent. This high field localisation of the light can be used for the application in biosensors, a nanophotonic waveguide with electric control and photonic detectors can be realized. Thus, the SPP combines the benefit of the electronics and photonics to realize the nanophotonic devices.

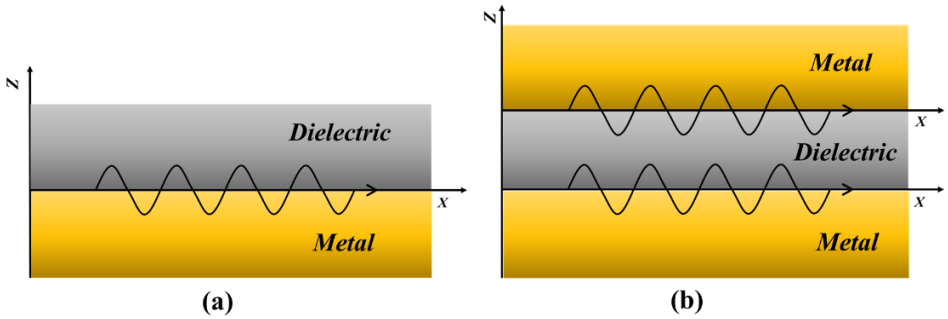


Figure 2.2 The diagram showing propagation of SPP at (a) metal dielectric interface for MI (b) in MIM this two SPP wave couples resulting in better confinement and propagation.

2.2.2 Energy-momentum dispersion of SPP modes

The dispersion relation for a propagation photon wave in a vacuum is shown in figure 2.3, $k^2=\omega^2/c^2$, where '*k*' is the wave vector and *'c'* is the speed of light in the vacuum. The dispersion relation for the planar metal-dielectric surface the dispersion relation can be given by

$$k(\omega) = \left(\frac{\omega}{c}\right).\left(\frac{\varepsilon}{(\varepsilon + 1)}\right)^{\frac{1}{2}} \qquad (2.2)$$

Considering ideal cases of metal permittivity, the frequency is zero at k=0 and approaching the asymptomatic value $\omega_{spp}= \omega_p /\sqrt{2}$ at $k \rightarrow \infty$. In this frequency range for the metal, the real part of permittivity is negative which makes possible the formation surface plasmon polariton. In Figure 2.3 the upper blue branch is for the bulk plasmons.

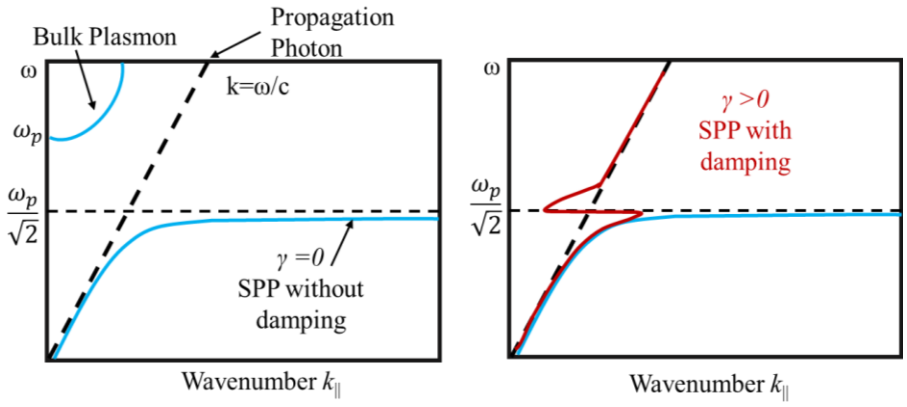


Figure 2.3 the dispersion relation for the plasmons in metal surface and bulk. (a) the ideal case when no loss in metal (b) red line shows relation when metallic losses are taken into consideration.

The SPP guided at the metal-dielectric interface is shown in Figure 2.4. The material at z>0 is dielectric in nature with a permittivity of ε_1 and the z<0 is metal with permittivity of ε_2. The figure shows the surface charge distribution in the direction of surface plasmon propagation in the y-direction. The surface plasmon supports the transverse magnetic TM profile.

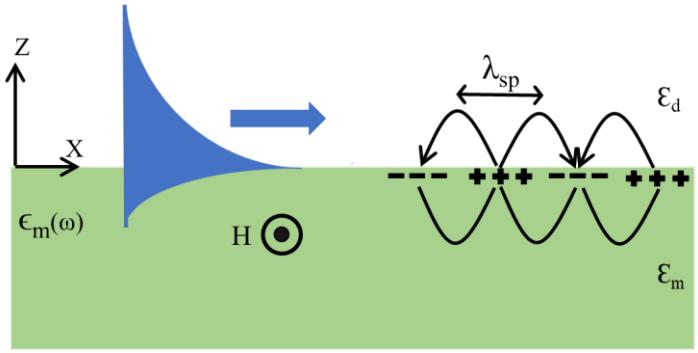


Figure 2.4 Schematic showing the plasmon oscillation at the interface of the metal and the dielectric.

The dispersion relation for the metal-dielectric interface is the same as equation (2), but with dielectric constant ε_1 instead of air.

$$\beta = k_o \sqrt{\frac{\varepsilon_1 \varepsilon_2}{\varepsilon_1 + \varepsilon_2}} \tag{2.3}$$

Where, $'k_o = 2\pi/\lambda_0'$ is the free space wavenumber and β is the propagation constant. The Drude model [58] gave the expression for lossless metal-dielectric permittivity given as

$$\varepsilon_2 = 1 - \frac{\omega_p^2}{\omega^2} \tag{2.4}$$

ω is the angular frequency of the light ω_p is the plasma frequency of the metal. Substituting the above two equation dispersion relation is given by

$$\beta = k_o \sqrt{\frac{\varepsilon_1 \left(1 - \frac{\omega_p^2}{\omega^2}\right)}{\varepsilon_1 + \left(1 - \frac{\omega_p^2}{\omega^2}\right)}} \tag{2.5}$$

As ω approaches the surface plasmon resonance ω_{sp} ; $approaches$ infinity $\omega_{sp}$is given by

$$\omega_{sp} = \frac{\omega_p}{\sqrt{1 + \varepsilon_1}} \tag{2.6}$$

This condition is known as surface plasmon resonance. Near the surface plasmon resonance frequency, the wave greatly slows down and the extent of the field on either side of the interface becomes vanishingly small.

2.2.3 Losses in plasmonic waveguides

The plasmonic waveguide suffers from various metallic losses due to radiative and dephasing by inter electron collision and by generating hot electrons. These hot electrons radiate their energy to nanostructures nearby losing all energy. Which leads to high losses and small propagation length in the plasmonic waveguide. These energy dissipation of SPP leads to localized heating of the on-chip devices. On the other hand, this localizing of the high intensity can be used for the application in spectroscopy and sensing applications, various applications are shown in Figure 2.5. For the ideal dielectric metal interface, SPPs are non-lossy to conserve the momentum. From dispersion relation, it can be concluded that the SPP has large momenta i.e. shorter wavelength at the same frequency. But to achieve this high momentum the interface of two materials should be smooth and there should not be any losses due to material absorptions.

The dispersion relation discussed in the previous section is considered for an ideal case where no metallic loss is present. The permittivity plasmon should consider the effect of external potential on the electrons and the potential by the internal crystal structure, the effect of nearby electron charges, and decay of collision (Landau damping). By considering all these parameters Drude gave a new formula for permittivity as:

$$\varepsilon = 1 - \frac{\omega_p^2}{(\omega^2 + i\gamma\omega - \beta k^2)} \tag{2.7}$$

Where γ is the damping parameter, which defines the lifetime of collective oscillation of the electrons, β is the Landau damping process. Some of these losses are unavoidable but can be compensated by different waveguiding structures. One of the schemes was proposed by [59] where the leaky optical mode is coupled with plasmonic mode to compensate for the losses resulting in hybrid plasmonic mode. The

subsequent section discusses the various structure proposed by researchers on similar schemes.

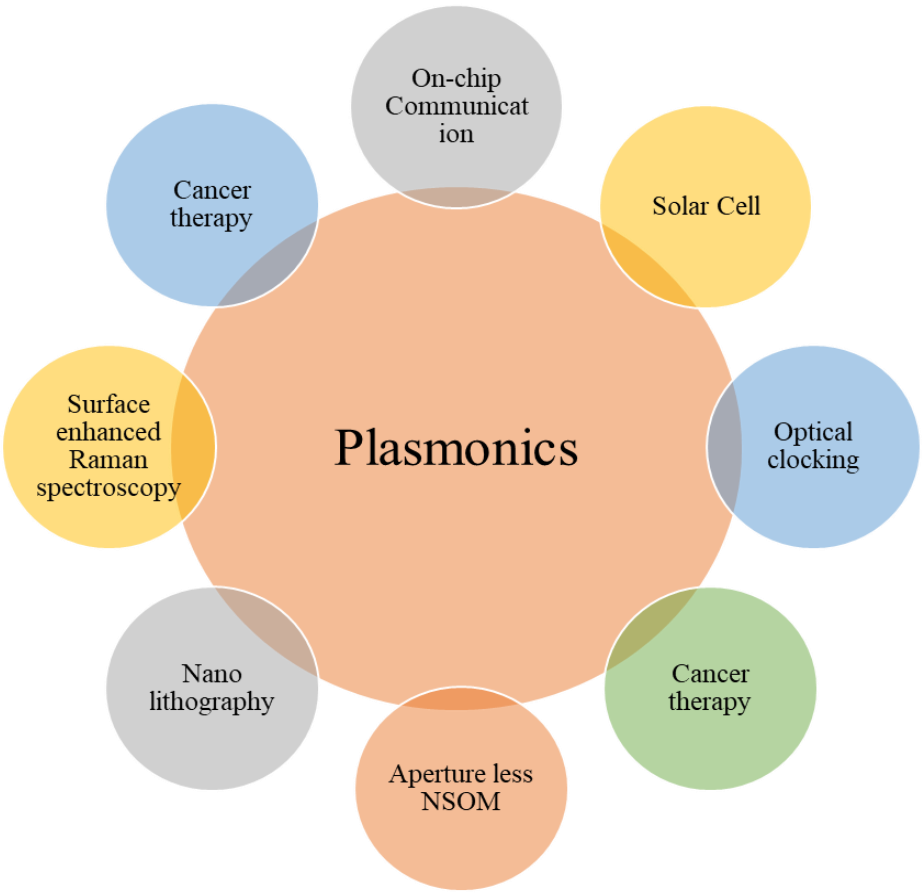


Figure 2.5 Various applications of the plasmonic waveguide.

2.3 Hybrid plasmonic waveguide

The solution to the problem of large losses in the plasmonic waveguide can be solved by coupling the guided SPP with the leaky optical mode, resulting in a hybrid plasmonic waveguide [59], [60]. The Hybrid plasmonic waveguide is a combination of two waveguides i.e. dielectric waveguide and plasmonic waveguide. Both the waveguide is stacked such that only leaky optical mode travels from the high index layer coupled with the plasmonic mode. The usual configuration for the hybrid plasmonic waveguide consists of low

index material separating the metal layer and the high index semiconductor layer shown in Figure 2.6.

The configuration provides the benefit of both the waveguide i.e. low loss propagation of the signal and tight confinement in nano low index material. Because of these benefits, the hybrid plasmonic configuration has attracted the attention of researchers and scientists in the field of integrated photonics. The plasmonic waveguide has also coupling issues i.e. coupling the light from the source to the plasmonic waveguide. The HPW has also solved this issue in many configurations of the waveguide. The large light-matter interaction also helps in this waveguide for the application in optical modulation through the external electrical electric filed. The subsequent section discusses some of the waveguides and devices proposed using hybrid plasmonic configuration.

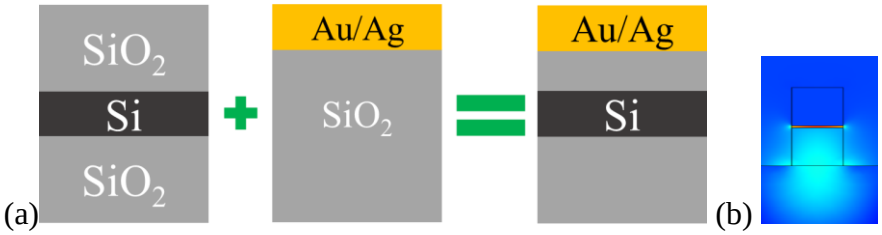


Figure 2.6 (a) Hybridization of Silicon photonic waveguide and plasmonic waveguide resulting in the hybrid plasmonic waveguide. For the communication wavelength 1550-nm the Au and Ag are the best choices of metal (b) Mode profile showing the maximum intensity of the hybrid plasmonic mode in the dielectric layer.

2.3.1 Introduction to hybrid plasmonic waveguide

Hybridization of optical mode and plasmonic mode leads to hybrid mode. The hybrid plasmonic waveguide has a low loss and tight confinement of the electromagnetic field with a small foot area of the device. This concept was introduced by M.Z. Alam et.al. [37] at a conference in 2007. Later on, taking inspiration from it a detailed

analysis was published by R. F. Oulton et.al. [59] in Nature Photonics in 2008, where they have taken a high index layer in cylindrical form spaced from the metal layer by some gap filed with low index dielectric material, Figure 2.7. They demonstrated that when the gap is reduced significant enough between the high index layer and metal, a strong electromagnetic field is confined between the two. They also demonstrated that the high index layer should be small enough that it allows only leaky optical mode flow through it. As the concept has reduced major drawback of the plasmonic waveguide while keeping the nano dimensional confinement of the filed researchers started admiring the concept for its application in on chip devices.

The Xiaodong Yang et.al. [61] have shown that due to the strong coupling of the two modes in HPW, the optical force that is exerted on the high index waveguide is stronger than that of the dielectric photonic waveguide. They have also shown that the optical trapping force at the nanoscale on a single particle is much stronger which enables its application in optical tweezers, for light manipulation and biosensing, [62].

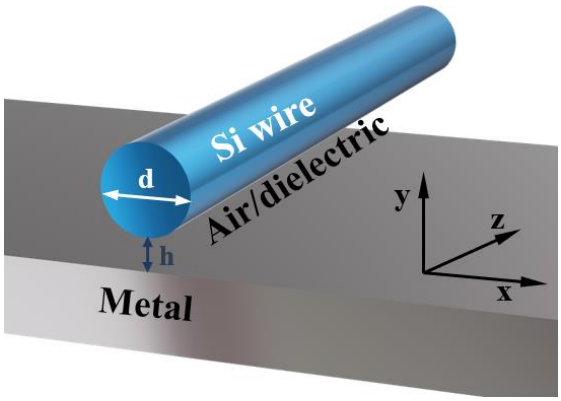


Figure 2.7 Schematic of the proposed concept of hybrid plasmonic waveguide

The mode factor defines the quality of the hybrid mode. The equation (8) gives the mode factor [59]. It defines the figure of merit in terms of how much SPP energy and Optical energy couples together.

$$|a(d,h)|^2 = \frac{n_{hyb}(d,h) - n_{spp}}{(n_{hyb}(d,h) - n_{cyl}(d)) + (n_{hyb}(d,h) - n_{spp})} \qquad (2.8)$$

|a| is the mode factor for the hybrid plasmonic waveguide n_{hyb}, n_{spp} and n_{cyl} are the effective refractive index of the hybrid mode, metal-dielectric plasmonic mode and optical mode respectively.

$$A = \frac{1}{max\{W(r)\}} \int W(r)dA \qquad (2.9)$$

The effective mode area is given by equation (9). It defines the area of maximum energy density. W(r) is energy density per unit length along the direction of propagation. The true figure of merit for hybrid plasmonic mode is defined by the ratio of how long the light can travel and how tightly the mode is confined in the waveguide. The FOM is given by

$$\text{FOM} = \frac{L}{\sqrt{A_{eff}}} \qquad (2.10)$$

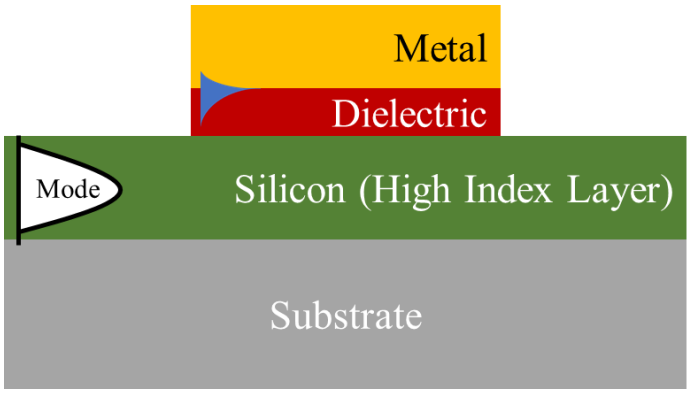


Figure 2.8 The Schematic showing how the coupling issues in the plasmonic waveguide can be resolved using the high index layer as the primary waveguide and the plasmonic waveguide in parallel to the silicon rib waveguide.

2.3.2 Electrical control of optical signal in hybrid plasmonic waveguide

Electrically control of light at nanoscale is an absolute necessity for on-chip optical devices. The optical switches and electro-optic modulators are the main components of any photonic integrated circuits. Silicon has a week nonlinear effect and at 1550-nm the silicon has high transmission and low absorption hence difficult to modulate light in silicon-based electro-optic modulators. Increasing silicon-based modulator length can help in modulation but device size will not be suitable for on-chip devices. Micro-ring resonators, MZI and silicon hybrid material-based modulator can be the possible solution for reducing the modulator size. These schemes have the drawback of low fabrication toleration, works in a narrow bandwidth of operation and temperature sensitive. A plasmonic waveguide is a possible solution to overcome these limitations of a large footprint. Combing the benefits of plasmonic and silicon devices i.e. using hybrid plasmonic waveguide various optical modulators and switches have been proposed [86–90].

A hybrid plasmonic waveguide-based modulator is experimentally demonstrated by Sorger et. al. [63]. The three-layer device has an Au-ITO-Si configuration. When the electric field is applied on the top metal the charge accumulation in the silicon layer is formed. The greater number of charges absorb the light intensity and also effects the phase of the light. They have demonstrated phase and intensity modulation by plasma dispersion effect and using changes in refractive index ITO. The researchers have also shown optical modulation in the hybrid waveguide by using phase change materials (e.g. vanadium oxide). VO_2 changes from n = 3.243+0.3466i for the insulating phase to n = 1.977+2.53i in the metallic phase at a wavelength of 1550 nm. These devices have shown a large depth of field. Due to changes in materials takes time the modulation speed is slow in this type of modulators.

Joushaghani et al. have also demonstrated a VO_2 sub-volt hybrid plasmonic switch [64]. The device is fabricated by depositing a sliver of 300 -nm on silica space on VO_2. They have shown a change in mode profiles which is accompanied by a large change in propagation losses. They have predicted driving voltage for the device is 4.6 V and the total energy consumption is only 2.6 fJ/bit.

Similarly, Sun et al. have proposed a modulator that consists of an Ag-Polymer-Si-Polymer-Ag structure [89]. They have used the two-slot design of the hybrid model. They act as a coupler in the same waveguide by exchanging energy between the two spacers, this affects the overall modulation. They have shown a 16% transmission to a 1% transmission. They have shown a modulation bandwidth of more than 40 GHz with a power consumption of 0.27 mW. Li et al. have demonstrated 16-QAM modulation using HPWG [65]. They have used nonlinear medium in place of the dielectric layer as a spacer. They reported that device size will be less than 100 μm with a modulation bandwidth of 1 THz.

2.4 Nanophotonic restive switch

The transistor-based electronics is approaching its scale down limits. The channel length has to be small to fit a large amount of the transistors in a small footprint area. This shrinkage has caused difficulty in manipulating the flow of electrons in logic and memory devices. In 2008 [66] has demonstrated that a two-terminal device acting as a memory device by storing the information in terms of resistance change. They called it as memristor, and some time is also called a resistive switch. The researchers have demonstrated its application in the computing component as well as for the memory unit. The switching occurs usually by changing the crystal structure or formation of ion's conduction bridge with the influence of external electric field, magnetic or by changing the temperature. These are not limited by the transistor scaling and their multitasking capability

allows them for high-density packing on a silicon chip, they can be arranged in crossbar arrays Figure 2.9. Silicon-based resistive switches have also been demonstrated [67]–[70] which are CMOS compatible. Some of the resistive switches have shown inherent stochastic nature, allowing them for the application in the neuromorphic computations [68], [71]–[73]. The device has been used for application as Resistive Random-Access Memory (RRAM) [74]. The Restive switch can be fundamentally scaled down to 10-nm size. They have shown to retain memory for years. The also provides high switching speed with high endurance i.e. large read-write cycles. It has been shown that these devices consume much low energy. All these properties made them attractive and a lot of research has been started using these devices and studying the fundamental mechanism of the working.

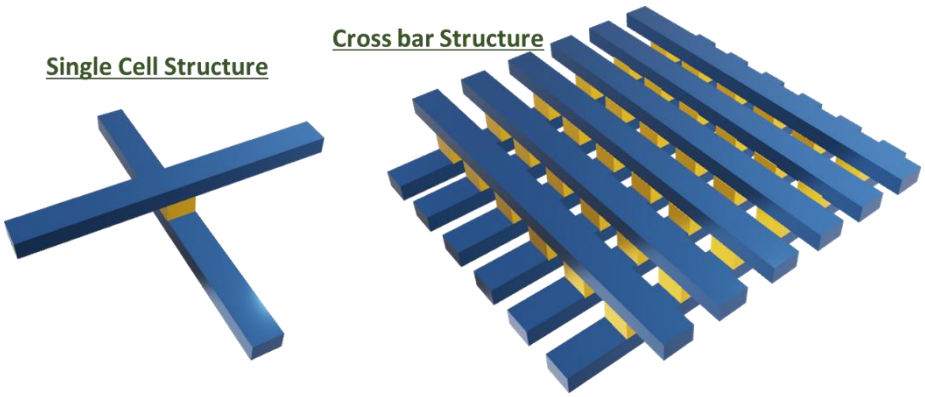


Figure 2.9 Schematic showing single element and crossbar array of resistive switch. Controlling (yellow) material is sandwiched between (blue) metal contact terminals.

In resistive switch changes occurs usually at nanoscale. The plasmonic waveguide has the similar device configuration as that of the resistive switch. Combining these two we can harvest the benefits from both technologies. The large bandwidth of optical signal and nanoscale changes on the influence of external field. The applications have been reported where the optical signal is used to control the resistive switch and the optical signal being controlled by the mechanism involved in the resistive switching.

2.4.1 Resistive switch mechanism

The resistive switches are the two terminal devices which regulates and control the flow of the current through the control layer. They also remember the charge flow through them. The typical resistive devices have two high conducting electrodes which sandwiches controlling/storage layer usually dielectric in nature. On the application of external stimuli, such as electric field or temperature variation, make some changes in the active controlling sandwiched layer. The characterization of the resistive switch/memory device has shown that the formation of the conduction bridge (CB) is due to the ion migration and redistribution. The IV hysteresis curve for volatile and non-volatile restive switch is shown in Figure 2.10. The based on the origin of these ions the mechanism are reported anionic based and cationic based. The formation and annihilation of the conduction bridge can be abrupt or gradual depending upon the mechanism of the formation of the CB. The speed of the device relied on these mechanisms. Depending upon the retention characteristics the resistive switch can be volatile or non-volatile in nature.

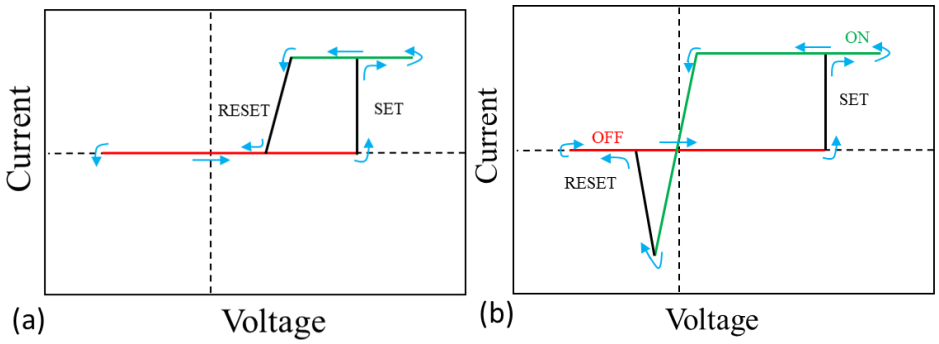


Figure 2.10 The IV characteristics of resistive switch, showing hysteresis curve of (a) volatile memory (b) non-volatile memory.

The mechanism can be distinguished based upon the filament localization, physical changes during formation of the CB. Based on the filament localization can be further distinguished in two parts: single filament model and area distributed process. Single filament

model has better control over the formation of the filament. The device is fabricated such that the formation of the filament only takes place at a location. These devices have deterministic behaviour but are difficult to fabricate. The devices working on the single filament models SET at lower voltages as the filed localization is very at the point of the CB formation. On the other hand, the area distributed model has multiple places to form the CB. Their behaviour is stochastic in nature. These devices easy to fabricate but the device characteristics repeatability is poor. Usually field is distributed over large surface area hence required large voltage compare to single filament model.

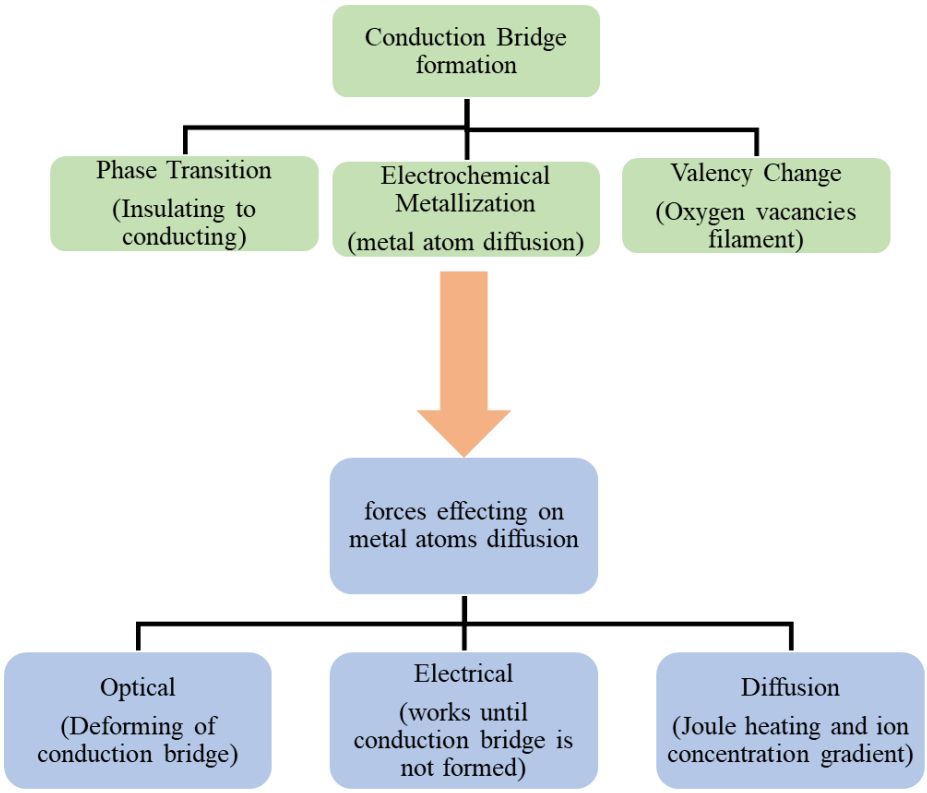


Figure 2.11 Different types of mechanism of Resistive switch.

Figure 2.11, shows resistive switch mechanism type distinguished based upon the physical changes in the controlling layer. When the high electric field is applied across the controlling layer (usually dielectric), physical changes result in change in the resistance from high to low and vice-versa. In Phase transition mechanism the controlling material changes itself from insulating to conducting by

joule heating or other mechanism. In Valency change effect, usually involves oxides materials, the material breaks itself in oxygen ions and the ions align themselves with direction of the applied filed providing low conductance path between the two electrodes. The third mechanism which is widely used for optical control using resistive switch is electro-chemical metallization. On the application of the electric field the electrode atoms (metal) gets ionized and start to diffuse into the buffer controlling layer. When the atom reaches the lower electrode the conduction path completed, and the effect of electric field stop bothering the atoms diffusion. The joule heating also helps in the diffusion of the atom in ECM mechanism, whereas when external optical light is shined it applies forces in the opposite direction. As the mechanism involves direct involvement of the metal atom and it absorbs the light it has shown its application in optical switches. The effect of nano changes can be used in nanophotonic devices for optical control. The next section discusses the electro-optic interaction.

2.4.2 Electro-optic interaction

The plasmonic or hybrid plasmonic waveguide has direct interaction of optical signal with plasmons from the materials used for SPP. This interaction can be harnessed for the manipulation of light in nanophotonic devices. The possible solution for manipulation is using resistive switch mechanism, as in these resistive switch material properties changes resulting in either change in refractive index of the material or increase in absorption. Another possible reason of the change in light is increase in irregularity or defects when a CB form or deform. When the conduction bridge is formed a large current start to flow which alters the path of the SPP, might be one of the reasons. Upon interaction with light in some material the electron hole pair generates they effect the mechanism of the formation or conduction bridge. The light may also affect by change in resonance condition in

some waveguide due to the resistance changes. These effects may all be affecting or combinations from them. The next section discusses the some of the application proposed by other researchers in electro optic resistive switch.

2.4.3 Optical resistive switch

Among the four-mechanism explained in resistive switching the electrochemical metallization, the phase transition effect and valency change effect has shown change in optical signal when made it propagate through the switching area. Whereas with the phase change effect the optical manipulation in resistive switch is not reported till now. Here are some state of art example for the optical manipulation with resistive mechanism.

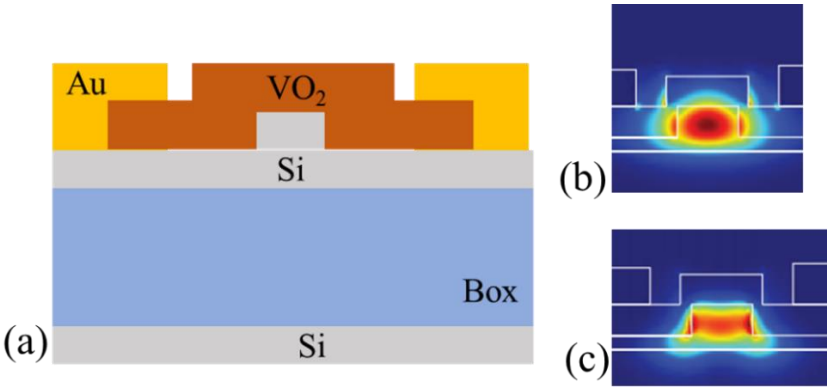


Figure 2.12 (a) Schematic of Si-VO_2 based optical switch. (b) Optical mode in Si rib when electrically OFF state. (c) Optical mode in Si rib when electrically ON state, behave like plasmonic mode MIM waveguide.

Phase transition effect: The phase transition of active material VO_2 vanadium dioxide is used electrical switching. The changes in the phase of material can be achieved by substrate heating, optical absorption, electric field [75]–[81]. The active material VO_2 is placed between Gold and Silicon rib waveguide [64], Figure 2.12. The optical signal is propagated through silicon rib. On the application of external electric field, the at a voltage of 6 V the insulator material changes its

phase from insulting to metallic phase. The effect of this change can be seen in the optical output. As the VO_2 becomes metallic in nature it starts behaving like plasmonic waveguide and most of the optical energy is absorbed by the waveguide. They have reported an optical extinction ratio of 5 dB. When the device is off, optical output have high intensity, photonic like shape in silicon rib and when it is electrically on the mode shape become like MIM plasmonic in nature shown in Figure 2.12 and most out optical intensity is low. Due to the slow change in the change in the physical state of the material due to the joule heating effect the device overall behavior is slow in nature and it is volatile. The size of this device is 3 times smaller Si and hybrid Si based electro absorptive modulator.

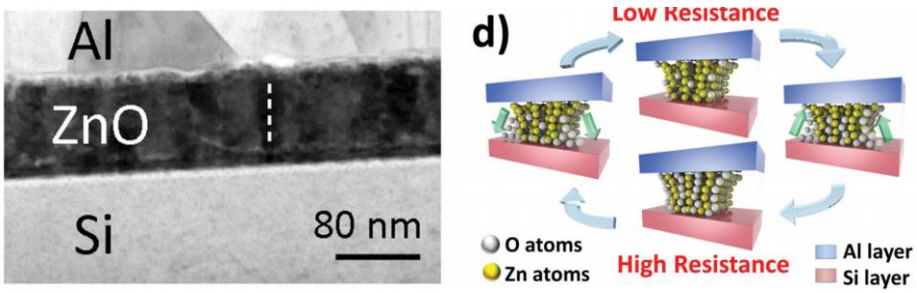


Figure 2.13 The TEM image showing the oxygen ions forming the conduction bridge. Adapted from [82]

Valency change effect: The optical switching by change in the oxygen ions in the active layer. The [82] proposes MIS metal insulator semiconductor-based device. Where the light is guided in ZnO insulator layer and the metal is Al and bottom layer is Silicon. The ZnO is 80 nm thick layer, shown in Figure 2.13. When electric field is applied the oxygen-ion breaks from ZnO forming the conduction bridge. This change in the material results in the optical intensity change at the output. They have reported extinction ratio ER of 0.35 dB. The low extinction is due to the noninvolvement of the metal atoms comparing to ECM based device and the example shown above. They have reported this as nonvolatile memory.

Electrochemical metallization: Resistive switching with electro metallization has shown very high optical extinction ratio due to the involvement of the metal atom diffusion. The [83] has proposed device using hybrid plasmonic waveguide that shows also has hysteric electric curve for resistive switching, Figure 2.14. Metal dielectric semiconductor-based device where top metal is silver followed by amorphous silicon and Silicon rib waveguide. The 1550-nm wavelength of light is guided in the waveguide. As the electric field is applied to the top metal the sliver metal atom starts to diffuse in the a-Si which blocks and absorbs most of the light intensity resulting in optically off condition. They have slowly swept the voltage from -3V to 9 V and recorded optical as well as electrical hysterics curve. The modulation depth of 1% is achieved which is enough for the optical memory application. The device is nonvolatile reset its resistance state in negative cycle.

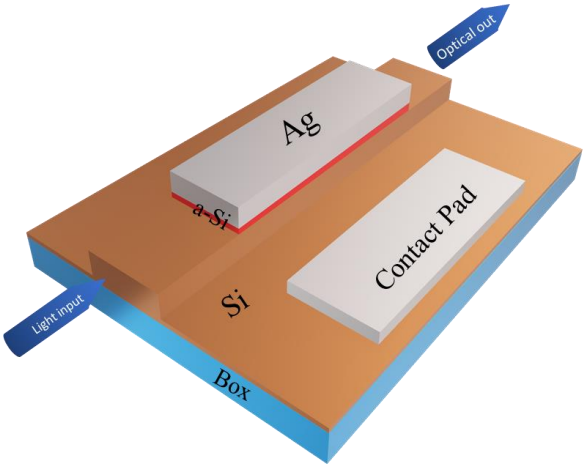


Figure 2.14 Schematic of Ag-a-Si-Si resistive switch with optical readout.

Atomic scale resistance switching: The process of single filament model is difficult to demonstrate. To define such schemes the model must include electronic transport coupling, electrochemical reactions and the diffusion of ions [72, 73]. They [53] demonstrated the atomic origin of resistance. The have Pt-Ag on silicon Rib waveguide separated by small gap of few nanometer [84], Figure 2.15. When high electric field is applied in small gap the metal atom diffuses which

block the path of optical signal. These schemes have better characteristics, but the fabrication is difficult to control.

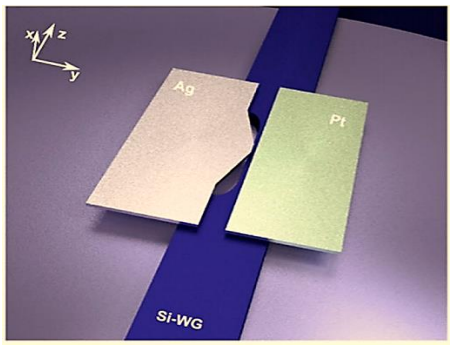


Figure 2.15 Atomic scale metallization resistive switch. MIM device Adapted from [84].

2.4.4 Photodetection with resistive switch

A discussed above the optical signal effect the mechanism of the resistive switch which can be utilized in many applications. One of them was proposed with photodetection capability by [85]. They have reported resistive switching in ZnO/p-Si heterojunction with ITO as the top electrode, Figure 2.16. The ITO is transparent to visible light. When the electric field is applied across the two electrodes the devices behave like a normal resistor. As the light incident on the device, it starts behaving like a resistive switch. The extra electron-hole pair generated in the devices makes helps in forming the conduction bridge. They have reported that the device avoids the undesirable overshoot of the current in the device. The filament growth when light shine of wavelength 532 nm is demonstrated by [85].

A light-controlled resistive switching memory was proposed by [86]. They have shown that light can add an extra parameter in controlling the resistive switch. When the light was shined on $Pd/Al_2O_3/SiO_2$ the photocurrent results in lowering the resistance a further step. The proposed that the device has a multilevel of resistive switching. The application is in the multifunctionality of the device using photocurrent.

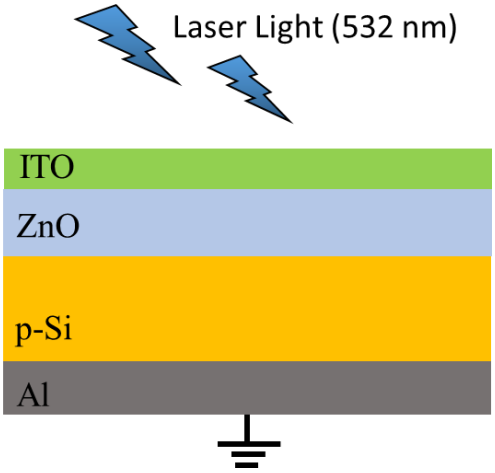


Figure 2.16 Schematic of light assisted resistive switch, which activated with photocurrent.

2.5 Thesis objectives and contributions

From the above discussion, we found the following area of improvement and worked through that. Finding the solution for a silicon-based on-chip nanophotonic device with low loss and small on-chip footprint. To electrically control the light at the nanoscale using the proposed nanophotonic waveguide. Then to fabricated, characterized, and analyze the device.

Following are the objectives of the research work carried out for this thesis:

- To realize dispersion control in nanophotonic devices using hybrid plasmonic waveguide for on-chip high data rate applications

- To control phase and optical absorption electronically in FET like structure using plasma dispersion effect

- Design, fabrication, and characterization of a nanophotonic resistive switch with optical readout capability

- To optically assist electro-metallization in resistive switching device to enhance the optical extinction ratio.

Chapter 3

Design, Fabrication and Analysis of Hybrid Plasmonic Waveguide

A photonic waveguide at real nanoscales based on the concept of hybridization of plasmonic and photonic modes is designed and fabricated. A high-index layer of silicon to control vertical and lateral confinement is introduced under the nano-confinement layer of thermally grown SiO_2 which together with optimized waveguide-width provides low-loss guidance of hybrid-plasmonic-mode. 11-nm thick SiO_2 on silicon provides us an optical-confinement at real nanoscales with an acceptably low loss of 7 dB/cm. Also, the proposed device exhibits ultra-low dispersion on introducing a grating in the silicon layer. In addition, the dispersion value crosses 'zero-dispersion' many times over a broad range of wavelengths.

3.1 Proposed hybrid plasmonic waveguide

The impact of photonic devices on communication and sensing is still evolving [87], [88]. Compact photonics at real nano scales can be the key to realize optical interconnects and label-free cell-level detection of chronic diseases [89]–[92]. The recent advances in the nanofabrication have given the ability to control the structure and properties of the devices to the desired levels. The miniaturization of the photonics devices is ideally limited by the diffraction limit of light which has been addressed with proposal of various novel guiding mechanisms [19], [24], [93]–[95]. The coupling of light with collective oscillations of free electrons at a metal-dielectric interface is a potential candidate for nanoscale optical confinement beyond the diffraction limit. Such plasmonic waveguide with surface plasmon polariton (SPP) modes suffers from large metallic losses which limit its use in practical

devices [96]–[100]. The optical waveguide loss of 0.02 dB/cm with mode area larger than $\lambda^2/4$ is reported by many groups [99], [100]. Whereas in a plasmonic waveguide mode area can be as small as $\lambda^2/4000$ with high loss of 0.4 dB/μm [59], [101]. A promising approach for optical confinement at real nano scales with low loss is the hybridization of SPP and optical modes [59]. Guided SPP mode in such hybrid plasmonic waveguide is dragged away from the metal-dielectric interface with a proper choice of dimensions which relaxes the effect of large metallic resistance on the guided (hybrid plasmonic, HP) mode resulting in a longer propagation length [59], [62], [102]–[104].

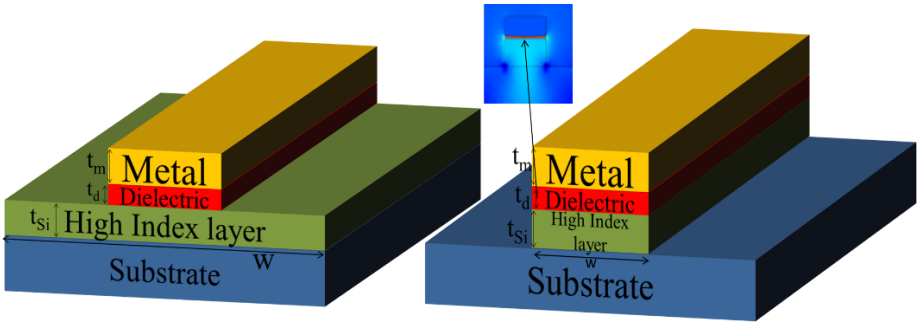


Figure 3.1 Schematic of the proposed nanoscale photonic waveguide, width of high index layer is (a) larger than core-width (b) equal to core-width of the waveguide where thicknesses of Si, SiO_2 and gold are 150-nm, 11-nm and 100-nm respectively. Inset shows mode confinement in dielectric layer.

A leaky mode confinement in a high refractive index layer underneath the HP confinement layer can further reduce the losses and can control propagation characteristics of the hybrid plasmonic waveguide for nano scale devices [105], [106]. A low loss hybrid plasmonic waveguide is designed and fabricated. The hybridization of plasmonic and optical modes is improved by controlling vertical and lateral optical confinement in a high-index layer. Presence of a high-index silicon layer and thermally grown SiO_2 on it provide us an acceptably low loss of 7 dB/cm in a 350-nm wide waveguide for

hybrid plasmonic mode guided in an 11-nm thick SiO_2. The excellent interface between confinement layer and the high-index silicon layer, the presence of leaky optical mode in silicon and optimized waveguide-width altogether result in a low-loss guidance of HP mode at real nano scales where mode area remains small enough. Also, the introduction of a grating layer in the silicon layer of the hybrid plasmonic waveguide provides us an ultra-low dispersion of 10 pico-sec^2/m and it passes through zero-dispersion value many times over a broad range of wavelength. The fabrication tolerance of the device is acceptable in the sense it provides low-loss operation where propagation loss remains low enough for practically short nanophotonic devices. The proposed work can be useful in realizing photonic platform at real nano scales for a variety of on-chip functionalities including high data rate optical interconnects which require low dispersion at nanoscales.

3.2 Role of high index layer

Controlling the hybridization of SPP and optical modes is necessary to increase the coupling between the two modes while keeping mode character at the value of 0.5 [106]. The coupling between SPP and optical modes should be so as to provide a reduced contribution of metallic resistances in guided mode propagation. This can be achieved by controlling vertical as well as lateral confinement of leaky optical mode in high index layer, silicon. The vertical confinement and hence the vertical coupling between SPP and optical mode can be controlled with thickness high index layer [62]. The contribution of metallic resistance (losses) into HP guided mode can be further reduced by improving the lateral optical confinement in a high-index layer which can be done by decreasing the width of the high-index layer. The schematic of the proposed hybrid plasmonic waveguide is shown in Figure 3.1. It consists of 150-nm thick patterned silicon on a silicon-substrate which is thermally oxidized to

give 11-nm thick (measured) SiO_2, providing us a defect-free interface between high-index layer silicon and confinement layer SiO_2. The thickness of Au at the top is 100-nm where the overall waveguide width is 350-nm. Figure 3.1(a) shows proposed structure without lateral confinement. The lateral optical confinement in high index layer (silicon) can be controlled by reducing the width of silicon. The lateral spread of the optical mode (leaky in this case) in silicon-layer can also control the coupling of SPP and optical mode into dielectric (SiO_2) layer. Lateral spread can be controlled by changing waveguide-width which is shown in Figure 3.1(b). The computed confinement of guided HP mode is shown in the inset of Figure 3.1(b).

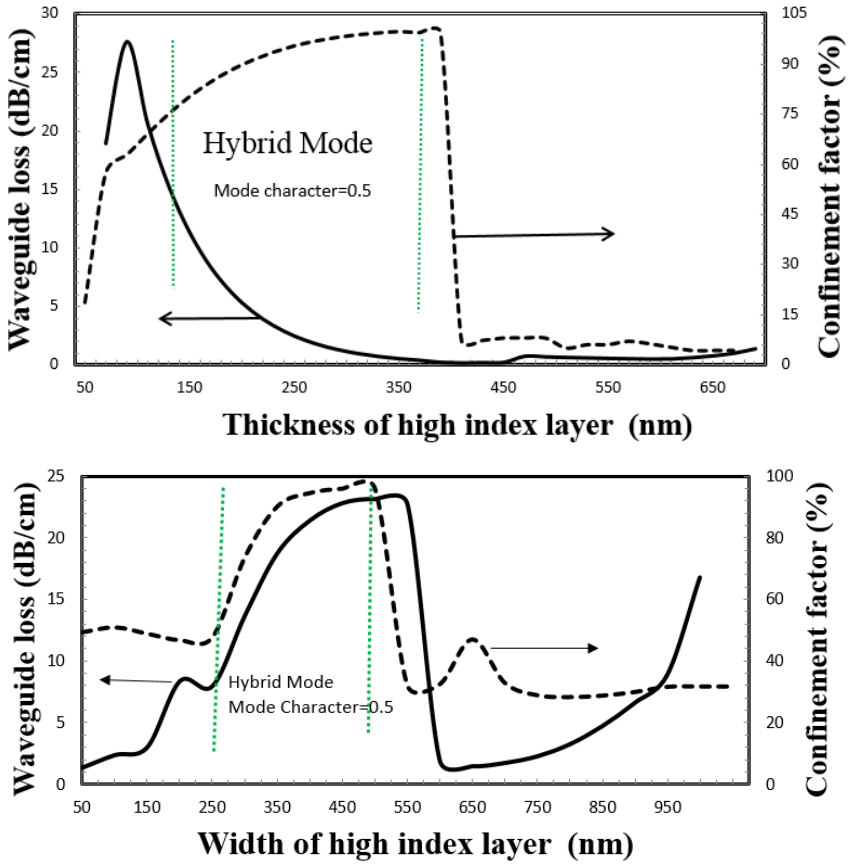


Figure 3.2 (a) Variation in waveguide loss with change in thickness of high index layer at constant width of 350-nm. (b) Variation in waveguide loss with change in width of high index layer where thicknesses of Si, SiO_2 and gold are 150-nm, 11-nm and 100-nm respectively

The hybrid plasmonic waveguide usually supports the TM mode. The leaky optical mode in the silicon layer controls the HP mode [104]. Figure 3.2(b) shows the effect (FEM simulation) of change in the width of high index layer on the waveguide loss. The width of high index layer is varied from 50-nm to 1-µm and graph is plotted along with the optical confinement factor. When the width is less than 250-nm the optical confinement is weak in the dielectric layer and the low loss we are getting is because of the leaky mode in high index layer. We have chosen an optimum value of width (350-nm) because of the low propagation loss and strong guided HP mode at this width. At other values of widths of high index layer either loss is very high, or the confinement of guided HP mode is weak. The graph Figure 3.2 (a) shows the variation in waveguide loss with change in thickness of high index layer below 130-nm of thickness loss is high, and confinement is low. After a thickness λ/4 (380-nm) optical confinement is weak in the dielectric layer.

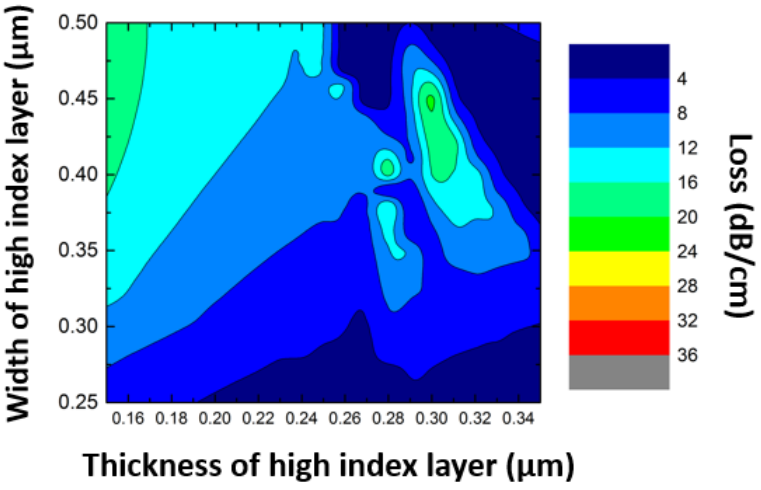


Figure 3.3 Variation in waveguide loss with change in width (250-nm to 500-nm) and thickness (150-nm to 350-nm) of high index layer.

It is observed from the simulation that when the width and the thickness of the high index layer become more than 450-nm and 350-nm respectively, this layer supports optical mode and all the mode energy is confined in the high index layer rather than in the desired layer (SiO_2) hence a sudden drop in waveguide loss is observed. 2D FEM simulation result shows a propagation loss of 12 dB/cm, when

width of the waveguide is 350-nm. The computed propagation loss remains acceptably low (for practical applications) and fabrication errors can still be accommodated while showing low loss operation. The effective mode area found to be $\lambda^2/260$ which is an indication of nano-scale optical confinement in the proposed waveguide. For the optimized results simulations are carried in 2D-space with variation in the width and the thickness of high index layer. Figure 3.3 shows the effect of the thickness (ranging from 150-350 nm) and that of the width (ranging from 250-500 nm). In 2D computation, the ranges of silicon thickness and width are 150-200 nm and 300-450 nm respectively; outside these specified ranges support hybrid plasmonic mode do not get supported.

3.3 Analysis of dispersion

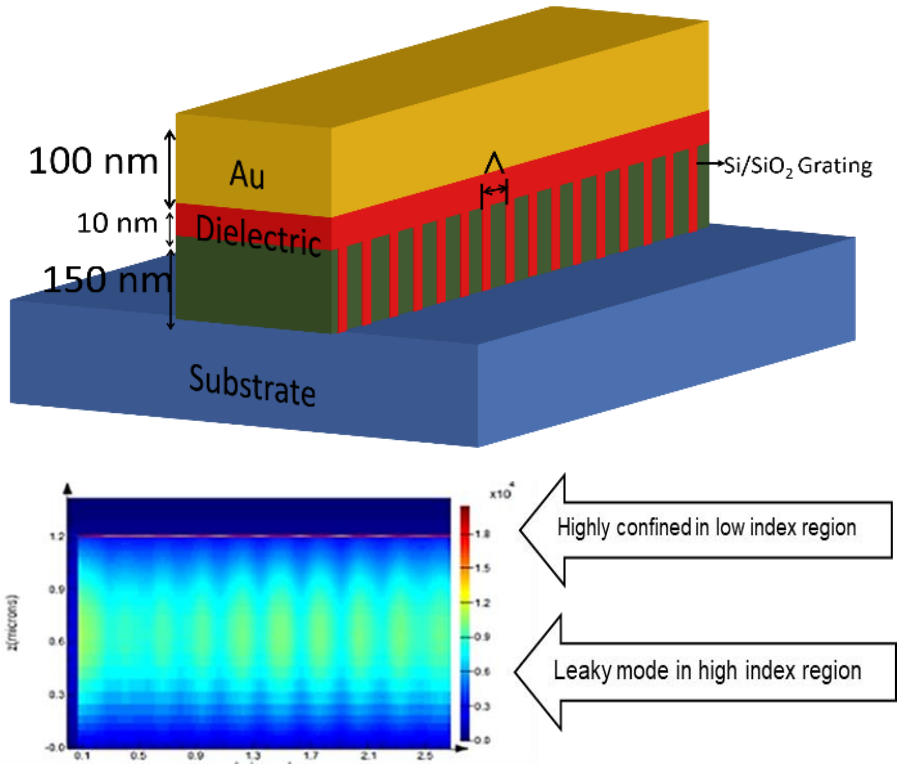


Figure 3.4 (a) Schematic of proposed waveguide with grating introduced in high index layer for low dispersion. (b) Side cross-sectional electromagnetic power profile showing high intensity of power in dielectric layer and leaky optical mode in grating layer.

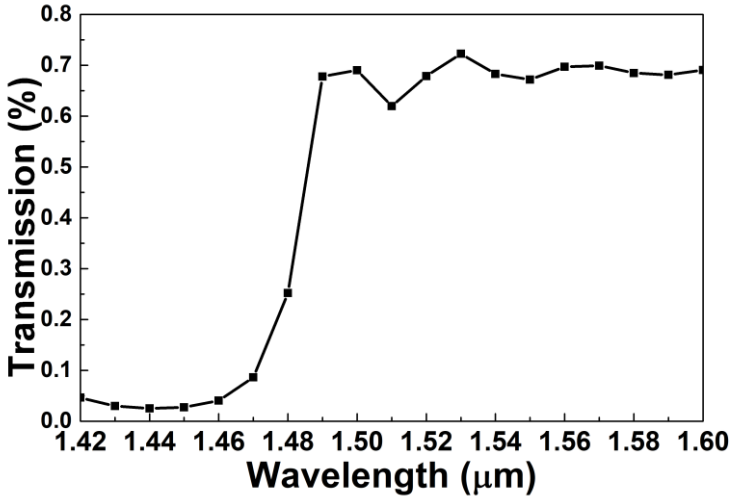
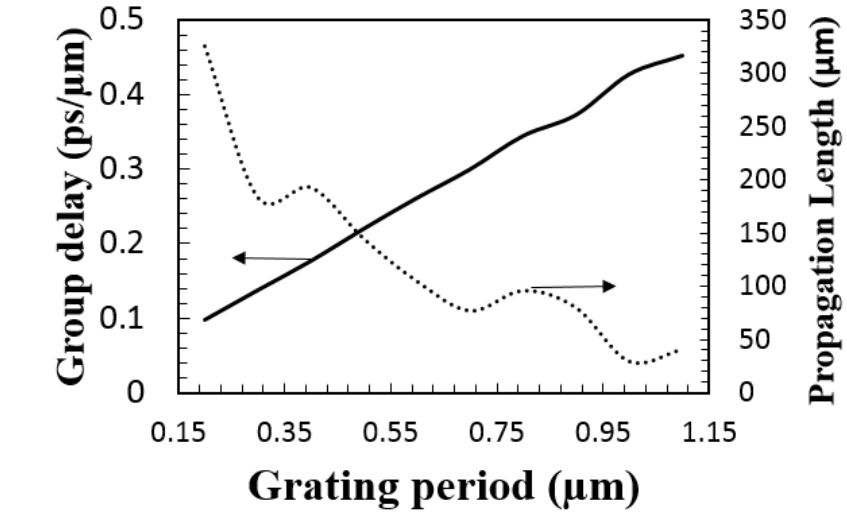


Figure 3.5 Transmission of the 1550-nm wavelength light at 70% duty cycle and 600 nm grating period.

One of the major requirements for high data rate application is low dispersion which causes small pulse broadening [107]–[109]. The requirement of low dispersion is of major concern for optical interconnects where devices are of low (nano scale) dimensions. In our proposed structure, the high index silicon layer provides a tight control on the HP mode characteristics. The introduction of a phase control layer in silicon should provide a filtering response to control the dispersion of guided mode [109], [110]. Figure 3.4(a) shows the schematic of grating embedded hybrid plasmonic structure for high data rate applications. The Si-SiO_2 grating controls the HP mode guided in SiO_2 through leaky mode on the high-index (grating) layer. Transmission of the proposed device with grating using the Lumerical FDTD solution is simulated. The transmission before 1500-nm wavelength is below 10% and after that it is almost constant for 100 nm bandwidth with more than 70% transmission, Figure 3.5. The transmission is calculated with 70% duty cycle and with 600-nm grating period.



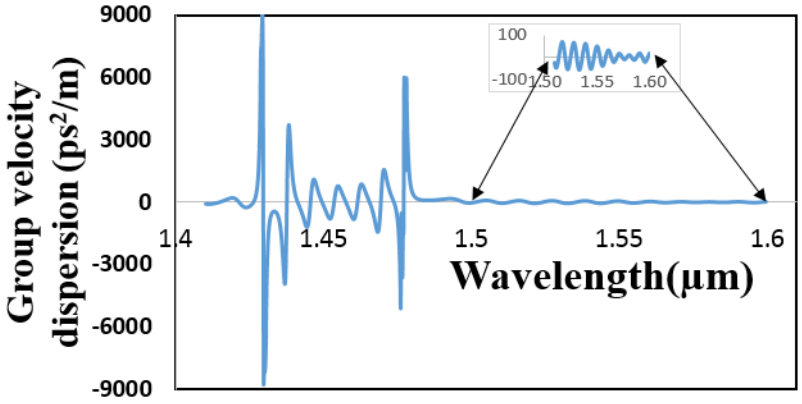


Figure 3.6 (a) Effect of grating period on waveguide propagation length and group delay at wavelength 1550-nm. (b) Group velocity dispersion of proposed waveguide over a wide wavelength band range is shown. Here grating of Si/SiO₂ is with period (∧) 800-nm and duty cycle of 70%.

The proposed waveguide structure shows low insertion loss of 25% in the wavelength range of 1.5-μm to 1.6-μm and a higher insertion loss for wavelength ranging from 1.4 μm to 1.5 μm. It is observed that by changing grating period we can change the wide bandwidth range. Figure 3.6(a) shows that the group delay increases with an increase in the grating-period which shows that the dispersion can be controlled with the grating-period at a particular wavelength which is 1550-nm in this case. The grating period is varied from 150-nm to 1150-nm. Beyond 850-nm of the period the grating induced

losses are further high and hybrid plasmonic mode ceases to propagate. The propagation length for waveguide is defined by $L_p=\lambda/(4\pi(n_{eff(imaginary)})$. A continuous decrease in propagation length is observed with the increment in the grating period. After a grating period of an 850-nm significant drop in propagation length is observed. Figure 3.6(b) shows that dispersion is near zero for a wide range of wavelength. The dispersion is measured with phase value extracted from time-field monitor and differentiated with angular frequency. The group velocity dispersion crosses zero many times (shown in the inset of Figure 3.6(b)) over a wide wavelength range of 1.48-µm to 1.6-µm and the dispersion varies with the maximum value of 10-ps^2/m. The reported ultra-low dispersion can be utilized for high data applications where pulse broadening is an issue.

Table 3.1 Comparison between dispersion parameter and flatness between various silicon based nanophotonic waveguides

Parameters →	***Dispersion Parameter ps/(nm·km)***	***Wavelength Broadband Range (nm)***	***Wavelength range (nm)***	***Flatness***	***Zero Crossing***
Si strip [111]	0 ± 200	172	1479~1651	1.16	2
Si strip +Si_3N_4[112]	0 ± 160	259	1346~1605	0.62	2
Si + slot (As_2S_3) [113]	0 ± 170	249	1460~1709	0.68	2
Si + slot (Si-NC) [108]	0 ± 16	553	1562~2115	0.03	4
This Work	**0±20**	**120**	**1480~1680**	**0.01**	**10**

The Figure 3.7(a) shows the confinement factor with variation in grating period and duty cycle. It is observed that the confinement factor varied with the variation in grating parameters. The variation can be seen in near multiple of λ. The waveguide mode characteristics is also calculated by FOM figure of merit. As the duty cycle changes and the period varies the mode characteristics changes with each

perturbation which effected overall hybrid mode characteristics. Figure 3.7 (b) shows the FOM is best with 90% duty cycle with λ/4 grating period. With the change in grating period the propagation length is calculated shown in Figure 3.8. It is observed that when the grating period is near the half wavelength or smaller the propagation length is large. The propagation length is also affected with the change in the duty cycle. It is observed that the duty cycle is 70% and more the and grating period is less than 500 nm the propagation length is in the order of 200 μm, which is acceptable for optical on chip communication.

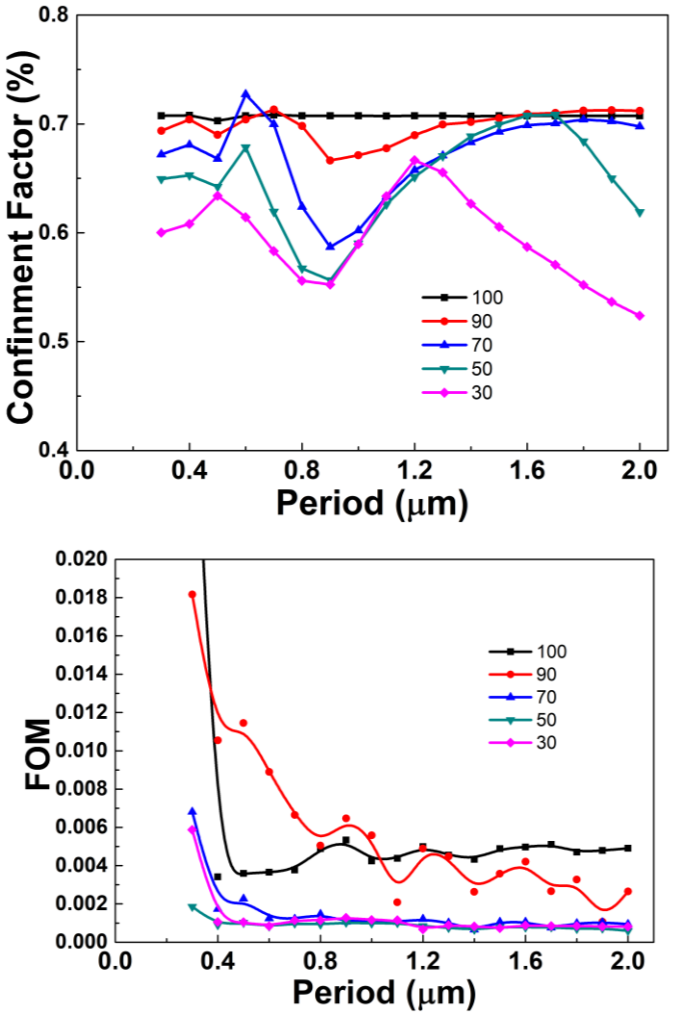


Figure 3.7 (a) Effect of grating period and duty cycle on mode confinement at wavelength 1550-nm. (b) and FOM figure of merit for the propagated mode.

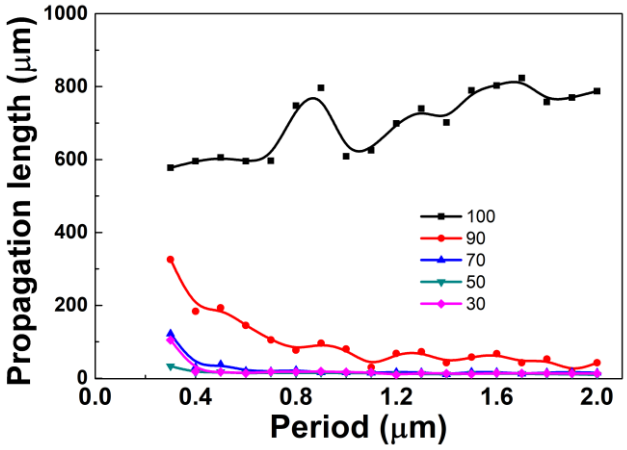


Figure 3.8 Effect of grating period and duty cycle on the propagation length at wavelength 1550-nm.

3.4 Fabrication of hybrid plasmonic waveguide

The fabrication process steps are summarized in Figure 3.9. We start with a crystalline silicon substrate with a thickness approximately 400-μm as shown in Figure 3.9 (a). Figure 3.9 (b) shows the rapid thermal process adopted for the growth of the oxide layer (SiO_2) on the substrate which results in an 11-nm thick SiO_2 layer (measured using ellipsometry). Figure 3.9 (c) shows the deposition of a 100-nm thick gold layer on SiO_2 using E-beam evaporation at room temperature. The rate of deposition is kept 2 Å /s, the base pressure 1.87x 10^{-6} Torr and the dep. pressure is 3x 10^{-6} Torr. Figure 3.9 (d) shows coating PMMA resist followed by electron-beam (E-beam) lithography and then removal of PMMA to obtain the desired pattern. Figure 3.9 (e, f), After the masking process, wet etching is used to etch gold to achieve 100-nm thickness. KI_2:I_2:DI (4g:1g:40ml) is used as etching material. The etch material is kept on the hot plate until the temperature reaches up to 750 ºC. The etching is done at a rate of 4 nm/sec and the etch duration is 25 sec. Then by reactive ion etching and PMMA mask extra SiO_2 is etched up to 11-nm thick SiO_2 shown in Figure 3.9 (g). After the etching of Au and SiO_2, reactive ion etching of silicon is performed to obtain 150-nm thick and 350-nm wide silicon as shown in Figure 3.9 (h).

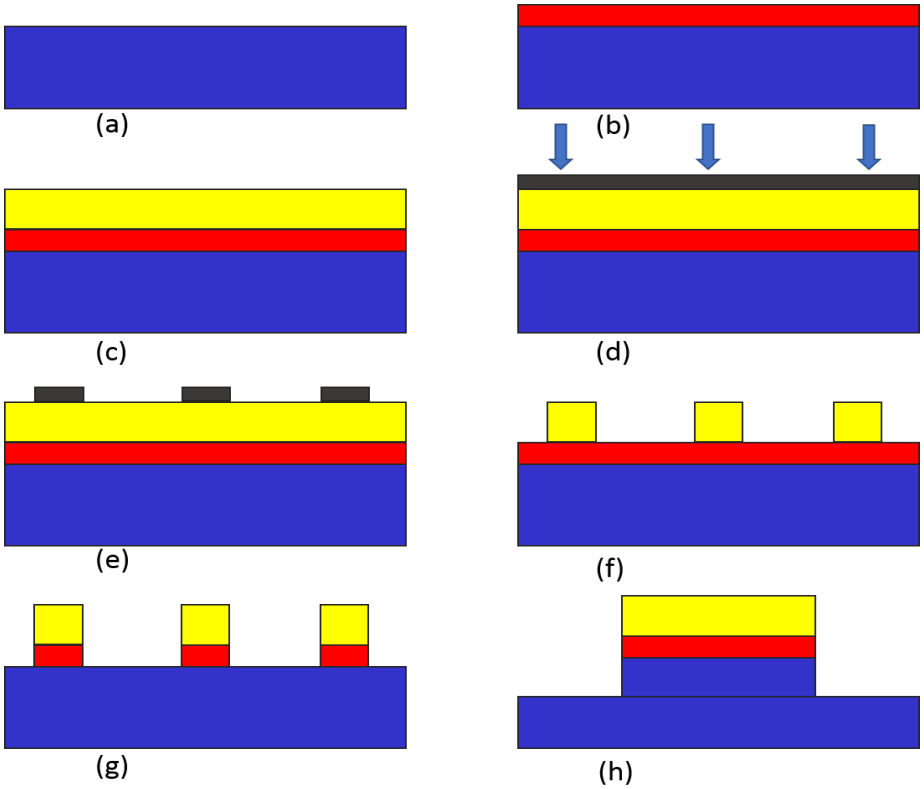


Figure 3.9 Process flow for the fabrication of an array of the proposed nanophotonic waveguide. (a) Starting from (cleaned, using RCA 1 and RCA 2) p-type silicon substrate, (b) thermally grown SiO_2 on Si after rapid thermal oxidation, (c) electron beam evaporated gold over entire surface of SiO_2, (d) coating of PMMA resist, (e) patterning using E-beam lithography and PMMA removal (f) wet etching of gold (g) dry etching of extra SiO_2 and (h) etching of silicon to get a desired design of the waveguide.

The Near Field Scanning Optical Microscopy (NSOM) is used to characterize the optical confinement in the nano-scale region. Figure 3.10(a) shows the measurement set-up for the proposed nanophotonic waveguide. The input light is coupled into the waveguide (side shown in Figure 3.10 (a)) with help of a tapered optical fibre. Output light is then collected by the silicon tip of the NSOM set-up [114]. The NSOM experiment is performed by focusing the 1550 nm wavelength laser beam on the waveguide-device (with various lengths) through a lensed fibre with a power of 1.5 mW. Few arrays of the proposed waveguide are fabricated SEM view of which are shown in the inset of Figure

3.10(a). After dicing and CMP (Chemical-Mechanical-Polishing) process the samples are made ready for measurement. Measurement is performed on three samples each of specified lengths and over three samples of each length the insertion loss remains almost constant for a particular length as shown in Figure 3.10 (b). The slope of the curves shows a propagation loss 7.0 dB/cm. The whole experiment is carried out at room temperature. The propagation loss of 12 dB/cm is calculated through simulation. The difference is because of the excellent quality of the interface resulting from the growth of dielectric layer i.e. SiO_2 by thermal oxidation of underlying silicon. This results in the guidance of HP mode in a rather defect-free interface between Silicon and SiO_2. It may_also be because of alignment errors during measurements. The reported loss is acceptable for practical applications of the waveguide in short devices.

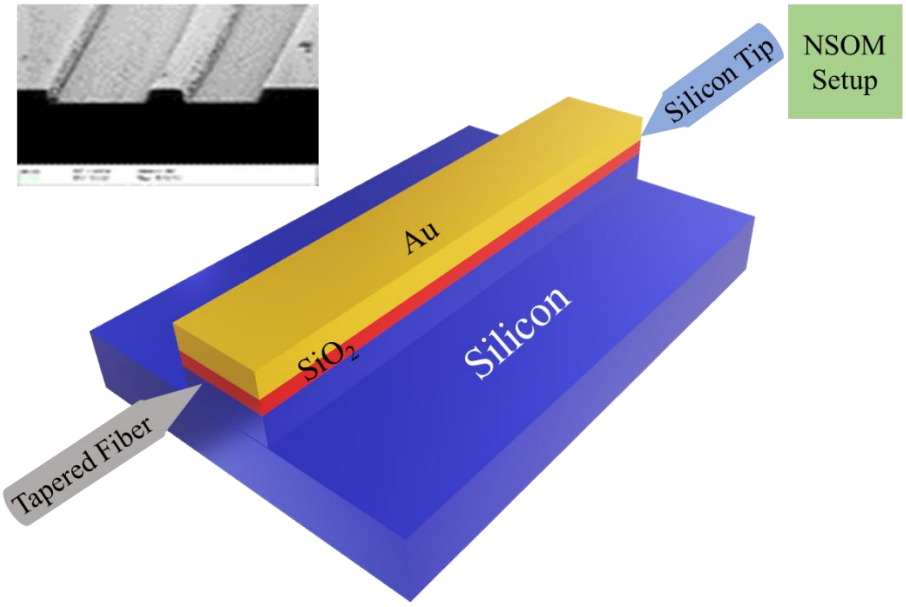


Figure 3.10 (a) Schematic of the measurement set-up for proposed nano-photonics waveguide (side-view shown). Light is coupled from (left) a tapered optical fibre into the waveguide-device and the output signal is collected (at the right) by the silicon tip of the NSOM set-up; Inset shows an SEM view of the part of an array of fabricated waveguides.

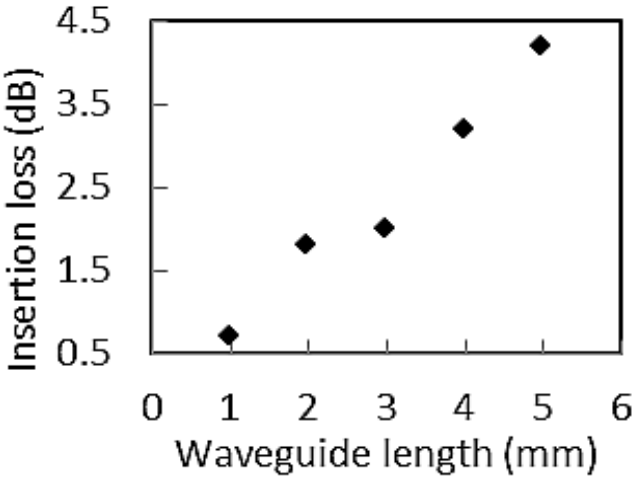


Figure 3.11 Shows measured insertion loss for various lengths of the waveguide.

3.5 Summary

A low loss nanophotonic waveguide is designed and fabricated. A high index layer under the dielectric confinement layer provides improved hybridization of plasmonic and optical modes resulting from controlled lateral and vertical confinement. The measured loss for a 350-nm wide waveguide comes out to be 7-dB/cm for a hybrid plasmonic mode guided in the 11-nm thick region. The proposed design is doubly benefitted from the presence of a high-index silicon layer, it provides efficient coupling between plasmonic and photonic modes, and it offers a defect-free interface for the nano-optical confinement. In addition, the introduction of a grating structure in the silicon layer opens a way of utilizing the proposed device for the high data rate applications where an ultralow dispersion is required. The filtering response of Si/SiO_2 grating provides an ultralow dispersion of 10-ps^2/m. The proposed waveguide can be useful for the realization of compact photonic devices at nanoscales for large-scale photonic integration.

Chapter 4

Guiding and Controlling Light at Nanoscale in Field Effect Transistor

In order to utilize the full potential of the proposed hybrid plasmonic waveguide for the on-chip practical applications electrical control is to be incorporated. Transistors are the basic building block for semiconductor electronics. The MOS based matured electronic technology can be used for the controlling the optical signals. Controlling light at nanoscale is another issue to tackle. In hybrid plasmonic waveguide the leaky optical mode from the plasma dispersion effect can be used to modulate the optical signal. The metal-oxide-semiconductor field-effect transistor (MOSFET) and tunnel field-effect transistor (TFET) are proposed to guide and control the light at nanoscale utilizing the hybridization of plasmonic and optical modes. The hybrid plasmonic (HP) mode is confined in the dielectric sandwiched between metal gate and semiconductor channel which results from the coupling of surface plasmonic polariton (SPP) mode at the metal-dielectric interface with the optical mode in the dielectric. Conventional conductivity modulations in the channel through gate and drain-source voltages are utilized to control the guided light. A long propagation length of 74 μm and a very small mode area of $\lambda^2/96$ are reported for field-effect transistor at an operating wavelength of 1550 nm which are useful to realize low-loss and compact optoelectronic devices. The charge-carrier dynamics along with the plasma dispersion effect in the silicon-channel, through voltages applied on the gate and source-drain, result in the optical phase modulation in MOSFET and TFET. Phase shift of π radian at a length of 1.2 mm and 0.21 mm are obtained in MOSFET and TFET respectively. The proposed concept has the potential to enable multifunctionality of the mature field effect transistors.

4.1 Optical guidance in field effect transistor

The rising Silicon Photonics holds a strong promise to revolutionize short-reach optical interconnects [6], [115], [116]. Wide deployment of broadband optical communications has become crucial especially for internet data centers and high-performance computing systems [117], [118]. Integration of silicon based complementary metal-oxide-semiconductor (CMOS) field-effect transistor (FET) and silicon integrated photonics, also known as silicon CMOS-integrated photonics, carries the potential to play a key role in enabling such deployment [119], [120]. The limitations of using copper in interconnects in electronic ICs have heralded the emergence of optical interconnects [18], [121]. The strong presence of silicon in electronic ICs favors the use of silicon to realize integrated photonic devices. During last couple of decades, integrated silicon photonic devices have seen notable advances [14], [122]–[126]. The realization of photonic devices at Nanoscale for large-scale photonic integration remains a hot topic on which lot of research efforts are being made. Several mechanisms are proposed to reduce photonic device size beyond diffraction limit [126]–[128]. Sub-wavelength optics based on surface plasmon polaritons (SPP) allows controlling and guiding of light at Nano-scale structures mainly at metal-dielectric interfaces [129], [130]. Because of the opposite polarities of permittivity of the two materials i.e. noble metals (gold) and dielectric (silicon-oxide), the optical field can be squeezed into much smaller dimensions than the diffraction limitation of the light. High optical losses associated with SPP based waveguides can be reduced with Hybrid plasmonic (HP) by exploiting optical confinement deeper into the dielectric and away from the metal-dielectric interface [59], [103], [131], [132]. HP waveguide can support HP mode to propagate longer with low loss with very small mode area, on the order of $\lambda^2/400$; hence it can be a building block to realize photonics at Nanoscale. A number of on-chip optical functions have been realized to guide the light in different

materials and then to control the light for different applications e.g. optical modulation. Guiding the light in silicon at Nanoscale and then controlling it electrically are two fundamental requirements for the realization of compact silicon photonic platform e.g. for silicon CMOS-integrated photonics.

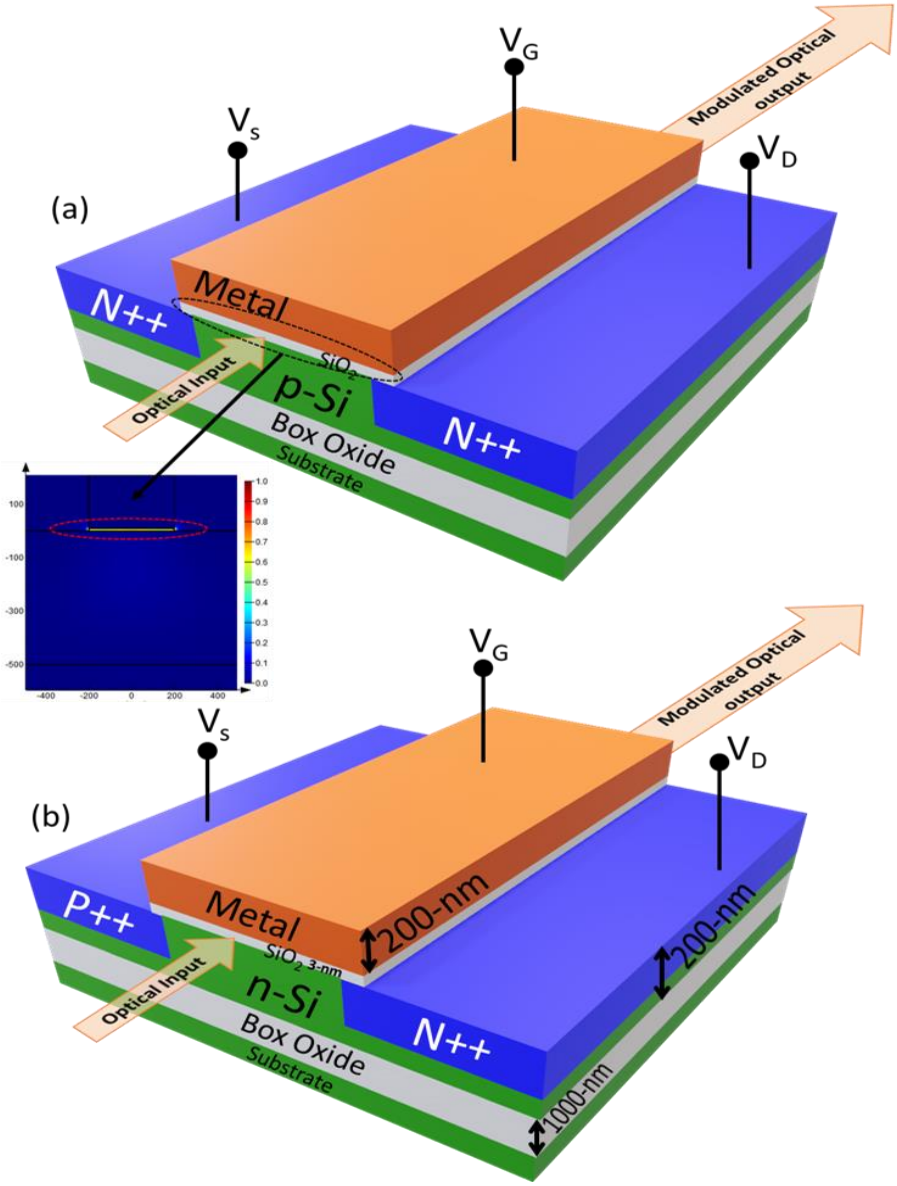


Figure 4.1 Schematic of nanophotonic waveguide cum phase modulator based on hybrid plasmonic concept using (a) MOSFET (inset shows the optical field confinement in gate oxide) and (b) tunnel FET, both on silicon-on-insulator with a 120-nm channel length.

The MOSFET configuration has an advantage, over PIN diode with isolation trenches, of negligible dc power consumption along with localization of refractive index change under the gate electrode [133]. Metal-oxide-semiconductor based silicon modulator based on free carrier effect offers bandwidth exceeding 1GHz with a V_π L product of 8Vcm [134]. The speed of silicon photonic modulators also depends on the free charge carrier concentration and the contact pad placements. The device speed can be increased by introducing a graded doping profile in the vertical direction in a way such that higher doping density exists near the gate oxide and lower doping concentrations in rest of the waveguide [25]. Nanoscale photonic functionality using MOS based structures is still missing; it can be exciting to use MOSFETs underlying in electronic ICs as Nano-scale optical waveguides with an electronic control for the realization of various photonic devices.

Here we report Nano-scale optical guidance and controlling a MOSFET and in a tunnel TFET with mode field area of $\approx \lambda^2/100$. The 1550-nm wavelength light is made to confine in the gate oxide of few nanometer thickness sandwiched between gate metal and underlying silicon. The concept of hybrid plasmonic waveguide is used to guide the hybrid plasmonic mode in 2-3 nm dielectric. The guided HP mode shows a propagation length of 72 μm for TFET and 48 μm for MOSFET. The mode areas are reported to be $\lambda^2/46$ and $\lambda^2/96$ respectively for MOSFET and tunnel FET. The very electronic nature of FET is utilized to control the guided light at Nanoscale. The design and analysis of the devices are performed with finite difference eigenmode (FDE) using LUMERICAL [135]. Conductivity modulations in FETs using applied voltages are shown to control the phase of the guided HP mode. An efficient optical phase modulation is reported in both the devices. On varying drain source voltage phase shifts of radian at a length of 204 μm and 1235 μm are obtained for TFET and MOSFET respectively. On varying gate-voltage, the change in effective refractive index is in the order of 10^{-5} which is smaller than

that for a change, in drain-voltage resulting in 10^{-3} change in effective refractive index. The proposed concept adds an extra degree of freedom in the application of FETs. The reported results are the excellent examples for enabling multifunctionality in FETs.

4.2 Device design and motivation

The schematic of the proposed devices is shown in Figure 4.1. A nanoscale optical waveguide as well as phase modulator is functional through the gate-oxide of Figure 4.1 (a) n-channel MOSFET and Figure 4.1 (b) n-channel tunnel FET. The hybrid plasmonic mode is guided in the gate-oxide on the semiconductor channel as shown in 3D view of the proposed device. The inset of the Figure 4.1 (a) shows optical field confinement contour map. The charge carrier dynamics of the channel in both the cases is made to control the guided HP mode utilizing the conductivity modulations by varying terminal voltages. HP mode confined in the gate-oxide is the result of the coupling of SPP with the optical mode (leaky) in the underlying semiconductor (channel). The hybridization of leaky optical mode from high index layer silicon is coupled with SPP from interface of dielectric and metal. The square norm of mode amplitude of hybrid mode is crucial parameters which is defined as

$$|b|^2 = \frac{n_{hyb} - n_d}{2n_{hyb} - n_d - n_{spp}} \tag{4.1}$$

Where n_{hyb}, n_d, n_{spp} are the real refractive index of hybrid, dielectric(optical) and plasmonic mode. The mode character study on the similar designed is done in [59], [132], if the mode character is greater than 0.5 the hybrid mode is more inclined towards leaky optical field and if it is less than the field is more plasmonic mode. The coupled (HP) mode supports long propagation while maintaining a mode area small enough to cause Nano-scale confinement. Electric field associated with excited plasmonic wave decays exponentially along both the sides of interface. Gold is used as the top gate metal for

the proposed device, with relative permittivity of = -115.13+i11.259 [136]. The field enhancement exists at the top and bottom surfaces of the low index SiO_2 layer. The bottom surface i.e., Si-SiO_2 interface, has field enhancement due to a strong discontinuity of the normal component of the electric field. This phenomenon takes places only when the thickness of the SiO_2 becomes less than the penetration depth of the evanescent wave resulting into overlapping of optical mode and surface plasmonic mode on each other. Coupling of two modes has potential to propagate at longer distance of several tens of microns realizing a promising platform for ultra-dense photonic integration. Two major factors contributing the performance of conventional MOSFET for optical behavior are 1) carrier induced channel formation and 2) voltage-controlled displacement of channel charge carriers from source to drain. In TFET, source and drain are of opposite doping types and the substrate has doping type same as that of drain influencing injection and depletion of carrier charge concentration on applied voltage. The light matter interaction due to graded doping profile and charge carrier concentration density helps in electrooptic phase modulation [131].

4.3 Optical characteristics

Lumerical DEVICE's drift-diffusion transport solver is used to analyze the electrical characteristics of the proposed device by defining the component geometry and gaussian doping profile [135]. Simulation of the charge distribution in response to an applied voltage is performed. Lumerical optical solver, MODE solutions, is used to perform FDE simulations of the guided-wave structures and extract the phase response as a function of the applied voltage with respect to change in effective refractive index. Fixed source wavelength of 1500 nm is used for simulation. The refractive index used at 1550-nm of wavelength for SiO_2 and Si is 1.44 and 3.48 respectively, and dielectric constant for gate metal gold is = -115.13+i 11.259 [136]. PML is

designed to absorb the outgoing waves from active computation domain without reflecting them back to the active region of the device. The perfectly matched layer boundaries and metal boundaries are located at more than three times the dimensions of the device being simulated along x-axis and z-axis. The electrical characteristics for the phase modulation are analyzed using drift-diffusion transport method by studying the distribution of charge component in response to an applied voltage. The modulation occurs in a transverse device where the current flow is perpendicular to the direction of light propagation. MOSFET utilizes single injection carrier (hole or electron) altering the refractive index. Following equation shows change in refractive index because of the changes in electron hole densities [137].

$$\Delta n_e = -8.8 \times 10^{-22} \Delta N_e \tag{4.2}$$

$$\Delta n_h = -8.5 \times 10^{-18} (\Delta N_h)^{0.8} \tag{4.3}$$

ΔN_e and ΔN_h representing electron and hole charge densities respectively. The equations reveal that effective refractive index change due to holes is three times larger than electrons for same carrier concentration.

4.4 Electrical characteristics

The dimensions of high index layer silicon are chosen such that only leaky optical mode can travel through it. The lateral and vertical dimension of high index layer is taken from [133]. The insulator thickness affects the properties of waveguide mode. The optimized designs of both the devices exhibit electronic characteristics in line with conventional FETs. The silicon layer thickness is 200 nm (optimized to achieve hybrid mode confined in SiO_2). Figure 4.2(a) and (b) show the transfer and output characteristics of the MOSFET transistors respectively formed on p-type Si. Figure 4.2 (c) and (d)

show the input and output characteristics of the TFET transistor. The analysis for MOSFET and TFET includes trap assisted (SRH) and band-to-band tunneling models respectively. All the characteristics are in compliance with the basic requirements of a transistor.

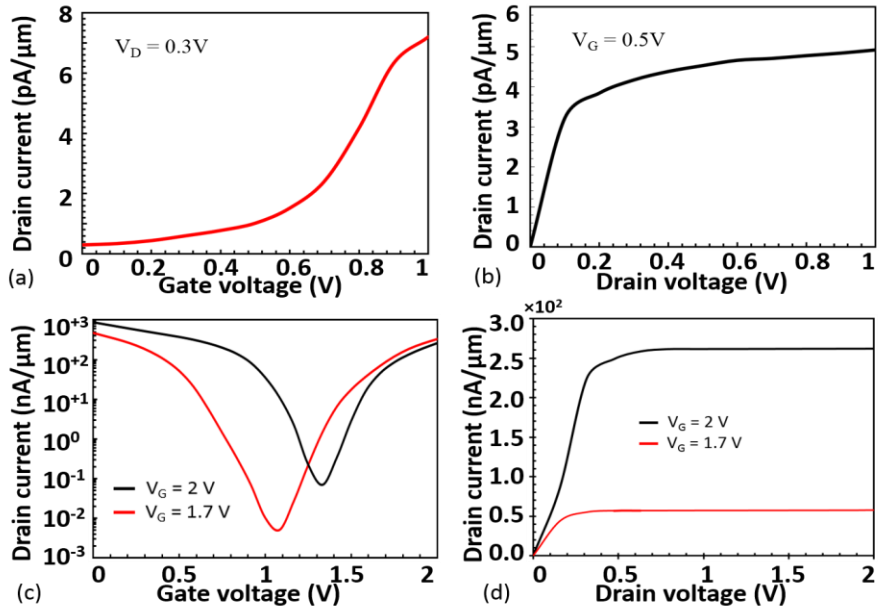


Figure 4.2 Simulated characteristics of n-type MOSFET (a) Transfer characteristics for a fixed drain of 0.3 voltage (b) Output characteristics for a fixed gate voltage. Simulated characteristics of n-TFET (c) IDVG characteristics for different drain voltages (d) I_DV_D characteristics for a drain voltage of 2 V and 1.7 V.

In n -type MOSFET, applying positive voltage at the gate terminal tends to repel holes near oxide and are pushed downwards leaving behind negative ions. This forms the uniform channel thickness and length called inversion layer. Impact of charge density on effective refractive index is observed at a fixed positive gate voltage and on the applying negative voltage to drain, the potential difference of gate-to-drain region becomes less positive compare to potential difference to that of gate-to-source region as shown in Figure 4.3(a). The presence of less positivity of the voltage among the two-potential difference regions above the channel results in lesser number of holes being

repelled. As a result, more holes are present in a region that is less positive. Figure 4.3 (a) and (b) together explains the shortening of channel thickness taking place from gate-to-source region being more positive towards gate-to-drain region being less positive, initially increasing the n_{eff} as increase in the depleted layer region. On applying negative to positive voltage at drain terminal the thickness of the depletion region starts increasing, pushing a greater number of holes from gate-to-drain region resulting in linear increase in effective refractive index because of the push-pull effect of drain voltage. Figure 4.3 (c) further shows inversion layer with stationary immobile ions. Current flows when channel starts to form when $V_G > V_{TH}$ injection of carriers into the channel takes place. The propagation length is defined as the distance for the SPP intensity to decay by a factor of 1/e. This condition is satisfied at a length for the guided HP mode given by [137].

$$L_{prop}(\mu m) = \frac{\lambda}{4\pi(n_{eff(imag)})} \tag{4.4}$$

The device modulation speed is dependent on many factors. The speed of the optical phase modulation of the proposed device is limited by the charge carrier injection in the channel and the transistor internal high frequency capacitance. Further the increases in doping concentration in drain/source region affect the modulation speed of the device. The choice and the placement of physical contact pads also play a role in lowering the speed of the phase modulation of the device. The p+ doped region is named as source and the n+ doped region is name as drain. The substrate is lightly n-doped as intrinsic region. The drain voltage is the onset of tunneling barrier saturation obtained at constant gate voltage. Optically in NTFET, forward bias affects change in refractive index compare to reverse bias. Figure 4.3 (d) shows injection of holes and electrons into intrinsic region.

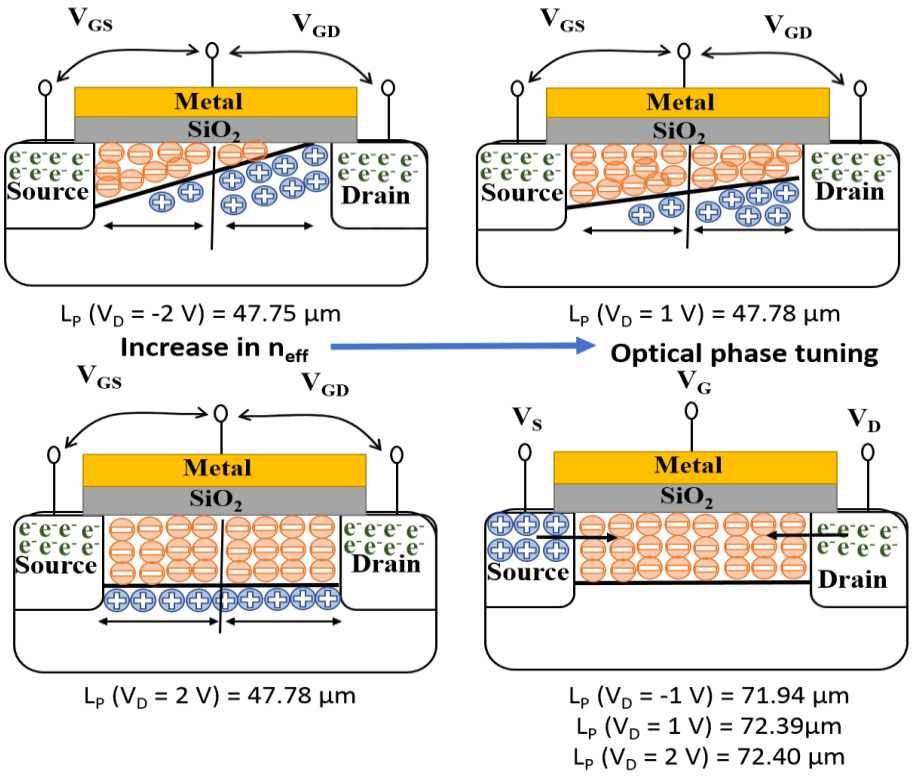


Figure 4.3 Opto-electronic n-type MOSFET mechanism at VG = 1V and VS = 0V showing (a) and (b) increase in effective refractive index resulting in optical phase tuning (c) formation of inversion layer resulting into negligible change in effective refractive index. (d)N-TFET carrier injection from source as well as from drain into intrinsic region. The light propagation length with respect to applied drain voltages is mentioned below respective mechanism.

4.5 Optical modulation in MOSFET and TFET

Major contribution of the optical losses comes from the absorption of charge carriers and/or from the plasmonic ohmic losses. The larger the charge carriers the larger will be the optical absorption. The other sources of optical losses may be related to the in and out coupling of the device. In proposed device the optical field intensity is mainly concentrated in the gate oxide layer of 3-nm where the major losses are incorporated due to the plasmonic ohmic losses. Figure 4.4 shows a slope of 0.01 for propagation length at V_G = 1V because of the

injected carriers. When V_G = 0V, there is no formation of channel as well as no carrier injection with zero slope. The propagation length for fixed gate voltage, varying drain voltage is $L_p(V_G$ =0V) = 47.74 μm at V_D = -3V and $L_p(V_G$ =1V)= 47.70 μm at drain voltage of -3V. Figure 4.4 shows a slope of 0.01 for propagation length at V_G = 1V because of the injected carriers. When V_G = 0V, there is no formation of channel as well as no carrier injection with zero slope. The propagation length for fixed gate voltage, varying drain voltage is $L_p(V_G$ =0V) = 47.74 μm at V_D = -3V and $L_p(V_G$ =1V)= 47.70 μm at V_D = -3V. The n-channel tunnel FET device structure has resemblance to a MOSFET forming the inversion or accumulation layer on applying gate voltage and the substrate region works similar to PIN diode [138]. The change in refractive index results in a phase shift $\Delta\varphi$ in the hybrid plasmonic mode given by:

$$\Delta\phi = \frac{2\pi L}{\lambda}\,\Delta n_{eff} \tag{4.5}$$

Where L_π is the active length of the phase shifter for π phase shift, Δn_{eff} is the change in effective index of the waveguide on application of external electrical field, and λ is the wavelength of light in free space.

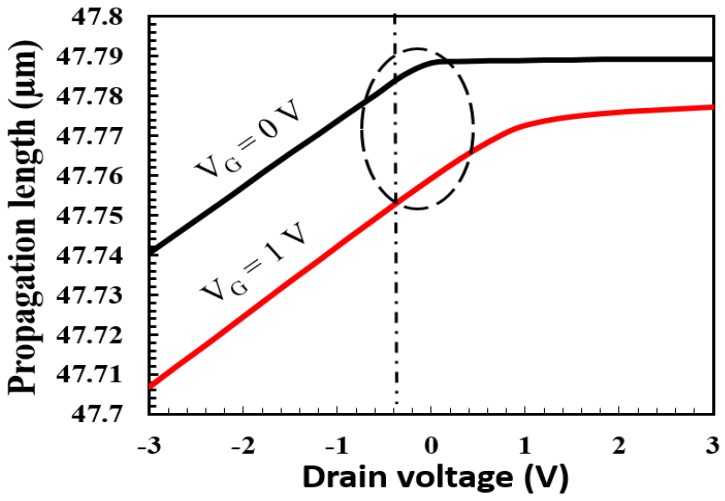


Figure 4.4 Effect on propagation length of hybrid plasmonic mode by varying drain voltage at a fixed gate voltage for conventional proposed MOSFET.

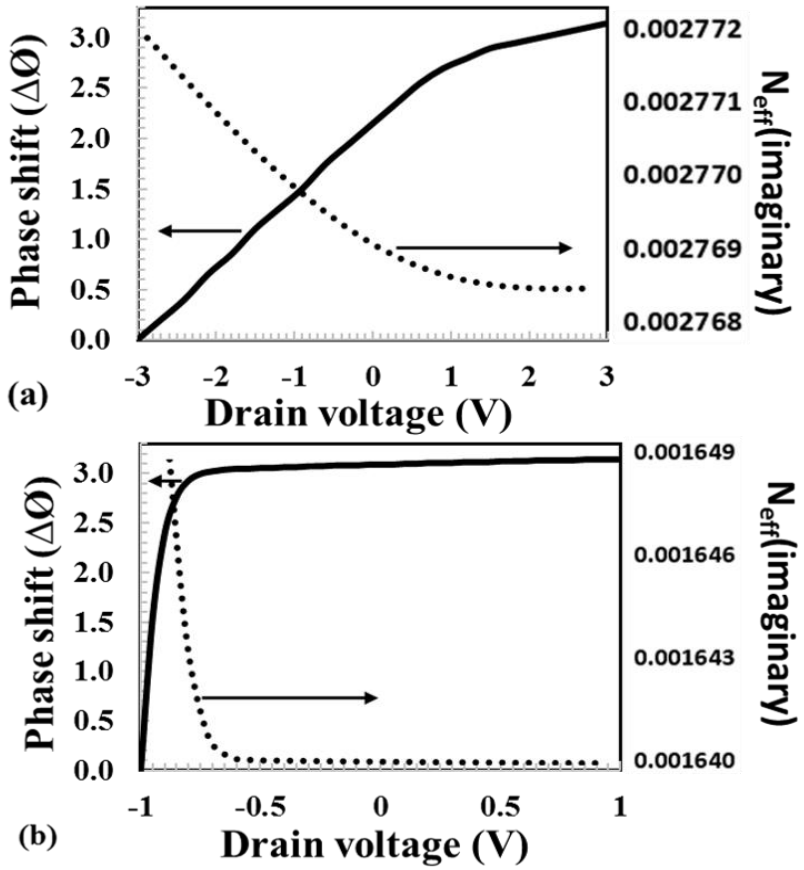


Figure 4.5 Optical phase shift(solid line) in relation with change in effective refractive index on varying drain voltage at fixed VG=1V in (a) n-type MOSFET (b) NTFET, the dotted line shows the change in imaginary part of effective refractive index of hybrid mode.

The effect of change in drain voltage on the imaginary part of effective refractive index is shown in Figure 4.5(dotted line).

Figure 4.5 (a) shows change in optical phase shift of MOSFET on applying drain voltage from -3V to 3V for a waveguide length of 1.235 mm. linear slope is observed from -3V to 1V and thereafter the slope decreases, because as the voltage on drain varies from -3 V to 1V, the effective refractive index increases linearly. After a voltage of 1V to 3V the change in effective refractive index is almost negligible resembling to strong inversion region. Similarly, Figure 4.5 (b) optical phase shift in tunnel FET on applying voltage from -1 V to 1V for a waveguide length of 0.204 mm. sudden change in phase shift is observed from -1V to -0.6V i.e., tremendous change at a very short

voltage range. In this condition the tunnel FET works in forward bias. Hence a very large number of holes and injected into intrinsic region. After a voltage of zero volts the tunnel FET works in reverse bias leading to negligible change in charge carrier concentration resulting in negligible change in effective refractive index.

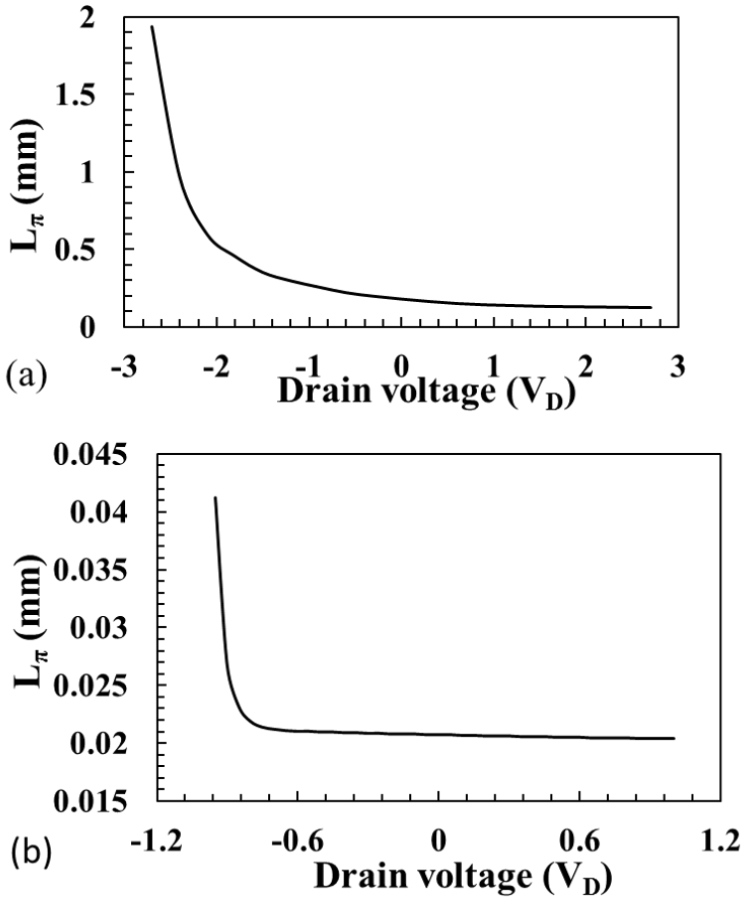


Figure 4.6 Effect on Lπ with change in voltage (a) from -3V to 3V of proposed n-type MOSFET (b) -1V to 1V of proposed NTFET for guided hybrid plasmonic mode at optical wavelength of 1550 nm.

Considering MOSFET device structure, Δn_{eff} of 10^{-4} is observed implying an active length of 1.235 mm. In Figure 4.6 (a) the length for phase shift starts decreasing from -3V to 1V due to more negative potential difference of gate-to-drain region. For a wavelength of 1.55 μm, L_π is 1.937 mm at V_D = -3V and 1.43 mm at V_D = 1V. From 1V onwards the length reduces gradually to 1.2 mm at 3V. As per equation (12), in hybrid plasmonic n-channel tunnel FET device the n_{eff} of 10^{-3}

is predicted for 1×10^{16} injection level. This implies an active length of 0.21 mm at a fixed gate voltage of 1V for a drain sweep from positive to negative. In Figure 4.6 (b) L_π is inversely proportional to the applied drain voltage. The light guiding region is influenced by dual carrier injection affecting change in refractive index. For example, with applied voltage of -1 V, the length is 0.4 mm meanwhile at 1 V, the required length is 0.210 mm. Hybrid plasmonic waveguide phase modulation is more in device structure similar to that of tunnel FET than in n-type MOSFET. Conventional MOSFET utilizes only one type of carrier injection (electron or hole) whereas advantage of conventional TFET over MOSFET implies injection of both, electron and hole increasing Δn_{eff}.

4.6 Summary

The MOSFET and tunnel FET are proposed in the form of nanophotonic devices. A nanoscale optical waveguiding utilizing hybrid plasmonic concept and electrical control of guided mode are realized in FETs. An efficient optical phase modulation in the HP mode is reported in the proposed devices. The electrical and optical characteristics of field effect transistor are studied in relation with working mechanism of device perturbing the effective refractive index. Improving the device performance to meet the requirement of application and to compete with other devices some optimizations in further needed. Increasing the doping concentration of source and drains can increase the device performance in terms of modulation efficiency but with increased optical losses. The device dimension can further be optimized to achieve efficient optical coupling. For example, increasing the gate oxide thickness may lower the optical losses but at the cost of high energy consumption to achieve π phase shift of the optical signal. The optimization of lateral dimensions should improve the amount of charge carrier injection which interns may show larger change in real part of effective refractive index of the proposed device.

Conductivity modulations in FETs are used to electrically control optical properties due to free carrier plasma dispersion effect. Minimum length for phase shift achieved by voltage swing of -3 V to 3V for n-channel MOSFET is 1.235 mm and that in n-channel tunnel FET is 0.21 mm on voltage swing of -1 V to 1 V for the propagated hybrid plasmonic mode. The MOSFET and TFET utilizes single injection carrier type and dual injection carriers respectively affecting the refractive index. In n-channel tunnel FET, observed refractive index change is of 0.003 at a very small voltage range from -1V to -0.6 V. The proposed concept can open up new areas for applications of FETs. The reported results create a novel way to use FETs in integrated photonics thereby provides an extra degree of freedom in their applications.

Chapter 5

Electrically Writable Silicon Nanophotonic Resistive Switch

The physical and chemical changes at the nanoscale in semiconductor electronics, on the application of the electrical field, can be utilized to manipulate light. To further improve the electrical control at nanoscale we have combined the strength of the resistive switch with that of the photonics which has resulted in an interesting optical switching element. An electrically writable resistive memory with optical readout based on a silicon nanophotonic structure is proposed. Hybridization of optical and surface plasmonic modes in the device enables nanoscale optical confinement to efficiently detect resistive memory effect in a 13-nm thick SiO_2 layer sandwiched between p-type silicon and gold. Electrical write and optical readout capabilities are experimentally demonstrated with well-defined optical and electrical hysteresis curves at a wavelength of 1550-nm in the proposed nanophotonic device. The p-type silicon carries multifold benefit – it provides low propagation loss and defect-free interface resulting from thermally (local) grown oxide; the combination of p-silicon, SiO_2, and gold results in self-rectifying operation to enable the realization of multilayer memory. An on-off extinction ratio of 10 dB is demonstrated for a 5 mm long device. The proposed device shows inherent stochasticity property where set (writing) voltage reduces in each set-reset cycle which can be used for optical readout of synaptic weight for neuromorphic computations.

5.1 Silicon based nanophotonic resistive switch

The resistive memory technology is considered to be the future of high-speed computing and information storage with low power

consumption for variety of applications [66], [139]–[142]. Silicon has proven its capability to be used in memristor based devices [143]–[146]. Memristor or resistive memory is a two-terminal device in which switching between low-resistance level and high resistance level usually in a metal-insulator-metal (MIM) structure forms the basis to realize a scalable memory [66]. Information processing at optical frequencies has its own advantages specially in terms of bandwidth [147]. The photonic devices are rapidly emerging as a saviour to meet the bandwidth requirements in communication networks and in high-speed computing [18], [30], [148]. Combining the strength of the resistive memory with that of the photonics has resulted in an interesting memory element [149]. Reading the state of a resistive memory optically can enhance the bandwidth of operation while providing less interference with the electric write signals which in turn increases the information processing capacity [83], [149], [150]. A CMOS compatible version of an optical resistive memory can be regarded as a potential platform to realize a multi-level system for information storage and processing. A resistive memory with optical readout functionality in some nanophotonic structure can be the key to build such system. Silicon photonics at real nano scales along with the current advances in electronics can be the key to realize low power on-chip communications [11], [87], [151]. The miniaturization of the photonics devices to the scale of CMOS transistor is hindered by the diffraction limitation. The coupling of the electromagnetic wave with the electrons is a potential candidate for confining the light beyond the diffraction limit. These surface plasmon polariton (SPP) waveguide suffers from high metallic losses [11]. The controlled hybridization of the plasmonic and dielectric photonic waveguides results in long propagation with nano scale confinement. The hybrid waveguide has shown an excellent optical property with a very small mode area of $\lambda^2/200$ and low loss [59], [88], [132], [152]. A leaky mode confinement in a high refractive index layer underneath the hybrid plasmonic (HP) confinement layer can further reduce the losses and can control propagation characteristics of the hybrid plasmonic

waveguide for nano scale devices [59], [88], [132]. This hybrid plasmonic concept can be used to make a silicon nanophotonic resistive memory.

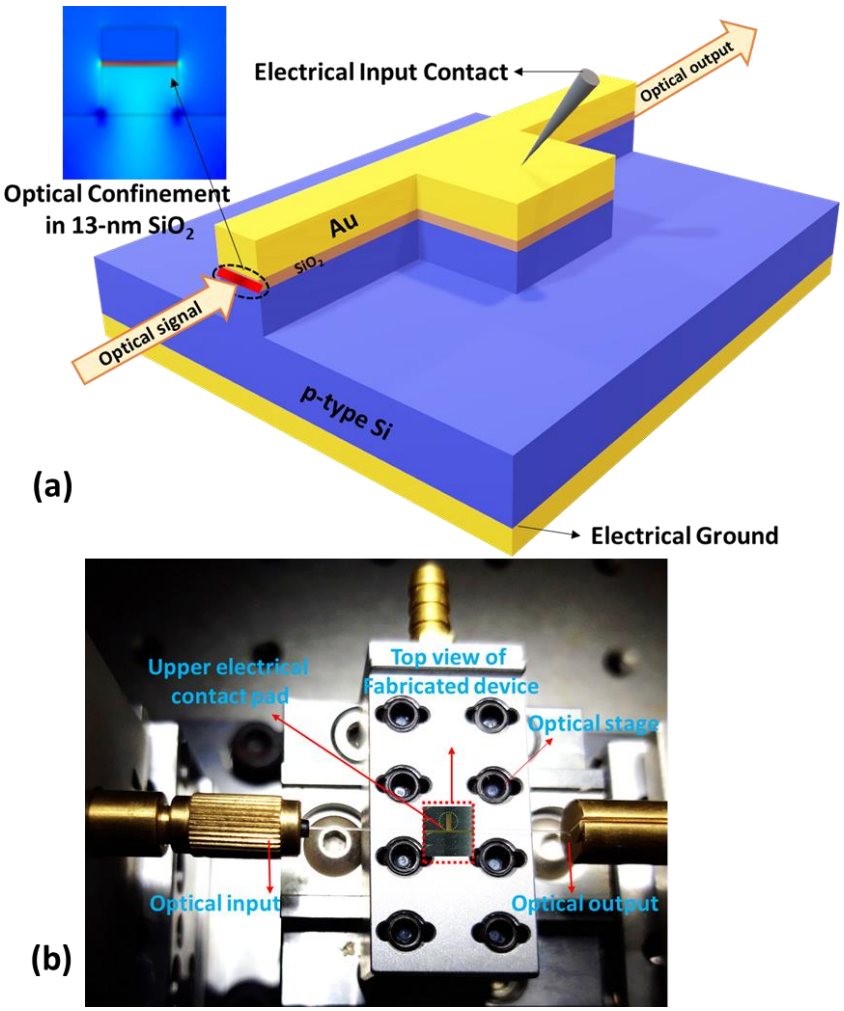


Figure 5.1 (a) Schematic of the proposed resistive memory device with optical readout capability, the plasmonic mode is confined in the 13-nm of silicon dioxide layer. The 1550-nm telecommunication wavelength is used for the reading the state of memory device. Inset shows field confinement in dielectric region in hybrid plasmonic waveguide. (b) Top view of the fabricated device including alignment stage and input/output lensed optical fibre used to excite the light into the device and to collect the light out from the device.

In this work, a resistive memory with electrical write and optical read-out function using a CMOS compatible silicon nanophotonic

structure (hybrid plasmonic waveguide) is proposed. The optical readout makes the device less prone to error with a clear optical extinction ratio of 10-dB and providing high bandwidth operation at 1550-nm of wavelength. The device exhibits characteristics necessary for neuromorphic computation for AI applications. The set voltage decreases in each succeeding set-reset cycle from 10 to 6.2 volts which is similar to the adaptive weights needed for AI computing. Instead of popular MIM structure we used MIS, where p-Si provide two-fold benefits- low loss waveguiding and self-rectifying nature essential for fabrication of 3-D stacks of the memory array.

5.2 Device design & fabrication

The proposed device, Figure 5.1(a), consists of high quality thermally oxidized 13-nm thick layer of silicon dioxide sandwiched between two electrodes. The top electrode is 150-nm thick gold deposited using DC sputtering and p-type silicon as the bottom electrode which is back plated for the electrical contact. The leaky optical mode from high index layer of silicon is coupled with surface plasmon polaritons (SPP) oscillating at interface of gold and SiO_2. The high intensity TM polarized optical mode is confined in 13-nm thick oxide layer. The mode field distribution is shown as inset in Figure 5.1 (a). The proposed device exhibits a low propagation loss of 12 dB/cm in a 350-nm wide waveguide for hybrid plasmonic mode guided in a 11-nm thick SiO_2 [132]. Figure 5.1 (b) shows the top view of the fabricated device including alignment stage with input and output optical fibres. The lensed optical fibres are used to excite the light into the device and to collect the light out from the device. The output optical signal is characterized on the photodiode as wells in the optical spectrum analyser. A 375-µm thick p-type silicon substrate is oxidized using a rapid thermal annealing furnace at 1000^{o}C for 10 minutes. The electron microscopy and the Energy-dispersive X-ray spectroscopy (EDAX) reveal a top surface with 10.42% of oxygen atoms and

89.22% of Si atoms as shown in the inset of Figure 5.2. As shown in the Figure 5.1 (a) the extended top gold layer acts as an actual top electrode to provide the appropriate coupling of electrical RF pulse with the HP mode guided in the waveguide. A further large contact pad (top gold layer) can slow down the performance of the device by increasing RC time constant. The oxide layer sandwiched between metal and silicon layer provides the oxygen ions for the formation of conductive bridges (CB); the controlled diffusion of the metal ions into the oxide layer helps in providing optical resistive memory effect as shown in Figure 5.9.

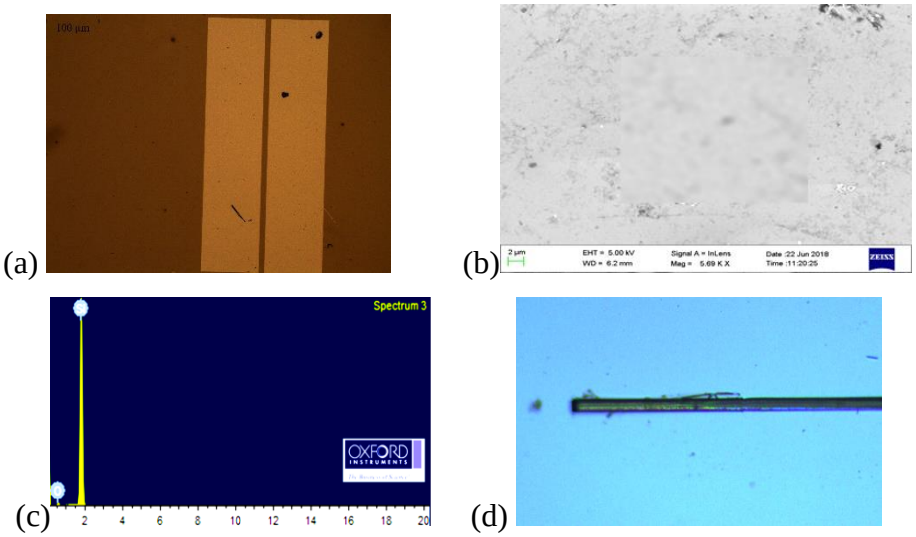


Figure 5.2 (a) Optical image after the photoresist development (b) SEM image of top layer of SiO_2 (c) EDAX of thermally grown SiO_2 (d) after etching the rib of fabricated waveguide.

5.3 Electrical characteristics and measurements

The application of voltage on the silicon oxide layer breaks it down into oxygen ions and silicon. These oxygen ions help in the formation of the CB between metal and silicon. The formation of CB leads to high current flow between electrodes i.e. metal (gold) and the p-silicon. Further, upon high current flow the gold ions started diffusing into the SiO_2 layer. The Gold ions exhibit large optical

absorption when light passes through the silicon oxide layer which leads to a high extinction ratio in the process of optical readout. Figure 5.3 shows the measured I-V characteristics with a clear hysteresis loop of current. A ramping pulse voltage from 0 to 10 volts is applied on the top electrode of the device while another electrode is kept grounded. The applied voltage is ramped for 1-ms from 0 to 10 volts with a pulse width of 5-µs. It is observed that in each succeeding set-reset pulse cycle current increases from its value during the previous cycle and set voltage decreases. After the second set-reset loop current difference become less and decreases slowly. A clear difference between first and the tenth loop is shown in Figure 5.3; inset shows the I/V loop for all the cycles studied. The initial IV measurements are done with the Keithley 4200A source meter by ramping the voltage from -10 V to +10 V. The hysteresis of resistance voltage curve is shown in Figure 5.4 depicting a very large resistance difference of 20-MΩ in set-reset cycle is observed between 0.8 to 6.2 volts. The proposed device structure is such that it forms a p-n junction along with the dielectric in between (Silicon-SiO_2-Gold) which leads to a negligible leakage current (tens of nano-ampere) at negative biasing cycle. This self-rectifying property of our device makes it eligible for the 3D integration on monolithic silicon chips.

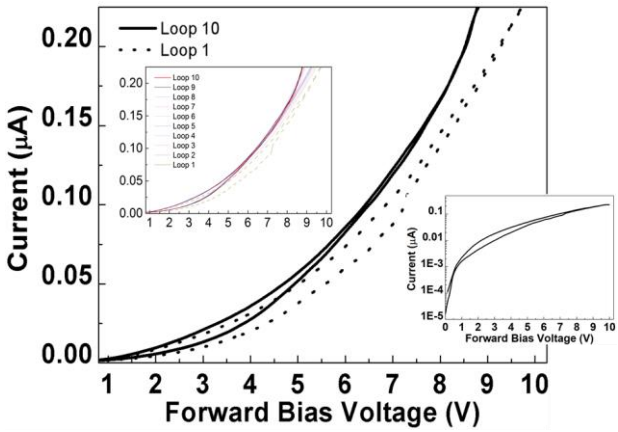


Figure 5.3 Current voltage characteristics for the ten set-reset pulse cycles. The dimensions of active resistive memory device are 0.2×5 mm (lower inset shows logarithmic IV curve for one cycle).

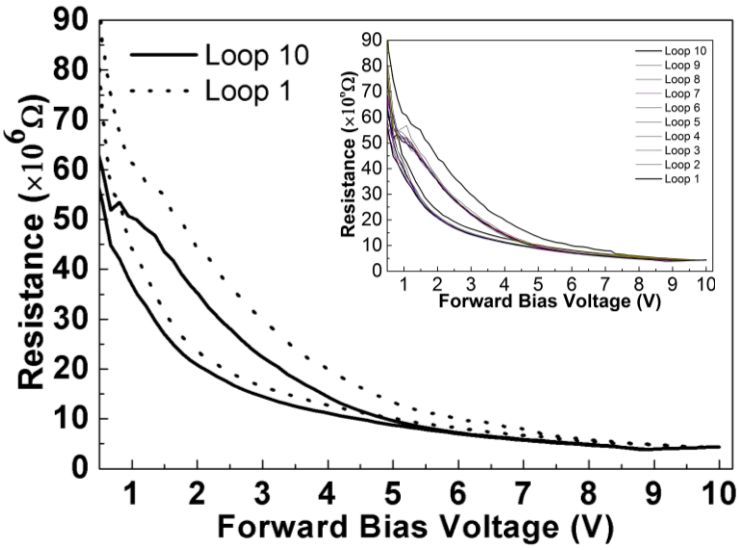


Figure 5.4 Variation in resistance of the device with change in voltage across the resistive memory. The resistance loop shows a very large difference in the resistance in forward and reverse cycle.

The current-voltage characteristics were again measured by slowly varying the voltage across the device. A sharp change in current can be seen just after the 7 V is applied, Figure 5.5. As the speed of varying the voltage increases the opening of the hysteresis curve decreases. The larger the time of applying voltage the larger and better will be hysteresis curve, as the local temperature increases. The device has shown nonvolatile characteristics. After a voltage of 4 V the small increase in the current can be observed up to 7 V. On decreasing the voltage from 7 V, the device remains in LRS until the 0 V is reached. When the voltage further decreases in the negative direction the very small current flows through the device resulting in good rectification ratio, Figure 5.6. A large rectification ratio of 400 times is observed when device is in HRS and 700 times when device is in HRS. This rectification ratio is sufficiently large for multilayer fabrication allowing high density packaging. The joule heating effect on the hysteresis cure and the SET voltages is verified by heat the DUT while measuring the IV characteristics, Figure 5.7. The SET voltage decreases from 8 V to 4 V by varying the temperature from room temperature to 175 ^{o}C.

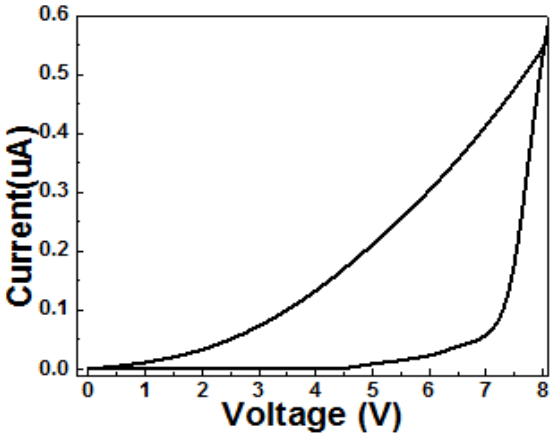


Figure 5.5 Current voltage characteristics for one set-reset pulse cycles recorded by slowly varying the voltage. The dimensions of active resistive memory device are 0.2×5 mm.

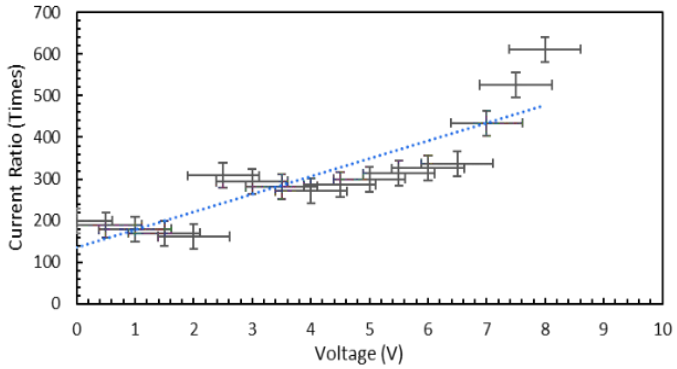


Figure 5.6 Rectification ratio is calculated for many cycles and average error graph is plotted. Showing a good rectification ratio of 600 times.

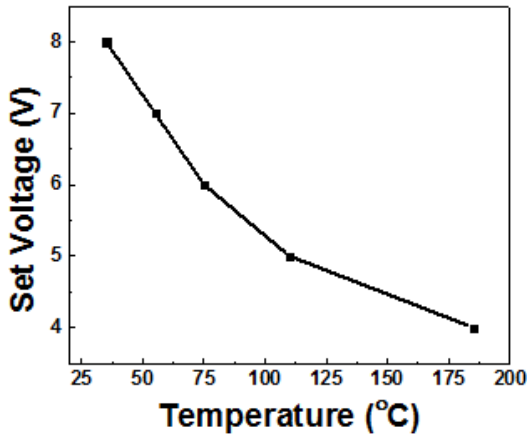


Figure 5.7 The effect on the set voltage with increase in the temperature.

5.4 Optical waveguiding characteristics

For the proposed nanophotonic resistive switch based on hybrid plasmonic waveguide, numerical analysis is done to analysis the mode profile and light propagation. The Presence of a high-index silicon layer and thermally grown SiO_2 on it provide us an acceptably low loss of 12 dB/cm for hybrid plasmonic mode guided in an 10-nm thick SiO_2. The dielectric constant for the metal Au is − 115.13 + i 11.259. The Figure 5.8 shows the mode profile for the simulated hybrid plasmonic waveguide. The maximum intensity can be seen in the 10-nm thick dielectric waveguide. The real effective refractive index for this hybrid mode is 2.08. The effective mode area is near $\lambda^2/200$.

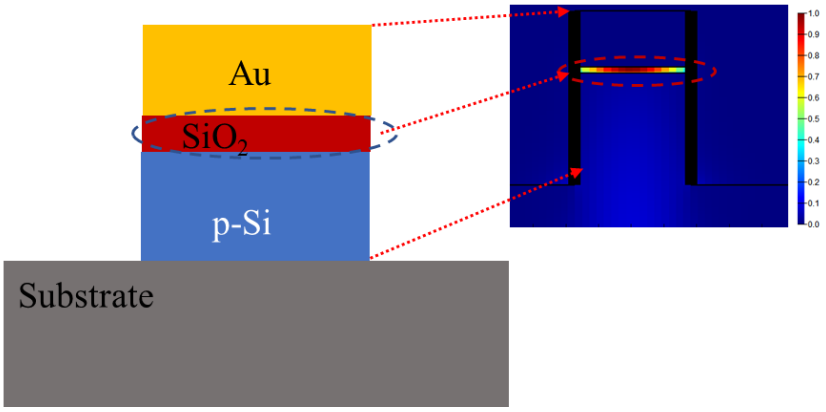


Figure 5.8 Schematic of the hybrid plasmonic waveguide used for the simulation. The inset shows the guided hybrid mode with maximum intensity in thin dielectric layer.

5.5 Optical measurements

The optical readout has the benefit of large bandwidth of operation and do not interfere with the electrical write signals hence less prone to error. The optical intensity transmitted through the device is measured by changing the voltages. The optical output shows the similar hysteresis loop as that of electrical on the application of the voltage, shown in Figure 5.10. The optical readout from MIM devices

is hindered by high optical absorption of metals. To overcome this, the hybridization of optical and plasmonic mode is enabled by replacing one of the electrodes with p-silicon. This hybridization of leaky optical mode and plasmonic mode helps in realizing low loss plasmonic device with few nano-meters of optical confinement. It is observed that in high resistance state of the proposed device the optical output intensity is high i.e. the device is optically ON. The optical intensity decreases when the device is in low resistance state, because of the diffusion of metal ions into the oxide layer to switch the device optically OFF, Figure 5.9. When the reset voltage of become less than 0.8 volts the optical intensity again increases. A clear 10-dB extinction ratio is found in the voltage range 6-10 volts. It is difficult to read the status electrically in this range as resistance difference remains very small. Figure 5.10 (inset) shows the relation between the increase in current value with a change in the intensity of the optical signal when device is in low resistance state.

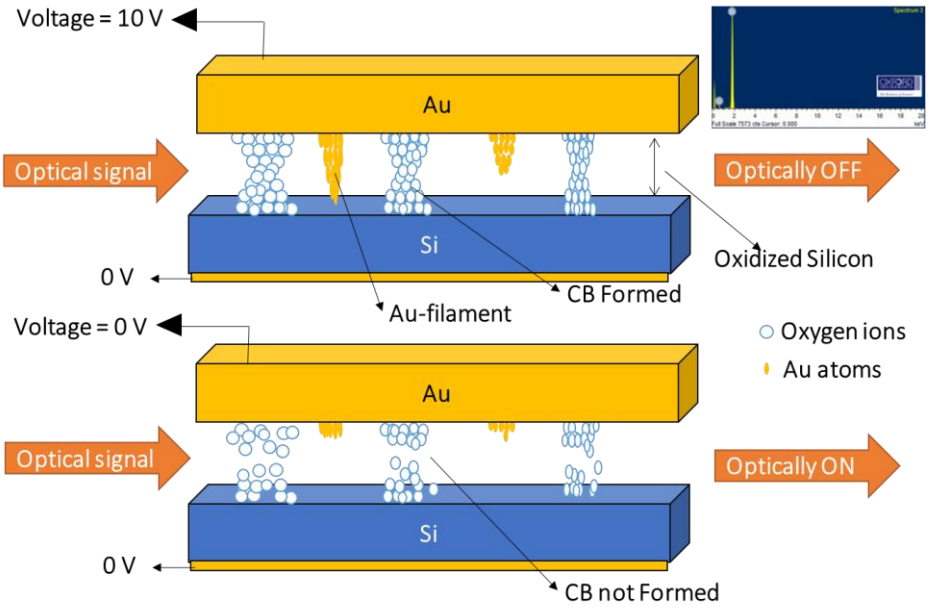


Figure 5.9 The schematic shows the effect on optical signal on the formation of conduction bridge and gold metal ion diffusion into silicon dioxide layer. The inset shows the EDAX which confirms the formation of oxide layer over the silicon top surface.

Table 5.1 Comparison between optical and electrical switching characteristics of nanophotonic resistive switch.

Parameters	***ECM*** [83]	***VCM*** [150]	***PCM*** [64]	***This work*** ***(ECM+VCM)***
Optical Extinction Ratio	12 dB	12 dB	0.04 dB	10 dB
Switching Energy (μW)	0.15	0.200	2700	0.3
Retention	Non-Volatile	Volatile	Volatile	Volatile
SET/RESET Voltage (V)	9/-3	3/ 0	10/0	7/0
Endurance	few 100	1000 &more	few 100	500 & more
Self-Rectification	Low	No	No	Very High

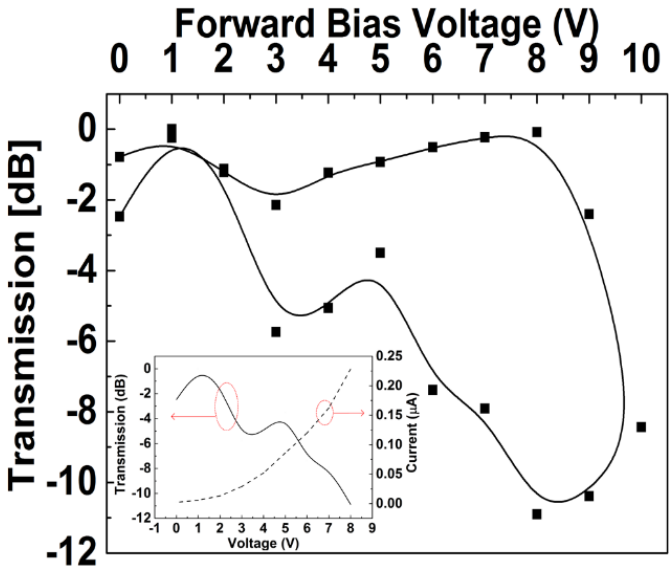


Figure 5.10 Variation in the transmission intensity of the transmitted light (1550-nm wavelength) on the application of the voltage loop (from 0 to 10 volts). Inset shows effect on optical intensity with change in electrical current on variation of the bias voltage

A relation between the electrical current and the optical intensity can be easily pointed out – the higher the current lower is the optical intensity at the output of the device. As the current increases, the overall temperature of device increases which results in a diffusion of larger number of Gold atoms into SiO_2 which is also shown in the

Figure 5.9. The more the number of the metal ions more will be the absorption of the optical signal. The diffusion of the metal atoms in the same region where hybrid plasmonic mode exists makes our device optically more responsive than the devices that rely only on optical guided mode. Table 5.1 shows the comparison between various nanophotonic resistive switch with optical readout.

5.6 Application in neuromorphic computation

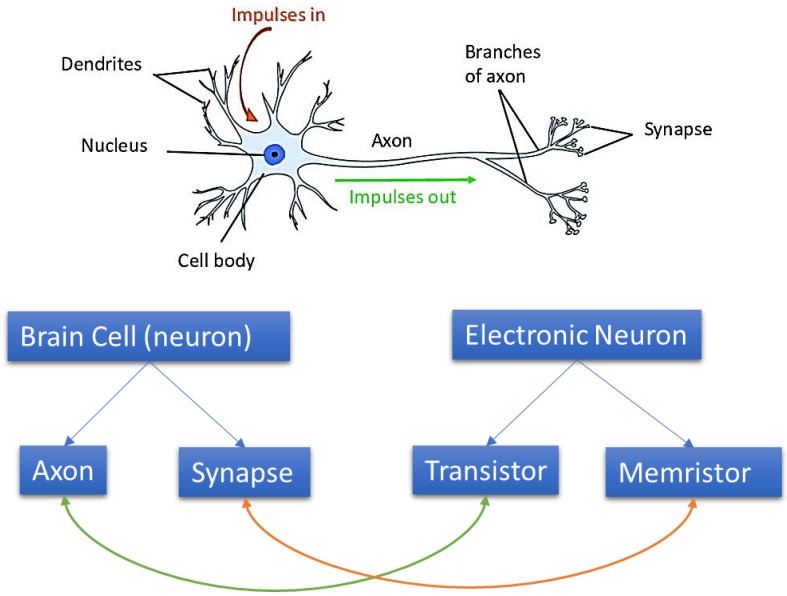


Figure 5.11 Showing relation between electronic neuron and brain cell neuron.

Recently there are reports on the increased research interests in neuromorphic computing for the application in artificial intelligence [153]–[155]. A behaviour of memristor as the neuron is based on an integrate and fire model. The small input voltages from different neurons (resistive memory) accumulated and once a threshold voltage reaches, the active layer provides a conduction bridge to it and a spike is generated [156]. The resistive memory recalls its last state of the resistance. A single electronic neuron requires many CMOS transistors on the contrary only one memristor device is required for one synapse,

shown in Figure 5.11. For the application of artificial intelligence adaptive weights are needed [72]. Similarly, our proposed device adapts the set voltage with increase in number of set-reset cycles.

Figure 5.12 shows the change in set voltage with respect to increase in number of set-reset cycle. After the first set-reset loop the set voltage decreases from 9.5 to 7.5 volts. Thereafter the rate of change in set voltage decreases gradually. This property makes our device eligible to be used in neuromorphic computing for AI application. Its optical counterpart shows the similar property by changing the optical extinction ratio at different set voltages. The diffusion of metal ions into the oxide layer increases on every set/reset cycle which will result in higher optical extinction ratio at lower voltages. The optical extinction value can further be improved by using a proper adhesion layer between the dielectric (silicon dioxide) and top electrode (gold). Using (3-Aminopropyl) trimethoxysilane (APTMS), Ti, or Cr as the adhesion layer between the two layers has shown enhancement in coupling of SPP with the optical electromagnetic field, which in turn increases the optical extinction ratio [157].

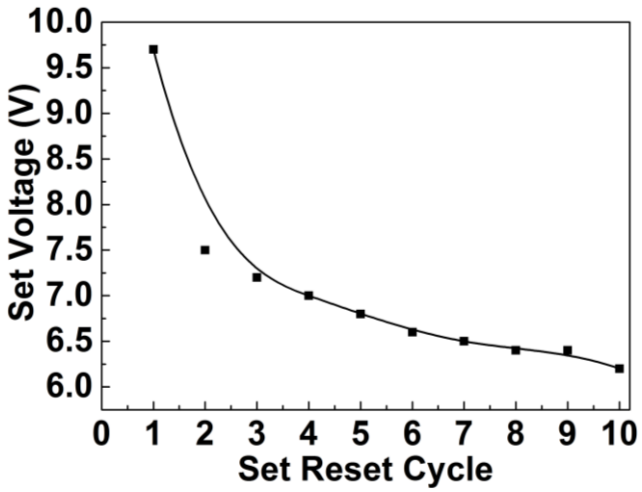


Figure 5.12 Effect on the set voltage with respect to the operational cycle of set/reset voltage. The change in set voltage tell its stochasticity inheritance property.

5.7 Material analysis and scope for improvement

In ECM based resistive switching the major role is played by the material used for metal contact, as the atoms of this metal diffuses in the buffer layer to for a conduction bridge. If ionization energy of metal atom is large it is difficult to ionize, hence difficult to diffuse on the influence of external electric field for ECM. The small electronegative material like Al can easily diffused and they move with the influence of the applied field. Whereas large electronegative material is difficult diffuse, and they don't follow the electric field direction e.g. Pt, as shown in Figure 5.13. The table 1 show the various metal atoms property for plasmonic waveguide based nanophotonic restive switch. At MIGS metal induced gap state due to the roughness the atoms ionize, and these can help in the diffusion of the metal atom. But easily diffusible material has drawback of low endurance value, as large number of atoms gets diffused and make permanent low resistance path. Whereas metal Au and Pt difficult to diffuse but has large endurance.

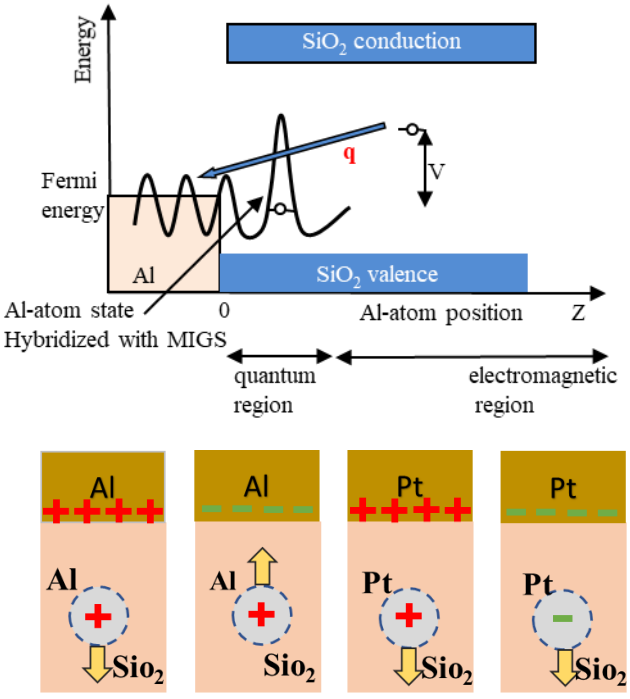


Figure 5.13 Metal atom diffusion with respect to the applied field and ionization energy is shown.

Table 5.2 showing comparison between different materials for ECM in nanophotonic resistive switch

S.N.	Gold	Silver	Copper	Platinum	Aluminium
Density (g/cm^3)	19.3	10.5	8.96	21.5	2.70
Atomic radius (A_0)	2.14	2.11	1.96	2.13	1.84
Electron affinity ($Kjmol^{-1}$)	222.749	125.624	119.159	205.321	41.762
Electronegativity	2.4	1.93	1.9	2.2	1.61
Ionization energy ($KJmol^{-1}$)	890.128	730.995	1745.482	864.393	577.539
Work function (ev)	5.47	4.64	5.10	6.35	4.2

In summary for top metal requirement for nanophotonic resistive switch:

- Low ionization, work function and electronegative material is best for ECM
- It has high optical extinction ratio, but it has very low endurance
- A high electronegative material with low ionization and work function is better choice
- A compromise between endurance and optical extinction must be made
- Material engineering like defects in buffer layer to create more ions in MIGS can be a solution with high electronegative material.

5.8 Summary

A self-rectifying electrically writable resistive memory with optical readout based on silicon nanophotonic structure is proposed. The optical mode is made to guide in the thin layer of SiO_2 where the formation of conduction bridges occur which can easily detect resistive memory effect. The electrical control of the guided nano optical mode in the proposed device shows inherent stochasticity for neuromorphic computation. An optical extinction ratio of 10-dB is measured at an

operating wavelength of 1550-nm. The device shows a low power consumption of 0.15-pJ which is tested up-to 2-MHz of frequency set-reset pulse cycles with no distortion. The presence of silicon, in our device, in place of one of the two metal layers in popular MIM structures provides an effective control over mode hybridization and over the formation of conduction bridges in insulating layer. The proposed device also carries an interesting property of inherent stochasticity with adaptive weights which can be utilized for applications like neuromorphic computing in artificial intelligence. The self-rectifying nature, CMOS compatibility and optical confinement much below the sub-diffraction limitation of light ($\lambda^2/200$) make the proposed device a potential candidate for large-scale integrated photonic circuits for applications in communication networks, computing and information storage.

Chapter 6

Optically Assisted Electro-Metallization in Resistive Switch Device

From the previous discussion, it is noted that the optical extinction ratio of the nanophotonic resistive switch can be improved by increasing the metal atom diffusion in the controlling buffer layer (insulator). The top metal electrode should have low electronegativity, low ionisation energy, low density and should support SPP propagation with low loss of 1550-nm wavelength. Considering all these parameters an optically assisted electrically writable non-volatile resistive memory device is proposed. The three-layered device of Ag/TiO_2/p-Si has shown large hysteresis current loop in the presence of a blue wavelength of light at a lower voltage. The electrical resistive state of the device is read out at 1550-nm of wavelength. The pump light generates extra hole-electrons in TiO_2 which lowers the set voltage compared to dark. Thus, the process avoids undesired current overshoots. The optical guidance in few nanometre layers of TiO_2 and the formation (low resistance state) and dissolution (high resistance state) of conductive path filament is discussed. The device has also shown its capability to use as an optical switch with an optical extinction ratio of 16 dB for 1 mm of device. The proposed nanophotonic functionality can be useful in realizing ultra-compact on-chip devices for optical switching, modulation and neuromorphic computing.

6.1 Photodetection in hybrid plasmonic device

Silicon has an energy band gap of 1.1 eV. It cannot be used for the detection of light beyond 1.1 μm wavelength of light, as beyond that wavelength the light is not enough to make electrons jump from

the valence band to the conduction band. The internal photoemission-based technique can be used using the Schottky junction. Schottky based photodiode has a high dark current and leakage current. To overcome this a buffer layer of SiO_2 can be placed. The photodetection based on MIS is similar to our proposed hybrid plasmonic waveguide. The schematic of the proposed simulated device is shown in Figure 6.2. The device is numerically analyzed to study the photodetection behavior the results were required to analyze the effect of carrier generation in the proposed resistive switch [158]. The difference in dark current and photocurrent is found out enough for the clear distinction between them. As the insulator buffer layer is used the charge carriers generated crosses the junction is less and hence current came out in 0.4 pA range. Which on experimentally measurements is measurable due to fabrication errors and materials impurities.

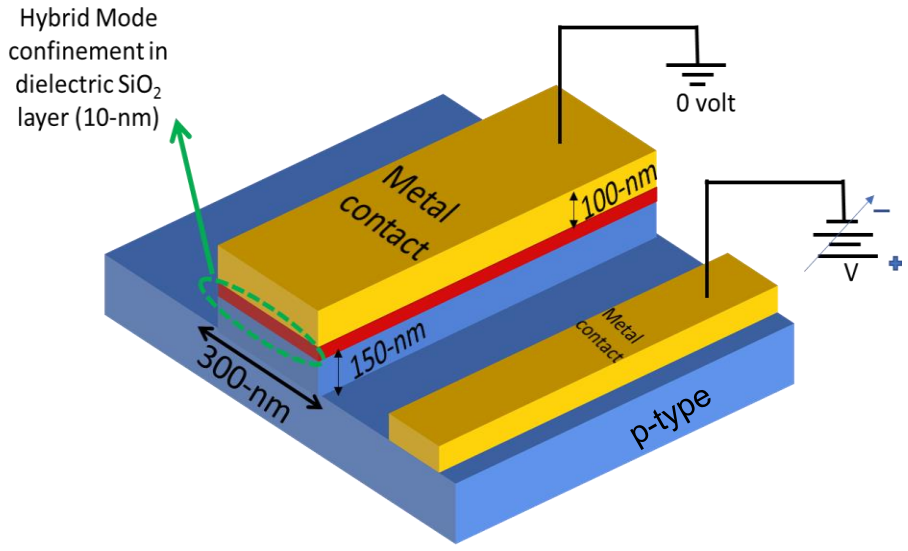


Figure 6.1 Schematic for photodetection used for numerically analyzing the photocurrent and dark current to be used in a resistive switch mechanism.

The 3 dB bandwidth responsivity is calculated, and it is clearly seen that this type of photodetection has a good frequency response. The response is as high as 80 GHz, as shown in Figure 6.3. The ratio of

dark to photocurrent is sufficiently large to be detected without any error. The insulator layer helps in blocking the leakage current, but it also blocks the photogenerated charge carriers to transfer from metal to Si, resulting in low current. The device is limited by measuring instruments. Photodetection of visible light can be helpful in the resistive switch mechanism.

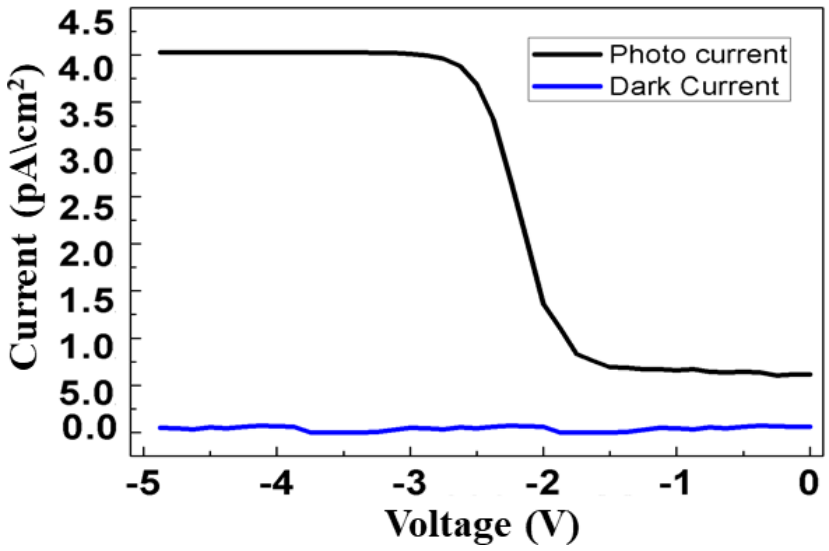


Figure 6.2 Photocurrent vs Dark current for the MIS based device.

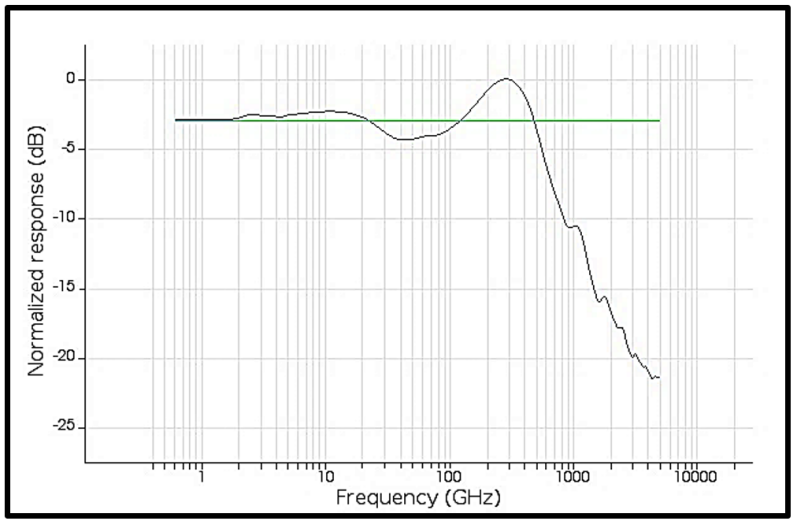


Figure 6.3 3dB frequency response of the MIS photodetection, it incredibly fasts response shows it's capability for state of art applications.

6.2 Optically assisted electro-metallization

To improve the photo-current in silicon based on device presented in above section, a buffer material which upon application of pump light can generate photogenerated charge carriers can be used. This scheme can provide an extra dimension to control the overall device current values. This process can be used with resistive switching mechanism [85]. The miniaturization of photonic devices gave us the ability to control the light signal with changes in the device at nano dimensions on the application of the external electric field. The resistive switch works on a mechanism involving nano dimension physical and chemical changes in the material [84], [142], [159]–[161]. The resistive switch is not limited by the transistor scaling which leads to high-density fabrication with low power consumption devices [162]. These are the two-terminal devices separated by a controlling layer which can change its resistance state between high resistance state (HRS) and low resistance state (LRS)[163]. The change in the resistance is governed by the formation and dissolution of the conductive filament in the active material between two electrodes. The filament formation broadly governs by the two mechanism Valency change effect (VCM) and Electrochemical metallization (ECM)[83], [159], [164], [165]. The mechanism by which the formation of ions takes place decides the mechanism from these two. The ion diffusion plays a crucial role in filament formation. These changes in the nano-dimensions with light as a signal can benefit dually- first is light signal can record these changes and the light signal can be controlled by these diffused ions. The photonic devices suffer from the diffraction limit of light. To overcome this hindrance the light can be coupled with the plasmons known as surface plasmon polariton (SPP) which can be used to guide the light in even a few nanometres of dimensions [36], [94], [102], [166]. The typical plasmonic device contains a metal-insulator-metal (MIM) configuration, which is similar to that of a resistive switch. These plasmonic devices have a direct relationship

between the material and light which makes it suitable to record the small changes in the material. These plasmonic devices suffer from large ohmic losses results. To overcome this hurdle a new scheme is proposed where SPP is coupled with leaky optical mode results in hybrid plasmonic mode. The hybrid plasmonic devices usually have metal insulator semiconductor configuration. They maintain the nanoconfinement of light with low loss waveguiding. A similar configuration has been used by [158] for the application in the optical readout of a resistive switch. The filament formation in those devices is controlled by the electrical phenomena and the position of the filament is random which some time results in undesirable current overshoot result in short life span of the device i.e., low endurance.

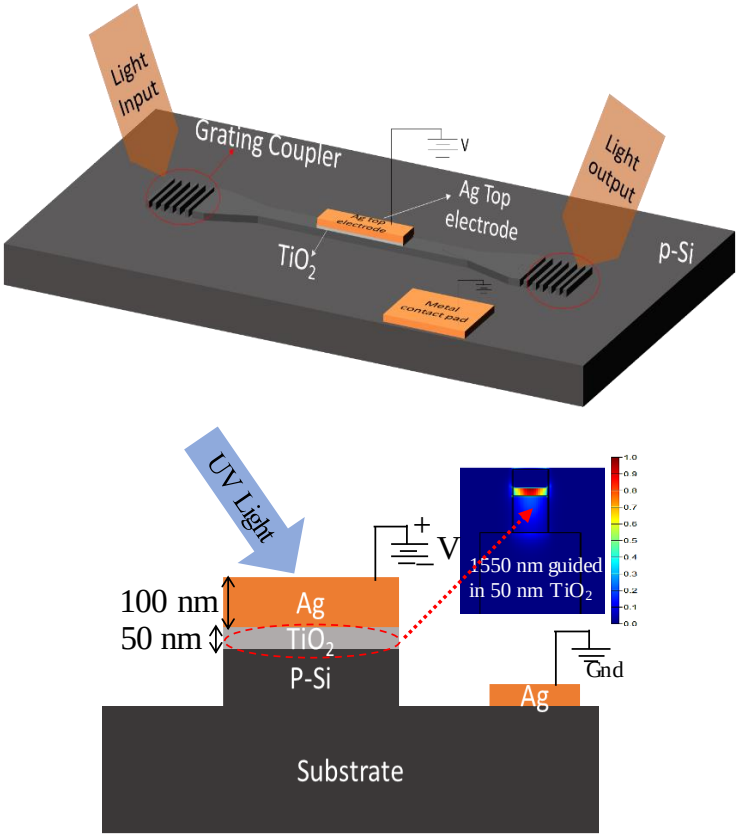


Figure 6.4 (a) The schematic of the proposed device. The blue light is used to control the electroforming in the TiO_2 layer. The 1550-nm is used to guide the light. the inset image shows the mode profile of the guided light. (b) Schematic of the cross-sectional view of the proposed waveguide. The inset showing the guided mode analyzed by numerical analysis.

In this work, we propose a non-volatile nanophotonic resistive switch which is controlled by the external UV light to avoid undesirable overshoot of the current. The 1550-nm communication wavelength signal is used to read the status of the resistance. The proposed device forms filament at a lower voltage on the illumination of external UV light. The generation of extra hole electron pairs results in lowering the filament formation voltage. The proposed device can be used as the optical switch with 16 dB of extinction ratio for a 1 mm long device. Along with the experimental measurements, the chapter also discusses the simulated optical characteristics of the waveguide. The device has the application in the optical switch, memory, and neuromorphic computations.

6.3 Device design

The proposed three-layered nanophotonic device is arranged in metal Insulator Semiconductor (MIS) configuration. A dielectric layer of TiO_2 is a sandwich between two electrodes. The top electrode is Ag of 100 nm and the bottom electrode is a highly doped p-Si substrate. The thickness of the deposited TiO_2 is found out to be 50 nm. The bottom electrode is then connected with other Ag metal for providing contact with the external contacts, Figure 6.4(a). The gold coated probe arms were used to provide the contacts over the two-metal contact. A UV light source is placed over the device. The lensed fibre is used to couple the light from a tunable laser source to the device and output is taken from the other end using a collimator lens coupled with optical fibre. The spectrum is observed in the Optical spectrum analyzer and the photodiode current was measured. Figure 6.4(b) shows numerically calculated the mode filed.

On the application of the external electric field, the Silver ions that exist because of metal-induced gap state at the interface of the metal and insulator start to diffuse into the insulator layer TiO_2.

Initially, the diffused ions try to align themselves in the direction of the electric field applied. The direction of the electric field is from the top electrode towards the bottom electrode. The positive ions of the Ag experience the ions concentration gradient which also makes them diffuse into the insulator layer. When the ions reach the bottom electrode the effect of the external electric field vanishes and a large current starts to flow through the conduction bridge formed, making the device in low resistance state. The device remains in that state until the negative voltage of the same magnitude is not applied. Due to the large metal electrodes, it is expected that the device is having multiple filament formation results in unnecessary unavoidable conduction bridge formation. When a UV light is incident over the device the large amount hole electron pairs were generated and results in increasing the leakage current which in turn increases the local temperature and the process of metal atom diffusion ramps up results in conduction bridge formation at the lower voltage.

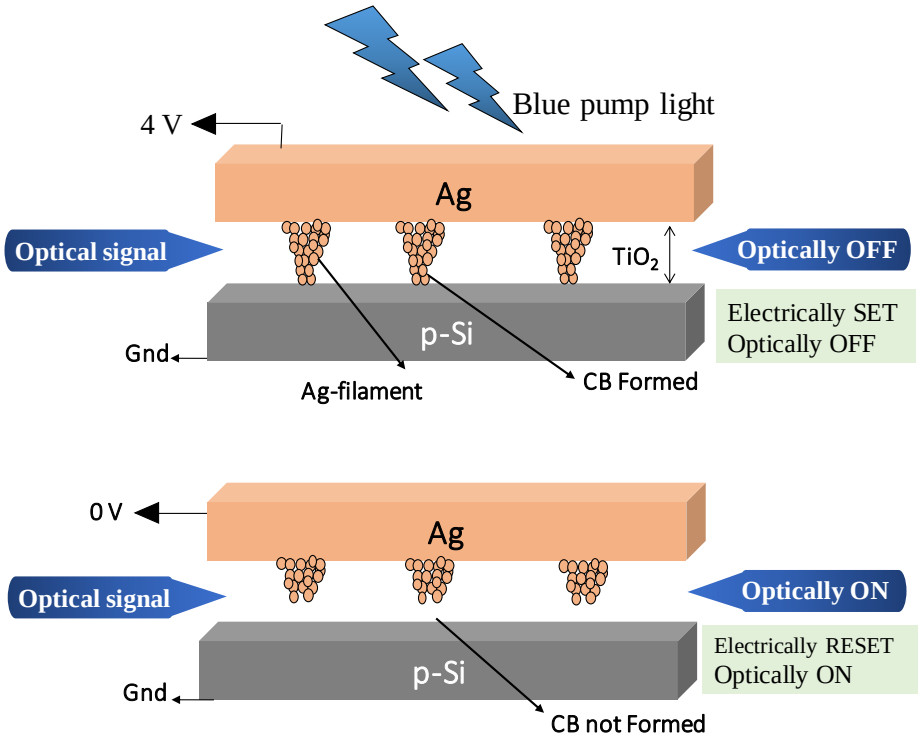


Figure 6.5 Image explaining the resistive switching mechanism and how metal atom diffusion effects the optical intensity.

6.4 Fabrication of proposed device

The device is fabricated on the heavily doped p-Si substrate. The TiO_2 ¬layer is deposited using sol-gel. The precursor used for the formation of the TiO_2 is titanium butoxide. The 35 ml of a precursor is mixed with 45 ml of ethanol until it turns milky. Then 1ml of acetone and 5ml of DI water are added which makes it transparent in color. When it is spin-coated on the p-Si the two-color are observed green (5000 rpm to 6500 rpm) and blue (7000 rpm to 9000 rpm). The thickness achieved for the blue colored coated TiO_2 using the ellipsometry is 50-nm. It is observed that the resistive switching characterizes were only presents for the blue colored TiO_2, Figure 6.6. Then the sample is annealed in a vacuum at 500℃ for 2 hours. The SEM image of the spin coated TiO2 film is shown in Figure 6.6. From the inspection, it is observed that the layer is uniform, crack free and has the constant color across the dimensions with the grain size of 30 nm approx., which depicts that the layer is of good quality and uniform in nature. The top electrode and the side electrode were deposited using DC sputtering to form contact pads. The p-Si acts as the lower electrode.

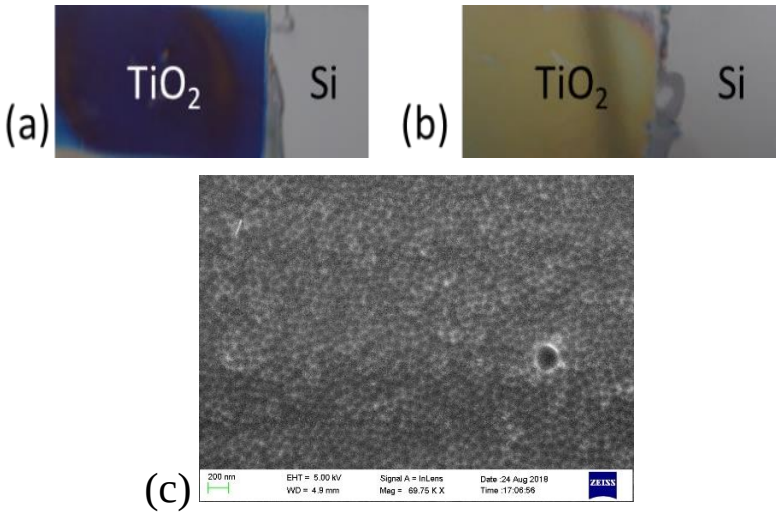


Figure 6.6 (a) TiO_2 coated at 8000 rpm, this sample has shown the resistive switching characteristics (b) TiO_2 coated at 5500 rpm, this sample has not shown the resistive switching characteristics (c) SEM image of top surface of TiO_2.

The device is planned to get coupled with the grating coupler of silicon air grating. The SEM image is shown in Figure 6.7(a). The grating is fabricated using positive photoresist PMMA-A4. For the etching purpose, DRIE is used with the chrome layer mask under the photoresist. The size of deposited chrome grain size is optimized for proper etching. The SEM images showing the grain size of chrome deposited at different DC currents resulting in small grain size at lower voltages, Figure 6.7(b).

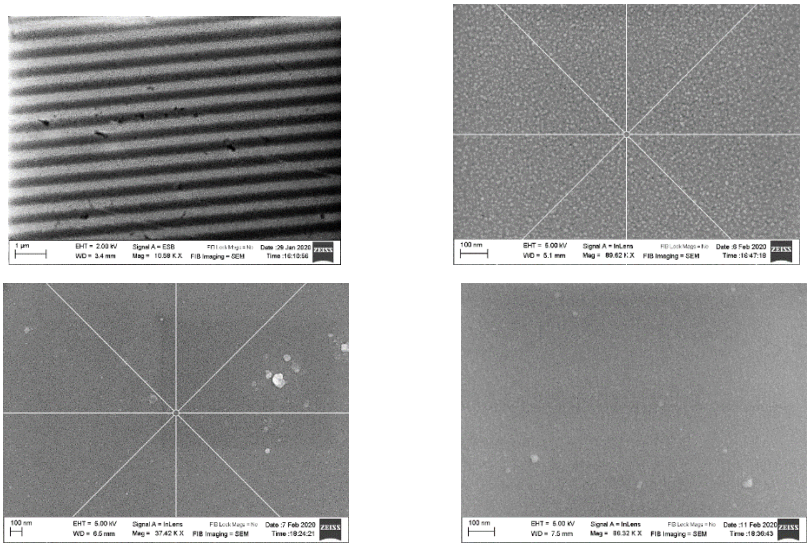


Figure 6.7 SEM image of (a) Gratings with 300nm period (b, c, d) Grain size comparison with different DC sputtered chrome.

6.5 Electrical measurements

A slow ramping voltage sweep is applied across the two-metal electrode. The lower electrode is placed over the p-Si. The top layer of the silver is also required for the SPP formation. A voltage sweeps of -15 to +15 is given and IV characteristics were recorded, Figure 6.8. For the device protection, the compliance current was set to the 0.1 mA. When the compliance current is kept large the device unable to handle the large current and burnt out. The SET voltage is high of 12 V when measured in dark. After the set voltage, a sudden spike in the current is observed resulting in a clear hysteresis curve. When the

voltage sweeps down from +15 V the device maintains its low resistance state only after a negative voltage of -10 V or more the device reset itself confirming the non-volatility nature of the device. The reported bandgap for the TiO_2 is 2.8 to 3.4 eV the energy lies in the UV spectrum. On the application of the external UV light, the electron jumps from the valence band to the conduction band resulting in the large electron-hole pair generation. This increases the photocurrent which in turn increases the local temperature. This results in a large amount of silver ion diffusion into the active layer. The SET voltage decreases to 4 volts from the 12 volts. This control over the set voltage gives us the extra dimensions of controllability over the device performance. It also helps in increasing the endurance of the device by avoiding unnecessary SET at other voltages. The optical measurement setup with probe arms for providing electrical contact is shown in Figure 6.9. tapered fibre is used for coupling the light to the fabricated device and out is collected from collimated lens fibre.

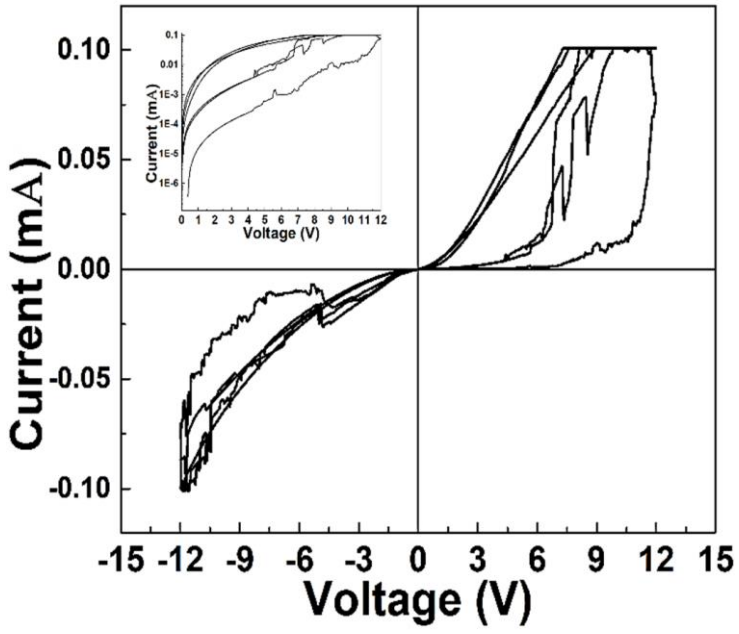


Figure 6.8 IV characteristics showing a clear hysteresis curve. After giving a negative voltage device reset itself proving non-volatile nature. The second and third curves are the set voltages when blue light is shine over the device with different intensity (inset shows logarithmic IV curve).

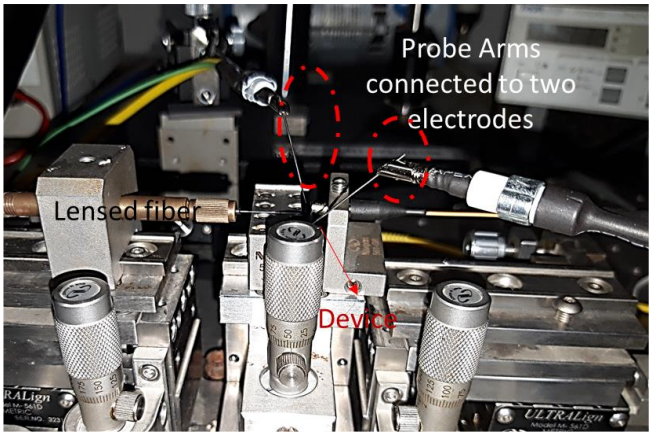


Figure 6.9 The measurement setup used for the optical readout of the resistance state of the device. Showing probe arms and lensed fiber used.

The measurements are more focused on increasing the optical characteristics such as decreasing the waveguiding loss and increasing the optical extinction ratio. The proposed device in Chapter 5 uses oxygen ion conduction bridge initially and then it follows the diffusion of the top metal atom-ions. The prediction is proved by the optical transmission graphs. Whereas in the Chapter 6 the device is predicted to use only electro-chemical metallization mechanism. The predicted mechanism is proved by comparing the transmission graph of both the devices. The prediction of the same is not possible only by the IV current voltage characteristics.

6.6 Optical waveguiding characteristics

It is essential to verify whether the optical modulation is due to the metal diffusion or the plasma dispersion in silicon on the application of the external electric field. The device is simulated and the effect of charge carrier depletion on the effective refractive index of the nanophotonic resistive switch is analysed. Figure 6.10 shows that the real part of the effective refractive index has small changes with changes in the applied voltage. The imaginary part which corresponds to the optical absorption in negligible comparing to the optical absorption due to metal diffusion. The electrons density

displaces from 10^{17} cm^{-3} to 10^{21} cm^{-3} on average in the top 4 nm of the silicon layer on the application of negative voltage. A similar fashion can be seen for holes displacement when a positive field is applied to the top electrode. The combined changes are reflected in the change in the effective refractive index. It is observed the change in holes affect the most in the modulation. The slope of the change in the number of the holes is similar to that of change in optical extinction when the resistive switching mechanism is used. Which validates that the experimentally measured results are because of the resistive effect.

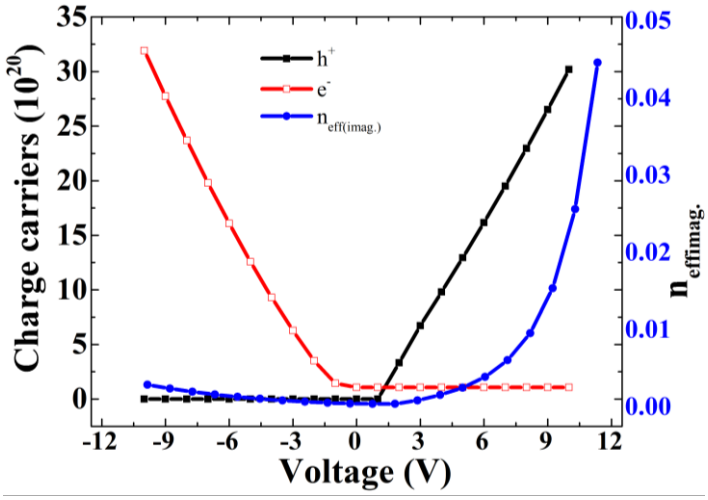


Figure 6.10 The variation in charge carriers and its relation to changes in effective refractive index, necessary to validate whether the modulation is due to the plasma dispersion effect or resistive switching.

6.7 Optical measurements

The lensed fibre is used to couple the 1550-nm light from the laser to the proposed device. When the voltage is zero the optical intensity is high as the voltage starts increasing towards the positive the more Silver atom ions starts to diffuse into the TiO_2 and block the path for the transmission of the light. At the output, intensity decreases up to 16 dB as the light is observed by the metal atoms, Figure 6.11. The results were measured with pump light (UV) is present. When the voltage starts decreasing few of the metal atoms try to move with the

electric field direction resulting in the improvement of the optical transmission at the output. The output is collected with the collimator lens and intensity is measured photodiode amplifier. Comparing to our previously reported result [158] with gold as the electrode the optical hysteresis is more profound because the electronegativity of the Au atom is large and it is once diffused then difficult to reverse with opposite polarity (explained in section 5.7). Whereas the silver has low electronegativity and ionization energy hence when reversing the voltage large amount of Ag ions reverses its direction of diffusion. The results depict that we can use it for optical switching applications. Figure 6.12 shows the effect of change in pump light intensity on the value of SET voltage. The set voltage decreases as the photocurrent increases because of the pump light. The two electrodes were given a slow voltage sweep from +12 V to -12 V. The device is shined with a blue light of 452 nm and the intensity of shined is varied. It is observed that the device SET at lower voltages as the intensity is varied from low to high intensity. This may be due to the reason that the in presence of shorter wavelength the titanium oxide absorbs light and extra hole electron pairs generated. As the leakage current increases, the diffusion rate of silver metal also increases due to the increase in local temperatures by joule heating.

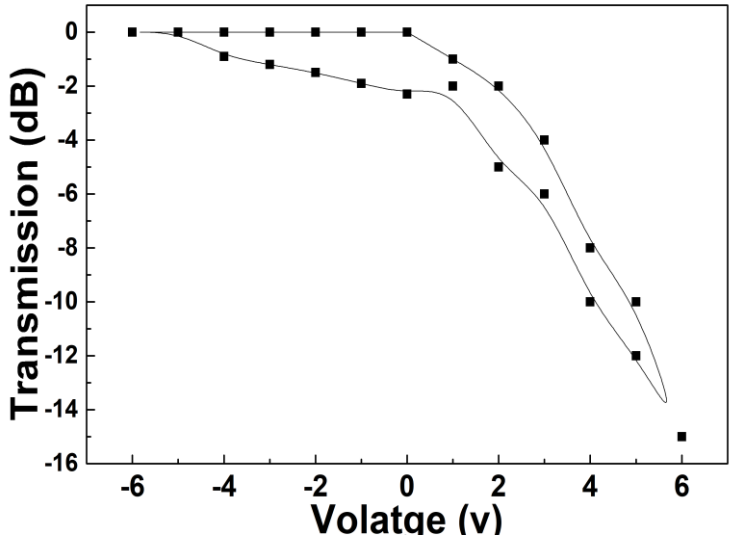


Figure 6.11 Measured changed in optical transmission with the change in the applied voltage. 1550-nm wavelength is used for the optical readout of the proposed device.

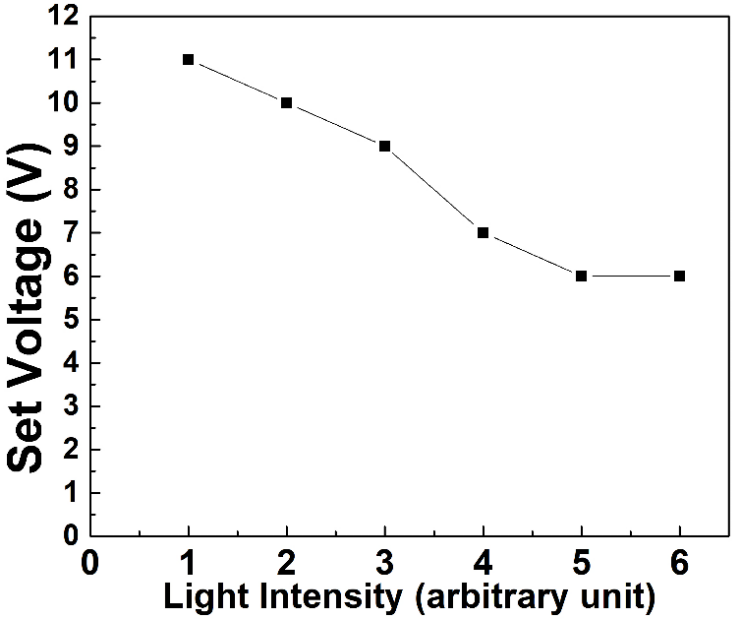


Figure 6.12 The effect of change in pump light intensity on the value of SET voltage. The set voltage decreases as the photocurrent increases because of the pump light.

6.8 Summary

The photodetection in a silicon-based device is demonstrated with an ON/OFF ratio of 100 times. The internal photoemission-based device uses silicon oxide as a buffer layer to decrease the dark current value. A 3 dB frequency response for 80 GHz obtained. An electrically writable optically controlled three layered nanophotonic resistive switch is proposed. The SET voltage of the device is controlled by pump light illuminating over the device. The optical readout of the resistance state is demonstrated using 1550-nm of wavelength. The optical extinction ratio of 16 dB is achieved for a device length of 1 mm. The switching characteristics of the device can further be improved by improving the optical coupling and by reducing the thickness of TiO_2. The optical readout is less error prone compare to electrical readout and large bandwidth operation. The electroforming of the conduction bridge at lower voltages reduces the overall power consumption of the device. The device can be used as optical switch with pump light activation. The proposed functionality of the nanophotonic resistive switch can be used to increase the endurance of the device by avoiding undesired current overshoot at higher voltages. The CMOS compatibility of the device design, nanoscale optical confinement and ability to control the SET voltage by using pump light make the proposed silicon based nanophotonic resistive device a potential candidate for a large scale integrated photonic circuits for the applications in optical switching, modulation and neuromorphic computing.

Chapter 7

Conclusion & Future scope

The present research work aims to design, fabricate, and analyze silicon-based nanophotonic devices for controlling optical signals at the nanoscale. A low loss hybrid plasmonic waveguide is designed, fabricated and characterized. For ultrafast communication, the device is modified for broadband ultra-low dispersion. The Field-Effect Transistors (FET) is used for electrical control of optical signals in a hybrid plasmonic waveguide. To further improve the electrical control a resistive switch is proposed and changes at the nanoscale are used to control the intensity of the optical signal of 1550-nm wavelength. Further, the experimental measurements are performed demonstrating the application of the proposed nanophotonic resistive device in the optical readout of the resistive switch, characteristics that help in neuromorphic computation and as an optical switch or intensity modulator.

The major contribution of the are summarized as follows:

- The light is guided in silicon at the nanoscale and then electrically controlled for applications in a compact integrated nanophotonic platform.
- A silicon-based nanophotonic waveguide is designed, fabricated, and characterized. The wavelength 1550-nm is confined in an only 10-nm thick layer of low index material with an acceptably low loss of 7 dB/cm in a 350-nm wide waveguide with a mode character of 0.5. The guided HP mode at nanoscales has a very small mode area of $\lambda^2/250$. The device is designed keeping in mind the less complex fabrication. The dielectric layer where 90% of light intensity resides is thermally grown from underlying silicon to reduced fabrication defects at the silicon-dielectric interface.

- The high index silicon layer is then modified by introducing grating to achieve an ultra-low dispersion of 10 pico-sec^2/m. The dispersion curve passes through zero value many times over a broad range of wavelengths. The broadband wavelength can be designed for the desired application by just changing the grating period. This makes our device capable of the application in high data rate optical fibre communication.
- To electrically control the light, MOSFET and tunnel FET like structures are incorporated in a hybrid plasmonic waveguide. The plasma dispersion effect is used to modulate light in the proposed waveguide. On varying the drain-source voltage a π-phase shift is achieved at a length of 204 μm and 1235 μm for TFET and MOSFET respectively. On varying gate-voltage, the change in effective refractive index is in the order of 10^{-5} which is smaller than that for a change in drain-voltage resulting in a 10^{-3} change in effective refractive index.
- A nanophotonic resistive switch is designed, fabricated, and characterized for improving the optical control. The plasmonic waveguide has a direct coupling of plasmons and electromagnetic fields which is beneficial for directly influencing the optical absorption. In the proposed device the direct metal diffusion in the active dielectric layer improved the optical absorption. The scheme is used for optical readout of resistive memory with a clear optical extinction ratio of 10-dB is achieved, with a low power consumption of 0.15pJ for one cycle. It is observed that the set voltage decreases gradually in each subsequent cycle. This property makes our device eligible to be used in neuromorphic computing for AI applications. Unlike the typically reported mechanism for resistive switching, our proposed device uses two techniques simultaneously i.e. valency change effect and electrochemical metallization.
- The optical extinction ratio is further improved by studying and analyzing the role of the top metal atom diffusion and replacing it

with another material with low ionization energy and electro-negativity. A light-activated resistive switch with optical accessibility with an improvement in the optical extinction ratio of 16 dB for a 1 mm device is reported with silver as the top electrode and Titanium oxide as an active dielectric layer. The three-layered device has shown a large hysteresis current loop in the presence of a blue wavelength of light at a lower voltage. The electrical resistive state of the device is read out at 1550-nm of wavelength. The pump light generates extra hole-electrons in TiO_2 which lowers the set voltage compared to dark. Thus, the process avoids undesired current overshoots. The device set at lower voltages in the presence of visible light. With a change in intensity, the set voltage changes.

Following are the future scope for the presented work:

- Investigation for the new plasmonic material can be done to reduce metallic losses. A highly doped semiconductor can be a possible choice as a plasmon source instead of metal.
- The dielectric material can be replaced with a material having high dielectric permittivity for optical phase and intensity modulation.
- Optical extinction is controlled by metal atom diffusion. The metal atom diffusion can be improved by using a top electrode with low electronegative material and with low ionization energy. The higher the metal diffusion the larger will be the optical extinction ratio. But this will reduce the endurance of the device.
- A semipermeable material as a capping layer can be used to control the metal atom diffusion.
- Instead of area distributed conduction bridge formation, the device can be fabricated with a single location-based conduction bridge formation.
- The application can further be found in ultra-fast photodetection using resistive switching.

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