An Analytical Approach for Designing Ultra Low Power (ULP) Subthreshold Logic Blocks with Germanium Junctionless Transistors

MS (Research) Thesis

By

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DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

June 2021

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A THESIS

Submitted in fulfillment of the
requirements for the award of the degree
of
Master of Science (Research)

by
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DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY INDORE

June 2021

INDIAN INSTITUTE OF TECHNOLOGY INDORE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **An Analytical Approach for Designing Ultra Low Power (ULP) Subthreshold Logic Blocks with Germanium Junctionless Transistors** in the partial fulfillment of the requirements for the award of the degree of **MASTER OF SCIENCE (RESEARCH)** and submitted in the **DEPARTMENT OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from July 2019 to June 2021 under the supervision of Dr. Abhinav Kranti, Professor, Discipline of Electrical Engineering, Indian Institute of Technology Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Pshrivas 08/06/2021

Signature of the student with date
(PRADEEP KUMAR SHRIVAS)

This is to certify that the above statement made by the candidate is correct to the best of my/~~our~~ knowledge.

08/06/2021

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ACKNOWLEDGEMENT

I would like to express my sincere gratitude to my M.S. thesis supervisor, Prof. Abhinav Kranti, for providing me an opportunity to join his research group at IIT Indore. I am extremely grateful for his support, guidance, motivation, encouragement, and feedback towards my MS (Research) work. His continuous support and effort have made me achieve the research goals in this thesis.

I sincerely thank my PSPC members, Dr. Vipul Singh, and Dr. Bhupesh Kumar Lad, for their insightful remarks and valuable suggestions on the M.S. work from different aspects. I warmly acknowledge IIT Indore for providing me the necessary infrastructure and research facilities. I am thankful to all the faculty members of the Department of Electrical Engineering for their kind support during my MS (Research) work. I would also like to thank all the staff members of IIT Indore for their generous help concerning academics and accommodations.

I would like to express my sincere gratitude to IIT Indore and the Ministry of Education, Government of India, for providing the fellowship during the M.S. program. I also acknowledge the support of TCAD tools enabled by externally funded project (CRG/2019/002937) by Department of Science and Technology, Government of India.

I am deeply grateful to my colleagues, especially Sandeep, Nivedita, Bhuvaneshwari, and Manish for their kind support and motivation during my research work. I would also like to extend my gratitude towards other colleagues Saurabh, Shruti, and Somesh for their kind co-operation and healthy working environment in the research lab.

I would like to express my earnest thanks to my friend Shubham for motivating me to pursue post-graduate program at IIT Indore. A special thanks to all my M.S. friends at IIT Indore who are like family to me. I cannot forget to thank my other friends Snehitha, Hitesh, Shubham, Ajay, Vishal, Anchit, Harsh, Wayam, Mayuri, Shemon, Apurve, and Sumit for their friendship and motivation during the research work.

I would like to express my deepest gratitude to my parents: my father, Mr. Dinesh Kumar Shrivas, and my mother, Mrs. Sudha Shrivas, for their wholehearted love, encouragement, and support during the M.S. work. I am also heartily grateful to my cousins Ayush, Bindu, and Mansi for their affection and support during my research work.

Finally, I want to express my heartiest gratefulness to Almighty God, who gave me life, faith, and capability for this crucial period of my life.

Pradeep Kumar Shrivas

Dedicated to my parents

Abstract

AN ANALYTICAL APPROACH FOR DESIGNING ULTRA LOW POWER (ULP) SUBTHRESHOLD LOGIC BLOCKS WITH GERMANIUM JUNCTIONLESS TRANSISTORS

For the past few decades, the semiconductor industry has focused on emerging transistor architectures to meet the projections of Moore's law. As a result, much interest has been directed towards transistors with simpler fabrication process and reduced Short Channel Effects (SCEs). The semiconductor industry has continuously evolved in technological advancement and fabrication of Integrated Circuits (ICs) for High Performance (HP), Low Power (LP) and Ultra Low Power (ULP) logic applications. A miniaturized transistor with ideal subthreshold swing (S_{Swing}) and a small extent of Drain Induced Barrier Lowering (DIBL) is prudent for ULP devices. However, due to the downscaling of gate length (L_g), SCEs can be observed in the characteristics of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). SCEs result in a decrease in threshold voltage (V_{th}) with decreasing L_g, higher drain induced barrier lowering, as well as deterioration in S_{Swing}.

A practical method adopted to reduce SCEs and to improve electrostatic controllability of gate over the channel region is by employing more number of gates in a transistor. Multi-gate junctionless (JL) transistors can be potential alternatives to conventional MOSFET for downscaling owing to the absence of traditional *pn* junctions, eased fabrication steps and thermal budgets, good control over the channel by multiple gates and improved immunity towards SCEs. Literature has shown the prospects of heavily doped (10^{19} cm^{-3}) JL MOSFET over conventional MOSFET for LP logic devices as compared to HP logic device applications. A reasonably doped JL MOSFET (10^{18} cm^{-3} to 5×10^{18} cm^{-3}) can additionally enhance LP transistor performance, decrease sensitivity and ease gate workfunction requirement. The use of wider underlap regions is also critical for LP devices.

For a conventional JL MOSFETs, due to the same dopant type (ideally higher doping) across the semiconductor film, the elongation of depletion regions outside the channel region can occur in the off-state. Consequently, the effective channel length (L_{eff}) becomes longer than L_g. An elongated L_{eff} in the subthreshold operating region can reduce

SCEs in these transistors and has the possibilities for LP devices while allowing miniaturization. This outstanding feature is present in predominantly all JL architectures. The thesis imparts exhaustive and purposeful approach to evaluate as well as alleviate SCEs in Germanium (Ge) Double Gate (DG) JL architectures (Ge DG JL with G-S/D underlap), by comprehensively focusing on effective gate length in the subthreshold region of operation which is important for ultra low power (ULP) applications. An emerging technology option should be able to support device for HP, LP and ULP applications. While Ge exhibiting higher mobility and can support HP and LP technologies catering to above threshold operation, the choice of ULP applications with Ge devices has been a bottleneck due to enhanced degree of SCEs in Ge based devices. This thesis also point towards important design parameters that can be utilized for better short channel immunity, and hence, improved architecture for Ge based DG JL transistor can find application in ULP subthreshold logic.

The presented multi-region semi-analytical model can reasonably capture electrostatic channel potential at wider gate-underlap length and has shown good agreement with simulated data. A simplified analytical solution for subthreshold drain current can be utilized to evaluate threshold voltage, subthreshold swing and SCEs related parameters. The developed model results have shown acceptable agreement with simulation for predicting SCEs for varying underlap length, gate workfunction, channel doping, gate length and drain biases for Ge DG JL MOSFET. The results obtained from TCAD simulation and developed model suggest that channel doping together with underlap region decide the short channel performance of Ge DG JL transistor.

An ULP CMOS inverter is implemented using Ge JL *n*MOS and *p*MOS DG devices. Universal gates, NAND and NOR, are also implemented in order to show the applicability of the developed approach for building subthreshold logic blocks. The sensitivity of subthreshold CMOS inverter is evaluated in terms of logic threshold (V_{LT}), gain (A_V), nominal high output voltage (V_H) and nominal low output voltage (V_L) which depends on the subthreshold swing of the devices. A variation in device parameters, Ge film thickness (T_{Ge}), L_g and GeON thickness (T_{GeON}) affects V_L, V_H, V_{LT} and A_V more than other parameters considered in the analysis. An in-depth analysis focusing on Ge DG JL transistors for subthreshold logic has been presented in this thesis.

LIST OF PUBLICATIONS

A. Peer-reviewed Journals:

1. **Pradeep Shrivas**, Nivedita Jaiswal, Sandeep Semwal and Abhinav Kranti, "Ultra-Low Power Subthreshold Logic with Germanium Junctionless Transistors", **Semiconductor Science and Technology,** 2021, Accepted (Journal impact factor: 2.361).

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NOMENCLATURE

S_{Swing}	*Subthreshold swing degradation*	*mV/dec*
dV_{th}	*Voltage roll-off*	*V*
L_g	*Gate length*	*nm*
T_{Semi}	*Semiconductor film thickness*	*nm*
T_{BOX}	*Buried oxide thickness*	*nm*
I_{on}	*On-current*	*mA*
I_{off}	*Off-current*	*nA*
I_{on}/I_{off}	*On-current to off-current ratio*	*Unitless*
C_{gg}	*Gate capacitance per unit area*	F/cm^2
V_{th}	*Threshold voltage*	*V*
V_{fb}	*Flatband voltage*	*V*
T_{OX}	*Gate oxide thickness*	*nm*
T_{Ge}	*Germanium film thickness*	*nm*
I_{ds}	*Drain to source current*	*µA*
V_{ds}	*Drain to source voltage*	*V*
V_{gs}	*Gate to source voltage*	*V*
V_H	*Nominal high output voltage*	*V*
V_L	*Nominal low output voltage*	*V*
V_{LT}	*Logic threshold voltage*	*V*
A_V	*Gain*	*V*
V_{DD}	*Supply voltage*	*V*
ΔS	*Change in subthreshold swing*	*mV/dec*
V_{ds1}	*Low drain bias*	*V*
V_{ds2}	*High drain bias*	*V*
$L_{g,S}$	*Short channel gate length*	*nm*
$L_{g,L}$	*Long channel gate length*	*nm*
S_S	*Subthreshold swing for short channel device*	*mV/dec*
S_L	*Subthreshold swing for long channel device*	*mV/dec*
S_1	*Subthreshold swing for low drain bias case*	*mV/dec*

S_2	*Subthreshold swing for high drain bias case*	*mV/dec*
$V_{th,S}$	*Threshold voltage for short channel device*	*V*
$V_{th,L}$	*Threshold voltage for long channel device*	*V*
V_{th1}	*Threshold voltage for low drain bias case*	*V*
V_{th2}	*Threshold voltage for high drain bias case*	*V*
L_{eff}	*Effective channel length*	*nm*
L_{und}	*Underlap length*	*nm*
N_{ch}	*Channel doping of Ge film*	cm^{-3}
n_e	*Electron concentration*	cm^{-3}
T_{GeON}	*Germanium oxynitride thickness*	*nm*
L_1	*Depletion width towards the source*	*nm*
L_2	*Depletion width towards the drain*	*nm*
φ_I	*Potential distribution in region-I*	*V*
$n_{i,Ge}$	*Intrinsic carrier concentration in Ge*	cm^{-3}
k	*Boltzmann's constant*	*J/K*
q	*Electronic charge*	*C*
$\varphi_{f,I}(x)$	*Electron quasi-Fermi potential*	*V*
T	*Temperature*	*K*
$\varphi_{bi,ch}$	*Channel built-in voltage*	*V*
ε_{Ge}	*Permittivity of Germanium*	*F/cm*
ε_{GeON}	*Permittivity of Germanium oxynitride*	*F/cm*
L_D	*Extrinsic Debye length*	*nm*
A_I, B_I	*Constant coefficients*	-
φ_{II}	*Potential distribution in region-II*	*V*
ϑ_S	*Potential distribution at* $x = -L_1$	*V*
ξ_S	*Electric field at* $x = -L_1$	*V/cm*
φ_{III}	*Potential distribution in region-III*	*V*
a_1, a_2, a_3	*Constant coefficients*	-
φ_S	*Surface potential*	*V*
λ_N	*Natural length*	*nm*

ζ	*Intermediate parameter*	-
A_{III}, B_{III}	*Constant coefficients*	-
φ_{IV}	*Potential distribution in region-IV*	*V*
ϑ_D	*Potential distribution at* $x = L_g + L_2$	*V*
ξ_D	*Electric field at* $x = L_g + L_2$	*V/cm*
φ_V	*Potential distribution in region-V*	*V*
A_V, B_V	*Coefficients*	*V*
N_{sd}	*Heavily doped* (n^{++}) *region*	cm^{-3}
W_g	*Device width*	μm
$\mu_{n,Ge}$	*Low field electron mobility of Ge*	$cm^2/V\text{-}s$
φ_c	*Centre channel potential*	*V*
Φ_f	*Workfunction*	*eV*
ΔV_{th}	*Threshold voltage shift*	*V*
x	*Distance along the channel*	*nm*
V_{IN}	*Input voltage of CMOS Inverter*	*V*
V_O	*output voltage of CMOS Inverter*	*V*
$V_{th,n}$	*Threshold voltage for nMOS*	*V*
$V_{th,p}$	*Threshold voltage for pMOS*	*V*
V_{Swing}	*Full output swing*	*V*
I_O	*Technology-dependent parameter*	*nA*
α	*Technology-dependent parameter*	*Unitless*
V_{th0}	*Threshold voltage at very low* V_{ds}	*V*
β	*Technology-dependent parameter*	*Unitless*
Φ_{fn}	*Gate workfunction for nMOS*	*eV*
Φ_{fp}	*Gate workfunction for pMOS*	*eV*
$V_{DD,IRDS}$	*Supply voltage for each technology node*	*V*
V_{IN1}	*Input 1 for NAND and NOR gates*	*V*
V_{IN2}	*Input 2 for N ND and NOR gates*	*V*

ACRONYMS

MOSFETs	*Metal Oxide Semiconductor Field-Effect Transistors*
FET	*Field-Effect Transistor*
MOS	*Metal Oxide Semiconductor*
SCEs	*Short Channel Effects*
DIBL	*Drain Induced Barrier Lowering*
CMOS	*Complementary MOS*
SOI	*Silicon-on-Insulator*
SiO_2	*Silicon dioxide*
BOX	*Buried Oxide*
RDFs	*Random Dopant Fluctuations*
n	*Donor type*
p	*Acceptor type*
n^+	*Heavily doped donor type*
p^+	*Heavily doped acceptor type*
FBEs	*Floating Body Effects*
PD	*Partially Depleted*
FD	*Fully Depleted*
PDSOI	*Partially Depleted Silicon-on-Insulator*
FDSOI	*Fully Depleted Silicon-on-Insulator*
n^{++}	*Heavily doped with n-types*
p^-	*Moderate doped with p-type*
UTB	*Ultra-Thin Body*
UTBB	*Ultra-Thin and BOX*
GP	*Ground Plane*
DG	*Double Gate*
DELTA	*Fully DEpleted Lean-channel TrAnsistor*
MIGFET	*Multiple Independent Gate FET*
Ω-gate	*Omega-gate*
π-gate	*Pi-gate*

GAA	*Gate-All-Around*
TG	*Triple-Gate*
CPU	*Central Processing Unit*
RDF	*Random Dopant Fluctuation*
RDD	*Random Discrete Dopant*
Si	*Silicon*
Ge	*Germanium*
JL	*Junctionless*
BTBT	*Band-to-Band Tunneling*
IRDS	*International Roadmap for Devices and Systems*
SRAM	*Static Random Access Memory*
1D	*One-Dimensional*
2D	*Two-Dimensional*
S/D	*Source or Drain*
TCAD	*Technology Computer-Aided Design*
VLSI	*Very Large Scale Integration*
Si_3N_4	*Silicon Nitride*
VB	*Valence Band*
CB	*Conduction Band*
$GeCl_4$	*Germanium chloride*
GeO_2	*Germanium dioxide*
GeO	*Germanium monoxide*
GeS_2	*Germanium disulphide*
DC	*Direct Current*
AC	*Alternating Current*
G-S/D	*Gate-Source/Drain*
ULP	*Ultra-Low-Power*
PVT	*Process Voltage Temperature*
LP	*Low Power*
HP	*High Performance*
IGFET	*Insulated Gate Field Effect Transistor*

BSIM	*Berkeley Short-channel IGFET Model*
BSIM-SOI	*BSIM-Silicon-On-Insulator*
BSIM-IMG	*BSIM-Independent Multi-Gate*
BSIM-CMG	*BSIM-Common Multi-Gate*
RTL	*Resistor-Transistor Logic*
DTL	*Diode-Transistor Logic*
TTL	*Transistor- Transistor Logic*
ECL	*Emitter-Coupled Logic*
ICs	*Integrated Circuits*
RC	*Product of Resistance and Capacitance*

Chapter 1

Introduction

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are considered as a backbone of the semiconductor industry. Due to higher computational power and faster processing requirements, a MOSFET needs to be scaled down considerably. In 1965, it was anticipated by Gordon Moore that it would take nearly 18 months for the number of transistors on a chip to double [1], [2]. The semiconductor manufacturing industry has followed this trend successfully for nearly six decades. However, certain device and process limits are now challenging the further miniaturization of conventional (bulk) Metal Oxide Semiconductor (MOS) devices. It is increasingly difficult for bulk MOSFETs to cope with the desired performance indicators due to Short Channel Effects (SCEs) [3]-[5]. The different challenges associated with scaling down the device to the lower technology nodes are current drive, gate controllability, parasitic capacitance, power consumption, reliability, and parameter variation [6]. Poor gate controllability results in SCEs like an increase in Subthreshold Swing (S_{Swing}), Threshold Voltage roll-off (dV_{th}), Drain Induced Barrier Lowering (*DIBL*), and Band-to-Band Tunneling [7], [8], [3]-[5]. The drain current can be increased to boost the device characteristics in short channel devices [9]. Several approaches have been adopted for enhancing effective channel mobility, such as mobility enhancement through strained silicon, using high mobility material like Germanium [10]-[11]. For a device with a thin semiconductor layer and heavily doped substrate, there will be variability and reliability issues at shorter gate lengths [12].

1.1 Evolution of MOSFET Technology

1.1.1 Bulk Technology

The fabrication of more transistors on an integrated chip needs aggressive scaling of device dimensions in deep sub-micrometer regime [13]. Due to this,

further miniaturization of complementary MOS (CMOS) integrated circuits fabricated in bulk silicon technology has reached its physical limits [14]. Also, in a bulk MOSFET, only about 10% of the silicon wafer is used for current conduction. In addition, many unwanted parasitic effects come into play due to the interaction of the channel with the substrate [14]-[16]. These effects are described below:

(1) **The capacitance between source/drain and substrate:** The scaling of the device diminishes the gate control over the channel [14], and therefore, enhances SCEs. To overcome this problem, higher channel doping is employed. However, higher doping further increases the parasitic junction capacitance and adversely affects threshold voltage, mobility, device variability, and transconductance [14].

(2) **Latch-up phenomena**: It originates due to the parasitic *npn* and *pnp* transistors in the diffused regions. The device acts as a thyristor causing an uncontrollable higher current, and hence, damaging the circuit [16].

(3) **Radiation hardening:** The generation of electron and hole pairs from the high-energy particles (alpha particles) results in a higher drain current in channel region of bulk MOSFET [15]. Subsequently, the operation of bulk MOSFET gets seriously affected.

1.1.2 Silicon-on-Insulator (SOI) Technology

In order to address the issues related to parasitic effects in bulk MOSFETs and enable downscaling, Silicon-on-Insulator (SOI) technology [17]-[20] was introduced. This technology involves the isolation of channel region from the substrate through a dielectric (SiO_2). Using SOI technology, monolithic integrated circuits can be built with dielectric isolation that is expected to reduce various parasitic capacitances. Different advantages [3], [4], [14], [21] of SOI technology are listed below:

(1) Dielectric isolation: The isolation between channel and substrate region provides the following benefits over bulk MOSFETs [22]

(a) Higher transconductance

(b) Reduction in parasitic capacitances

(c) Reduced leakage current

(d) Less power consumption

(e) No latch-up

(2) Short channel effects (SCEs): SCEs arise when gate controllability gets hampered by the source/drain electric field. In SOI devices, the depletion width is limited by the Buried Oxide (BOX) [14]. Hence, gate controllability is enhanced in thin-film undoped devices. The electric field lines can also penetrate BOX before affecting the gated region. This reduces gate controllability [14], [23]. This behavior can be suppressed by using ultra-thin BOX, which can terminate the field lines from the source/drain at the substrate.

(3) Random Dopant Fluctuations (RDFs): Undoped/lower body doping reduces variability in the device, and therefore, more immune to RDFs [21].

(4) Reliability: SOI MOSFETs offer excellent immunity towards radiation effects [14], [22]. Therefore, SOI devices are more reliable than bulk devices, even at higher temperatures.

(5) Improved integrity: SOI device structure shows the ability to stack more than a single layer of devices [24], thus expanding the scope of 3D integration.

(6) Circuit design and processing: Fabricating CMOS circuits using SOI technology is much easier than in bulk silicon. There is a notable reduction in fabrication steps due to the absence of wells and inter-device trenches present in bulk technology [24], [3].

(7) Suppressed *pn* junction leakage: In SOI devices, the leakage current is suppressed due to the presence of BOX. Only a small amount of leakage current flows through the junction [25]. This low leakage is important in low stand-by power applications and minimizes the power consumption.

In addition to the advantages mentioned above, SOI is more versatile than bulk. It facilitates additional features in optimizing silicon film thickness, BOX thickness, and substrate bias for enhancing device performance [17]-[20]. SOI

technology has numerous benefits, but the device suffers from interconnection problems and issues related to self-heating [21]. The other concerns for SOI include (i) Floating Body Effects (FBEs), and (ii) series resistance, which can be reduced to an extent using raised source/drain [24] topology or by using a fully depleted device.

1.1.3 Partially and Fully Depleted SOI MOSFETs

MOS device can be operated in either Partially Depleted (PD) or Fully Depleted (FD) regimes depending on the silicon layer thickness [14]

(1) Partially Depleted Silicon-on-Insulator (PDSOI): When the top of the silicon film is depleted without applying any bias, and the bottom portion remains neutral, the structure is known as a partially depleted SOI device (shown in Fig. 1.1(a)).

(2) Fully Depleted Silicon-on-Insulator (FDSOI): When silicon film is thin, then the complete film is depleted of the carriers at zero bias, and the structure is known as fully depleted SOI MOSFET (shown in Fig. 1.1(b)).

Since the bottom of the silicon film is neutral for PDSOI device, it suffers from floating body and kink effect [26], [27]. In PDSOI structures, although the depletion region does not vary with respect to film thickness, but the body potential varies as the number of holes that are accumulated in the body and can affect electrical properties and change the threshold voltage [28]. Additionally, PDSOI structures are more susceptible to the influence from source/drain regions, and thus, second order effects can be more profound [14].

On the other hand, the depletion in FDSOI is independent of the bias condition, and the complete (or total) depletion of semiconductor film takes place. Due to improved gate controllability in the silicon film, higher transconductance can be expected [27]. Therefore, the device is less affected by second order effects. Also, in FDSOI, the subthreshold slope is steeper, and hence, the device can be used for low power applications [25].

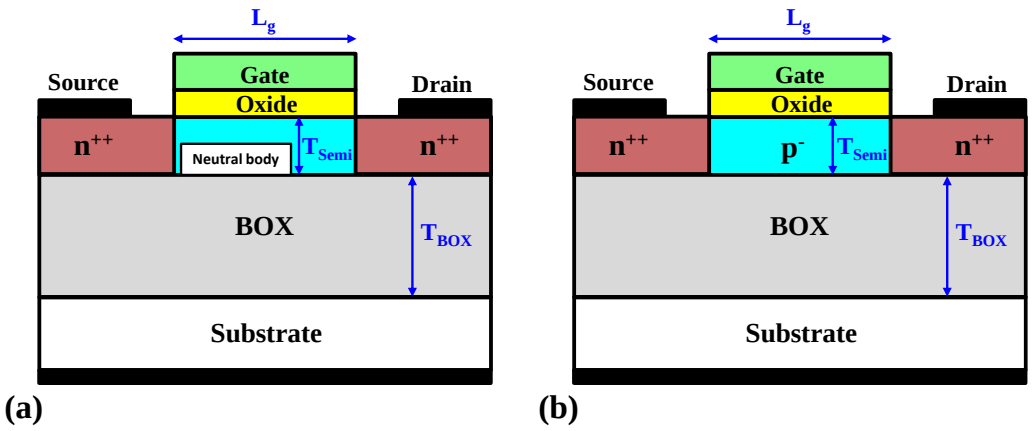

Fig. 1.1: Schematic of an *n*-type **(a)** partially depleted and **(b)** fully depleted Silicon-on-Insulator (SOI) MOSFET with a gate length of L_g, film thickness of T_{Semi}, buried oxide thickness of T_{BOX}. For **(a)** The doping of substrate is neutral and for **(b)** moderate *p*-type (p^-). The source/drain regions are heavily doped with *n*-type impurities (n^{++}).

1.1.4 Ultra-Thin Body (UTB) and Ultra-Thin and BOX (UTBB) MOSFET

As devices are scaled down to nanoscale regime, DIBL poses a big challenge for further improvement of SOI MOSFET. In order to overcome the problem of SCEs faced by sub-50 nm SOI devices, the film thickness can be thinned down to 10 nm or below [29], [30]. These scaled thin film SOI devices are known as ultra-thin body (UTB) SOI MOSFET [30], [14]. In FDSOI structures, the electric field is controlled by the silicon film thickness. Since potential lines are almost flat in UTB devices, the electrostatic integrity of the transistor is improved [14]. Also, SCEs in FDSOI devices can be reduced by using a thin BOX that suppresses the lateral field [31], propagating from source/drain depletion regions through buried oxide, as shown in Fig 1.2(a).

However, with the realization of ultra-thin BOX (shown in Fig 1.2(b)), the horizontal coupling of source and drain through the substrate is enhanced, which requires a heavily doped layer under the BOX referred to as Ground Plane (GP) [14]. The main advantage with GP implementation is that most of the electric

field lines terminate at the ground plane, thus preventing lateral coupling to the substrate. However, body effect and capacitance tend to increase, which degrades the performance of the device [30].

Reducing the BOX thickness attracts other effects [31], such as

(a) Large influence of depletion region formed in the underlying substrate

(b) Increase in parasitic capacitances, and

(c) Increase in gate-to-gate coupling effects [31].

As a result, all the previously mentioned advantages of SOI structures in terms of high current drive and excellent subthreshold behavior may be reduced. Hence, finding an alternative device that can significantly reduce the SCEs in the nanoscale regime is necessary.

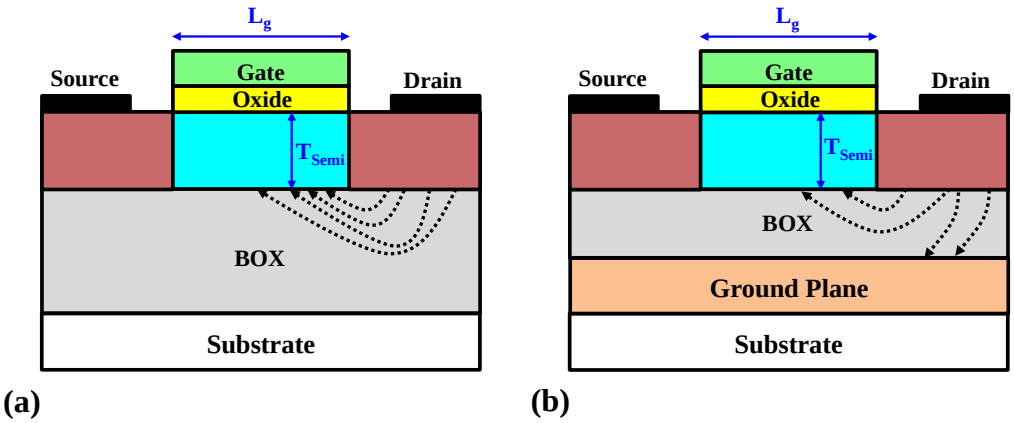

Fig. 1.2: Schematic diagram of **(a)** Ultra Thin Body (UTB) and **(b)** Ultra Thin Body BOX (UTBB) fully depleted (FD) SOI MOSFETs, with a gate length of L_g, and film thickness of T_{Semi}.

1.1.5 Double Gate (DG) MOSFET

Double Gate MOS device acts as a potential alternative to further extend the CMOS technology in nanoscale regime. In this architecture, as the name suggests, two gates control the channel potential. In 1984, Sekigawa and Hayashi first proposed the device structure, and the same was shown to minimize threshold voltage roll-off at shorter channel lengths [32]. In DG operation, both gates (front and back) can be coupled electrically to each other (symmetric MOS) or can be

decoupled with independent bias operation (asymmetric MOS). The main advantages [33]-[36] of this device are as follows:

(a) Excellent immunity towards SCEs

(b) High transconductance

(c) Ideal subthreshold swing

(d) Better on-current (I_{on}) to off-current (I_{off}) ratio (I_{on}/I_{off})

The electrostatic integrity is enhanced due to the dual gate control over the channel. The gate capacitance (C_{gg}) is expected to double due to DG architecture [36]. DG devices are electrostatically more robust than single gate UTB and UTBB devices, as channel is controlled by two gates from both front and back which allow additional gate scalability by a factor of two [37]. The electric field from source/drain in DG SOI transistor can propagate through the semiconductor film and may influence the gated region. However, the electric field lines from the source/drain regions through the back oxide are suppressed, and thus, device is more scalable [32]. The relaxed body film thickness is highly desirable from a manufacturing viewpoint as the fabrication of ultra-thin film can pose major technological challenges [38]. The improved scalability of thin-body DG devices makes them viable for nanoscale CMOS technology [39].

1.1.6 Multiple-Gate MOSFET

The need of further scaling down of the MOS transistor has paved the way for an aggressive evolution of the transistor architecture [40]. Thus, multiple-gate transistors have been evolved to reduce SCEs and to improve the device performance. FinFET, omega-gate, pi-gate, gate-all-around, and triple-gate SOI devices are few examples of multiple-gate architectures [40].

Initially, DG architecture has been evolved in planar topology i.e. similar to that of FDSOI MOSFET, with an additional gate at the bottom of the silicon film [34]. However, due to the complexity in the fabrication process for perfect positioning of front and back gates [38], a fully DEpleted Lean-channel TrAnsistor (DELTA) was developed [33]. This structure consists of vertically positioned silicon film with gates on both sides of the silicon film, and was named

as DG FinFET [40]. The only difference between DELTA and DG FinFET is that a FinFET contains a hard mask at the front gate which prevents the current conduction at the top corner of the device [33], [40]. In a FinFET, if the two gates are electrically decoupled from each other and are biased independently using two different potentials, then the structure is known as Multiple Independent Gate FET (MIGFET) [41].

The other multiple-gate architectures that have been proposed to achieve higher electrostatic integrity are Omega-gate (Ω-gate) [42], Pi-gate (π-gate) [43], Gate-All-Around (GAA) with circular cross-section [44] and Triple-Gate (TG) with rectangular cross-section [45]. In TG MOSFET, gates at the top and along the two sidewalls control the current conduction [45]. For better channel controllability, π-gate and Ω-gate have been introduced due to an additional electric field that propagates at the bottom of the silicon film in addition to front and side wall gates [42], [43]. The circular and square cross-section nanowires consist of gate that wraps around the silicon film and provides additional gate controllability to the device [44].

In 2011, Intel announced [40] that a 22 nm triple gate MOSFET to be used for the next-generation Central Processing Unit (CPU) platform [40] can save nearly 50% of active power as compared to 32 nm technology. In multiple gate SOI MOSFETs, the total current drive is proportional to the total gate width [46]. Hence, due to their excellent gate controllability, a larger current drive (~20%) per unit area of the wafer can be achieved with less demanding requirements on silicon channel dimensions [46]. As the channel length is reduced to few nanometers, the dopant atoms distribution results in discrete and random nature, which affects I_{on}, I_{off}, V_{th}, and subthreshold slope and can degrade the device's performance [40], [46].

Several works [47], [48] have reported that Random Dopant Fluctuation (RDF) can be reduced significantly in case of multiple-gate transistors as compared to single gate devices. RDF poses problems when devices are miniaturized in nanoscale regime as the overall number of atoms resulting from doping becomes

discrete. For higher channel doping, Random Discrete Dopant (RDD) is the main origin of irregularity in the case of heavily doped devices [49], [50]. However, using Germanium (Ge) as a channel material in such devices, a greater immunity towards variation in threshold voltage as compared to Silicon due to RDD can be observed due to the higher relative permittivity for Germanium compared to Silicon [51]. The effects of RDF are expected to be prominent at higher doping levels of 10^{19} cm^{-3} in heavily doped devices [49].

1.1.7 Junctionless Architecture

Conventional transistors have reached such dimensions where the formation of *pn* junctions with doping concentration gradients changing within a few nanometers is required. The necessity for ultra-sharp *pn* junctions imposes severe limitations on fabrication processes and thermal attributes. In 2009, Colinge *et al.* [52] experimentally demonstrated a new multi-gate nanowire transistor architecture named as Junctionless (JL) transistor (shown in Fig. 1.3). Colinge *et al.* [52] demonstrated full CMOS functionality without radically changing the process technology [52], [53]. JL transistors offer various inherent benefits such as full CMOS functionality, compatibility with current CMOS fabrication processes, lower thermal budget, simple expensive annealing techniques, easy fabrication of devices with shorter channels, less mobility degradation by transverse fields in the on-state, and enhanced immunity towards SCEs [52], [53], [54], [55]. However, conventional JL devices with high doping suffer from several drawbacks too, such as mobility degradation due to impurity scattering [56], [57] and reduced current drive due to increased source/drain series resistance [58], [59] when operated at higher gate overdrive, poor turning off capabilities for thicker semiconductor film or higher doping levels [52], [60], off-state Band-to-Band Tunneling (BTBT) [61], enhanced sensitivity of device characteristics towards temperature [56], and device parameter variations [49], [62], [63].

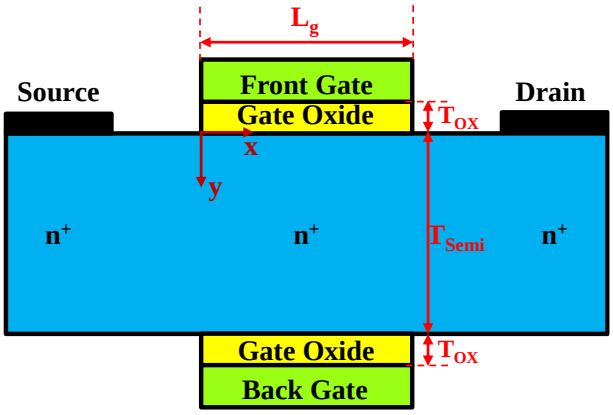

Fig. 1.3: Schematic diagram showing longitudinal cross-sectional view of junctionless (n^+-n^+-n^+) transistors [53], explaining the difference in doping profile across the semiconductor film. L_g represents gate length, T_{OX} is oxide thickness, and T_{Semi} is Germanium Film thickness.

1.2 International Roadmap for Devices and Systems (IRDS)

The IRDS report [64] is created annually by semiconductor professionals, mainly from nations with semiconductor fabrication facilities. The motive behind this group is to set out new major recommendations for academic institutions and industry associations to pursue innovation and engineering for achieving industry targets fulfilling the requirement of downscaling [64].

According to the roadmap, the different challenges faced by present CMOS technology are [64]:

(1) Scaling of ultra-fast, large size, volatile/non-volatile memory technologies in order to substitute Static Random Access Memory (SRAM) and flash memory for relevant implementation

(2) Miniaturization of CMOS

(3) To carry on the practical scaling and optimization of device significantly, the CMOS device needs to be scaled aggressively at lower technology nodes

(4) Platform technology can be developed using scaled CMOS devices which in turn allows newer scaled CMOS technologies to come up with features and functionalities

(5) To traverse the gap between novel architectures and unorthodox devices

To overcome these challenges, some possible solutions [64] that have been suggested are as follows:

(a) Emerging materials for memory

(b) Emerging architectures for future CMOS technology

(c) Emerging materials for novel computing

The IRDS speaks for a planned movement of the technological capacity, requirements and segment of upcoming chances [64]. With the extent of this new outlook, IRDS roadmap constitutes the work in progress which has to be oriented in order to achieve the relevant targets.

1.3 Organization of the Thesis

The thesis presents a detailed approach to model SCEs in symmetric mode Germanium DG JL transistors with underlap length for ultra-low power (ULP) subthreshold logic applications. A Semi-analytical model is developed to efficiently capture the electrostatic potential of the channel in the subthreshold region. The modeling approach involves solutions of 2D Poisson's equations using parabolic potential approximations in the vertical direction [65]-[69]. The one-dimensional channel potential along the lateral direction, governing the subthreshold conduction, is obtained by considering source/drain (S/D) depletion extensions outside the gated portion. Appropriate device-dependent boundary and continuity conditions are used while solving the region-wise Poisson's equations. The subthreshold drain current is then derived from the channel potential at the different gate and drain biases, and V_{th} and S_{Swing} are extracted from I_{ds}-V_{gs} characteristics. The parameters indicating SCEs are estimated and optimal device is proposed. The derived model results are validated with ATLAS Silvaco Technology Computer-Aided Design (TCAD) simulation results [70].

Acknowledging the need for developing relative simple and useful expression for drain current (even for an advanced device) to facilitate circuit design, relevant parameters have been extracted from the developed model and utilized for analyzing a subthreshold inverter.

The extracted parameters for advanced subthreshold devices are then applied to the model developed by Alioto [71], and nominal high output voltage (V_H), nominal low output voltage (V_L), logic threshold voltage (V_{LT}) and Gain (A_V) of Complementary MOS (CMOS) inverter for underlap Ge JL DG transistors has been evaluated. The values of gate length considered in the analysis is taken from IRDS data [64], while the values of the supply voltage ($V_{DD,IRDS}$) for each technology node is reduced by a factor of 2 i.e. $V_{DD} = V_{DD,IRDS}/2$ to ensure subthreshold operation. This approach presents a reasonable assessment of Ge JL CMOS inverter for subthreshold logic applications. Various possible scenarios are also considered to enhance the gain at lower technology nodes.

Chapter 1 describes the basic introduction of MOSFET technology. Starting from the device evolution and technological advancements in the semiconductor industry, this chapter covers the fundamental background regarding the evolution of different architectures, which is important to follow the discussion in the rest of the thesis. The chapter also discusses the IRDS roadmap for the upcoming technological standards and advancements.

Chapter 2 discusses Silicon and Germanium as two possible options for channel material. Further, basic concepts of junctionless transistors such as conduction mechanism and threshold voltage are explained. Short Channel Effects (SCEs) such as *DIBL*, dV_{th}, and degradation in S_{Swing} are also discussed. At last, numerical simulation using ATLAS TCAD has been discussed.

Chapter 3 presents a semi-analytical model for an *n*-channel Germanium DG JL MOSFET under symmetric mode operation to estimate gate-underlap dependent SCEs. The model derived in this chapter primarily predicts the electrostatic channel potential by evaluating the S/D depletion region extensions as functions of underlap length, gate workfunction, channel doping, and gate and drain biases.

A detailed analysis for subthreshold logic applications is carried out to identify the optimal design for Ge JL transistor with suppressed SCEs.

Chapter 4 deals with the application part of the novel device, which is modeled in chapter 3. A CMOS inverter is implemented using Ge DG JL *n*MOS and *p*MOS. Focusing on subthreshold logic with Ge JL MOSFETs for the 3 nm technology node and with a power supply of 0.35 V [64], the performance of NOT, NAND and NOR gates designed with optimized devices have been evaluated to show the applicability of the developed model for digital applications.

Chapter 5 summarizes the conclusions drawn from the research work presented in the thesis. It also mentions the scope for future work

References

[1] Moore G. E., (1965) Cramming more components onto integrated circuits, Electronics, 38, 114-117.

[2] Moore G. E., (1975) Progress in digital integrated electronics, In Proc. IEEE International Electron Devices Meeting 1975, 11-13.

[3] Taur Y., and Ning T. H., (2009) MOSFET devices. In: Fundamentals of modern VLSI devices, 2nd edn., Cambridge University Press, pp. 148-203 (ISBN 978-0-521-83294-6).

[4] Streetman B. G., and Banerjee S. K., (2009) Field-effect transistors. In: Solid State Electronic Devices, 6th edn., PHI Learning Pvt. Ltd., pp. 251-335 (ISBN 978-81-203-3020-7).

[5] Pierret R. F., (2006) Carrier modeling. In: Semiconductor Device Fundamentals, 1st edn., Pearson Education Inc., pp. 691-712 (ISBN 978-81-7758-977-1).

[6] Kim Y.B., (2010) Challenges for nanoscale MOSFETs and emerging nanoelectronics, Transactions on Electrical and Electronic Materials, 11, 93-105.

[7] Colinge J.-P., (2004) Multiple-gate SOI MOSFETs, Solid-State

Electronics, 48, 897-905.

[8] Ferain I., Colinge C. A., and Colinge J.-P., (2011) Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors, Nature, 479, 310-316.

[9] Veeraraghavan S. and Fossum J.G., (1989) Short-channel effects in SOI MOSFETs, IEEE Transactions on Electron Devices, 36, 522-528.

[10] Hoyt J. L., Nayfeh H. M., Eguchi S., Aberg I., Xia G., Drake T., Fitzgerald E. A., and Antoniadis D. A., (2002) Strained silicon MOSFET technology, IEEE Electron Devices Meeting, 23-26.

[11] Welser J., Hoyt J. L., and Gibbons J. F., (1992) NMOS and PMOS transistor fabricated in strained silicon/relaxed silicon-germanium structures, IEEE Electron Devices Meeting, 1000-1002.

[12] Chaudhry A. and Kumar M.J., (2004) Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review, IEEE Transactions on Device and Materials Reliability, 4, 99-109.

[13] Moore G. E., (1965) Cramping more components onto integrated circuits, Electronics, 38.

[14] Colinge J.-P., (1997) Silicon-on-insulator technology: Materials to VLSI, third ed. Springer Science Business Media, New York (ISBN 789-1-4613-4795-8).

[15] Roche P., Autran J.-L., Gasiot G., and Munteanu D., (2013) Technology Downscaling Worsening Radiation Effects in Bulk: SOI to the Rescue, Proc. IEEE Electron Devices Meeting, 766–769.

[16] Ochoa A., and Dawes W., (1979) Latch-up control in CMOS integrated circuits, IEEE Transaction on Nuclear Science, 26, 5065-5068.

[17] Colinge J.-P., (1989) Thin-film SOI technology: the solution to many submicron CMOS problems, IEEE Electron Devices Meeting, pp. 817–820.

[18] Mao B. Y., Sundaresan R., Chen C. E. D., Matloubian M., and Pollack G., (1988) Characteristics of CMOS Devices in oxygen-implanted Silicon-on-Insulator Structures., IEEE Transaction on Electron Devices, 35, 629–633.

[19] Nowak E. D., Ding L., Loh Y. T. and Hu, C., (1994) Speed, power, and yield comparison of thin bonded SOI versus bulk CMOS technologies, IEEE International SOI Conference, pp. 41-42.

[20] Choi J.-Y., and Fossum J. G., (1990) Analysis and control of BJT latch in fully depleted floating-body submicron SOI MOSFETs, IEEE SOS/SOI Technology Conference. Proceedings, pp. 21-22.

[21] Cristoloveanu S., and Lee S., (1995) Electrical characterization of silicon on insulator materials and devices, The Kluwer International Series in Engineering and Computer Science, (ISBN 978-0-7923-9548-5).

[22] Chan M., Yuen S. S., Ma Z., and Hui K. Y., (1994) Comparison of ESD Protection Capability of SOI and BULK CMOS Output Buffers, IEEE International Reliability Physics Symposium, pp. 292–298.

[23] Su L. T., Jacobs J. B., Chung J. E., and Antoniadis D. A., (1994) Deep-Sub micrometer Channel Design in Silicon-on-insulator (SOI) MOSFET‘s, IEEE Electron Device Lett., 15, 183–185.

[24] Kononchuk O., and Nguyen B.-Y., (2014) Silicon-on-Insulator Technology: Manufacture and applications, first ed. Woodhead Publishing, Elsevier, Oxford, (ISBN-978-0-857-09526-8).

[25] Sakurai T., Matsuzawa A., and Douseki T. (2006) Fully depleted SOI CMOS circuits and technology for ultra-low-power applications, Springer, Japan (ISBN 978-0-387-29218-2).

[26] Choi J. Y., and Fossum J. G. (1991) Analysis and control of floating body bipolar effects in fully depleted submicrometer SOI MOSFET’s, IEEE Transaction on Electron Devices, 38, 1384–1391

[27] Kato K., Wada T., and Taniguchi K. (1985) Analysis of kink characteristics in silicon-on-insulator MOSFETs using two-carrier modelling, IEEE Transaction on Electron Devices, 32, 458-462.

[28] Adan A. O., Higashi K., and Fukushima Y. (1999) Analytical threshold voltage model for ultrathin SOI MOSFET’s including short channel and floating-body effects, IEEE Transaction on Electron Devices, 46, 729–737.

[29] Yan R. H., Ourmazd A., and Lee K. F. (1992) Scaling the Si MOSFET: From bulk to SOI to bulk, IEEE Transaction on Electron Devices, 39, 1704–1710.

[30] Beranger C. F., Denorme S., Perreau P., Buj C., Faynot O., Andrieu F., Tosti L., Barnola S., Salvetat T., Garros X., Cassé M., Allain F., Loubet N., Pham-Nguyen L., Deloffre E., Gros-Jean M., Beneyton R., Laviron C., Marin M., Leyris C., Haendler S., Leverd F., Gouraud P., Scheiblin P., Clement L., Pantel R., Deleonibus S., Skotnicki T. (2009) FDSOI devices with thin BOX and ground plane integration for 32 nm node and below, Solid-State Electronics, 53, 730–734.

[31] Yeh P. C., and Fossum J. G. (1995) Physical subthreshold MOSFET modeling applied to viable design of deep submicrometer fully depleted SOI low-voltage CMOS technology, IEEE Transaction on Electron Devices, 42, 1605–1613.

[32] Sekigawa T., and Hayashi Y. (1984) Calculated threshold voltage characteristics of an XMOS transistor having an additional bottom gate, Solid-State Electronics, 27, 827-828.

[33] Hisamoto D., Kaga T., Kawamoto Y., and Takeda E. (1989) A fully depleted lean channel transistor (DELTA)-a novel vertical ultra-thin SOI MOSFET, IEEE Electron Devices Meeting, 833-836.

[34] Balestra F., Cristoloveanu S., Benachir M., Brini J and Elewa T (1987) Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance, IEEE Electron Device Letters, 8, 410-412.

[35] Suzuki K., Tanaka T., Tosaka Y., Horie H., and Arimoto Y. (1993) Scaling theory for double-gate SOI MOSFETs, IEEE Transaction on Electron Devices, 40, 2326-2329.

[36] Fossum J.G., Ge L., and Chiang M-H. (2002) Speed superiority of scaled double-gate CMOS, IEEE Transaction on Electron Devices, 49, 808-811.

[37] Wong H.-S. P., frank D. J., and Solomon P. M. (1998) Device design consideration for double-gate, ground-plane and single-gate ultra-thin SOI

MOSFETs at the 25 nm channel length generation, IEEE Electron Devices Meeting, 407-410.

[38] Wong H.-S. P., Chan K. K., and Taur Y. (1997) Self-aligned (top and bottom) dual-gate MOSFET with a 25 nm thick silicon channel, IEEE Electron Devices Meeting, 427-430.

[39] International Technology Roadmap for Semiconductors, (SIA) http://public.itrs.net, SEMATECH, 2003 edition of ITRS.

[40] Colinge J.-P., (2004) Multiple gate SOI MOSFETs, Solid-State Electronics, 48, 897-905.

[41] Zhang W., Fossum J. G., Mathew L., and Du Y. (2005) Physical insights regarding design and performance of independent-gate FinFETs, IEEE Transaction on Electron Devices, 52, 2198-2206.

[42] Ritzenthaler R., Dupré C., Mescot X., Faynot O., Ernst T., Barbé J.C., Jahan C., Brévard L., Andrieu F., Deleonibus S. and Cristoloveanu S, (2006) Mobility behavior in narrow Ω-gate FET devices, IEEE International SOI Conference, 77-78.

[43] Park J. T., Colinge J. P. and Diaz C. H (2001) Pi-gate SOI MOSFET, IEEE Electron Device Letters, 22, 405-406

[44] Moldovan O., Iniguez B., Jimenez D., and Roig J. (2007) Analytical charge and capacitance models of undoped cylindrical surrounding gate MOSFETs, IEEE Transaction on Electron Devices, 54, 162-165.

[45] Doyle B. S., Datta S., Doczy M., Jin B., Kavalieros J., Linton T., Murthy A., Rios R., Chau R. (2003) High performance fully-depleted tri-gate CMOS transistors, IEEE Electron Device Letters, 24, 263-265.

[46] Shrivastava M., Mehta R., Gupta S., Agrawal N., Baghini M. S., Sharma D. K., Schulz T., Arnim K. V., Molzer W., Gossner H., and Rao V. R. (2011) Toward system on chip (SoC) development using FinFET technology: Challenges, solutions, process co-development & optimization guidelines, IEEE Transaction on Electron Devices, 58, 1597-1607.

[47] Xia L., and Gan X. (2004) Random dopant induced threshold voltage

fluctuations in double gate MOSFETs, International Conference Solid-State and Integrated Circuits and Technol., 138-141.

[48] Lin C.-H., Kambhampati R., Miller R. J., Hook T. B., Bryant A., Haensch W., P. Oldiges, Lauer I., Yamashita T., Basker V., Standaert T., Rim K., Leobandung E., Bu H., and Khare M. (2012) Channel Doping Impact on FinFETs for 22nm and Beyond, Symposium on VLSI Technology, 15-16.

[49] Nawaz S M, Dutta S, Chattopadhyay A and Mallik A (2014) Comparison of random dopant and gate-metal workfunction variability between junctionless and conventional FinFETs, IEEE Electron Device Letters, 35**,** 663-65.

[50] Leung G and Chui C O (2012) Variability impact of random dopant fluctuation on nanoscale junctionless FinFETs, IEEE Electron Device Letters, 33**,** 767-69.

[51] Nawaz S M, Dutta S and Mallik A (2015) A comparison of random discrete dopant induced variability between Ge and Si junctionless p-FinFETs, Appl. Phys. Lett., 107**,** 033506.

[52] Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., and Colinge J.-P., (2009) Junctionless multigate field-effect transistor, Applied Physics Letters, 94, 053511.

[53] Colinge J.-P., Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., Razavi P., O'Neill B., Blake A., White M., Kelleher A.-M., McCarthy B., and Murphy R., (2010) Nanowire transistors without junctions, Nature Nanotechnology, 5, 225-229.

[54] Colinge J.-P., Lee C.-W., Ferain I., Akhavan N. D., Yan R., Razavi P., Yu R., Navarob A. N., and Doria R. T., (2010) Reduced electric field in junctionless transistors, Applied Physics Letters, 96, 073510.

[55] Lee C.-W., Ferain I., Afzalian A., Yan R., Akhavan N. D., Razavi P., and Colinge J.-P., (2010) Performance estimation of junctionless multigate transistors, Solid-State Electronics, 54, 97-103.

[56] Doria R. T., Pavanello M. A., Trevisoli R. D., de Souza M., Lee C.-W., Ferain I., Akhavan N. D., Yan R., Razavi P., Yu R., Kranti A., and

Colinge J.-P., (2011) Junctionless multiple-gate transistors for analog applications, IEEE Transaction on Electron Devices, 58, 2511-2519.

[57] Lee C.-W., Borne A., Ferain I., Afzalian A., Yan R., Akhavan N. D., Razavi P., and Colinge J.-P., (2010) High-temperature performance of silicon junctionless MOSFETs, IEEE Transaction on Electron Devices, 57, 620-625.

[58] Doria R. T., Trevisoli R. D., and Pavanello M. A., (2011) Impact of the series resistance in the I-V characteristics of nMOS junctionless nanowire transistors, ECS Transactions, 39, 231-238.

[59] Jeon D.-Y., Park S. J., Mouis M., Barraud S., Kim G.-T., and Ghibaudo G., (2017) Impact of series resistance on the operation of junctionless transistors, Solid-State Electronics, 129, 103-107.

[60] Barbut L., Jazaeri F., Bouvet D., and Sallese J.-M. (2013) Transient off-current in junctionless FETs, IEEE Transactions on Electron Devices, 60, 2080-2083.

[61] Sahay S., and Kumar M. J., (2016) Insight into lateral band-to-band tunneling nanowire junctionless FETs, IEEE Transaction on Electron Devices, 63, 4138-4142.

[62] Choi S.-J., Moon D.-I., Kim S., Duarte J. P., and Choi Y.-K., (2011) Sensitivity of threshold voltage to nanowire width variation in junctionless transistors, IEEE Electron Device Letters, 32, 125-127.

[63] Parihar M. S., Ghosh D., and Kranti A., (2013) Ultra low power junctionless MOSFETs for subthreshold logic applications, IEEE Transactions on Electron Devices, 60, 1540-1546.

[64] IEEE International Roadmap for Devices and Systems 2020. Available online: https://irds.ieee.org/

[65] Oproglidis T. A., Tsormpatzoglou A., Tassis D. H., Karatsori T. A., Barraud S., Ghibaudo G., and Dimitriadis C. A., (2016) Analytical drain current compact model in the depletion operation region of short-channel triple-gate junctionless transistors, IEEE Transactions on Electron Devices, 64, 66-72.

[66] Shin Y. H., Weon S., Hong D., and Yun I., (2017) Analytical model for junctionless double-gate FET in subthreshold region, IEEE Transactions on Electron Devices, 64, 1433-1440.

[67] Gola D., Singh B., and Tiwari P. K., (2018) Subthreshold modeling of tri-gate junctionless transistors with variable channel edges and substrate bias effects, IEEE Transactions on Electron Devices, 65, 1663-1671.

[68] Shalchian M., Jazaeri F., and Sallese J. M., (2018) Charge-based model for ultrathin junctionless DG FETs, including quantum confinement, IEEE Transactions on Electron Devices, 65, 4009-4014.

[69] Lee C. W., Ferain I., Kranti , Akhavan N. D., Razavi P., Yan R., Yu R., O'Neill B., Blake A., White M., Kelleher A. M., McCarthy B., Gheorghe S., Murphy R., and Colinge J. P., (2010) Short-channel junctionless nanowire transistors, In Proceedings of International Conference of Solid State Devices and Materials (SSDM), Tokyo, Japan, pp. 1044-1045.

[70] Atlas user's manual (2015) TCAD tool, Silvaco Inc., Santa Clara, CA, USA.

[71] Alioto M (2010) Understanding DC behaviour of subthreshold CMOS logic through closed-form analysis, IEEE Trans. Circuits and Systems–I, 57, 1597-1607.

Chapter 2

Semiconducting Materials for Advanced Transistor Architectures

2.1 Silicon

Silicon (Si) is widely used in the semiconductor industry as the substrate material due to its low cost. Also, it forms a good quality of oxide (silicon dioxide (SiO_2)), which is used for gate dielectric [1]. Silicon is the paramount material used in the electronics manufacturing industry, forming about 90% coverage and governing the Very Large Scale Integration (VLSI) industry across the globe [2].

Si mainly has two natural dielectrics, namely silicon nitride (Si_3N_4), and silicon dioxide (SiO_2), which are crucial in device fabrication [3]. In general, SiO_2 forms the underlying foundation for MOSFETs. These devices can be fabricated at high temperatures on top of a silicon wafer. Si is thermally and chemically stable and forms covalent bonds [4]. The interfacial defects in these SiO_2, which are obtained at high temperatures by reaction of silicon wafer with oxygen, are many orders smaller as compared to those of any deposited thin film [3]. Si is non-harmful, relatively cheaper (Si consists approximately 26% of the Earth's covering, which is next to oxygen in case of abundance on the earth) [1]. Si has a band gap of 1.12 eV at room temperature and ~1.21 eV at low temperatures [5]. Also, it has excellent mechanical properties such as thermal conductivity, strength, brittleness, hardness, etc. [5].

However, one of the essential constraints of Si technology is poor performance for optoelectronic applications due to its inability to emit light [6], [7] suitably. This can be due to the fact that a material with an indirect energy band gap sustaining optical transitions is an occasional process at 300 K in Si [5]. For a semiconductor having an indirect energy band gap, the minimum energy level of the conduction band and the maximum energy level of the valence band are

obtained at distinct locations in the *k*-space region, and hence, energy greater than the band gap is needed for transition [8]. Recombination mechanism due to single photon of trivial momentum is not permitted due to the law of conservation of momentum. The involvement of a phonon with the appropriate momentum is essential to assure that momentum is conserved [8], [9]. For a solid material, lattice vibrations occur when phonons are quantized. The optical transition is weak in a phonon aided optical transition for the bulk Si material [7]. This allows other non-radiative processes and a decrease in the light emission efficiency. Therefore, Si bulk is not preferred for optoelectronic device fabrication. Si has a diamond shaped crystal structure in an intrinsic semiconductor. Si has an atomic number of 14, and its atomic mass is 28.08 g mol^{-1} [10]. The compounds formed by Si with other elements are generally tetravalent in nature but bivalent perpetually. Si has a boiling point of 3265^{o}C and a melting point of 1410^{o}C [8]. The structural, electrical, and chemical properties are discussed below.

2.1.1 Structural Properties

The atomic number of Si is 14. The electronic configuration in the ground state is $3s^2\ 3p^2$. There are four valence electrons present, which occupy the 3s and 3p orbitals [8]. Therefore, forming four covalent bonds in the atomic structure can complete its octet and achieve stability. Due to its valency of four, Si generally forms the covalent bonds with other elements. Si has tetrahedral SiY_4 derivatives where the central Si atom shares an electron pair with the four other bonded atoms [10]. Si has the first four ionization energies as 786.3 kJ/mol, 1576.5 kJ/mol, 3228.3 kJ/mol, and 4354.4 kJ/mol, respectively. Also, the single bond covalent radius of Si is 117.6 pm in between the radius of Carbon and Germanium [11], and the ionic radius of the Si is nearly 40 pm [11].

2.1.2 Electrical Properties

Due to the small band gap between Valence Band (VB) and Conduction Band (CB), the resistivity of the Si decreases with an increase in temperature [8]. In intrinsic Si, the Fermi level is located at the midway of the energy gap. Therefore,

undoped Si behaves like an insulator at 300 K. As a result, dopants are added to pure Si to increase its conductivity. The elements from the fifth group can donate one extra electron per dopant atom, forming an *n*-type semiconductor [9]. Similarly, for *p*-type semiconductor, third group elements are used as impurities as they have a vacancy in the atom and can accept one electron for every dopant atom [10]. The simplest possible device using *n*-type and *p*-type semiconductor is a *pn* junction diode [9]. The extent of band bending at zero applied bias is characterized as built-in potential [8].

2.1.3 Chemical Properties and Compounds

Crystalline Si bulk is non-reactive in nature, but can be reactive at very high temperatures [8], [12]. Si forms a gradual and thin layer of silicon dioxide (SiO_2) on the surface of metal which prevents it from oxidation. Generally, Si does not react with the air below 900 °C. The formation of silica dioxide takes place when temperature is kept in between 950 °C and 1160 °C [12]. When temperature is further increased to 1400 °C, Si also reacts with atmospheric nitrogen to form nitrides like SiN and Si_3N_4. At 600 °C, it also reacts with gaseous sulphur. Si also reacts with gaseous phosphorus at 1000 °C [10], [12].

Meanwhile, the formation of oxide cannot prevent reaction with the halogens (fluorine, chlorine, bromine, and iodine). Fluorine reacts with the Si aggressively at 27 °C, chlorine at 300 °C, and bromine and iodine at a temperature of 500 °C [12]. Generally, Si does not react with most liquid acids, but hydrofluoric acid is the exception which tends to get oxidized on reacting with Si [10], [12]. It voluntarily dissolves in heated liquid alkali to form silicates [12]. Also, Si reacts with alkyl halides in presence of copper catalyst to yield organo-silicon chlorides as antecedent to silicone polymers [12]. Si becomes highly reactive on melting, alloying with metals to synthesize silicides [9], [10].

2.2 Germanium

There are many technological requirements that a MOSFET must meet in order to be useful for a future technology node. Although optimistic, the IRDS roadmap [13] is a good indicator of those requirements for the so-called high performance and low power MOSFETs as outlined in chapter 1. The first of the two requirements are that a MOSFET needs to have a certain physical gate-length which means that chosen materials need to be able to be integrated at a tight pitch [8]. The second criterion, the MOSFET must have a certain on-state current (I_{ds} at $V_{ds} = V_{gs} = V_{DD}$, where V_{DD} is the supply voltage) for a given off-state current (**I_{ds}** at $V_{ds} = V_{DD}$ and $V_{gs} = 0$ V) at a given V_{DD}, can be split into several smaller requirements [14]:

a) The channel material should have a high enough carrier velocity or mobility

b) The gate oxide is scalable to achieve good electrostatic integrity and have a low interface trap density

c) The desired threshold voltage can be obtained

d) The MOSFET can meet the off-state current level for low power

Germanium (Ge) has been identified as one of the leading candidates behind Si and a probable channel material for MOSFETs in future nodes because of its ease of integration with Si, and the fact it has one of the highest hole mobility in all semiconductors [15]. For Germanium, the band gap at room temperature is 0.66 eV and at 0 K, it is ~0.74 eV [10]. In general, Ge based transistors show higher degree of SCEs, which occurs due to higher permittivity of Ge as compared to its Si counterpart [16]. The higher permittivity allows the drain bias to penetrate more deeply into the gated region, and hence, decreases the gate controllability over the channel [16]. These devices find application in low power technology if SCEs in Ge based devices can be reduced. The physical and chemical properties of Ge are discussed below.

2.2.1 Physical Properties

The atomic number of Ge is 32 [17]. This material is a hard, lustrous, brittle, and metalloid in the carbon family. Ge is chemically close to its group elements, silicon and tin [17]. Intrinsic germanium is similar in appearance with silicon. Like silicon, germanium naturally reacts and forms complexes with oxygen in nature. Ge also reacts with the oxygen naturally to form the oxides similar to that of Si. The relative permittivity of Germanium material is 16.2. These are high mobility materials which can be used for higher current drives compared to Si material [16]. Some properties of Ge are shown in Table. 2.1.

Properties	**Germanium**
Atomic mass (amu)	72.63
Density (g/cm^3)	5.35
Melting point (K)	947
color	Gray
Oxide type	Refractory dioxide
Oxide density (g/cm^3)	4.7
Oxide activity	Feebly basic
Chloride boiling point(^0C)	86 ($GeCl_4$)
Chloride density (g/cm^3)	1.9

Table 2.1: Basic properties of the Germanium (Ge) material [17].

2.2.2 Chemical Properties

Germanium slowly reacts with oxygen at a temperature of 250 ^oC to form Germanium dioxide (GeO_2) [18]. It is non-soluble in alkalis and dilute acids. It dissolves gradually in the heated concentrated sulphuric and nitric acids [19]. Ge reacts aggressively with melted alkalis to form germinates ($[GeO3]^{2-}$) [18], [19]. Generally, Ge is found in the +4 oxidation state even though several +2 compounds are known to exist [20]. Supplementary oxidation states are occasional as +3 oxidation states occur in Ge_2Cl_6 [19]. Ge has two oxides, namely

Germanium dioxide (GeO_2) and Germanium monoxide (GeO) [18]. GeO_2 can be formed by heating Germanium disulphide (GeS_2), which gives a white powder and is marginally soluble in water but reacts with Alkalis to give germanates [19]. GeO can be formed by reacting GeO_2 and Ge at high temperature [20]. The Ge oxides show an unexpected characteristic of having a high refractive index for light in the visible spectrum, but exhibits transparent nature for infrared light [19], [20].

2.3 Junctionless Transistors

Each proposed transistor design is based on the formation of a junction between the source/drain and channel region. Since 1950, this design is in use for transistor architectures [21]. These junctions are essential as they control the flow of current in the device on applying the bias. Junction formation has always been an integral part of transistor design as it defines the device characteristics. However, due to aggressive scaling, the fabrication of ultra-sharp junction is difficult because of the diffusion process and statistical distribution of doping atoms which results in concentration gradients that are extremely difficult to control [21]. In 2010, a new transistor design was proposed by Colinge *et al.*, [22], which does not consist of any junction, and the same is referred to as Junctionless (JL) transistor (shown in Fig. 2.1). These devices are also known as gated resistors as they have no junctions and very limited doping concentration gradient [23]. Despite the unconventional design, JL devices have shown full CMOS functionality [23], [25]. The important considerations which should be kept in mind while fabricating a JL transistor [23] are as follows:

(i) **Heavy doping:** In order to supply significant drive current in the on-state of the device, the device is preferably heavily doped.

(ii) **Choosing a proper gate-metal workfunction:** JL MOSFET behaves as a normally-on device because of the same doping across the semiconductor film. An *n*-channel (*p*-channel) JL device needs a higher (lower) value of gate

workfunction to turn off the device and to obtain positive (negative) values of the threshold voltage.

(iii) **Narrow and thin semiconductor film:** In order to fully deplete the majority charge carriers from the channel region, a narrow and thin semiconductor film should be used.

JL transistors can offer superior subthreshold characteristics and are excellent candidates for low power logic [22], [23], and analog/RF applications [24], [25]. The application of high permittivity gate dielectric in junctionless devices has shown significant improvement for analog applications at both device and circuit level [22]-[25]. However, conventional JL transistor suffers from several problems like reduced current drive due to increased source/drain series resistance [26], [27] when operated at higher gate overdrive and mobility degradation due to impurity scattering [28],[29], poor turning off capabilities for thicker semiconductor film or higher doping levels [22], [30], off-state Band-to-Band Tunneling (BTBT) [31], and device parameter variations [22], [27] and random dopant fluctuations [32]-[34].

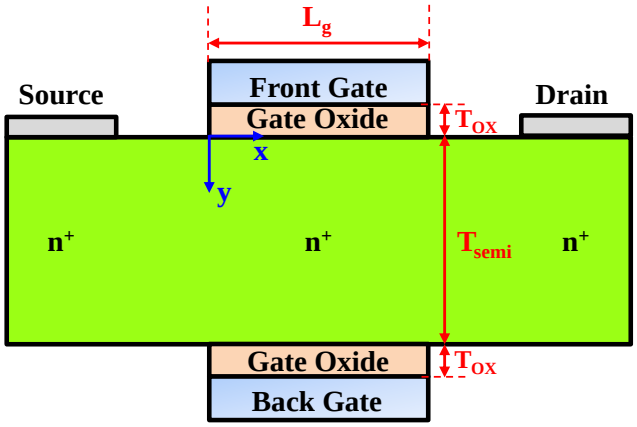

Fig. 2.1: Schematic diagram of double gate junctionless (n^+-n^+-n^+) transistor [27]. L_g represents gate length, T_{OX} is oxide thickness, and T_{Semi} is Film thickness.

A unique feature of the JL transistor is the location of the subthreshold conduction channel. The subthreshold conduction is located in the bulk of the film in JL devices [26]. Therefore, the carriers in JL devices are relatively immune towards surface roughness scattering [28], [29]. Park *et al.,* [35] have demonstrated that JL devices have shown less mobility degradation due to transverse electric fields in comparison with their inversion mode counterparts. As JL devices are designed with heavily doped channel (~10^{19} cm^{-3}), transistor characteristics such as threshold voltage, off-current, and DIBL can vary even for a slight change in device parameters, and this increases the variability in the device [22], [32]-[34].

2.3.1 Conduction mechanism in JL MOSFET

In order to switch on the device, a gate voltage is applied and further increased in order to form a region of majority carriers (channel). Since JL devices are normally on, the difference between the semiconductor workfunction and gate electrode (higher) workfunction shifts the threshold voltage and flatband voltage towards non-negative values [36]. In flatband case, when the device is turned on, the device behaves like a linear resistor [36]. The conduction mechanism in different types of devices (inversion mode, accumulation mode, and junctionless) is elaborated below:

(i) When gate bias is reduced below the threshold voltage, depletion occurs in the device in inversion mode devices. This depletion can be either complete or partial depletion, and flatband voltage is below the threshold level, and the device remains in off state, as shown in Fig. 2.2(a). Similarly, when the gate bias is reduced below the flatband potential, the status of the body is neutral with the overall doping of *p*-type [36]. Now, if gate bias is increased beyond the threshold voltage, an inversion charge layer is formed [36].

(ii) When gate bias is reduced below the threshold voltage, depletion occurs in an accumulation mode transistor (n^+-n-n^+). In this case, the complete depletion of carriers takes place. The threshold condition can be reached by increasing the gate bias in order that the gated portion of the device is not depleted of charge carriers

[36]. If gate bias is increased beyond the threshold voltage, then the flatband potential is achieved [21]. The location of the corresponding flatband voltage is marginally higher than threshold. A further increase in gate bias, allows for accumulation of electrons at the surface as shown in Fig. 2.2(b).

(iii) In the case of heavily doped junctionless MOSFETs, depletion occurs when the gate bias is lower than the threshold voltage. In this case, the complete depletion of carriers takes place, and the device is off [36]. In order to increase the concentration of majority carriers, the voltage at the gate terminal is increased. In this condition, the threshold voltage is attained when the electron carrier concentration in the channel region becomes equal to the channel doping concentration [36]. Now, if gate bias is increased further, the conduction channel spreads out until flatband is reached. The condition for the occurrence of flatband, spreading of channel over the entire film, is shown in Fig. 2.2(c). A significant difference (with reference to accumulation mode devices) is observed between flatband and threshold voltages.

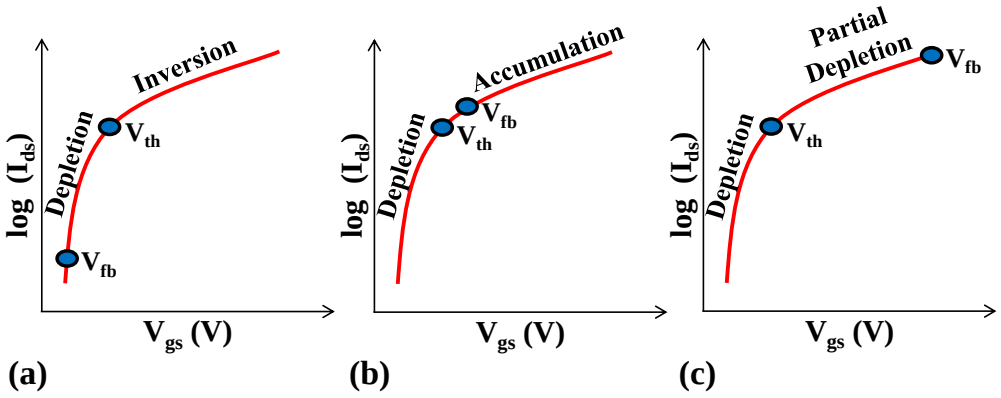

Fig. 2.2: Schematic diagram for showing current conduction mechanisms [36] in (a) inversion-mode (b) accumulation mode, and (c) partial depletion mode in Junctionless MOSFETs.

2.3.2 Threshold Voltage (V_{th})

For a JL device, the threshold voltage relies on the depth (for planar devices) or on the diameter (for nanowire devices) of the thin film, doping of the channel,

gate oxide thickness, and gate workfunction [21]. Appropriate V_{th} can be obtained by varying film thickness and doping. It is essential to estimate the change in Vth with variation in parameters correctly, and hence, V_{th} sensitivity is an essential parameter from the fabrication point of view [36]. The statistical behavior of the dopants dispersed at the S/D regions can result in a change in the implied channel length [36]. These variations are immanent in the fabrication steps, such as ion implantation and diffusion methods. In JL architecture, the formation of a steep concentration gradient does not take place at the source, channel, and drain regions.

2.4 Short Channel Effects (SCEs) in MOSFETs

Short Channel Effects (SCEs) are the unwanted effects seen in the characteristics of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) due to a reduction in the gate length [8]-[10]. For a long channel device, source and drain regions are distant from each other such that their electric fields have negligible effects over the channel potential underneath the gate. The electrostatics is mainly controlled by the gate and is one-dimensional (1D) (i.e. varying mainly along the vertical (*y*-direction) [8]. However, due to the closeness of source and drain depletion regions at shorter gate lengths, their electric fields interfere with the gate electric field, and compete for depletion charge in the channel [37], [38]. The lateral encroachment of source and drain electric fields deteriorates control of the gate over the channel. The potential distribution becomes 2D, rather than 1D, having significant variations in vertical as well as lateral directions [8].

Fig. 2.3(a), (b) compares the off-state (V_{gs} = 0 V) energy barrier seen by the electrons for low (V_{ds} = 50 mV) and high (V_{ds} = 1 V) drain biases for long and short channel cases, respectively. In the long channel case, the channel electrostatics is controlled by the gate field, and therefore, the energy band is flat in most of the channel (Fig. 2.3(a)). Only the near ends of the channel (adjacent to source/drain regions) are influenced by the source and drain electric fields. The energy barrier height remains unchanged even if the drain field

increases with increasing bias (when V_{ds} changes from 50 mV to 1 V). However, for a short channel case (Fig. 2.3(b)), the interference of source and drain electric field against the gate field causes the barrier height to lower than the long channel case. The energy barrier lowering increases when the drain-channel junction is more reverse biased (i.e. V_{ds} rises from 50 mV to 1 V). SCEs can be observed in the device characteristics through a decrease in threshold voltage and degradation in subthreshold swing [8]-[10], [37], [38], as indicated in Fig. 2.3(c), (d). SCEs are outlined below.

a) Reduction in threshold voltage [8]-[10], [37], [38]: Threshold voltage (V_{th}) can be defined as the gate voltage at which a significant amount of drain current flows through the device, and the device is considered to be turned on [9], [10]. In Fig. 2.3(c), (d), V_{th} is usually extracted from I_{ds}-V_{gs} curve of the device using the constant current method [39]. In a long channel device, V_{th} is independent of the gate length. In a short channel device, the lowered energy barrier causes easy injection of charge carriers (electrons in *n*-channel MOSFET) from source to drain [8]-[10]. This reduction in barrier tends to increase the subthreshold current, thereby forcing the transistor to turn-on at a relatively low gate bias, and hence, at reduced threshold voltage. The reduction in V_{th} with decreasing L_g (relative to long channel case) is known as threshold voltage roll-off (dV_{th}) [8], [9], as explained in Fig. 2.3(c). The reduction in V_{th} is enhanced when a high drain bias is applied, and the effect is termed as Drain Induced Barrier Lowering (DIBL) [8]-[10], as shown in Fig. 2.3(d). The short channel threshold voltage is a function of gate length as well as drain bias.

ii) Degradation in the subthreshold swing [8]-[10], [37], [38]: Subthreshold swing, or inverse subthreshold slope or simply subthreshold slope, is defined as the gate voltage required for changing the drain current by a decade, below the threshold [10], [38]. Subthreshold swing is a direct indicator of gate controllability over the channel region. It has a minimum limit of 2.3 times the thermal voltage (~60 mV/dec at room temperature) under perfect gate-channel electrostatic coupling [10], [38]. In a long channel device, the subthreshold drain

current varies exponentially with the gate bias and is independent of drain bias (provided V_{ds} > few times the thermal voltage) [10]. In short channel devices, the gate does not solely control the channel electrostatics, and hence, a degraded subthreshold swing value (> 60 mV/dec) is usually achieved [8], [10]. In short channel MOSFET, subthreshold swing increases with both decreasing gate length and increasing drain bias [10], as shown in Fig. 2.3(c), (d) by ΔS.

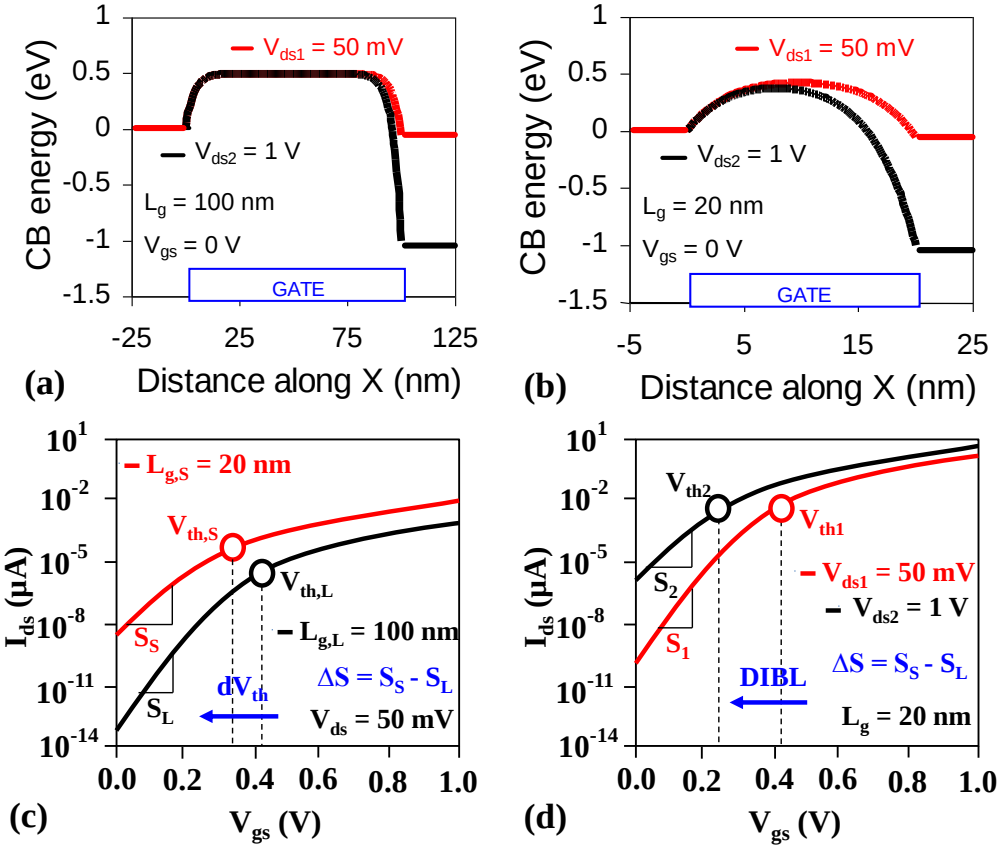

Fig. 2.3: Variation of Conduction Band (CB) energy along the lateral (*x*-direction) with drain bias for **(a)** long channel and **(b)** short channel MOSFETs. Comparison of transfer (I_{ds}-V_{gs}) characteristics: **(c)** long channel versus short channel case and **(d)** low drain bias versus high drain bias cases.

2.5 Numerical Simulation using TCAD Tools

Numerical simulations using Technology Computer-Aided Design (TCAD) tools help to comprehend, develop and optimize semiconductor devices, circuits and processes. These tools also aid in reliable predictions of future generation

devices, new circuit designs, and novel process techniques [40], [41]. All device numerical simulations reported in the thesis have been carried out using Atlas TCAD 2D device simulator by Silvaco [42]. ATLAS provides a detailed understanding of the underlying physical phenomena and mechanisms associated with semiconductor devices or structures. It also facilitates decent predictions of the device's electrical characteristics. Appropriate physical models are incorporated in the simulator to capture the underlying physics of semiconductor devices [42]. ATLAS TCAD allows simulating a device with novel architecture and shows concentration and potential profiles in different regions.

The mixed-mode simulation, another feature of ATLAS simulation tool, is used for transient analysis of NOT, NAND, and NOR gates in chapter 4. It is a circuit simulator that consists of advanced devices and compact circuit models [42]. It incorporates some degree of freedom to simulate comparatively smaller circuits where compact models for single devices are not available or adequately precise. Mixed Mode simulation also enables multi-device simulations. It uses numerical algorithms that are systematic and sturdy for Direct Current (DC), transient, small-signal Alternating Current (AC), and small-signal circuit analysis [42]. Physical modules such as Boltzmann's carrier statistics, concentration, and field-dependent mobility, bandgap narrowing generation/recombination, and models are used in the simulation.

2.6 Conclusion

In this chapter, the properties of Silicon and Germanium have been studied. High mobility materials like Germanium can be utilized in emerging transistor architectures to enhance effective channel mobility. JL transistors, proposed in order to overcome the problems faced due to the formations of sharp *pn* junction at lower gate lengths, can benefit through the use of Ge as channel material. However, Ge based devices show higher SCEs as compared to Si devices due to the higher permittivity of the Ge [16]. Therefore, it is essential to optimize the device parameters for Ge JL transistor in order to reduce SCEs. In the next

chapter, we will discuss the optimization of device parameters in order to alleviate the SCEs in the nanoscale regime.

References

[1] Chen P.H., Peng H.Y., Hsieh C.M., and Chyu M.K. (2001) The characteristic behavior of TMAH water solution for anisotropic etching on both silicon substrate and SiO2 layer, Sensors and Actuators A: Physical, 93, 32-137.

[2] Morris P.R., (1990) A history of the world semiconductor industry, IET, 12

[3] Wilk G.D., Wallace R.M., and Anthony J. (2001) High-κ gate dielectrics: Current status and materials properties considerations, Journal of applied physics, 89, 5243-5275.

[4] Schmidt J., Kerr M. and Cuevas A. (2001) Surface passivation of silicon solar cells using plasma-enhanced chemical-vapour-deposited SiN films and thin thermal SiO2/plasma SiN stacks, Semiconductor science and technology, 16, 164.

[5] Eranna G., (2014) Crystal Growth and Evaluation of Silicon for VLSI and ULSI, CRC Press, pp. 7 (ISBN 978-1-4822-3281-3).

[6] Sung G.Y., Park N.M., Shin J.H., Kim K.H., Kim T.Y., Cho K.S., and Huh C. (2006) Physics and device structures of highly efficient silicon quantum dots based silicon nitride light-emitting diodes IEEE Journal of selected topics in quantum electronics, 12, 1545-1555.

[7] Tsu R., Zhang Q., and Filios A. (1997) Visible electroluminescence in Si/adsorbed gas superlattice, Optoelectronic Integrated Circuits II, 3290, 246-256.

[8] Taur Y., and Ning T. H., (2009) MOSFET devices. In: Fundamentals of modern VLSI devices, 2nd edn., Cambridge University Press, pp. 148-203 (ISBN 978-0-521-83294-6).

[9] Streetman B. G., and Banerjee S. K., (2009) Field-effect transistors. In:

Solid State Electronic Devices, 6th edn., PHI Learning Pvt. Ltd., pp. 251-335 (ISBN 978-81-203-3020-7).

[10] Pierret R. F., (2006) Carrier modeling. In: Semiconductor Device Fundamentals, 1st edn., Pearson Education Inc., pp. 691-712 (ISBN 978-81-7758-977-1).

[11] Kumar D., and Johari M. (2020) Characteristics of silicon crystal, its covalent bonding and their structure, electrical properties and uses, AIP Conference Proceedings, 2220, p. 040037.

[12] Greenwood N.N., and Earnshaw A., (2012), Chemistry of the Elements, 2nd edn., Elsevier (ISBN 978-0-750-63365-9)

[13] IEEE International Roadmap for Devices and Systems 2020. Available online: https://irds.ieee.org/

[14] Qiu Y., Wang R., Huang Q., and Huang R. (2014) A comparative study on the impacts of interface traps on tunneling FET and MOSFET, IEEE Transactions on Electron Devices, 61, 1284-1291.

[15] Sze S. M. (1981) Physics of semiconductor devices, second ed., Wiley-Interscience, New York (ISBN 0-471-05661-8)

[16] Tsormpatzoglou A., Dimitriadis C.A., Clerc R., Rafhay Q., Pananakakis G., and Ghibaudo G. (2007) Semi-analytical modeling of short-channel effects in Si and Ge symmetrical double-gate MOSFETs, IEEE Transactions on Electron devices, 54,1943-1952.

[17] Emsley J., (2012) Nature's Building Block, Oxford University Press, pp. 506-510 (ISBN 978-0-19-850341-5).

[18] Tabet N.A. and Salim M.A. (1998) KRXPS study of the oxidation of Ge (001) surface, Applied surface science, 134, 275-282.

[19] Greenwood N.N., and Earnshaw A., (1997) Chemistry of the Elements, 2nd edn., Butterworth-Heinemann (ISBN 978-0-08-037941-8).

[20] Tabet N.A., Salim M.A., and Al-Oteibi A.L. (1999) XPS study of the growth kinetics of thin films obtained by thermal oxidation of germanium substrates, Journal of electron spectroscopy and related phenomena, 101, 233-238.

[21] Sahay S. and Kumar M.J. (2019) Junctionless field-effect transistors: design, modeling, and simulation, 1st edn., John Wiley & Sons, pp.55-59 (ISBN 978-1-11-952351-2).

[22] Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., and Colinge J.-P., (2009) Junctionless multigate field-effect transistor, Applied Physics Letters, 94, 053511.

[23] Colinge J.-P., Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., Razavi P., O'Neill B., Blake A., White M., Kelleher A.-M., McCarthy B., and Murphy R., (2010) Nanowire transistors without junctions, Nature Nanotechnology, 5, 225-229.

[24] Colinge J.-P., Lee C.-W., Ferain I., Akhavan N. D., Yan R., Razavi P., Yu R., Navarob A. N., and Doria R. T., (2010) Reduced electric field in junctionless transistors, Applied Physics Letters, 96, 073510.

[25] Lee C.-W., Ferain I., Afzalian A., Yan R., Akhavan N. D., Razavi P., and Colinge J.-P., (2010) Performance estimation of junctionless multigate transistors, Solid-State Electronics, 54, 97-103.

[26] Doria R. T., Pavanello M. A., Trevisoli R. D., de Souza M., Lee C.-W., Ferain I., Akhavan N. D., Yan R., Razavi P., Yu R., Kranti A., and Colinge J.-P., (2011) Junctionless multiple-gate transistors for analog applications, IEEE Transaction on Electron Devices, 58, 2511-2519.

[27] Lee C.-W., Borne A., Ferain I., Afzalian A., Yan R., Akhavan N. D., Razavi P., and Colinge J.-P., (2010) High-temperature performance of silicon junctionless MOSFETs, IEEE Transaction on Electron Devices, 57, 620-625.

[28] Doria R. T., Trevisoli R. D., and Pavanello M. A., (2011) Impact of the series resistance in the I-V characteristics of nMOS junctionless nanowire transistors, ECS Transactions, 39, 231-238.

[29] Jeon D.-Y., Park S. J., Mouis M., Barraud S., Kim G.-T., and Ghibaudo G., (2017) Impact of series resistance on the operation of junctionless transistors, Solid-State Electronics, 129, 103-107.

[30] Barbut L., Jazaeri F., Bouvet D., and Sallese J.-M., (2013) Transient off-

current in junctionless FETs, IEEE Transactions on Electron Devices, 60, 2080-2083.

[31] Sahay S., and Kumar M. J., (2016) Insight into lateral band-to-band tunneling nanowire junctionless FETs, IEEE Transaction on Electron Devices, 63, 4138-4142.

[32] Nawaz S M, Dutta S, Chattopadhyay A and Mallik A, (2014) Comparison of random dopant and gate-metal workfunction variability between junctionless and conventional FinFETs, IEEE Electron Device Letters, 35**,** 663-65.

[33] Leung G and Chui C O, (2012) Variability impact of random dopant fluctuation on nanoscale junctionless FinFETs, IEEE Electron Device Letters, 33**,** 767-69.

[34] Nawaz S M, Dutta S and Mallik A, (2015) A comparison of random discrete dopant induced variability between Ge and Si junctionless p-FinFETs, Appl. Phys. Lett., 107**,** 033506.

[35] Park J.-T., and Colinge J.-P., (2002) Multiple-gate SOI MOSFETs: device design guidelines, IEEE Transaction on Electron Devices, 49, 2222-2229.

[36] Colinge J.P., Lee C.W., Akhavan N.D., Yan R., Ferain I., Razavi, P., Kranti A., and Yu R., (2011) Junctionless transistors: physics and properties, In Semiconductor-On-Insulator Materials for Nanoelectronics Applications, Springer, 187-200 (ISBN 978-3-642-15867-4).

[37] Colinge J.-P., (2004) Multiple-gate SOI MOSFETs, Solid-State Electronics, 48, 897-905.

[38] Ferain I., Colinge C. A., and Colinge J.-P., (2011) Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors, Nature, 479, 310-316.

[39] Ortiz-Conde A., Sánchez F. G., Liou J. J., Cerdeira A., Estrada M., and Yue Y., (2002) A review of recent MOSFET threshold voltage extraction methods, Microelectronics reliability, 42, 583-596.

[40] Saha S. K., (2013) Introduction to technology computer aided design. In: Sarkar C. K. Technology computer aided design: simulation for VLSI

MOSFET, CRC Press, pp. 1-44 (ISBN 978-1-4665-1265-8).

[41] Mar J., (1996) The application of TCAD in industry, In Proceedings of 1996 International Conference on Simulation of Semiconductor Processes and Devices, Tokyo, Japan, pp.139-145.

[42] Atlas user's manual (2015) TCAD tool, Silvaco Inc., Santa Clara, CA, USA.

[43] Ning T. H., (2007) A perspective on the theory of MOSFET scaling and its impact, IEEE Solid-State Circuits Society Newsletter, 12, 27-30.

[44] Jeon D.-Y., Park S. J., Mouis M., Berthomé M., Barraud S., Kim G.-T., and Ghibaudo G., (2013) Revisited parameter extraction methodology for electrical characterization of junctionless transistors, Solid-State Electronics, 90, 86-93.

[45] Parihar M. S., and Kranti A., (2014) Revisiting the doping requirement for low power junctionless MOSFETs, Semiconductor Science and Technology, 29, 075006.

[46] Ghosh D., Parihar M. S., Armstrong G. A., and Kranti A., (2012) High-performance junctionless MOSFETs for ultralow-power analog/RF applications, IEEE Electron Device Letters, 33, 1477-1479.

[47] Gupta M., and Kranti A., (2019) Relevance of device cross section to overcome Boltzmann switching limit in 3-D junctionless transistor, IEEE Transactions on Electron Devices, 66, 2704-2709.

[48] Kranti A., Lee C.-W., Ferain I., Yan R., Akhavan N., Razavi P., Yu R., Armstrong G. A., and Colinge J.-P., (2010) Junctionless 6T SRAM cell, IET Electronics Letters, 46, 1491-1493.

[49] Ansari M. H. R., Navlakha N., Lin J.-T., and Kranti A., (2018) Doping dependent assessment of accumulation mode and junctionless FET for IT DRAM, IEEE Transactions on Electron Devices, 65, 1205-1210.

[50] Young K. K., (1989) Short-channel effect in fully depleted SOI MOSFET's, IEEE Transactions on Electron Devices, 36, 399-402

[51] Yan R. H., Ourmazd A., and Lee K. F., (1992) Scaling the Si MOSFET: From bulk to SOI to bulk, IEEE Transactions on Electron Devices, 39,

1704-1710.

[52] Suzuki K., Tanaka T., Tosaka Y., Horie H., and Arimoto Y., (1993) Scaling theory for double-gate SOI MOSFET's, IEEE Transactions on Electron Devices, 40, 2326-2329.

[53] Jaiswal N., and Kranti A., (2018) A model for gate-underlap-dependent short-channel effects in junctionless MOSFET, IEEE Transactions on Electron Devices, 65, 881-887.

[54] Jaiswal N., and Kranti A., (2018) Modeling short-channel effects in asymmetric junctionless MOSFETs with underlap, IEEE Transactions on Electron Devices, 65, 3369–3375

[55] Bhuvaneshwari Y. V., and Kranti A., (2018) Assessment of mobility and its degradation parameters in a shell doped junctionless transistor, Semiconductor Science and Technology, 33, p. 115020.

[56] Matsukawa T., Endo K., Ishikawa Y., Yamauchi H., O'uchi S., Liu Y., Tsukada J., Ishii K., Sakamoto K., Suzuki E., and Masahara M., (2009). Fluctuation analysis of parasitic resistance in FinFETs with scaled fin thickness, IEEE Electron Device Letters, 30, 407-409.

[57] Colinge J.-P., (1997) Introduction. In Silicon-on-insulator technology: Materials to VLSI, 3rd edn., Springer Science Business Media, pp. 1-8 (ISBN 789-1-4613-4795-8).

[58] Doris B., DeSalvo B., Cheng K., Morin P., and Vinet M., (2016) Planar fully-depleted-silicon-on-insulator technologies: toward the 28 nm node and beyond. Solid-State Electronics, 117, 37-59.

[59] Colinge J.-P., (2004) Multiple-gate SOI MOSFETs, Solid-State Electronics, 48, 897-905.

[60] Ferain I., Colinge C. A., and Colinge J.-P., (2011) Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors, Nature, 479, 310-316.

[61] Park J.-T., and Colinge J.-P., (2002) Multiple-gate SOI MOSFETs: device design guidelines, IEEE Transaction on Electron Devices, 49, 2222-2229.

[62] Thompson S. E., and Parthasarathy S., (2006) Moore's law: the future of

Si microelectronics, Materials today, 9, 20-25.

[63] Haensch W., Nowak E. J., Dennard R. H., Solomon P. M., Bryant A., Dokumaci O. H., Kumar A., Wan X., Johnson J. B., and Fischetti M. V., (2006) Silicon CMOS devices beyond scaling, IBM Journal of Research and Development, 50, 339-361.

Chapter 3

Modeling of Short Channel Effects in Germanium Junctionless Transistors

3.1 Device Modeling in Semiconductors

Device modeling mainly focuses on mathematically capturing physical and electrical behavior of the semiconductor devices [1]-[5]. These mathematical models can be widely classified as either compact or physical device models [3], [4] and are as described below.

i) Physical device models [3], [4]: These models enable us to understand the underlying physics involved, obtain the non-measurable quantities, and characterize physical parameters related to devices. These models also define the electrical behavior at the device terminals (e.g., current-voltage characteristics, capacitance-voltage relation, etc.) in all the regions of operations. The model involves defining materials, the geometry of the device, dimensions, region-wise doping distribution, and different carrier transport phenomena. These models provide a comprehensive and precise understanding of the device operation and underlying physics, and therefore, are commonly used in commercial numerical device simulators.

ii) Compact model [3],[4]: These models consist of interconnected electrical elements to reproduce the electrical behavior at the terminals of the semiconductor architecture. Its equivalent physical model represents the circuit element, and the overall model depends on the device characteristics. Due to their compact and fast computational nature, these models are broadly used in circuit simulators.

Even though physical device models are highly accurate, these models are data-wise and computationally intensive and may not be suitable for faster and extensive simulations (devices and circuits).

BSIM (Berkeley Short-channel Insulated Gate (IG) FET Model) [6] refers to the set of transistor compact models for integrated circuit design developed by the University of California, Berkeley. These models are widely used in the semiconductor industry as the standard for compact modeling. The first model of BSIM series was BSIM3 followed by BSIM4, BSIM-Silicon-On-Insulator (BSIM-SOI), BSIM-Independent Multi-Gate (BSIM-IMG), and BSIM-Common Multi-Gate (BSIM-CMG) [7]. These models include physical effects like mobility degradation, SCE, DIBL, etc. [7]. Following approaches are adopted to simplify a purely physical device model [3]-[5] into compact models:

a) Analytical models [3]-[5]: These models are dependent on device physics and popularly utilized in circuit simulators. They consist of closed-form solutions for physical quantities (e.g., charge density, surface potential) that are valid up to a specific operating regime(s) only. Due to complex MOSFET behavior, it may not always be possible to obtain a compact and continuous closed-form analytical model applicable throughout all operating regimes.

b) Empirical models [3]-[5]: These models are based on the idea of curve fitting (e.g., polynomial or an exponential function). There are adjustable parameters, such as coefficients, exponents, etc., that are available to fit the device characteristics and rarely have physical significance. A purely empirical model is generally not preferred for circuit simulators and is often accompanied by analytical models to describe complex physical phenomena.

c) Lookup table models [3]-[5]: These models consist of tables containing values of a physical or electrical quantity (e.g., mobility or drain current) for a large number of combinations of another quantity (e.g., doping or gate bias). These values can be derived from numerical simulations or experimental measurements. The simulator then ‘looks up’ and selects the suitable values from the table in place of calculating them. These models save time but need a massive set of data and interpolation functions between the values to be stored for high precision.

The developed model reported in the later part of this chapter is semi-analytical physical model. Most of the expressions involved in the proposed

model have closed-form solutions, except for some equations that require numerical computation and analysis to determine the values of unknown quantities.

3.2 Model development

Multi-gate JL transistors can possibly provide new paths to extend the miniaturizing limits imposed by conventional MOSFETs. The key features of these transistors include the absence of traditional abrupt *pn* junctions, simple fabrication processes, thermal budget relaxation, efficient gate controllability over the channel due to the presence of multiple gates, and enhanced SCEs immunity [8]-[12]. In JL MOSFETs, due to similar dopant types (preferably high doping) in the source, drain, and gate regions, the extension of depletion regions outside the gated portion also occurs in the subthreshold region [13]. Due to the longer effective channel length (L_{eff}), the gate controllability over the channel region enhances, and hence, SCEs can be reduced significantly. An L_{eff} can be employed to suppress SCEs in JL transistors at lower technology nodes and can be utilized for low-power applications [14], [15].

The optimization of Gate-Source/Drain (G-S/D) underlap regions is favorable for achieving better subthreshold characteristics in conventional (inversion mode) undoped DG MOSFETs [16]-[22]. These G-S/D underlap JL configurations can be more preferable in Ultra-Low-Power (ULP) subthreshold logic implementations where the main concern is to reduce the off-current and static power dissipation [14], [20], [23], [24], [25]-[27]. Since, underlap region offers a high resistance that significantly reduces the on-state current. Therefore, underlap length is more suitable for low power and ultra-low power applications than high-performance application [14].

Different analytical models [29]-[33] have been proposed in the literature for short channel DG JL transistors that have approximated the S/D boundaries to be abrupt. They have ignored the potential drop across the horizontally extended depletion regions outside the gated portion. But, this assumption is valid and works accurately when the S/D depletion width extensions are negligibly small as

compared to the gate length. However, in JL transistors with moderate doping concentration and shorter gate length, the lateral (horizontal) extension of depletion widths contributes significantly to the effective channel length [13], [34], [35]. Therefore, the approximation may no longer be valid and can introduce a certain amount of error in evaluating the channel potential and short channel performance of these devices [13], [34]. Recently, some reported models for DG JL transistors [36], [37] have tried to incorporate these depletion width extensions by utilizing an appropriate device-dependent effective built-in voltage. Moreover, some recent models [13], [38], [39] have considered these S/D depletion widths through dynamic S/D boundaries at the gate edges. However, these reported models are limited to cases when the maximum extent of the depletion region permitted by the device is much less than the source/drain extension lengths.

Most of the modeling approaches for junctionless transistors are restricted to Silicon-based devices [29]-[39]. While the higher mobility of carriers in Ge is definitely advantageous of high-performance logic technology, the higher permittivity of Ge dissuades its use for ULP subthreshold logic applications due to SCEs. As means of exploring the prospects of Ge for subthreshold logic applications, this chapter investigates the operation of Ge JL DG MOSFETs for ULP applications through a physics-based analytical model. Reported approaches for Ge-based inversion mode devices cannot be applied to Ge JL transistors [40]. Further, the developed model should also consider the mobile charge term for threshold voltage evaluation [40]. However, many inversion mode and junctionless devices have considered mobile charge and doping terms for long channel devices, but not for short-channel junctionless device [40]. In principle, Ge film can be divided into three regions i.e. (i) underneath the gate, (ii) source side underlap region, and (iii) drain side underlap region [16], [41]. Since JL devices exhibit a horizontal extension of depletion widths past the channel edge [40], the length of this extended region should be accurately ascertained for ULP design. For a smaller underlap region, the horizontal widening of depletion width will be limited by underlap length (L_{und}). However, if L_{und} is relatively longer, then the horizontal widening of depletion width will be limited by the channel

doping (N_{ch}) of Ge film. To incorporate such cases in our analysis, we have further sub-divided the underlap region into two parts. Consequently, Ge film is divided into five regions along the channel direction, as shown in Fig. 3.1(a). For representative purposes, electron concentration (n_e) and doping, extracted at the centre of the film, is shown in Fig. 3.1(b). Regions I and V are the underlap regions closest to the source/drain, while regions II and IV represent the underlap regions near the gate edges. Region III represents the gated portion of the Ge film.

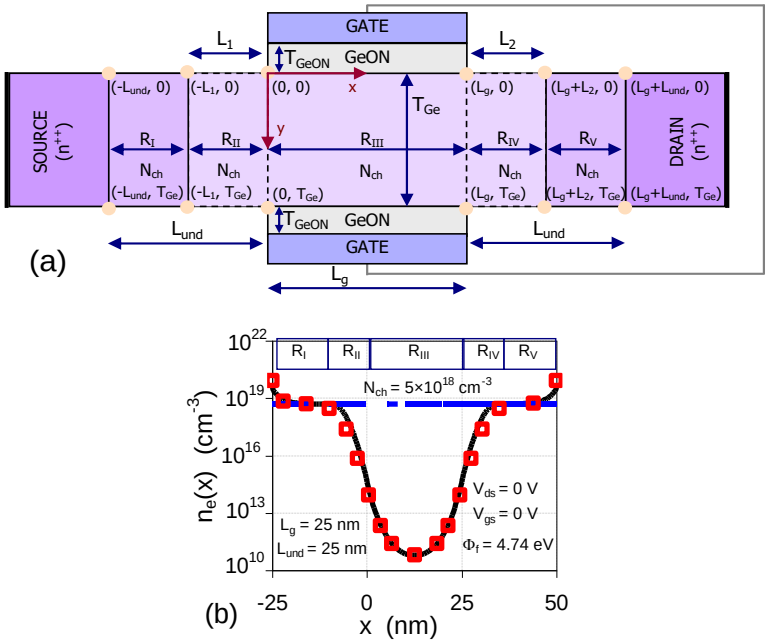

Fig. 3.1: (a) Schematic diagram illustrating Ge based junctionless (JL) MOSFET along with different regions **(b)** Variation of electron concentration (n_e) through the channel direction (x) at the centre of the Ge film ($y = T_{Ge}/2$). Symbols (□) denote simulation results, whereas line (—) indicates the developed model for Ge double gate JL transistor in **(b)**. The channel doping of 5×10^{18} cm^{-3} is represented by a horizontal line in **(b).**

3.2.1 Potential Distribution in Region-I

Region–I, defined by limits $-L_{und} \le x \le -L_1$ (where L_{und} is the underlap length and L_1 is the depletion width towards the source) is closest to the heavily doped

source. At the edge of region–I towards the source i.e. $x = -L_{und}$, a transition in dopant concentration is observed. This transition occurs between the heavily doped (n^{++}) source and the underlap boundary (n^{+}). Since the transition in electrostatic potential is realized over Debye length [42]-[45], the corresponding 1D Poisson's equation controlling the potential distribution in region-I ($\varphi_I(x)$) is given by equation 3.1

$$\frac{\partial^2 \varphi_I(x)}{\partial x^2} = \frac{-q}{\varepsilon_{Ge}}\left(N_{ch} - n_{i,Ge} \exp\left(\frac{q\left(\varphi_I(x) - \varphi_{f,I}(x)\right)}{kT} \right) \right) \tag{3.1}$$

where, $n_{i,Ge}$ is intrinsic carrier concentration in Ge, k is the Boltzmann's constant, q is the electronic charge, N_{ch} represents doping in the semiconductor, $\varphi_{f,I}(x)$ is the electron quasi-Fermi potential, and T is temperature. Accounting for built-in voltage, $\varphi_{bi,ch} = (kT/q)\ln(N_{ch}/n_{i,Ge})$, $n_{i,Ge}$ in equation (3.1) which can be rewritten as

$$\frac{\partial^2 \varphi_I(x)}{\partial x^2} = \frac{-q}{\varepsilon_{Ge}}\left(N_{ch} - N_{ch} \exp\left(\frac{-q\varphi_{bi,ch}}{kT} \right) \exp\left(\frac{q\left(\varphi_I(x) - \varphi_{f,I}(x)\right)}{kT} \right) \right)$$

$$\frac{\partial^2 \varphi_I(x)}{\partial x^2} = \frac{-q\,N_{ch}}{\varepsilon_{Ge}}\left(1 - \exp\left(\frac{q\left(\varphi_I(x) - \varphi_{bi,ch} - \varphi_{f,I}(x)\right)}{kT} \right) \right) \tag{3.2}$$

Since $\varphi_{f,I}(x)$ at the source end will not be a function of position, hence, $\varphi_{f,I}(x)$ is assumed to be Zero. In order to solve differential equation Eq. (3.2) in the closed-form, we are considering only zeroth and first-order terms. This assumption is valid as the region of operation is below threshold and the magnitude of electrostatic potential (in region I) is nearly comparable to the built-in-potential. Hence, the difference between the two terms ($\varphi_I(x)$ and $\varphi_{bi,ch}$) is negligible. This allows for the simplification of the exponential term by using series expansion up to the first order term. Higher order terms do not add any significant contribution, and also impedes the development of a closed form solution, which is not desirable from a compact model point of view. Therefore, equation (3.2) can be simplified as

$$\frac{\partial^2 \varphi_I(x)}{\partial x^2} - \frac{\left(\varphi_I(x) - \varphi_{bi,ch}\right)}{L_D^2} = 0 \tag{3.3}$$

where, $L_D = \sqrt{kT\varepsilon_{Ge}/\left(q^2 N_{ch}\right)}$ is the extrinsic Debye length for N_{ch}-doped Ge layer. The solution of (3.3) can be expressed as

$$\varphi_I(x) = A_I e^{\frac{x+L_{und}}{L_D}} + B_I e^{\frac{-(x+L_{und})}{L_D}} + \varphi_{bi,ch} \tag{3.4}$$

The unknown coefficients, A_I and B_I, can be determined using appropriate boundary conditions.

3.2.2 Potential Distribution in Region-II

Region II represents the depleted portion of source side underlap region. 1D Poisson's equation is solved from $x = -L_1$ (edge of depletion region towards the source) to $x = 0$ (starting of the gate) to ascertain the potential ($\varphi_{II}(x)$) [46], [47]. The corresponding Poisson's equation for the depleted region becomes

$$\frac{\partial^2 \varphi_{II}(x)}{\partial x^2} = \frac{-q}{\varepsilon_{Ge}}\left(N_{ch}\right) \tag{3.5}$$

Integrating equation (3.5) twice results in the following solution

$$\varphi_{II}(x) = \vartheta_S - (x + L_1)\left\{\xi_S + \frac{qN_{ch}}{2\varepsilon_{Ge}}(x + L_1)\right\} \tag{3.6}$$

where, ϑ_S and ξ_S represents the potential distribution and electric field respectively, at $x = -L_1$.

3.2.3 Potential Distribution in Region-III

Region-III is the gated part ($0 \le x \le L_g$, where L_g is gate length) of the Ge film and requires the solution of two-dimensional Poisson's equation. At first, an analysis is conducted with neglecting the mobile carriers as the operation is confined to the subthreshold region. Later, the solution is modified to accommodate the repercussions of mobile charge density within the model. The simplified 2D Poisson's equation (neglecting mobile charge carriers) for region–III is given by equation 3.7

$$\frac{\partial^2 \varphi_{III}(x,y)}{\partial x^2} + \frac{\partial^2 \varphi_{III}(x,y)}{\partial y^2} = \frac{-q}{\varepsilon_{Ge}}\left(N_{ch}\right) \tag{3.7}$$

For subthreshold operation, the suppression of SCEs is of uttermost importance. As the developed model caters to an ULP underlap DG JL MOSFET, the resultant gate length (in subthreshold region) is expected to be greater than the gate length. The structure is itself very complex due to five regions where the continuity of (a) potential and (b) electric field of two adjacent regions has to be maintained at the boundary. Hence, using parabolic potential approach [48] for solving the Poisson's equation is expected to yield results with reasonable accuracy along with a closed form solution. The solution of (3.7) can be derived by solving the parabolic potential approximation [48] given by

$$\varphi_{III}(x,y) = a_1(x) + a_2(x)\,y + a_3(x)\,y^2 \tag{3.8}$$

The boundary conditions required to calculate the coefficients $a_1(x)$, $a_2(x)$ and $a_3(x)$ can be written as

(i) Similar values of surface potential ($\varphi_S(x)$) at front ($y = 0$) and back ($y = T_{Ge}$) interconnections can be obtained due to symmetric mode operation

$$\varphi_{III}(x, y=0) = \varphi_{III}(x, y=T_{Ge}) = \varphi_S(x) \tag{3.9}$$

(ii) Electric fields at front and back interconnections is given by

$$\left.\frac{\partial \varphi_{III}(x,y)}{\partial y}\right|_{y=0} = \frac{\varepsilon_{GeON}}{\varepsilon_{Ge} T_{GeON}}\left(\varphi_S(x) - V_{gfb}\right) \tag{3.10}$$

$$\left.\frac{\partial \varphi_{III}(x,y)}{\partial y}\right|_{y=T_{Ge}} = \frac{\varepsilon_{GeON}}{\varepsilon_{Ge} T_{GeON}}\left(V_{gfb} - \varphi_S(x)\right) \tag{3.11}$$

Where, V_{gs} is the gate bias, $V_{gfb} = V_{gs} - V_{fb}$, ε_{GeON} is the permittivity of Germanium Oxynitride (GeON), T_{GeON} is the thickness of GeON layer, and V_{fb} is the gate flatband voltage with respect to Ge. Using equations (3.9)–(3.11), the coefficients are determined and equation (3.8) can be rewritten as

$$\varphi_{III}(x,y) = \varphi_S(x) + \frac{\varepsilon_{GeON}\left(\varphi_S(x) - V_{gfb}\right)}{\varepsilon_{Ge} T_{GeON}} y - \frac{\varepsilon_{GeON}\left(\varphi_S(x) - V_{gfb}\right)}{\varepsilon_{Ge}\, T_{Ge}\, T_{GeON}} y^2 \tag{3.12}$$

The subthreshold conduction occurs at the centre of the Ge film i.e. $y = T_{Ge}/2$. Therefore, Poisson's equation can be reduced in terms of the centre potential ($\varphi_{C,III}(x)$) shown in equation 3.13

$$\frac{\partial^2 \varphi_{C,III}(x)}{\partial x^2} - \frac{1}{\lambda_N^2}\left(\varphi_{C,III}(x) - \left(V_{gfb} + \left(q\,\lambda_N{}^2 N_{ch} / \varepsilon_{Ge}\right)\right)\right) = 0 \tag{3.13}$$

where, λ_N is the natural length of Ge JL device, and can be written as

$$\lambda_N = \sqrt{((\varepsilon_{Ge} T_{Ge} T_{GeON} / 2\varepsilon_{GeON})(1 + (\varepsilon_{GeON} T_{Ge} / 4\varepsilon_{Ge} T_{GeON}))} \tag{3.14}$$

It should be noted that equation (3.13) has been derived by neglecting mobile charges and considering only the doping dependent term i.e. $-qN_{ch}/\varepsilon_{GeON}$. A closer look at equation (3.13) reveals that the term ($V_{gfb}+qN_{ch}\lambda^2/\varepsilon_{GeON}$) essentially denotes the long channel potential. Although this approach (neglecting mobile charges in subthreshold region) has been adopted by most researchers [29]-39[], the impact of mobile charge [49], [50] in the solution of 1D Poisson's equation and modifying equation (3.13) as

$$\frac{\partial^2 \varphi_{C,III}(x)}{\partial x^2} - \frac{1}{\lambda_N^2}\left(\varphi_{C,III}(x) - \left(V_{gfb} + \frac{qN_{ch}T_{Ge}^2}{8\varepsilon_{Ge}} + \frac{qN_{ch}T_{Ge}T_{GeON}}{2\varepsilon_{Ge}} - \frac{4\zeta kT\varepsilon_{Ge}T_{GeON}\tan(\zeta)}{qT_{Ge}\varepsilon_{GeON}} + \frac{2kT\ln(\cos(\zeta))}{q}\right)\right) = 0 \tag{3.15}$$

where, ζ is an intermediate parameter, which depends on gate bias and device parameters, and can be extracted following the approach of [49], [50]. The general solution for equation (3.15) is represented by

$$\varphi_{C,III}(x) = A_{III}\, e^{x/\lambda_N} + B_{III} e^{-x/\lambda_N} + (\gamma + V_{gfb}) \tag{3.16}$$

where, $\gamma = \frac{qN_{ch}T_{Ge}^2}{8\varepsilon_{Ge}} + \frac{qN_{ch}T_{Ge}T_{GeON}}{2\varepsilon_{Ge}} - \frac{4\zeta kT\varepsilon_{Ge}T_{GeON}\tan(\zeta)}{qT_{Ge}\varepsilon_{GeON}} + \frac{2kT\ln(\cos(\zeta))}{q}$

The unknown coefficients, A_{III} and B_{III}, can be evaluated through appropriate boundary conditions.

3.2.4 Potential Distribution in Region-IV

Region–IV ($L_g \le x \le L_g+L_2$) represents the underlap region (of width L_2) towards the drain side. 1D Poisson's equation represents the electrostatic potential in region–IV i.e. $\varphi_{IV}(x)$ and is given by 3.17

$$\frac{\partial^2 \varphi_{IV}(x)}{\partial x^2} = \frac{-q}{\varepsilon_{Ge}}(N_{ch}) \tag{3.17}$$

Integrating equation (3.17) twice results in the following solution

$$\varphi_{IV}(x) = \vartheta_D - \left(x - \left(L_g + L_2\right)\right)\left\{\xi_D + \frac{q\,N_{ch}}{2\varepsilon_{Ge}}\left(x - \left(L_g + L_2\right)\right)\right\} \tag{3.18}$$

The coefficients ϑ_D and ξ_D describes the potential distribution and electric field, respectively, at $x = L_g + L_2$.

3.2.5 Potential Distribution in Region-V

Similar to the approach followed for the region–I, the 1D Poisson's equation for electrostatic potential ($\varphi_V(x)$) in the region–V ($L_g + L_2 \le x \le L_g + L_{und}$) can be written as

$$\frac{\partial^2 \varphi_V(x)}{\partial x^2} = \frac{-q\,N_{ch}}{\varepsilon_{Ge}}\left(1 - \exp\left(\frac{q\left(\varphi_V(x) - \varphi_{bi,ch} - \varphi_{f,V}(x)\right)}{kT}\right)\right) \tag{3.19}$$

Utilizing the series expansion for the exponential term in equation (3.18) and noting that $\varphi_{f,V}(x)$ is equal to drain bias (V_{ds}) [51] at the drain end, equation (3.19) is simplified as

$$\frac{\partial^2 \varphi_V(x)}{\partial x^2} - \frac{\left(\varphi_V(x) - \varphi_{bi,ch} - V_{ds}\right)}{L_D^2} = 0 \tag{3.20}$$

The solution of equation (3.20) can be expressed as

$$\varphi_V(x) = A_V e^{\frac{x-\left(L_g+L_{und}\right)}{L_D}} + B_V e^{\frac{-\left(x-\left(L_g+L_{und}\right)\right)}{L_D}} + \left(\varphi_{bi,ch} + V_{ds}\right) \tag{3.21}$$

The unknown coefficients, A_V and B_V, can be determined using appropriate boundary conditions. Equations (3.4), (3.6), (3.16), (3.18) and (3.21) represent the potential distribution in the Ge film. In order to determine the unknown coefficients, the following conditions for ensuring the continuity of potential and electric field are utilized.

$$\varphi_I\left(-L_{und}\right) = \varphi_{bi} \tag{3.22a}$$

$$\varphi_I\left(-L_1\right) = \varphi_{II}\left(-L_1\right) \tag{3.22b}$$

$$\left.\frac{\partial \varphi_I(x)}{\partial x}\right|_{x=-L_1} = \left.\frac{\partial \varphi_{II}(x)}{\partial x}\right|_{x=-L_1} \tag{3.22c}$$

$$\varphi_{II}(0)=\varphi_{III}(0) \tag{3.22d}$$

$$\left.\frac{\partial\varphi_{II}(x)}{\partial x}\right|_{x=0}=\left.\frac{\partial\varphi_{III}(x)}{\partial x}\right|_{x=0} \tag{3.22e}$$

$$\varphi_{III}\left(L_g\right)=\varphi_{IV}\left(L_g\right) \tag{3.22f}$$

$$\left.\frac{\partial\varphi_{III}(x)}{\partial x}\right|_{x=L_g}=\left.\frac{\partial\varphi_{IV}(x)}{\partial x}\right|_{x=L_g} \tag{3.22g}$$

$$\varphi_{IV}\left(L_g+L_2\right)=\varphi_{V}\left(L_g+L_2\right) \tag{3.22h}$$

$$\left.\frac{\partial\varphi_{IV}(x)}{\partial x}\right|_{x=L_g+L_2}=\left.\frac{\partial\varphi_{V}(x)}{\partial x}\right|_{x=L_g+L_2} \tag{3.22i}$$

$$\varphi_{V}\left(L_{und}+L_g\right)=\varphi_{bi}+V_{ds} \tag{3.22j}$$

$$\varphi_{I}\left(\infty\right)=\varphi_{bi,ch} \tag{3.22k}$$

$$\varphi_{V}\left(-\infty\right)=\varphi_{bi,ch}+V_{ds} \tag{3.22l}$$

where, $\varphi_{bi}=\frac{kT}{q}\ln\left(\frac{N_{sd}}{n_{i,Ge}}\right)$ with N_{sd} (> N_{ch}) denoting the heavily doped (n^{++}) source/drain regions (10^{20} cm^{-3}). Applying the boundary conditions represented by equations (3.22a) – (3.22l). Using equations (3.4), (3.6), (3.16), (3.18) and (3.21), we obtain

$$A_1=0 \tag{3.23a}$$

$$B_1=\varphi_{bi}-\varphi_{bi,ch} \tag{3.23b}$$

$$\vartheta_S=\varphi_{bi,ch}+\left(\varphi_{bi}-\varphi_{bi,ch}\right)e^{\frac{L_1-L_{und}}{L_D}} \tag{3.23c}$$

$$\xi_S=\frac{\varphi_{bi}-\varphi_{bi,ch}}{L_D}e^{\frac{L_1-L_{und}}{L_D}} \tag{3.23d}$$

$$A_{III}=\frac{\left(\vartheta_D-\frac{qN_{ch}}{\varepsilon_{Ge}}\left(\lambda_N^2+\frac{L_2^2}{2}\right)-V_{gfb}+\xi_D L_2\right)-\left(\vartheta_S-\left(\gamma+\frac{qN_{ch}L_1^2}{2\varepsilon_{Ge}}\right)-V_{gfb}-\xi_S L_1\right)e^{\frac{-L_g}{\lambda_N}}}{2\sinh\left(\frac{L_g}{\lambda_N}\right)} \tag{3.23e}$$

$$B_{III}=\frac{\left(\vartheta_S-\frac{qN_{ch}}{\varepsilon_{Ge}}\left(\lambda_N^2+\frac{L_1^2}{2}\right)-V_{gfb}-\xi_S L_1\right)e^{\frac{L_g}{\lambda_N}}-\left(\vartheta_D-\left(\gamma+\frac{qN_{ch}L_2^2}{2\varepsilon_{Ge}}\right)-V_{gfb}+\xi_D L_2\right)}{2\sinh\left(\frac{L_g}{\lambda_N}\right)} \tag{3.23f}$$

$$\vartheta_D=\varphi_{bi,ch}+V_{ds}+\left(\varphi_{bi}-\varphi_{bi,ch}\right)e^{\frac{L_2-L_{und}}{L_D}} \tag{3.23g}$$

$$\xi_D=\frac{\varphi_{bi,ch}-\varphi_{bi}}{L_D}e^{\frac{L_2-L_{und}}{L_D}} \tag{3.23h}$$

$$A_V=\varphi_{bi}-\varphi_{bi,ch} \tag{3.23i}$$

$$B_V=0 \tag{3.23j}$$

It should be noted that the maximum value of L_1 and L_2 (determined numerically through equations (3.22c) and (3.22i)) is limited to L_{und}.

The drain current (I_{ds}) in the subthreshold region for Ge junctionless transistor can be evaluated as [44]

$$I_{ds}=\left(kT\mu_{n,Ge}n_{i,Ge}\right)\left(\frac{W}{L_T}\right)\left(1-e^{-\frac{qV_{ds}}{kT}}\right) \tag{3.24}$$

where, W represents device-width, $\mu_{\text{n,Ge}}$ is low field electron mobility of Ge and L_{T} can be given as

$$L_T=\int_{-L_1}^{0}\frac{dx}{\int_0^{T_{Ge}}e^{\frac{q\varphi_{II}(x)}{kT}}dy}+\int_0^{L_g}\frac{dx}{\int_0^{T_{Ge}}e^{\frac{q\varphi_{III}(x,y)}{kT}}dy}+\int_{L_g}^{L_g+L_2}\frac{dx}{\int_0^{T_{Ge}}e^{\frac{q\varphi_{IV}(x)}{kT}}dy} \tag{3.25}$$

It is noted that L_{T} is a dimensionless quantity that depends on the potential and lengths of regions II, III, and IV. The value of L_{T} depends on the effective channel length, which results from the lateral extension of depletion width toward source/drain regions. The higher value of L_{T} indicates a higher effective channel length (lower off-current) while a lower L_{T} reflects on shorter effective channel length and higher off-current.

The general expression for electron density (n_{e}(x)) can be expressed as

$$n_e(x) = n_{i,Ge}.\left(\exp\left(\frac{\left(\varphi_C(x)-\varphi_f(x)\right)}{V_T}\right)\right) \tag{3.26}$$

The above expression can be modified to evaluate the electron concentration in various regions as

$$n_{e,j}(x) = n_{i,Ge}.\left(\exp\left(\frac{\left(\varphi_{C,j}(x)-\varphi_{f,j}(x)\right)}{V_T}\right)\right) \tag{3.27}$$

where *j* represents the respective region i.e. R_I to R_V.

3.2.6 Evaluation of Short Channel Effects

As discussed in chapter 2, SCEs can be interpreted mainly from the device transfer characteristics using three parameters: Drain-Induced Barrier Lowering (DIBL), Threshold voltage roll-off *(dV_{th})*, and degradation in the subthreshold swing (S_{Swing}). These parameters can be calculated using the following expressions:

i) DIBL can be defined as the reduction in V_{th} with an increase in drain bias (V_{ds}) [29], [36]

$$DIBL = V_{th}(V_{ds} = 50\ mV) - V_{th}(V_{ds}) \tag{3.28}$$

ii) dV_{th} can be defined as the decrease in V_{th} for a reduction in L_g with respect to long channel V_{th} [29]

$$dV_{th} = V_{th}(Long\ channel) - V_{th}(L_g) \tag{3.29}$$

iii) An increase in subthreshold swing occurs for short channel devices, and can be calculated using following expression [52]

$$S_{swing} = \frac{\partial V_{gs}}{\partial(\log(I_{ds}))} \tag{3.30}$$

3.3 Results and Model Validation

Following device parameters are kept constant for Ge DG JL MOSFET throughout the analysis in this chapter: T_{GeON} = 1.65 nm, T_{Ge} = 9 nm, doping of n^{++} (source/drain) region is 1×10^{20} $cm^{-3,}$ and gate width (W_g) = 1µm. The derived

model is mainly investigated for N_{ch} varying from 10^{18} cm^{-3} to 10^{19} cm^{-3}. The results obtained from the model are validated with the results derived from ATLAS TCAD simulator [53]. In all the subsequent figures of this chapter, solid line represents developed model results, whereas symbols denote TCAD simulation data.

Germanium DG transistors were analyzed with appropriate parameters for Ge as channel material, Germanium oxynitride (GeON) as the native oxide for Ge, and models for concentration-dependent mobility to account for the carrier transport. As the focus of the work is towards subthreshold logic, the analysis was restricted to 0.5 V for V_{gs} and V_{ds}. Fig. 3.1(a) shows the five different regions i.e. R_I to R_V that were considered in the analysis along with coordinates for each region.

Fig. 3.1(b) shows the variation of electron concentration (n_e) along the channel position at zero bias calculated using eq. (3.27). The reasonable agreement between simulation and model data shows the validity of our model for assessing Ge DG JL transistors. The impact of underlap region is clearly visible as the depletion region is extended above the gate edge leading to a greater resultant channel length in the subthreshold region. Since the operation is limited to 0.5 V, the longer effective channel length will not degrade the device performance due to series resistance. Further, Fig. 3.1(b) also shows that it is possible to fully deplete Ge film as very low values of n_e ~10^{11} cm^{-3} are achieved.

Fig. 3.2(a)-(d) shows the change in centre potential (φ_c) across the channel direction (x) as a function of drain bias (Fig. 3.2(a)), gate bias (Fig. 3.2(b)), gate workfunction (Fig. 3.2(c)) and channel doping concentration (Fig. 3.2(d)). The proposed model is able to capture the variation of φ_c over a wide range of parameters and agrees well with the simulation data. In the subthreshold region, the centre potential in region III i.e. underneath the gate will be lower than that in regions II and IV due to a greater degree of depletion by the gate electrode. The centre potential in regions I and V will be higher than that exhibited by regions II and IV because of extension of depletion regions in regions II and IV. An increase

in V_{ds} from 0 to 0.5 V results in a marginal increase (< 10 mV) in the minimum channel potential, thus indicating effective reduction in SCEs. Reducing the gate bias from 0.1 V to -0.1 V translates into an enhanced depletion, which reduces the minimum channel potential, while a reduction in the gate workfunction from 4.74 eV to 4.54 eV at N_{ch} = 5×10^{18} cm^{-3} considerably decreases the extent of depletion in the channel and results in an increase in the minimum channel potential. N_{ch} is critical to the functioning of the device as a higher doping limits depletion, lateral extension of depletion regions and minimum channel potential. Here, L_{und} = 25 nm (maximum possible L_{und}) is considered in order to show its effect in reducing the SCEs.

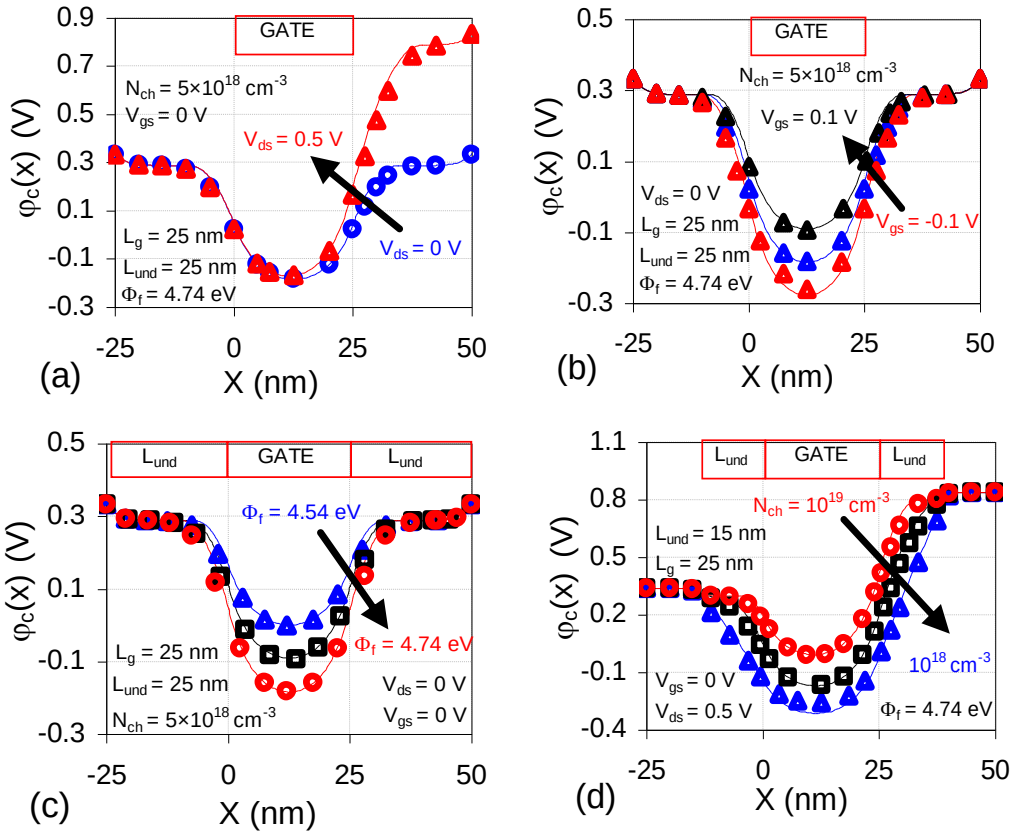

Fig. 3.2: Variation in centre potential (φ_c) across the channel (x) direction for distinct values of **(a)** drain bias (V_{ds}), **(b)** gate bias (V_{gs}), **(c)** gate workfunction (Φ_f), and **(d)** doping (N_{ch}). Symbols (Δ, o, □) denote simulation results whereas lines (—) represent the developed model.

Fig. 3.3(a)-(b) represents the change in channel potential and electron concentration across the vertical direction (y) at the mid-gate position ($x = L_g/2$). A lower value of $\varphi_{III}(L_g/2, y)$ and $n_e(L_g/2, y)$ indicates an enhanced depletion in the subthreshold region. The developed model data is in close agreement with the simulated data. Results also indicate that the choice of channel doping (N_{ch}) is important to limit the off-current (leakage current) for given gate workfunction and film thickness. At higher channel concentration, $N_{ch} = 10^{19}$ cm^{-3} off-current is higher as compared to that achieved with $N_{ch} = 5\times10^{18}$ cm^{-3}.

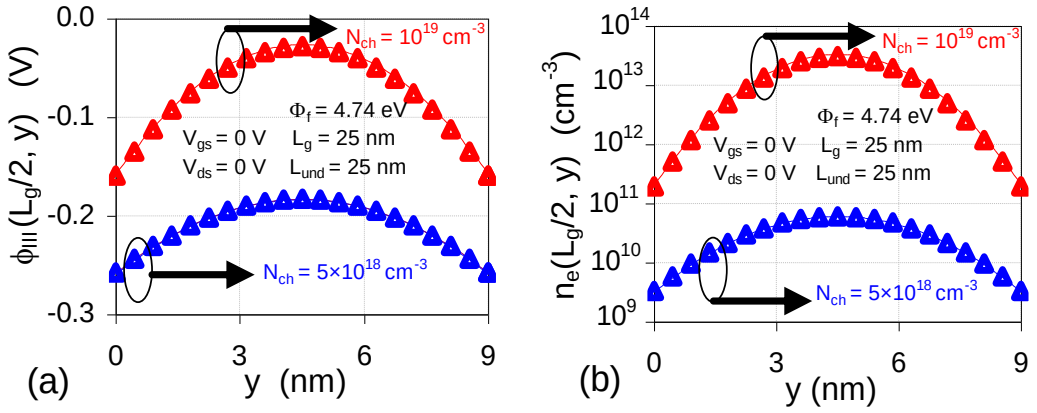

Fig. 3.3: Variation of **(a)** centre potential and **(b)** electron concentration at mid gate position ($x = L_g/2$) along the vertical (y) direction for different values of doping. Lines (—) represent the derived model whereas symbols (Δ) denote simulation results.

Fig. 3.4(a)-(d) shows the effect of channel doping on the performance of DG Germanium JL devices. As shown in Fig. 3.4(a), the subthreshold swing (S_{Swing}) is less than 80 mV/decade even at $N_{ch} = 10^{19}$ cm^{-3} while S_{Swing} is limited to 68 mV/decade at $N_{ch} = 10^{18}$ cm^{-3} for $L_g = 15$ nm. Similarly, the threshold voltage shift (ΔV_{th}) is also minimum at lower N_{ch} as lower doping allows for a greater extension of the depletion width beyond the gate edge, which results in an increase in effective channel length in the subthreshold region of operation (Fig 3.4(b)). The degradation in ΔV_{th} is reflected in the threshold voltage (V_{th}) variation shown with gate length (L_g) in Fig. 3.4(c). The change in V_{th} is least in case of

lower doping concentration due to lower carrier concentration (enhanced depletion) at zero bias. Also, V_{th} at lower N_{ch} values can be appropriately tuned by reducing the gate workfunction. The same trend of enhanced immunity from SCEs can be seen in Drain Induced Barrier Lowering (DIBL) variation shown in Fig. 3.4(d). These graphs clearly indicate the possibility of limited SCEs in DG Ge JL MOSFETs by appropriately selecting device parameters.

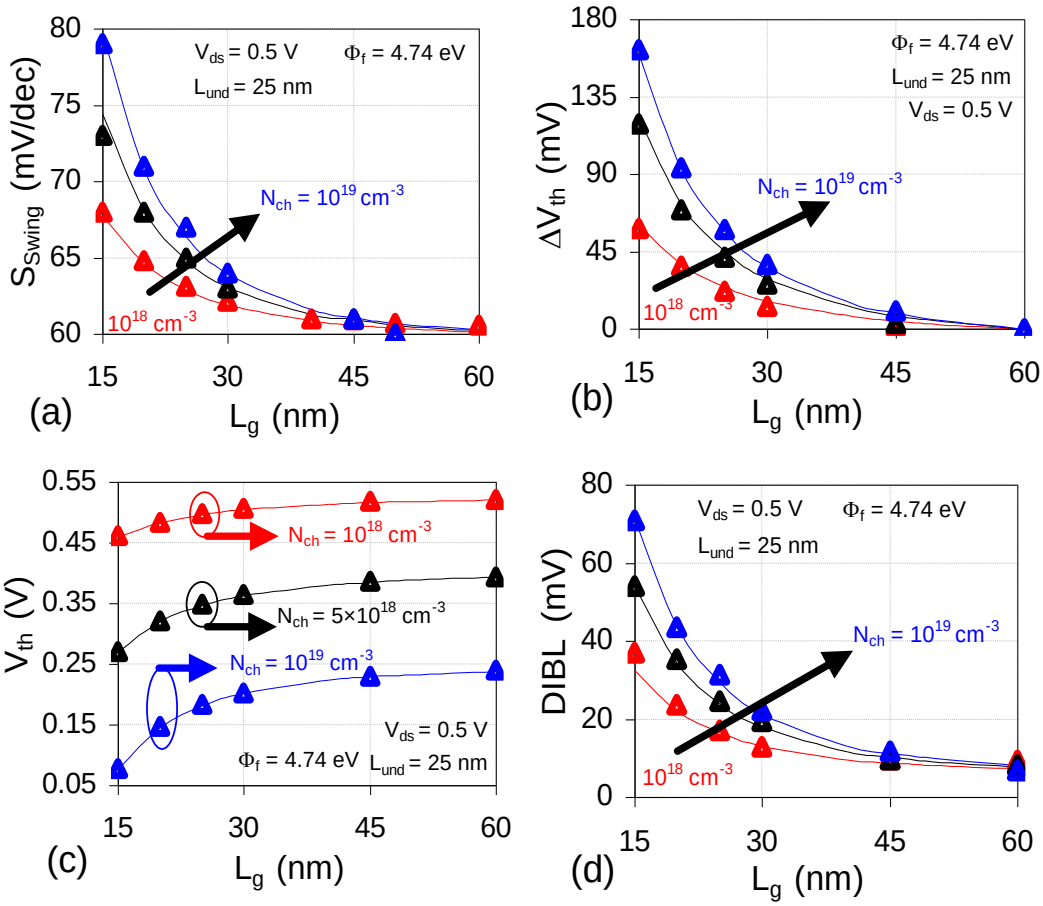

Fig. 3.4: Variation of **(a)** subthreshold swing (S_{Swing}), **(b)** threshold voltage roll-off (ΔV_{th}), **(c)** threshold voltage (V_{th}) and **(d)** DIBL with gate length. Lines (—) represent the derived model whereas symbols (Δ) denote simulation results. The three different values of N_{ch} correspond to 10^{18} cm^{-3}, 5×10^{18} cm^{-3}, and 10^{19} cm^{-3}.

The underlap length (L_{und}) plays a vital role in enhancing short channel immunity at lower gate lengths. As shown in Fig. 3.5(a)-(b), S_{Swing} and DIBL reduce appreciably as L_{und} is increased from 5 nm to 25 nm, with the reduction being more prominent at lower gate lengths (15 nm). The results obtained through analytical modeling agree reasonably well with the simulated data.

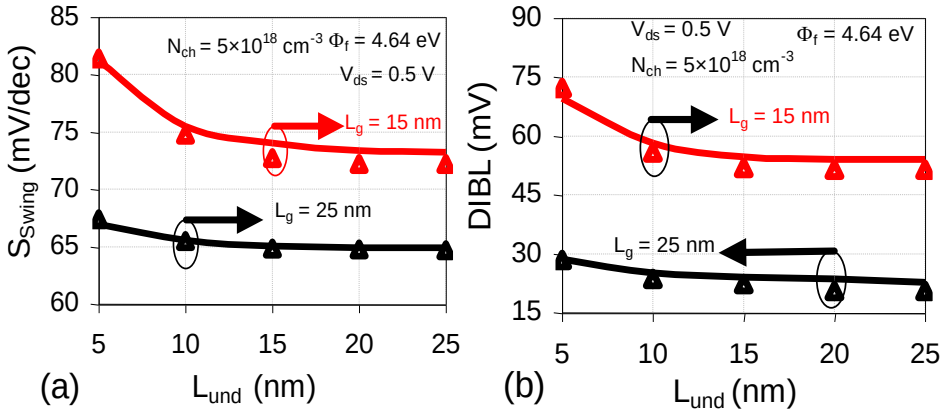

Fig 3.5: Dependence of **(a)** subthreshold swing (S_{Swing}) and **(b)** DIBL on underlap length (L_{und}) for two different gate lengths (25 nm and 15 nm). Lines (—) represent the derived model whereas symbols (Δ) denote simulation results.

Fig. 3.6(a)-(b) depicts the variation of drain current (I_{ds}) with gate bias (V_{gs}) as a function of gate length and channel doping. The model is able to capture the expected variation with respect to L_g and N_{ch}. Due to the longer underlap length of 25 nm, the off-current can be limited to 1 nA even at a small gate length of 15 nm. As shown in Fig. 3.3, lower depletion of charge carriers essentially translates into a higher subthreshold current at relatively higher doping (10^{19} cm^{-3}) concentration. The same trend is followed in Fig. 3.6(b) where the maximum off-current (~7×10^{-9} A) is obtained for N_{ch} = 10^{19} cm^{-3}.

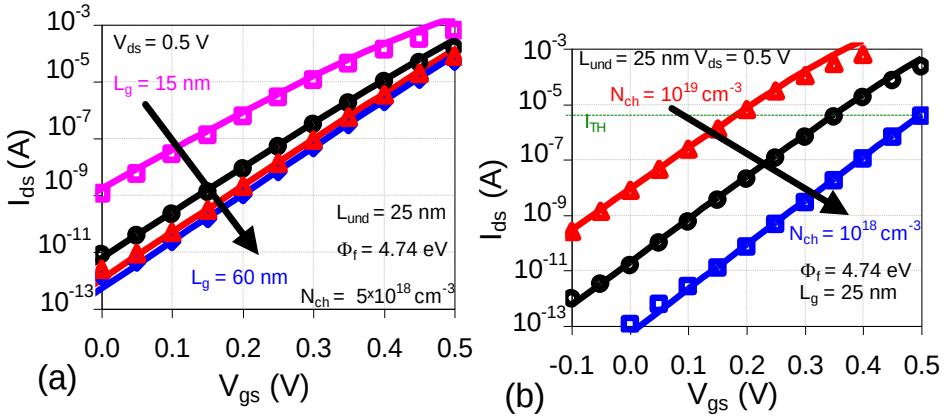

Fig. 3.6: I_{ds}–V_{gs} characteristics of Ge *n*MOS double gate JL transistors for different **(a)** gate length (L_g) and **(b)** doping (N_d). Symbols (Δ, o, □, ◊) denote simulation results whereas lines (—) represent the developed model. The four different values of L_g in **(a)** correspond to 60 nm, 45 nm, 30 nm and 15 nm.

Apart from *n*MOS Ge devices, the developed analytical model can be used to estimate I_{ds}–V_{gs} characteristics for *p*MOS transistors. The results, shown in Fig. 3.7(a)-(b), resemble a good agreement between modelled and simulated data for a wide range of L_g and N_{ch}. For *p*MOS, the workfunction is taken as 3.95 eV.

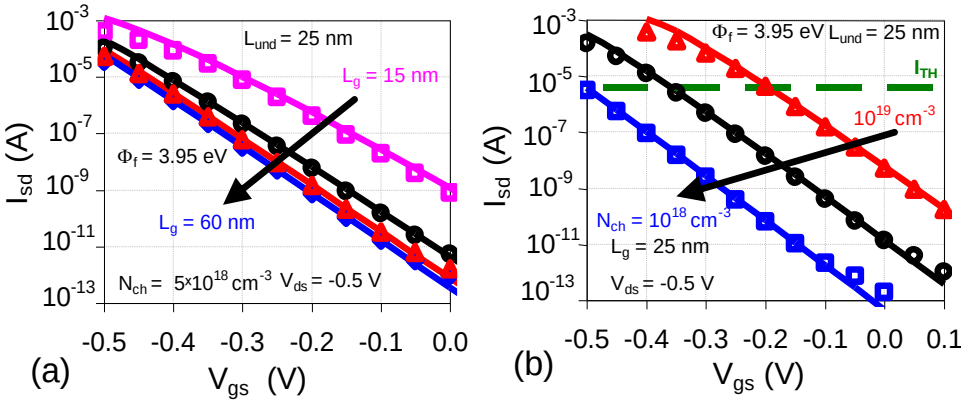

Fig. 3.7: I_{ds}–V_{gs} characteristics of Ge *p*MOS double gate JL transistors for different **(a)** gate length (L_g) and **(b)** doping (N_d). Symbols (Δ, o, □, ◊) denote simulation results whereas lines (—) represent the developed model. The four different values of L_g in **(a)** correspond to 60 nm, 45 nm, 30 nm and 15 nm.

3.4 Conclusion

This chapter has provided a detailed methodology to analyze the subthreshold characteristics, which can be utilized to suppress SCEs in Germanium-based DG JL MOSFETs by optimizing the gate-underlap regions, channel doping, and gate work function. The presented five-region semi-analytical model can reasonably capture electrostatic channel potential at any gate-underlap length and has shown good agreement with simulated data. A simplified analytical solution for subthreshold drain current can be utilized to evaluate threshold voltage, subthreshold swing, and SCEs related parameters. The developed model results have shown acceptable agreement with simulation for predicting SCEs for varying underlap length, gate workfunction, channel doping, gate length, and drain biases. The results obtained from TCAD simulation and developed model suggest that channel doping together with underlap region decide the short channel performance of Ge DG JL transistor, whereas SCEs remain unaffected by gate workfunction. An optimally long underlap length along with moderate doping can be advantageous to improve SCEs at shorter gate lengths.

References

[1] Snowden C. M., (1985) Semiconductor device modeling, Reports on Progress in Physics, 48, 223-275.

[2] Engl W. L., Dirks H. K., and Meinerzhagen B., (1983) Device modeling. In Proceedings of the IEEE, 71, pp. 10-33.

[3] Arora N., (2007) Overview. In MOSFET modeling for VLSI simulation: theory and practice, World Scientific Publishing Co. Pte. Ltd., pp. 1-14 (ISBN 978-981-256-862-5).

[4] Sou A., (2016) Modeling and simulation. In Practical guide to organic field effect transistor circuit design, Smithers Rapra Technology Ltd, pp. 29-44 (ISBN 978-1-91024-271-1).

[5] Yeo K. S., Rofail S. S., and Goh W. L., (2002) Device behavior and

modeling. In CMOS/BiCMOS ULSI: low voltage, low power. Pearson Education, Inc., pp.159-340 (ISBN 978-81-317-0826-2).

[6] Sheu B.J., Scharfetter D.L., Ko P.K., and Jeng M.C. (1987) BSIM: Berkeley short-channel IGFET model for MOS transistors, IEEE Journal of Solid-State Circuits, 22, 558-566.

[7] Kao S.K. and Sheu B. (2021) Bulk-Referenced Metal-Oxide Semiconductor Transistor Modeling With BSIM: A systematic approach to facilitate symmetric characteristics, IEEE Nanotechnology Magazine.

[8] Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., and Colinge J.-P., (2009) Junctionless multigate field-effect transistor, Applied Physics Letters, 94, 053511.

[9] Colinge J.-P., Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., Razavi P., O'Neill B., Blake A., White M., Kelleher A.-M., McCarthy B., and Murphy R., (2010) Nanowire transistors without junctions, Nature Nanotechnology, 5, 225-229.

[10] Jeon D.-Y., Park S. J., Mouis M., Berthomé M., Barraud S., Kim G.-T., and Ghibaudo G., (2013) Revisited parameter extraction methodology for electrical characterization of junctionless transistors, Solid-State Electronics, 90, 86-93.

[11] Colinge J.-P., Lee C.-W., Ferain I., Akhavan N. D., Yan R., Razavi P., Yu R., Navarob A. N., and Doria R. T., (2010) Reduced electric field in junctionless transistors, Applied Physics Letters, 96, 073510.

[12] Lee C.-W., Ferain I., Afzalian A., Yan R., Akhavan N. D., Razavi P., and Colinge J.-P., (2010) Performance estimation of junctionless multigate transistors, Solid-State Electronics, 54, 97-103.

[13] Lee C. W., Ferain I., Kranti , Akhavan N. D., Razavi P., Yan R., Yu R., O'Neill B., Blake A., White M., Kelleher A. M., McCarthy B., Gheorghe S., Murphy R., and Colinge J. P., (2010) Short-channel junctionless nanowire transistors, In Proceedings of International Conference of Solid State Devices and Materials (SSDM), Tokyo, Japan, pp. 1044-1045.

[14] Parihar M. S., Ghosh D., and Kranti A., (2013) Ultra low power

junctionless MOSFETs for subthreshold logic applications, IEEE Transactions on Electron Devices, 60, 1540-1546.

[15] Parihar M. S., and Kranti A., (2014) Revisiting the doping requirement for low power junctionless MOSFETs, Semiconductor Science and Technology, 29, 075006

[16] Fossum J. G., Chowdhury M. M., Trivedi V. P., King T.-J., Choi Y.-K., An J., and Yu B., (2003) Physical insights on design and modeling of nanoscale FinFETs, IEEE IEDM Technical Digest 2003, 29.1.1-29.1.4.

[17] Fossum J. G., (2007) Physical insights on nanoscale multi-gate CMOS design, Solid-State Electronics, 51, 188-194.

[18] Trivedi V., Fossum J. G., and Chowdhury M. M., (2005) Nanoscale FinFETs with Gate-Source/Drain underlap, IEEE Transactions on Electron Devices, 52, 56-62.

[19] Bansal A., and Roy K., (2007) Analytical subthreshold potential distribution model for gate underlap double-gate MOS transistors, IEEE Transactions on Electron Devices, 54, 1793-1798.

[20] Paul B. C., Bansal A., and Roy K., (2006) Underlap DGMOS for digital-subthreshold operation, IEEE Transactions on Electron Devices, 53, 910-913.

[21] Kim J. J., and Roy K., (2004) Double gate-MOSFET subthreshold circuit for ultralow power applications, IEEE Transactions on Electron Devices, 51, 1468-1474.

[22] Bansal A., Paul B. C., and Roy K., (2004) Impact of gate underlap on gate capacitance and gate tunneling current in 16nm DGMOS devices, In Proc. 2004 IEEE International SOI Conference, Charleston, SC, USA, pp. 94-95.

[23] Jan C. H., Bhattacharya U., Brain R., Choi S .- J., Curello G., Gupta G., Hafez W., Jang M., Kang M., Komeyli K., Leo T., Nidhi N., Pan L., Park J., Phoa K., Rahman A., Staus C., Tashiro H., Tsai C., Vandervoorn P., Yang L., Yeh J.-Y., and Bai P., (2012) A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low

power, high performance and high density SoC applications, IEEE IEDM Technical Digest 2012, 3.1.1-3.1.4.

[24] Parihar M. S., and Kranti A., (2014) Revisiting the doping requirement for low power junctionless MOSFETs, Semiconductor Science and Technology, 29, 075006.

[25] Bol D., Ambroise R., Flandre D., and Legat J. D., (2009) Interests and limitations of technology scaling for subthreshold logic, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 17, 1508-1519.

[26] Soeleman H., and Roy K., (1999) Ultra-low power digital subthreshold logic circuits, In Proceedings of 1999 International Symposium on Low Power Electronics and Design (Cat. No. 99TH8477), San Diego, CA, USA, pp. 94-96.

[27] Gupta S. K., Raychowdhury A., and Roy K., (2010) Digital computation in subthreshold region for ultralow-power operation: a device-circuit-architecture co-design perspective. Proceedings of the IEEE, 98, 160-190.

[28] Sharma R., Rana A.K., Kaushal S., King J., and Raman A., (2021) Analysis of Underlap Strained Silicon on Insulator MOSFET for Accurate and Compact Modeling.

[29] Chiang T. K., (2012) A quasi-two-dimensional threshold voltage model for short-channel junctionless double-gate MOSFETs, IEEE Transactions on Electron Devices, 59, 2284-2289.

[30] Jin X., Liu X., Kwon H.-I., Lee J.-H., and Lee J.-H., (2013) A subthreshold current model for nanoscale short channel junctionless MOSFETs applicable to symmetric and asymmetric double-gate structure, Solid-State Electronics, 82, 77-81.

[31] Hur J., Choi J.-M., Woo J.-H., Jang H., and Choi Y.-K., (2015) A generalized threshold voltage model of tied and untied double-gate junctionless FETs for a symmetric and asymmetric structure, IEEE Transactions on Electron Devices, 62, 2710-2716.

[32] Jazaeri F., Barbut L., Koukab A., and Sallese J.-M., (2013) Analytical

model for ultra-thin body junctionless symmetric double gate MOSFETs in subthreshold regime, Solid-State Electronics, 82, 103-110.

[33] Xie Q., Wang Z., and Taur Y., (2017) Analysis of short-channel effects in junctionless DG MOSFETs, IEEE Transactions on Electron Devices, 64, 3511-3514.

[34] Gnudi A., Reggiani S., Gnani E., and Baccarani G., (2013) Semianalytical model of the subthreshold current in short-channel junctionless symmetric double-gate field-effect transistors, IEEE Transactions on Electron Devices, 60, 1342-1348.

[35] Xiao Y., Zhang B., Lou H., Zhang L., and Lin X., (2016) A compact model of subthreshold current with source/drain depletion effect for the short-channel junctionless cylindrical surrounding-gate MOSFETs, IEEE Transactions on Electron Devices, 63, 2176-2181.

[36] Holtij T., Graef M., Hain F. M., Kloes A., and Iñíguez B., (2014) Compact model for short-channel junctionless accumulation mode double gate MOSFETs, IEEE Transactions on Electron Devices, 61, 288-299.

[37] Ávila-Herrera F., Cerdeira A., Paz B. C., Estrada M., Íñiguez B., and Pavanello M. A., (2015) Compact model for short-channel symmetric double-gate junctionless transistors, Solid-State Electronics, 111, 196-203.

[38] Xiao Y., Lin X., Lou H., Zhang B., Zhang L., and Chan M., (2016) A short channel double-gate junctionless transistor model including the dynamic channel boundary effect, IEEE Transactions on Electron Devices, 63, 4661-4667.

[39] Singh B., Gola D., Singh K., Goel E., Kumar S., and Jit S., (2017) 2-D analytical threshold voltage model for dielectric pocket double-gate junctionless FETs by considering source/drain depletion effect, IEEE Transactions on Electron Devices, 64, 901-908.

[40] Feng J., Liu P., Griffin P. B., and Plummer J. D., (2006) Integration of germanium-on-insulator and silicon MOSFETs on a silicon substrate, IEEE Electron Device Lett., 27, 911-914

[41] Kranti A. and Armstrong G. A., (2006) Engineering source/drain

extension regions in nanoscale double gate (DG) SOI MOSFETs: Analytical model and design considerations, Solid-State Electron., 50, 437-47

[42] Tsividis Y. and McAndrew C., (2010) Operation and Modeling of the MOS Transistor, 3rd edition, Oxford University Press, UK (*ISBN* 978-0-07-065381-8).

[43] Arora N. D., (2007) MOSFET Models for VLSI Circuit Simulation, 4th edition, World Scientific, Singapore (*ISBN* 978-0-387-82395-9).

[44] Taur Y., and Ning T. H., (2009) MOSFET devices. In: Fundamentals of modern VLSI devices, 2nd edn., Cambridge University Press, pp. 148-203 (ISBN 978-0-521-83294-6).

[45] Pierret R. F., (2006) Carrier modeling. In: Semiconductor Device Fundamentals, 1st edn., Pearson Education Inc., pp. 691-712 (ISBN 978-81-7758-977-1).

[46] Jaiswal N. and Kranti A., (2019) Modeling short channel effects in core-shell junctionless MOSFET, IEEE Transaction Electron Devices, 66, 292-299.

[47] Mohammadi S. and Khaveh H. R. T., (2017) An analytical model for double-gate tunnel FETs considering the junctions depletion regions and channel mobile charge carriers, IEEE Transaction Electron Devices, 64, 1276-1284.

[48] Young K. K., (1989) Short-channel effect in fully depleted SOI MOSFETs IEEE Transaction Electron Devices, 36, 399-402.

[49] Jin X., Liu X., Lee J.-H., and Lee J.-H., (2010) A continuous current model of fully-depleted symmetric double-gate MOSFETs considering a wide range of body doping concentrations, Semiconductor Science Technology, 25, 055018.

[50] Jin X., Liu X., Wu M., Chuai R., Lee J.-H., and Lee J.-H., (2013) A unified analytical continuous current model applicable to accumulation mode (junctionless) and inversion mode MOSFETs with symmetric and asymmetric double-gate structures, Solid-State Electronics, 79, 206-209.

[51] Lim C.-M., Zhao Z., Sumita K., Toprasertpong K., Takenaka M. and Takagi S., (2020) Operation of (111) Ge-on-Insulator n-channel MOSFET fabricated by smart-cut technology, IEEE Transaction Electron Devices, 67, 2988-2994.

[52] Ferain I., Colinge C. A., and Colinge J.-P., (2011) Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors, Nature, 479, 310-316.

[53] Atlas user's manual (2015) TCAD tool, Silvaco Inc., Santa Clara, CA, USA.

[54] Mar J., (1996) The application of TCAD in industry, In Proceedings of 1996 International Conference on Simulation of Semiconductor Processes and Devices, Tokyo, Japan, pp.139-145.

[55] Narang R., Saxena M., and Gupta M., (2017) Analytical model of pH sensing characteristics of junctionless silicon on insulator ISFET, IEEE Transactions on Electron Devices, 64, 1742-1750.

Chapter 4

Ultra-Low Power Logic Implementation with Germanium Junctionless Transistors

4.1 Introduction

Integrated circuits (ICs) are major building blocks of digital circuits. Different digital logic families were considered before finally moving to CMOS logic. Resistor-Transistor Logic (RTL) was the first in the digital logic family to be used commercially [1]. NAND and NOR are basic gates that were emphasized for the logic families and discussed as they were universal gates and forms basic building blocks for all advanced digital circuits. The different logic families are discussed below:

(i) Resistor-Transistor Logic (RTL) and Diode-Transistor Logic (DTL) [1-3]

NOR gate is the basic circuit for RTL family. Every input is assigned to one transistor and one resistor. The output is commonly connected to the collector of each transistor. The logic low can be represented by 0 V to 0.2 V voltage levels and logic high can be represented by 1 V to 3.6 V voltage levels. If RTL gate has a high input then the corresponding transistor is turned on and will be operated in the saturation region, and the output will be low regardless of the state of the other transistor. The dissipated power for a RTL logic gate is nearly 12 mW and the average propagation delay is 25 ns [1].

NAND gate is the basic circuit for DTL family [1]. Every input is auxiliary to a single diode. An AND gate is implemented using diode and resistor. A transistor is used as a current amplifier in common-emitter configuration to provide 180^{o} phase shift. The output is commonly connected to the collectors of the transistors. The logic low can be represented by 0 V to 0.2 V voltage levels and logic high can be represented by 4 V to 5 V voltage levels. If all RTL gates have a high input then only the corresponding transistors are turned on and the device will operate

in the saturation region. The dissipated power for a RTL logic gate is nearly 12 mW and the average propagation delay is 30 ns [1].

(ii) Transistor-Transistor Logic (TTL) [1]-[3]

TTL gate provides a slender enhancement over the DTL gate [1], [2]. For a transistor operating in the saturation region, the propagation delay is depends on time constant (*RC*) and the storage time [1]. The delay tends to reduce with decreasing the storage time. Similarly, if the resistor value in the circuit is reduced then the time constant decreases, and hence, propagation delay also decreases. However, for low resistance, more current will be drawn from the power supply and hence, power dissipation will increase significantly. Also, the speed of the gate directly depends on the propagation delay [2], [3]. The delay should be as small as possible to increase the gate speed. NAND gate is the basic circuit for TTL family implemented using NAND gate. The dissipated power for a TTL logic gate is nearly 10 mW and the average propagation delay is 9 ns [1].

(iii) Emitter-Coupled Logic (ECL) [1]

Both NOR and OR gates can be implemented using ECL logic. Since, earlier discussed logic families are based on the saturation region operation for transistor, but ECL represents non-saturated digital logic family. ECL family has the minimum propagation delay among digital logic families and even delay of 1 to 2 ns is achievable. ECL is generally used in very high speed applications. Some of the disadvantages of ECL family are poor noise immunity and higher power dissipation. The logic low can be represented by -0.8 V voltage and logic high can be represented by -1.8 V [1]. ECL circuitry incorporates a temperature and voltage compensated bias circuit, a differential amplifier, and an emitter follower output. The dissipated power for a TTL logic gate is nearly 25 mW and the average propagation delay is 2 ns [1].

(iv) Metal-Oxide-Semiconductor (MOS) Logic [1]-[3]

The reduction in integrated circuit area led to the emergence of MOS transistors. The gated region is insulated from the channel region by a dielectric

(generally Silicon dioxide for Silicon substrate). MOSFETs are basically are of two types (*n* and *p* type) depending on the charge carriers taking part in the current conduction. These are unipolar devices in which current flows mainly due to a particular charge carrier (either electron or hole). In *n*MOS, the current flows from drain to source. Similarly, for *p*MOS, current flows from source to drain. The device can be operated either in depletion or enhancement mode. MOS devices can be used as a transistor as well as a resistor operating in linear region of operation. The drain to source voltage and current determines the conduction, and hence, the resistance offered by the transistor. NAND and NOR gates can be implemented using both *n*MOS and *p*MOS. The static dissipated power for *n*MOS logic gate is 5 mW and the average propagation delay is 12 ns [1], [2].

(v) Complementary MOS (CMOS) Logic [1]-[6]

In CMOS circuits, both *n*MOS and *p*MOS are fabricated on a single substrate. These circuits are used to realize relatively complex Boolean logic functions. An inverter is the most basic CMOS circuit. It consists of both *n*MOS and *p*MOS with a common input connected at the gate terminals and V_{DD} is the supply voltage. The reference voltage is set to 0 V for logic low and V_{DD} for logic high. The value of V_{DD} generally varies from 3 V to 18 V in a standard circuit [1].

The static power dissipation of a typical CMOS is nearly 0.01 mW which is quite low as compared to other logic families [1], [3]. CMOS offers a small propagation delay and significantly enhances the noise immunity when operated at a higher supply voltage. Moreover, CMOS logic can be connected to the input and output of TTL based ICs. The CMOS fabrication process is easier as compared to TTL and imparts a higher packing density i.e. more number of transistors can be fabricated in the same area which makes it cost effective.

For Ultra Low Power (ULP) applications, the supply voltage is generally kept below the threshold voltage of the transistor which significantly reduces the power dissipation [4]. Therefore, CMOS can be operated below threshold without degrading the characteristics [4], [5]. Static leakage current and device sensitivity are two major concerns in ULP technology. The power consumption, propagation

delay, and circuit reliability are the factors which get affected by device reliability [5], [6]. These problems can be solved by using CMOS technology which has a low leakage current and sensitivity in the acceptable range [5], [6]. All these characteristics together make the CMOS family popular to be used in different digital logic applications. The static dissipated power for a CMOS logic gate is 0.01 mW and the average propagation delay is 8 ns [1].

4.2 CMOS Inverter

CMOS inverter serves as a basic logic concept, which is widely used in the modern day integrated circuits due to its low power consumption, negligible static power dissipation, and relatively higher switching speeds [3]. Moreover, CMOS inverter possesses excellent logic buffer characteristics with a significantly higher noise margins for both low and high logic levels [1]-[3]. Fig. 4.1(a) shows the CMOS inverter where V_{IN} is the input voltage applied at the gate terminal of *n*MOS and *p*MOS, V_{DD} is the supply voltage and V_O is the output voltage of the inverter. When the input voltage is increased from 0 to V_{DD}, *n*MOS and *p*MOS devices change operation from one region to another (linear, saturation or cut-off) as shown in Table 4.1.

Input voltage (V_{IN})	***n*MOS operating region**	***p*MOS operating region**
$0 < V_{IN} < V_{th,n}$	Cut-off	Linear
$V_{th,n} < V_{IN} < V_{DD}/2$	Saturation	Linear
$V_{IN} = V_{DD}/2$	Saturation	Saturation
$V_{DD}/2 < V_{IN} < (V_{DD}/2) - \lvert V_{th,p} \rvert$	Linear	Saturation
$(V_{DD}/2) - \lvert V_{th,p} \rvert < V_{IN} < V_{DD}$	Linear	Cut-off

Table 4.1: Operating regions for *n*MOS and *p*MOS for different input voltage (V_{IN}) range in a CMOS inverter. $V_{th,n}$ and $V_{th,p}$ are the threshold voltages for *n*MOS and *p*MOS, respectively [3].

Fig. 4.1(b) shows the dc transfer characteristics of an inverter. V_{IN} and V_O represent the input and output voltages, respectively, with V_{DD} denoting the supply voltage. V_H represents the nominal high output voltage (at V_{IN} = 0) which should ideally be equal to V_{DD}. Similarly, V_L is the nominal low output voltage at V_{IN} = V_{DD}, should be as close to zero as possible. V_{LT} represents the logic threshold value (V_{LT} = V_{IN} = V_O) which should ideally be equal to $V_{DD}/2$. For a symmetric CMOS inverter, the point at which the curve intersects at both the axis is referred to as V_{LT}. V_{Swing} represents full output swing when the input swings from 0 to V_{DD} and A_V is the magnitude of the small-signal voltage gain around the logic threshold. V_H, V_L, V_{LT}, and A_V are the characteristic parameters for a CMOS inverter. From Table 4.1 and Fig 4.1(b), it is clear that the gain corresponds to the region where V_{IN} = V_O, so that a small change in input causes a high change in the output.

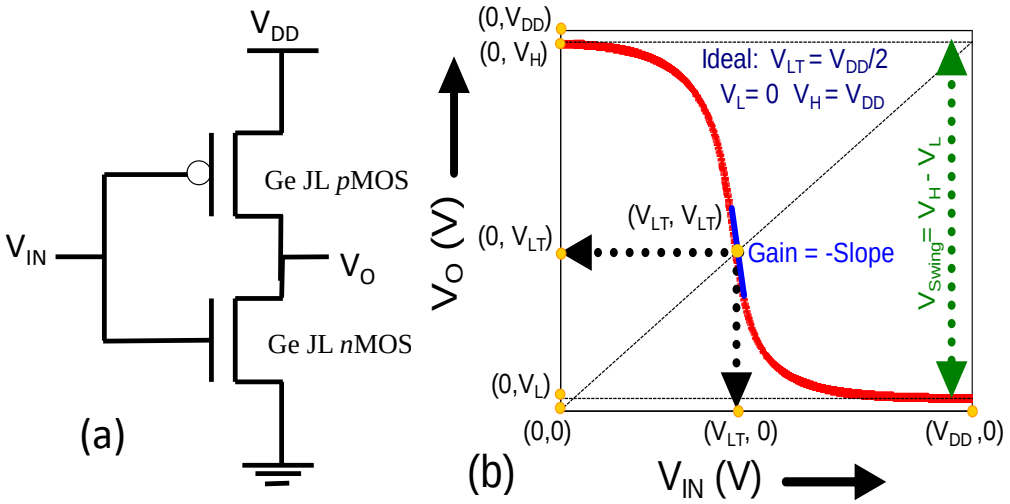

Fig 4.1: (a) Schematic diagram of a CMOS inverter. **(b)** Inverter characteristics highlighting key performance indicators

4.2.1 CMOS Inverter with Advanced MOSFETs

In this section, the validity of the proposed modeling approach to predict the key metrics of an inverter operating in the subthreshold region has been

demonstrated. The drain current in subthreshold region is usually expressed as [8], [9]

$$I_{ds} = I_O \frac{W}{L_g} \exp\left(\frac{q(V_{gs} - V_{th})}{\alpha kT}\right)\left(1 - \exp\left(\frac{-qV_{ds}}{kT}\right)\right) \tag{4.1}$$

where, I_O and α are the technology-dependent parameters. In order to utilize the relatively simple expression for I_{ds} given by equation (4.1) to assess the performance of an inverter, few parameters needs to be extracted first, the approach for the same is outlined below. In equation (4.1), the dependence of V_{th} on V_{ds} is formulated as

$$V_{th} = V_{th0} - \beta V_{ds} \tag{4.2}$$

where, V_{th0} is the threshold voltage at very low V_{ds} while β is a technology-dependent parameter that determines the extent of threshold voltage degradation with respect to V_{ds} and provides an indication of DIBL in the device. Thus, equation (4.1) contains three unknown parameters (α, β and I_O) which need to be evaluated. The value of β, for a given set of device parameters, can be easily extracted by the fitting equation (4.2) with V_{th} extracted through the model i.e. equation (3.24). The value of α can be evaluated from the subthreshold swing. Thereafter, I_O can be obtained as

$$I_O = \left(\frac{kT\mu_{n,Ge} n_{i,Ge} L_g}{L_T}\right) e^{\frac{-q(V_{th} - V_{gs})}{\alpha kT}} \tag{4.3}$$

The values of the extracted parameters for *n*MOS and *p*MOS devices are mentioned in Table 4.2.

Parameters	V_{th0} (V)	α	β	I_0 (A)
*n*MOS	0.387	1.11	0.061	8.6×10^{-8}
*p*MOS	0.40	1.11	0.0621	9.8×10^{-8}

Table 4.2: Extracted parameters for Ge based DG JL *n*MOS and *p*MOS MOSFET. Parameters: L_g = 30 nm, W = 1 μm, T_{Ge} = 9 nm and T_{GeON} = 1.65 nm, $N_{ch} = 5\times10^{18}$ cm^{-3}, L_{und} = 25 nm, Gate workfunction for *n*MOS (Φ_{fn})= 4.74 eV, and Gate workfunction for *p*MOS (Φ_{fp}) = 3.95 eV.

For the given set of parameters, the value of α for *n*MOS and *p*MOS transistors is determined to be ~1.11, which translates into S_{Swing} (= $\alpha KTln(10)/q$) of ~66 mV/decade. The DIBL factor, determined from β value as βV_{ds}, was extracted to be 24.4 mV for *n*MOS and 24.8 for *p*MOS devices. The off-current is given by

$$I_{off} = I_O\left(W/L_g\right)e^{\frac{-qV_{th0}}{\alpha kT}} e^{\frac{q\beta V_{ds}}{\alpha kT}}\left(1-e^{\frac{-qV_{ds}}{kT}}\right) \tag{4.4}$$

It is evaluated to be 7.4 pA and 5.8 pA for *n*MOS and *p*MOS transistors, respectively. The variation in V_{th} with V_{ds}, and I_{ds}-V_{gs} characteristics of *n*MOS and *p*MOS transistors is shown in Fig. 4.2(a)-(b). The performance of subthreshold Ge CMOS inverter depends on the on-to-off current ratio (I_{on}/I_{off}) of *n*MOS and *p*MOS transistors. Defining, I_{on} as the current at V_{th} for ULP subthreshold logic, I_{on}/I_{off} for both *n*MOS and *p*MOS devices is > 10^6 as shown in Fig. 4.2(b).

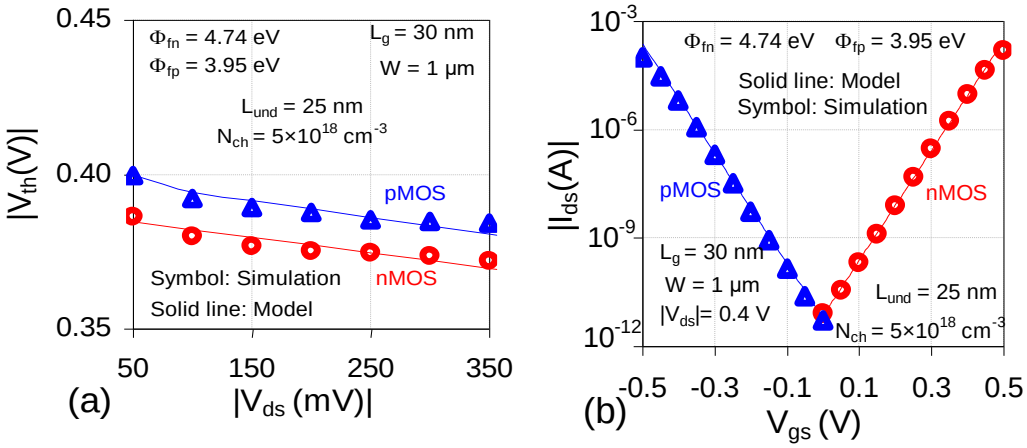

Fig. 4.2: (a) Variation of threshold voltage of *n*MOS and *p*MOS with the drain bias for extracting V_{th0} and β. **(b)** Drain current (I_{ds}) – gate voltage (V_{gs}) characteristics *n*MOS and *p*MOS Ge JL transistors used for extracting I_0 and α. Symbols (Δ, o) denote simulation results whereas lines (—) represent the developed model. Parameters: L_g = 30 nm, W = 1 μm, T_{Ge} = 9 nm and T_{GeON} = 1.65 nm, N_{ch} = 5×10^{18} cm^{-3}, L_{und} = 25 nm, Φ_{fn} = 4.74 eV and Φ_{fp} = 3.95 eV.

It should be noted that equation (4.1) is relatively simple, and therefore, the same cannot be directly applied to advanced devices such as nanoscale underlap transistors. However, after the extraction of relevant parameters (α, β and I_O) for advanced architectures through equation (3.24), equation (4.1) can be utilized to analyze an inverter operating in the subthreshold region. In subthreshold region, lower I_{on}/I_{off} ratio is the main concern for reducing V_H and V_L form their ideal values of V_{DD} and 0, respectively. This reduction in I_{on}/I_{off} occurs due to (i) reduction in V_{DD}, (ii) degraded S_{Swing} i.e. value of $\alpha > 1$, and (iii) an enhanced DIBL, exhibited through higher βV_{ds} value, in short channel transistors.

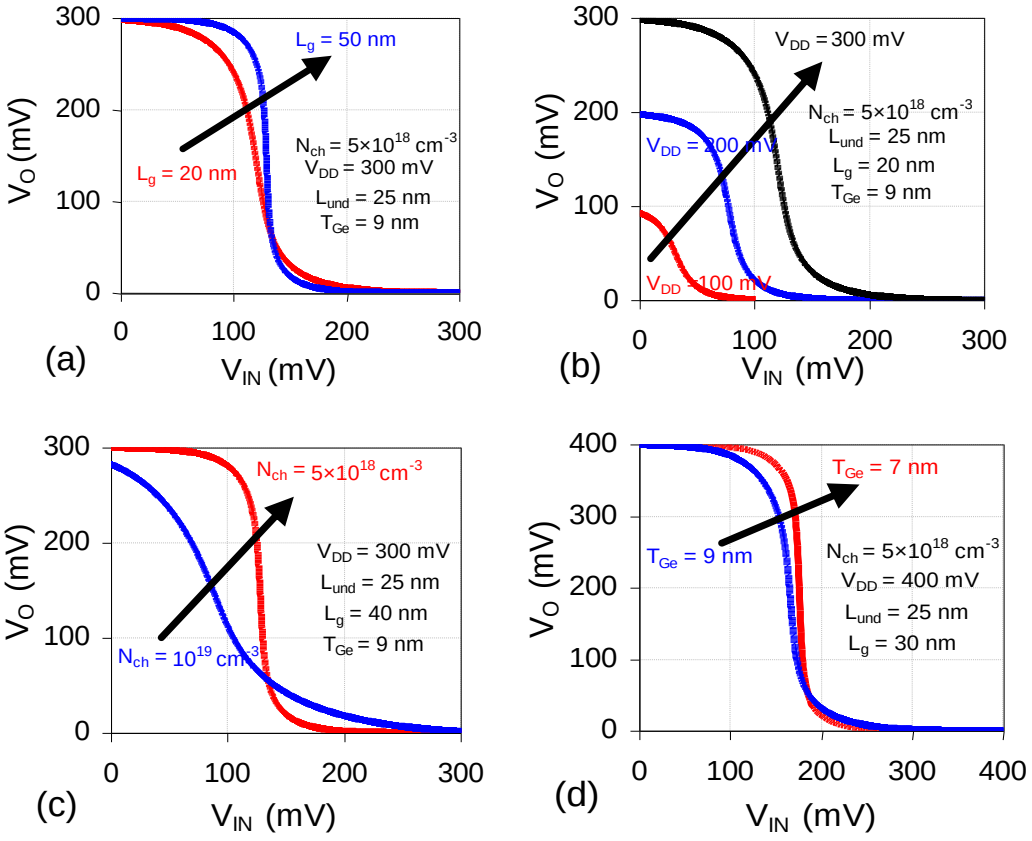

Fig. 4.3: Simulated transfer characteristics of DG Ge JL subthreshold inverter for various values of **(a)** gate length (L_g), **(b)** supply voltage (V_{DD}), **(c)** channel doping (N_{ch}) and **(d)** Ge film thickness (T_{Ge}).

4.2.2 Results and Discussion

Fig. 4.3(a) shows the impact of L_g downscaling from 50 nm to 20 nm on CMOS inverter characteristics. As evident from Fig. 4.3(a), V_{LT} and gain degrades due the higher I_{off} current at shorter channel length. The extracted α values are 1.21 and 1.18 for 20 nm for *n*MOS and *p*MOS Ge JL devices, respectively, whereas at 50 nm, α values improve to ~1.07 for both *n*MOS and *p*MOS Ge JL transistors. Similarly, β values are nearly 3 times higher (~0.09) at 20 nm as compared to those achieved (~0.03) for 50 nm devices. I_O values are also higher (0.86 nA and 0.97 nA for 20 nm *n*MOS and *p*MOS devices, respectively) as compared to those achieved (0.83 nA and 0.87 nA for 20 nm *n*MOS and *p*MOS devices, respectively) at 50 nm. The higher V_{th} values at 50 nm (0.40 V and 0.411 V for *n*MOS and *p*MOS, respectively) as compared to those achieved at 20 nm (0.362 V and 0.375 V for *n*MOS and *p*MOS, respectively) also indicate improved performance.

As shown in Fig. 4.3(b), a reduction in V_{DD} lowers I_{on}/I_{off} ratio, and inverter characteristics are degraded. For moderate V_{DD} values (200 mV and 300 mV), the inverter characteristic is similar to that exhibited by traditional above-threshold logic circuits [3]. However, the inverter characteristics are strongly degraded at very low supply voltage (~ 100 mV) which is due to the reduction in I_{on} i.e. on-current decreases from ~1.5 μA to ~1.3 nA. Therefore, at very low V_{DD} values, the device is unable to turn-on (offers high resistance), which results in a large voltage drop across the transistor. As a result, V_O does not reach V_{DD} (when *p*MOS is on) or 0 (when *n*MOS is on) and inverter characteristic is strongly degraded. The reduction in V_H (92 mV instead to 100 mV), V_{LT} (36 mV instead of 50 mV) and gain (2.44) is clearly visible for V_{DD} = 100 mV.

In Fig. 4.3(c), an increase in channel doping from 5×10^{18} cm^{-3} to 10^{19} cm^{-3} can drastically deteriorate the characteristics through a degradation in V_H, V_L, V_{LT} due to a reduction in V_{th} and S_{Swing} which consequently results in a higher I_{off}. Moreover, as described earlier in Fig. 3.6–3.7, a higher doping results in a substantial increase in carrier concentration which cannot be effectively depleted

in the off–state with the selected gate workfunction. By increasing the channel doping from 5×10^{18} cm^{-3} to 10^{19} cm^{-3}, α degrades from 1.08 to 1.15 for *n*MOS and from 1.08 to 1.3 for *p*MOS devices, β increases from 0.037 to 0.04 for *n*MOS and from 0.034 to 0.04 for *p*MOS transistors, V_{tho} decreases from 0.39 V to 0.238 V for *n*MOS (0.41 V to 0.25 V for *p*MOS). Due to significant change in values of V_{tho} and α, both swing and I_{off} degrade by a significant amount as discussed earlier. In Fig. 4.3(c), V_H degrades from 299.8 mV to 282 mV as N_{ch} is increased from 5×10^{18} cm^{-3} to 10^{19} cm^{-3}, respectively. Similarly, V_L degrades from 0 mV to 1.96 mV, V_{LT} from 128 mV to 103.5 mV, and gain from 23.6 to 2.4 for the same doping concentration.

The influence of Ge film thickness on the characteristics of subthreshold inverter can be seen clearly in Fig. 4.3(d). A thinner film suppresses SCEs and improves the gain of the inverter characteristics. The values of V_L (< 0.5 mV) and V_H (~ 400 mV) do not change much with T_{Ge} range shown in Fig. 4.3(d). However, the improvement in gain, from 15 to 30 for a reduction in T_{Ge} from 9 nm to 7 nm, respectively, is due to an improvement in β value from 0.060 (T_{Ge} = 9 nm) to 0.034 (T_{Ge} = 7 nm). It should be noted that the gain of subthreshold inverter is inversely proportional to β. I_{on}/I_{off} values do not change much to a reduction in both I_{off} and I_{on} with T_{Ge}.

In order to proceed further, the approach of Alioto [7] has been used, and adapted the already existing expressions for V_H, V_L, V_{LT} and A_V by utilizing the extracted values of α, β and I_O for underlap Ge JL DG transistors described in the preceding paragraphs. Fig. 4.4(a)-(f) shows the performance of subthreshold inverter with Ge junctionless devices. V_L and V_H values agree well with the simulation data for $V_{DD} \geq 100$ mV. This is due to the efficient transistor design and extraction methodology adopted for α, β and I_O, V_L values are limited to 5 mV in Ge JL transistors. A 16% error (~ 8 mV) is observed in simulation and modeled data for V_H at V_{DD} = 50 mV which reduces to less than 3% at $V_{DD} \geq 100$ mV.

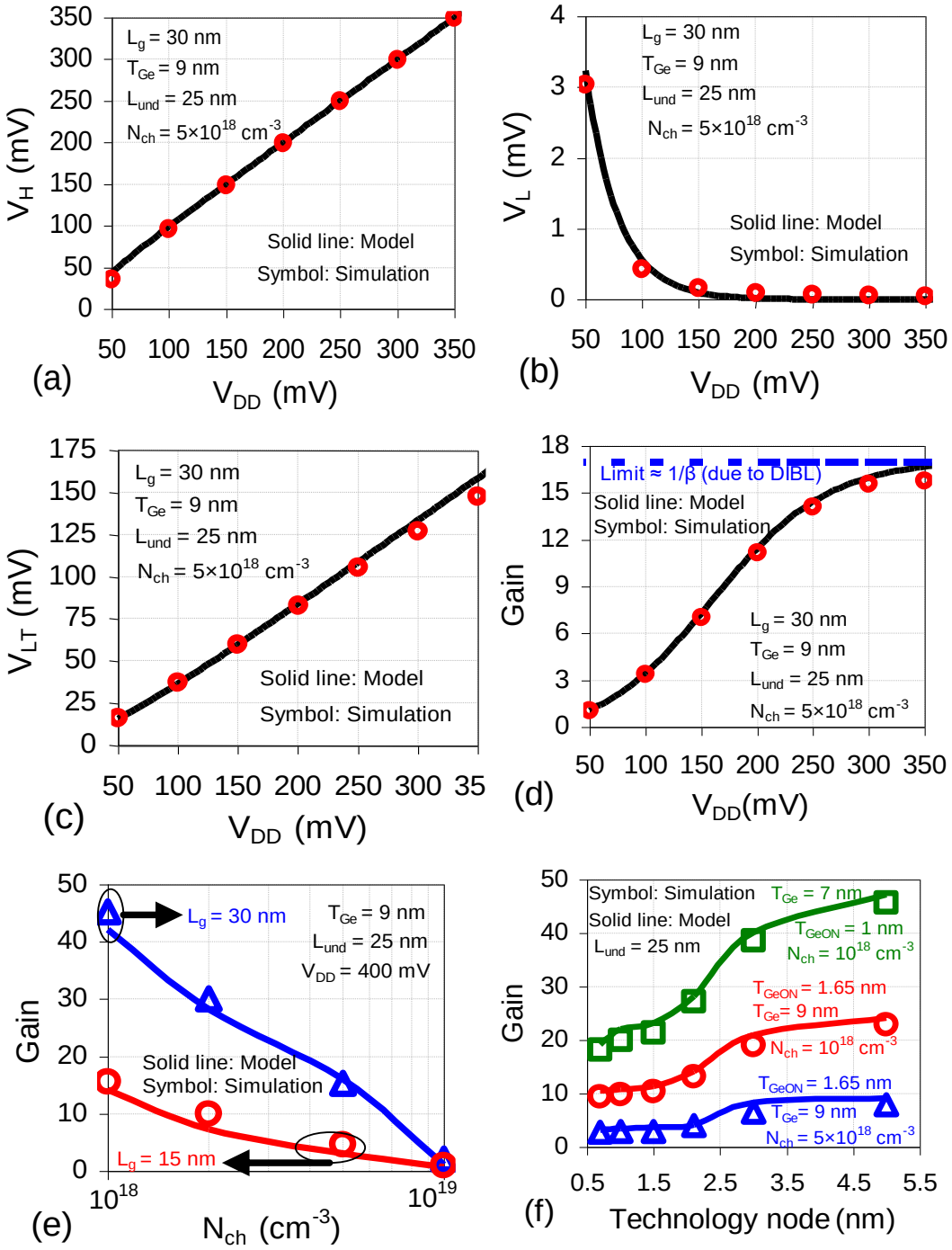

Fig. 4.4: Variation of **(a)** V_H, **(b)** V_L, **(c)** V_{LT}, and **(d)** subthreshold inverter gain with supply voltage (V_{DD}). Dependence of subthreshold inverter gain on **(e)** N_{ch} and **(f)** technology node downscaling. In Fig. 4.4(f), three different scaling options are shown to improve the gain at lower nodes. Symbols (Δ, o, □) denote simulation results whereas lines (—) represent the developed model.

As Ge *n*MOS transistor is slightly stronger than Ge *p*MOS device, the modeled results for V_{LT}, shown in Fig. 4.4(c), are slightly lower than $V_{LT} \approx V_{DD}/2$. As shown in fig. 4.4(d), the gain of the subthreshold inverter increases with V_{DD}, and finally saturates to ~16.5, a value determined by $1/\beta$ [7]. Efficient device design due to the incorporation of underlap region minimizes SCEs and reduces DIBL governing parameter (β) in sub-50 nm Ge JL devices. Fig. 4.4(e) shows the variation of gain with N_{ch}. This reduction in gain is due to the lesser extent of depletion and lower contribution of underlap regions at higher N_{ch}. The reduction in gain at lower L_g values can be compensated by reducing N_{ch}. Gain (~ 15) of subthreshold inverter at L_g = 30 nm with $N_{ch} = 5\times10^{18}$ cm^{-3} is nearly similar to that achieved at L_g = 15 nm with $N_{ch} = 10^{18}$ cm^{-3}. At a moderate doping of 2×10^{18} cm^{-3}, the gain is reduced by nearly 3 times as gate length is reduced by a factor of 2.

Technology node (nm)	Gate length (L_g) (nm)	Supply voltage ($V_{DD,IRDS}$) (V)	Subthreshold supply voltage ($V_{DD} = V_{DD,IRDS}/2$) (V)
5	20	0.70	0.350
3	18	0.70	0.350
2.1	14	0.65	0.325
1.5	12	0.65	0.325
1	12	0.60	0.300
0.7	12	0.55	0.275

Table 4.3: IRDS data for high density logic applications [10]. The supply voltage was reduced by a factor of 2 i.e. $V_{DD} = V_{DD,IRDS}/2$ to ensure subthreshold operation.

Since, no roadmap for subthreshold logic is available, and International Roadmap for Devices and Systems (IRDS) [10] concentrates on the high performance and high density applications, the impact of technology downscaling on the performance of Ge JL subthreshold inverter has been studied. The values of gate length considered in the analysis is taken from IRDS data [10] while the values of supply voltage ($V_{DD,IRDS}$) for each technology node is reduced by a

factor of 2 i.e. V_{DD} = $V_{DD,IRDS}$/2 to ensure subthreshold logic operation (Table 4.3).

This approach presents a reasonable assessment of Ge JL CMOS inverter for subthreshold logic applications. Various possible scenarios are also considered to enhance the gain in the technology evaluation. Gain reduces as the technology progresses to lower nodes. The maximum gain of the inverter designed with *n*MOS and *p*MOS Ge JL devices with N_{ch} = 5×10^{18} cm^{-3} is 9 whereas the minimum value is 3. These values can be enhanced to 25 at 5 nm technology node and 10 at 0.7 nm equivalent nodes if the channel doping is reduced to 10^{18} cm^{-3}.

Further improvement is possible if the values of gate insulator [11], [12] and Ge film thickness are also scaled down from 1.65 nm and 9 nm to 1 nm and 7 nm, respectively. An appreciable gain of 47 is achieved at 5 nm node while the value of gain is 19 for 0.7 nm node. The relatively high gain (~19) exhibited by the inverter at 0.7 nm node (L_g = 12 nm, V_{ds} = V_{DD} = $V_{DD,IRDS}$/2 = 0.275 V, N_{ch} = 10^{18} cm^{-3}) is due to the optimum design of Ge devices with a wider underlap (25 nm) which results in S_{Swing}, for both *n*MOS and *p*MOS Ge JL devices, of ~69 mV/decade. This translates into α of 1.15 for both devices.

The threshold voltage (V_{th}) of *n*MOS and *p*MOS Ge JL devices is 0.540 V and 0.547 V, respectively. The DIBL parameter is limited to ~21 mV for both *n*MOS and *p*MOS Ge JL transistors and I_{on}/I_{off} ratio ($\approx1.4\times10^{-7}/4.7\times10^{-13}$) is maintained to be $\sim3\times10^{5}$. These metrics for optimized Ge JL devices translates into a V_H = 274.9 mV, V_L = 6 μV and V_{LT} = 121.5 mV for the subthreshold inverter. These results clearly demonstrate a way forward to enhance the performance of subthreshold Ge JL CMOS inverter down to 0.7 nm node. Using this approach, a CMOS inverter is demonstrated and analyzed. Now in the next section, NAND and NOR gate logic is implemented using Ge devices. Since, these gates are universal; their implementation is of utter importance in order to perform digital logic operations and realize complex digital circuits.

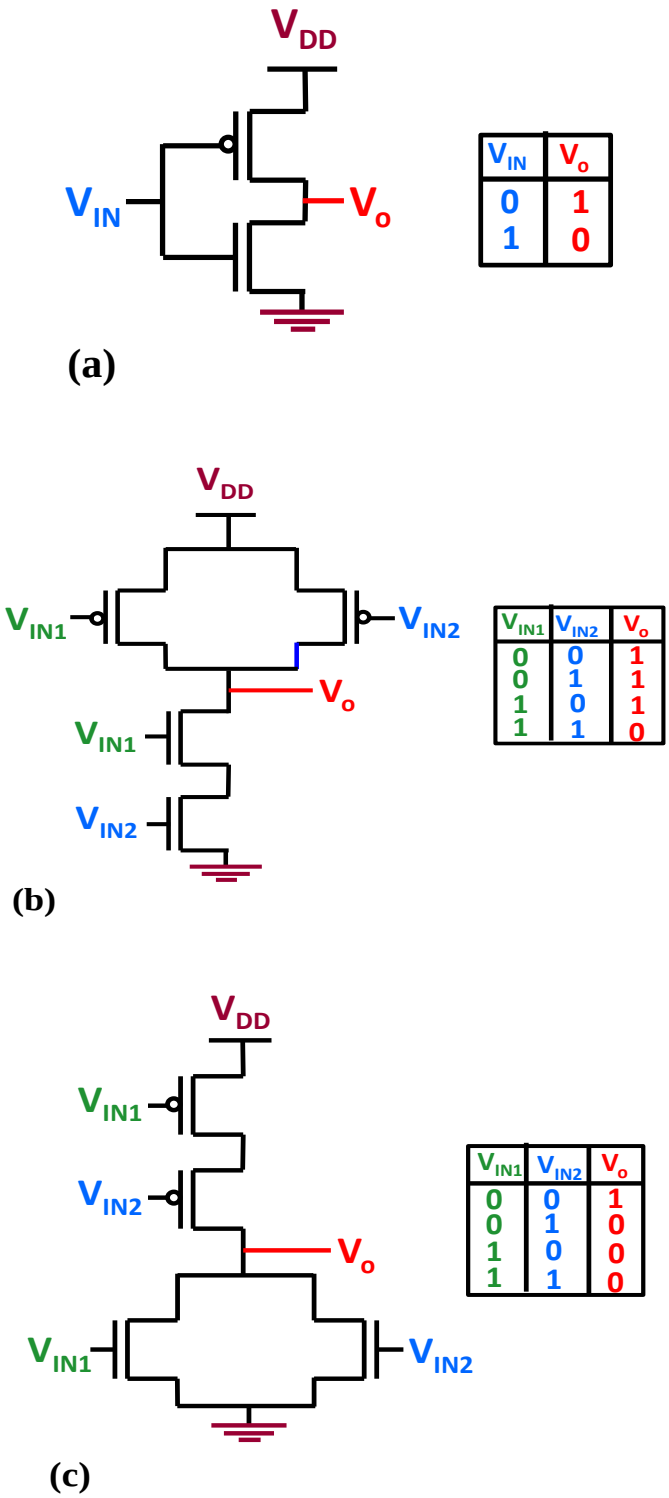

Fig. 4.5: Schematic diagram and truth table logic for (a) NOT gate, (b) NAND gate, and (c) NOR gate.

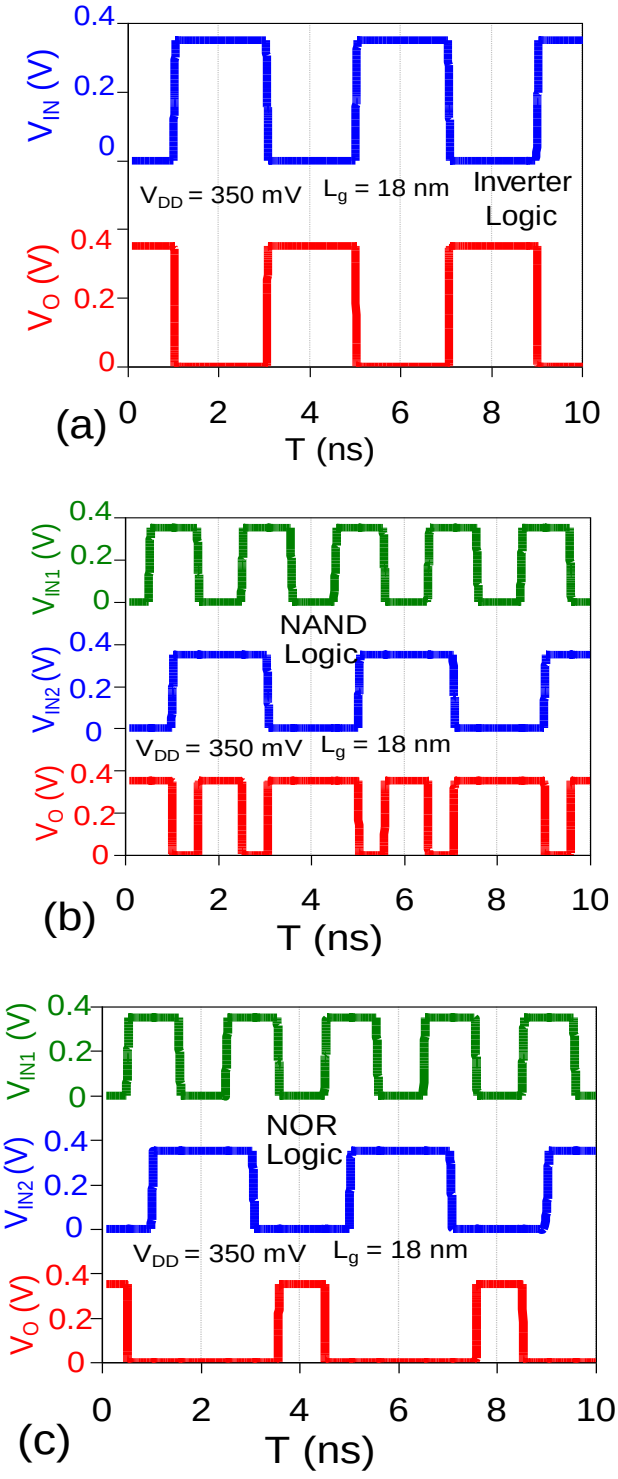

Fig. 4.6: Transient analysis of Ge ULP CMOS subthreshold **(a)** NOT (inverter), **(b)** NAND, and **(c)** NOR logic operations at 3 nm technology node with the power supply of 0.35 V. Parameters: L_g = 18 nm, N_{ch} = 10^{18} cm^{-3}, T_{Ge} = 7 nm and T_{GeON} = 1 nm.

4.3 NAND and NOR Gate Implementation

Focusing on subthreshold logic with Ge JL MOSFETs for the 3 nm technology (L_g = 18 nm) with a power supply of 0.35 V [10], the performance of NOT, NAND and NOR gates have been evaluated. For optimized devices, an optimal doping of 10^{18} cm^{-3} have been considered, film thickness (T_{Ge}) of 7 nm and oxide thickness (T_{GeON}) of 1 nm is used. NOT, NAND, and NOR schematics and logic truth tables are shown in Fig. 4.5(a)-(c), where logic 1 (HIGH) corresponds to ~V_{DD} (0.35 V) and logic 0 (LOW) to ~0 V. NAND and NOR are universal gates and their implementation shows the feasibility of utilizing optimally designed Ge JL devices for subthreshold logic applications.

Fig. 4.6(a) shows the transient analysis of CMOS inverter (NOT logic) designed using optimal Ge JL device for V_{DD} = 350 mV at 3 nm technology node. It indicates that even at lower technology nodes, a subthreshold CMOS inverter with optimized *n*MOS and *p*MOS device works reasonably well, and the reduction in nominal high output voltage is limited to ~13 μV, whereas low output voltage deteriorates only by ~2 μV. This considerably suppressed degradation reflects on the suitability of Ge JL CMOS devices for ULP applications. The nominal high output voltage of NAND and NOR logic operation degrades by ~6 μV and ~52 μV, respectively, while the nominal low output voltage corresponding to NAND and NOR gates is reduced by ~5 μV and ~2 μV, respectively. The analysis clearly reflects on the importance of selecting optimal device parameters to achieve decent subthreshold circuit performance at lower technology nodes.

4.4 Process Voltage Temperature (PVT) Variations

Sensitivity is an essential metric for ultra-low power (subthreshold) applications apart from the base performance indicators (I_{off}, V_{th}, DIBL, S_{Swing}). As described earlier in [13], the parameter sensitivity can be suppressed effectively by using moderate channel doping of 10^{18} cm^{-3} in junctionless devices instead of the usual doping of 10^{19} cm^{-3}. In subthreshold logic design, impact of PVT variations should be considered in the device as well as in circuit analysis.

Therefore, an analysis is conducted to evaluate the impact of variation in process dependent parameters (gate length (L_g), oxide thickness (T_{GeON}), channel thickness (T_{Ge}), channel doping (N_{ch}), and underlap length (L_{und})), voltage (supply voltage (V_{DD})), and temperature (T) on threshold voltage (V_{th}), off-current (I_{off}), and subthreshold swing (S_{Swing}) of Ge JL MOSFET. Similarly, the impact of process dependent parameters, supply voltage and temperature has been analyzed on low output voltage (V_L), high output voltage (V_H), logic threshold (V_{LT}) and gain (A_V) of a subthreshold CMOS inverter.

The sensitivity of a metric (M) on a parameter (P) is defined as [14] $S(P) = (\Delta M/M) / (\Delta P/P)$ where P can be any process dependent parameter (L_g, T_{Ge}, T_{GeON}, N_{ch} and L_{und}) or voltage (V_{DD}) or temperature (T) and M is the performance metric (V_{th}, I_{off}, S_{Swing} and A_V). The sensitivity has been evaluated by considering a ±5% variation in L_g, T_{Ge}, T_{GeON}, N_{ch}, L_{und}, V_{DD}, and temperature. Tables 4.4 and 4.5 show the sensitivity of PVT parameters on the device (V_{th}, I_{off}, S_{Swing}) and inverter (V_L, V_H, V_{LT} and A_V) metrics, respectively.

As expected, Ge film thickness is most sensitive parameter to V_{th} and I_{off}, followed by doping, gate oxide thickness, gate length, and underlap length (Table 4.4). Therefore, film thickness and doping should be carefully selected to ensure full depletion and lower current (in the off-state) in Ge ULP JL devices. Hence, V_{th} sensitivity on T_{Ge} and N_{ch} is higher than that obtained for other parameters. Off-current and subthreshold swing strongly depend on gate length as compared to N_{ch} and T_{GeON} at smaller technology nodes (~3 nm). T_{GeON} sensitivity on S_{Swing} is higher than N_{ch} because of the dependence of S_{Swing} on the gate oxide capacitance (= $\varepsilon_{GeON}/T_{GeON}$). For an optimal doping of 10^{18} cm^{-3}, the depletion region is expected to be extended into the underlap regions [15], [16] and therefore, sensitivity on L_{und} is less. As the effective channel length (in subthreshold) is longer than the gate length, the change in gate length leads to does not appreciably influence V_{th}, and sensitivity on L_g is rather less. As Ge JL device can suppress short channel effects comprehensively due to longer effective gate length, the sensitivity of V_{ds} on all the parameters is relatively low. As

expected, the sensitivity towards temperature is rather high. Among all the device metrics (V_{th}, I_{off}, S_{Swing}), I_{off} is the most sensitive to parameter variations.

Parameters		Sensitivity		
		V_{th}	I_{off}	S_{Swing}
Process dependent device parameters	T_{Ge}	0.171	2.97	0.067
	N_{ch}	0.077	0.884	0.003
	T_{GeON}	0.054	0.750	0.033
	L_g	0.050	1.454	0.065
	L_{und}	0.012	0.13	0.018
Voltage	V_{DD}	0.012	0.16	0.001
Temperature	T	0.215	26.436	1.035

Table 4.4: Sensitivity of V_{th}, I_{off} and S_{Swing} on process dependent device parameters, voltage, and temperature. Base parameters: L_g = 18 nm, T_{Ge} = 7 nm, T_{GeON} = 1 nm and V_{ds} = 0.35 V.

The sensitivity of subthreshold CMOS inverter is evaluated in terms of V_L, V_H, V_{LT} and A_V which depends on the subthreshold swing of the devices [7], [17]. Therefore, a variation in T_{Ge}, L_g and T_{GeON} will affect the above-mentioned metrics more than other parameters shown in Table 4.5. Due to the involvement of *n*MOS and *p*MOS Ge JL devices in the subthreshold inverter, maximum sensitivity values are reported for V_L, V_H, V_{LT} and A_V after considering different possible combinations for each device parameter. For example, all cases corresponding to ±5% variation in L_g for *n*MOS and *p*MOS Ge JL devices are considered and maximum sensitivity value is reported. Also, the sensitivity of subthreshold supply voltage (V_{DD}) on the gain is significant because a reduction in V_{DD} lowers I_{on}/I_{off} ratio, and consequently, inverter characteristics are degraded [7].The sensitivity of V_L and V_{LT} is higher as compared to all other metrics because of a degradation in off-current and threshold voltage of both *n*MOS and

*p*MOS devices due to a variation in parameters. The sensitivity of V_H is negligible for all the parameters which are expected for V_{DD} because of the higher dependence of I_{on}/I_{off} ratio on V_{DD} [7].

Parameters		Sensitivity			
		V_L	V_H	V_{LT}	A_V
Process dependent device parameters	T_{Ge}	2.27	0.085×10^{-3}	0.529	1.629
	L_g	2.23	0.083×10^{-3}	0.512	1.586
	T_{GeON}	1.10	0.041×10^{-3}	0.332	0.756
	N_{ch}	0.30	0.011×10^{-3}	0.061	0.130
	L_{und}	1.09	0.040×10^{-3}	0.189	0.051
Voltage	V_{DD}	1.10	1.0	1.05	0.955
Temperature	T	16.1	0.00128	1.41	3.062

Table 4.5: Sensitivity of V_L, V_H, V_{LT}, and A_V on process dependent device parameters, voltage, and temperature.

4.5 Conclusion

The static power dissipation of CMOS logic family is quite low as compared to other logic families, which makes CMOS family as a suitable option for downscaling and ultra-low power applications. A subthreshold CMOS inverter using Ge junctionless transistor has been analyzed in this chapter. The performance of subthreshold Ge CMOS inverter depends on the on-to-off current ratio (I_{on}/I_{off}) of *n*MOS and *p*MOS transistors. At very low V_{DD} values, the device is unable to turn-on (offers high resistance), which results in a relatively larger voltage drop across the transistor. As a result, the output voltage (V_O) does not reach V_{DD} (when *p*MOS is on) or 0 (when *n*MOS is on) and inverter characteristic is strongly degraded (as observed for V_{DD} = 100 mV case).

Higher doping concentration increases the carrier concentration and the device cannot be effectively depleted in the off–state with the selected gate workfunction. Also, increasing the channel doping from 5×10^{18} cm^{-3} to 10^{19} cm^{-3}, the value of subthreshold parameters α and β degrades (increases) for both *n*MOS and *p*MOS devices.

The influence of Ge film thickness on the characteristics of subthreshold inverter has been studied. A thinner film suppresses SCEs and improves the gain of the inverter characteristics. Efficient device design due to the incorporation of underlap region minimizes SCEs and reduces DIBL governing parameter (β) in sub-50 nm Ge JL devices. At a moderate doping of 2×10^{18} cm^{-3}, the gain is reduced by nearly 3 times as gate length is reduced by a factor of 2.

The circuit performance is improved by considering optimized device parameters. The values of gate oxide and Ge film thickness are scaled down from 1.65 nm and 9 nm to 1 nm and 7 nm, respectively. An appreciable gain of 47 is achieved at 5 nm node while the value of gain is 19 for 0.7 nm node.

References

[1] Mano M.M., and Ciletti, M., (2013) Digital design: with an introduction to the Verilog HDL, 3rd edn., Pearson India (ISBN 978-0-132-77420-8)

[2] Kumar A.A., (2016) Fundamentals of digital circuits, 4th edn., PHI Learning Pvt. Ltd. (ISBN 978-8-120-35268-1)

[3] Weste N., and Harris D., (2010) CMOS VLSI Design: A Circuits And Systems Perspective, 4th edn., Pearson India (ISBN 978-9-332-55904-2).

[4] Tajalli A., and Leblebici Y., (2011) Design trade-offs in ultra-low-power digital nanoscale CMOS, IEEE Transactions on Circuits and Systems, 58, 2189-2200.

[5] Bol D., Ambroise R., Flandre D., and Legat J.D., (2009) Interests and limitations of technology scaling for subthreshold logic, IEEE Transactions

on Very Large Scale Integration (VLSI) Systems, 17, 1508-1519.

[6] Calhoun B.H., Khanna S., Mann R., and Wang J., (2009), Sub-threshold circuit design with shrinking CMOS devices, IEEE International Symposium on Circuits and Systems, 2541-2544.

[7] Alioto M., (2010) Understanding DC behaviour of subthreshold CMOS logic through closed-form analysis, IEEE Transactions on Circuits and Systems–I, 57, 1597-1607.

[8] Tsividis Y. and McAndrew C., (2010) Operation and Modeling of the MOS Transistor, 3rd edition, Oxford University Press, UK (ISBN 978-0-07-065381-8).

[9] Arora N. D., (2007) MOSFET Models for VLSI Circuit Simulation, 4th edition, World Scientific, Singapore (ISBN 978-0-387-82395-9).

[10] IEEE International Roadmap for Devices and Systems 2020. Available online: https://irds.ieee.org/

[11] Lee T. I., Ahn H. J., Kim M. J., Shin E. J., Lee S. H., Shin S. W., Hwang W. S., Yu H.-Y. and Cho B. J., (2019) Ultrathin EOT (0.67 nm) high-k dielectric on Ge MOSFET using Y-doped ZrO_2 with record-low leakage current, IEEE Electron Device Letter, 40, 502-505.

[12] Yi S.-H., Chang-Liao K.-S., Hsu C.-W., and Huang J., (2018) Improved electrical characteristics of ~0.5 nm EOT Ge pMOSFET with GeON interfacial layer formed by NH_3 plasma and microwave annealing treatments, IEEE Electron Device Letter, 39, 1278-1281.

[13] Parihar M. S., and Kranti A., (2014) Revisiting the doping requirement for low power junctionless MOSFETs, Semiconductor Science Technology, 29, 075006.

[14] Lim T. C., and Armstrong G. A., 2005 Parameter sensitivity for optimal design of 65 nm node double gate SOI transistors, Solid-State Electronics, 49, 1034-1043.

[15] Fossum J. G., Chowdhury M. M., Trivedi V. P., King T.-J., Choi Y.-K., An J., and Yu B., (2003) Physical insights on design and modeling of nanoscale FinFETs, IEEE IEDM Technical Digest 2003, 29.1.1-29.1.4.

[16] Kranti A. and Armstrong G. A., (2006) Engineering source/drain extension regions in nanoscale double gate (DG) SOI MOSFETs: Analytical model and design considerations, Solid-State Electron., 50, 437-47.

[17] Kim J.-J., and Roy K., (2004) Double Gate-MOSFET subthreshold circuit for ultralow power applications, IEEE Transaction on Electron Devices, 51, 1468-1474.

[18] Parihar M. S., Ghosh D., and Kranti A., (2013) Ultra low power junctionless MOSFETs for subthreshold logic applications, IEEE Transaction on Electron Devices, 60, 1540-1546.

[19] Choi S.-J., Moon D.-I., Kim S., Duarte J. P., and Choi Y.-K., (2011) Sensitivity of threshold voltage to nanowire width variation in junctionless transistors, IEEE Electron Device Letters, 32, 125-127.

[20] Doria R. T., Pavanello M. A., Trevisoli R. D., de Souza M., Lee C.-W., Ferain I., Akhavan N. D., Yan R., Razavi P., Yu R., Kranti A., and Colinge J.-P., (2011) Junctionless multiple-gate transistors for analog applications, IEEE Transaction on Electron Devices, 58, 2511-2519.

[21] Shrivastava M., Mehta R., Gupta S., Agrawal N., Baghini M. S., Sharma D. K., Schulz T., Arnim K. V., Molzer W., Gossner H., and Rao V. R. (2011) Toward system on chip (SoC) development using FinFET technology: Challenges, solutions, process co-development & optimization guidelines, IEEE Transaction on Electron Devices, 58, 1597-1607.

[22] Doyle B. S., Datta S., Doczy M., Jin B., Kavalieros J., Linton T., Murthy A., Rios R., Chau R. (2003) High performance fully-depleted tri-gate CMOS transistors, IEEE Electron Device Letters, 24, 263-265.

[23] Zhang W., Fossum J. G., Mathew L., and Du Y. (2005) Physical insights regarding design and performance of independent-gate FinFETs, IEEE Transaction on Electron Devices, 52, 2198-2206.

[24] Colinge J.-P. (2004) Multiple gate SOI MOSFETs, Solid-State Electronics, 48, 897-905.

[25] Fossum J.G., Ge L., and Chiang M-H. (2002) Speed superiority of scaled double-gate CMOS, IEEE Transaction on Electron Devices, 49, 808-811.

[26] Wong H.-S. P., frank D. J., and Solomon P. M. (1998) Device design consideration for double-gate, ground-plane and single-gate ultra-thin SOI MOSFETs at the 25 nm channel length generation, IEEE Electron Devices Meeting, 407-410.

[27] Wong H.-S. P., Chan K. K., and Taur Y. (1997) Self-aligned (top and bottom) dual-gate MOSFET with a 25 nm thick silicon channel, IEEE Electron Devices Meeting, 427-430.

[28] Suzuki K., Tanaka T., Tosaka Y., Horie H., and Arimoto Y. (1993) Scaling theory for double-gate SOI MOSFETs, IEEE Transaction on Electron Devices, 40, 2326-2329.

[29] Balestra F., Cristoloveanu S., Benachir M., Brini J and Elewa T (1987) Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance, IEEE Electron Device Letters, 8, 410-412.

[30] Choi J. Y., and Fossum J. G. (1991) Analysis and control of floating body bipolar effects in fully depleted submicrometer SOI MOSFET's, IEEE Transaction on Electron Devices, 38, 1384–1391.

[31] Jaiswal N., and Kranti A., (2018) A Model for gate-underlap- dependent short-channel effects in junctionless MOSFET, IEEE Transaction Electron Devices, 65, 881-887.

[32] Jaiswal N., and Kranti A., (2019) Modeling short channel effects in core-shell junctionless MOSFET, IEEE Transaction Electron Devices, 66, 292-299.

[33] Taur Y., and Ning T. H., (2009) MOSFET devices. In: Fundamentals of modern VLSI devices, 2nd edn., Cambridge University Press, pp. 148-203 (ISBN 978-0-521-83294-6).

[34] Pierret R. F., (2006) Carrier modeling. In: Semiconductor Device Fundamentals, 1st edn., Pearson Education Inc., pp. 691-712 (ISBN 978-81-7758-977-1).

[35] Atlas user's manual (2015) TCAD tool, Silvaco Inc., Santa Clara, CA, USA.

[36] Ghosh D., Parihar M. S., Armstrong G. A., and Kranti A., (2012) High-performance junctionless MOSFETs for ultralow-power analog/RF applications, IEEE Electron Device Letters, 33, 1477-1479.

[37] Yan R., Kranti A., Ferain I., Lee C.W., Yu R., Dehdashti N., Razavi P., and Colinge J.-P., (2011) Investigation of high-performance sub-50 nm junctionless nanowire transistors, Microelectronics Reliability, 51, 1166-1171.

Chapter 5

Conclusions and Scope for Future Work

5.1 Conclusion

JL transistors can possibly be good substitutes to replace conventional nanoscale MOSFETs for the next generation of devices [1]-[4]. These transistors eliminate the requirement for abrupt *pn* junction formation. Their main features include simple fabrication processes requirements, improved short channel immunity and increased miniaturization boundaries than conventional MOSFETs [5], [6]. Since Low Power (LP) or Ultra Low Power (ULP) logic technology require transistors that exhibit greater command over subthreshold characteristics along with suppressed SCEs [7], JL MOSFETs show capabilities for LP or ULP technologies rather than for High Performance (HP) logic applications [8], [9].

In accordance with the nearly identical doping concentration and dopant type throughout the semiconductor film, an effective extended length that is greater than gate length in the off-state is achieved in a JL. This reflects on the improved short channel performance of the device as compared to the conventional MOSFETs [10], [11]. However, the value of effective length in the subthreshold regime depends on lateral S/D depletion extensions, which vary with device parameters. The thesis has deduced semi-analytical model to predict SCEs in Germanium DG JL FETs considering the lateral extension of the depletion region in the source/drain extension regions. The architecture that has been analyzed considers simultaneously-driven symmetric DG structure with S/D underlap lengths. The developed 2D models have satisfactorily captured the dependence of device parameters and biases on SCEs in Ge DG JL MOSFETs. Overall Germanium is used as the film material, where by optimizing the device parameters the short channel effects associated with Ge device can be reduced to an adequate level. Also, at lower technology nodes, the use of underlap length is

also vital for the suppression of short channel effects. Channel doping also played an important role in the working of the device.

The static power dissipation of CMOS logic family is quite low as compared to other logic families, which makes CMOS family as a potential alternative for ultra-low power applications. A subthreshold CMOS inverter using Ge junctionless transistor is implemented in the later section of the thesis. The performance of subthreshold Ge CMOS inverter depends on the on-to-off current ratio (I_{on}/I_{off}) of *n*MOS and *p*MOS transistors. At very low V_{DD} values, the device is unable to turn-on (offers high resistance), which results in a large voltage drop across the transistor. As a result, the output voltage (V_O) does not reach V_{DD} (when *p*MOS is on) or 0 (when *n*MOS is on) and inverter characteristic is strongly degraded (as observed for V_{DD} = 100 mV case). Higher doping concentration increases the carrier concentration and the device cannot be effectively depleted in the off–state with the selected gate workfunction. Also, increasing the channel doping from 5×10^{18} cm^{-3} to 10^{19} cm^{-3}, the value of subthreshold parameters α and β degrade (increases) for both *n*MOS and *p*MOS devices. The influence of Ge film thickness on the characteristics of subthreshold inverter has been studied. A thinner film suppresses SCEs and improves the gain of the inverter characteristics. Efficient device design due to the incorporation of underlap region minimizes SCEs and reduces DIBL governing parameter (β) in sub-50 nm Ge JL devices. At a moderate doping of 2×10^{18} cm^{-3}, the gain is reduced by nearly 3 times as gate length is reduced by a factor of 2. The circuit performance is improved by considering optimized device parameters. The values of gate oxide and Ge film thickness are scaled down from 1.65 nm and 9 nm to 1 nm and 7 nm, respectively. An appreciable gain of 47 is achieved at 5 nm node while the value of gain is 19 for 0.7 nm node.

(i) Modeling the Dependence of SCEs on G-S/D Underlap Regions in JL Transistor

The derived five-region semi-analytical model for channel potential has resulted in the evaluation of G-S/D underlap-dependent SCEs in *n*-type Ge double

gate JL MOSFET for symmetric operation (i.e., simultaneously operated front and back gates with same values of gate oxide thicknesses and work-functions, and gate-source/drain underlap lengths) with the inclusion of mobile charge density. This derived model can be applicable for every underlap length, and hence, has a generic formulation. Approximate analytical solutions of subthreshold drain current can be utilized to obtain the device transfer characteristics, thereby to extract V_{th}, S_{Swing} and SCEs related parameters. The derived model results agree fairly well with the simulation data. Past investigations have shown that L_{und} and N_{ch} are two key parameters that can be varied to control SCEs in these devices. Reducing N_{ch} allows easy penetration of the gate electric field, thereby leading to better electrostatic control of gate over the gated region. With increasing L_{und}, SCEs can be reduced until maximal space charge region extensions allowed by the device parameters are achieved. Thus, the option of sufficiently longer L_{und} and moderate N_{ch} can prove advantageous to suppress SCEs in these devices at lower technology nodes.

(ii) Applicability of Proposed Model for Subthreshold Logic Applications

The application part of the implemented novel device is shown in chapter 4. A subthreshold CMOS inverter is implemented using Ge JL *n*MOS and *p*MOS devices. The approach of Alioto [12] is adapted in the CMOS inverter analysis. Universal gates (NAND and NOR) are also implemented in order to show the applicability of the developed model. The sensitivity of subthreshold CMOS inverter is evaluated in terms of V_L, V_H, V_{LT} and A_V which depends on the subthreshold swing of the devices [12], [13]. The sensitivity results have been analyzed. A variation in T_{Ge}, L_g and T_{GeON} affects the V_L, V_H, V_{LT} and A_V more than other parameters considered for analysis. The sensitivity of V_L and V_{LT} is higher as compared to all other metrics because of a degradation in off-current and threshold voltage of both *n*MOS and *p*MOS devices due to a variation in parameters. The sensitivity of V_H is negligible for all the parameters which are expected for V_{DD} because of the higher dependence of I_{on}/I_{off} ratio on V_{DD} [12].

An in-depth analysis focusing on Ge junctionless transistors for subthreshold logic has been presented. Contrary to the conventional viewpoint, short channel effects in Ge transistors can be effectively suppressed by adopting an underlap architecture which will be most useful for ultra-low power (subthreshold) logic applications at lower technology nodes. Optimally designed Ge JL transistors with 12 nm gate length and underlap length of 25 nm exhibit DIBL of ~21 mV with subthreshold swing of ~69 mV/decade with off-current of ~0.5 pA. The subthreshold drain current of *n*MOS and *p*MOS Ge JL transistors has been modeled through the solution of Poisson's equation in which the effect of underlap regions has been considered. The developed framework is further applied to extract relevant technology dependent parameters (α, β and I_O) that makes it convenient to utilize the conventional subthreshold current expression to advanced (with underlap) transistor topologies. The work is further extended to examine the performance of Ge JL CMOS subthreshold inverter down to 0.7 nm technology node and logic operations for NOT gate. NAND and NOR functionality have been shown. Sensitivity analysis highlights the need for precise control of critical parameters for optimal device/circuit performance. This thesis provides much needed insights into the design and optimization of Ge based devices for subthreshold logic applications at lower technology nodes.

5.2 Scope for Future Work

In the present work, symmetric mode operation of Germanium Double-gate Junctionless transistor is analyzed. Similar work can be possible for asymmetric mode working of Ge DG JL transistor. For asymmetric mode operation, DG MOSFET provides additional flexibility to alter its performance [14]-[19]. In recent years, structural asymmetries (non-identical front and back gate workfunctions and oxide thicknesses) and independent gate operation (front and back bias asymmetry) have been widely exploited to tune V_{th} [14], [15], to improve S_{Swing} and I_{OFF} [15]-[17] and to enhance performance [18], [19] of DG MOSFETs.

Core shell architecture DG JL transistor can also be implemented using Germanium thin film. Symmetric and asymmetric mode operation DG MOSFET suffers from various detrimental effects that can be unfavorable for downscaling and LP applications. These effects include off-state BTBT [20], [21], RDFs [22]-[24], mobility degradations due to impurity scattering [35], [36], and limits on the choice of gate workfunction for obtaining appropriate threshold voltage [13], [27]. Using Core shell architecture for JL transistors can significantly improve S_{Swing} [28], higher I_{ON}/I_{OFF} ratio [29], and lower sensitivity towards RDFs [30], [31]. These devices have also shown to provide suppressed off-state BTBT current [32] and higher mobility values [33], thus showing favorable prospects for downscaling and LP technology.

References

[1] After Moore's Law (2016) Technology Quarterly, The Economist. https://www.economist.com/sites/default/files/march_2016.pdf. Accessed 12 March 2016.

[2] International Technology Roadmap for Semiconductors (ITRS) 2.0 Publications (2015), http://www.itrs2.net/itrs-reports.html.

[3] Kahng A. B., (2017) Scaling: more than Moore's law, IEEE Design & Test of Computers, 27, 86-87.

[4] Bohr M. T., and Young I. A., (2017) CMOS scaling trends and beyond, IEEE Micro, 37, 20-29.

[5] Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., and Colinge J.-P., (2009) Junctionless multigate field-effect transistor, Applied Physics Letters, 94, 053511.

[6] Colinge J.-P., Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., Razavi P., O'Neill B., Blake A., White M., Kelleher A.-M., McCarthy B., and Murphy R., (2010) Nanowire transistors without junctions, Nature Nanotechnology, 5, 225-229.

[7] Jan C. H., Bhattacharya U., Brain R., Choi S .- J., Curello G., Gupta G.,

Hafez W., Jang M., Kang M., Komeyli K., Leo T., Nidhi N., Pan L., Park J., Phoa K., Rahman A., Staus C., Tashiro H., Tsai C., Vandervoorn P., Yang L., Yeh J.-Y., and Bai P., (2012) A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications, IEEE IEDM Technical Digest 2012, 3.1.1-3.1.4.

[8] Parihar M. S., and Kranti A., (2014) Revisiting the doping requirement for low power junctionless MOSFETs, Semiconductor Science and Technology, 29, 075006.

[9] Rios R., Cappellani A., Armstrong M., Budrevich A., Gomez H., Pai R., Rahhal-orabi N., and Kuhn K., (2011) Comparison of junctionless and conventional trigate transistors with L_g down to 26 nm, IEEE Electron Device Letters, 32, 1170-1172.

[10] Lee C.-W., Ferain I., Afzalian A., Yan R., Akhavan N. D., Razavi P., and Colinge J.-P., (2010) Performance estimation of junctionless multigate transistors, Solid-State Electronics, 54, 97-103.

[11] Lee C. W., Ferain I., Kranti , Akhavan N. D., Razavi P., Yan R., Yu R., O'Neill B., Blake A., White M., Kelleher A. M., McCarthy B., Gheorghe S., Murphy R., and Colinge J. P., (2010) Short-channel junctionless nanowire transistors, In Proceedings of International Conference of Solid State Devices and Materials (SSDM), Tokyo, Japan, pp. 1044-1045.

[12] Alioto M., (2010) Understanding DC behaviour of subthreshold CMOS logic through closed-form analysis, IEEE Transaction Circuits and Systems–I, 57, 1597-1607.

[13] Parihar M. S., and Kranti A., (2014) Revisiting the doping requirement for low power junctionless MOSFETs, Semiconductor Science Technology, 29, 075006.

[14] Han J. W., Kim C. J., and Choi Y.-K., (2008) Universal potential model in tied and separated double-gate MOSFETs with considerations of symmetric and asymmetric structures, IEEE Transactions on Electron Devices, 55, 1472-1479.

[15] Liu Y., Matsukawa T., Endo K., Masahara M., O'uchi S., Ishii K., Yamauchi H., Tsukada J., Ishikawa Y., and Suzuki E., (2007) Cointegration of high-performance tied-gate three-terminal FinFETs and variable threshold-voltage independent-gate four-terminal FinFETs with asymmetric gate-oxide thicknesses, IEEE Electron Device Letters, 28, 517-519.

[16] Masahara M., Surdeanu R., Witters L., Doornbos G., Nguyen V. H., Van den bosch G., Vrancken C., Devriendt, Neuilly F., Kunnen E., Jurczak M., and Biesemans S., (2007) Demonstration of asymmetric gate-oxide thickness four-terminal FinFETs having flexible threshold voltage and good subthreshold slope, IEEE Electron Device Letters, 28, 217-219.

[17] Dey A., Chakravorty A., DasGupta N., and DasGupta A., (2008) Analytical model of subthreshold current and slope for asymmetric 4-T and 3-T double-gate MOSFETs, IEEE Transactions on Electron Devices, 55, 3442-3449.

[18] Ieong M., Jones E. C., Kanarsky T., Ren Z., Dokumaci O., Roy R. A., Shi L., Furukawa T., Taur Y., Miller R. J., and Wong H-S P., (2001) Experimental evaluation of carrier transport and device design for planar symmetric/asymmetric double-gate/ground-plane CMOSFETs, IEEE IEDM Technical Digest 2001, 19.6.1-19.6.4.

[19] Widiez J., Poiroux T., Vinet M., Mouis M., and Deleonibus S., (2006) Experimental comparison between sub-0.1-μm ultrathin SOI single- and double-gate MOSFETs: performance and mobility, IEEE Transactions on Nanotechnology, 5, 643-648.

[20] Sahay S., and Kumar M. J., (2016) Insight into lateral band-to-band tunneling nanowire junctionless FETs, IEEE Transaction on Electron Devices, 63, 4138-4142.

[21] Gundapaneni S., Bajaj M., Pandey R. K., Murali K. V. R. M., Ganguly S., and Kottantharayil A., (2012) Effect of band-to-band tunneling on junctionless transistors, IEEE Transactions on Electron Devices, 59, 1023-1029.

[22] Nawaz S M, Dutta S, Chattopadhyay A, and Mallik A, (2014) Comparison of random dopant and gate-metal workfunction variability between junctionless and conventional FinFETs, IEEE Electron Device Letters, 35**,** 663-65.

[23] Leung G and Chui C O, (2012) Variability impact of random dopant fluctuation on nanoscale junctionless FinFETs, IEEE Electron Device Letters, 33**,** 767-69.

[24] Nawaz S M, Dutta S and Mallik A, (2015) A comparison of random discrete dopant induced variability between Ge and Si junctionless p-FinFETs, Appl. Phys. Lett., 107**,** 033506.

[25] Doria R. T., Pavanello M. A., Trevisoli R. D., de Souza M., Lee C.-W., Ferain I., Akhavan N. D., Yan R., Razavi P., Yu R., Kranti A., and Colinge J.-P., (2011) Junctionless multiple-gate transistors for analog applications, IEEE Transaction on Electron Devices, 58, 2511-2519.

[26] Lee C.-W., Borne A., Ferain I., Afzalian A., Yan R., Akhavan N. D., Razavi P., and Colinge J.-P., (2010) High-temperature performance of silicon junctionless MOSFETs, IEEE Transaction on Electron Devices, 57, 620-625.

[27] Colinge J.-P., Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., Razavi P., O'Neill B., Blake A., White M., Kelleher A.-M., McCarthy B., and Murphy R., (2010) Nanowire transistors without junctions, Nature Nanotechnology, 5, 225-229.

[28] Lee Y.-J., Cho T.-C., Kao K.-H., Sung P.-J., Hsueh F.-K., Huang P.-C., Wu C.-T., Hsu S.-H., Huang W. -H., Chen H.-C., Li Y., Current M. I., Hengstebeck B., Marino J., Büyüklimanli T., Shieh J.-M., Chao T.-S., Wu W.-F., and Yeh W.-K., (2014) A novel junctionless FinFET structure with sub-5 nm shell doping profile by molecular monolayer doping and microwave annealing, IEEE IEDM Technical Digest 2014, 32.7.1-32.7.4.

[29] Lee Y.-J., Cho T.-C., Sung P.-J., Kao K.-H., Hsueh F.-K., Hou F.-J., Chen P.-C., Chen H.-C., Wu C.-T., Hsu S.-H., Chen Y.-J., Huang Y.-M., Hou Y.-F., Huang W.-H., Yang C.-C., Chen B.-Y., Lin K.- L., Chen M.-

C., Shen C.-H., Huang G.-W., Huang K.-P., Current M. I., Li Y., Samukawa S., Wu W.-F., Shieh J.-M., Chao T.-S., and Yeh W.-K., (2015) High performance poly Si junctionless transistors with sub-5 nm conformally doped layers by molecular monolayer doping and microwave incorporating CO_2 laser annealing for 3D stacked ICs applications, IEEE IEDM Technical Digest 2015, 6.2.1-6.2.4.

[30] Song Y., and Li X., (2014) Scaling junctionless multigate field-effect transistors by step-doping, Applied Physics Letters, 105, 223506.

[31] M. P. V. Kumar, C.-Y. Hu, K.-H. Kao, Y.-J. Lee, and T.-S. Chao, (2015) Impacts of the shell doping profile on the electrical characteristics of junctionless FETs, IEEE Transactions on Electron Devices, 62, 3541-3546.

[32] Sahay S., and Kumar M. J., (2016) Controlling L-BTBT and volume depletion in nanowire JLFETs using core-shell architecture, IEEE Transaction on Electron Devices, 63, 3790-3794.

[33] Bhuvaneshwari Y. V., and Kranti A., (2018) Assessment of mobility and its degradation parameters in a shell doped junctionless transistor, Semiconductor Science and Technology, 33, p. 115020.

[34] Jaiswal N., and Kranti A., (2018) Modeling short-channel effects in asymmetric junctionless MOSFETs with underlap, IEEE Transaction on Electron Devices, 65, 3369–3375

[35] Jaiswal N. and Kranti A., (2019) Modeling short channel effects in core-shell junctionless MOSFET, IEEE Transaction Electron Devices, 66, 292-299.