STEP UP PWM DC-DC CONVERTERS BASED ON QUASI Z-SOURCE AND QUADRATIC BOOST CONVERTER

Ph.D. Thesis

By

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DISCIPLINE OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

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A THESIS

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Dedicated to my Parents

ABSTRACT

Step-up DC-DC converters are having increasing demand because of its applications in photovoltaic (PV) power generation, fuel cell based energy conversion, uninterrupted power supplies (UPS) and battery powered equipment. In general, a conventional boost converter can be adopted to provide a high step-up voltage gain with a large duty ratio. However, the conversion efficiency and the step-up voltage gain are limited due to the constraints of the losses of power switches and diodes, the equivalent series resistance of inductors and capacitors, and the reverse-recovery problem of diodes.

Therefore, a step-up converter with a low duty ratio to achieve high efficiency and high voltage gain is very important for these applications. In order to improve the conversion efficiency at low power, non-isolated converters are preferred for these high step-up applications. Among non-isolated topologies reported in literature for step up applications, Z-source converter and Quasi Z-source converter topologies are comparatively new with many desirable features.

The work in the thesis focuses on study and development of new configurations based on Quasi Z-source DC-DC converters and quadratic boost converter for high step-up applications. Fourth order step up converter based on quasi Z-source converter is presented with its small signal mode and controller design in second chapter of thesis. The fourth-order converter poses many desirable features. Proposed converter's design equations are established and same are validated through laboratory prototypes. The work also focuses on control of these converters, One Cycle Control technique is used for controlling output voltage of Z-source and quasi Z-source based converters.

Further, tapped-inductor and coupled-inductor variations of QZS based fourth order DC-DC converter are proposed. Tapped-inductor is utilized for voltage gain enhancement of fourth-order converter. In tapped-inductor based configuration voltage gain of the converter is depend upon duty ratio and turns ratio. Voltage gain expressions for ideal and non-ideal tapped-inductor based converter is derived and experimentally verified. The main aim of coupled-inductor based converter is to reduce input current ripple of

fourth order quasi z-source converter. Theoretical analysis of current ripple in coupled inductor is presented and also verified using simulation and hardware results.

A high step up converter based on fourth order quasi Z-source converter and boost converter is derived. Performance of non-ideal converter is theoretically analyze and demonstrated. Small signal model of the converter is utilized for controller design of high step up converter. Two converter configurations based on quadratic boost converter and tapped-inductor are introduced in sixth chapter of thesis. Performance of both converters for different load resistance and for different combination of turns ratio is studied.

TABLE OF CONTENTS

Chapter 3

3.1 Tapped-inductor Quasi-Z-source Based PWM DC-DC converter

3.2: A step-up PWM DC-DC converter with zero input current ripple

Chapter 4: One Cycle control of Z-source, Quasi-Z-source and fourth-order step-up DC-DC Converters

Chapter 7: Conclusions

LIST OF FIGURES

LIST OF TABLES

NOMENCLATURE

Symbol- Definition

V_{in} - Input DC voltage

V_0 -Output voltage

S -Switch

R -Load resistance

F -Switching frequency

P_0 - Output power

η - Efficiency

T_S - Switching period

V_{DC} - dc link voltage

V_{C1} - quiescent voltage of C_1 capacitor

V_{C2} - quiescent voltage of C_2 capacitor

v_{C1} - C_1 capacitor voltage

v_{C2} - C_2 capacitor voltage

I_{L1} -quiescent value of L_1 inductor current

I_{L2} -quiescent value of L_2 inductor current

i_{L1} - L_1 inductor current

i_{L2} - L_2 inductor current

Φ_1 - quiescent value of flux through L_1

Φ_2 - quiescent value of flux through L_2

n_1,n_2 - turns ratio of L_1 and L_2

k,k_x - coupling coefficient

D - quiescent value of duty ratio

d - average value of duty ratio

r_{L1} - resistance of inductor L_1

r_{L2} - resistance of inductor L_2

D_x - diodes

φ_1 - flux through inductor core L_1

φ_2 - flux through inductor core L_2

L_1 - inductor 1

L_2 - inductor 2

L_{11} - first part of tapped inductor L_1

L_{12} - second part of tapped inductor L_1

L_{21} - first part of tapped inductor L_2

L_{22} - second part of tapped inductor L_2

N_{11} - number of turns of L_{11}

N_{12} - number of turns of L_{12}

N_{21} - number of turns of L_{21}

N_{22} - number of turns of L_{22}

r_{L11} - resistance of inductor L_{11}

r_{L12} - resistance of inductor L_{12}

r_{L21} - resistance of inductor L_{21}

r_{L22} - resistance of inductor L_{22}

r_{C1} - resistance of C_1capacitor

r_{C2} - resistance of C_2capacitor

K_o - One cycle control constant

K_C - constant in boundary condition

$\hat{i}_x$ - Small signal variation in current

$\hat{v}_x$ - Small signal variation in voltage

$\hat{d}$ - Small signal variation in duty ratio

Δv_x - Voltage ripple

Δi_x - Current ripple

δv_x - Variation from average value of voltage

δi_x - Variation from average value of current

i_S - Switch current

i_D - Diode current

$\widehat{v}_x$ - Peak value of voltage

$\widehat{i}_x$ - Peak value of current

M, M_{ideal}- Ideal Gain

$M_{nonideal}$ - Non-Ideal Gain

P_{loss} - Sum of losses

P_D - Power loss in diode

P_S - Power loss in switch

P_{rlx} - Power loss in inductor

P_{rcx} - Power loss in capacitor

V_{SM} - Maximum value of voltage across switch

I_{XAV} - Average value of current

V_{XAV} - Average value of voltage

I_R - Remaining current

$G_{vg}(s)$ -Transfer function of output to input voltage

$G_{ig}(s)$ - Transfer function of input current to input voltage

$G_{vd}(s)$ -Transfer function of output voltage to duty ratio

$G_{ilxd}(s)$ -Transfer function of inductor current to duty ratio

$C_X(s)$ -Transfer function of compensator

$T_X(s)$ -Transfer function of loop

V_F - Forward drop voltage of diode

L_f - Filter inductor

C_f - Filter capacitor

$\dot{i}_{Lx}$ - Ripple current

ACRONYMS

ZS - Z-Source

ZSC - Z-Source Converter

ZSI - Z-Source Inverter

QZS - Quasi Z-Source

QZSI - Quasi Z-Source Inverter

OCC - One Cycle Control

CCM - Continuous Conduction Mode

DCM - Discontinuous Conduction Mode

PWM - Pulse Width Modulation

RHP - Right Hand Plane

EMI - Electro Magnetic Interference

Chapter 1
Introduction and literature review

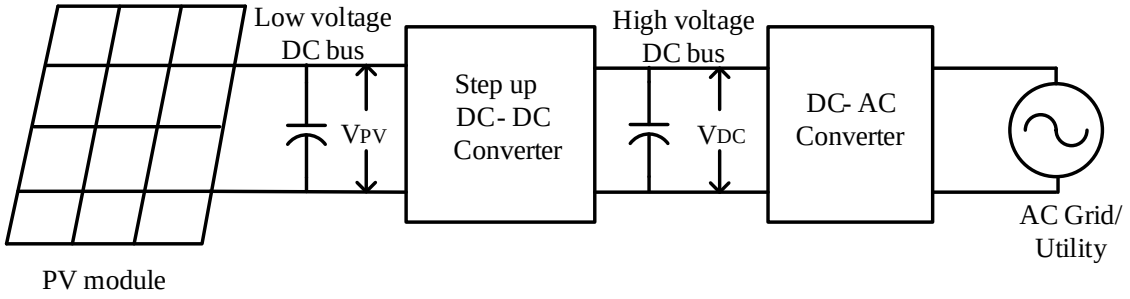
1.1 Introduction

DC-DC converters with high voltage conversion ratio are now having increasing demand because of its applications in photovoltaic (PV) power generation systems, fuel cell based energy conversion systems, uninterrupted power supplies (UPS), high-intensity-discharge headlamps of automobiles and battery powered equipment.

Commercial PV module presents normally maximum power point power is lower than 300W and maximum power point voltage range from 15V-50V [1]. PV modules are connected in series and parallel to increase voltage and power level. However, a common problem in this arrangement is generation reduction due to partial shading of series connected PV modules [2]. Fuel-cells have been considered as excellent candidate to replace conventional fossil fuel in vehicles and emergency energy sources. Fuel-cells stack can provide voltage in the range of 40V-80V [3]. In order to use PV modules and fuel-cells for AC load or utility, it is required to process available energy to convert in suitable form as shown in Fig. 1. Front-end stage circuits of these applications need high step up converters to increase the source's voltage to the level required by the application and to produce a stable output voltage despite variations on the source voltage. Second stage of this process requires DC-AC converter. High intensity discharge lamp ballasts for automobile head lamps needs high step-up converters to boost 12V from battery to almost 100V at steady operation [4], [5].

Conventionally, boost converter or buck-boost converter with high duty ratio can be used for such applications. However, in practical implementation, the extreme high duty ratio operation may result in serious reverse-recovery problem, low efficiency and electromagnetic interference (EMI) problem [6]. Therefore many step-up topologies are reported in literature for high step-up operations. The main motive behind these topologies is to get higher boost with lower duty ratio and to reduce losses for a given power.

Following section reviews some of the basic non-isolated and isolated topologies of high step-up converters reported in literature.



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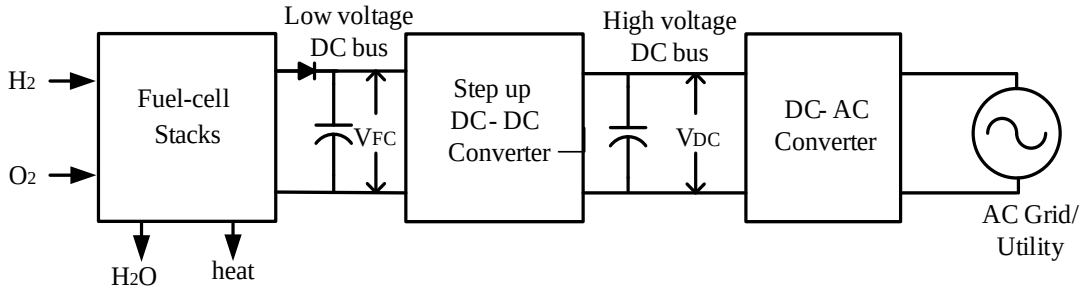

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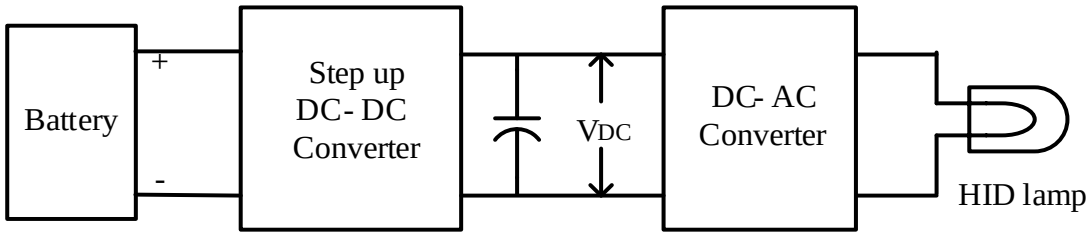


(c)

Fig.1.1: Applications of high step-up DC-DC converters (a) PV power generation system, (b) Fuel-cell power generation system and (c) HID lamp ballast.

1.2 Review of step-up DC-DC converters

In step-up applications, high step-up DC-DC converters are required as an integral interface between low voltage sources and the output loads, which operates at higher voltages. In literature, many researchers concentrate on how to realize high step-up converter to satisfy the requirement of above mentioned applications. This section gives an overview on available high step-up converters. The converter topologies reported in literature are mainly classified in isolated and non-isolated configurations of converters. Further, converters are grouped according to technique used for obtaining high conversion ratio.

1.2.1 Non-isolated converter topologies

1.2.1.1 Boost converter

The conventional single switch boost converter is shown in Fig. 1.2. Theoretically voltage gain of boost converter can be infinite when duty ratio approaches to one. However, the switch turn-off becomes short when duty ratio increases. At high duty ratio switch power loss increases and current ripples are large. This converter also suffers reverse recovery and electromagnetic interference at high duty ratio [7]. The voltage gain of boost converter can be given by

$$\frac{V_0}{V_{in}} = \frac{1}{1-D} \tag{1.1}$$

Where V_0 - output voltage, V_{in} - input voltage and D is duty ratio. The duty ratio can be defined as the ratio of switch ON time to sum of switch ON and switch OFF time.

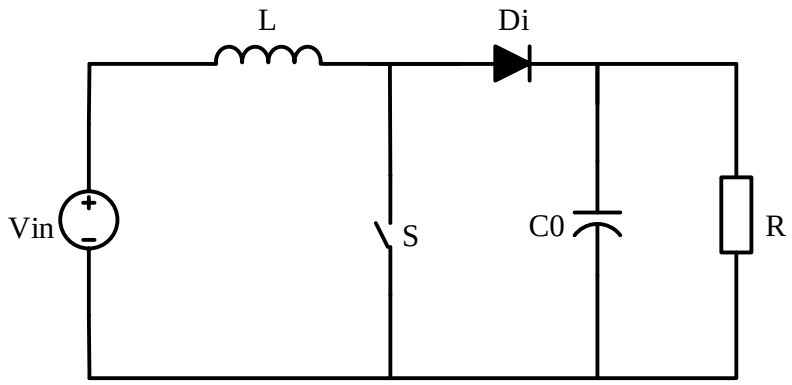


Fig. 1.2: Boost converter.

1.2.1.2 Interleaved boost converters

The interleaved boost converter shares the input current and reduces the current ripple. Input current ripple reduction is desirable feature for fuel cell and PV energy sources. Figure 1.3(a) shows a two phase conventional interleaved boost converter. The efficiency is limited and output diode reverse recovery problem is still serious for high output voltage applications. Interleaved boost converter voltage gain can be improved by using couple inductor in place of uncoupled inductors as shown in Fig. 1.3(b) [8].

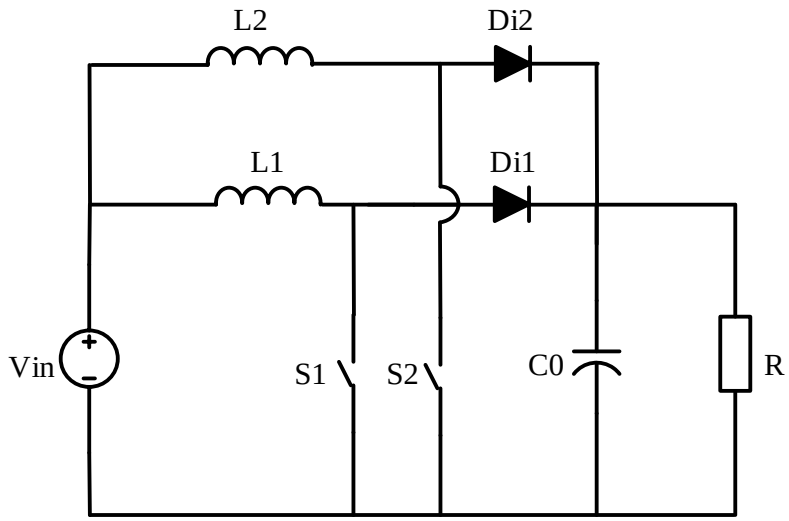


Fig. 1.3(a): Interleaved boost converter.

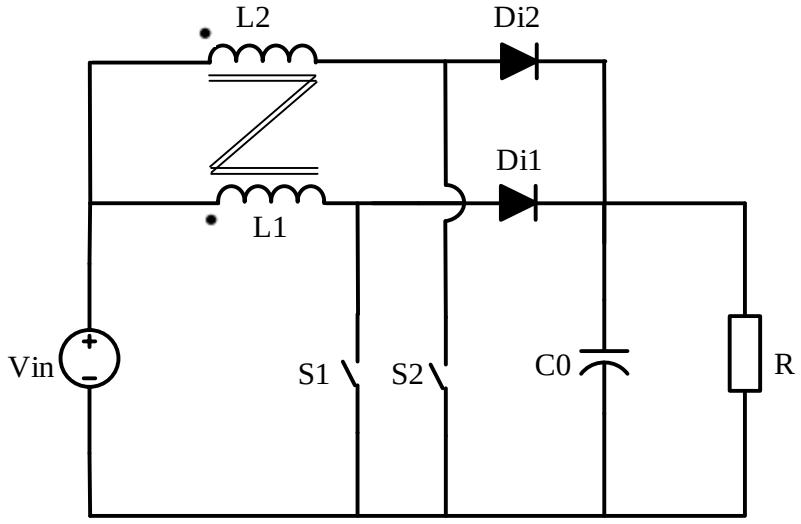


Fig. 1.3(b): Coupled-inductor interleaved boost converter.

1.2.1.3 Three level boost converter

The conventional three level boost converter is as shown in Fig. 1.4. This converter can double the voltage gain and can reduce voltage stress of the power device in comparison with the conventional boost converter, these features makes it more suitable for low–voltage-input high voltage output applications. Due to lower voltage stress on power device, MOSFETs with lower switch-ON resistance can be used to reduce the converter cost and the conduction losses. However output diode reverse recovery problem is severe.

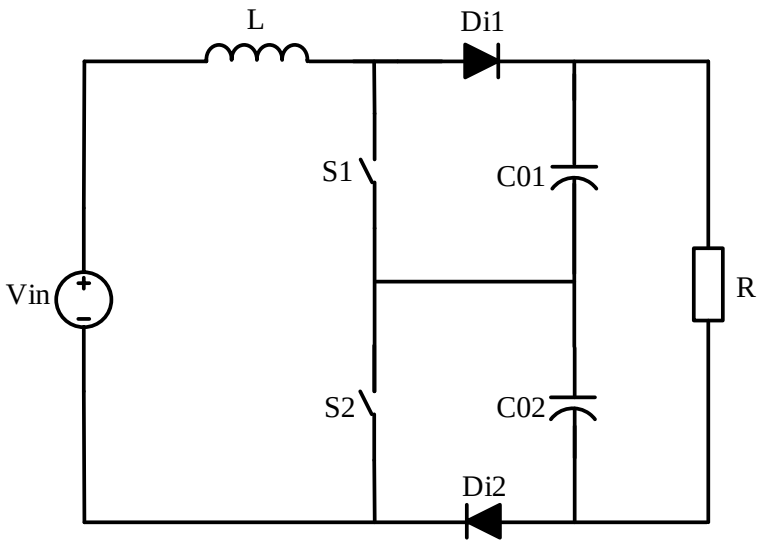


Fig. 1.4: Three level boost converter.

1.2.1.4 Cascaded boost converter

The voltage gain of three level boost converter is still not large enough for high step-up applications. The voltage gain can be increased to satisfy the requirements by using cascade structure as shown in Fig. 1.5(a). In this topology, the voltage stress of the first stage is low and it can be switched with high switching frequency to improve the power density. The second stage can be switched with lower switching frequency to reduce the switching losses. However, this topology requires two sets of switching circuits, control circuits and power devices, which makes it complex and expensive. The two switch of cascaded boost converter can be integrated to reduce complexity of this topology as shown in Fig. 1.5(b) [9]. The voltage gain of this configuration can be given by

$$\frac{V_0}{V_{in}} = \frac{1}{(1-D)^2} \tag{1.2}$$

1.2.1.5 Switched inductor based converters

Figure 1.6(a) shows the switched inductor based boost converter [10].

The voltage gain of this configuration can be given by

$$\frac{V_0}{V_{in}} = \frac{1+D}{1-D} \tag{1.3}$$

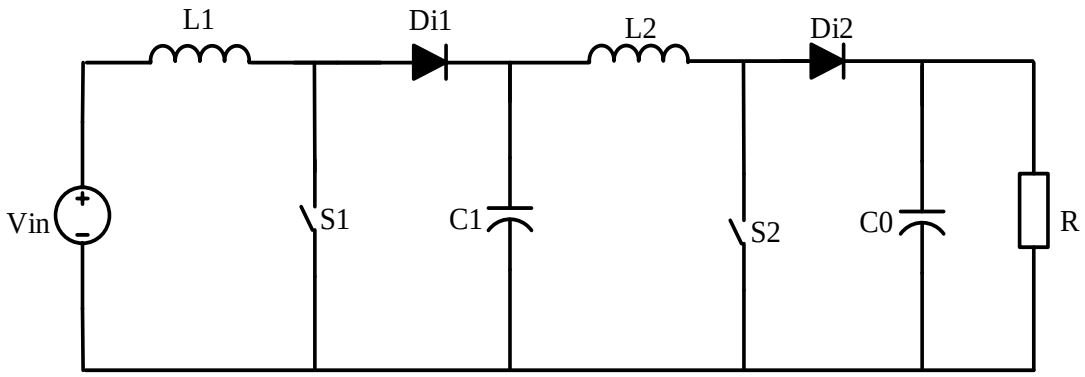


Fig. 1.5(a): Cascaded boost converter.

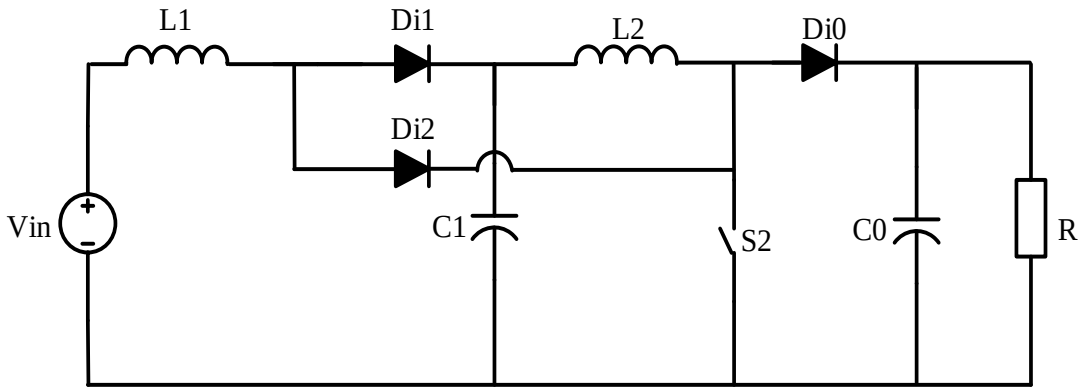


Fig. 1.5(b): Quadratic boost converter.

Voltage gain of this converter is higher than conventional boost converter but not much suitable for high voltage gain applications. Switch voltage stress is also high in this converter. Figure 1.6(b) shows another example of switched inductor based converter [10], and the voltage gain of this converter can be given by

$$\frac{V_0}{V_{in}} = \frac{1+3D}{1-D} \qquad (1.4)$$

1.2.1.6 Coupled inductor based converters

A coupled inductor can serve as a transformer that is used to enhance the voltage gain in non-isolated step-up converters [11].

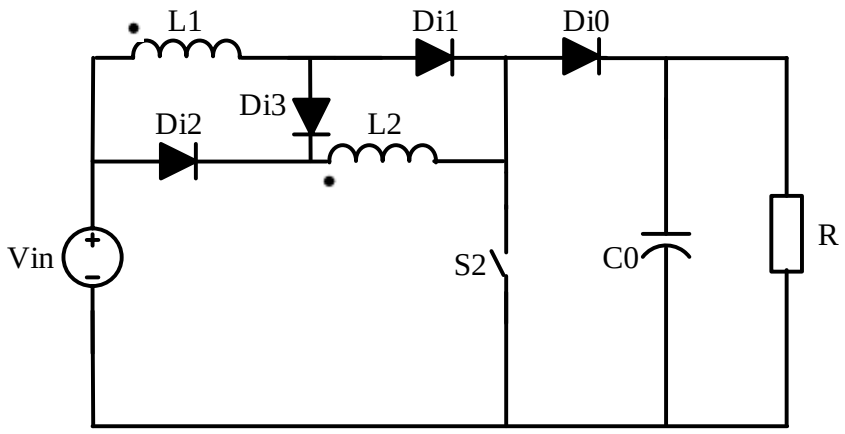


Fig. 1.6(a): Switched-inductor boost converter.

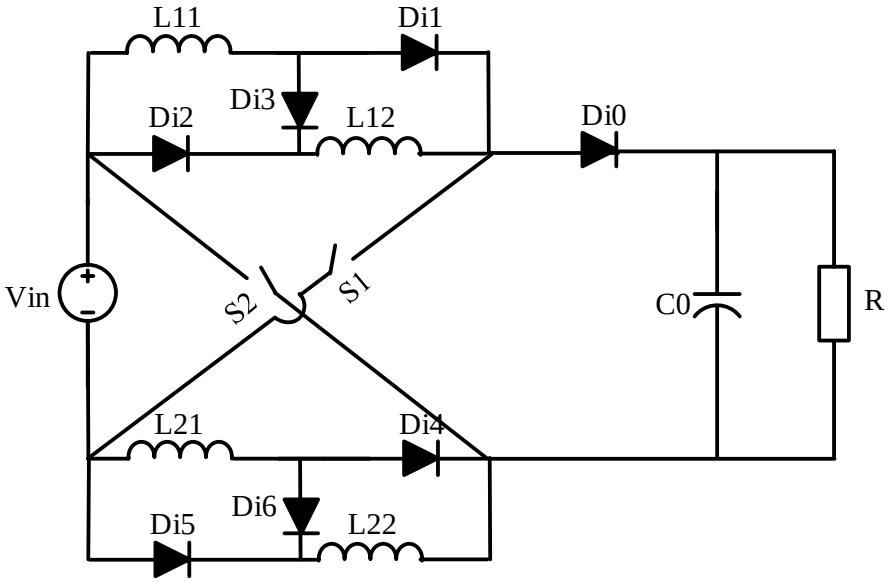


Fig. 1.6(b): Switched-inductor with active network circuit converter.

Figure 1.7(a) shows a coupled inductor based high step-up converter. The voltage gain of coupled inductor based converter can be extended by proper design of turns ratio. A high step-up flyback-boost converter is derived by combining the conventional boost with flyback converter. Figure 1.7(b) shows coupled inductor based flyback-boost converter. The voltage gain of ideal converter for this configuration can be given by

$$\frac{V_0}{V_{in}} = \frac{1+nD}{1-D} \qquad (1.5)$$

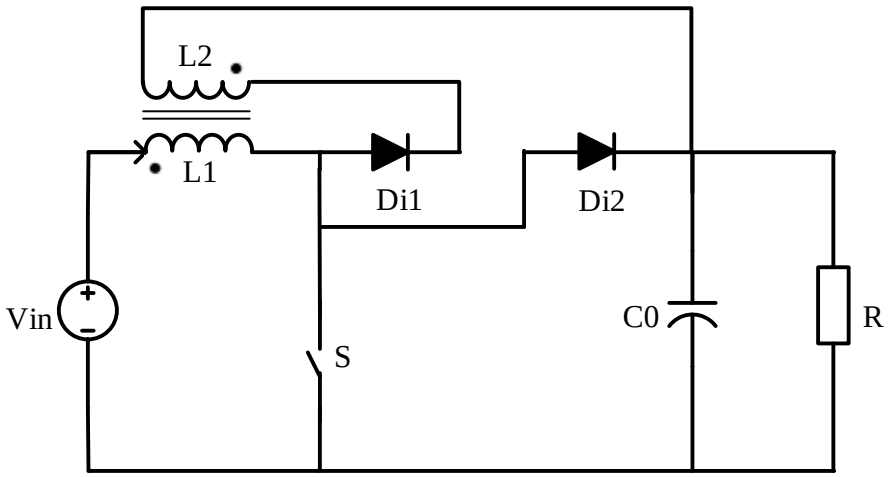


Fig. 1.7(a): Coupled-inductor high step-up converter.

Where **n** is turns ratio. In literature many variations are reported based upon combination of flyback and boost converter [12]. The advantages of coupled inductor based topologies are high gain and reduction in size of converter due to common magnetic core. The converters reported in [13], [14], [15] and [16] also uses coupled inductors to achieve high step-up ratio. However, the leakage energy induces high voltage stress and increased switching losses and also create EMI problem. An active clamp circuit can be used to minimize these problems in coupled inductor based converters.

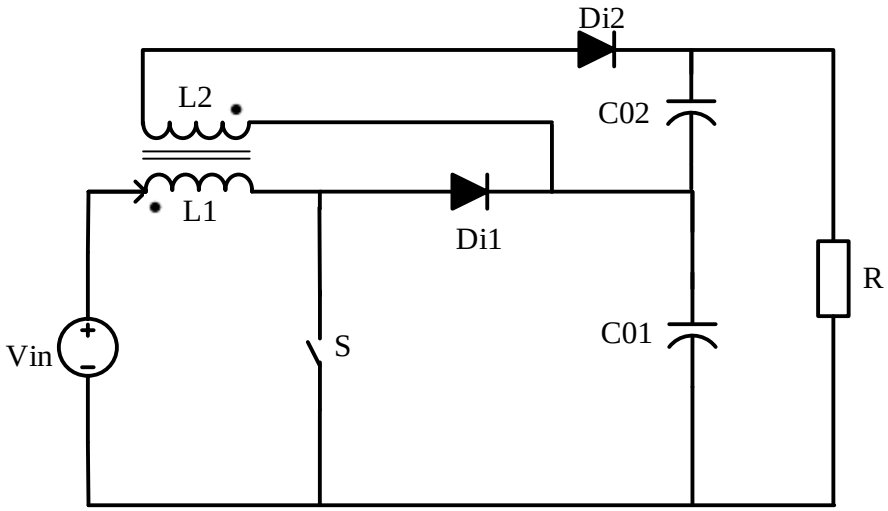


Fig. 1.7(b): High step-up flyback-boost converter using coupled inductor.

1.2.1.7 Switched capacitor based converters

Converters based upon switched capacitors can give high voltage gain depending upon number of capacitors used [17]. Figure 1.8(a) shows switched capacitor high step-up converter.

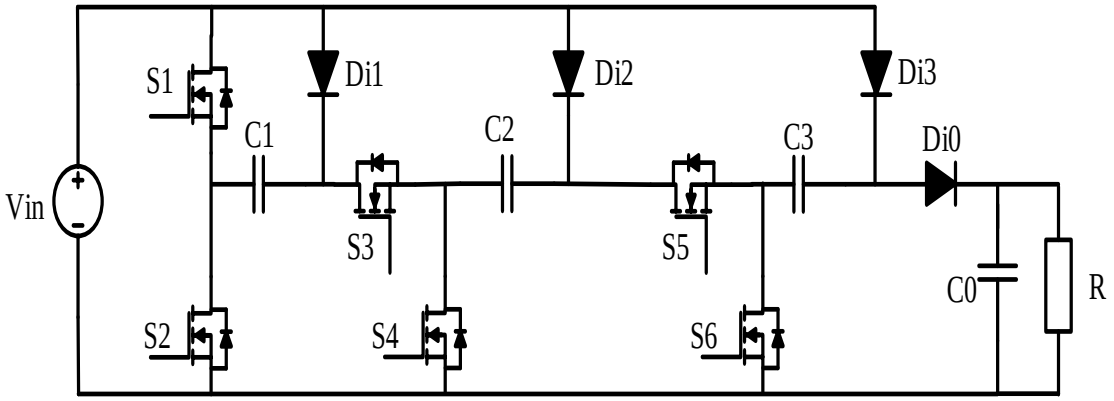


Fig. 1.8(a): High step-up converter with switched capacitor.

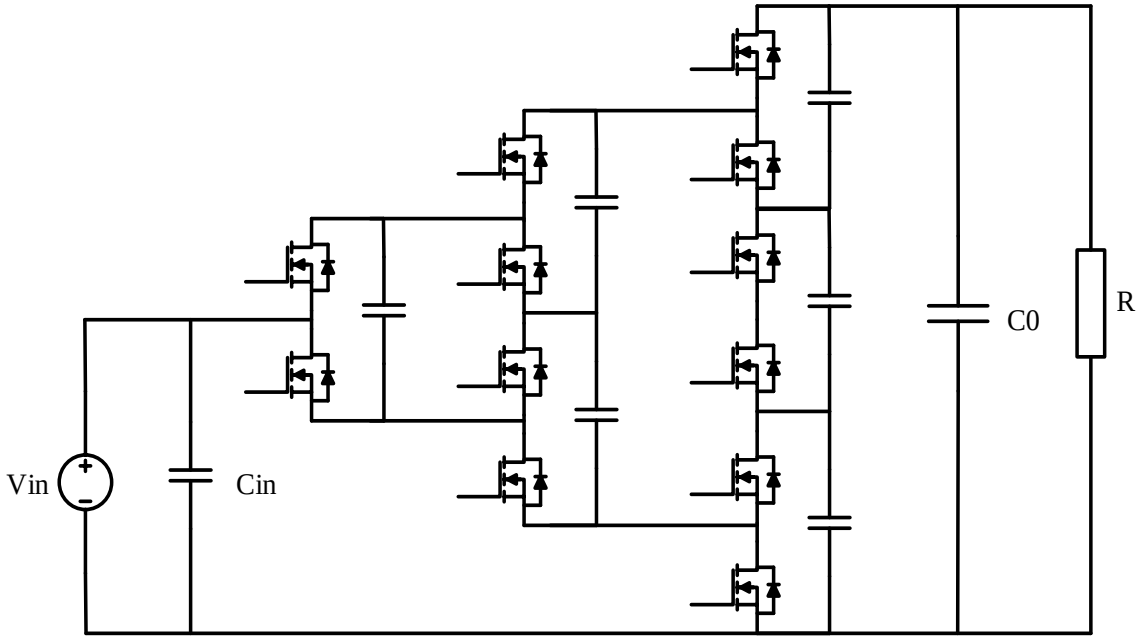


Fig. 1.8(b): High step-up converter with multilevel cell.

Another variation of switched capacitor converter is hybrid switched capacitor converter as shown in Fig. 1.8(b), which uses capacitor diode multiplier cell to increase reliability and efficiency of the converter. The converters reported in [18], [19] and [20] also used switched capacitors for high voltage gain.

The converters based upon switched capacitor do not require magnetic components such as inductors and transformers due to which size, cost and weight of converter is reduced. However, number of switches is high, which increases converter complexity and cost. The main disadvantages of switched capacitor based converters are (i) pulsating input current, (ii) voltage regulation is poor and difficult and (iii) the voltage gain is usually predetermined by the converter structure.

1.2.1.8 Switched capacitor and inductor based converters

The switched capacitor based converter can be integrate with boost converter to get step less voltage gain [21]. Figure 1.9(a) shows an example of this type of converter. This converter can provide high gain with lower duty ratio but it suffers from pulsating output current. Another family of single switch high step-up dc-dc converter is introduced in [22], Fig. 1.9(b) shows an example of this family. The voltage gain of converter shown in Fig. 1.9(b) is given by

$$\frac{V_0}{V_{in}} = \frac{1+D}{1-D} \qquad (1.6)$$

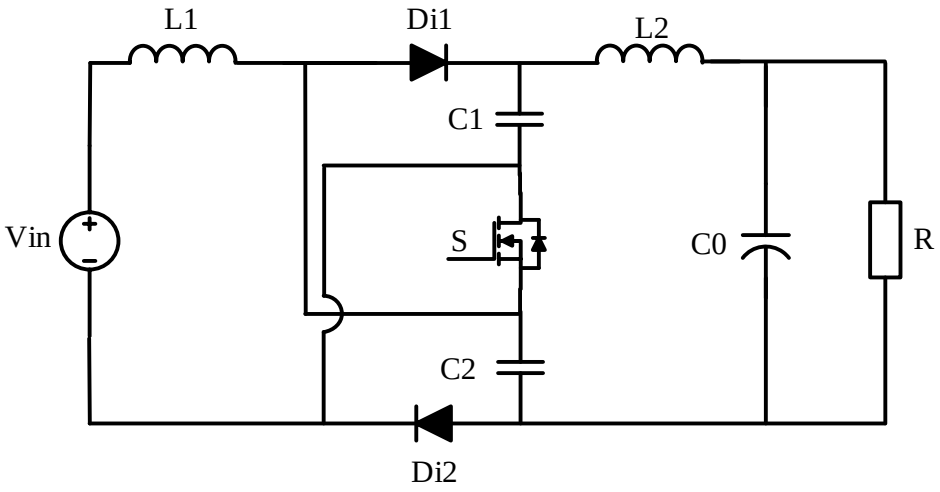


Fig. 1.9(a): High step-up converter presented in [21].

1.2.1.9 Coupled inductor and switched capacitor based converter

The concept of coupled inductor and switched capacitor can be integrate to derive high voltage gain converters [23]. Figure 1.10(a) shows an example of such combination of converter [24]. The reverse recovery problem of output diode is alleviated by leakage inductance of coupled inductor.

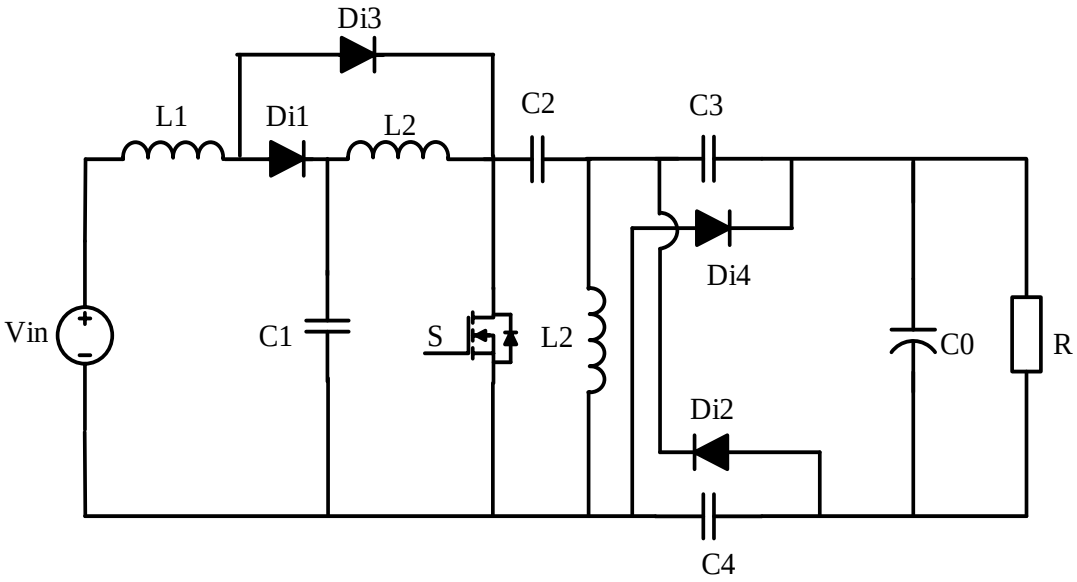


Fig. 1.9(b): High step-up converter presented in [22] .

The voltage gain of converter shown in Fig. 1.10(a) can be given for coupling coefficient equal to one by

$$\frac{V_0}{V_{in}} = \frac{1+2n+nD}{1-D} \qquad (1.7)$$

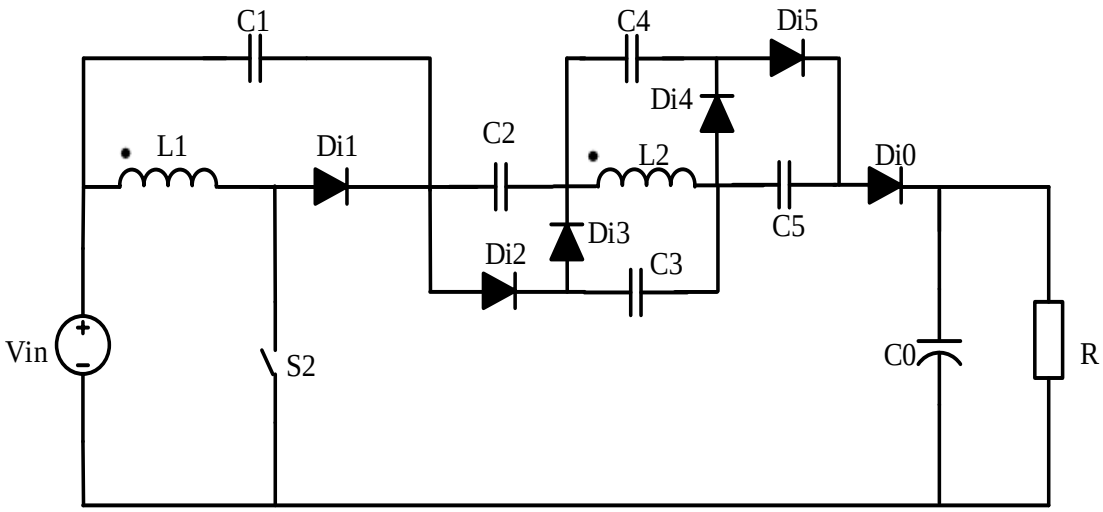


Fig. 1.10(a): High step-up converter presented in **[24]**.

Another example of this combination is as shown in Fig. 1.10(b) [25] and the voltage gain of this configuration can be given by

$$\frac{V_0}{V_{in}} = \frac{1+(1+D)n}{1-D} \tag{1.8}$$

The main features of this converter are (i) large step-up conversion ratio, (ii) less voltage stress on switch and (iii) recycling of leakage energy of coupled inductor.

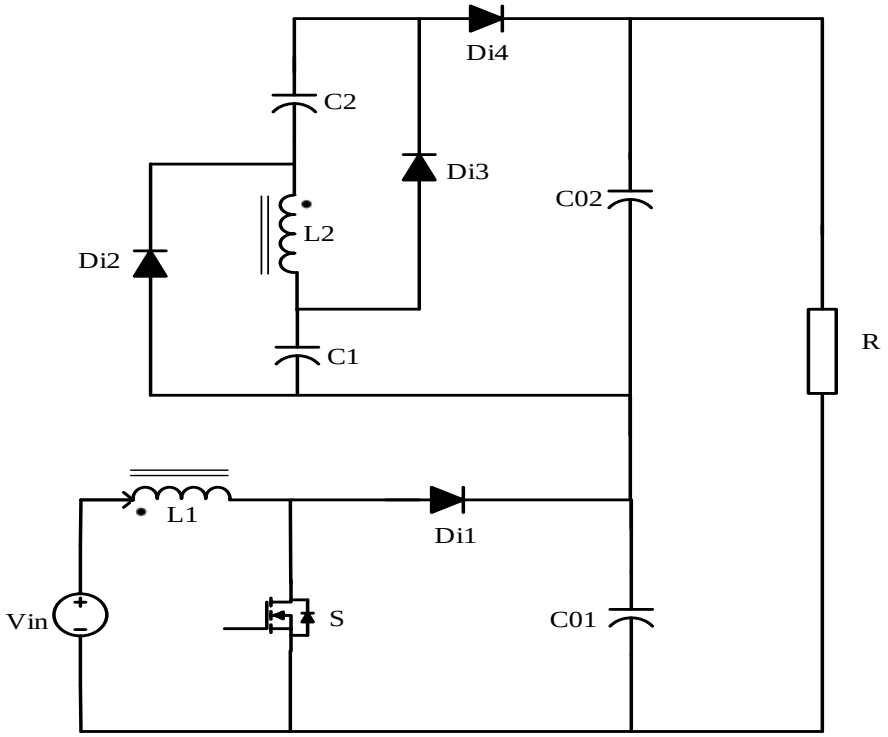


Fig. 1.10(b): High step-up converter presented in [25].

1.2.1.10 Z-source (ZS)/quasi Z-source (QZS) based converters

Z-source converter is comparatively new topology [26]. The Z-source based converters can be used for high step-up applications [3], [27]. Figure 1.11(a) shows Z-source based PWM DC-DC converter [28]. The voltage gain of the converter shown in Fig. 1.11(a) is given by

$$\frac{V_0}{V_{in}} = \frac{1-D}{1-2D} \tag{1.9}$$

Compared to conventional boost converter, the PWM Z-source converter has desirable features for high step-up applications such as (i) higher voltage gain for

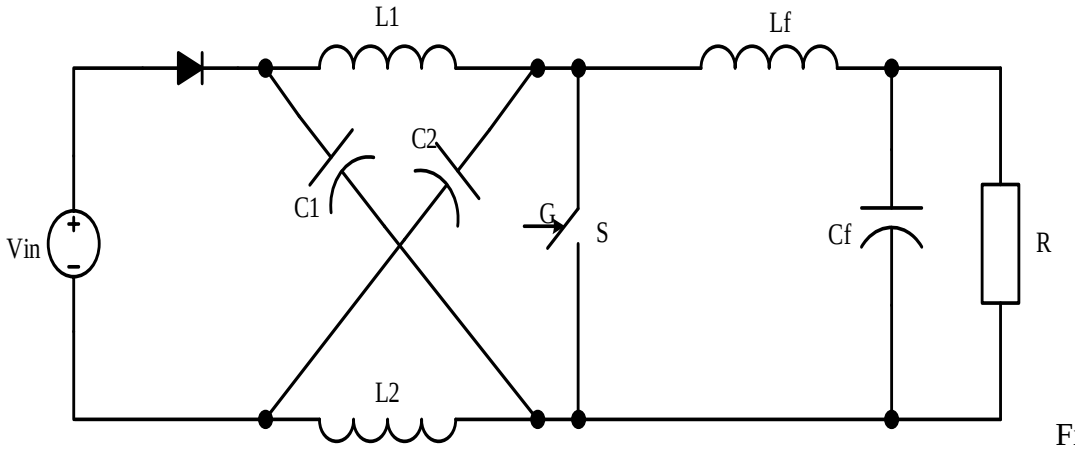


Fig. 1.11(a): Z-source DC-DC converter.

same duty ratio, (ii) it isolates source from load in case of a short circuit at load side. Limitations of this converter are discontinuous input current and floating switch.

The QZS converter has been proposed as a new converter topology based on Z-source inverter topology. Figure 1.11(b) shows QZS based DC-DC converter [29], which inherits all the advantages of ZSC and has several more advantages such as reduced passive component rating and common ground for source load and switch. The voltage gain of this converter is same as ZS based converter [28], as given by (1.9).

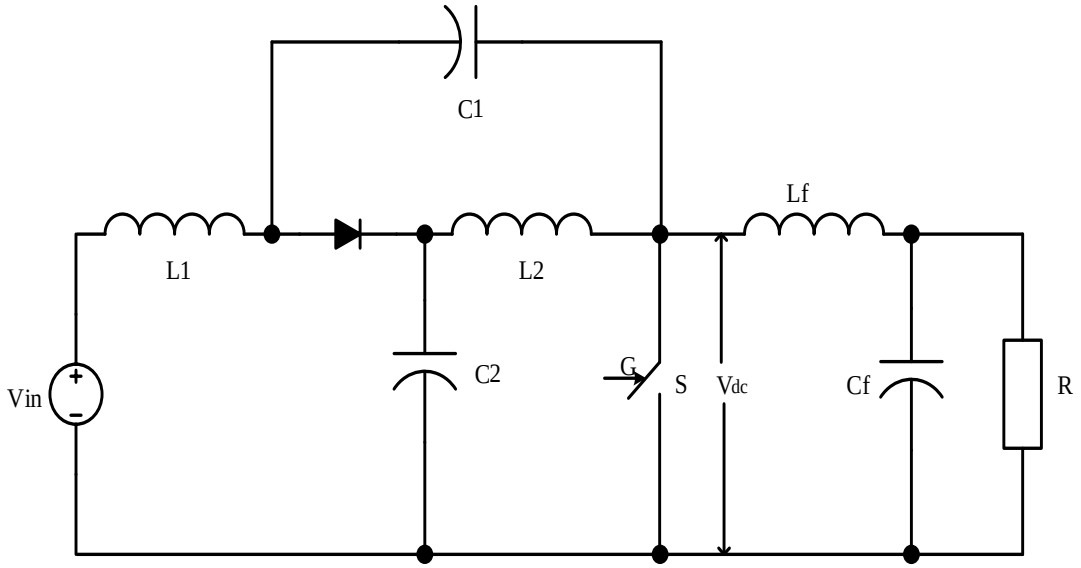


Fig. 1.11(b): Quasi Z-source DC-DC converter.

1.2.2 Isolated converter topologies

In some countries galvanic isolation of PV energy source is necessary as per their electrical regulations and standards. In view of their requirement many isolated topologies are reported in literature [30]. The electrical isolation can be provided by transformer either at line frequency or at high frequency. Transformer at line frequency is not often used because of its size, weight and high price.

1.2.2.1 Basic isolated step-up converter topologies

A number of isolated step-up converter configurations are known, and some of these are briefly given here. Figure 1.12(a) shows full-bridge topology of isolated step-up converter. In this configuration voltage gain is transformation ratio times of boost converter as given by equation (1.10), and when turn ratio is one voltage gain is same as boost converter.

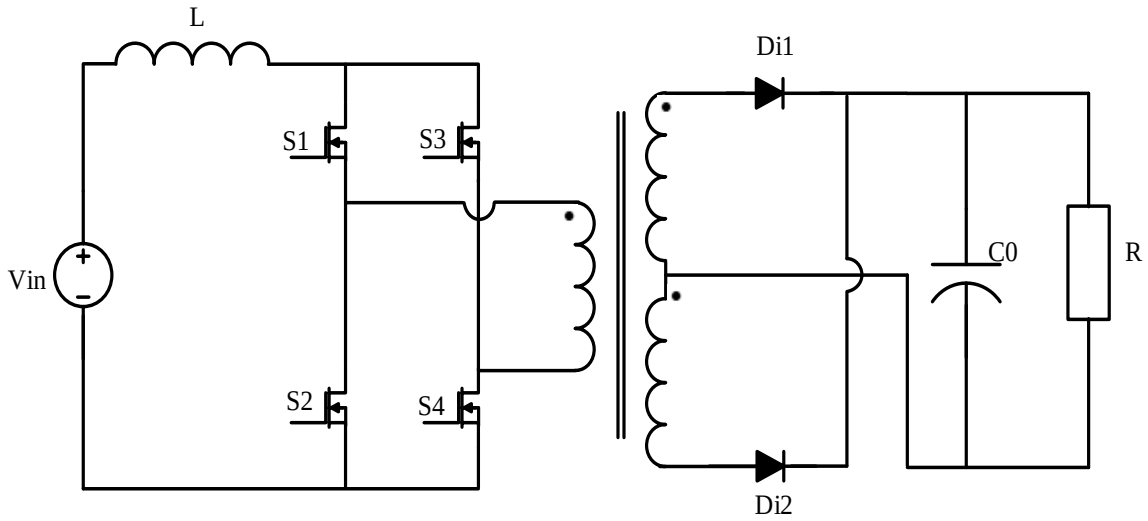


Fig. 1.12(a): Full-bridge isolated step-up converter.

$$\frac{V_0}{V_{in}} = \frac{n}{1-D} \qquad (1.10)$$

An isolated converter based on push-pull configuration is depicted in Fig. 1.12(b) [31]. In comparison with isolated full bridge boost topology it requires only two active switches. However the voltage rating of switches are higher than isolated full bridge boost topology. Operation is otherwise similar to isolated full bridge boost converter.

Figure 1.12(c) shows active clamp step-up DC-DC converter. This isolated converter configuration has the advantages of both flyback and forward converter. This topology uses active clamp circuit in both duration of switching operation so the input power is delivered to output in both switch-ON and switch-OFF duration.

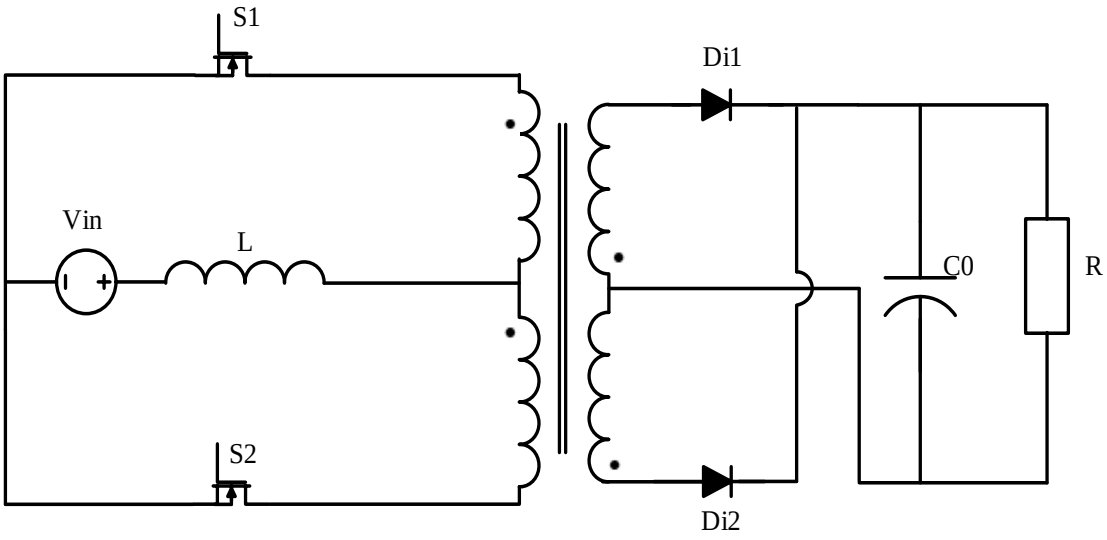


Fig. 1.12(b): Isolated step-up converter based on push-pull configuration.

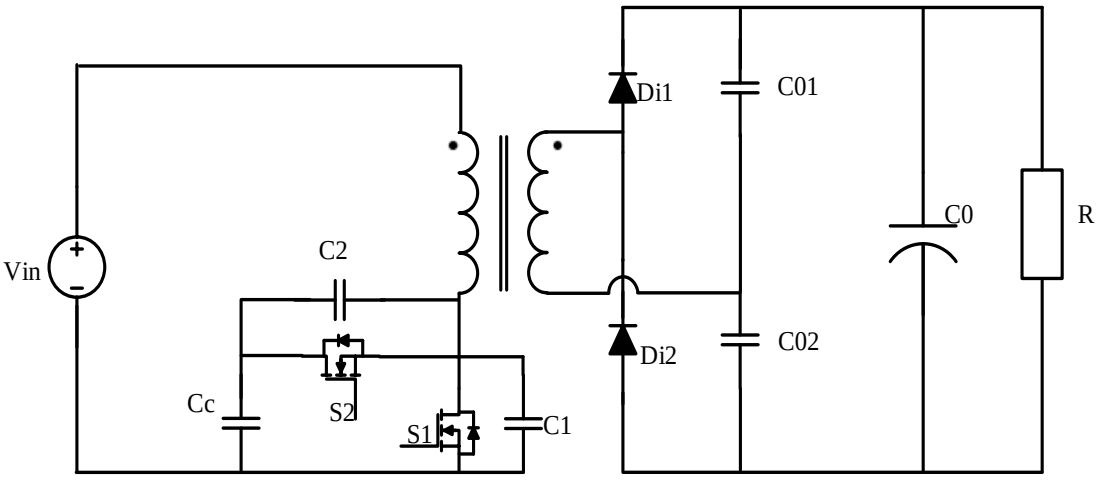


Fig. 1.12(c): Active clamp isolated step-up converter.

In this configuration voltage doubler circuit is used with secondary side of transformer. In primary side capacitors are used in parallel with diode to eliminate reverse recovery losses of diode.

The voltage gain of this configuration can be given as

$$\frac{V_0}{V_{in}} = \frac{2nD}{1-D} \qquad (1.11)$$

1.2.2.2 Isolated resonant converters

Resonant soft-switching techniques can be incorporate with converters to achieve higher efficiency operation. In these converters only conduction losses are dominates as switching losses are negligible.

Figure 1.13(a) shows half bridge resonant converter [32]. The zero current switch (ZCS) condition is achieved by connecting appropriate value of capacitor Cr in series with transformer to form resonant tank with transformer leakage inductance.

The zero voltage switch (ZVS) condition based converter [33] is shown in Fig. 1.13(b). During switch-OFF capacitor C1 and C2 resonates with inductor Lr thus zero voltage switch-OFF is achieved. Switch-ON occurs when voltage across capacitor is zero.

In literature many other soft-switching based isolated converter configurations such as resonant push-pull converter [34], current fed multi-resonant converter [35] and series parallel resonant converters [36] are also reported for high step-up operation.

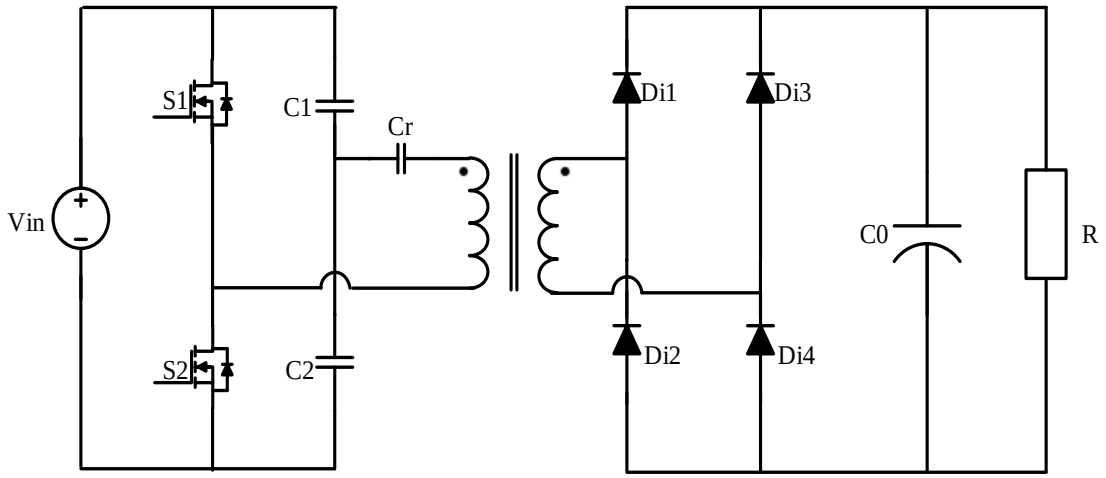


Fig. 1.13(a): Half-bridge resonant converter.

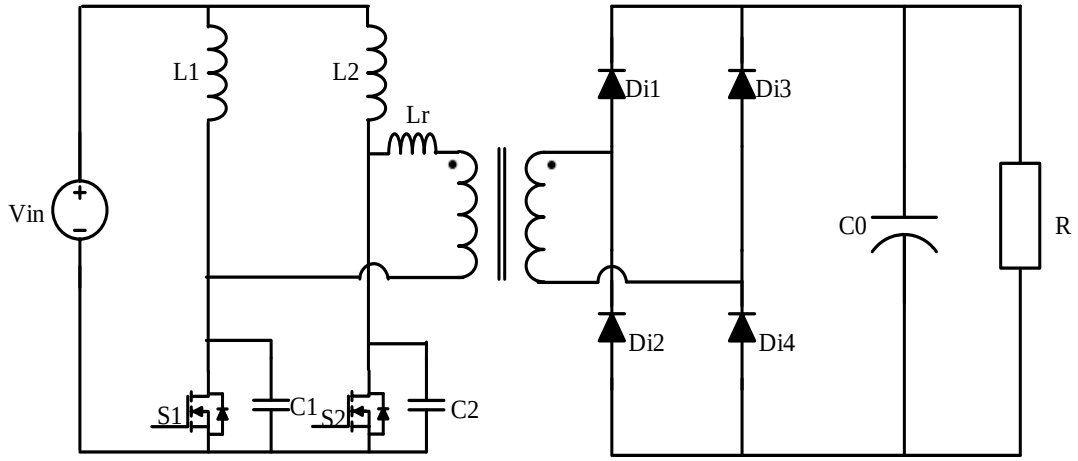


Fig. 1.13(b): Resonant half-bridge dual converter.

1.2.2.3 Z-source/quasi Z-source based isolated converters

Z-source based another topology was proposed in [37], which utilized coupled inductor for higher boost and load is isolated from the source. Figure 1.14(a) shows isolated DC-DC converter based upon Z-source topology. The voltage gain of this configuration can be given as

$$\frac{V_0}{V_{in}} = 2nk\frac{1-D}{1-2D} \qquad (1.12)$$

Where **n** is turns ratio and **k** is coupling coefficient.

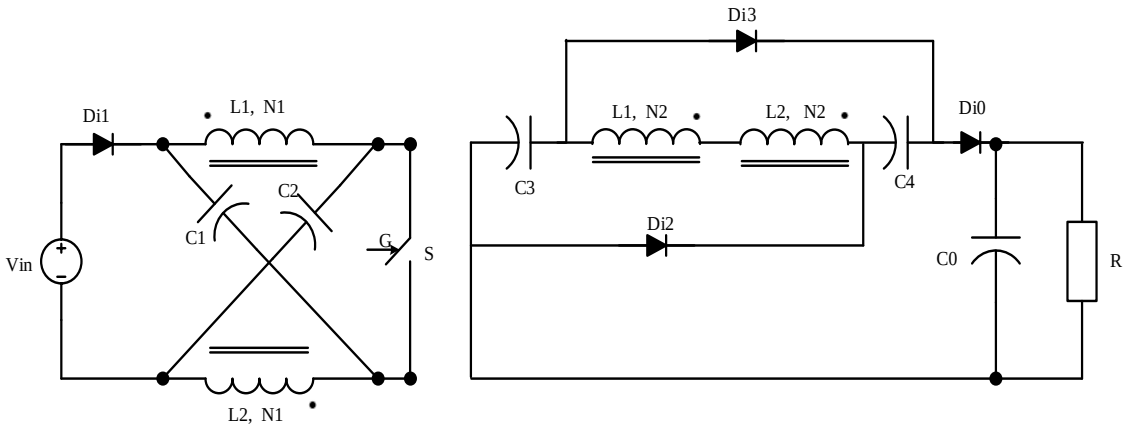


Fig. 1.14(a): Z-source isolated DC-DC converter.

The main features of this converter are (i) low turns ratio of coupled inductor, (ii) the leakage inductor energy does not create voltage stress over active switch or diode, (iii) switch voltage rating is low and (iv) isolation exists between input and output. The main limitation of this topology is the reverse recovery problem, which is alleviated due to secondary leakage inductance.

In [38] QZS based isolated DC-DC converter was proposed, which is similar to ZSC based isolated DC-DC converter. Figure 1.14(b) shows circuit of QZS based isolated DC-DC converter, it also utilize coupled inductors for isolation and to obtain high gain. The voltage gain of the converter shown in Fig. 1.14(b) can be given by

$$\frac{V_0}{V_{in}} = nk\frac{1-D}{1-2D} \tag{1.13}$$

The main features of this topology are (i) continuous input current, (ii) low turn ratio of coupled inductor, (iii) isolation exists between input and output, (iv) low voltage rating of switch and (v) leakage energy does not create stress on the active switch and diode.

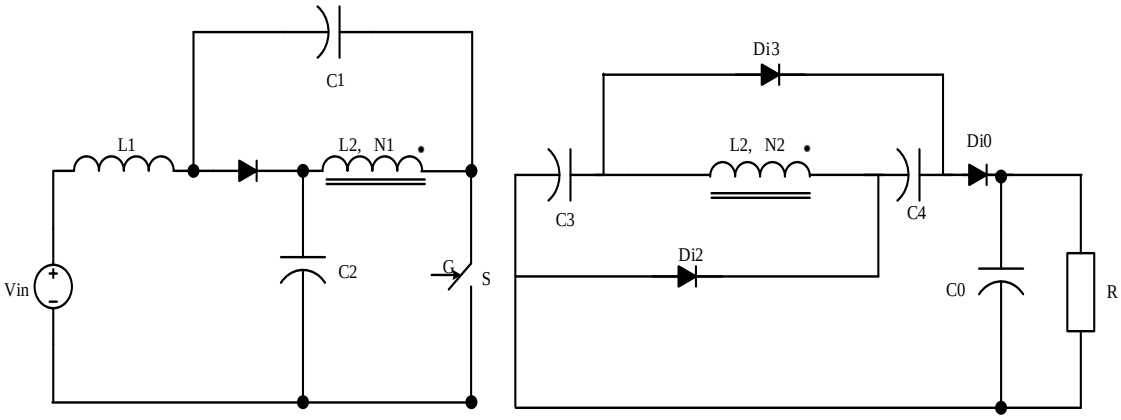


Fig. 1.14(b): Quasi Z-source isolated DC-DC converter.

Figure 1.14(c) shows QZS based isolated converter [3]. This configuration contains QZS inverter, high frequency step-up transformer and voltage doubler rectifier. This topology can be used for providing stabilized output voltage with galvanic isolation for widely varying input voltage. The voltage gain of converter shown in Fig. 1.14(c) is given by

$$\frac{V_0}{V_{in}} = \frac{2n}{(1-2D)} \tag{1.14}$$

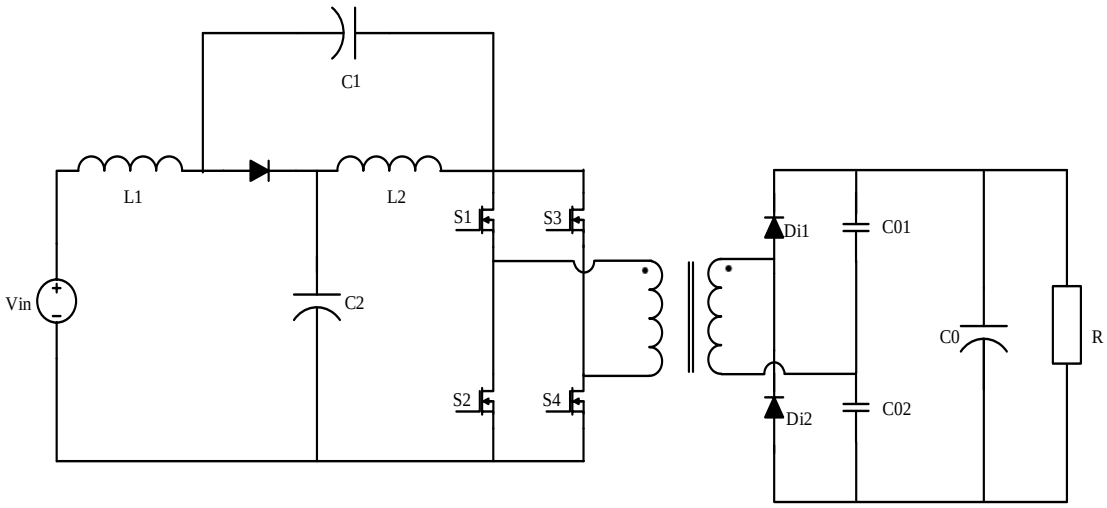


Fig. 1.14(c): QZSI based isolated high step-up DC-DC converter.

Cascaded QZS network based high step-up converter is proposed in [27]. Cascaded network decreases duty ratio required for high step-up operation. Low duty ratio operation reduces the required value of capacitor and inductor. As shown in Fig. 1.14(d) the secondary side of high frequency transformer is voltage doubler rectifier, same as given in [3] . The voltage gain of converter shown in Fig. 1.14(d) is given by

$$\frac{V_0}{V_{in}} = \frac{2n}{(1-3D)} \qquad (1.15)$$

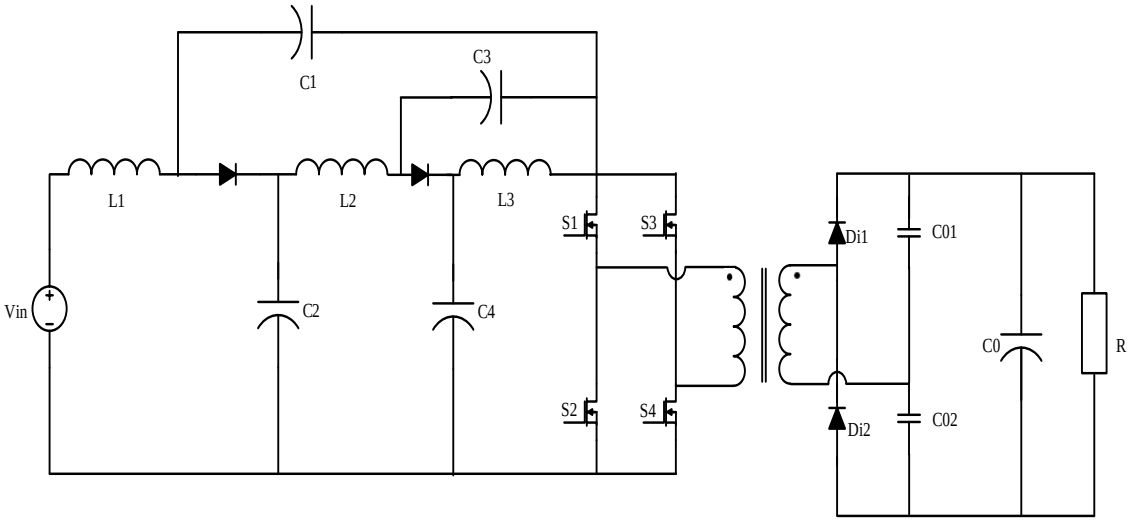


Fig. 1.14(d): Cascaded QZS network based high step-up converter.

QZS push-pull based isolated high step-up DC-DC converter is proposed in [39] as shown in Fig. 1.14(e). The voltage gain of this configuration is given by

$$\frac{V_0}{V_{in}} = \frac{2n}{3-4D} \tag{1.16}$$

This configuration provides wide voltage gain with small duty ratio and small turn ratio of isolation transformer. Hence conduction losses of switches and transformer is less in comparison with other configuration of same origin isolated configuration.

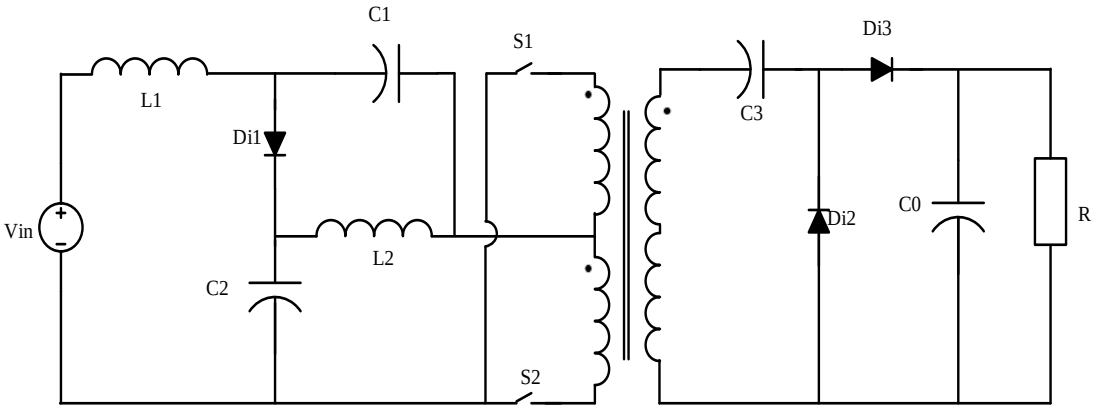


Fig. 1.14(e): QZS push-pull based high step-up converter.

In summary, in non-isolated topologies, high conversion ratio is mainly achieved by using cascading, coupled-inductor, switched-capacitor and switched-inductor techniques or any combination of these techniques. In all the isolated topologies either line frequency or high frequency transformer is used for galvanic isolation. Transformer not only provides isolation but it also step-up input voltage due to turn ratio and transformer working principal.

1.3 Scope and objectives of thesis

It can be observed from the existing literature that non-isolated step up converters can reduce cost and improve efficiency for certain power levels and wherever there are no stringent requirement of isolation [1]. Therefore, many new non-isolated step up converter topologies are being proposed in the literature.

Z-source converter is one of the recently proposed converter topologies for DC-AC operation but it is also quite useful for DC-DC converter. In literature, few DC-DC converter configurations are available based on ZS or QZS networks which are

mainly isolated converters. It can be seen from the previous studies that ZS and QZS based DC-DC converters are also potential candidates for step-up applications. However, some of the non-isolated topologies are not well explored which are based on QZS converter. Further, some non-isolated topologies also can be developed which are based on these converters.

On the similar note, quadratic boost converters are well known for getting high step up ratios. Therefore, it will be interesting to investigate this topology for the development of new step-up converter topologies.

This thesis mainly focuses on study and development of various non-isolated converters based on QZS DC-DC converter and quadratic boost converter, which are of interest for high step-up applications.

The objectives of thesis are

- To analyze and control DC-DC converter based on ZS and QZS converter.
- To develop variations of QZS based DC-DC converters to achieve higher boost at low duty ratio.
- To develop a QZS based DC-DC converter to achieve minimum input current ripple.
- Development of tapped inductor based quadratic boost converters.

1.4 Contribution of thesis

In this thesis six converter configurations are introduced. Four configurations are based upon quasi Z-source network and two configurations are based upon quadratic boost converter using tapped-inductor. The steady state analysis and design guidelines are presented for these converters.

The first converter studied is QZS based DC-DC fourth order converter. The converter performance and control technique is explored in detail. The gain of this converter is same as the converter in [28], the advantage is with less number of components. Advantages of this converter are continuous input current, common ground for source, load and switch.

The second converter is a tapped-inductor variation of the first converter. The voltage gain of this converter is enhanced by using tapped inductor.

The coupled inductor variation of the first converter is also presented where coupled inductor is used to reduce the ripple in input current. The effect of coupling coefficient

on current ripple is studied in detail. In the coupled-inductor based topology, reduction in size and weight of converter can be achieved because of utilizing the same core for both the inductors.

Fourth converter is a high step-up non-isolated dc-dc converter which is derived from quasi Z-source converter and a boost converter. Compared to QZS and boost converters, it gives higher gain at a lower duty ratio.

Two converters which integrate the step-up capabilities of the quadratic boost converter and the tapped-inductor based converter are proposed in the sixth chapter. These proposed converters also have an advantage of low voltage stress on active switch.

Further One Cycle Control technique is used for the voltage control of conventional ZS and QZS DC-DC converters along with fourth order QZS-based converter. Either capacitor voltage or output voltage can be controlled by using this method. It gives fast dynamic response, excellent reference tracking and input disturbance rejection.

1.5 Organization of thesis

The work presented in this thesis is organized as follows.

Chapter 2: Detailed steady state and dynamic analysis of the fourth order QZS based converter is presented. Boundary condition between continuous conduction mode and discontinuous conduction mode is derived. Expressions for power loss in components are derived. Average current mode control based closed loop controller design is also presented. Simulation and experimental results are presented to substantiate the theoretical analysis.

Chapter 3: Tapped-inductor and coupled-inductor based fourth order QZS based converter topologies are proposed in this chapter. Steady state analysis of both the topologies is presented. Simulation and experimental results are reported.

Chapter 4: One cycle control operation of conventional ZS and QZS based converters are presented. Conditions are derived for changing controlled variable such as DC link voltage and intermediate capacitor voltage. Simulation and experimental results are demonstrated to verify the theoretical analysis.

Chapter 5: A high step-up converter based on QZS converter and boost converter is proposed. Steady state analysis and small signal model of converter is presented. Boundary condition for continuous conduction mode and discontinuous conduction

mode is derived. Closed loop controller design is presented. Simulation and experimental results for closed loop control and open loop operation are demonstrated.

Chapter 6: presents two new topologies based on quadratic boost converter topology. These converter uses tapped-inductor to achieve high voltage gain. Advantages of these topologies and operation are explained. Voltage gain and efficiency variation with different load and duty ratio is reported. Results are presented for different combination of turn ratio.

Chapter 7: Thesis is concluded in this chapter and future scope of work is discussed.

Chapter 2

A Fourth Order PWM DC-DC Boost Converter derived from Quasi Z-Source Topology

2.1 Introduction

In applications like DC-AC conversion where voltage boost is obtained in a single stage, Z-source converter is a well-known converter topology. It uses an impedance network to couple the power source with converter main circuit [26]. In this topology, controlling of shoot-through state enables to control boost feature of converter with improved reliability. Further, its many variations like quasi Z-source inverter [40], series Z-source inverter [41], and Trans Z-source inverter [42] are present in the literature. In most of the currently available Z-source converter related literature, researchers have focused on DC-AC operation of Z-source converter and shoot through control techniques. Recently, in few publications authors have used Z-source converter for DC-DC mode of operation [28], [29] , [43]. In [28] detailed steady state analysis of PWM Z-source DC-DC converter in CCM and effect of non-idealities on converter performance has been presented. Small-signal modeling by circuit-averaging technique of Z-source DC-DC converter in CCM mode is given in [43] .Control for quasi Z-source dc-dc converter is proposed in [29]. Quasi-Z source inverter based isolated DC-DC converter is proposed in [3].

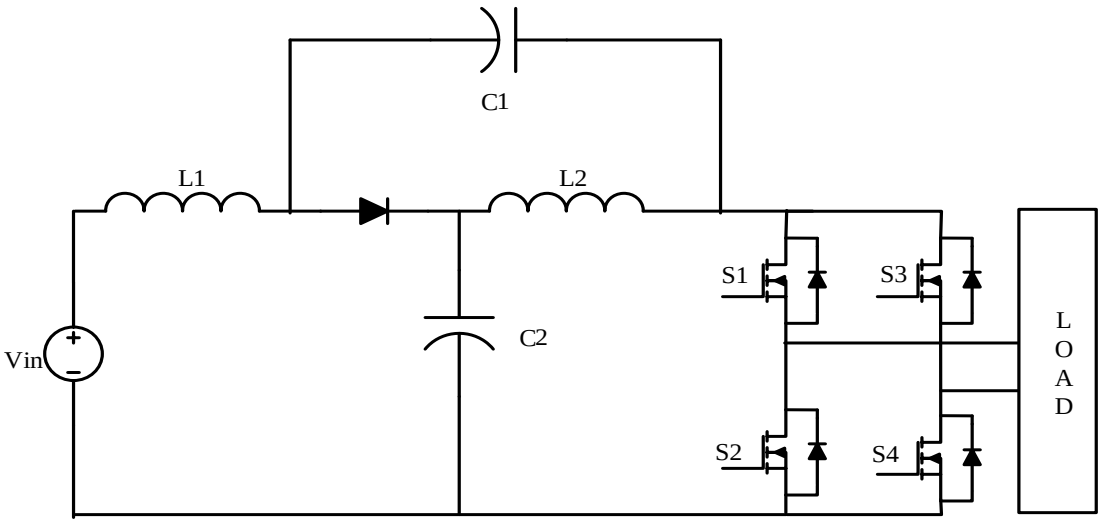


Fig. 2.1: Single phase Quasi Z-source inverter.

Figure 2.1 shows a single phase voltage fed quasi Z-source inverter. If four switches are replaced by one switch and circuit is rearranged as shown in Fig. 2.2, it results in a DC-DC converter configuration. This configuration can be called as fourth order step-up PWM DC-DC converter because of four dynamic elements and it is a hard switching converter.

The advantages of this converter in comparison with other Z-source based DC-DC converters [28] are reduced number of components for same output voltage, reduced voltage stress on one capacitor, continuous input current, lower inrush current and common ground for source, load and switch. In comparison of Quasi Z-source DC-DC converter as in [29], it has reduced number of components for the same gain.

These features lead to a possibility that it might be a potential topology for renewable energy applications. Its thorough investigation is still not reported in the literature.

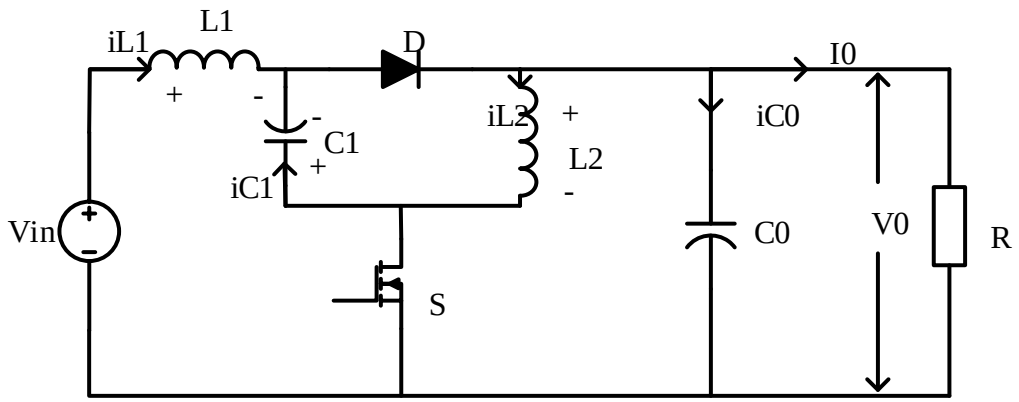


Fig. 2.2: Fourth order step-up converter.

In this chapter, a detailed steady state analysis, dynamic analysis and controller design has been presented for a fourth order step up converter. The objectives of this chapter are 1) to present equivalent circuits and associated expressions corresponding to different stages of operation in CCM and DCM, 2) to obtain the dc voltage transfer ratio along with the effect of parasitic resistances, 3) to obtain power loss in different components and overall efficiency, 4) to present a dynamic model and associated controller design, 5) To validate the theoretical results with simulation and experimental results.

The chapter is organized as follows. Section 2.2 presents the equivalent circuit in CCM and related idealized waveforms. Relevant expressions are derived from these waveforms. Section 2.3 presents boundary condition between CCM and DCM.

Further the analysis is extended for DCM operation of converter. Section 2.4 presents power loss analysis and overall efficiency expressions. Small-signal model and controller design for converter are presented in section 2.5. Simulation and experimental results are presented in section 2.6. Conclusions are presented in section 2.7.

2.2 Idealized circuit analyses

The steady state analysis is based on following assumptions

1. All components are ideal and all resistors, capacitors and inductors are linear time invariant.
2. C_1 and C_0 are large enough so that voltages across them can be treated as constant.
3. Natural time constant of converter is much higher than the one switching time period.

Referring to Fig. 2.2, the switch S is operating at switching frequency $f_S=1/T$ with the duty ratio $D=T_{on}/T$. where T_{on} is the duration for which switch S is ON. Figures 2.3(a) and Fig. 2.3(b) shows circuit during switch ON and switch OFF condition. Figure 2.4(a) and Fig. 2.4(b) shows idealized current and voltage waveforms for CCM. The slopes of different currents are also shown in Fig. 2.4(a).

2.2.1 For time interval $0 \leq t \leq DT$

For this duration, equivalent circuit of the converter is as shown in Fig. 2.3(a).

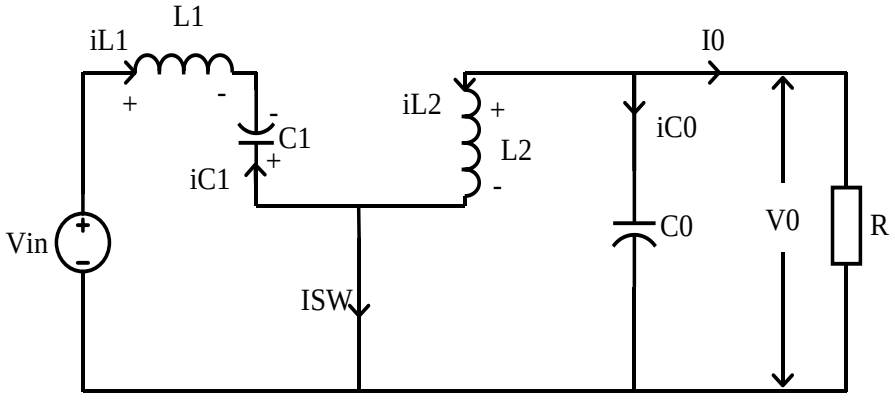


Fig. 2.3(a): Equivalent circuit of converter when S is ON.

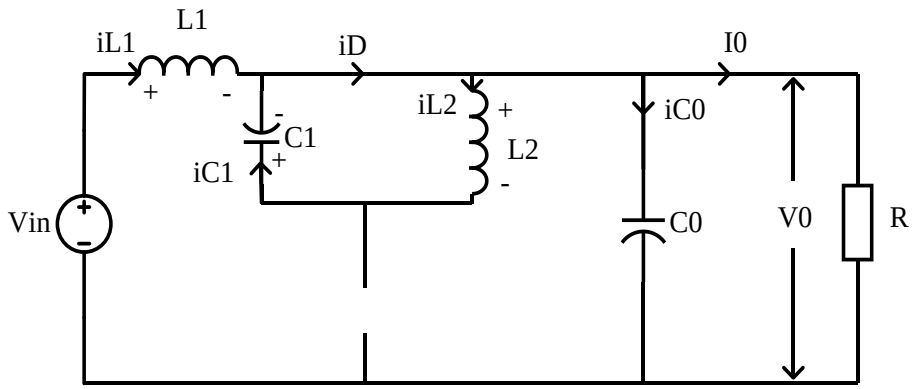


Fig. 2.3(b): Equivalent circuit of converter when S is OFF for CCM.

In this duration the main switch S is ON and diode is OFF. Diode is OFF due to reverse bias voltage (V_0+V_{C1}). For ideal components, voltage across switch S and current through diode are zero.

Here voltage across inductor L_1 is (V_{in}+V_{C1}) and voltage across L_2 is equal to output voltage V_0. The current through inductor L_1 and inductor L_2 are

$$i_{L1}(t) = \left(\frac{V_{in} + V_{C1}}{L_1}\right)t + i_{L1}(0) \tag{2.1}$$

$$i_{L2}(t) = \frac{V_0}{L_2}t + i_{L2}(0) \tag{2.2}$$

The current through the switch S is sum of both inductor current and is given by

$$i_S(t) = i_{L1}(t) + i_{L2}(t) = \left(\frac{V_{in} + V_{C1}}{L_1}\right)t + \left(\frac{V_0}{L_2}\right)t + i_{L1}(0) + i_{L2}(0) \tag{2.3}$$

From equation (2.1) and (2.2), the peak inductor currents which occurs at time t = DT are given as

$$i_{L1}(DT) = \left(\frac{V_{in} + V_{C1}}{L_1}\right)DT + i_{L1}(0) \tag{2.4}$$

$$i_{L2}(DT) = \frac{V_0}{L_2}DT + i_{L2}(0) \tag{2.5}$$

Peak to peak inductors current are expressed as

$$\Delta i_{L1} = i_{L1}(DT) - i_{L1}(0) = \left(\frac{V_{in} + V_{C1}}{L_1}\right) DT \tag{2.6}$$

$$\Delta i_{L2} = i_{L2}(DT) - i_{L2}(0) = \frac{V_0}{L_2} DT \tag{2.7}$$

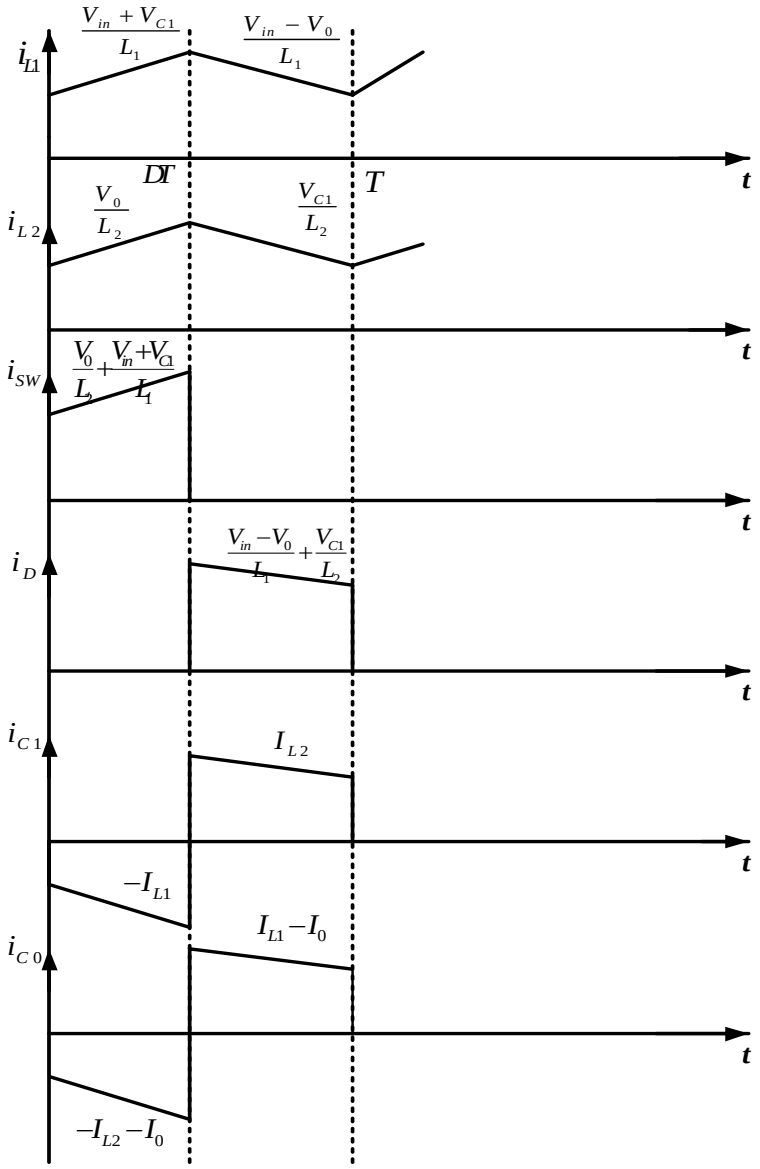


Fig. 2.4(a): Idealized current Waveforms for CCM.

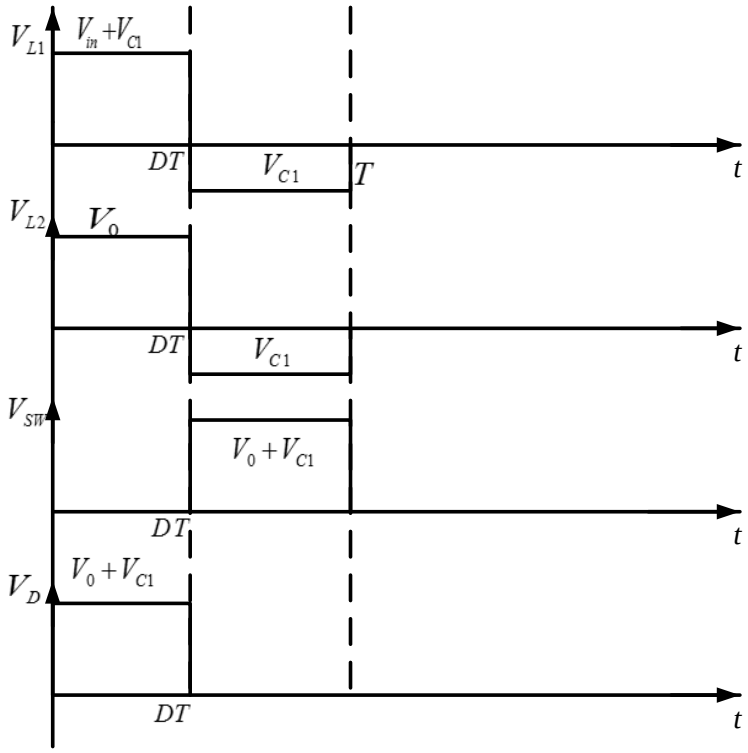


Fig. 2.4(b): Idealized voltage waveforms for CCM.

2.2.2 For time interval $DT \le t \le T$

Figure 2.3(b) shows equivalent circuit of converter for this time interval. The switch S is OFF and diode becomes ON, hence switch S current and voltage across diode are zero. The inductor L_1 current is given as

$$i_{L1}(t) = \frac{V_{in} - V_0}{L_1}\left(t - DT\right) + i_{L1}(DT) \tag{2.8}$$

Similarly inductor L_2 current is given as

$$i_{L2}(t) = \frac{V_{C1}}{L_2}\left(t - DT\right) + i_{L2}(DT) \tag{2.9}$$

In this interval, diode current will be equal to the sum of inductor currents and is given as

$$i_D(t) = \left(\frac{V_{in} - V_0}{L_1}\right)\left(t - DT\right) + \left(\frac{V_{C1}}{L_2}\right)\left(t - DT\right) + i_{L1}\left(DT\right) + i_{L2}\left(DT\right) \tag{2.10}$$

In steady state, inductor currents i_{L1} and i_{L2} at time T are given as

$$i_{L1}(T) = i_{L1}(0) = \left(\frac{V_{in} - V_0}{L_1}\right)(T - DT) + \left(\frac{V_{in} + V_{C1}}{L_1}\right)DT + i_{L1}(0) \tag{2.11}$$

$$i_{L2}(T) = i_{L2}(0) = \frac{V_{C1}}{L_2}(T - DT) + \frac{V_0}{L_2}DT + i_{L2}(0) \tag{2.12}$$

From equation (2.11) and (2.12), voltages V_{C1} is given as,

$$V_{C1} = \left(\frac{D}{1-D}\right)V_0 \tag{2.13}$$

Similarly from equation (2.11) and (2.13), output voltage in terms of input voltage is given as

$$V_0 = \left(\frac{1-D}{1-2D}\right)V_{in} \tag{2.14}$$

Therefore DC voltage transfer ratio in idealized converter is

$$M_{ideal} = \frac{V_0}{V_{in}} = \frac{1-D}{1-2D} \tag{2.15}$$

Figure 2.5 shows voltage gain response of ideal converter and it is derived by using equation (2.15). From Fig. 2.5 it can be observed that, converter provides positive gain for duty ratio range from 0 to 0.5 and for higher duty ratio converter gain is negative.

From equation (2.13) and (2.14), capacitor C_1 voltage in terms of input voltage is given by

$$V_{C1} = \left(\frac{D}{1-2D}\right)V_{in} \tag{2.16}$$

For ideal converter, $V_0I_0 = V_{in}I_{in}$, therefore by using equation (2.15)

$$\frac{V_0}{V_{in}} = \frac{I_{in}}{I_0} = \frac{1-D}{1-2D} \tag{2.17}$$

In this converter, average inductor current I_{L1} is same as input current I_{in}, therefore from equation (2.17)

$$I_{L1} = I_{in} = \left(\frac{1-D}{1-2D}\right) I_0 \tag{2.18}$$

To find average inductor current I_{L2}, amp-second balance principle is applied on capacitor C_1 which gives

$$-DI_{L1} + (1-D)I_{L2} = 0 \tag{2.19}$$

Therefore average inductor current I_{L2} is

$$I_{L2} = \left(\frac{D}{1-D}\right) I_{L1} = \left(\frac{D}{1-2D}\right) I_0 \tag{2.20}$$

The current through inductor L_1 at t=0 and current at $t = DT$ can be given from (2.6) and (2.18) as

$$i_{L1}(0) = I_{L1} - \frac{\Delta i_{L1}}{2} = \left(\frac{1-D}{1-2D}\right) I_0 - \frac{V_0}{2L_1} DT \tag{2.21}$$

$$i_{L1}(DT) = I_{L1} + \frac{\Delta i_{L1}}{2} = \left(\frac{1-D}{1-2D}\right) I_0 + \frac{V_0}{2L_1} DT \tag{2.22}$$

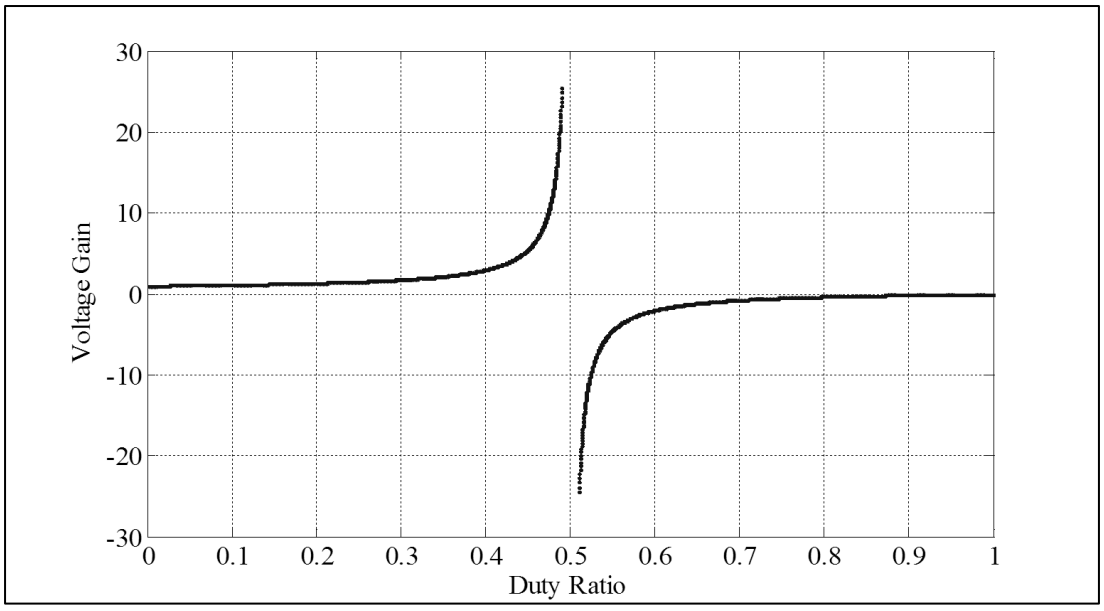


Fig. 2.5: Voltage Gain variation with duty ratio.

And similarly for inductor L_2 initial current and current at t = DT from (2.7) and (2.20) can be written as

$$i_{L2}(0) = I_{L2} - \frac{\Delta i_{L2}}{2} = \left(\frac{D}{1-2D}\right) I_0 - \frac{V_0}{2L_2} DT \tag{2.23}$$

$$i_{L2}(DT) = I_{L2} + \frac{\Delta i_{L2}}{2} = \left(\frac{D}{1-2D}\right) I_0 + \frac{V_0}{2L_2} DT \tag{2.24}$$

2.2.3 Peak and average values of currents and voltages for switch

According to Fig. 2.4(b) peak value of voltage across switch V_{SM} and peak reverse diode voltage V_{DRM} are equal and is given as

$$V_{SM} = V_{DRM} = V_0 + V_{C1}$$
$$V_{SM} = V_{DRM} = \frac{V_{in}}{1-2D} \tag{2.25}$$

Peak value of switch and diode current is sum of peak value of inductor currents,

$$I_{SM} = I_{DM} = I_{L1M} + I_{L2M} = I_{L1} + I_{L2} + \frac{\Delta i_{L1}}{2} + \frac{\Delta i_{L2}}{2} \tag{2.26}$$

Therefore from equation (2.6), (2.7), (2.18), (2.20) and (2.26),

$$I_{SM} = I_0 \left(\frac{1}{1-2D} + \frac{R}{2L} DT\right) \tag{2.27}$$

Where, L =L_1 || L2

Also from Fig. 2.4(a), average values of switch and diode currents are approximated as

$$I_{SAV} = \frac{D}{1-2D} I_0 \tag{2.28}$$

$$I_{DAV} = \frac{1-D}{1-2D} I_0 \tag{2.29}$$

2.2.4 Design of Capacitance values

For converter in CCM, the ripple voltages across capacitors can be found out by using averaged currents in the circuit. From Fig. 2.3(a), output capacitor C_0 current during switch ON is given as

$$C_0 \frac{\Delta V_0}{DT} = I_{L2} + I_0 \tag{2.30}$$

From equations (2.17), (2.20) and (2.30), capacitor value can be derived for a given voltage ripple ΔV_0 as

$$C_0 = \frac{V_{in}\left(1-D\right)^2 DT}{R\left(1-2D\right)^2 \Delta V_0} \tag{2.31}$$

Also current in capacitor C_1 during switch ON time is given as

$$C_1 \frac{\Delta V_{C1}}{DT} = I_{L1} \tag{2.32}$$

Using equations (2.17), (2.18) and (2.32), capacitor C_1 value can be derived for given voltage ripple as

$$C_1 = \frac{V_{in}\left(1-D\right)^2 DT}{R\left(1-2D\right)^2 \Delta V_{C1}} \tag{2.33}$$

2.3 Boundary between CCM / DCM and analysis in DCM

2.3.1 Minimum inductance value for CCM

The boundary between continuous and discontinuous mode occurs when minimum value of diode current and switch current reaches zero. So at boundary, $I_{S\min} = I_{D\min} = 0$. From equation (2.3), it can be inferred as

$$I_{S\min} = I_{L1} + I_{L2} - \frac{\Delta i_{L1}}{2} - \frac{\Delta i_{L2}}{2} = \frac{I_0}{1-2D} - \frac{V_0 DT}{2L} = 0 \tag{2.34}$$

Therefore

$$\frac{2L}{RT} = D\left(1-2D\right) \tag{2.35}$$

$$K_c \geq D(1-2D)$$

(2.36)

Where K_c= (2L/RT) and L =L_1 || L_2. From equation (2.36), minimum value of inductor can be derived for continuous mode of operation of converter, for given values of load resistance, switching frequency and duty cycle.

2.3.2 DC voltage transfer ratio in DCM and expression for remaining current

The boundary condition for switch current and diode current in discontinuous conduction mode is

$$i_S(0) = i_D(0) = i_{L1}(0) + i_{L2}(0) = 0$$

(2.37)

Therefore, the equivalent circuit of the converter in discontinuous conduction mode is shown in Fig. 2.6(a). Figure 2.6(b) shows different current waveforms in the circuit for the converter operating in DCM. Figure 2.6(b) also shows voltage waveform across inductor L_1 and L_2.

For one cycle, volt-second balance equation for inductor L_1 is

$$(V_{in} + V_{C1})D + (V_{in} - V_0)D_1 = 0$$

(2.38)

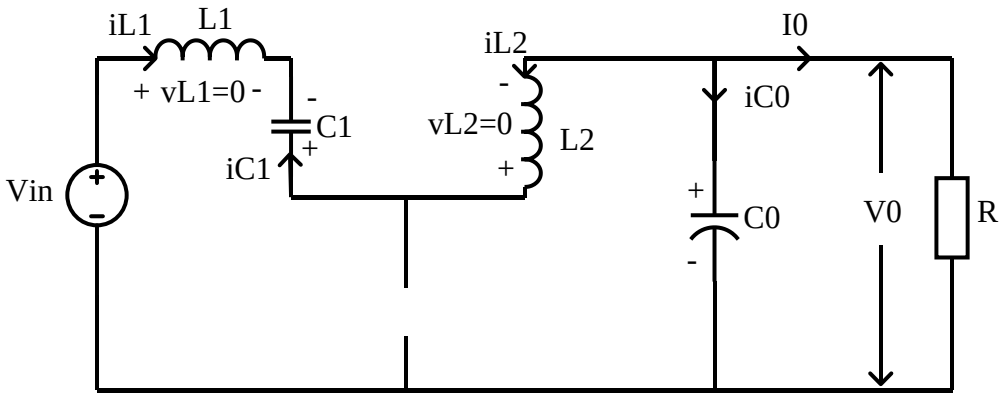


Fig. 2.6(a): Equivalent circuit of converter for DCM.

With reference to Fig. 2.6, $V_{C1} = V_0 - V_{in}$, hence equation (2.38) is simplified as

$$\frac{V_0}{V_{in}} = \frac{D_1}{D_1 - D} \tag{2.39}$$

Here D_1T is the duration in which inductor currents decreases to a constant value I_R after DT. The equation (2.39) is a DC Transfer ratio of the converter in discontinuous mode of operation. Remaining current I_R [44] flows through inductors during DCM can be calculated in a following way.

With reference to Fig. 2.6(b), amp-second balance equation for capacitor C_1 is

$$\bar{I}_{C1} = -\frac{\Delta i_{L1}}{2} D + \frac{\Delta i_{L2}}{2} D_1 - I_R = 0 \tag{2.40}$$

Where I_R is remaining current [44].

From equations (2.6), (2.7) and (2.40) remaining current expression can be written as

$$I_R = \frac{V_0 DT}{2}\left[\frac{D_1}{L_2} - \frac{D}{L_1}\right] \tag{2.41}$$

Similarly with reference to Fig. 2.6(b), amp-second balance equation for capacitor C_0 is

$$\bar{I}_{C0} = I_0 - I_R + D\frac{\Delta i_{L2}}{2} - D_1\frac{\Delta i_{L1}}{2} = 0 \tag{2.42}$$

Using equations (2.41) and (2.42), output current I_0 can be given as

$$I_0 = \frac{V_0 DT}{2}\left[\frac{D_1}{L_1} - \frac{D}{L_2}\right] + \frac{V_0 DT}{2}\left[\frac{D_1}{L_2} - \frac{D}{L_1}\right] \tag{2.43}$$

$$I_0 = \frac{V_0 DT}{2L}\left[D_1 - D\right] \tag{2.44}$$

$$\frac{V_0}{R} = \frac{V_0 DT}{2L}\left[D_1 - D\right] \tag{2.45}$$

$$K_c = D\left[D_1 - D\right] \tag{2.46}$$

Where $L = L_1 \parallel L_2$, and $K_c = \frac{2L}{RT}$.

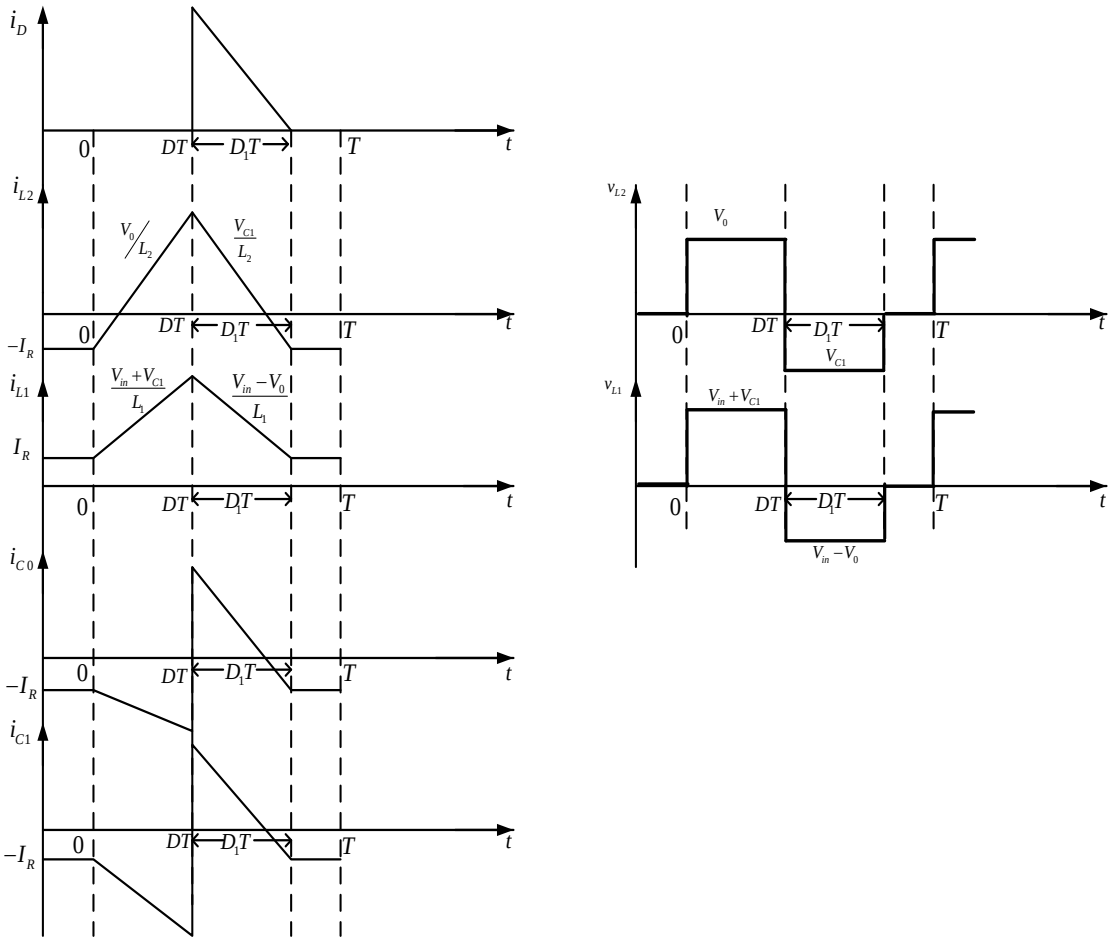


Fig. 2.6(b): Idealized current waveforms for DCM.

From equation (2.46), D_1 is

$$D_1 = \frac{K_c + D^2}{D} \tag{2.47}$$

From equation (2.47) substitute expression of D_1 in equation (2.39), therefore voltage gain in DCM is

$$M_{DCM} = \frac{K_c + D^2}{K_c} \tag{2.48}$$

Also from equation (2.41) and (2.47) remaining current expression in terms of K_c becomes

$$I_R = \frac{V_0 DT}{2}\left[\frac{K_c + D^2}{DL_2} - \frac{D}{L_1}\right] \tag{2.49}$$

$$I_R = \frac{V_0 DT}{2L_2}\left[D_1 - \sigma D\right] \tag{2.50}$$

Where $\sigma = \frac{L_2}{L_1}$

If in equation (2.50) $\sigma D > D_1$, then $I_R < 0$ Else, $I_R > 0$. Also, if $D_1 = \sigma D$, then $I_R = 0$

2.4 Power losses and dc voltage transfer ratio for non-ideal converter

For non-ideal converter, equivalent circuit is shown in Fig. 2.7. Inductors and capacitors are represented with their equivalent series resistance. MOSFET S is represented with an ideal switch and series equivalent drain to source resistance **r_{DS}**. Diode D is represented with forward voltage drop V_F in series with forward resistance R_F. The power loss in each component is estimated as given below.

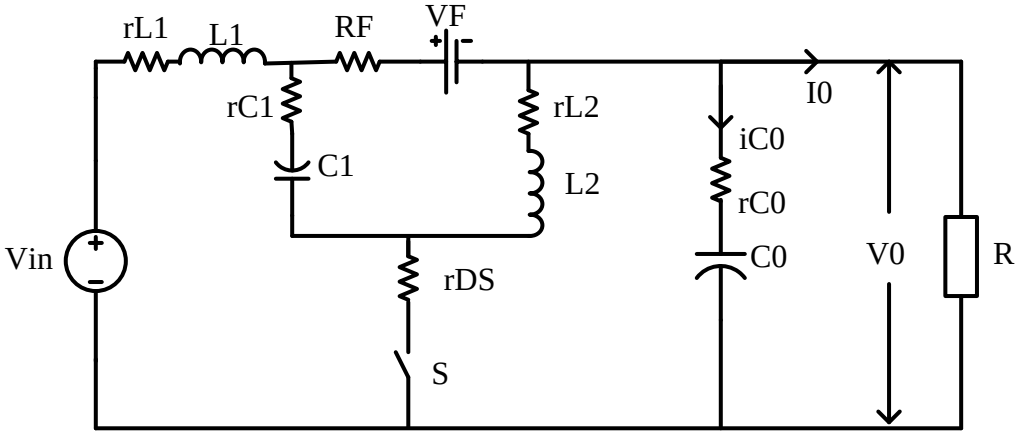


Fig. 2.7: Equivalent circuit for Non-ideal converter.

2.4.1 Power losses in QZ-source based dc-dc converter in CCM

From Fig. 2.3(b), an approximate RMS current through the switch S is

$$I_{S(RMS)} = \frac{\sqrt{D}}{(1-2D)} I_0 \tag{2.51}$$

Hence ohmic power loss in MOSFET S is

$$P_S = I_{S(RMS)}{}^2 r_{DS} = \frac{DI_0{}^2}{(1-2D)^2} r_{DS} = \frac{DP_0}{(1-2D)^2 R} r_{DS} \tag{2.52}$$

Here P_0 is output power, R is load resistance and r_{DS} is MOSFET ON resistance.

The approximate RMS value of current through diode derived from Fig. 2.3(b), is given as

$$I_{D(RMS)} = \frac{\sqrt{1-D}}{(1-2D)} I_0 \tag{2.53}$$

The ohmic power loss in forward resistance R_F of diode is

$$P_{RF} = I_{D(RMS)}{}^2 R_F = \frac{(1-D) I_0{}^2}{(1-2D)^2} R_F = \frac{(1-D) P_0}{(1-2D)^2 R} R_F \tag{2.54}$$

So power loss associated with the forward drop is given as

$$P_{VF} = V_F I_{D(AVG)} = V_F \left(\frac{1-D}{1-2D} \right) I_0 = \left(\frac{1-D}{1-2D} \right) \frac{P_0 V_F}{V_0} \tag{2.55}$$

Using (2.54) and (2.55), the total power loss in diode is

$$P_D = P_{RF} + P_{VF}$$

$$P_D = \left[\frac{(1-D) R_F}{(1-2D)^2 R} + \frac{(1-D) V_F}{(1-2D) V_0} \right] P_0 \tag{2.56}$$

In inductors power losses are of two type core loss and winding loss, in PWM converters core loss is negligible. The winding loss is depends up on winding resistance and RMS value of current flowing through it.

The approximate RMS value of current through inductor L_1 is derived from Fig. 2.3 (b) and it can be given as

$$I_{L1(RMS)} = I_{in} = \frac{(1-D)}{(1-2D)} I_0 \tag{2.57}$$

And similarly for inductor L_2 from Fig. 2.3(b), approximate RMS value of current is

$$I_{L2(RMS)} = \frac{D}{(1-2D)} I_0 \tag{2.58}$$

Resulting power losses are

$$P_{r_{L1}} = I_{L1(RMS)}{}^2 r_{L1} = \left(\frac{1-D}{1-2D}\right)^2 \frac{P_0 r_{L1}}{R} \tag{2.59}$$

$$P_{r_{L2}} = I_{L2(RMS)}{}^2 r_{L2} = \left(\frac{D}{1-2D}\right)^2 \frac{P_0 r_{L2}}{R} \tag{2.60}$$

From Fig. 2.3(b), RMS value of I_{C1} can be derived as

$$I_{C1(RMS)} = \left(\frac{\sqrt{D(1-D)}}{1-2D}\right) I_0 \tag{2.61}$$

Similarly RMS value of current through C_0 is

$$I_{C0(RMS)} = \left(\frac{\sqrt{D(1-D)}}{1-2D}\right) I_0 \tag{2.62}$$

The power loss associated with the capacitors from (2.61) and (2.62) is

$$P_{rc} = \frac{D(1-D)(rc_1 + rc_0) P_0}{(1-2D)^2 R} \tag{2.63}$$

The total power loss in QZS based DC-DC converter is

$$P_{loss} = P_S + P_D + P_{r_{L1}} + P_{r_{L2}} + P_{rc} \tag{2.64}$$

2.4.2 DC voltage transfer function of non-ideal converter

The efficiency of non-ideal converter is

$$\text{Efficiency } \eta = \frac{P_0}{P_{in}} = \frac{V_{0-NI} I_0}{V_{in} I_{in}} = \frac{1}{1 + \frac{P_{loss}}{P_0}} \tag{2.65}$$

Where, $V_{0\text{-}NI}$ is output voltage for a non-ideal converter. From equations (2.17) and (2.65), a non-ideal DC voltage gain $M_{non\text{-}ideal}$ is

$$\eta = M_{non-ideal}\frac{1-2D}{1-D} \tag{2.66}$$

$$M_{non-ideal} = \frac{1}{1+\frac{P_{loss}}{P_0}}\frac{1-D}{1-2D} \tag{2.67}$$

$$M_{non-ideal} = \frac{1}{1+\frac{P_{loss}}{P_0}}M_{ideal} \tag{2.68}$$

2.5 Small-signal model and controller design

2.5.1 Small-signal model

It would be interesting to study a dynamic model of this converter since it is a fourth order converter. A state space averaging approach is used to obtain a small-signal dynamic model. Inductor currents and capacitor voltages are chosen as state variables, and which are given in state vector form as $x(t) = \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & v_{C1}(t) & v_0(t) \end{bmatrix}^T$. An input voltage v_{in} is chosen as input variable and input vector is given as $u(t) = \begin{bmatrix} v_{in}(t) \end{bmatrix}$. After averaging and by applying small signal perturbations, the state equations of the small signal ac model are

$$\begin{pmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_0 \end{pmatrix}\frac{d}{dt}\begin{pmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_0(t) \end{pmatrix} = \begin{pmatrix} 0 & 0 & D & -D' \\ 0 & 0 & -D' & D \\ -D & D' & 0 & 0 \\ D' & -D & 0 & -1/R \end{pmatrix}\begin{pmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_0(t) \end{pmatrix} + \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \end{pmatrix}\begin{bmatrix} \hat{v}_{in}(t) \end{bmatrix} + \begin{pmatrix} V_{C1}+V_0 \\ V_{C1}+V_0 \\ -(I_{L1}+I_{L2}) \\ -(I_{L1}+I_{L2}) \end{pmatrix}\hat{d}(t) \tag{2.69}$$

After Laplace transformation and rearrangement, equation (2.69) becomes

$$\begin{pmatrix} sL_1 & 0 & -D & D' \\ 0 & sL_2 & D' & -D \\ D & -D' & sC_1 & 0 \\ -D' & D & 0 & sC_0+1/R \end{pmatrix}\begin{pmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_0(t) \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \end{pmatrix}\left[\hat{v}_{in}(s)\right] + \begin{pmatrix} V_{C1}+V_0 \\ V_{C1}+V_0 \\ -(I_{L1}+I_{L2}) \\ -(I_{L1}+I_{L2}) \end{pmatrix}\hat{d}(s) \qquad (2.70)$$

To obtain a transfer function of output voltage to input voltage, the perturbation of duty ratio is assumed to be zero and therefore

$$G_{vg} = \left.\frac{\hat{v}_0(s)}{\hat{v}_{in}(s)}\right|_{\hat{d}(S)=0} = \frac{D'\left(s^2L_2C_1 - D^2 + D'^2\right)}{Q} \qquad (2.71)$$

where

$$Q = s^4L_1L_2C_1C_2 + s^3L_1L_2C_1/R + s^2\left(C_1L_1D^2 + L_2C_1D'^2 + L_1C_2\right) + s\left(L_1/R + C_2D^2D'\right) + D^4 + D'^4 - 2D^2D'^2 + D^2D'/R$$

To obtain transfer function of input conductance, the perturbation of duty ratio is assumed to be zero and therefore

$$G_{ig} = \left.\frac{\hat{i}_{L1}(s)}{\hat{v}_{in}(s)}\right|_{\hat{d}(S)=0} = \frac{s^3L_2C_1C_2 + s^2L_2C_1/R + s\left(D^2C_1 + D'^2C_2\right) + D'^2/R}{Q} \qquad (2.72)$$

To obtain transfer fuction of output voltage to duty ratio, the perturbation of input voltage is assumed to be zero and therefore

$$G_{vd}(s) = \left.\frac{\hat{v}_0}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{\begin{array}{c} G_1(V_{C1}+V_0) + G_2(V_{C1}+V_0) \\ +G_3(-I_{L1}-I_{L2}) + G_4(-I_{L1}-I_{L2}) \end{array}}{Q} \qquad (2.73)$$

Transfer function of input current to duty ratio is obtained as

$$G_{i1d}(s)=\left.\frac{\hat{i}_{L1}(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0}=\frac{\begin{array}{l}P_1\left(V_{C1}+V_0\right)+P_2\left(V_{C1}+V_0\right)+P_3\left(-I_{L1}-I_{L2}\right)+\\P_4\left(-I_{L1}-I_{L2}\right)\end{array}}{Q} \quad (2.74)$$

$$G_{i2d}(s)=\left.\frac{\hat{i}_{L2}(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0}=\frac{\begin{array}{l}F_1\left(V_{C1}+V_0\right)+F_2\left(V_{C1}+V_0\right)+F_3\left(-I_{L1}-I_{L2}\right)+\\F_4\left(-I_{L1}-I_{L2}\right)\end{array}}{Q} \quad (2.75)$$

Where, details of G_1-G_4, P_1-P_4 and F_1-F_4 of equations (2.73)-(2.75) are given in appendix-A.

2.5.2 Controller design

By using the transfer functions derived above, a controller is designed for a proposed converter. Passive elements values are taken as L_1=L_2=355µH, C_1=60µF, C_0= 200µF, load resistance 40Ω and while deriving bode plot non-idealities of inductors and capacitors have not been considered. The design specification for the passive elements is discussed in section 2.6. Figure 2.8(a) shows open-loop bode plot obtained from control to output voltage transfer function for a duty ratio D=0.2 and the input voltage is 15V. If one substitutes all the values, it can be observed that transfer function of G_{vd}(s) and G_{i1d} (s) has non-minimum phase behavior that is RHP zeros and $\hat{i}_{L2}(s)/\hat{d}(s)$ is a minimum phase transfer function. Voltage mode control of the present converter will have low bandwidth due to presence of RHP zeros and resonance peaks [45], [46], [47], [48], [49]. Therefore average current mode control technique can be used to improve the dynamic performance [48]. Inductor L_2 current can be used for feedback in addition with output voltage. Figure 2.8(b) shows the simplified block diagram of average current mode control system consisting inner current control loop and outer voltage control loop. This control technique has been widely used for control of DC-DC converters, where current loop is designed to maximize bandwidth of closed loop and voltage control loop is designed to satisfy regulation conditions [46]. A MATLAB based controller design tool ‘SISOTOOL’ is used for design.

Design of current control loop:

For the converter parameters given above transfer function of inductor current i_{L2} to control can be given by

$$\frac{\hat{i}_{L2}(s)}{\hat{d}(s)} = T_i(s) = \frac{7.04\times10^4 s^3 + 3.775\times10^7 s^2 + 1.459\times10^{12} s + 4.133\times10^{14}}{s^4 + 125s^3 + 4.15\times10^7 s^2 + 3.991\times10^9 s + 2.38\times10^{14}} \qquad (2.76)$$

A PI controller is designed to get phase margin PM = 60º and crossover frequency f_c=3 KHz for feedback gain $H_1(s)$ =1. The transfer function of compensator can be given as

$$C_1(s) = 0.2228\frac{\left(s + 1.05\times10^4\right)}{s} \qquad (2.77)$$

The bode plot of compensated current control loop is as shown in Fig. 2.8(c).

Design of voltage control loop:

The dynamics of current control loop is much faster than outer voltage control loop. Hence, dynamics of current control loop are neglected during design of voltage control loop [45].

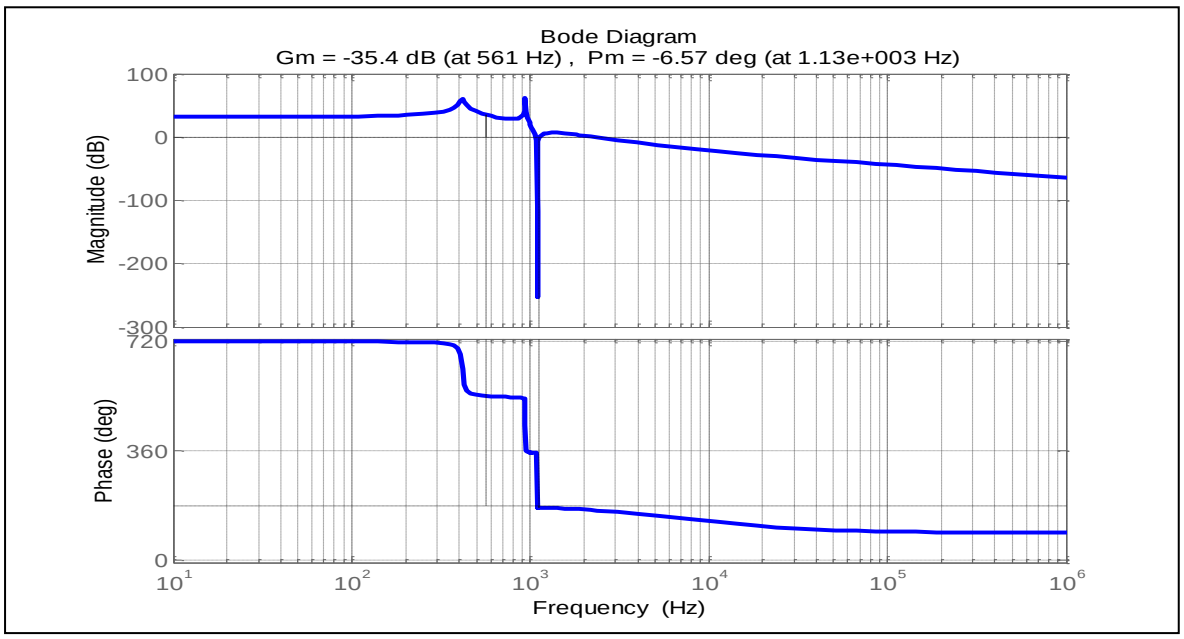


Fig. 2.8(a): Frequency response of system without controller.

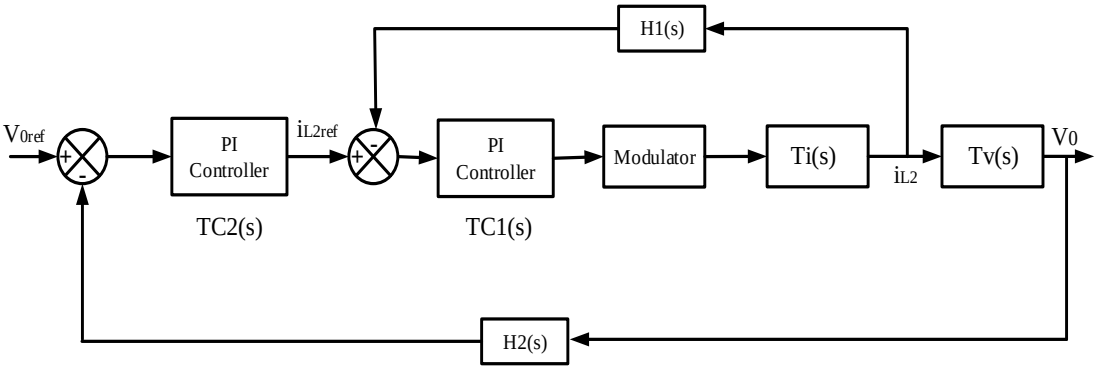


Fig. 2.8(b): Complete two loop control for average current control.

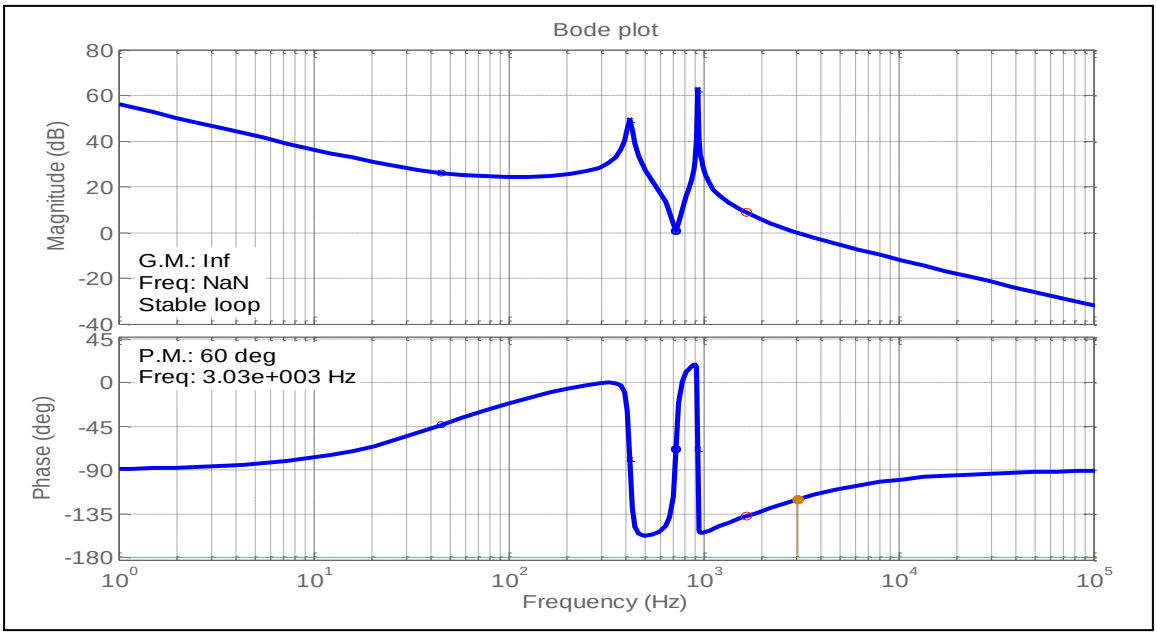


Fig. 2.8(c): Bode plot of current control loop with PI controller.

To design voltage control loop the transfer function of output voltage to inductor current i_{L2} is obtained using (2.75) and (2.77) as

$$\frac{\hat{v}_0(s)}{\hat{i}_{L2}(s)} = T_v(s) = \frac{-4167s^3 + 2.113\times10^8 s^2 - 1.956\times10^{11} s + 9.919\times10^{15}}{70420s^3 + 3.775\times10^7 s^2 + 1.459\times10^{12} s + 4.133\times10^{14}} \qquad (2.78)$$

The gain crossover frequency for voltage controller is selected 50 times slower than that of current control loop [45], that is 60 Hz and feedback gain $H_2(s)$=0.1. Figure 2.8(d) shows bode plot of voltage loop with PI controller. A PI controller is designed to get desired criteria and its transfer function is given as

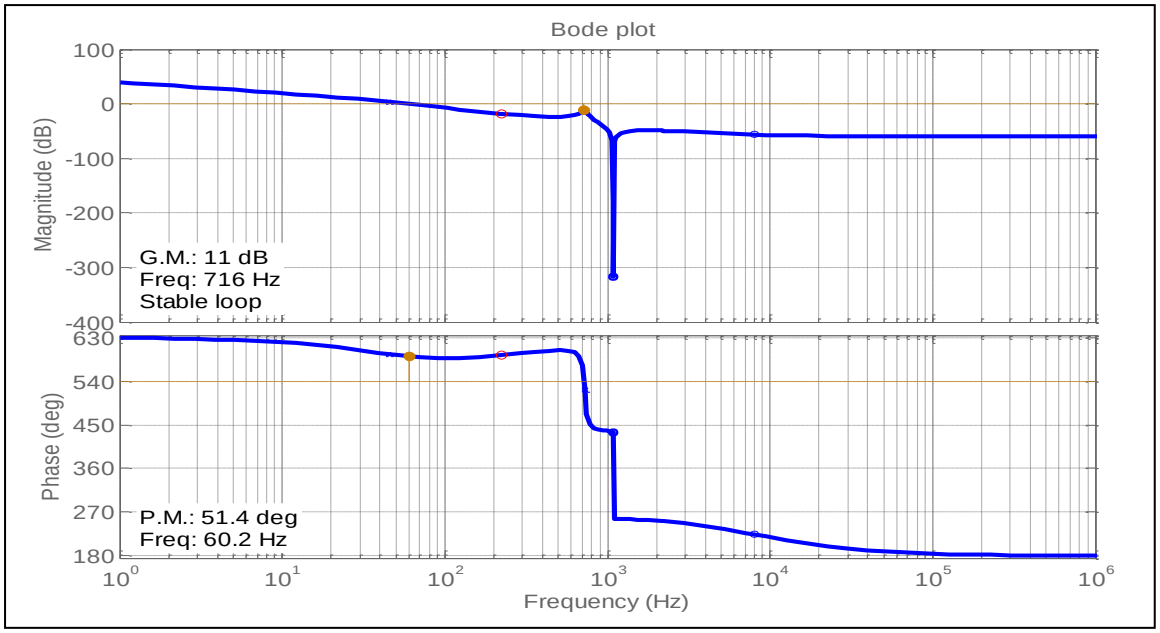


Fig. 2.8(d): Bode plot of voltage control loop with PI controller.

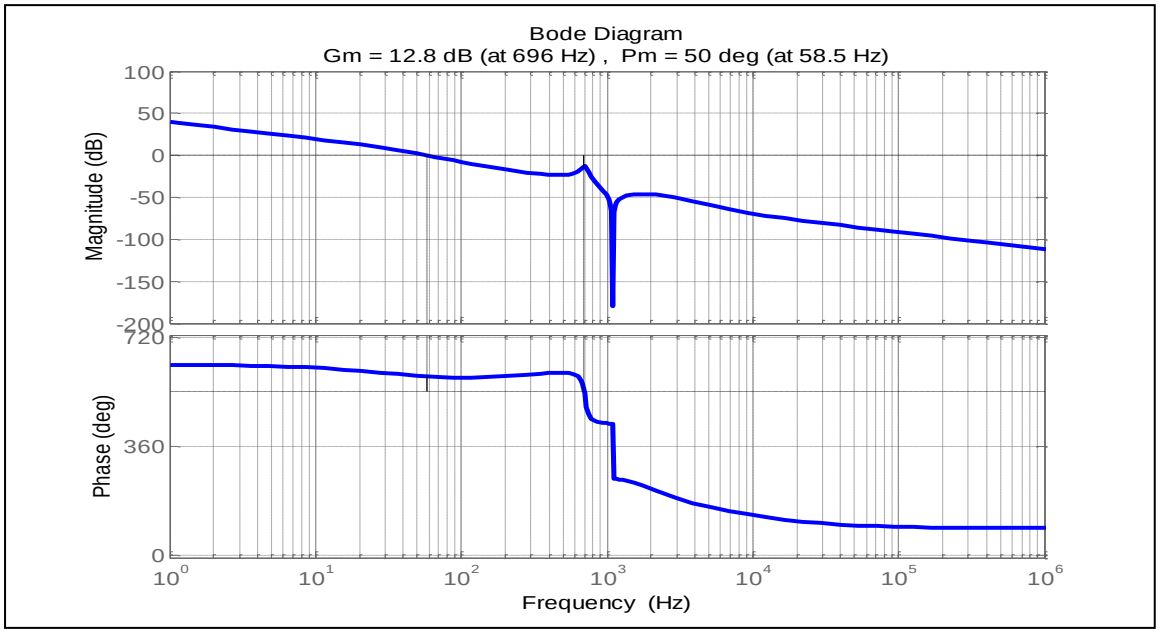


Fig. 2.9(a): Frequency response of overall system.

$$C_2(s) = 0.18\frac{(s+1400)}{s} \tag{2.79}$$

Taking into accounts the dynamics of current control system, the overall transfer function of the system is given as

$$T_{OL}(s) = \left[\frac{T_i(s)C_1(s)H_1(s)}{1+T_i(s)C_1(s)H_1(s)}\right]T_v(s)C_2(s)H_2(s) \tag{2.80}$$

Bode plot of overall system is as shown in Fig. 2.9(a) and it shows that a phase margin of 50º at 58.5Hz is achieved. Figure 2.9(b) shows schematic of converter with controller circuit realized by using op-amps and pulse width modulator.

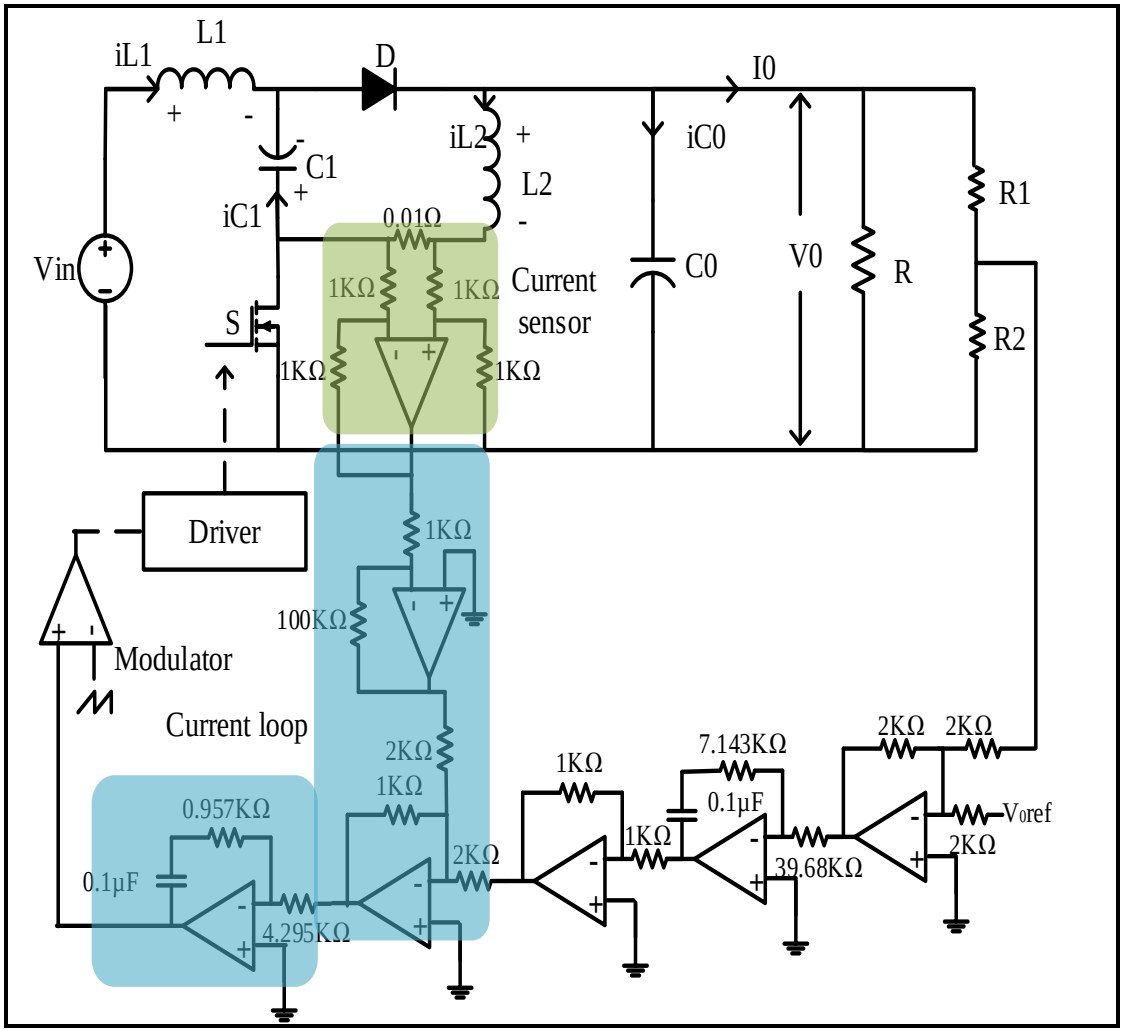


Fig. 2.9(b): Switching regulator using PWM QZS converter.

2.6 Results and comparison

2.6.1 Simulation and experimental results

The specifications of experimental set-up for fourth order step-up PWM DC-DC converter are as given in table 2.1. TL494 is used as a PWM pulse generator at 20 KHz frequency and converter is operates in open loop configuration. Inductors are

selected to maintain CCM operation for given circuit parameters as per equation (2.36). The capacitors are selected to maintain output voltage ripple below 1% and ripple across C_1 to below 5% as per equations (2.31) and (2.33).

Figure 2.10 shows simulation waveforms of inductor current i_{L1}, i_{L2} and output voltage V_0 for D = 0.30. Figure 2.11 shows experimental waveforms of inductor current i_{L1}, i_{L2} and output voltage V_0. The duty ratio is kept at 0.30 and converter operates in CCM. Figure 2.12 shows simulation waveforms in DCM operation of inductor current i_{L1}, i_{L2} and output voltage V_0 for D = 0.24. Figure 2.13 shows experimental waveforms of inductor current i_{L1}, i_{L2} and output voltage V_0 for same case of Fig. 2.12. The load resistance for this condition is kept as 250 Ω. It can be seen that the results fairly matches with the calculated values obtained from derived expressions.

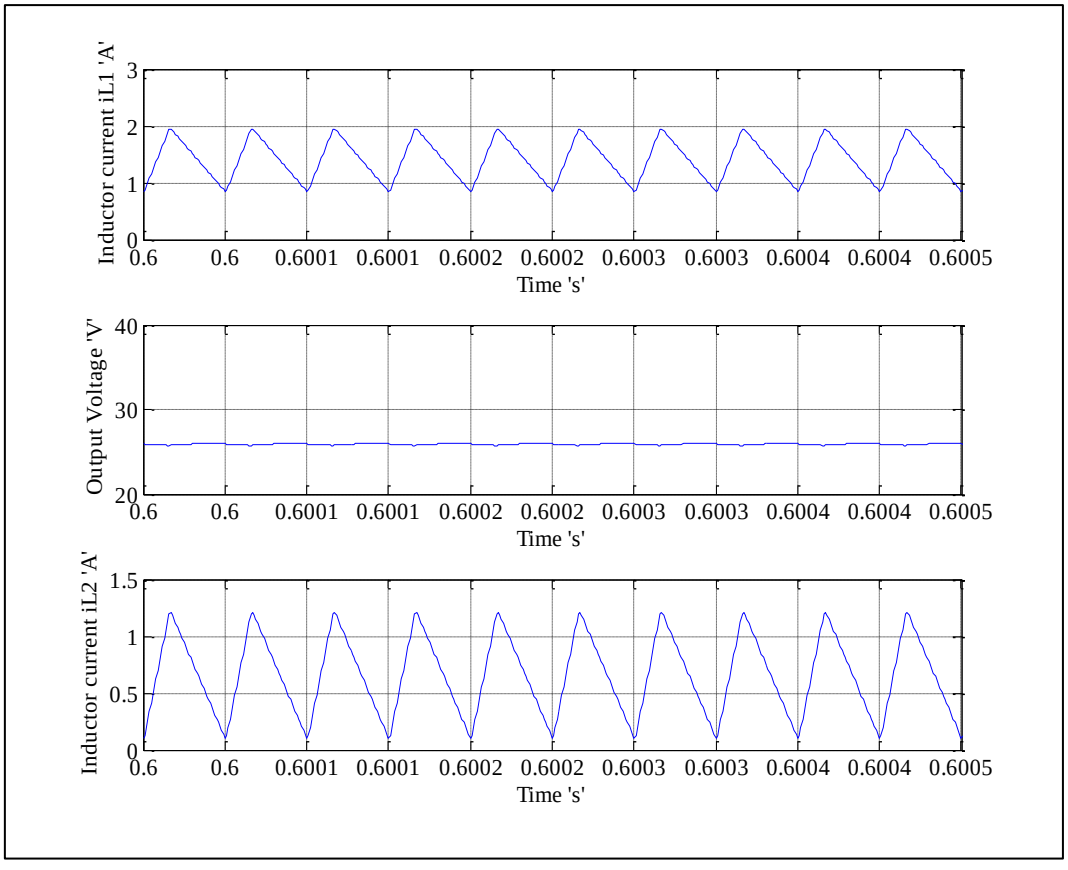
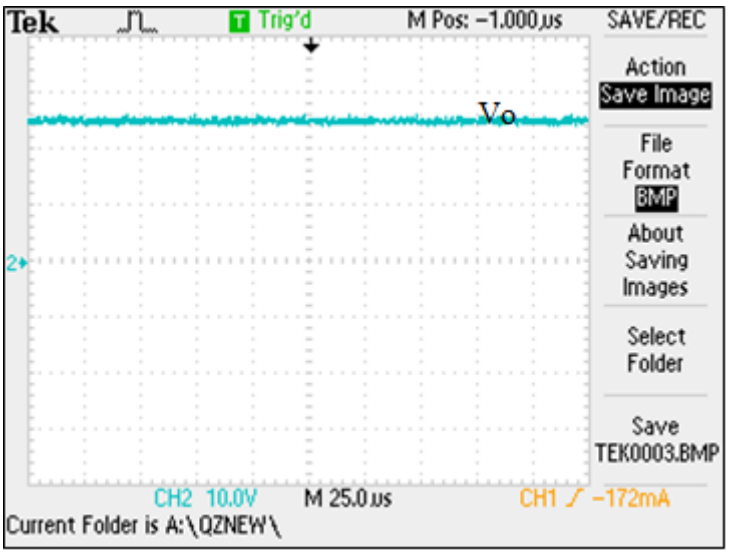


Fig. 2.10: Simulation results in CCM for D=0.3 and V_{in}=15V of output voltage, inductor current i_{L1} and i_{L2} .

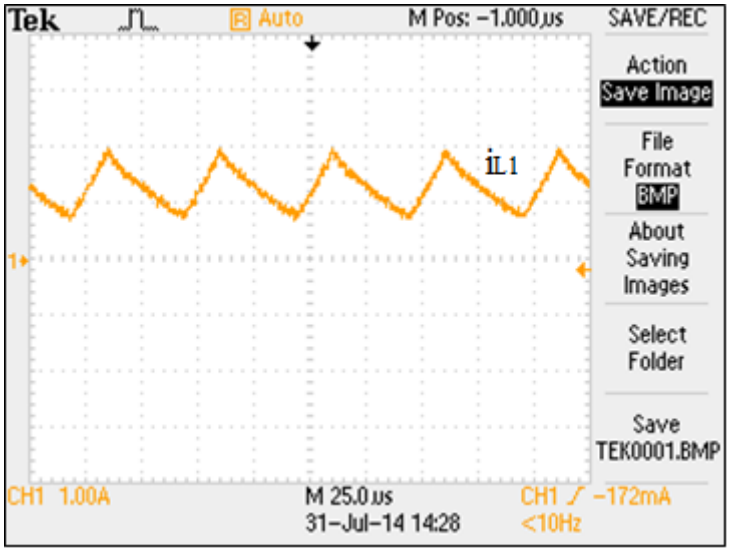
Table 2.1.1: Specifications of the converter.

S.No.	Parameter	value
1	Input voltage	15 V
2	Switching frequency	20 KHz
3	Inductors L_1,L_2,r_{L1},r_{L2}	355.5µH,356µH,0.035Ω,0.035Ω
4	Capacitor C_1,r_{C1}	60µF,0.155Ω
5	Capacitor C_0,r_{C0}	200µF,0.038Ω
6	MOSFET switch, R_{DS}, C_s	IRF540N,44mΩ,250pF
7	Diode ,V_F	MUR460, 1.05V
8	Duty Cycle D	For CCM = 0.3,For DCM = 0.24
9	Load resistance	ForCCM:40Ω, For DCM:250Ω

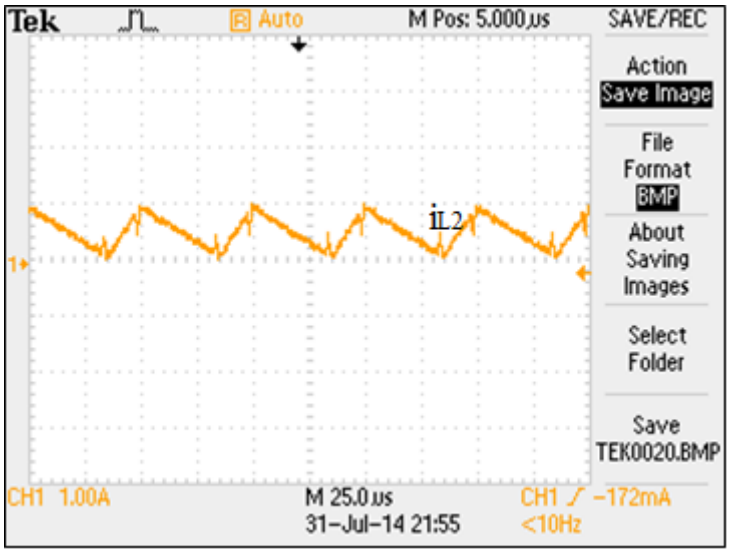
Figure 2.14(a) and Fig. 2.14(b) shows calculated and experimental results for output voltage and efficiency of the converter operates in CCM. In Fig. 2.14(a) calculated value of output voltage is derived by using equation (2.68), and in Fig. 2.14(b) calculated value of efficiency is derived by using equation (2.66).



(a)



(b)



(c)

Fig. 2.11: Experimental results in CCM for D=0.3 and V_{in}=15V of (a) output voltage, (b) inductor current i_{L1} and (c) i_{L2} .

The difference between experimental and calculated value can be attributed to the losses in the converter due to ringing in the MOSFET and stray inductances and capacitances in the set up.

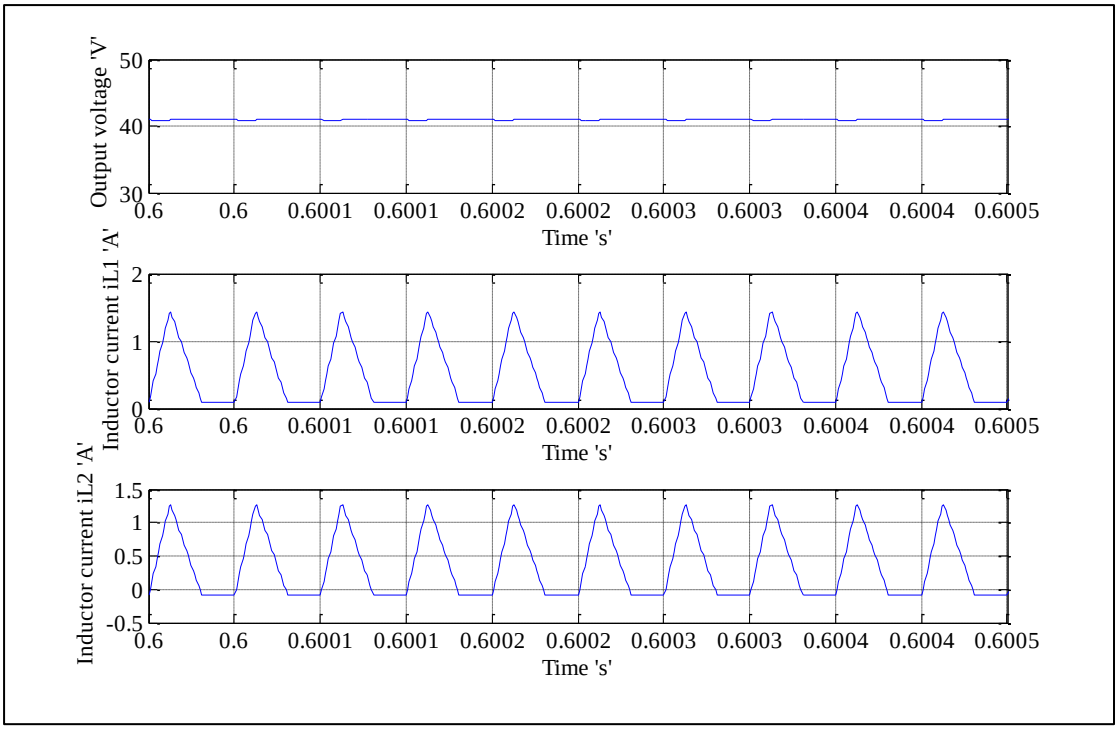
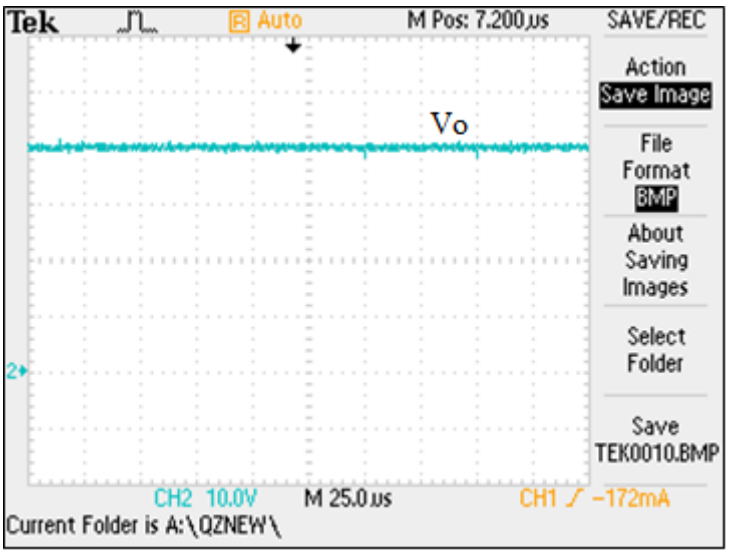
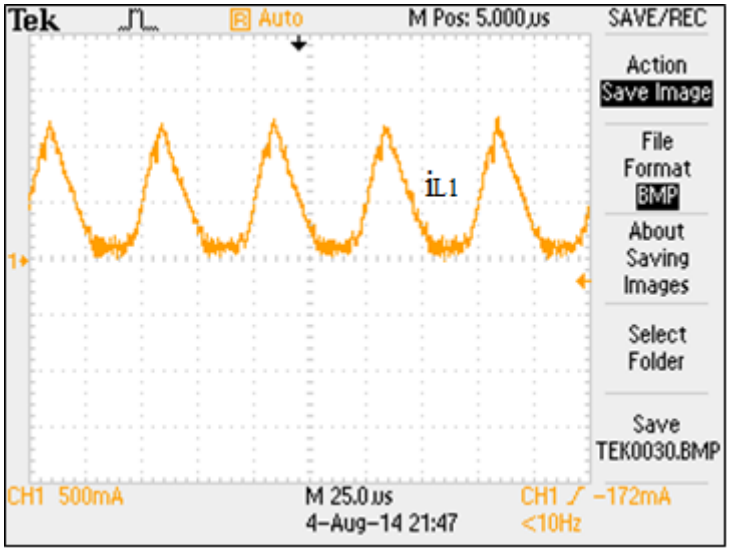


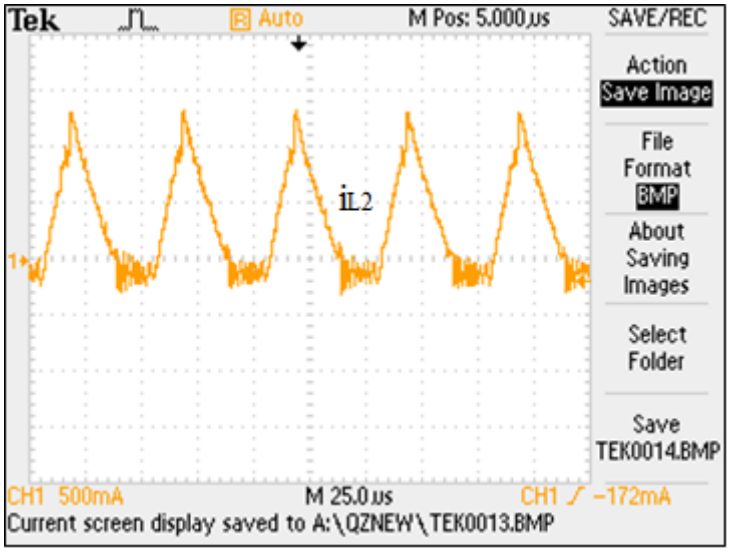
Fig. 2.12: Simulation results in DCM for D=0.24 and V_{in}=15V of output voltage, inductor current i_{L1} and i_{L2} .



(a)



(b)



(c)

Fig. 2.13: Experimental results in DCM for D=0.24 and V_{in}=15V of (a) output voltage,(b) inductor current i_{L1} and (c) i_{L2} .

Figure 2.15 shows simulation and experimental results for converter with closed loop control. Two cases are considered for step change in reference voltage. It can be observed that output voltage follows reference signal in a desired manner.

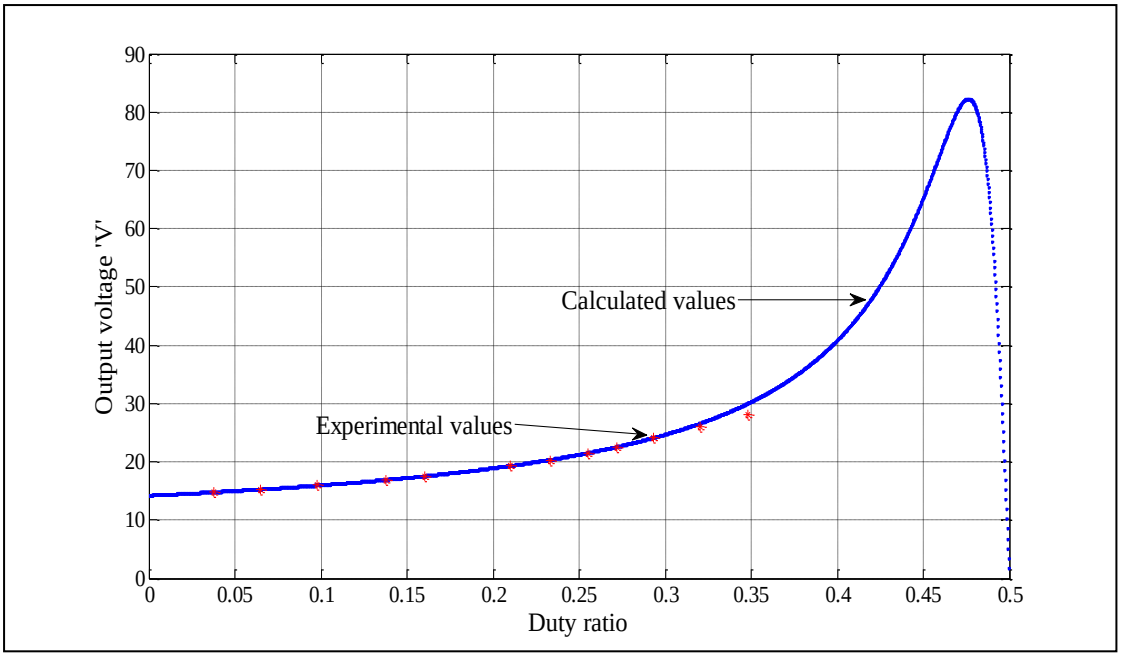


Fig. 2.14(a): Output voltage V_0 as a function of D for V_{in}= 15 V.

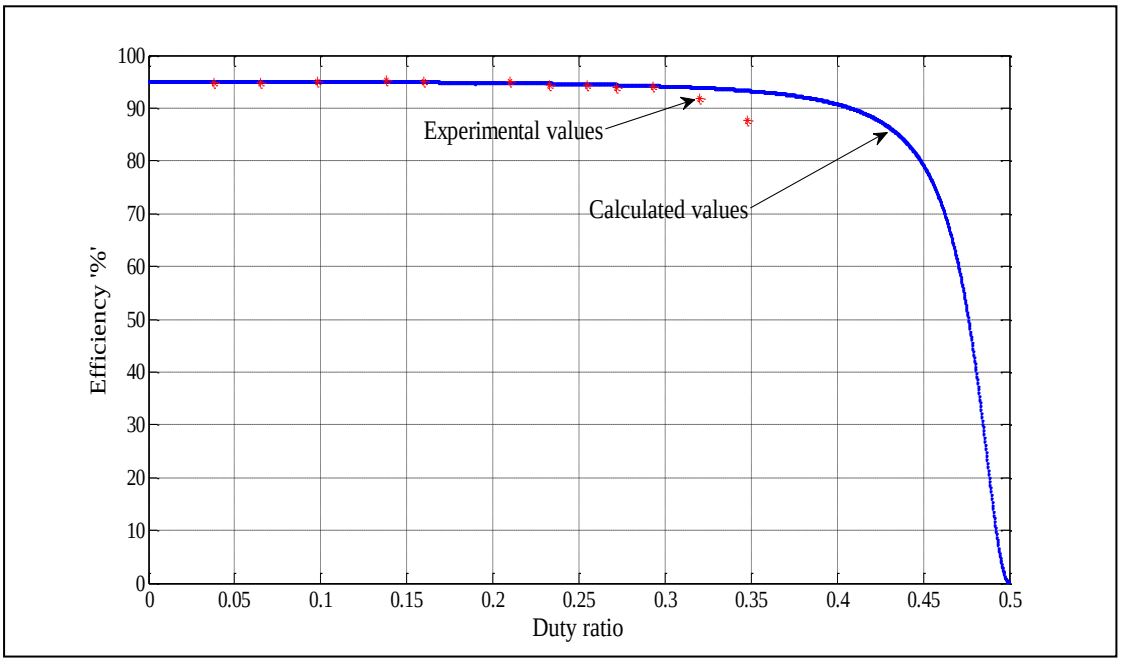


Fig. 2.14(b): Efficiency as a function of D.

In Fig. 2.16 (a) and Fig. 2.16(b) reference voltage is subjected to step change from 12.5 V to 15V. In Fig. 2.16 (c) and Fig. 2.16(d), step change is given in reference from 15 V to 12.5 V, which brings desired change in the output voltage also. It can be observed that simulation and experimental results matches quite well.

2.6.2 Comparison with PWM Z-source DC-DC converter

Since a proposed fourth order converter has its origin in Z-source converter based topologies, it will be quite interesting to compare it with the PWM Z-source DC-DC converter [28] of Fig. 2.15. The laboratory prototype of converter [28] is built for same voltage and power level for comparison.

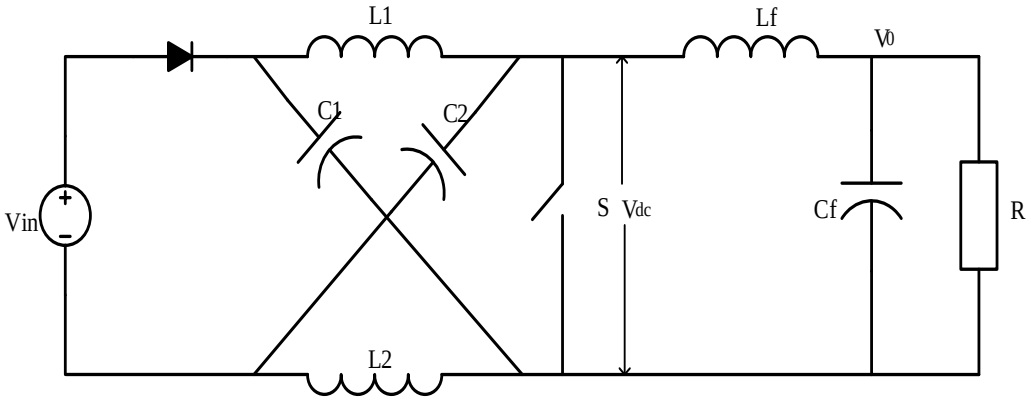


Fig. 2.15: PWM Z-source DC-DC converter.

Figure 2.17 shows relationship of efficiency with output voltage, for same operating condition. Table 2.2 gives comparison of the converter introduced with the converter given in [28].

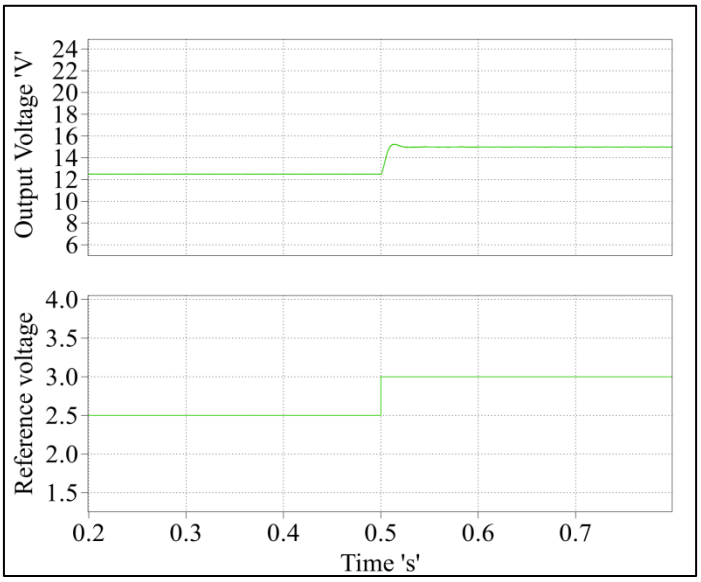


Fig. 2.16(a): Simulation result for step change in reference.

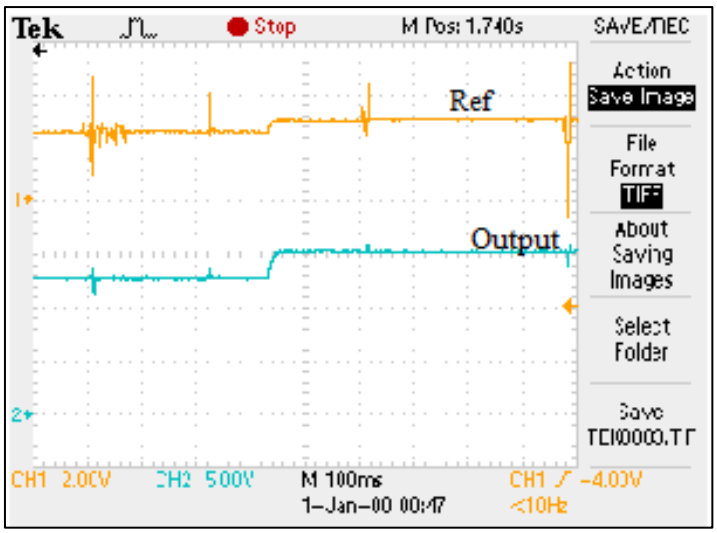


Fig. 2.16(b): Experimental results for step change in reference.

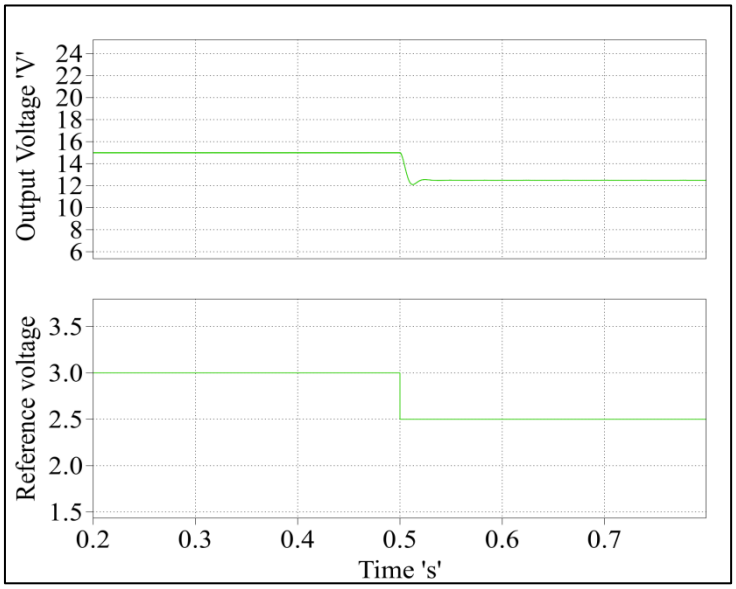


Fig. 2.16(c): Simulation result for step change in reference.

The main benefit of this new converter in comparison with [28] are less number of components for same voltage gain, hence size and cost is less. The other advantages are high efficiency, continuous input current, common ground for input, load and switch, and low voltage stress on C_1 capacitor. The active switch and diode stress for both of these converters is same.

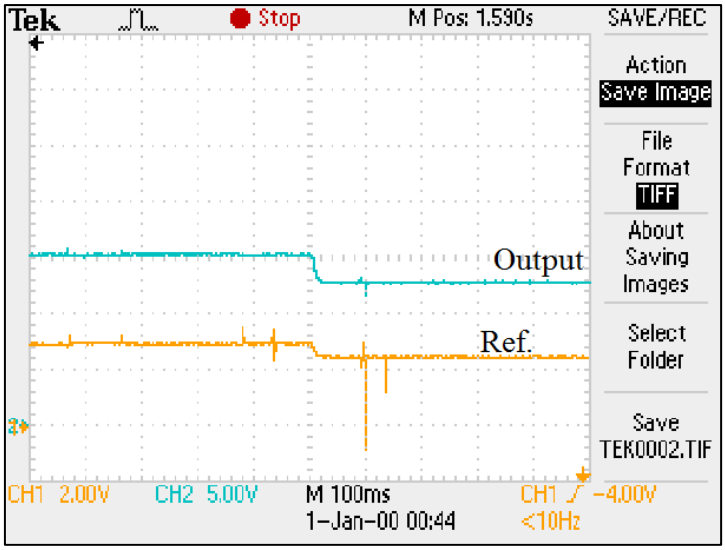


Fig. 2.16(d): Experimental results for step change in reference.

Table 2.2: Comparison between proposed converter and converter of **[28]**.

Converter	Converter of [28]	Proposed converter
Voltage gain	$(1-D)/(1-2D)$	$(1-D)/(1-2D)$
No. of passive elements	6	4
No. of active switch	1	1
No. of diode	1	1
Continuous input current	No	Yes
Floating active switch	Yes	No
Common ground for source, load and switch	No	Yes
Voltage stress on active switch	$V_{in}/(1-2D)$	$V_{in}/(1-2D)$

Voltage stress on capacitors	$V_{C1}=V_{C2}=V_{Cf}=\frac{1-D}{1-2D}V_{in}$	$V_{C1}=\frac{D}{1-2D}V_{in}$, $V_{C0}=\frac{1-D}{1-2D}V_{in}$
Voltage stress across diode	$V_{in}/(1-2D)$	$V_{in}/(1-2D)$

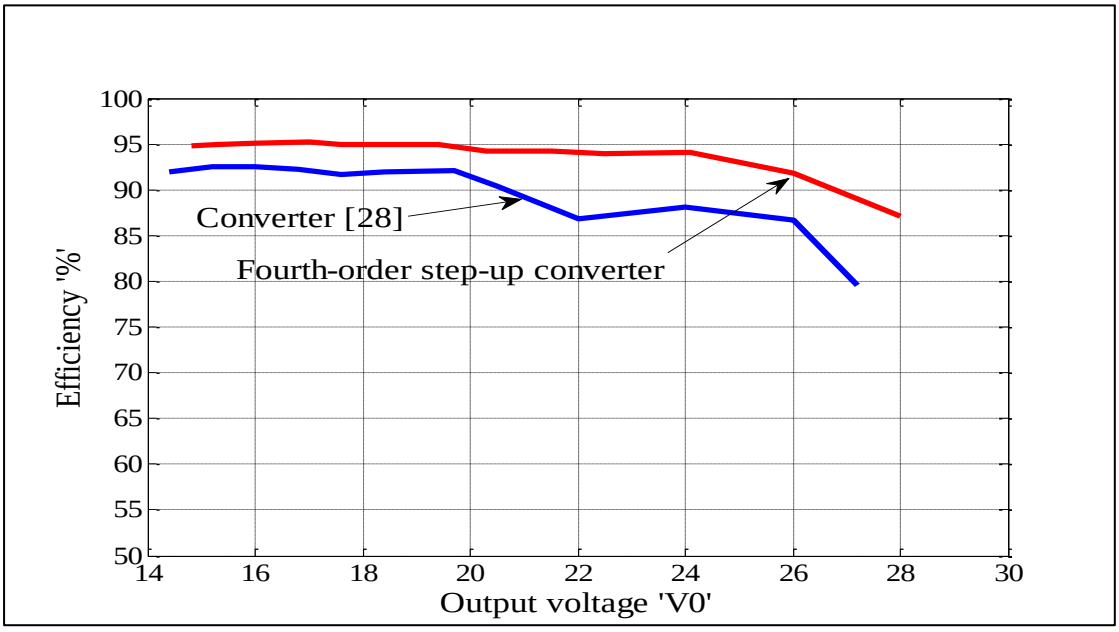


Fig. 2.17: Comparison of efficiency for different output voltage.

2.7 Conclusion

A detailed study of fourth order PWM DC-DC converter derived from quasi Z-source converter is presented in this chapter. Steady state expressions for inductor currents and capacitor voltages and also DC voltage transfer ratio for an ideal converter has been derived for converter operating in CCM and DCM. A boundary condition for CCM/DCM has been derived. Expressions for power loss in each of the components have been derived for non-ideal converter operating in CCM. Based on power loss, expression for efficiency has been derived. A small signal model for the converter is obtained and controller design is also discussed. Average current mode control is used for control of output voltage. Prototypes of converter and controller are built in the

laboratory, and used to verify theoretical analysis and simulation results. Experimental results fairly match with the theoretical results.

Compare to PWM Z-source DC-DC converter topology, this topology has lower number of parts for the same DC voltage conversion ratio, continuous input current and non-floating switch. Further, if one goes above D=0.5, one can get an inverted output. However, switches should be four quadrant switches for both inverting and non-inverting operation.

Chapter 3

Fourth order PWM DC-DC converter: Two Variations

3.1 Introduction

In the second chapter, fourth order step-up PWM DC-DC converter is studied in detail. This chapter discusses its two variations namely tapped inductor based fourth order DC-DC converter and coupled inductor based fourth order DC-DC converter. The purpose of introducing tapped inductor is to increase the voltage gain of the converter. The purpose of coupled inductor based converter is to minimize the input current ripple. This chapter is divided in two parts. First part discusses about tapped inductor based fourth order converter and second part discusses about coupled inductor based fourth order converter.

3.1 Tapped-inductor Quasi-z-source Based PWM DC-DC converter

3.1.1 Introduction

It is a well-known fact that tapped inductor can be used to increase or decrease the voltage gain substantially. It is possible due to turns ratio in the tapped inductor. The fourth-order step-up PWM DC-DC converter topology of chapter 2 can be modified using a tapped inductor to obtain a higher voltage gain for a given duty ratio. Without sacrificing all other advantages of fourth-order step-up PWM DC-DC converter. The voltage gain of this configuration is not only depends upon duty ratio but it also depends upon turns ratio of tapped inductor. The turns ratio of tapped-inductor plays a very important role for high step-up operation, the voltage gain of the converter can be enhance by increasing the turns ratio ($N=N_2/N_1$) of the tapped-inductor.

Figure 3.1.1 shows the circuit configuration of tapped-inductor quasi-z-source DC-DC converter. The inductor L_2 is tapped- inductor and both part are wound on same core, the inductance of primary part of tapped-coupled inductor is L_{21} and the inductance of secondary inductor is L_{22} with number of turns N_1 and N_2 respectively.

3.1.2 Operating principle of the converter

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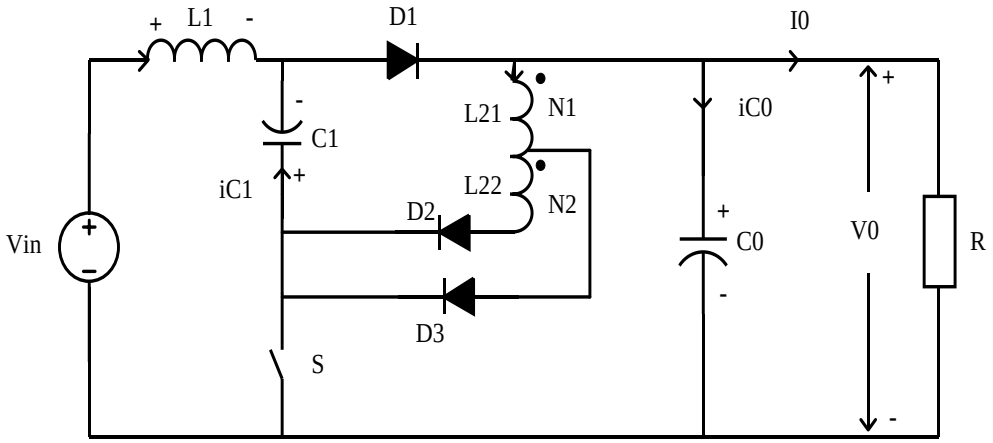


Fig.3.1.1:Tapped-inductor QZS DC-DC Converter.

The operating principle of the converter is that during switch-on inductor magnetic energy increases and it is released during switch-off period to charge capacitor and supply to the load resistance.

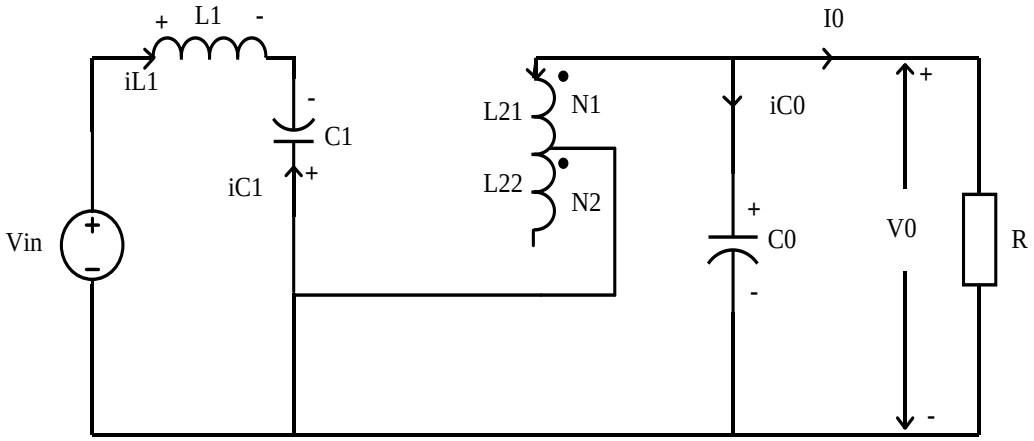


Fig. 3.1.2: Equivalent circuit of converter for switch-ON duration.

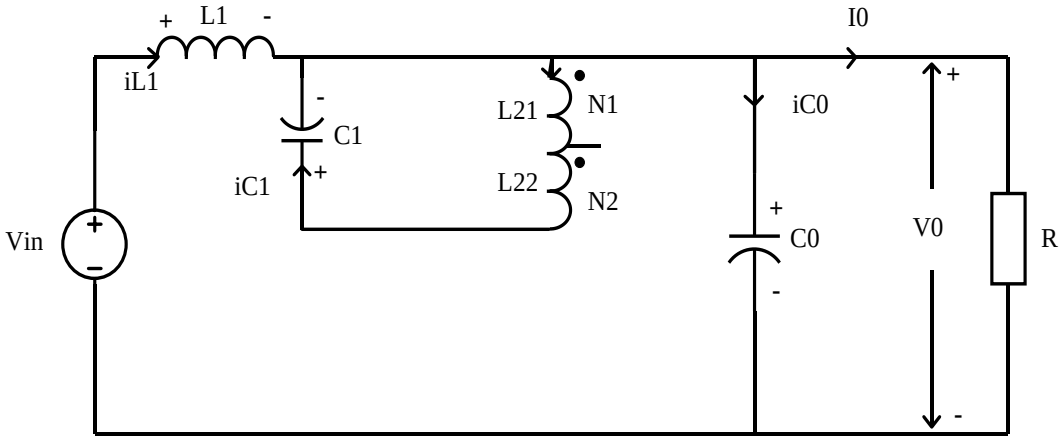


Fig. 3.1.3: Equivalent circuit of converter for switch-OFF duration.

To simplify the circuit analysis, the following conditions are assumed.

1) Capacitors, inductors and resistors are linear and frequency independent.
2) The coupling coefficient 'k' of tapped inductor is one.
3) Switching frequency is much higher than the natural frequency of converter.
4) Converter operates in continuous conduction mode.

The converter has two switching conditions in one operating period, and the corresponding equivalent circuit is shown in Fig.3.1.2 and Fig.3.1.3. The key waveforms of the converter are as depicted in Fig. 3.1.4.

Switch-ON:

The active switch S turns ON at time $\mathbf{t_0}$. The inductors L_1 and L_{21} are charged linearly, causing their current i_1 and i_2 increases linearly with the slopes proportional to voltage across them as shown in Fig.3.1.4. The voltage across inductor L_1 is equals to $V_{in}+V_{C1}$ and the voltage across inductor L_{21} is equals to V_{C0}. The diode D_1 and D_3 are OFF due to reverse bias voltages across them. The differential equations for this duration can be expressed in matrix form as equation (3.1.4).

Switch-OFF:

The switch S turns OFF and diode D_1 and D_2 turns ON for this duration. The inductors L_1 transfers energy to the output capacitor and load R. The inductor L_2 transfers its energy to charge capacitor C_1. So the inductor currents i_1 and i_2 decreases with different slopes in this duration. The voltage stress of the active switch S equals to V_0+V_{C1}. The diode D_2 gets reverse biased in this duration. The differential equations for this duration can be expressed in matrix form as equation (3.1.5).

3.1.3 Steady state analysis of the converter

The capacitor voltages v_{C1}, v_{C0}, inductor current i_{L1} and flux φ are chosen as state variables. The state variables are given in state vector x (t) as

$$x(t) = \begin{bmatrix} i_{L1}(t) & \phi(t) & v_{C1}(t) & v_{C0}(t) \end{bmatrix}^T \tag{3.1.1}$$

Where, φ(t) is the flux through the core of tapped-inductor L_2.
The converter has one independent input V_{in}. Hence the input vector is

$$u(t) = \begin{bmatrix} v_{in}(t) \end{bmatrix} \tag{3.1.2}$$

Since output voltage is already in state variable matrix, hence output vector consist only input current and it can be given as

$$y(t) = \begin{bmatrix} i_{in}(t) \end{bmatrix} \tag{3.1.3}$$

when switch S is ON, the converter equivalent circuit can be shown as in Fig. 3.1.2. The differential equations for this duration can be described as

$$K\dot{x} = A_1 x + B_1 u \tag{3.1.4}$$

Where

$$K = \begin{pmatrix} L_1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_0 \end{pmatrix}$$

and

$$A_1 = \begin{pmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & \frac{1}{N_1} \\ -1 & 0 & 0 & 0 \\ 0 & \frac{-N_1}{L_{21}} & 0 & \frac{-1}{R} \end{pmatrix} \qquad B_1 = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

when switch S is OFF, the converter equivalent circuit for this duration can be shown as in Fig. 3.1.3 and the differential equations for this duration can be given as

$$K\dot{x} = A_2 x + B_2 u \tag{3.1.5}$$

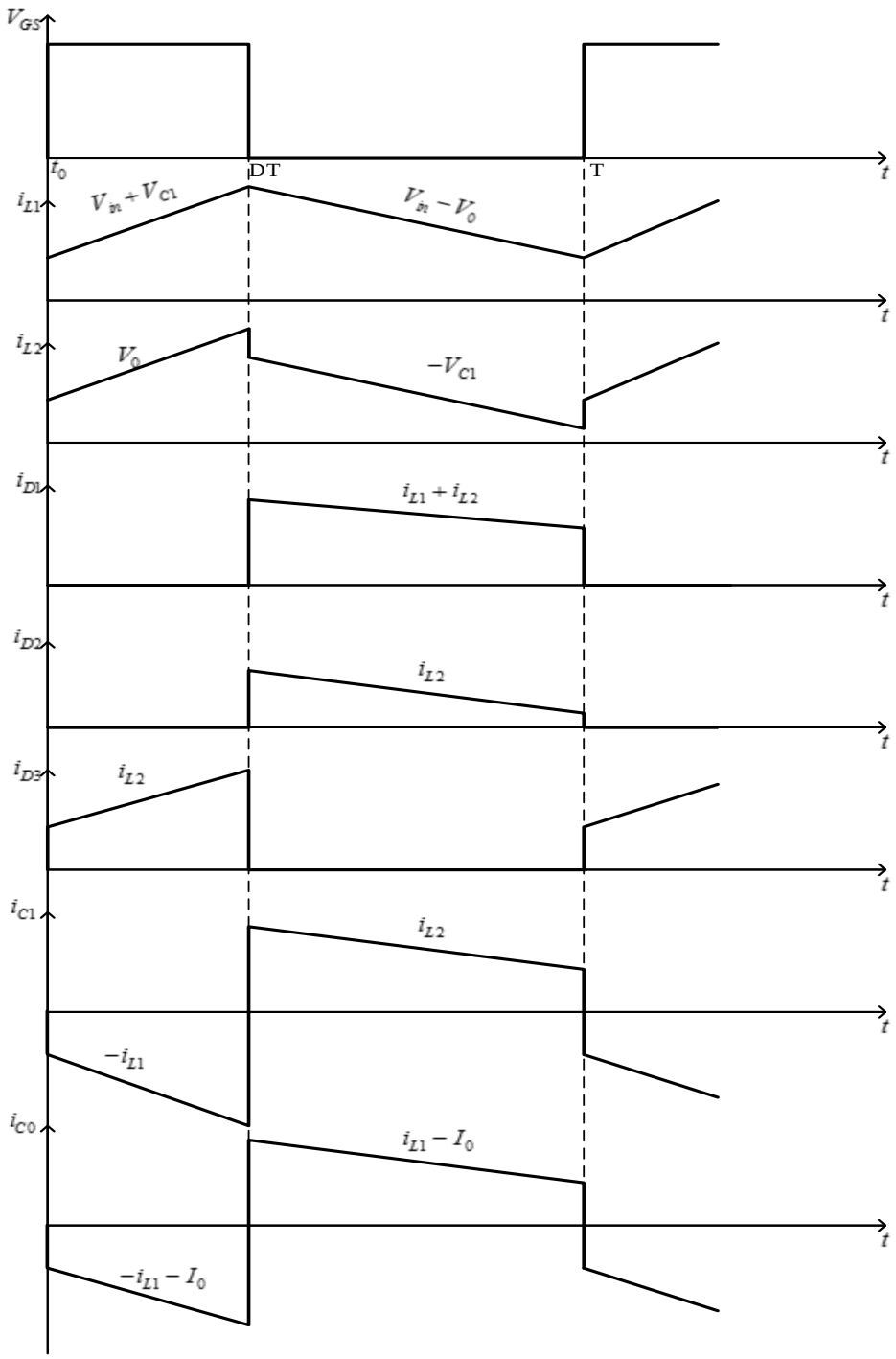


Fig. 3.1.4(a). Key current waveforms of converter.

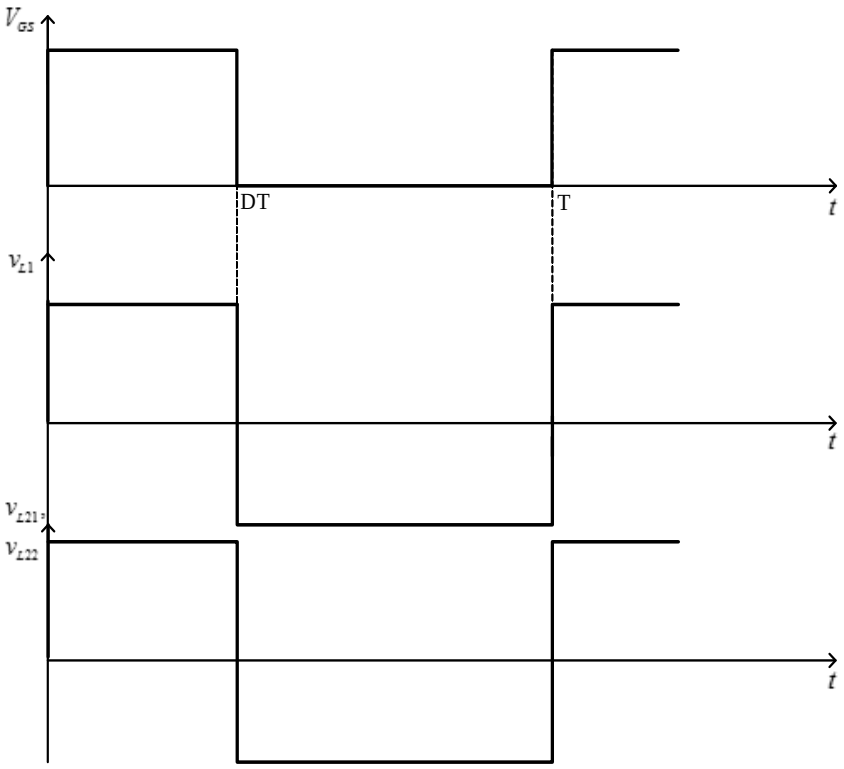


Figure 3.1.4(b): Key voltage waveforms of converter.

Where,

$$A_2 = \begin{pmatrix} 0 & 0 & 0 & -1 \\ 0 & 0 & \dfrac{-1}{N_1 + N_2} & 0 \\ 0 & \dfrac{N_1 + N_2}{L_2} & 0 & 0 \\ 1 & 0 & 0 & \dfrac{-1}{R} \end{pmatrix} \quad \text{and} \quad B_2 = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

Averaging of matrix

$$A = DA_1 + D'A_2 \quad \text{and} \quad B = DB_1 + D'B_2 \tag{3.1.6}$$

Where, D is duty ratio and D'= 1- D. Using equation (3.1.6), A and B can be given as

$$A=\begin{pmatrix} 0 & 0 & D & -D' \\ 0 & 0 & \dfrac{-D'}{N_1+N_2} & \dfrac{D}{N_1} \\ -D & \dfrac{N_1+N_2}{L_2}D' & 0 & 0 \\ D' & \dfrac{-N_1 D}{L_{21}} & 0 & \dfrac{-1}{R} \end{pmatrix} \quad \text{and} \quad B=\begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

The steady state averaged model for dc values can be given by expression (3.1.7)

$$0 = AX + BU \tag{3.1.7}$$

Where, X = equilibrium (dc) state vector and U = equilibrium (dc) input vector
Equation (3.1.7) can be solved to find the equilibrium state as

$$X = -A^{-1}BU \tag{3.1.8}$$

Using equation (3.1.8), the dc steady-state values of input current, flux through the core of inductor L_2 and voltage across capacitor C_1 and capacitor C_0 can be derived as

$$I_{L1} = I_{in} = \frac{(1-D)V_0}{(1-2D-nD^2)R} \tag{3.1.9}$$

$$\Phi = \frac{L_2 DD'V_{in}}{R(N_1+N_2)(1-2D-nD^2)^2} \tag{3.1.10}$$

$$V_{C1} = \frac{(1+N)DV_{in}}{(1-2D-nD^2)} \tag{3.1.11}$$

$$V_0 = V_{C0} = \frac{(1-D)V_{in}}{(1-2D-nD^2)} \tag{3.1.12}$$

From output voltage expression (3.1.12), the variation in output voltage with duty ratio for different values of turn ratio **n** can be plotted as in Fig.3.1.5.
For continuous input current DCM condition can be defined as i_{L1} is continuous and

i_{L2} reduces to zero during switch-off period.

The boundary condition for tapped-inductor quasi z-source based converter is derived by using flux expressions.

The maximum value of flux during switch-ON can be given by

$$\hat{\phi} = \phi_0 + \frac{V_0 DT}{N_1} \tag{3.1.13}$$

At boundary condition between continuous and discontinuous conduction mode, ripple in flux can be derived from expression (3.1.13) as

$$\Delta\phi = \frac{V_0 DT}{N_1} \tag{3.1.14}$$

At boundary $$\Phi - \frac{\Delta\phi}{2} = 0 \tag{3.1.15}$$

From equation (3.1.10), (3.1.14) and (3.1.15), the boundary operating condition between CCM and DCM can be derived and given as

$$K_c = (1+n)(1-2D-nD^2) \tag{3.1.16}$$

Where $K_c = 2L_2/RT$.

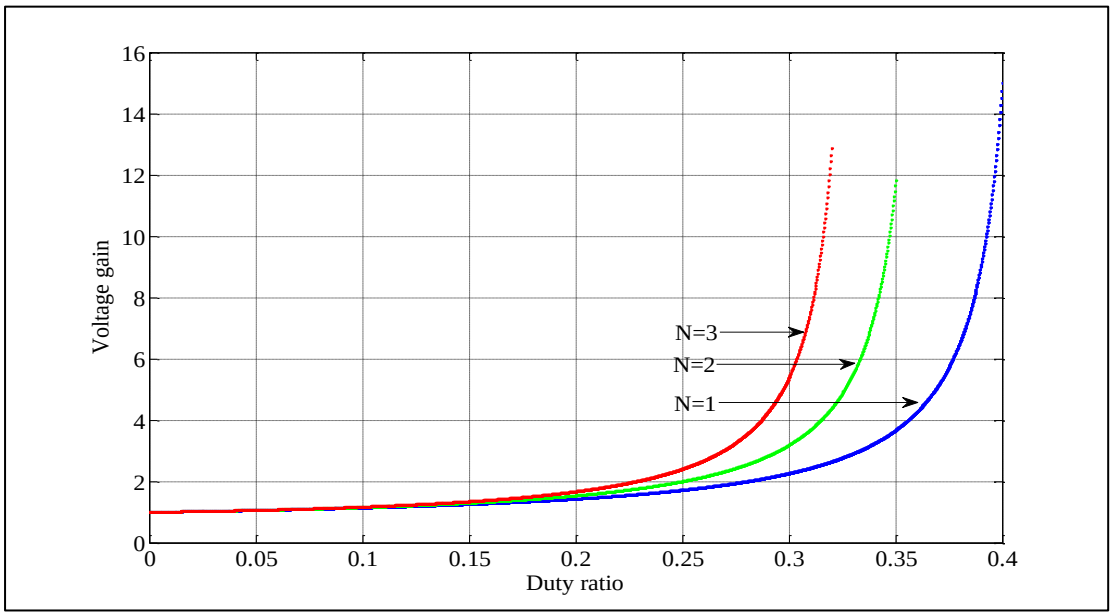


Fig.3.1.5: Variation in voltage gain for different values of **n.**

3.1.4 Design of converter elements

The passive elements are designed on the basis of switching frequency and voltage and current ripple relations.

The voltage ripple relations are given by

$$\Delta v_{C1} = \frac{(1-D)DTV_0}{(1-2D-nD^2)C_1R} \tag{3.1.17}$$

$$\Delta v_{C0} = \frac{(1-D-nD^2)DTV_0}{(1-2D-nD^2)C_0R} \tag{3.1.18}$$

The current ripple relation is

$$\Delta i_{L1} = \frac{(1-D+nD-nD^2)DTV_{in}}{(1-2D-nD^2)L_1} \tag{3.1.19}$$

The variation in capacitor voltages are

$$\delta v_{C1} = \frac{\Delta v_{C1}/2}{V_{C1}} = \frac{(1-D)T}{2(1+n)(1-2D-nD^2)C_1R} \tag{3.1.20}$$

$$\delta v_{C0} = \frac{\Delta v_{C0}/2}{V_{C0}} = \frac{(1-D-nD^2)DT}{2(1-2D-nD^2)C_0R} \tag{3.1.21}$$

The variations in inductor current are

$$\delta i_{L1} = \frac{\Delta i_{L1}/2}{I_{L1}} = \frac{(1-D+nD(1-D))DTR(1-2D-nD^2)}{2(1-D)^2 L_1} \tag{3.1.22}$$

For continuous conduction mode the current ripple is smaller than dc value of inductor current, hence

$$L_1 > \frac{(1-D+nD(1-D))DTR(1-2D-nD^2)}{2(1-D)^2} \tag{3.1.23}$$

And from equation (3.1.16)

$$L_2 > \frac{TR(1-2D-nD^2)(1+n)}{2} \tag{3.1.24}$$

3.1.5 Performance analysis of the converter

Figure 3.1.6 is the tapped-inductor QZS based boost converter with parasitic elements. In Fig. 3.1.6 r_{L1}, r_{L21} and r_{L22} are the ESR of inductors L_1, L_{21} and L_{22} respectively. The on-state resistance of MOSFET 'S' is represented by r_{DS}, r_{C1} and r_{C0} are ESR of capacitors C_1 and C_0. Resistances r_{D1}, r_{D2} and r_{D3} are on-state ESR of diodes; V_{FD1}, V_{FD2} and V_{FD3} are forward voltage drops of diodes D_1, D_2 and D_3 respectively. V_{in} is input voltage, V_0 is output voltage and R is load resistance. The details of parameters used for analysis of performance are given in table 3.1.1.

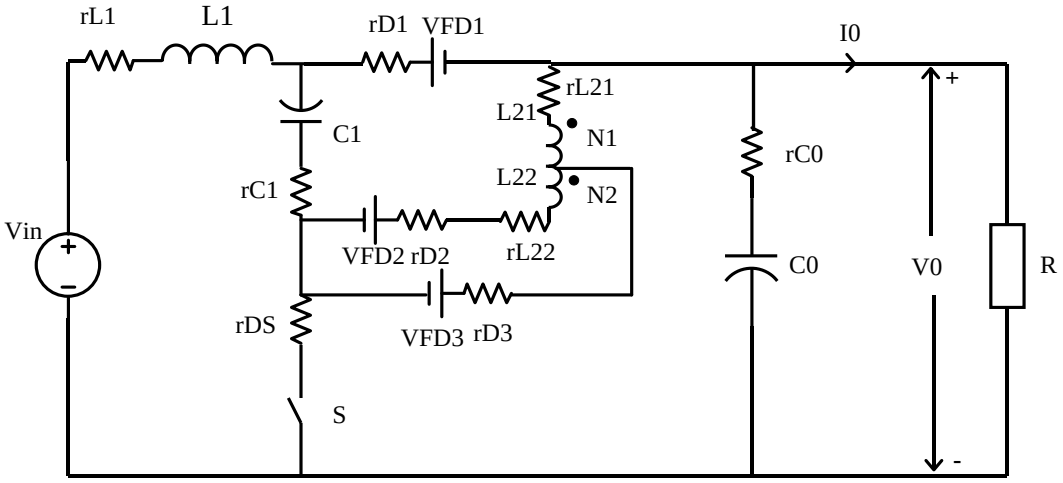


Fig.3.1.6: Equivalent circuit of converter with non-idealities.

The currents in inductors L_{21} during switch-on and in inductor L_2 during switch-off can be given as

$$I_{L21} = \frac{N_1 \Phi}{L_{21}} \tag{3.1.25}$$

$$I_{L2} = \frac{(N_1 + N_2)\Phi}{L_2} \tag{3.1.26}$$

The state space average model of tapped-inductor converter with parasitic elements is can be given as in (3.1.27)-(3.1.30).

$$\dot{i_{L1}}(t)=\frac{1}{L_1}\left\{V_{in}+d\left(v_{C1}-i_{L1}\left(r_{L1}+r_{C1}+r_S\right)\right)+\left(1-d\right)\left(\begin{array}{l}-V_{FD1}-i_{L1}\left(r_{L1}+r_{D1}\right)-r_{C0}\\ \left(I_{L1}-\frac{v_{C0}}{R+r_{C0}}\right)-v_{C0}-\\ \frac{\phi}{L_2}\left(N_1+N_2\right)r_{D1}\end{array}\right)\right\} \tag{3.1.27}$$

$$\dot{\phi}(t)=\frac{d}{N_1}\left(v_{C0}-\left(\frac{\phi N_1}{L_{21}}\left(r_{L21}+r_{D2}+r_{C0}+r_S\right)\right)-V_{FD2}-\frac{r_{C0}v_{C0}}{R+r_{C0}}\right)+\frac{\left(1-d\right)}{N_1+N_2}$$
$$\left(-v_{C1}-V_{FD1}-V_{FD3}-\frac{\phi\left(N_1+N_2\right)}{L_2}\left(r_{L2}+r_{D3}+r_{D1}+r_{C1}\right)-i_{L1}r_{D1}\right) \tag{3.1.28}$$

$$\dot{v_{C1}}(t)=\frac{1}{C_1}\left(-di_{L1}+\frac{\left(1-d\right)\phi\left(N_1+N_2\right)}{L_2}\right) \tag{3.1.29}$$

$$\dot{v_{C0}}(t)=\frac{1}{C_0}\left\{-\frac{v_{C0}}{R+r_{C0}}-d\,\frac{\phi\left(N_1\right)}{L_{21}}+\left(1-d\right)i_{L1}\right\} \tag{3.1.30}$$

In equations (3.1.27)-(3.1.30), **d** is average duty cycle.

After solving equations (3.1.27)-(3.1.30), Voltage gain of converter and input current can be given by equations (3.1.31) and (3.1.32) as

$$\frac{V_0}{V_{in}}=\left\{\begin{array}{l}\left\{1-\frac{D'V_{FD1}}{V_{in}}\right\}\left(g\left(i\cdot l+c\cdot j\right)\right)+\left\{-\frac{D'\left(V_{FD1}+V_{FD3}\right)}{V_{in}\left(N_1+N_2\right)}-\frac{DV_{FD2}}{V_{in}N_1}\right\}\\ \frac{\left(-c\left(i\cdot l+c\cdot j\right)\right)}{Y}\end{array}\right\} \tag{3.1.31}$$

$$I_{L1} = I_{in} = \left\{ \frac{\left\{V_{in} - D'V_{FD1}\right\}\left(-g \cdot i \cdot k\right) + \left\{ -\frac{D'\left(V_{FD1} + V_{FD3}\right)}{\left(N_1 + N_2\right)} - \frac{DV_{FD2}}{N_1} \right\}}{Y} \right\} \quad (3.1.32)$$

Where, details of coefficient Y and other coefficients used in equations (3.1.31) and (3.1.32) are given in appendix-B.

From equation (3.1.31), the voltage gain variation of the non-ideal converter with variation in duty ratio for **n**=1 and **n**=1.5 can be plotted as in Fig.3.1.7, this result is for load resistance of 100 Ω.

Table 3.1.1: Parameters used for analysis and simulation

S.No.	Parameters	Value
1.	Input voltage	15V
2.	Inductor L_1, L_2,L_{21} (for **n**=1) and L_{21} (for **n** =1.5)	1.1mH,2.6mH, 666.8µH and 426.5µH
3.	Capacitor C_1, C_2	88.6µF, 180µF
4.	r_{L1}, r_{L2}, r_{L21}(**n** =1) and r_{L21}(**n** =1.5)	0.114Ω, 0.196Ω, 0.098Ω and 0.0784Ω
5.	r_{C1}, r_{C2}	0.152 Ω,0.076 Ω
6.	V_{FD1}, V_{FD2}, V_{FD3}	1.05V each
7.	Load resistance R	50Ω ,100 Ω,200 Ω
8.	Switch resistance r_{DS}	0.044 Ω

The efficiency of the converter can be given by

$$\eta = \frac{V_0^{\,2} / R}{V_{in} I_{in}} \quad (3.1.33)$$

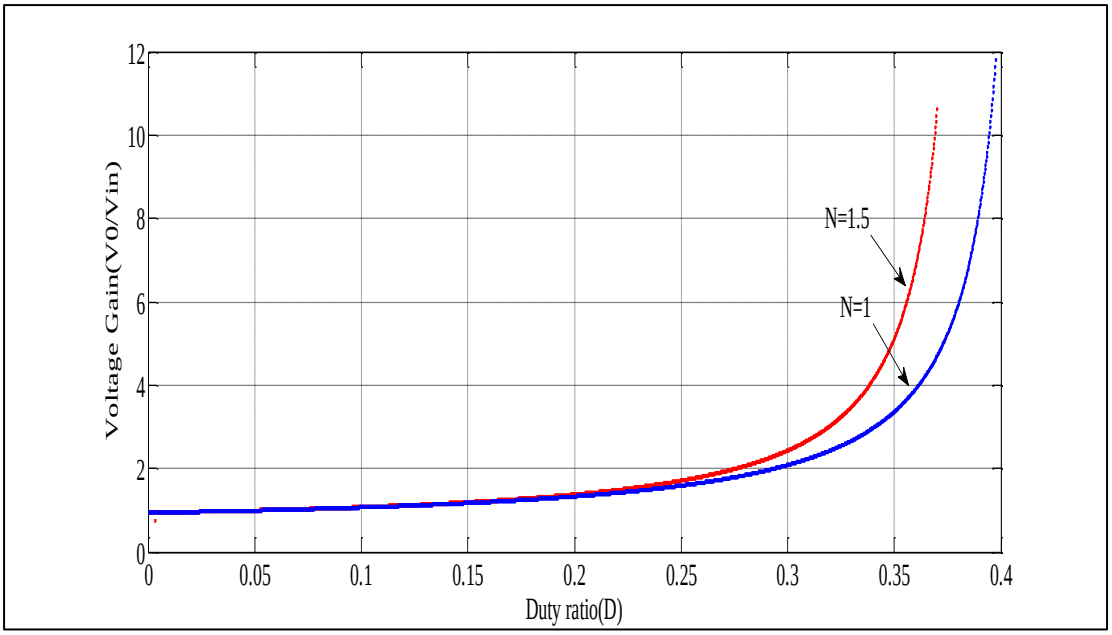


Fig. 3.1.7: Gain of non-ideal converter for different values of **n**.

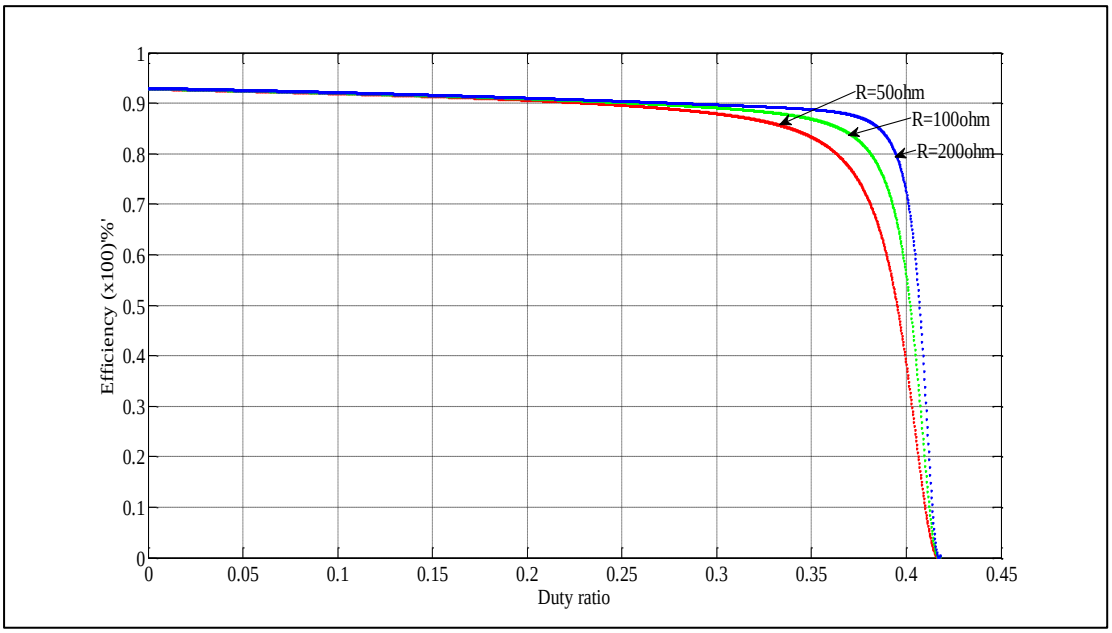


Fig.3.1.8: Variation in efficiency with duty ratio for different loads.

By using equations (3.1.31) - (3.1.33) and converter parameters, variation in efficiency with duty ratio can be plotted as in Fig.3.1.8 for different load resistances.

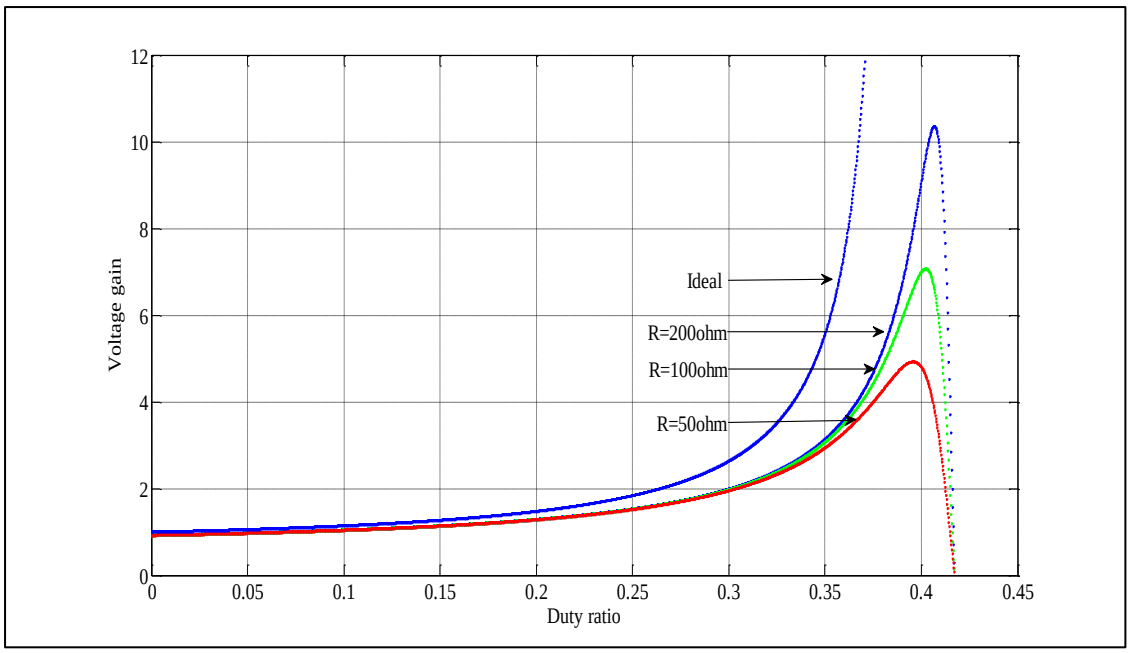


Fig.3.1.9: Variation in gain with duty ratio for different loads.

Figure 3.1.9 shows variation in voltage gain with change in duty ratio for different load resistances.

3.1.6 Simulation and experimental results

A laboratory prototype was built of the proposed converter. The details of specifications of experimental set-up are same as given in table 3.1.1,

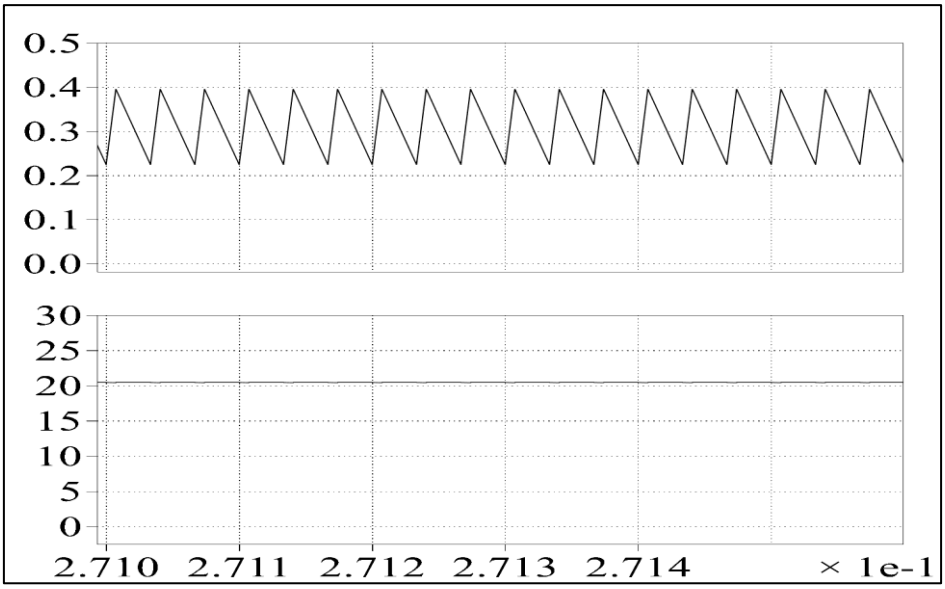


Fig. 3.1.10(a): Simulation results of input current and output voltage for D=0.2 and **n** =1.

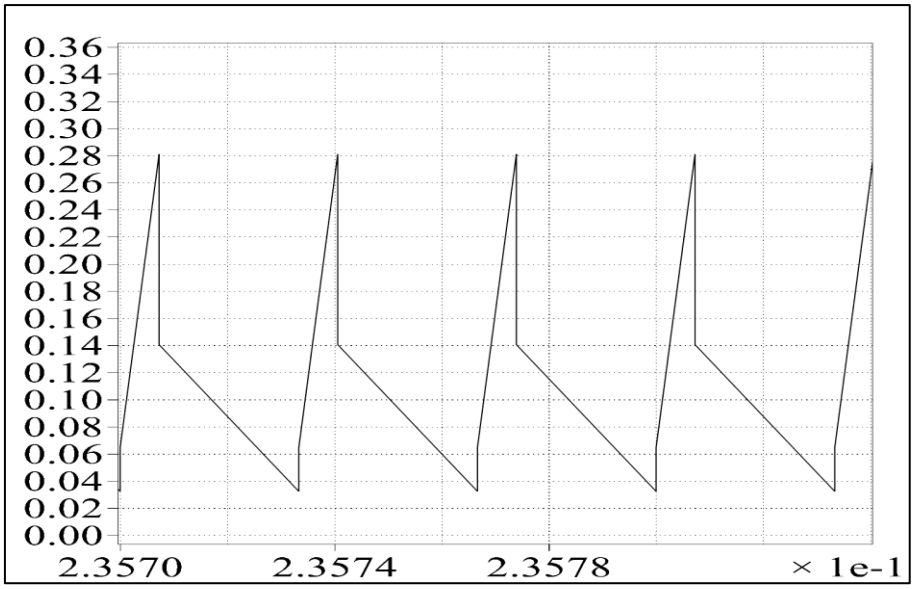


Fig. 3.1.10(b): Simulation results of tapped-inductor current and for D=0.20 and **n** =1.

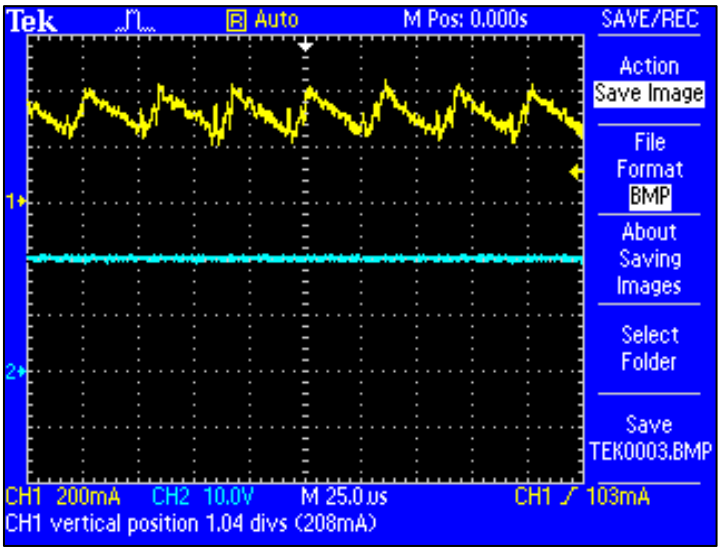


Fig. 3.1.11(a): Experimental results of input current for D=0.2 and **n** =1.

and the measured value of coupling coefficient is 0.9875. MOSFET IRF540 is used for active switch and MUR460 diodes are used as passive switches. The converter operates in open loop configuration and PWM IC TL494 is used for switching pulse generation at 30 KHz frequency. Tektronix A622 current probe is used to measure current of the converter. The converter circuit for similar parameters with parasitic components was simulated in PLECS PLEXIM software. Figure 3.1.10 and Fig. 3.1.11 shows simulation results and experimental results of i_{L1}, i_{L2} and output voltage for D=0.2, R=100Ω and turns ratio **n** =1

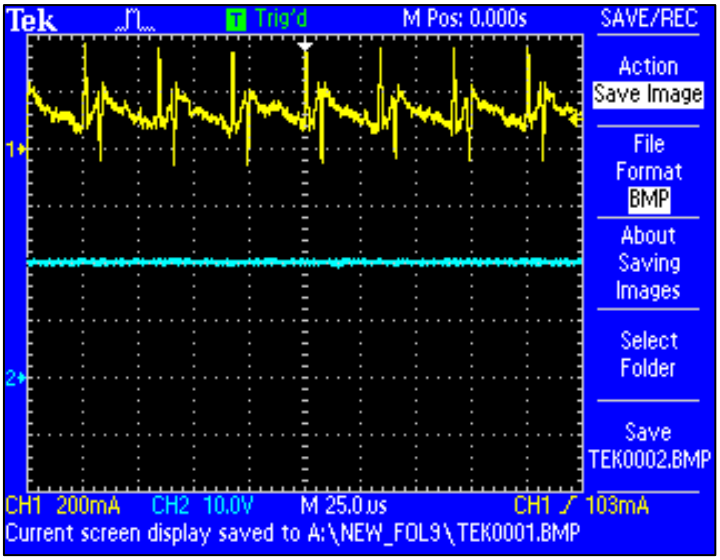


Fig.3.1.11(b):Experimental results for tapped-inductor current for D=0.2 and **n** =1.

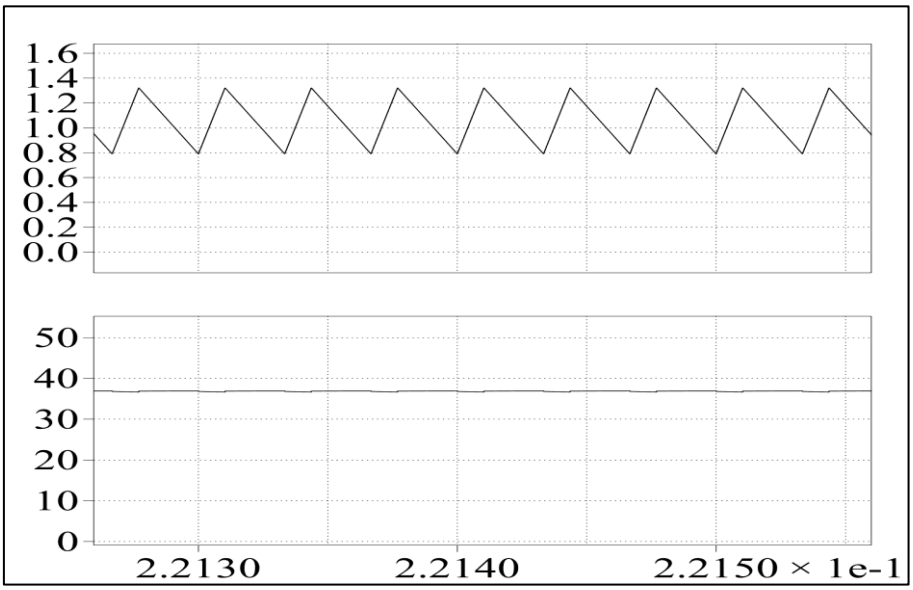


Fig. 3.1.12(a): Simulation results of input current and output voltage for D=0.30 and **n** =1.5.

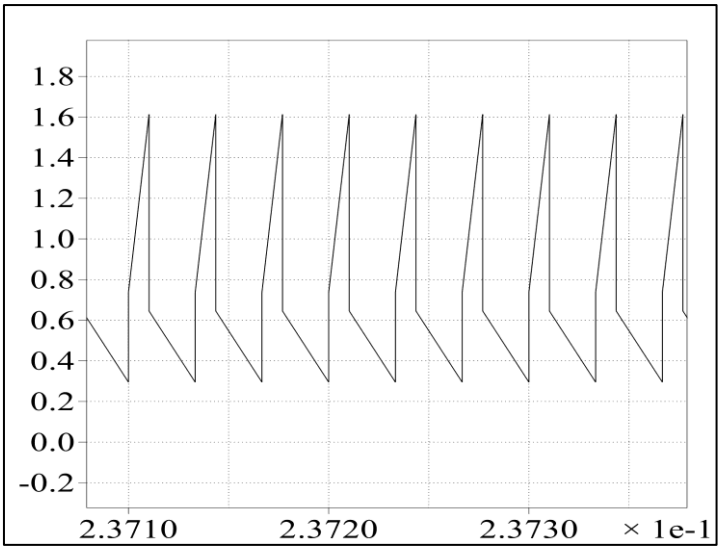


Fig.3.1.12(b):Simulation results of tapped-inductor current for D=0.3 and **n** =1.5.

Figure 3.1.12 and Fig. 3.1.13 show simulation and experimental results of output voltage, input current, tapped-inductor current for duty ratio D=0.30, R=100Ω and turns ratio **n** =1.5 respectively. Figure 3.1.14 and Fig. 3.1.15 present experimental and theoretically expected results for output voltage and efficiency respectively for turn ratio **n** =1.

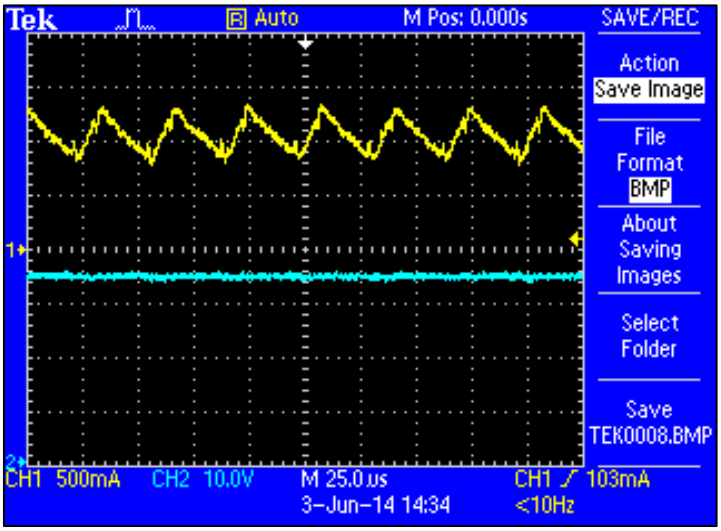


Fig. 3.1.13(a): Experimental results of input current and output voltage for D=0.3 and **n** =1.5.

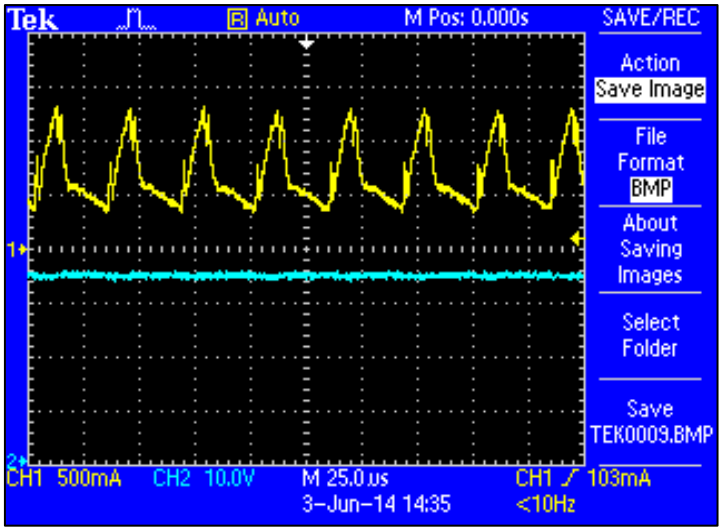


Fig. 3.1.13(b): Experimental results of tapped-inductor current for D=0.3 and **n** =1.5.

The difference in experimental and expected results at higher duty ratio in Fig. 3.1.14 and Fig. 3.1.15 can be attributed to losses in core of inductors and stray element losses, which are not included in analysis.

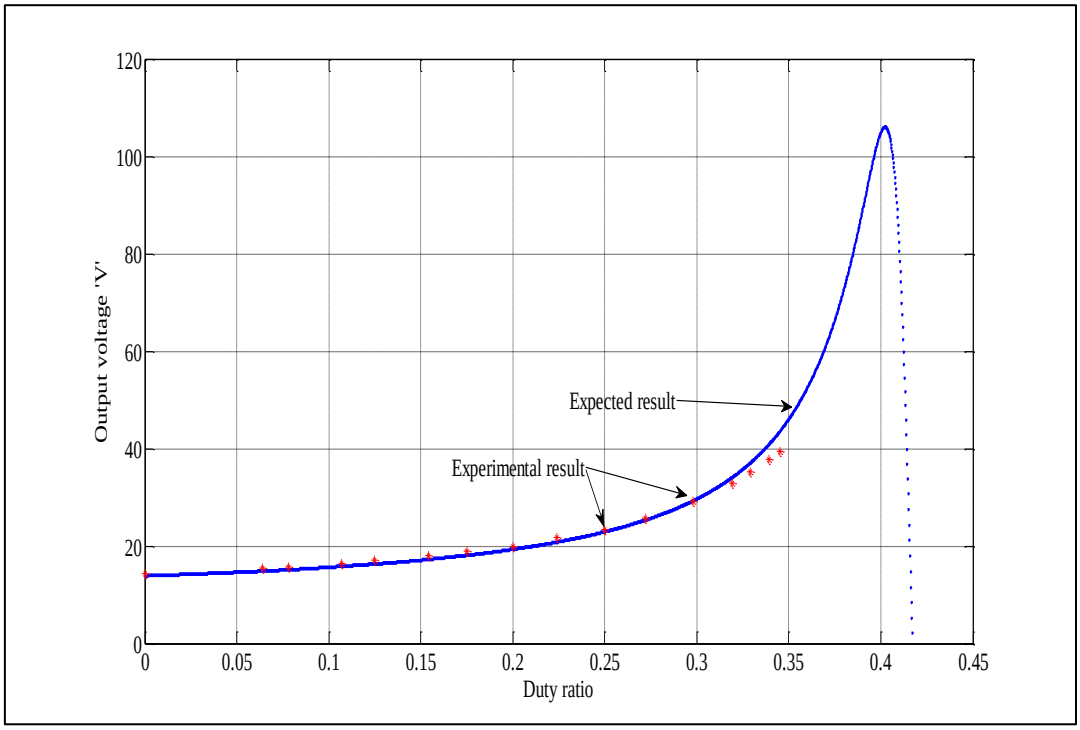


Fig. 3.1.14: Variation in output voltage with duty ratio for **n** =1.

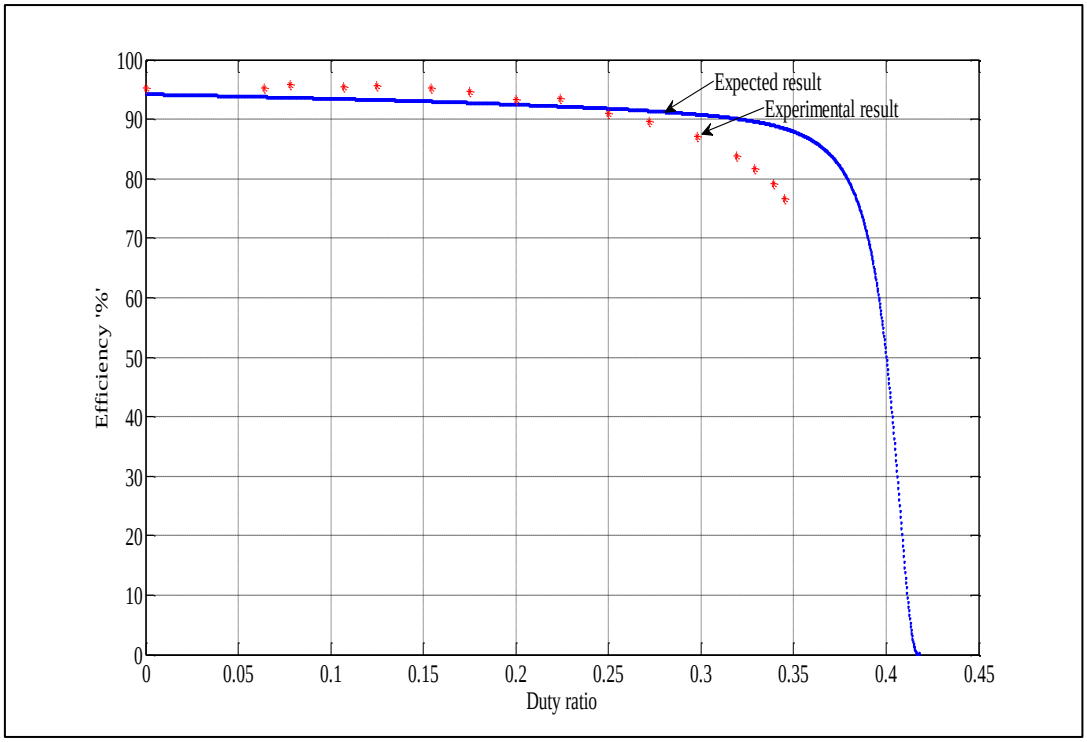


Fig. 3.1.15 : Variation in efficiency with duty ratio for **n** =1.

3.1.7 Conclusion

This part of chapter has introduced an extension of fourth order step-up DC-DC converter using a tapped-inductor. A detailed steady state analysis and key waveforms of converter has been presented. Voltage gain and efficiency variation with duty ratio of tapped-inductor based converter including non-idealities has been analyzed. A voltage transfer function that considers non-idealities has been derived.

A prototype circuit of tapped-inductor based converter is put into operation in laboratory. Theoretical analysis and experimental results illustrates that, the voltage gain of tapped-inductor based converter is higher than the conventional boost converter and fourth-order step-up DC-DC converter for the same duty ratio. The voltage gain of the converter can be further increased by increasing turns ratio. The disadvantage of the converter is higher voltage stress over main switch.

3.2 A step-up PWM DC-DC converter with zero input current ripple

3.2.1 Introduction

The renewable energy sources such as photovoltaic and fuel cells are low voltage energy sources, therefore high gain DC-DC converter is required to link this voltage to inverter. In such applications another requirement is to drain continuous current with minimum ripple [50], [51]. In order to minimize input current ripple input filter or large value of inductor can be used but this solution increases size and weight, which is quite unacceptable. The coupled inductor based converter can greatly reduce current ripple, with the advantage of decrease in size and weight of converter. Therefore converter with both features of high gain with minimum input ripple will find more suitable for above mentioned applications.

A coupled inductor based converter with minimum ripple input current is introduced here. Theoretically ripple can be minimized to zero, but it is difficult to achieve in

practice. The proposed converter is derived from fourth-order step-up PWM DC-DC converter, which is shown in Fig. 3.2.1.

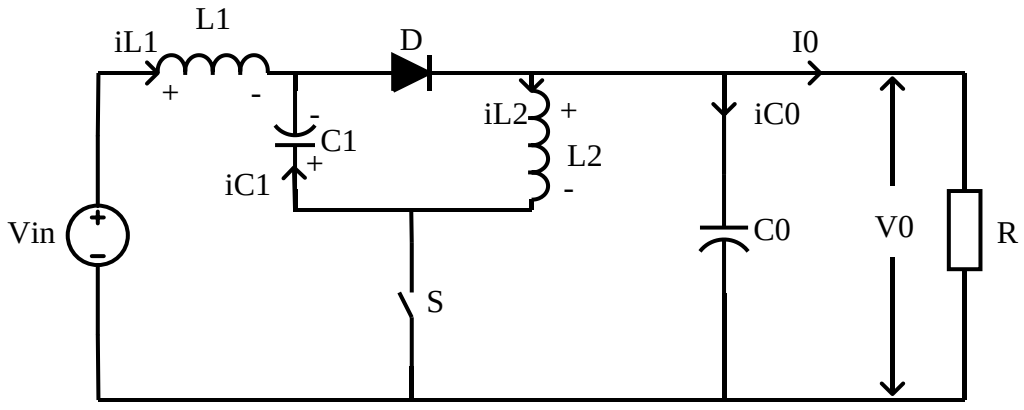


Fig.3.2.1: Fourth-order step-up PWM DC-DC converter.

3.2.2 Coupled inductor based high step-up converter

In fourth-order step-up converter of Fig. 3.2.1, voltage across inductors L_1 and L_2 during switch ON and switch OFF period can be given as:

When switch-ON

$$v_{L1} = V_{in} + v_{C1} \quad , \qquad v_{L2} = v_{C0} \tag{3.2.1}$$

When switch-OFF

$$v_{L1} = V_{in} - v_{C0} \quad , \qquad v_{L2} = -v_{C1} \tag{3.2.2}$$

In steady state voltage across capacitors can be given as

$$V_{C1} = \frac{V_{in} D}{(1-2D)} \ , \qquad V_0 = V_{C0} = \frac{V_{in}(1-D)}{(1-2D)} \tag{3.2.3}$$

From equations (3.2.1)-(3.2.3) the voltage waveform can be drawn as in Fig. 3.2.2.

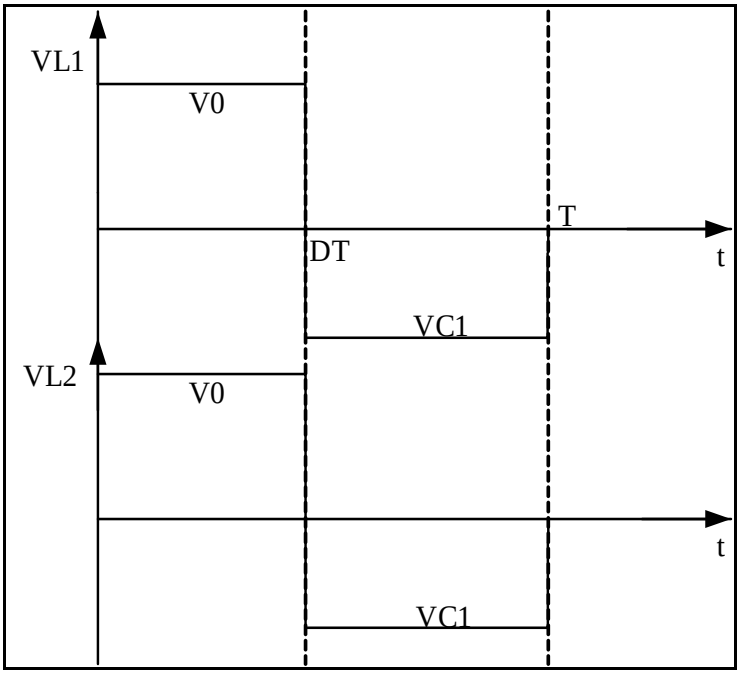


Fig.3.2.2: Inductor's voltage waveform.

As shown in Fig. 3.2.2, the voltage waveforms of the two inductors are identical in step-up PWM DC-DC converter, so it becomes clear that the two inductors L_1 and L_2 can be coupled without affecting the basic conversion property [52] as shown in Fig. 3.2.3 with the direction of coupling.

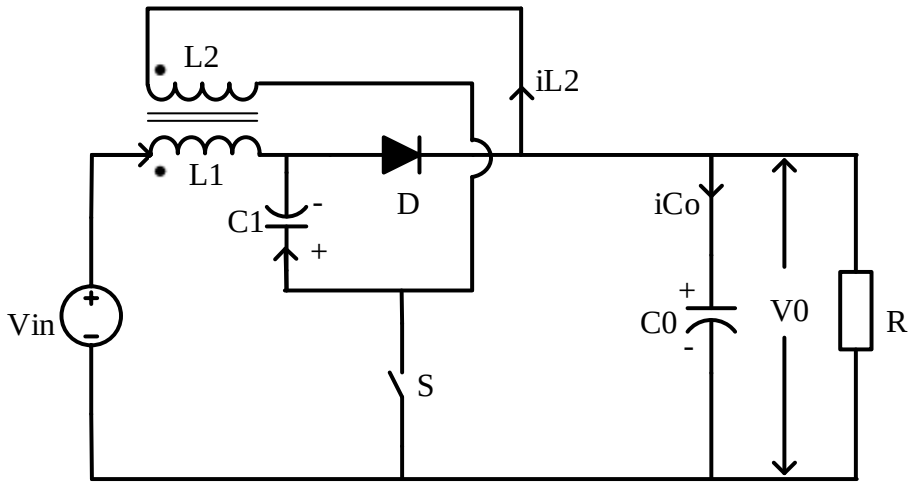


Fig.3.2.3: Coupled-inductor based step-up converter.

Figure 3.2.3 shows coupled inductor based high step-up converter. Instead of the two cores for two uncoupled inductors, a single core coupled inductor is used in this converter, thus reduction in size, weight and number of components can be additional advantage of this new converter. Besides these advantages additional and more important advantages in terms of performance are obtained, particularly in the substantial reduction in input current ripple.

3.2.2.1 Steady state analysis of the converter

Referring to Fig. 3.2.3, the switch S is operating with switching frequency fs=1/T and with duty ratio D=Ton/T. where Ton is switch-ON time for switch S.

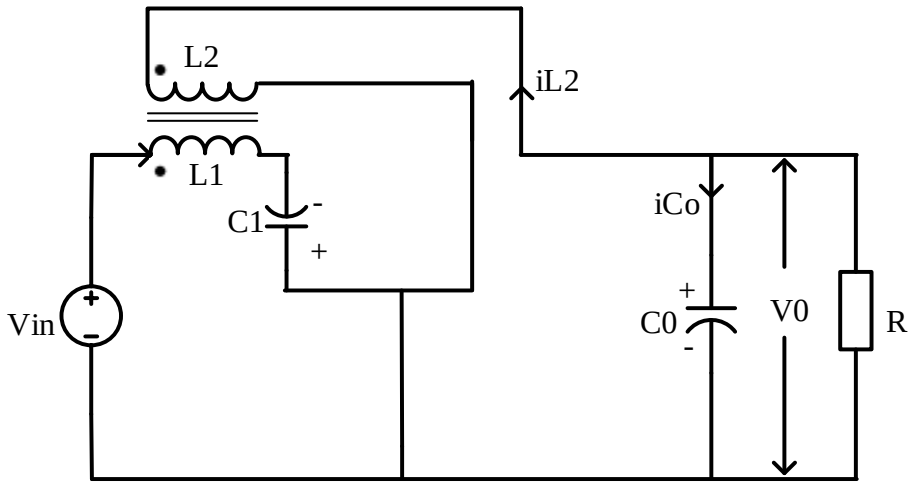


Fig. 3.2.4(a): Equivalent circuit of converter for switch-ON.

Figure 3.2.4(a) and Fig. 3.2.4(b) shows converter equivalent circuit for switch-ON and switch-OFF duration.

When switch-ON : In this duration equivalent circuit of converter is as shown in Fig. 3.2.4(a), the active switch S is ON and diode remain in OFF condition due to reverse bias voltage. The voltage across inductors and current through capacitors can be given as

$$L_1 \dot{i}_{L1} + M \dot{i}_{L2} = V_{in} + v_{C1} \ , \ L_2 \dot{i}_{L1} + M \dot{i}_{L1} = v_{C2} \ , \ C_1 \dot{v}_{C1} = -i_{L1}, \qquad (3.2.4)$$

$$C_0 \dot{v}_{C0} = -i_{L2} - \frac{v_{C0}}{R}$$

When switch-OFF: In this duration equivalent circuit of converter is as shown in Fig. 3.2.4(b), the switch S is OFF and diode is in ON condition. The voltage across inductors and current through capacitors can be given as

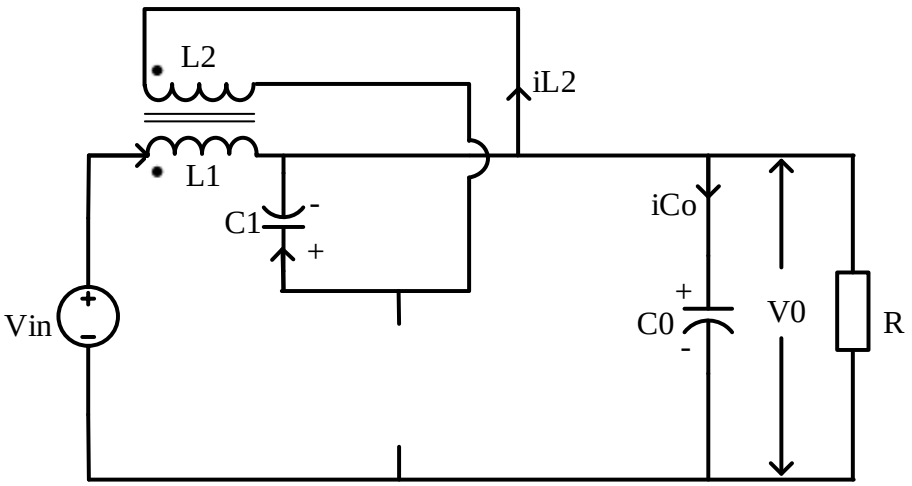


Fig. 3.2.4(b): Equivalent circuit of converter for switch-OFF.

$$L_1 \dot{i}_{L1} + M \dot{i}_{L2} = V_{in} - v_{C0} \ , \ L_2 \dot{i}_{L1} + M \dot{i}_{L1} = -v_{C1} \ , \ C_1 \dot{v}_{C1} = i_{L2}, \qquad (3.2.5)$$

$$C_0 \dot{v}_{C0} = i_{L1} - \frac{v_{C0}}{R}$$

Equation (3.2.4) can be written in matrix form as $K\dot{x} = A_1 x + B_1 u$,

where

$$K = \begin{pmatrix} L_1 & M & 0 & 0 \\ M & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_0 \end{pmatrix} \quad A_1 = \begin{pmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & \frac{-1}{R} \end{pmatrix} \quad B_1 = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

Equation (3.2.5) can be written in matrix form as $K\dot{x} = A_2 x + B_2 u$

Where

$$A_2 = \begin{pmatrix} 0 & 0 & 0 & -1 \\ 0 & 0 & -1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & \frac{-1}{R} \end{pmatrix} \qquad B_2 = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

Averaging of matrix

$$A = DA_1 + D'A_2 \quad \text{and} \quad B = DB_1 + D'B_2 \tag{3.2.6}$$

where D is duty ratio and D'= 1- D. Using (3.2.6) A and B can be given by

$$A = \begin{pmatrix} 0 & 0 & D & -D' \\ 0 & 0 & -D' & D \\ -D & D' & 0 & 0 \\ D' & -D & 0 & \frac{-1}{R} \end{pmatrix} \qquad B = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

The steady state averaged model for dc values can be given by expression

$$0 = AX + BU \tag{3.2.7}$$

where X= equilibrium (dc) state vector and U= equilibrium (dc) input vector.
Equation (3.2.7) can be solved to find the equilibrium state as

$$X = -A^{-1}BU \tag{3.2.8}$$

Using equation (3.2.8), the dc steady-state values of input current, current through inductor L_2 and voltage across capacitor C_1 and capacitor C_0 can be derived as

$$I_{L1} = \frac{V_{in}(1-D)^2}{R(1-2D)^2} = \frac{I_0(1-D)}{(1-2D)} \tag{3.2.9}$$

$$I_{L2} = \frac{V_{in}(1-D)D}{R(1-2D)^2} = \frac{I_0 D}{(1-2D)} \tag{3.2.10}$$

$$V_{C1} = \frac{DV_{in}}{(1-2D)} \tag{3.2.11}$$

$$V_{C0} = V_0 = \frac{(1-D)V_{in}}{(1-2D)} \tag{3.2.12}$$

These steady state values (3.2.9)-(3.2.12) are same as for QZS based converter of chapter 2. Hence the inductor coupling does not affect the steady state gain.
Using equation (3.2.4), the expression of inductor L_1 current for switch-ON duration can be written as

$$i_{L1} = \frac{V_{in}}{L_1}t + \frac{v_{C1}}{L_1}t - \frac{Mi_{L2}}{L_1} \tag{3.2.13}$$

The peak value of current i_{L1} can be given as

$$\hat{i}_{L1} = \frac{V_{in} + v_{C1}}{L_1}DT - \frac{Mi_{L2}}{L_1} \tag{3.2.14}$$

Similarly from equation (3.2.5), the expression of inductor L_2 current for switch-ON duration can be given as

$$i_{L2} = \frac{v_{C0}}{L_2} t - \frac{M i_{L1}}{L_2} \tag{3.2.15}$$

Using equation (3.2.14), equation (3.2.13) can be written as

$$i_{L1} = \frac{1}{\left(1 - \frac{M^2}{L_1 L_2}\right)} \left[\left(\frac{V_{in} + v_{C1}}{L_1} \right) t - \left(\frac{v_{C0} M}{L_1 L_2} \right) t \right] \tag{3.2.16}$$

And peak value of inductor L_1 current can be given as

$$\hat{i}_{L1} = \frac{1}{\left(1 - \frac{M^2}{L_1 L_2}\right)} \left[\left(\frac{V_{in} + v_{C1}}{L_1} \right) DT - \left(\frac{v_{C0} M}{L_1 L_2} \right) DT \right] + i_{L1}(0) \tag{3.2.17}$$

So peak to peak values are

$$\Delta i_{L1} = \frac{1}{\left(1 - \frac{M^2}{L_1 L_2}\right)} \left[\left(\frac{V_{in} + v_{C1}}{L_1} \right) DT - \left(\frac{v_{C0} M}{L_1 L_2} \right) DT \right] \tag{3.2.18}$$

$$\Delta i_{L2} = \frac{1}{\left(1 - \frac{M^2}{L_1 L_2}\right)} \left[\left(\frac{v_{C0}}{L_2} \right) DT - \left(\frac{\left(V_{in} + v_{C1}\right) M}{L_1 L_2} \right) DT \right] \tag{3.2.19}$$

Whereas, peak to peak value of current in inductor L_1 and L_2 are $\frac{V_{in} + v_{C1}}{L_1} DT$ and $\frac{v_{C0}}{L_2} DT$ respectively for fourth-order step-up PWM DC-DC converter of chapter 2.

So from equations (3.2.18) and (3.2.19), it can be concluded that current ripples get reduced for positive mutual coupling coefficient.

3.2.3 Analysis of current ripple

3.2.3.1 Current ripple in continuous conduction mode

In order to find the inductor L_1 and L_2 current waveforms, it is sufficient to analyze the equivalent model of the coupled inductor as shown in Fig.3.2.5.

The two leakage inductances L_{l1} and L_{l2} in Fig.3.2.5 are defined as

$$L_{l1} = L_1 - M \text{ and } L_{l2} = L_2 - M$$

Here L_1 and L_2 are self- inductance and M is mutual inductance, which can be defined as

$$M = k\sqrt{L_1 L_2} \tag{3.2.20}$$

where **'k'** is coupling coefficient.

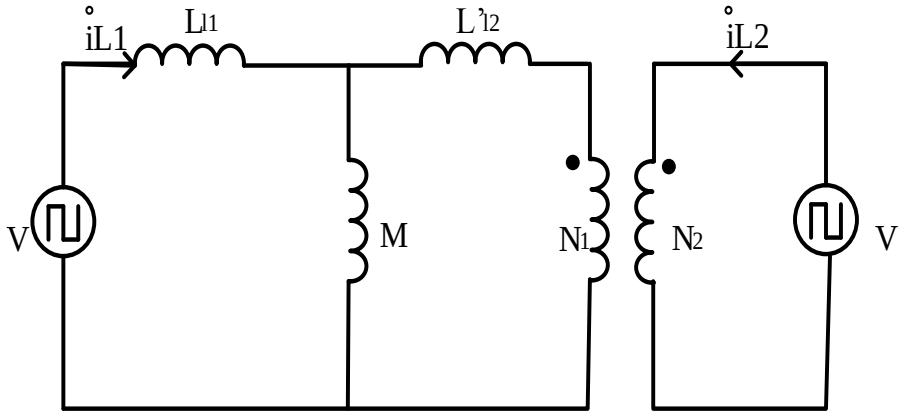


Fig. 3.2.5: Equivalent circuit of coupled inductor.

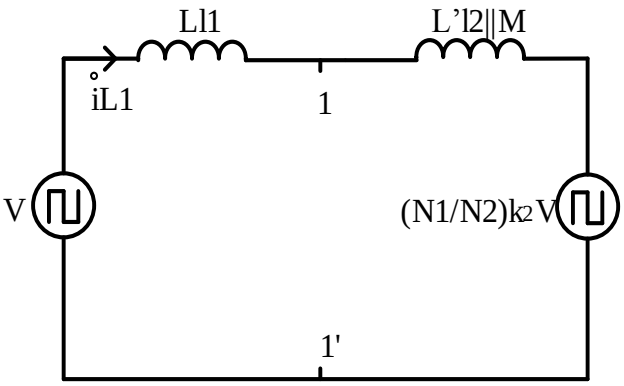


Fig. 3.2.6(a): Simplified equivalent circuit of coupled inductor referred to primary side.

To calculate current ripple in $\mathbf{i_{L1}}$ the portion of circuit to the right of leakage inductance L_{l1} is replaced with Thevenin's equivalent circuit as shown right side of the points 1-1' in Fig. 3.2.6(a).

$$V_{2TH} = \frac{N_1}{N_2}\frac{M}{M + L'_{l2}}V = \frac{N_1}{N_2}k_2 V \tag{3.2.21}$$

Where, $\mathbf{k_2}$ is secondary coupling coefficient.

Thevenin's equivalent inductance can be given by

$$L_{2TH} = L'_{l2} \parallel M \tag{3.2.22}$$

Therefore current ripple through L1 is

$$i_{L1} = \left(1 - \frac{N_1}{N_2}k_2\right)\int \frac{V}{L_{l1} + L'_{l2} \parallel M}dt \tag{3.2.23}$$

Similarly current ripple can be determined by calculating Thevenin's equivalent circuit referred to secondary side as shown to the left of 2-2'of Fig. 3.2.6(b).

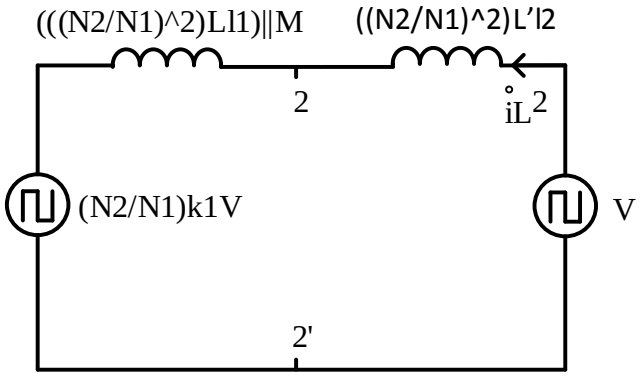


Fig. 3.2.6(b): Simplified equivalent circuit of coupled inductor referred to secondary side.

$$V_{1TH} = \frac{N_2}{N_1}\frac{M}{M + L_{l1}}V = \frac{N_2}{N_1}k_1 V \tag{3.2.24}$$

$$L_{1TH} = \left(\frac{N_2}{N_1}\right)^2 L_{l1} \parallel M \tag{3.2.25}$$

The equivalent circuit is shown in Fig. 3.2.6(b).

The current ripple through L_2 is

$$\dot{i}_{L2} = \frac{\left(1-\frac{N_2}{N_1}k_1\right)}{\left(\frac{N_2}{N_1}\right)^2}\int \frac{V}{L'_{l2}+L_{l1}\,||\,M}dt \qquad (3.2.26)$$

The expressions under integral sign are almost equal if M >> L_{l1}, L'_{l2}. Hence from (3.2.23) and (3.2.26) inductor current ripple expressions can be written as

$$\dot{i}_{L1} \propto \left(1-\frac{N_1}{N_2}k_2\right) \qquad \dot{i}_{L2} \propto \frac{\left(1-\frac{N_2}{N_1}k_1\right)}{\left(\frac{N_2}{N_1}\right)^2} \qquad (3.2.27)$$

Equation (3.2.27) represents normalized values of current ripple. From equation (3.2.27), it can be noticed that current ripples can be minimized to zero and can also become negative by adjusting turn ratio or coupling coefficient. For $\frac{N_1}{N_2}=\frac{1}{k_2}$ input current ripples become zero and for higher values of $\frac{N_1}{N_2}>\frac{1}{k_2}$ current ripples become negative. Similarly for $\frac{N_2}{N_1}=\frac{1}{k_1}$ current ripples of i_{L2} becomes zero.

3.2.3.2 Current ripple in discontinuous conduction mode

The main cause of DCM mode is due to unidirectional property of diode. When either of the two current minimum values reaches zero, no change occurs in converter operating mode. Further, it may be possible that one of the inductor current enters in negative region for some part of switching cycle. When sum of both inductor currents reaches zero and diode gets switch-off, results DCM mode. In this converter, both inductor currents goes in to DCM at same instant due to diode as shown in Fig. 3.2.7, so inductor voltage maintains proportionality regardless of operating mode as shown in Fig. 3.2.8. Hence, inductor current analysis given above is true for discontinuous current mode of operation.

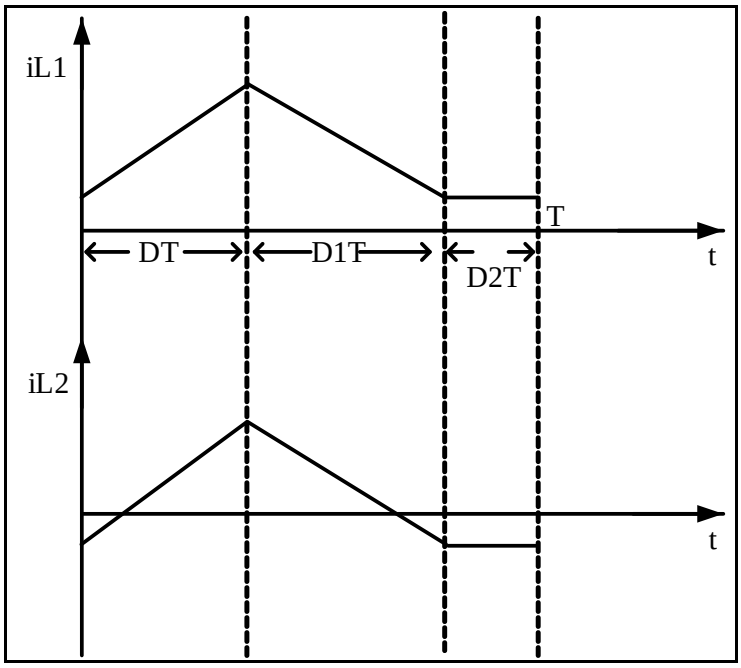


Fig.3.2.7: Inductor's current waveforms in DCM.

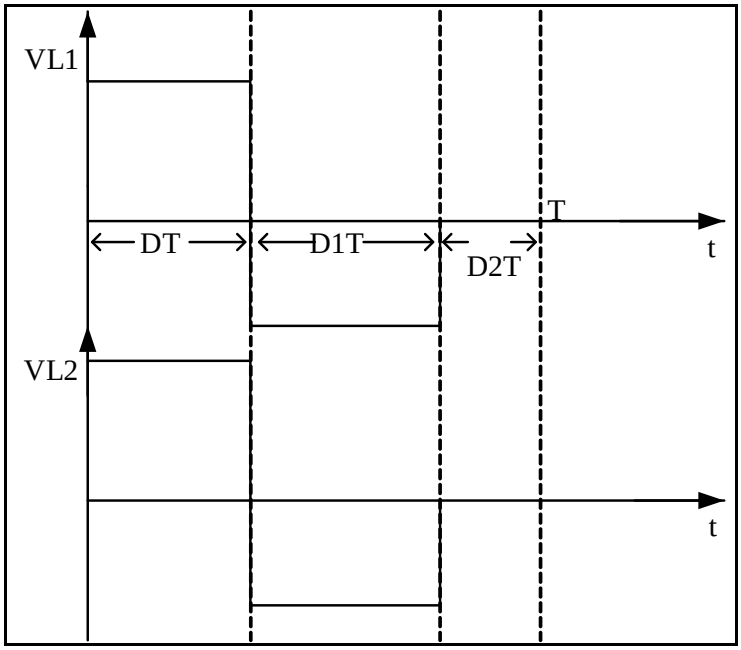


Fig.3.2.8: Inductor's voltage waveform for DCM.

3.2.4 Experimental set-up

The zero ripple condition derived from equation (3.2.27) can be achieved by either varying turns ratio or by varying coupling coefficient **k**. In practice it is not convenient to change turns ratio, so arrangement is made for the matching of coupling coefficient **k** with turns ratio by adjusting air-gap between coupled inductors.

An experimental set-up as shown in Fig. 3.2.9 is used to verify the steady state analysis and current ripple analysis of the proposed converter. As shown in Fig. 3.2.9 the coupled inductors are built on two UR- cores. The permeability of core material is equals to 2700. Each of the UR-core is wound with 22 SWG copper wire to form inductor and number of turns in inductor L_1 and L_2 are 55 and 36 respectively. The arrangement is made to varying air-gap between cores, the coupling coefficient **k** can be continuously changed over a wide range. For precise control of air-gap both UR-UR cores are mounted on separate micro-positioners as shown in photograph. The other details of the converter parameters are given in table 3.2.1.

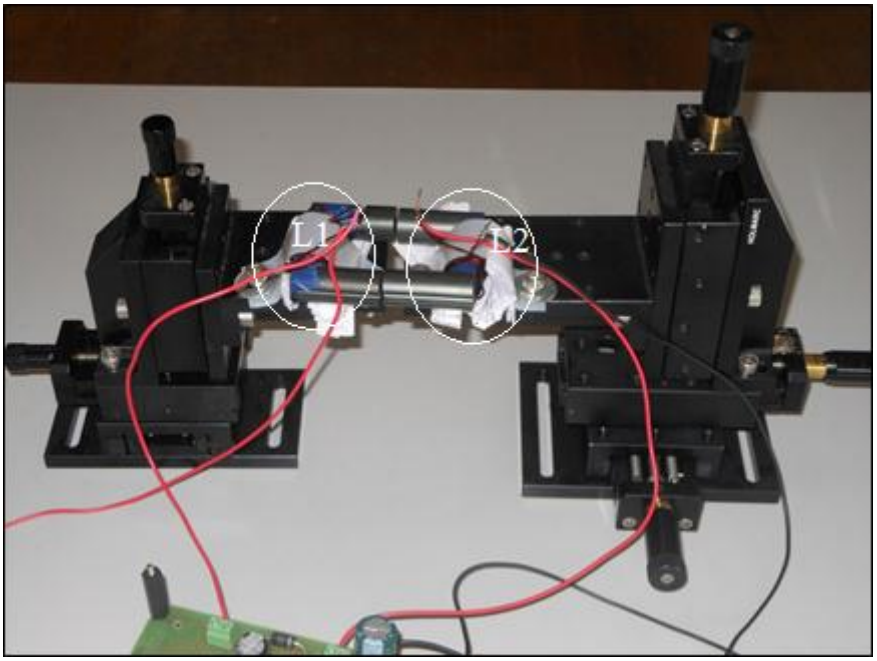


Fig.3.2.9: Experimental set-up for air-gap adjustment.

3.2.5 Simulation and experimental results

To validate theoretical analysis a laboratory prototype has been built. The converter parameters are listed in table 3.2.1. The converter operates in open-loop configuration and TL-494 is used for PWM pulse generation.

Table 3.2.1: Details of converter's parameters.

S.No.	Parameter	value
1	Input voltage	15 V
2	Switching frequency	20 KHz
3	Capacitor C_1,C_2,r_{C1}, r_{C2}	90.8µF,189.83µF,0.159Ω, 0.161Ω
4	Magnetic core	UR60/60
5	Number of turns N_1,N_2	55,36
6	MOSFET switch, R_{DS}	IRF540N,44mΩ
7	Diodes ,V_F	MUR460, 1.05V
8	Duty Cycle D	For CCM = 0.22, 0.29
9	Load resistance	For CCM:62Ω For DCM: 243 Ω

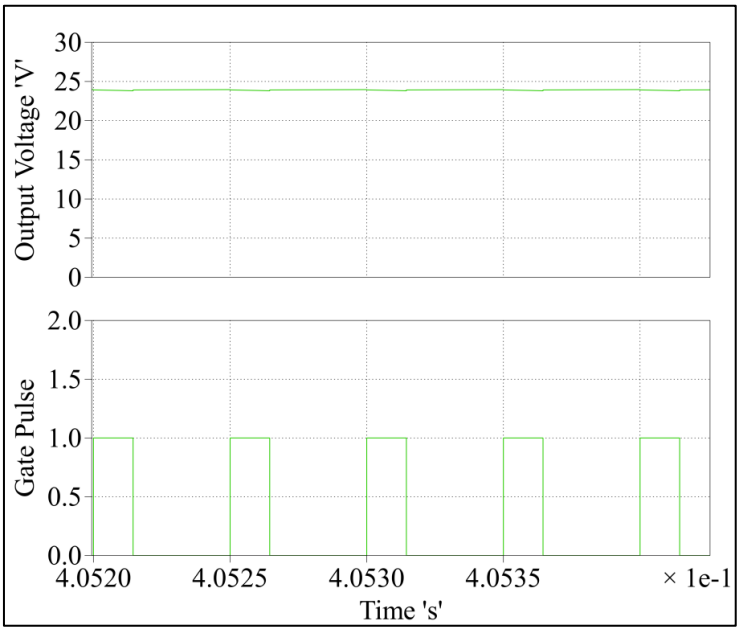


Fig. 3.2.10(a): Simulation result of output voltage for D=0.29 and Vin=15V.

Figure 3.2.10(a) and 3.2.10(b) shows simulation and experimental results of output voltage of the converter for duty ratio D=0.29. Simulation and experimental results for zero ripples in input current are shown in Fig. 3.2.11(a) and Fig. 3.2.11(b). The measured value of coupling coefficient for zero ripple in input current is **k=0.6585**,

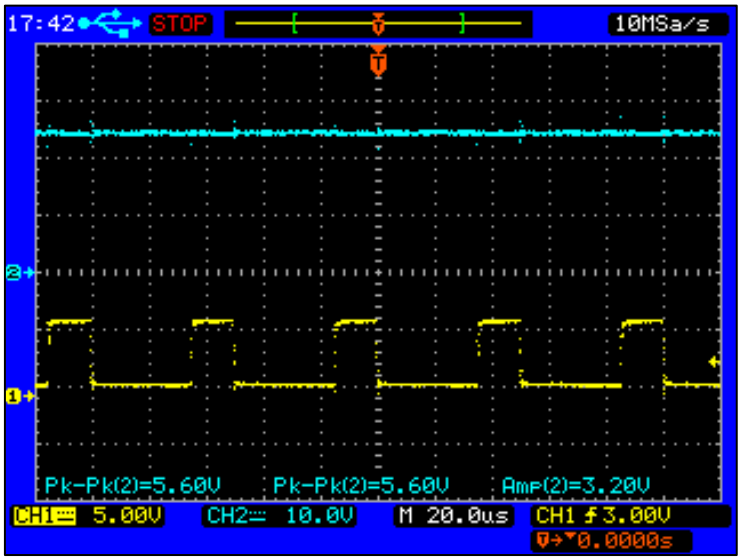


Fig. 3.2.10(b): Experimental result of output voltage for D=0.29 and Vin=15V.

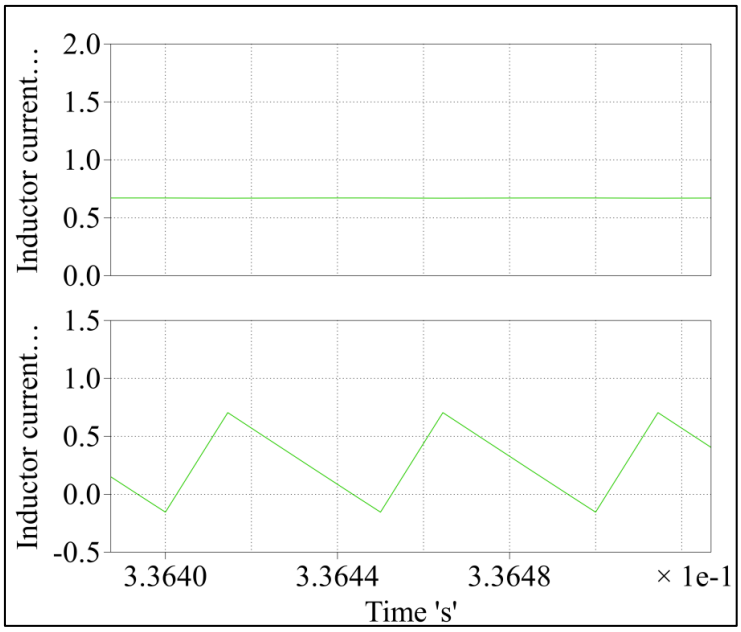


Fig. 3.2.11 (a): Simulation result for zero ripple input current.

which is very near to turn ratio N_2/N_1. The measured value inductance of inductor L_1=1mH and L_2=0.4mH. The calculated value of current ripples in inductor L_1 and inductor L_2 are -0.01A and 0.9A respectively. It can be observed from simulation and experimental results that the calculated values determined using equations (3.2.18) and (3.2.19) are approximately equal to simulation and experimental results.

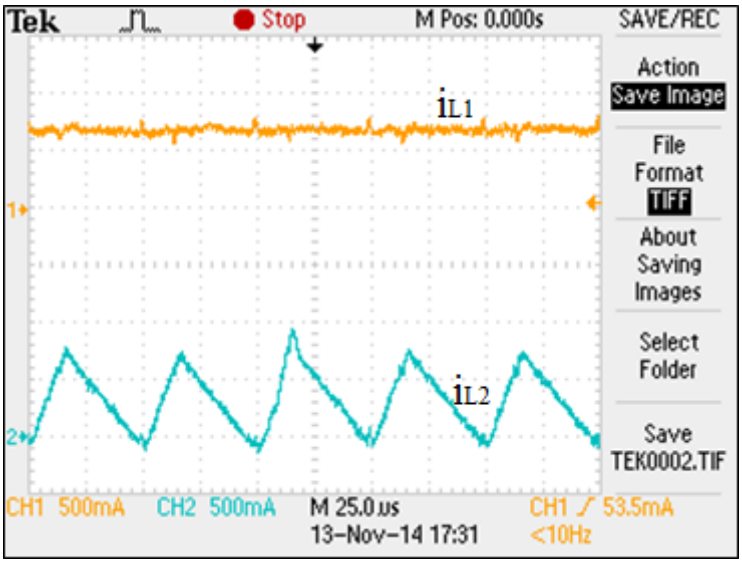


Fig. 3.2.11(b): Experimental result for zero ripple input current.

The simulation and experimental results for **k=0.687** is shown in Fig. 3.2.12(a) and Fig. 3.2.12(b). As shown in Fig. 3.2.12, the inductor L_1 current ripple is negative of inductor L_2 current ripple it is due to coupling coefficient **k** is greater than the ratio N_2/N_1. In this case measured value of inductance of inductors are L_1=0.9mH and L_2=0.39mH. The calculated value of current ripples in inductor L_1 and inductor L_2 are -0.05A and 0.85A respectively.

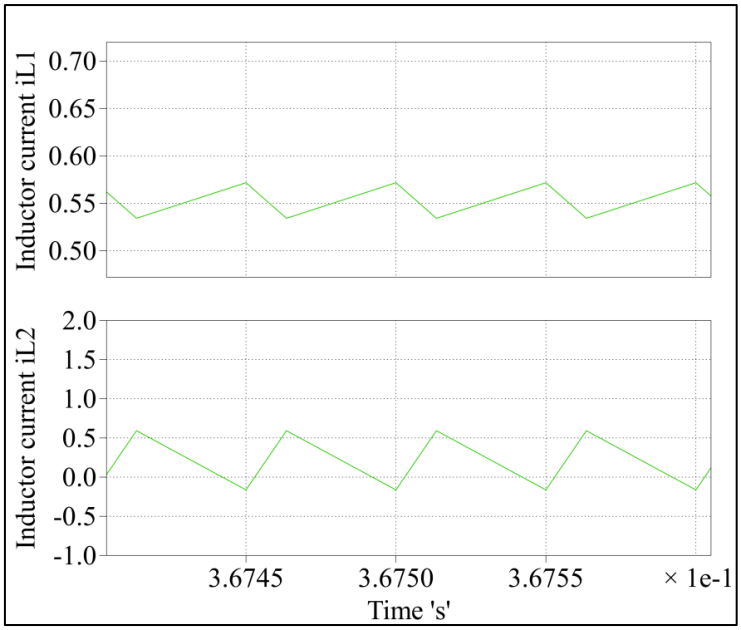


Fig. 3.2.12(a): Simulation result for negative ripple input current.

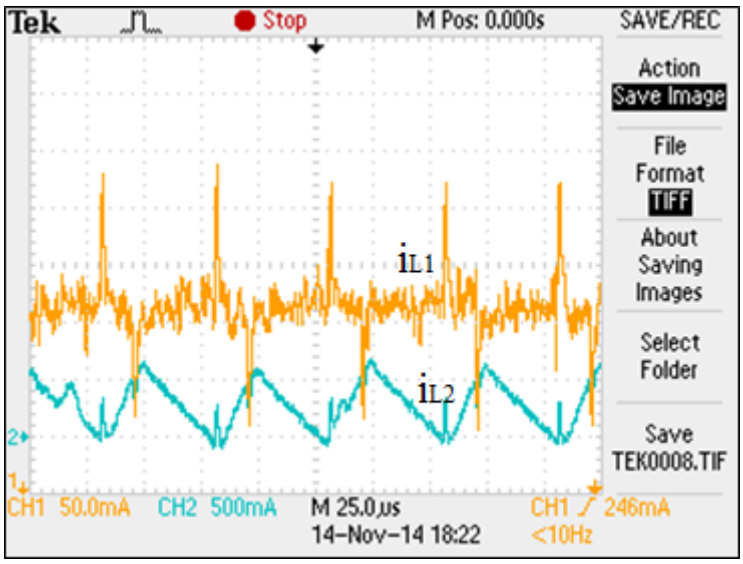


Fig. 3.2.12(b): Experimental result for negative ripple input current.

It can be observed from simulation and experimental results that the calculated values determined using equations (3.2.18) and (3.2.19) are approximately equal to these results.

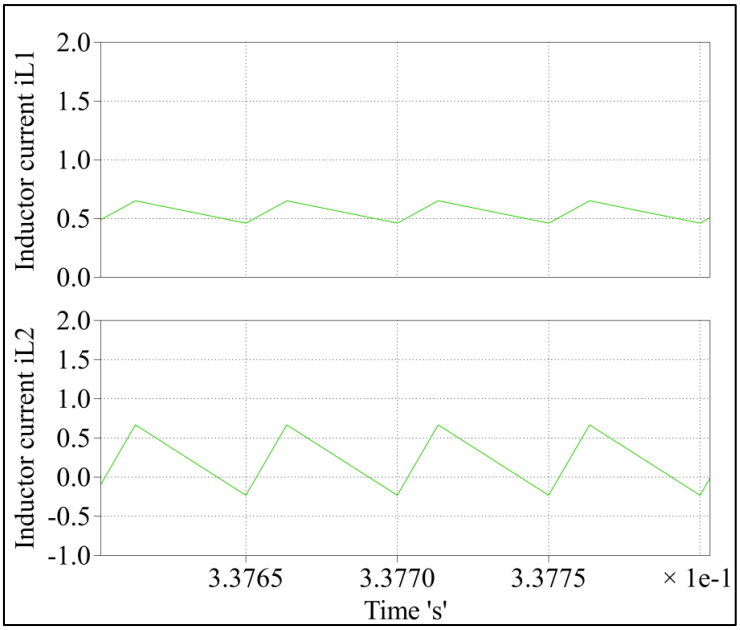


Fig. 3.2.13(a): Simulation result for $k<N_2/N_1$.

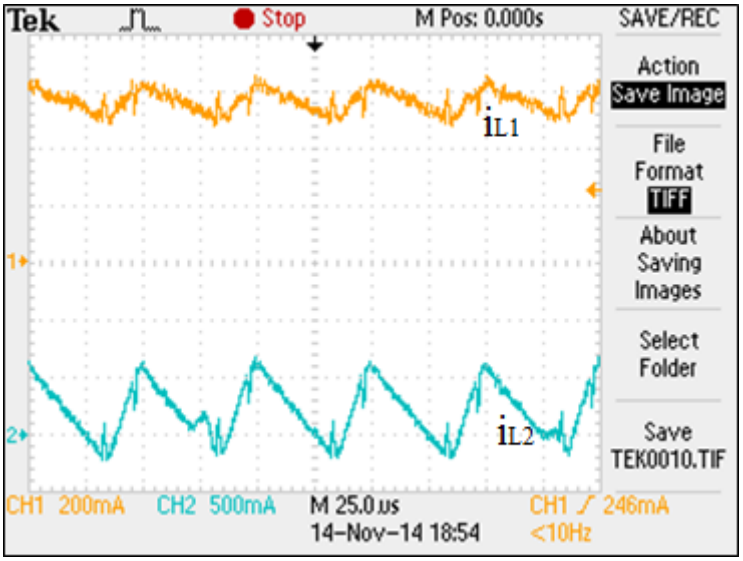


Fig. 3.2.13(b): Experimental result for $k<N_2/N_1$.

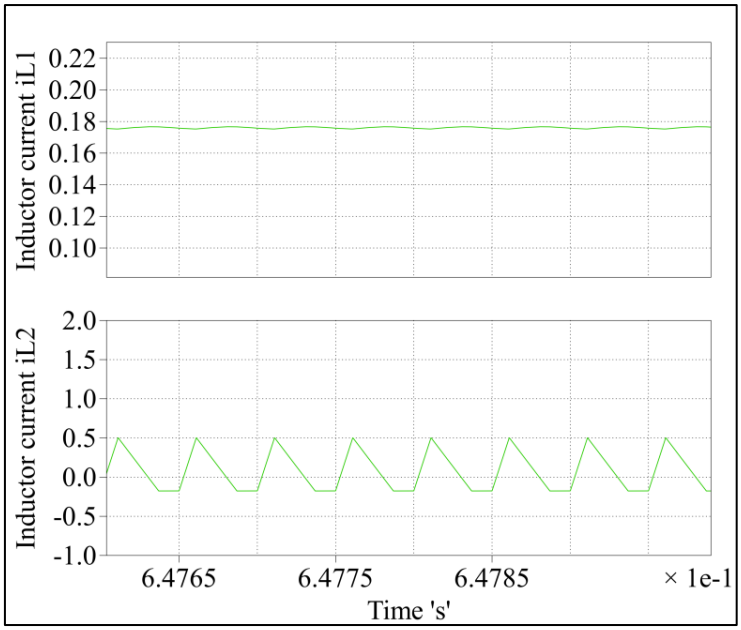


Fig. 3.2.14(a): Simulation result for zero ripple condition in DCM.

Figure 3.2.13(a) and Fig. 3.2.13(b) shows results for **k=0.4457**, in this case the current ripple increases because of coupling coefficient **'k'** is less than turn ratio N_2/N_1. Measured value of inductor L_1=0.63mH and of inductor L_2=0.29mH. The calculated value of ripple in inductor L_1 and inductor L_2 are 0.21A and 0.9A respectively for this case. Results of Fig. 3.2.14 verifies zero ripple condition in DCM mode for same value of coupling coefficient i.e. **k =0.6585**.

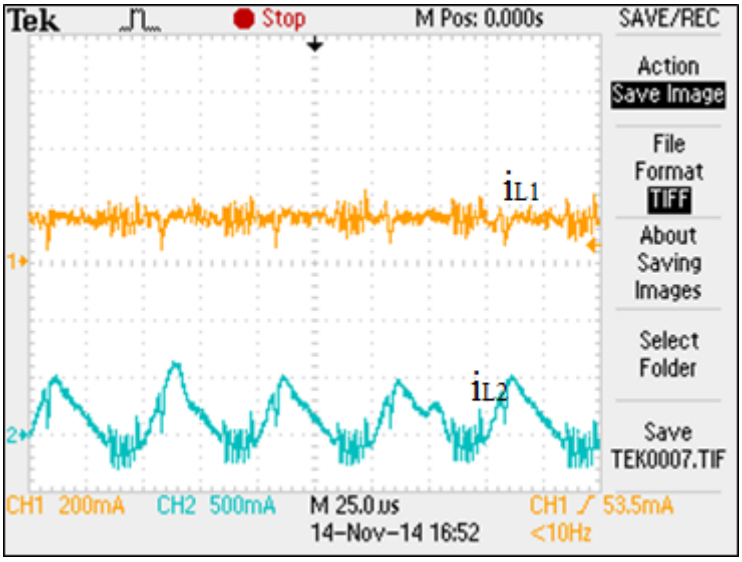


Fig. 3.2.14(b): Experimental result for zero ripples condition in DCM.

3.2.6 Conclusion

A coupled-inductor based step-up DC-DC converter is introduced in this section. Steady state analysis and current ripple analysis of the proposed converter has been carried out. Condition for zero current ripple and negative ripple was derived based on equivalent circuit model of coupled inductor. The laboratory set-up designed to experimentally verify the zero ripple condition by varying coupling coefficient and matching it with constant turn ratio. The effect of DCM mode on current ripple was investigated.

Chapter 4

One Cycle control of Z source, Quasi Z source and fourth-order step-up DC-DC Converters

4.1 Introduction

Z source inverter is proposed in 2002 [53], majority of the work reported in literature related to PWM Z-source converter (ZSC) focuses on the inverter mode of operation. The work of this chapter deals with the DC-DC converter mode of operation of the PWM Z-source converter and quasi Z-source based converter.

The quasi Z source converters [54] have been proposed as a new converter topologies based on the Z source inverter concept, which inherits all the advantages of the basic ZSC and has several more advantages, including reduced passive component ratings, continuous input current and a common dc rail between the source and inverter. Therefore it is more attractive for renewable energy sources interface applications requiring voltage boost power conversions.

In literature, several structures and voltage control methods of ZSC have been discussed. Most of the currently available publications mainly focus on the relevant theoretical research and practical application of the original Z source converter. In [55], the dynamic models of the ZSC are given from different perspectives, including various loading and parasitic components. In [29], various closed-loop control methods were proposed to achieve good control performance for the dc-link of the ZSC. In [56] and [57], the peak dc-link voltage (Vdc) is indirectly controlled by sensing capacitor voltage (V_C) and by controlling the shoot through duty ratio. However, since the relationship between V_C and Vdc and the shoot through time is non-linear, it is not possible to keep the peak dc-link voltage constant by only controlling the capacitor through regulating the shoot through duty ratio. In [58] and [59] direct measurement of the peak dc-link voltage is used as a feedback. Direct measurement will require a specially designed circuitry because of the pulsating nature of the dc-link voltage, which makes the control more complex. In [60], the voltage mode and current mode methods are used to control the dc-link voltage for ZSCs, where the peak dc-link voltage is estimated by measuring both the input and capacitor voltage. In [61] , the voltage mode and current mode methods are used to

control the dc-link voltage for quasi ZSCs, where the peak dc-link voltage is estimated by summing both the capacitor voltages.

This chapter proposes use of the One Cycle Control (OCC) method [62] for the control of peak dc link as well as capacitor voltages of ZSC and quasi ZSC. Use of one cycle control method to control the capacitor or dc link voltage in Z source converter or quasi z source converter is not reported in the literature yet. This chapter is organized as follows. Section 4.2 briefly discusses about one cycle control method. Section 4.3 and 4.4 describes the application of one cycle control to Z source as well as quasi Z source DC-DC converters. Section 4.5 presents the simulation and experimental results. Section 4.6 concludes the chapter.

4.2 One Cycle Control Method

One-cycle control (OCC) is a control technique, which achieves instantaneous dynamic control of the average value of a switched variable. The average value of the switched variable follows its control reference within a switching cycle and also rejects the power perturbations [62].

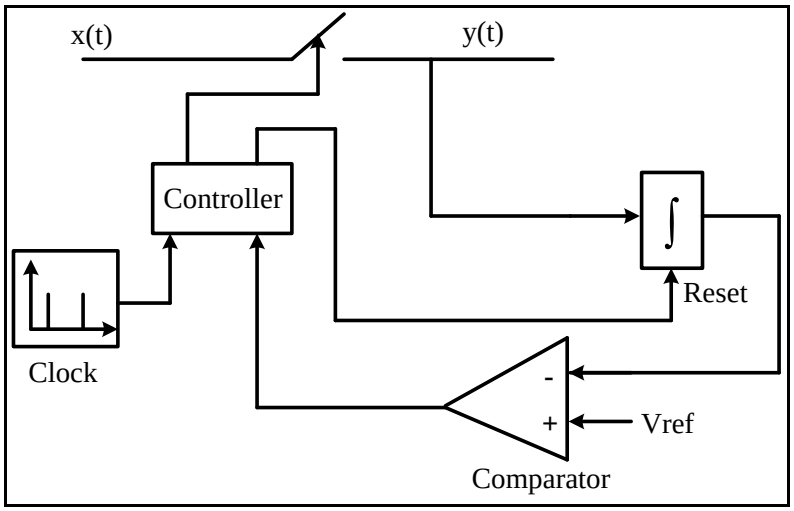


Fig. 4.1: Typical block diagram of OCC.

The output y(t) available is in chopped form and it can be called as switched variable. Here chopped pattern of switched variable y(t) is the same as that of the switch.

Another advantage of OCC is that the regulator is not required when the controlled variable is a switched variable that can be controlled directly by OCC. It has been widely applied in DC-DC conversion, power amplifier, power factor correction, active power filter, and maximum power point tracking (MPPT) of PV solar energy.

Figure 4.1 shows a typical one cycle control block diagram. The signal x(t) is the input to the switch and y(t) is output available at the output node of the switch. The switch is operating at frequency fs=1/Ts, which has a following switching function.

$$k_S(t) = \begin{cases} 1, & 0 < t < T_{ON} \\ 0, & T_{ON} < t < T_S \end{cases} \tag{4.1}$$

function $k_S(t)$,while the envelope of switch output y(t) is the same as that of the input signal x(t). The control reference $V_{ref}(t)$ is used to modulate the duty ratio which is given as $D = T_{ON}/T_S$.

If the duty ratio of the switch is controlled in such a way, that the integration of the switched variable is equal to or proportional to the control reference in each cycle, i.e.

$$k_S \int_0^{T_{ON}} x(t)\,dt = v_{ref}(t) \tag{4.2}$$

Where k_s is a constant, the average of the switched variable y(t) will be equal to or proportional to control reference. So it can be written as

$$y(t) = \frac{1}{T_S} \int_0^{T_{ON}} x(t)\,dt = K_o v_{ref}(t) \tag{4.3}$$

Where, $K_o = \dfrac{1}{k_S T_S}$ is also a constant. This method of control is defined as the One-Cycle Control technique. It can be implemented as shown in Fig. 4.1. The switch is turned ON by the fixed frequency clock pulse and as switch became ON integration starts. The integration value is given by

$$v_{\text{int}} = k_S \int_0^t x(t)\,dt \tag{4.4}$$

This integrated value is compared with the control reference $v_{ref}(t)$ instantaneously. When the integrated value v_{int} becomes equal to the control reference $v_{ref}(t)$, at that instant the controller turns off the switch and resets the integrator to zero. On the similar track, one cycle control for Z-source and quasi Z-source based converters is proposed in this chapter.

4.3 One Cycle Control of Z Source DC-DC Converter

Figure 4.2(a) shows a Z source DC-DC Converter [28]. Switch S controls the output voltage of the converter. Figure 4.2(b) shows a circuit when switch S is closed and Fig. 4.2 (c) shows a circuit when switch S is open. From the steady state analysis of the circuit [28] and assuming that the network is symmetric, the expressions for capacitor voltage V_C, dc-link voltage V_{dc} and output voltage V_0 can be found as

$$V_C = V_{C1} = V_{C2} = \frac{1-D}{1-2D}V_{in},\ V_{dc} = \frac{1}{1-2D}V_{in},\ V_0 = \frac{1-D}{1-2D}V_{in} = V_C \qquad (4.5)$$

Where, D is duty ratio of switch S.

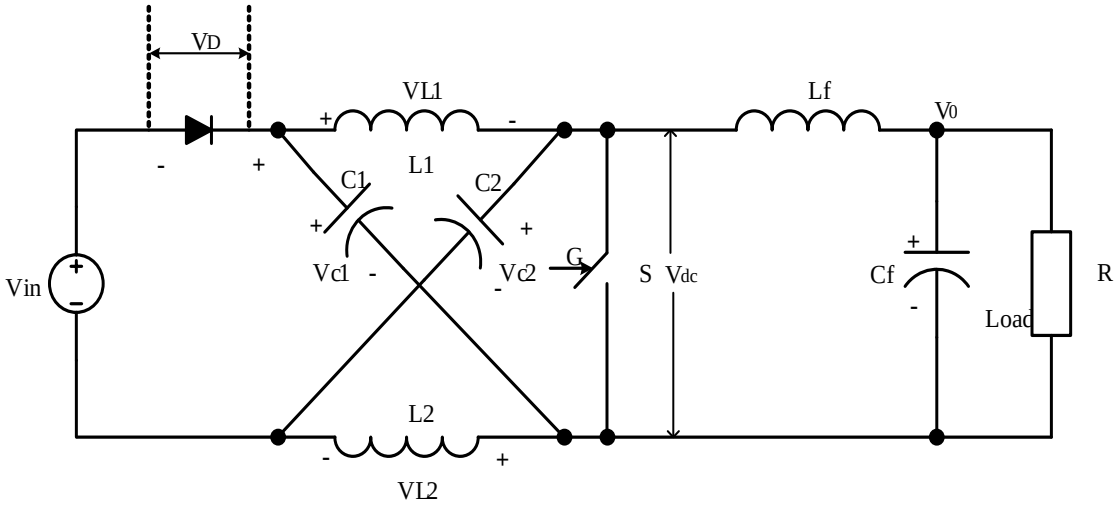


Fig. 4.2 (a): Z-source DC-DC converter.

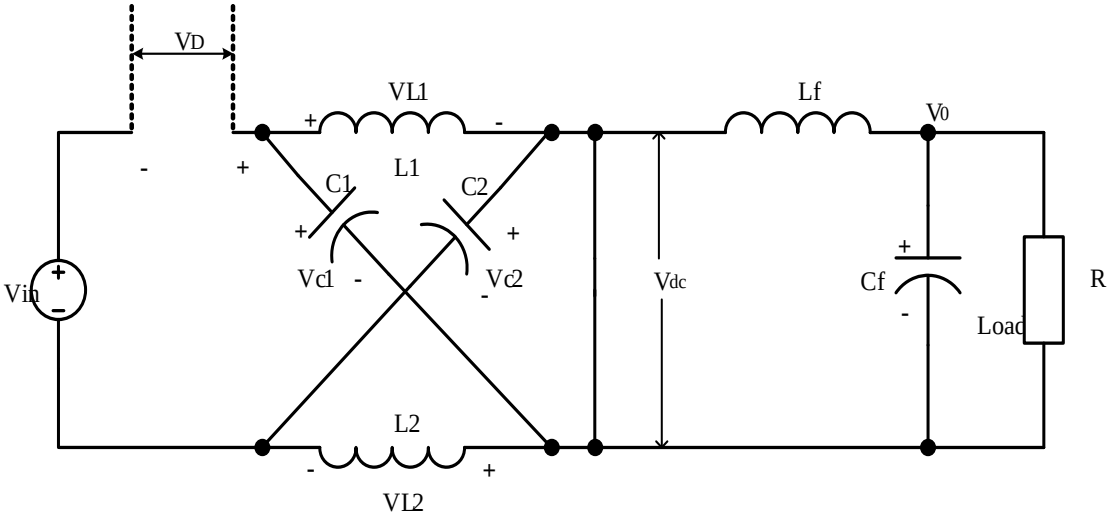


Fig. 4.2(b): Z-source DC-DC converter circuit when S is close.

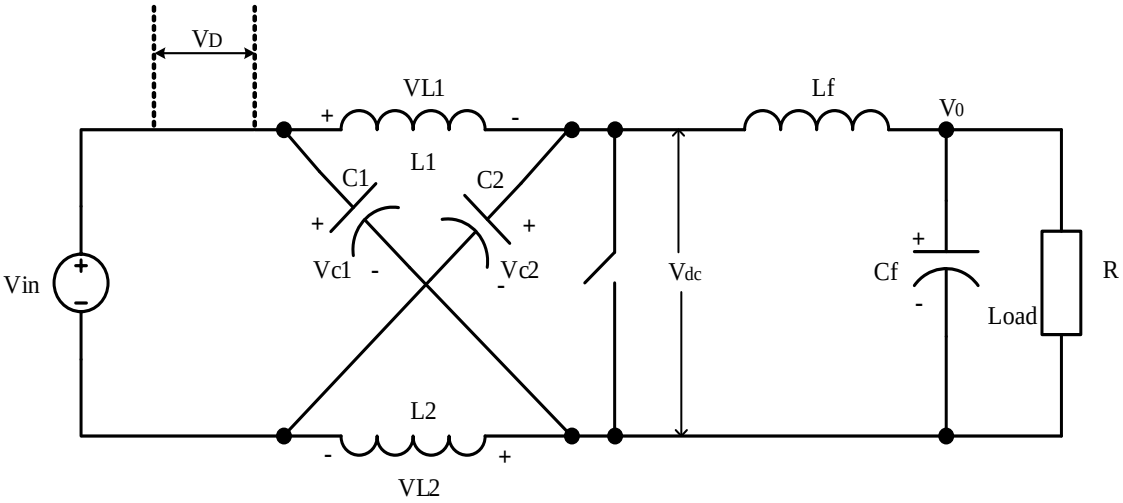


Fig. 4.2(c): Z-source DC-DC converter circuit when S is open.

Figure 4.3 shows a Z source converter with one cycle control. The diode reverse voltage V_D is chosen as a switched variable.

The input to the integrator is voltage across the input diode, V_D as shown in Fig. 4.3. From the circuit, the control equation can be written as

$$V_{ref} - V_{in} = K_o \int_0^{DT_S} V_D dt \qquad (4.6)$$

Note the control equation where apart from switched variable, one has to also sense the input voltage V_{in}. In steady state, the average diode voltage is equal to the difference of capacitor voltage and input voltage. When switch S in ON (Fig 4.2 (a)), the reverse voltage across diode is ($2V_C$-V_{in}) and when the switch S is OFF (Fig 4.2 b)), the voltage across diode is zero. Hence value of switched variable V_D switches between ($2V_C$-V_{in}) and zero. Therefore, equation (4.6) can be written as

$$V_{ref} - V_{in} = K_o \int_0^{DT_S} (2V_C - V_{in})dt \tag{4.7}$$

Also note the multiplier constant 'K_o'. It plays an important role in determining the voltage to be controlled. One can control either capacitor voltage or dc link voltage by using the appropriate value of K_o. If one wants to control the dc link voltage, the integration constant 'K_o' will be 2/Ts where Ts is the time period of switching signal. Therefore the equation (4.7) will be

$$V_{ref} - V_{in} = \frac{2}{T_S} \int_0^{DT_S} (2V_C - V_{in})dt \tag{4.8}$$

This result in

$$V_{ref} - V_{in} = 2D(2V_C - V_{in}) \tag{4.9}$$

By substituting V_C from equation (4.5) in (4.9) and simplifying (4.9) results in steady state DC link voltage equal to the reference V_{ref}.

$$V_{ref} = \frac{1}{1-2D} V_{in} = V_{dc} \tag{4.10}$$

Here 'dc link voltage' is referred to the voltage across switch S. This term is more relevant in applications such as Z source inverter where 'dc link voltage' is a DC voltage available for inversion. This highlights a feature of OCC method that it can be used in inverter applications for DC link voltage control.

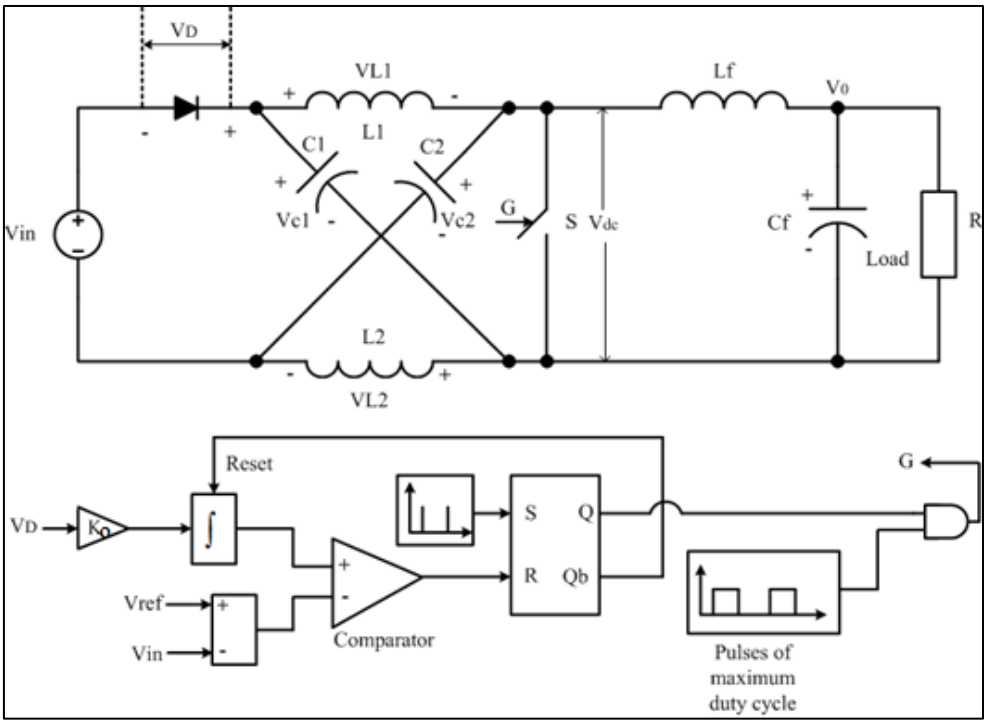


Fig. 4.3: Z source converter with one cycle controller.

Similarly, if the capacitor voltage V_C needs to be controlled, the integration constant 'K_o' will be 1/Ts. The equation (4.6) becomes

$$V_{ref} - V_{in} = D(2V_C - V_{in}) \tag{4.11}$$

By substituting V_C from equation (4.5) in (4.11), the capacitor voltage will be equal to reference voltage.

$$V_{ref} = \frac{1-D}{1-2D} V_{in} = V_C \tag{4.12}$$

For the DC-DC converter in Fig. 4.2, if one controls the capacitor voltage V_C, it is same as controlling the output voltage V_0 which is apparent from the equation (4.5). Thus, it can be seen that with one cycle control, either DC link voltage or capacitor voltage can be controlled.

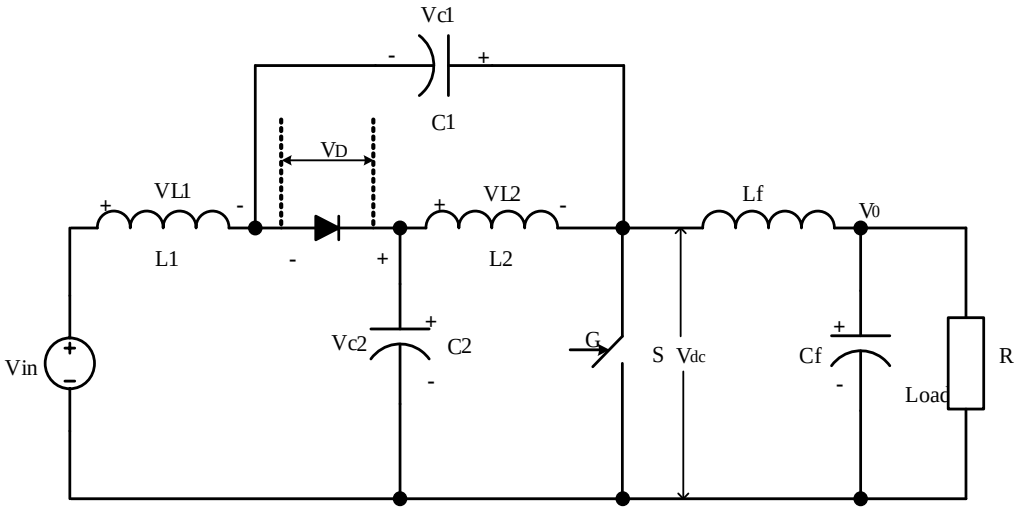


Fig. 4.4(a): Quasi Z-source DC-DC converter.

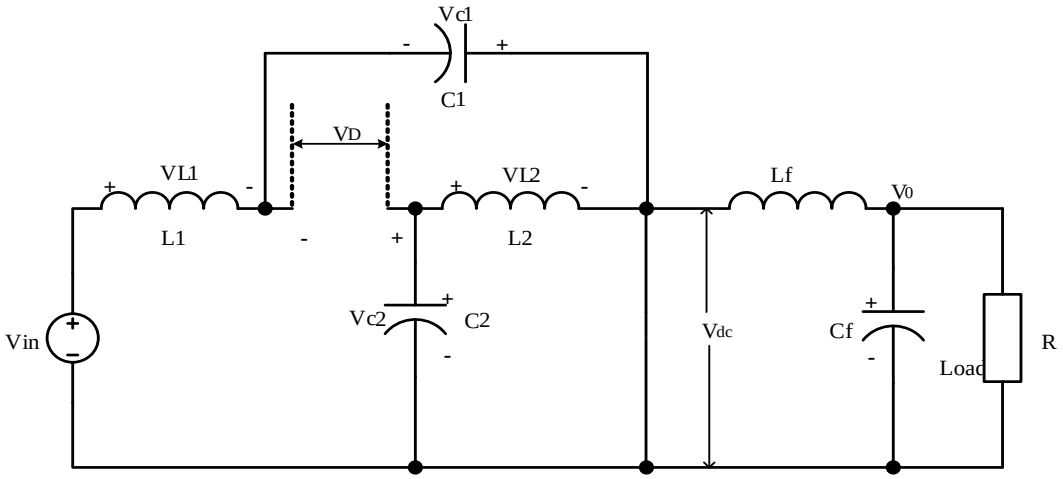


Fig. 4.4(b): Quasi Z-source DC-DC converter when switch is closed.

4.4 One Cycle Control of Quasi-Z Source DC-DC converter and fourth order Step-up DC-DC Converter

Figure 4.4(a) shows a Quasi Z source DC-DC Converter. Switch S controls the output voltage of the converter. Figure 4.4 (b) shows a circuit when switch S is closed and Fig. 4 (c) shows a circuit when switch S is open.

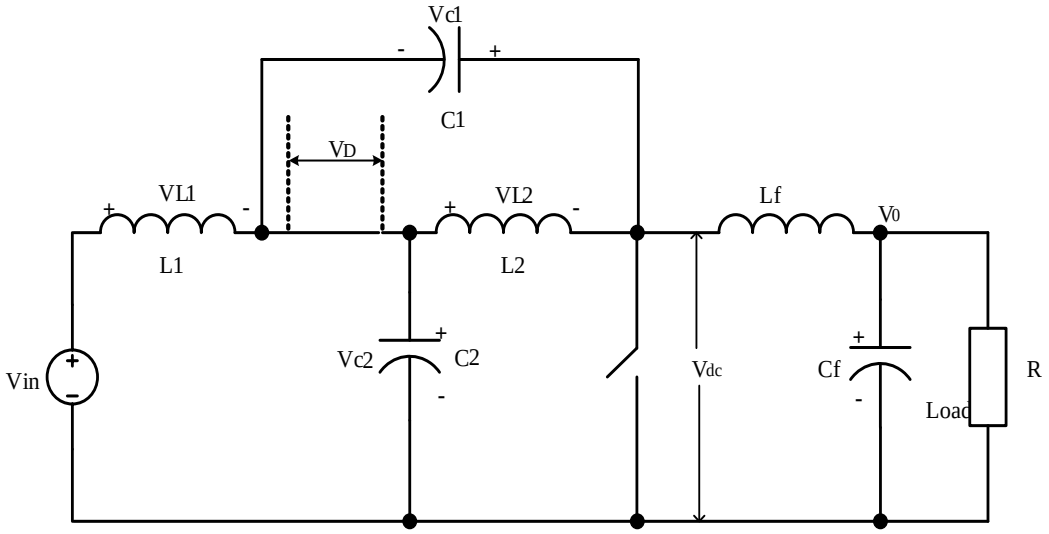


Fig. 4.4(c): Quasi Z-source DC-DC converter when switch S is open.

From the steady state analysis of the circuit [55] the expressions for capacitor voltages V_{C1} and V_{C2}, dc-link voltage V_{dc} and output voltage V_0 can be found as

$$V_{C1} = \frac{1-D}{1-2D}V_{in}, \qquad V_{C2} = \frac{D}{1-2D}V_{in}, \qquad V_{dc} = \frac{1}{1-2D}V_{in} \tag{4.13}$$

$$V_0 = \frac{1-D}{1-2D}V_{in} = V_{C1}$$

Figure 4.5 shows a one cycle controlled Quasi-Z source converter. Diode reverse voltage V_D is chosen as switched variable. The block diagram of the controller is same as that for Z source converter.

The input to the integrator is voltage across the diode, V_D as shown in Fig. 4.5. When switch S in ON (Fig 4.4 a), the reverse voltage across diode is (V_{C1}+V_{C2}) and when the switch S is OFF (Fig 4.4 b), the voltage across diode is zero.

Hence value of switched variable V_D switches between (V_{C1}+V_{C2}) and zero. In the similar manner as ZSC, the control equation can be written as

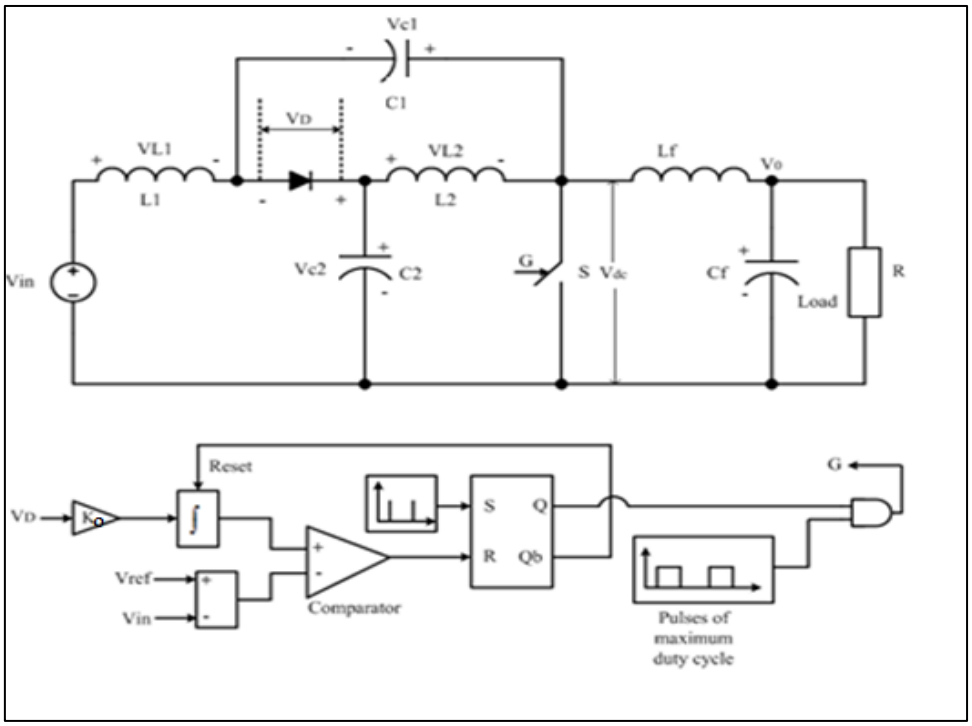


Fig. 4.5: Quasi Z source converter with one cycle controller.

$$V_{ref} - V_{in} = K_o \int_0^{DT_S} (V_{C1} + V_{C2})dt \tag{4.14}$$

If one wants to control the dc link voltage, the integration constant 'K_o' will be 2/Ts where Ts is the time period of switching signal. Therefore the equation (4.14) will be

$$V_{ref} - V_{in} = \frac{2}{T_S} \int_0^{DT_S} (V_{C1} + V_{C2})dt \tag{4.15}$$

Substituting V_{C1} and V_{C2} from equation (4.13) in (4.15) and simplifying (4.15) results in

$$V_{ref} = \frac{1}{1-2D} V_{in} \tag{4.16}$$

If one wants to control the capacitor voltage V_{C1}, the integration constant 'K_o' will be $1/T_s$. Therefore the final equation will become

$$V_{ref} = \frac{1-D}{1-2D} V_{in} \tag{4.17}$$

If one wants to control the capacitor voltage V_{C2}, the fundamental control equation (4.14) needs to be modified which is given as

$$V_{ref} = K_o \int_0^{DT_S} (V_{C1} + V_{C2}) dt \tag{4.18}$$

Substituting V_{C1} and V_{C2} from equation (4.13) in (4.18) and 'K_o' as T_s and simplifying (4.18) results in

$$V_{ref} = \frac{D}{1-2D} V_{in} \tag{4.19}$$

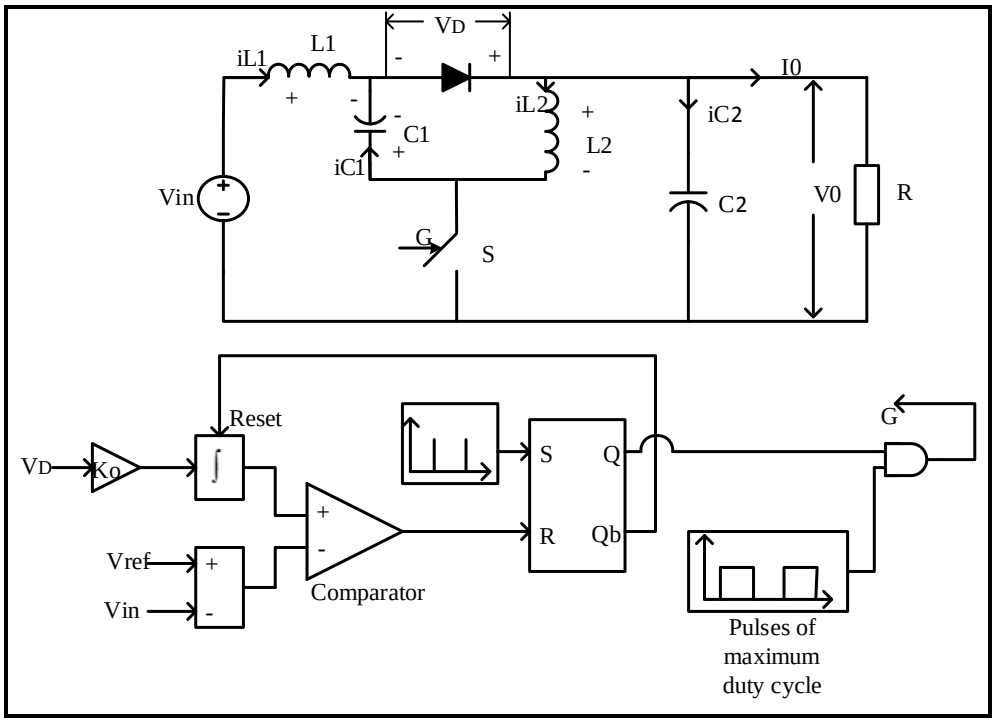


Fig. 4.6: One cycle control of fourth-order step-up DC-DC converter.

It can be observed that one does not need to sense V_{in} for controlling V_{C2}. Thus one cycle control will allow us to control V_{C1} or V_{C2} or V_{dc}. Based on requirement, one can choose appropriate control variable.

Figure 4.6 shows block diagram of one cycle control of fourth-order step-up DC-DC converter. The control equations for OCC of fourth-order step-up DC-DC converter

are derived, and it is found that one cycle control equations are same as equations (4.14), (4.17)-(4.19).

4.5 Simulation and experimental Results

Experimental setup of one cycle control circuit is designed to verify the theoretical analysis. The hardware circuit is designed for switching frequency of 10 KHz.

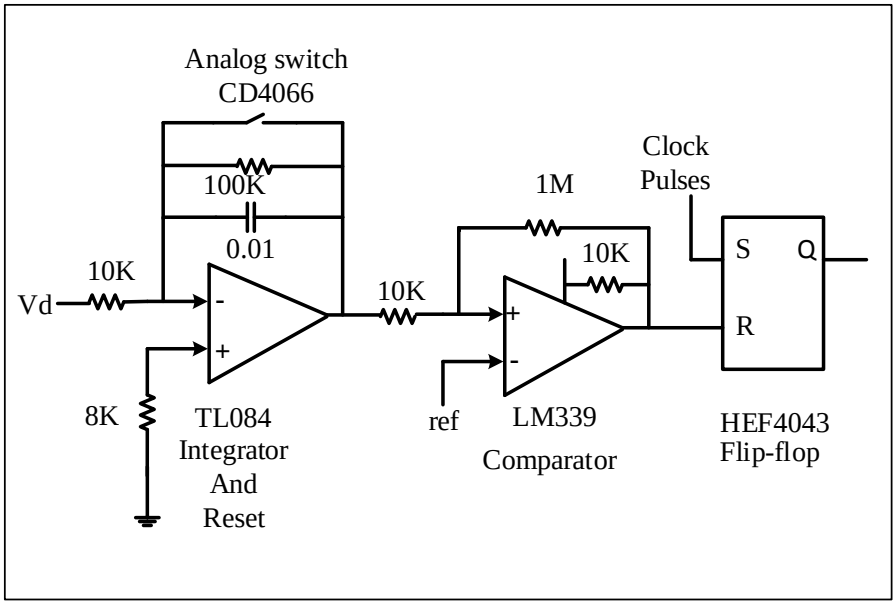


Fig. 4.7 (a): Core of One Cycle control circuit.

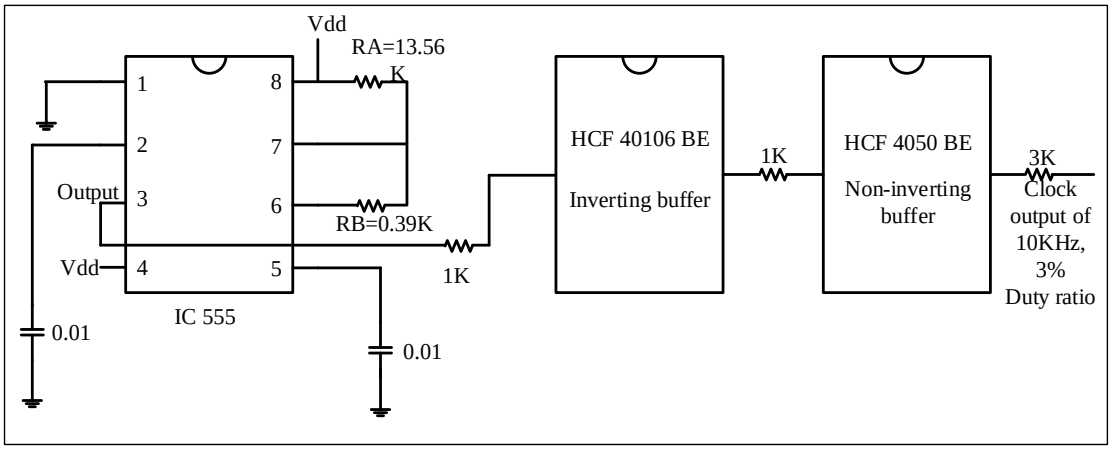


Fig. 4.7 (b): Clock pulse generation circuit.

The main circuit for implementation of OCC can be club in three parts. The main part of OCC is shown in Fig. 4.7(a), it consists integrator circuit, comparator circuit and integrator reset circuit. Figure 4.7(b) shows circuit for pulse generation of 10 KHz frequency and 3% duty ratio. In Fig. 4.7(b) IC 555 generate clock pulses of 97% duty ratio and then it is converted to suitable form by using buffer circuits. Figure 4.7(c) is used to sense diode voltage and for generating V_{ref}-V_{in} voltage signal.

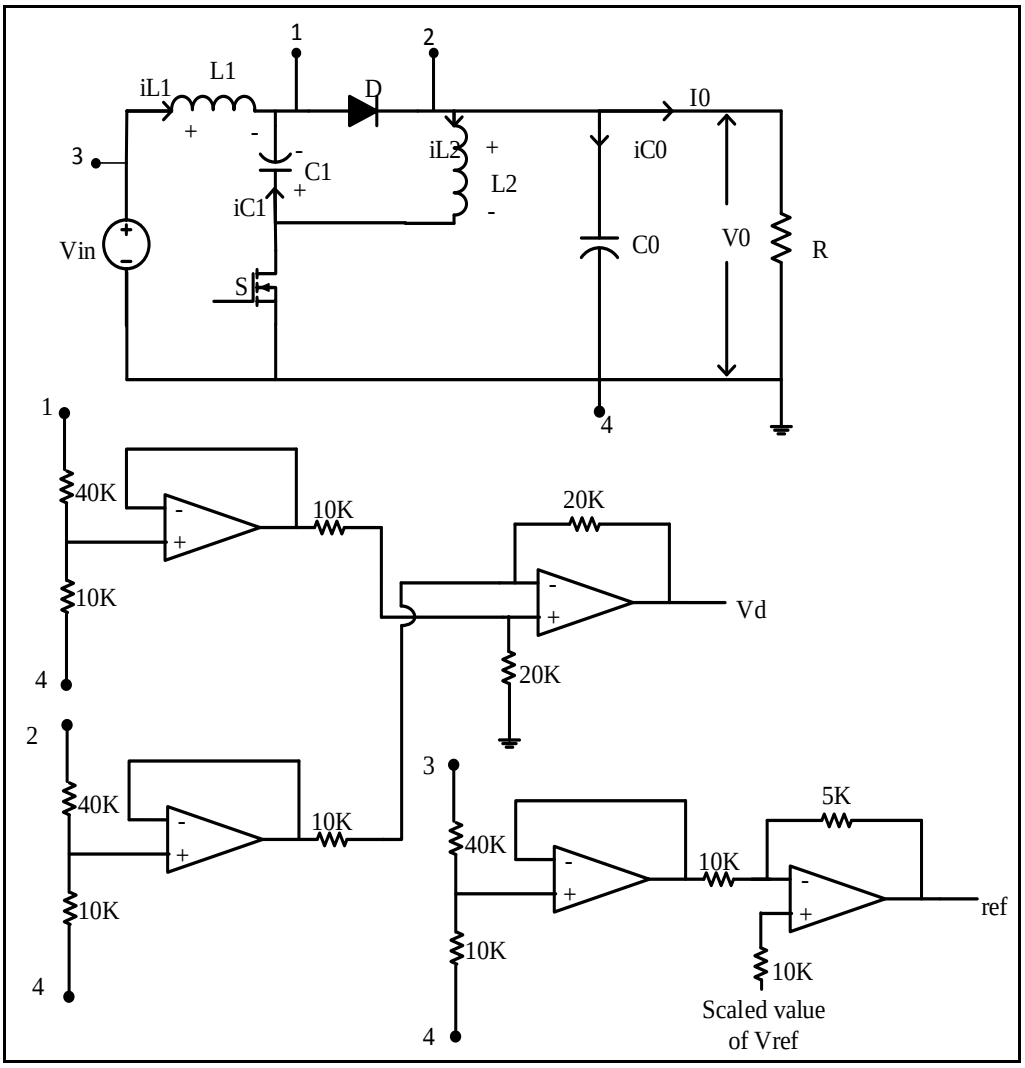


Fig. 4.7 (c): Diode voltage sensing and (V_{ref}-V_{in}) circuit.

4.5.1 Z Source DC-DC Converter

For the Z source DC-DC converter as shown in Fig. 4.2, the set of parameters chosen are as follows: L_1=L_2=2 mH, C_1=C_2=2 mF, R_{L1}=R_{L2}=0.1Ω, R_{C1}=R_{C2}=10 mΩ, L_f=1

mH, C_f=1 mF and R=30 Ω. R_{L1}, R_{L2}, R_{C1} and R_{C2} are not shown in the Fig. 4.2. Two cases are studied in simulation (i) response to input voltage variation and (ii) response to reference variation. The variable to be controlled is capacitor voltage V_C. The control equation is modified accordingly by substituting K_o=1/Ts. The switching frequency is taken as 10 kHz. All the simulations are carried out in PLEXIM-PLECS software.

4.5.1.1 Response to the variation in input voltage V_{in}

Figure 4.8 shows response of the capacitor voltage V_C with the variation in the input voltage V_{in}. The voltage V_{in} is varying between 40 to 60 volts as shown in Fig. 4.8. The reference voltage V_{ref} is set at 80 V. It can be seen that the input voltage disturbance is rejected completely since the integrator output changes immediately which in turn changes the duty cycle instantaneously within one cycle. The capacitor voltage is remains at 80 V which is equal to reference voltage. Figure 4.8 also shows the output voltage V_0 to emphasize that V_C is equal to V_0 for this converter.

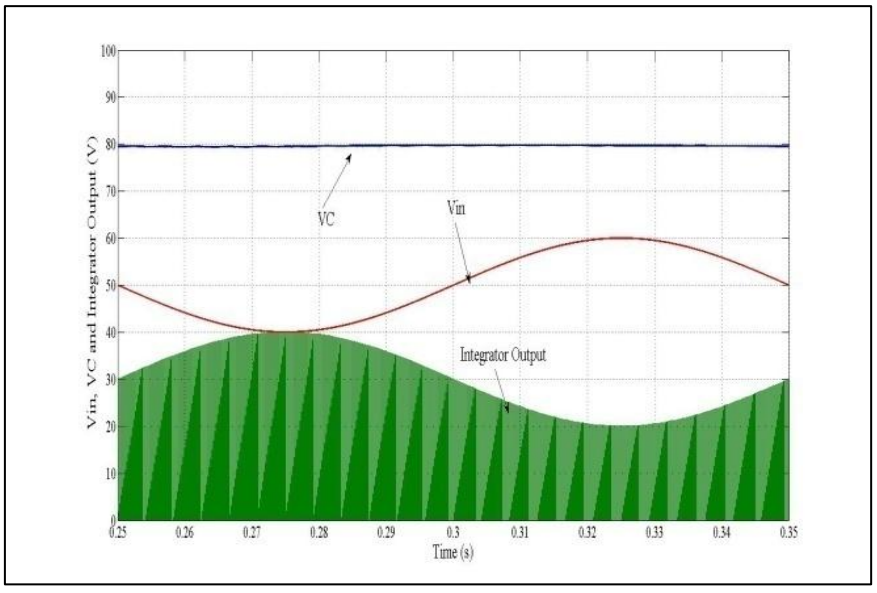


Fig. 4.8: Response of capacitor voltage with Vin.

4.5.1.2 Response to the variation in reference voltage Vref

Figure 4.9 shows response of the capacitor voltage V_C with the variation in the reference voltage V_{ref}. It can be clearly seen that the capacitor voltage is following the reference voltage. The output of the integrator along with this variation is also shown.

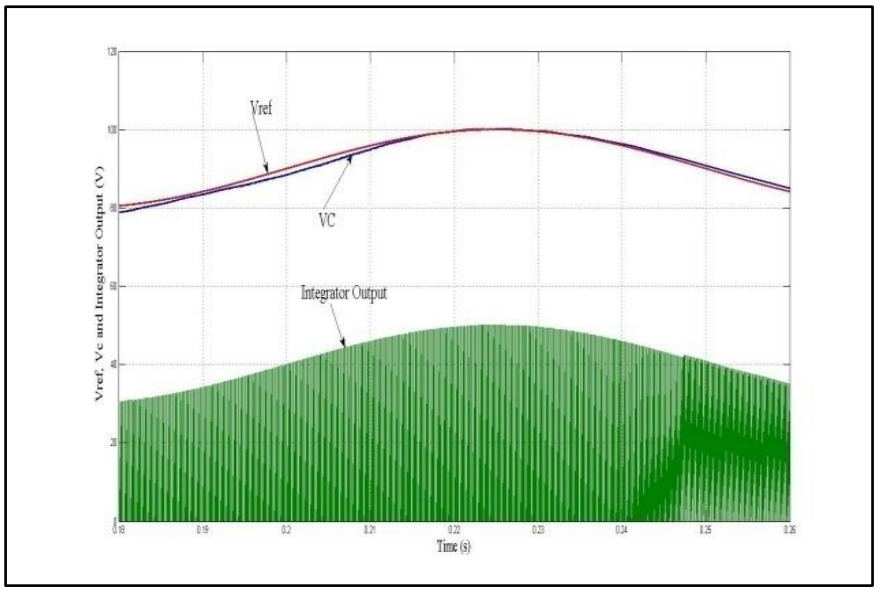


Fig. 4.9: Response of capacitor voltage with Vref.

4.5.2 Quasi Z source DC-DC converter

Figure 4.10 shows the experimental setup for One cycle control of Quasi Z-source DC-DC converter.

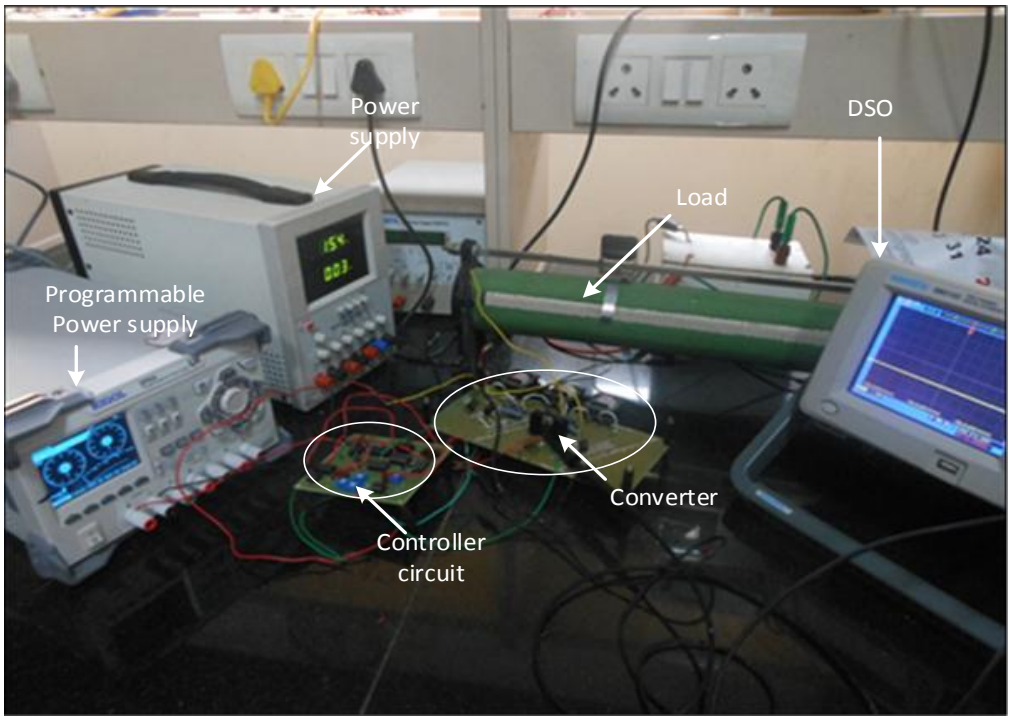


Fig. 4.10: Experimental setup for One cycle control.

For the Quasi Z source DC-DC converter as shown in Fig. 4.4, the set of parameters chosen are as follows: L_1=355µH, L_2=356µH, C_1=60 µF, C_2=200 µF , R_{L1}=R_{L2}=0.035Ω, R_{C1}=0.155Ω R_{C2}=0.038Ω, L_f=2mH, C_f=194.8µF, R_{Lf}=0.53Ω, R_{Cf}=0.065Ω and load resistance R=42 Ω. Three cases are studied in simulation (i) response to input voltage variation and (ii) response to reference variation and (iii) control of dc-link voltage. The control equation and K_o is modified accordingly. IRF 540 is used as active switch and MUR460 diode is used as passive switch in the converter. The switching frequency is taken as 10 kHz.

4.5.2.1 Response to the variation in input voltage V_{in}

Figures 4.11(a) and 4.11(b) shows simulation and experimental result of the output voltage with the variation in the input voltage V_{in}. The voltage V_{in} is changed from 15 to 18 volts as shown in simulation and experimental results in Fig. 4.11(a) and Fig. 4.11(b). The reference voltage V_{ref} is constant for output voltage is set at 24 V. It can be seen that the input voltage disturbance is rejected immediately since the integrator output changes immediately which in turn changes the duty cycle instantaneously within one cycle.

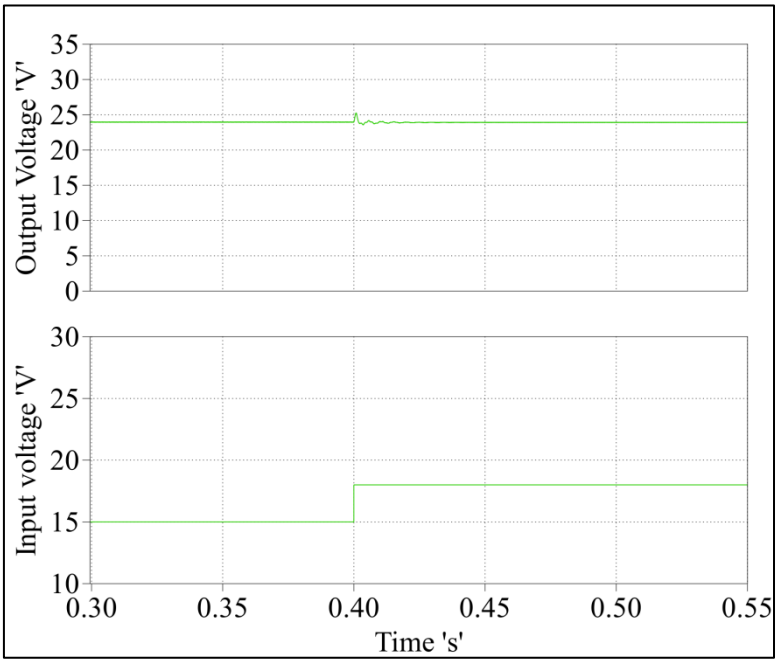


Fig. 4.11(a): Simulation result of output voltage with step change in V_{in}.

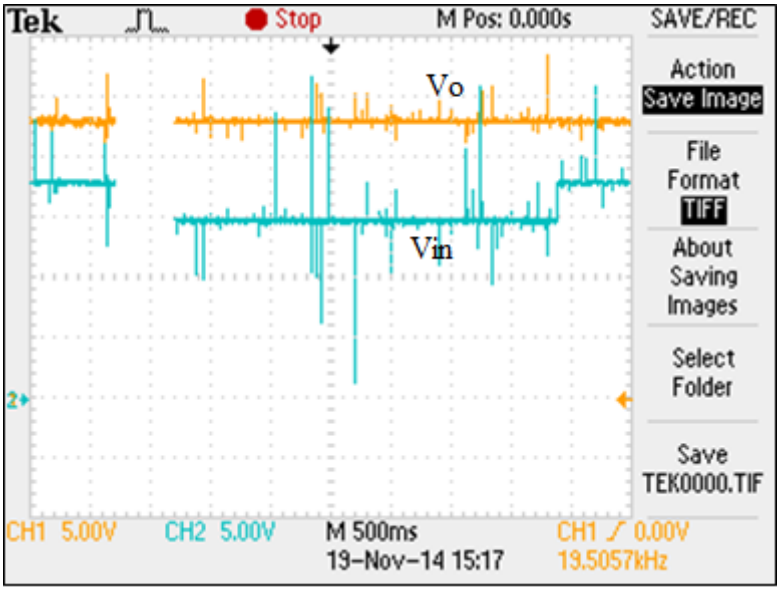


Fig. 4.11(b): Experimental result for step change in input.

4.5.2.2 Response to the variation in reference voltage V_{ref}

Figures 4.12(a) and 4.12(b) shows simulation and experimental results of output voltage with the variation in the reference voltage V_{ref} while keeping input voltage constant. It can be clearly seen that the output voltage is following the reference voltage

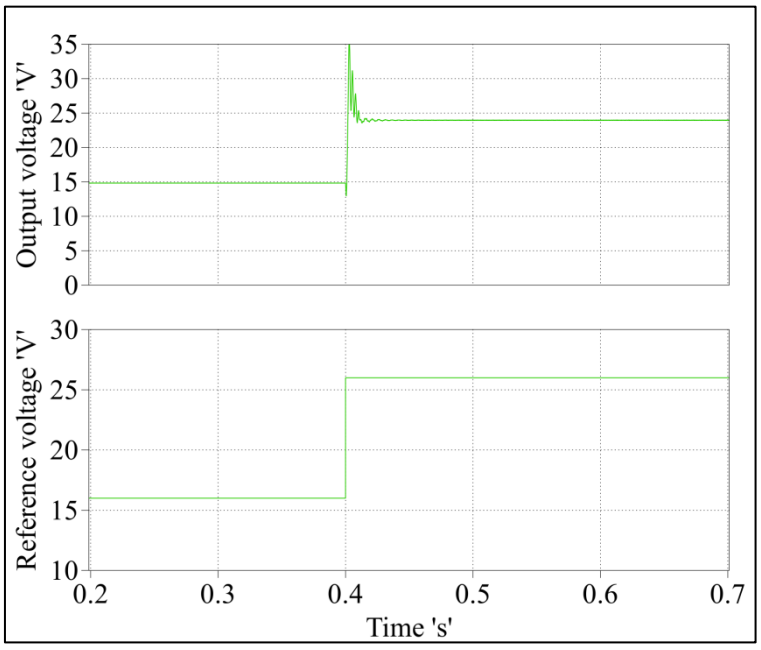


Fig. 4.12(a): Response of output voltage with V_{ref}.

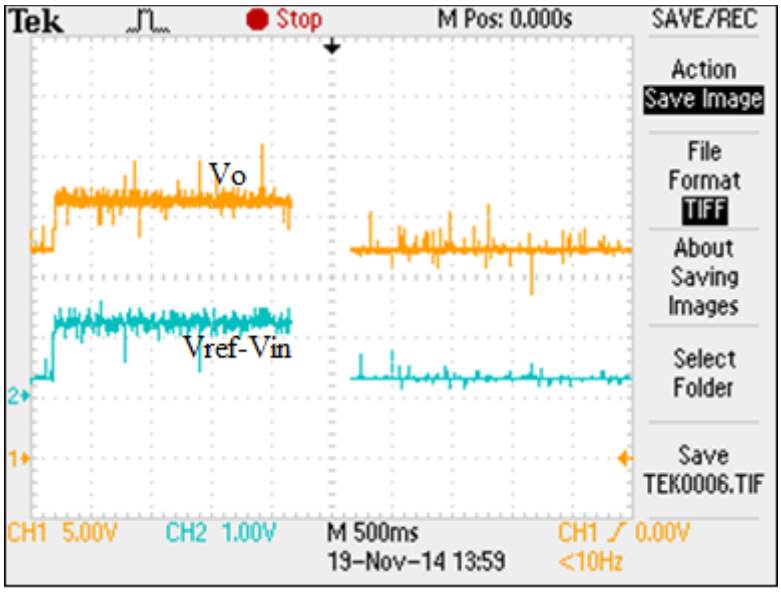


Fig. 4.12(b): Experimental result for step change in reference voltage.

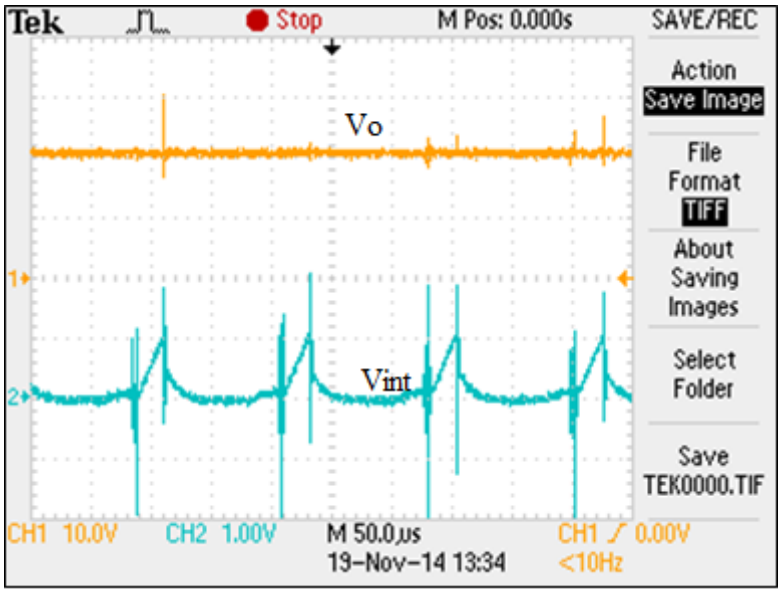


Fig. 4.13(a): Output voltage and Integrator waveform.

. Figure 4.12(a) shows the simulation results of output voltage for step change in reference voltage from 16V to 26V and Fig. 4.12(b) shows experimental result for same condition. In Fig. 4.12(b) lower waveform is showing scaled value of (V_{ref}-V_{in}). Figure 4.13(a) shows the scaled integrator voltage for 21V output voltage and Fig. 4.13(b) shows negative scaled value of diode voltage for 21V output voltage.

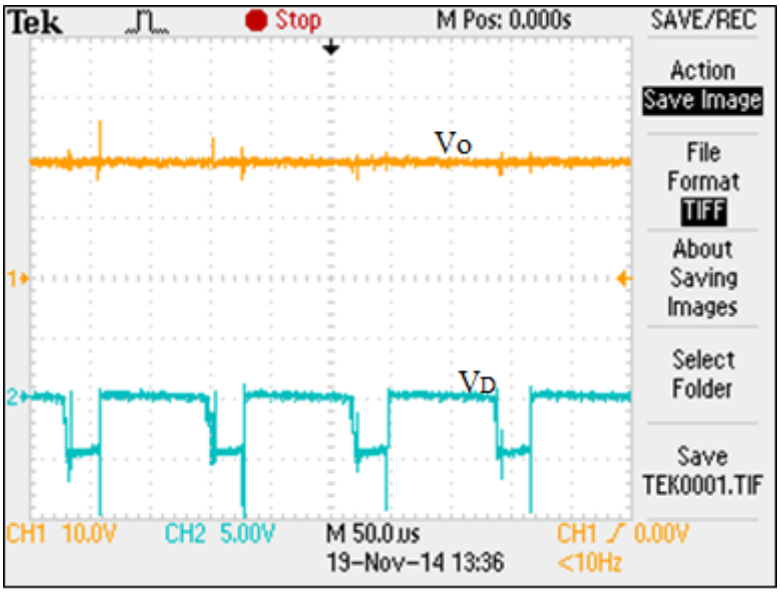


Fig. 4.13(b): Voltage across diode and Output voltage.

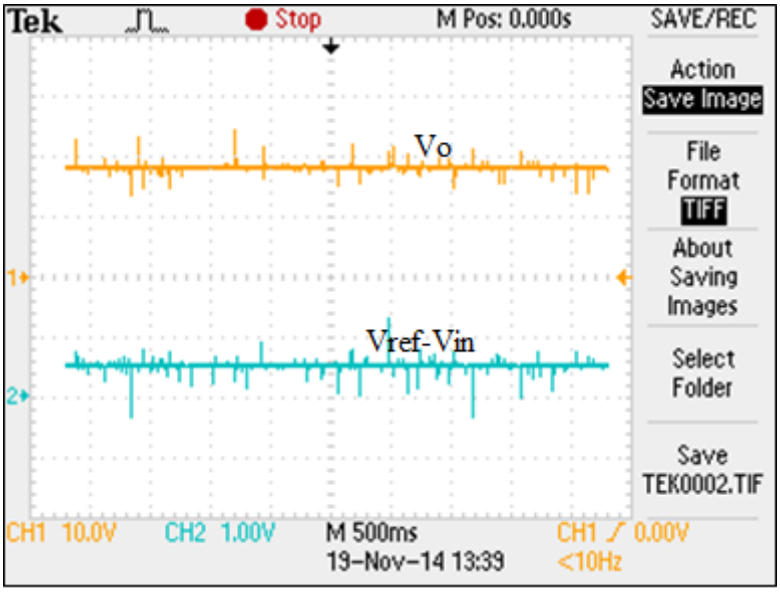


Fig. 4.13(c): Output voltage waveform.

Experimental result for 19Vscaled reference is shown in Fig. 4.13(c), where lower waveform is of scaled value of (V_{ref}-V_{in}).

4.5.2.3 Control of DC-link voltage

Figure 4.14(a) shows response of dc-link voltage with the variation in input voltage from 18V to 15V for a given dc-link voltage reference.

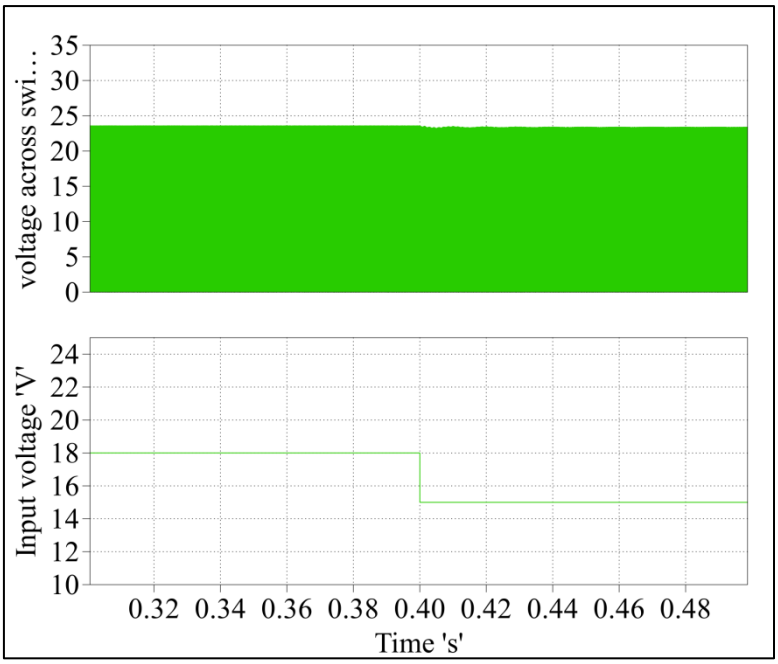


Fig. 4.14(a): Response of DC-link voltage for step change in input voltage.

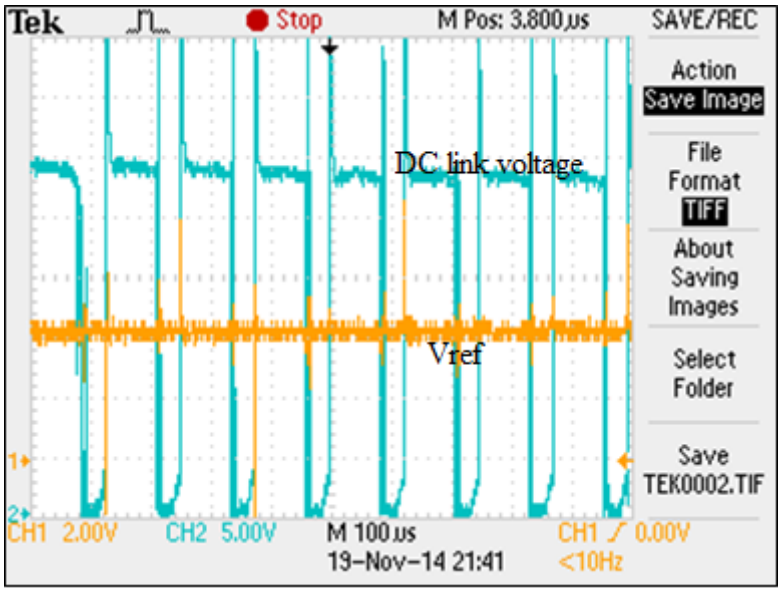


Fig. 4.14(b): Experimental result of DC-link voltage for given reference.

For controlling dc-link voltage directly, it is required to modify value of 'K_o'. Figure 4.14(b) shows experimental result of dc-link voltage and scaled value of dc-link reference voltage for 24V dc-link voltage.

4.5.3 OCC for fourth-order step up DC-DC converter

For the fourth-order step-up DC-DC converter as shown in Fig. 4.6, the set of parameters chosen are as follows: L_1=355µH, L_2=356µH, C_1=60 µF C_2=200 µF , R_{L1}=R_{L2}=0.035Ω, R_{C1}=0.155Ω R_{C2}=0.038Ω and load resistance R=42 Ω . Two cases are studied in simulation i) response to input voltage variation and ii) response to reference variation. The variable to be controlled is output voltage. The other converter parameters are same as given above for quasi Z-source DC-DC converter.

4.5.3.1 Response to the variation in input voltage V_{in}

Figure 4.15 and Fig. 4.16 shows results of the output voltage with the variation in the input voltage V_{in}. The voltage V_{in} is subjected to step change as shown in Fig. 4.15(a). The reference voltage V_{ref} is set at 18 V. Fig. 4.15(b) shows the experimental result for step change in input. It can be seen that the input voltage disturbance is rejected immediately since the integrator output changes immediately which in turn changes the duty cycle instantaneously within one cycle. The output voltage is remains 18 V.

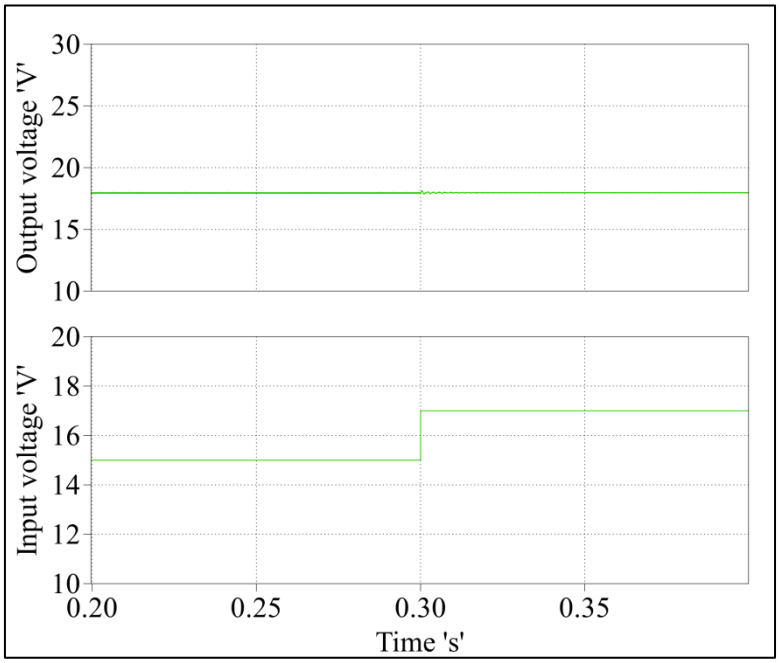


Fig. 4.15(a): Response to step change in input voltage.

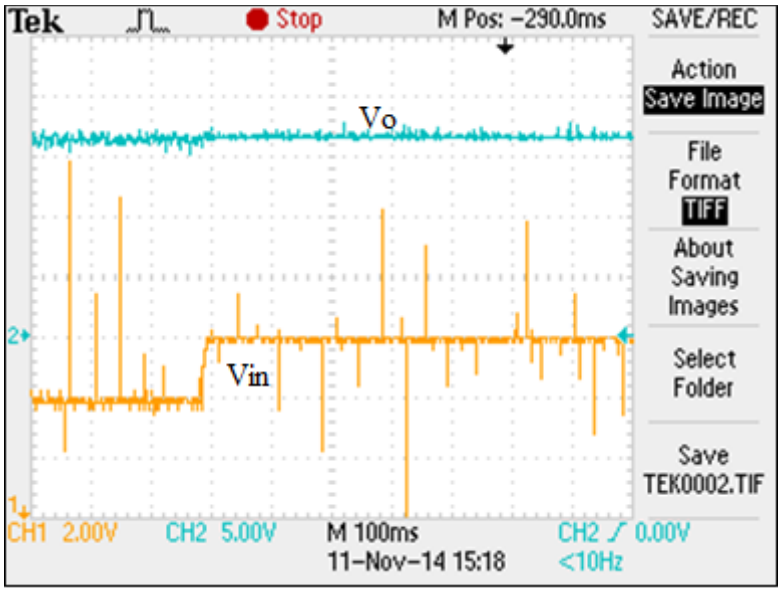


Fig. 4.15(b): Experimental result for step change in input voltage.

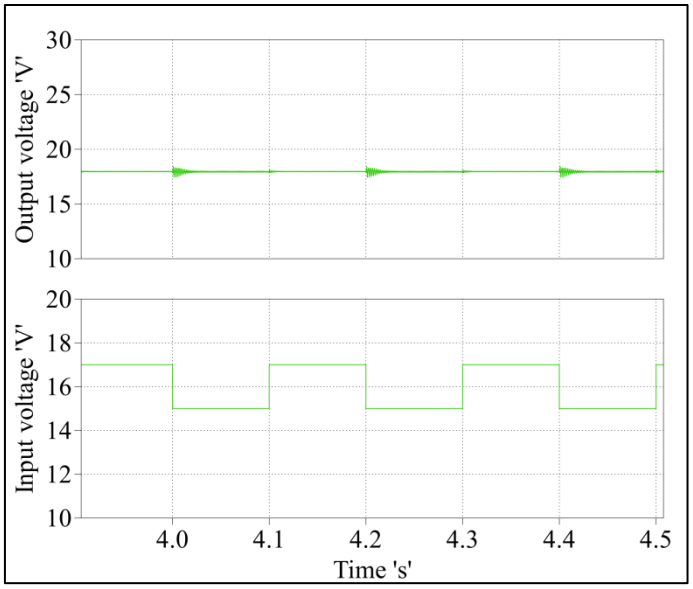


Fig. 4.16(a): Simulation result for change in input voltage.

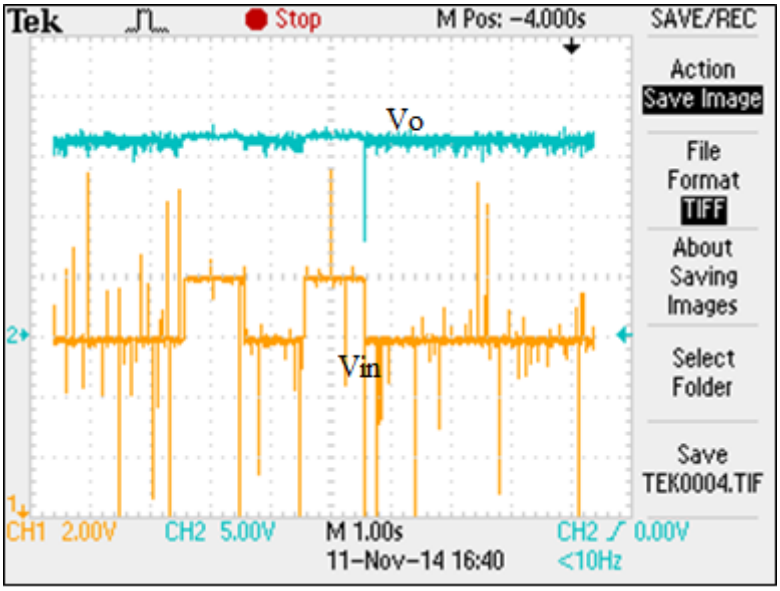


Fig. 4.16(b): Experimental result for change in input voltage.

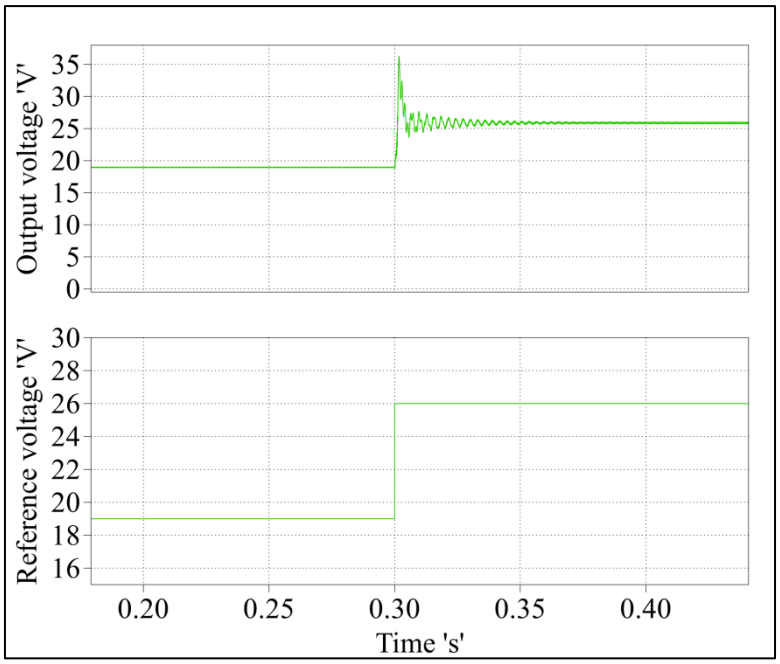


Fig. 4.17(a): Simulation result for step change in reference voltage.

4.5.3.2 Response to the variation in reference voltage V_{ref}

Figure 4.17 and 4.18 shows response of the output voltage with the variation in the reference voltage V_{ref}. Figure 4.17(a) and Fig.4.17(b) shows simulation and experimental result of step change in reference voltage from 19V to 26V. Figure

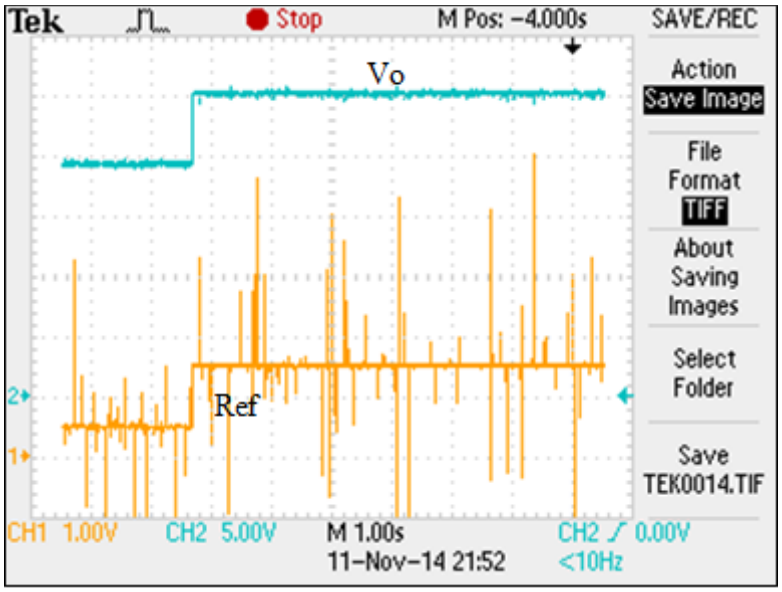


Fig. 4.17(b): Experimental result for step change in reference voltage.

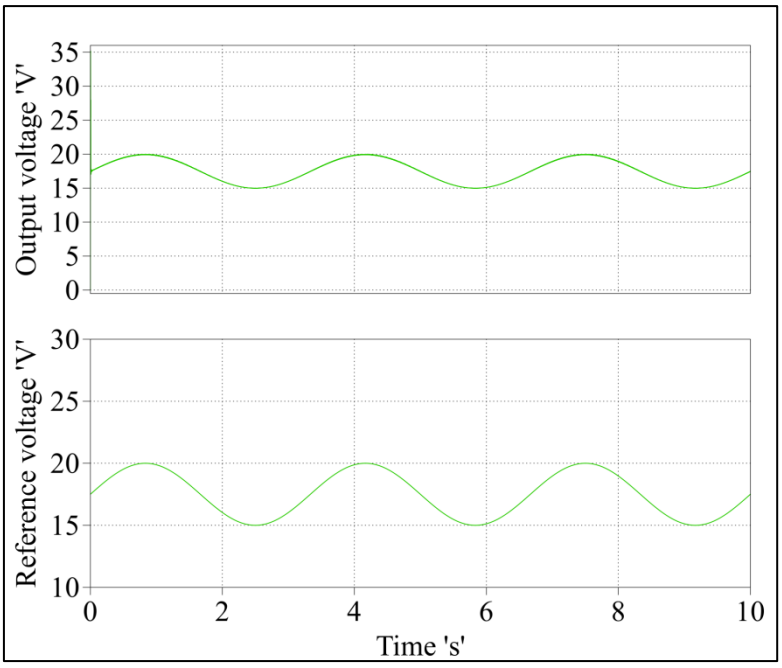


Fig. 4.18(a): Simulation result for continuous change in reference voltage.

4.18(a) shows output voltage for continuous change in reference voltage, here reference voltage is generated by adding DC to sinewave of 0.3 Hz frequency . In Fig. 4.18 (b) lower waveform is of scaled value of (V_{ref}-V_{in}).

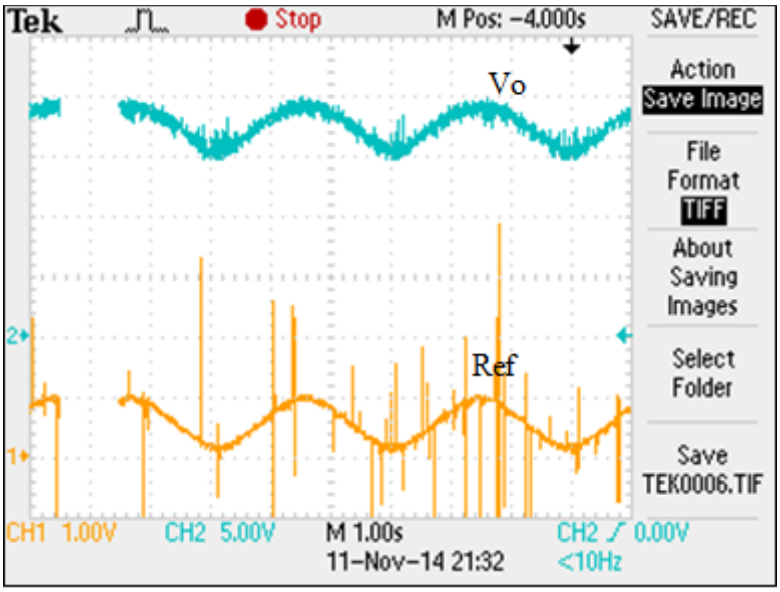


Fig. 4.18(b): Experimental result for continuous change in reference voltage.

4.6 Discussion

While studying application of one cycle control to Z source, Quasi Z source DC-DC and fourth-order step-up DC-DC Converter, following points have been observed

1) The input to the integrator is based on the state variable which is capacitor voltage V_C in Z source and V_{C1} and V_{C2} in quasi Z source converter. Therefore at startup, a maximum duty cycle limiter is needed to avoid the constant ON state of the switch unless the steady state voltages are reached. The maximum duty cycle limiter is realized using pulse generator with maximum duty cycle anded with pulses generated by S-R flipflop as shown in Fig. 4.3 and Fig. 4.5.

2) Due to parasitic resistances of inductors and capacitors, there is steady state output voltage error occurs due to drop in these components especially in high load condition.

3) In all the analysis above, it is assumed that the diode forward drop is zero. If diode forward drop is not zero, it will be interesting to study its effect. When diode is reverse biased, the integrator integrates the diode reverse voltage. During forward biased condition, input voltage to the integrator is negative voltage which is equal to

diode forward drop. It is observed that the one cycle controller inherently compensates for diode voltage drop and maintains the reference voltage.

Figure 4.19 shows the integrator waveform and capacitor voltage for Z source converter with diode forward voltage drop of one volt. It can be clearly observed that total duty cycle is increased for converter with diode drop. The reference is set at 50 V and Vin is 30 V. The diode drop is taken as 1 V. From the steady state analysis, the capacitor voltage with consideration of diode drop is given as

$$V_C = \frac{(1-D)}{(1-2D)}(V_{in} - V_f) \tag{4.20}$$

where V_f is the forward voltage drop. By substituting above values, D is found out as 0.295.

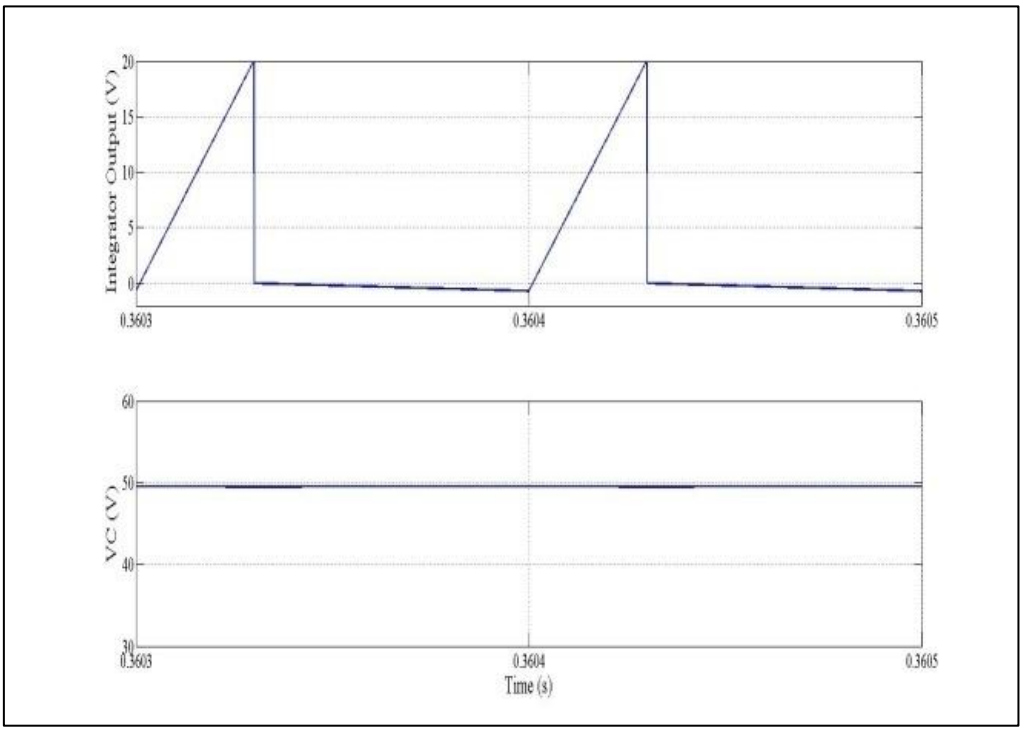


Fig. 4.19: Integrator output and Capacitor voltage.

4.7 Conclusion

One cycle control of Z-source, quasi Z-source and fourth-order step-up DC-DC converter offers fairly simple control of capacitor and dc link voltage. The diode voltage is chosen as switched variable. By choosing appropriate control equation, one can either control capacitor voltage or dc link voltage. One cycle control gives complete rejection of input voltage perturbation, inherent diode forward voltage drop compensation, and faster dynamic response. This technique can be easily extended to other converters of Z-source converter family.

Chapter 5

A High Step-up PWM DC-DC converter based on Quasi Z-source Topology

5.1 Introduction

A detailed study of fourth-order step-up converter is presented in chapter 2. This chapter presents a new topology of converter, which is an extension of fourth-order step-up converter by using cascading of two converters. Origin of this converter lies in fourth-order step-up PWM DC-DC converter and boost converter. Figure 5.1 shows cascade connection of conventional boost converter and fourth-order step-up PWM DC-DC converter. The proposed converter of Fig. 5.2 is derived by integrating both the switches S_1 and S_2 of Fig. 5.1 and replaced with a single switch as in quadratic boost converter. The main features of proposed converter are i) higher voltage gain ii) Common ground for switch; source and load and iii) continuous input current.

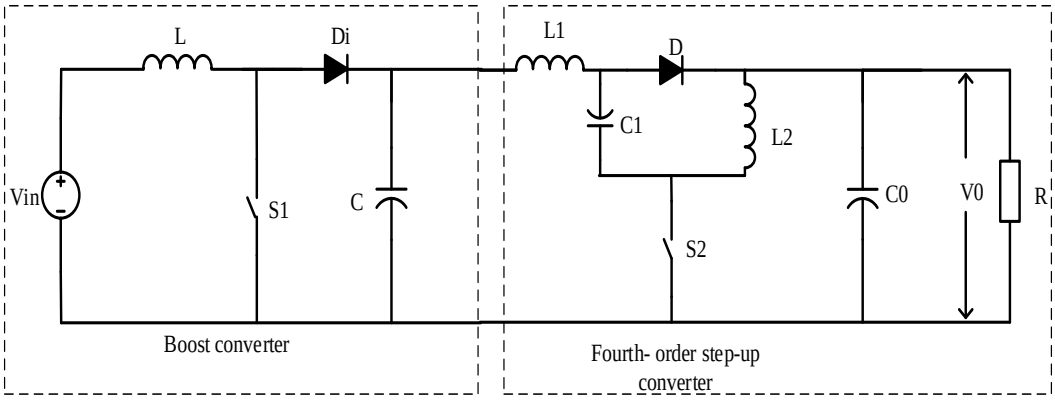


Fig. 5.1: Cascade connection of boost and fourth-order step-up converter.

In this chapter, a steady state analysis and design of the proposed converter is presented in section 5.2. Section 5.2 also presents boundary condition between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Power loss calculations by considering non-idealities in converter are carried out in section 5.3. The dynamic model and controller design for the proposed converter is presented in section 5.4. Section 5.5 presents simulation and experimental results of the converter and this section also include comparison results of the proposed

converter with the converter of [63] which has same number of elements as proposed converter. Conclusions are presented in section 5.6.

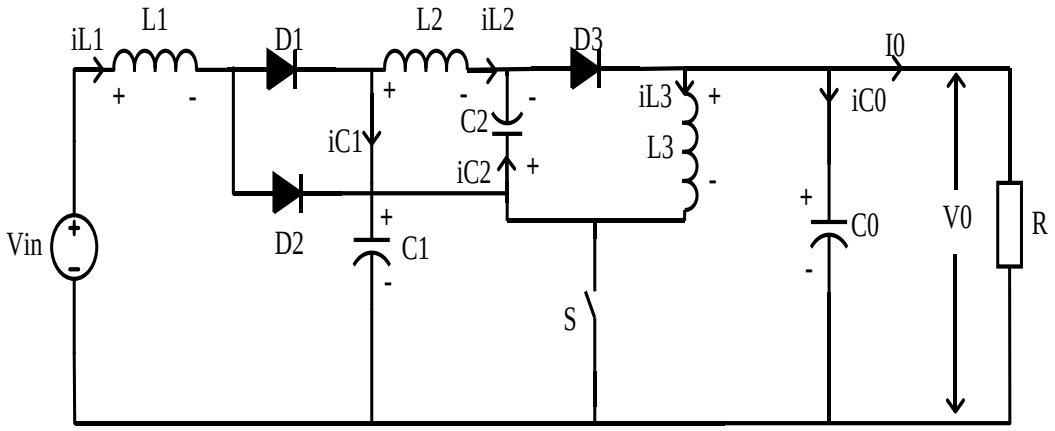


Fig. 5.2: Proposed Converter.

5.2 Steady-state analysis and boundary condition for DCM

The analysis of converter is based on the following assumptions.

(1) MOSFET and diodes are ideal.
(2) The capacitors are large enough, thus capacitor voltages are considered constant in one switching period.
(3) Inductors, capacitors and resistors are linear, time invariant and frequency independent.

In Fig. 5.2, the switch S is operating at switching frequency $f_s = 1/T$ with the duty ratio of switch is given by $D = T_{on}/T$, where T_{on} is the ON time of the switch. The proposed converter is operating in CCM. Fig. 5.5 shows nature of waveforms of current and voltage at different test points of converter. To evaluate the expression for output voltage, the steady state analysis of converter is carried out as following:

5.2.1 Steady state analysis

When switch is ON

For this period equivalent circuit of the converter is shown in Fig. 5.3. In this period switch S, diode D_2 is ON and diode D_1, D_3 are OFF. In this duration inductor current increases with slope proportional to voltage across respective inductor as in Fig. 5.5(b) and the voltages across inductors can be given by

$$V_{L1} = V_{in} \tag{5.1}$$

$$V_{L2} = V_{C1} + V_{C2} \tag{5.2}$$

$$V_{L3} = V_0 \tag{5.3}$$

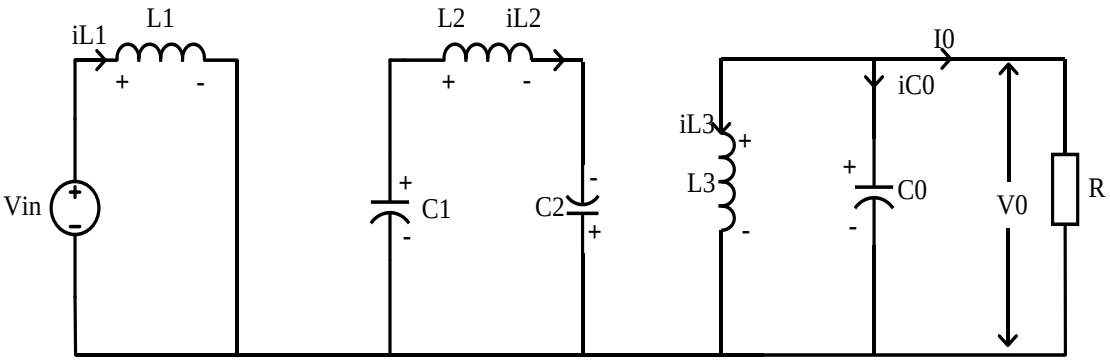


Fig. 5.3: Equivalent circuit of converter during switch-on.

When switch is OFF

The equivalent circuit for this duration is shown in Fig. 5.4. For this period diode D_1, D_3 are ON and switch S, diode D_2 is OFF. In this duration inductor current decreases as shown in Fig. 5.5(b) and the voltage across inductors can be given by

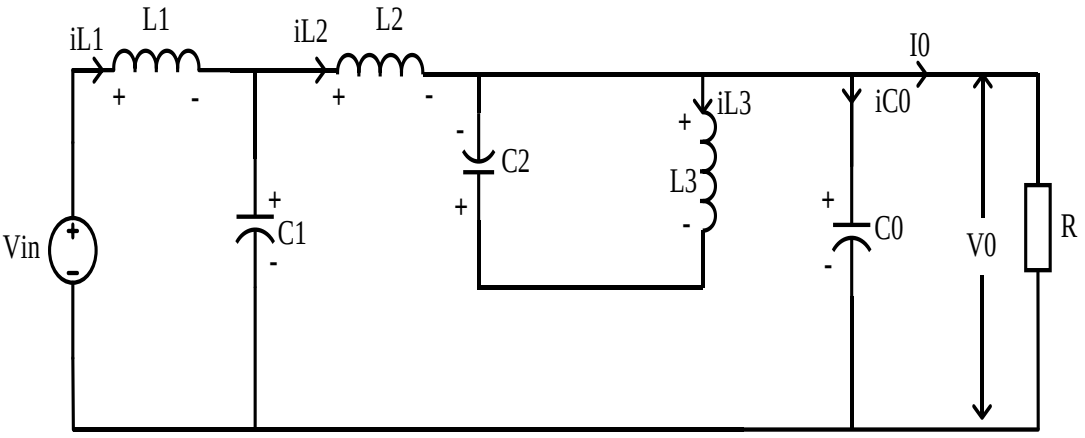


Fig. 5.4: Equivalent circuit of converter during switch-off.

$$V_{L1} = V_{in} - V_{C1} \tag{5.4}$$

$$V_{L2} = V_{C1} - V_0 \tag{5.5}$$

$$V_{L3} = -V_{C2} \tag{5.6}$$

Voltage across capacitor C_1 can be determined by applying volt-second balance principle on inductor L_1 and is given by

$$V_{C1} = \frac{V_{in}}{(1-D)} \tag{5.7}$$

Voltage across capacitor C_2 can be determined from volt-second balance for L_2 and is given

$$V_{C2} = \frac{DV_{C1}}{(1-2D)} \tag{5.8}$$

Similarly, voltage across capacitor C_0 can be given as

$$V_0 = \frac{(1-D)V_{C1}}{(1-2D)} \tag{5.9}$$

And it can also be given in terms of input voltage from equations (5.7) and (5.9) as

$$V_0 = \frac{V_{in}}{(1-2D)} \tag{5.10}$$

From equation (5.10), ideal DC voltage gain can be given as

$$M_{ideal} = \frac{V_0}{V_{in}} = \frac{1}{(1-2D)} \tag{5.11}$$

For ideal components $V_0I_0 = V_{in}I_{in}$, hence inductor current I_{L1} is

$$I_{in} = I_{L1} = \frac{I_0}{(1-2D)} = \frac{V_0}{R(1-2D)} = \frac{V_{in}}{R(1-2D)^2} \tag{5.12}$$

From converter equivalent circuits in ON and OFF state, by applying amp-second balance principle for capacitors, average value of inductor current I_{L2} are given as

$$I_{L2} = (1-D)\, I_{L1} = \frac{V_{in}(1-D)}{R(1-2D)^2} \tag{5.13}$$

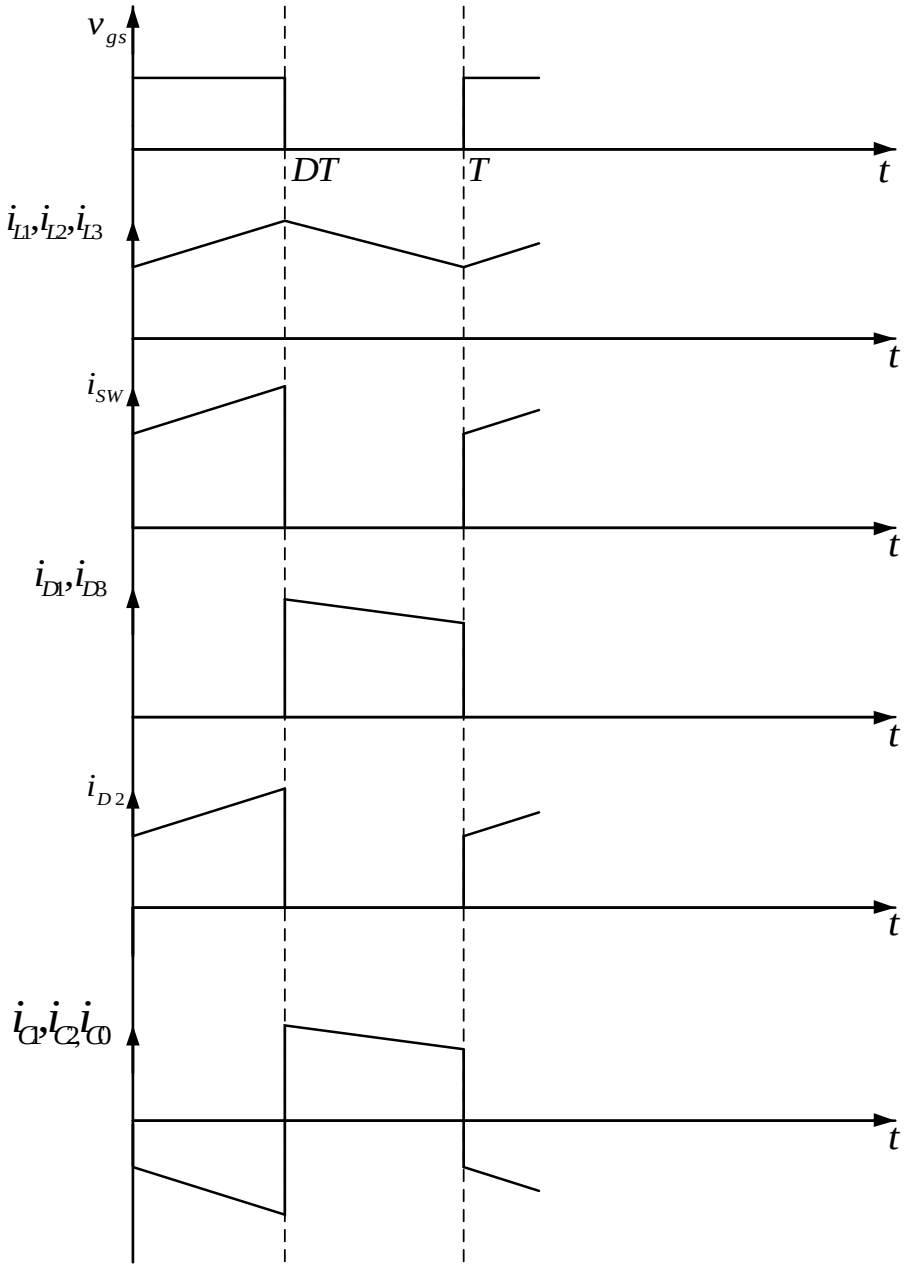


Fig. 5.5(a): Nature of Current waveforms of proposed converter.

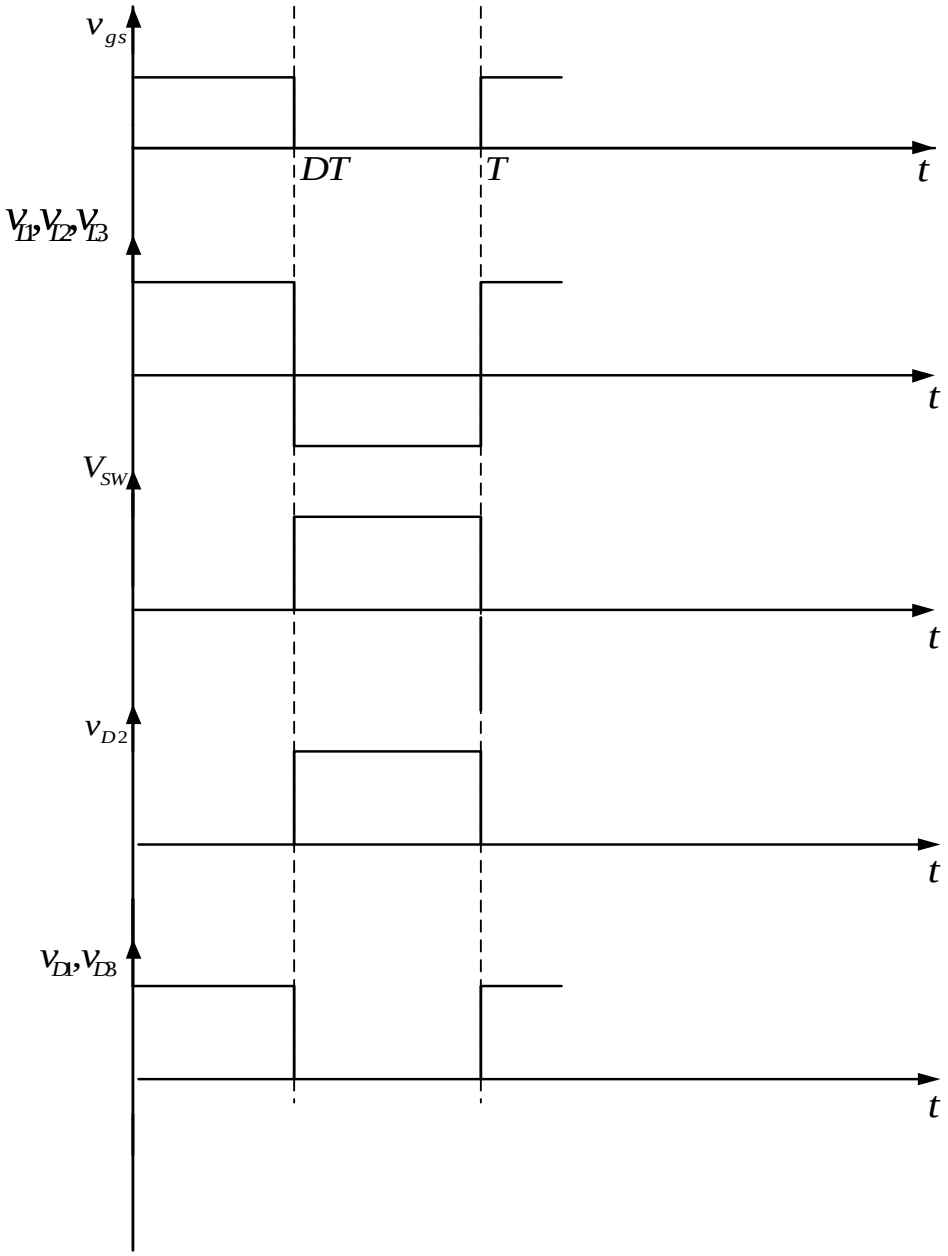


Fig. 5.5(b): Nature of Voltage waveforms of proposed converter.

Also average value of inductor current I_{L3} is

$$I_{L3} = \left(\frac{D}{1-2D}\right) I_0 = \frac{V_{in} D}{R(1-2D)^2} \tag{5.14}$$

5.2.3 Converter passive elements design

The passive elements are designed according to switching frequency and their voltage ripple and current ripple requirement. The peak to peak voltage ripple can be

calculated from the capacitor current. The capacitor current during switch-on time for output capacitor C_0 is can be given from Fig.5.4 as

$$C_0 \frac{\Delta V_0}{DT} = -I_{L3} - I_0 \tag{5.15}$$

Using equations (5.11), (5.14) and (5.15), the voltage ripple for capacitor C_0 is

$$\Delta V_0 = \left(\frac{1-D}{1-2D}\right)\frac{I_0 DT}{C_0} \tag{5.16}$$

Similarly voltage ripples across capacitors C_1 and C_2 can be calculated and given by

$$\Delta V_{C1} = \left(\frac{1-D}{1-2D}\right)\frac{I_0 DT}{C_1} \tag{5.17}$$

$$\Delta V_{C2} = \left(\frac{1-D}{1-2D}\right)\frac{I_0 DT}{C_2} \tag{5.18}$$

The capacitors value can be determined from (5.16)-(5.18) as

$$C_0 = I_0\left(\frac{1-D}{1-2D}\right)\frac{DT}{\Delta V_0} \qquad C_1 = \left(\frac{1-D}{1-2D}\right)\frac{I_0 DT}{\Delta V_{C1}} \qquad C_2 = \left(\frac{1-D}{1-2D}\right)\frac{I_0 DT}{\Delta V_{C2}} \tag{5.19}$$

From Fig. 5.3, the inductor current peak to peak ripple relations are given as

$$\Delta i_{L1} = \frac{V_{in} DT}{L_1} \qquad \Delta i_{L2} = \frac{(V_{C1} + V_{C2})DT}{L_2} \qquad \Delta i_{L3} = \frac{V_0 DT}{L_3} \tag{5.20}$$

A relevant factor of design converter elements is variation in inductor current; this factor corresponds to relation between current ripple to steady state value. The variation in inductor current using (5.7), (5.8), (5.12)-(5.14) and (5.20) is given as

$$\frac{\Delta i_{L1}/2}{I_{L1}} = \frac{(1-2D)^2 DTR}{2L_1}, \quad \frac{\Delta i_{L2}/2}{I_{L2}} = \frac{(1-2D)DTR}{2L_2(1-D)}, \quad \frac{\Delta i_{L3}/2}{I_{L3}} = \frac{(1-2D)TR}{2L_3} \tag{5.21}$$

To keep current ripple smaller than the DC component of inductor current, the condition which should be satisfied is

$$L_1 > \frac{D(1-2D)^2\, RT}{2} \quad , \quad L_2 > \frac{D(1-2D)RT}{2(1-D)} \quad , \quad L_3 > \frac{(1-2D)RT}{2} \tag{5.22}$$

5.2.4 Boundary condition between CCM/DCM

There are three cases for DCM mode of operation of converter. These are (i) inductor current i_{L1} in CCM and inductor current i_{L2}, i_{L3} are in DCM, (ii) inductor currents i_{L2}, i_{L3} are in CCM and inductor current i_{L1} in DCM and (iii) all inductor currents are in DCM. In this chapter first case is considered for analysis. A minimum diode current for diode D3 at boundary is

$$I_{D3\min} = I_{L2} + I_{L3} - \frac{\Delta I_D}{2} = 0 \tag{5.23}$$

Hence from equations (5.13), (5.14) and (5.20)

$$\frac{V_0}{R(1-2D)} - \frac{V_0 DT}{2L} = 0 \tag{5.24}$$

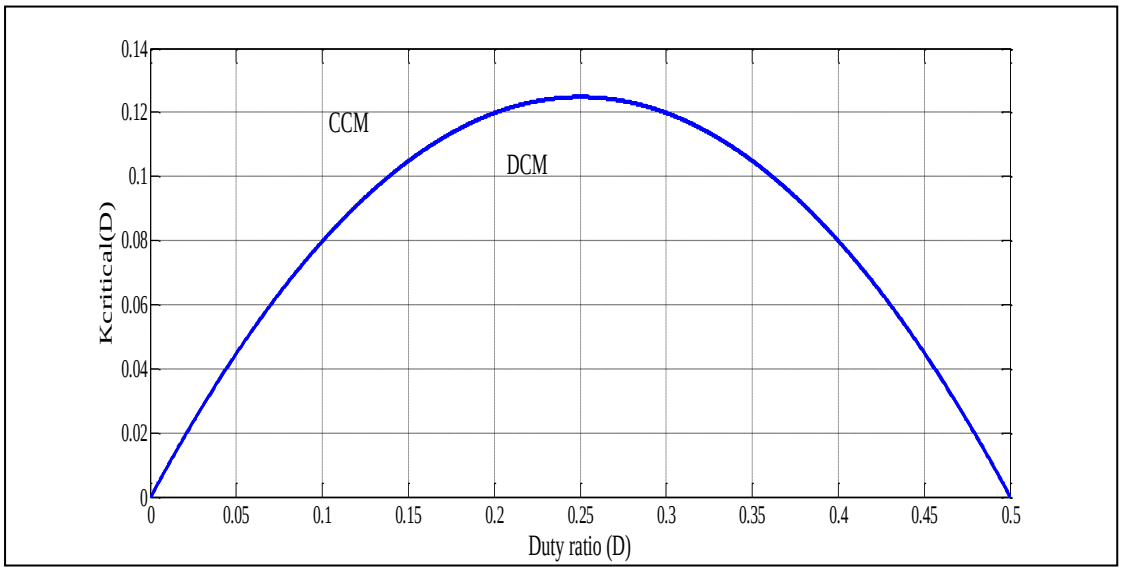


Fig. 5.6: Variation of K_c critical with Duty ratio D.

Therefore at boundary between CCM/DCM

$$K_c \geq D(1-2D) \tag{5.25}$$

Where, $K_c = \frac{2L}{RT}$ and L is equivalent of parallel combination of inductors L_2 and L_3.

Fig. 5.6 shows the plot of K_c critical as a function of duty ratio D.

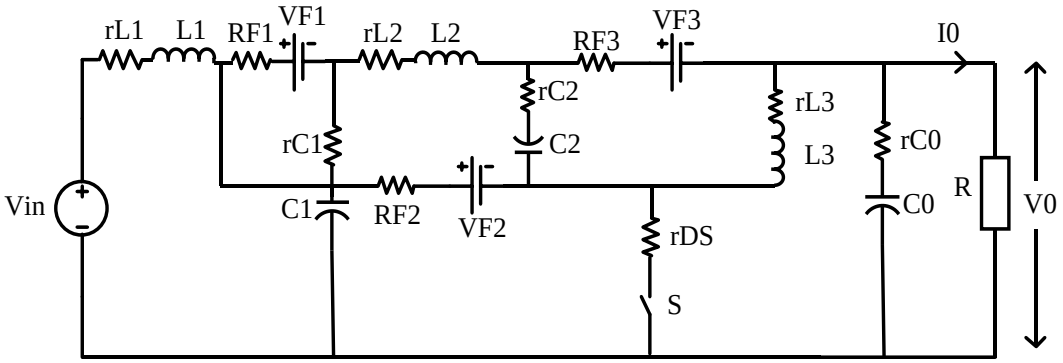


Fig. 5.7: Equivalent circuit of converter with non-idealities.

5.3 Power loss analysis and Voltage gain of non-ideal converter

5.3.1 Power loss analysis for converter in CCM

Fig. 5.7 shows equivalent circuit of proposed converter with parasitic resistances. The diodes are represented by voltage source in series with resistor and the MOSFET is represented by an ideal switch with its equivalent drain to source resistance. From equivalent circuit of converter and from switch waveform shown in Fig. 5.5(a), current through the switch S is

$$i_S = \begin{cases} i_{L1}+i_{L2}+i_{L3} & ON \\ 0 & OFF \end{cases} \tag{5.26}$$

An approximate RMS and average current through the switch S is can be derived from equations (5.12), (5.13), (5.14), (5.26) and switch current waveform in Fig. 5.5(a) as

$$I_{S(RMS)} = \frac{2\sqrt{D}}{(1-2D)} I_0, \; I_{S(AVG)} = \frac{2D}{(1-2D)} I_0 \tag{5.27}$$

Hence ohmic power loss in MOSFET S is

$$P_S = {I_{S(RMS)}}^2 r_{DS} = \frac{2D{I_0}^2}{(1-2D)^2} r_{DS} = \frac{2DP_0}{(1-2D)^2 R} r_{DS} \tag{5.28}$$

Here P_0 is output power, R is load resistance and r_{DS} is MOSFET ON resistance.

The approximate average and RMS value of current through diode D_1 is derived from circuit shown in Fig. 5.5 and using equation (5.12) and can be given as

$$I_{D1(RMS)} = \frac{\sqrt{1-D}}{(1-2D)} I_0,\ I_{D1(AVG)} = \frac{(1-D)}{(1-2D)} I_0 \tag{5.29}$$

The ohmic power loss in forward resistance R_{F1} of diode D_1 is

$$P_{RF1} = I_{D1(RMS)}{}^2 R_{F1} = \frac{(1-D) I_0{}^2}{(1-2D)^2} R_{F1} = \frac{(1-D) P_0}{(1-2D)^2 R} R_{F1} \tag{5.30}$$

Also power loss associated with the forward drop in diode D_1 is given as

$$P_{VF1} = V_{F1} I_{D1(AVG)} = V_{F1}\left(\frac{1-D}{1-2D}\right) I_0 = \left(\frac{1-D}{1-2D}\right)\frac{P_0 V_{F1}}{V_0} \tag{5.31}$$

Using (5.30) and (5.31), the total power loss in diode D_1 is

$$P_{D1} = P_{RF1} + P_{VF1}$$

$$P_{D1} = \left[\frac{(1-D) R_{F1}}{(1-2D)^2 R} + \frac{(1-D) V_{F1}}{(1-2D) V_0}\right] P_0 \tag{5.32}$$

Similarly power losses in diodes D_2 and D_3 can be expressed as

$$P_{D2} = \left[\frac{D R_{F2}}{(1-2D)^2 R} + \frac{D V_{F2}}{(1-2D) V_0}\right] P_0 \tag{5.33}$$

$$P_{D3} = \left[\frac{(1-D) R_{F3}}{(1-2D)^2 R} + \frac{(1-D) V_{F3}}{(1-2D) V_0}\right] P_0 \tag{5.34}$$

It is to be noted that the switch and diode current expressions in the above equations can be used to decide switch current ratings. In PWM converters power losses in inductors is due to mainly winding loss, and core loss is negligible. The winding loss is depends up on winding resistance and RMS value of current flowing through it.

The approximate RMS value of current through inductor L_1 can be derived from equation (5.12) as

$$I_{L1(RMS)} = I_{in} = \frac{1}{(1-2D)} I_0 \tag{5.35}$$

And similarly for inductor L_2 and L_3, approximate RMS value of currents are can be given from equations (5.13) and (5.15) as

$$I_{L2(RMS)} = \frac{(1-D)}{(1-2D)} I_0 \tag{5.36}$$

$$I_{L3(RMS)} = \frac{D}{(1-2D)} I_0 \tag{5.37}$$

Resulting power losses in inductors are

$$P_{r_{L1}} = I_{L1(RMS)}{}^2 r_{L1} = \left(\frac{1}{1-2D}\right)^2 \frac{P_0 r_{L1}}{R} \tag{5.38}$$

$$P_{r_{L2}} = I_{L2(RMS)}{}^2 r_{L2} = \left(\frac{1-D}{1-2D}\right)^2 \frac{P_0 r_{L2}}{R} \tag{5.39}$$

$$P_{r_{L3}} = I_{L3(RMS)}{}^2 r_{L3} = \left(\frac{D}{1-2D}\right)^2 \frac{P_0 r_{L3}}{R} \tag{5.40}$$

Capacitor current during switch-on and switch-off period can be given from Fig. 5.3 and Fig. 5.4 as

$$i_{C1} = \begin{cases} -I_{L2} & ON \\ I_{L1} - I_{L2} & OFF \end{cases} \tag{5.41}$$

$$i_{C2} = \begin{cases} -I_{L2} & ON \\ I_{L3} & OFF \end{cases} \tag{5.42}$$

$$i_{C0} = \begin{cases} -(I_0 + I_{L3}) & ON \\ I_{L2} - I_0 & OFF \end{cases} \tag{5.43}$$

Approximate RMS value of I_{C1}, I_{C2} and I_{C0} can be derived using equations (5.41) - (5.43) and (5.12)-(5.14) as

$$I_{C1(RMS)} = I_{C2(RMS)} = I_{C0(RMS)} = \left(\frac{\sqrt{D(1-D)}}{1-2D} \right) I_0 \tag{5.44}$$

The power loss associated with the capacitors from equation (5.44) is

$$P_{rc} == \frac{D(1-D)(rc_1 + rc_2 + rc_0) P_0}{(1-2D)^2 R} \tag{5.45}$$

The total power loss in converter is sum of all the power losses and it can be given by

$$P_{loss} = P_S + P_D + P_{r_{L1}} + P_{r_{L2}} + P_{r_{L3}} + P_{rc} \tag{5.46}$$

5.3.2 DC voltage transfer gain of non-ideal high step up DC-DC converter

The efficiency of non-ideal high step up DC-DC converter is given by

$$\text{Efficiency } \eta = \frac{P_0}{P_{in}} = \frac{V_{0-NI} I_0}{V_{in} I_{in}} = \frac{1}{1 + \frac{P_{loss}}{P_0}} \tag{5.47}$$

Where, $V_{0\text{-NI}}$ is output voltage of non-ideal converter. From equations (5.12) and (5.47)

$$\eta = M_{non-ideal} (1-2D) \tag{5.48}$$

Where $M_{non\text{-}ideal}$ is $V_{0\text{-NI}}/V_{in}$ which is voltage gain for converter with non-idealities. Since all non-idealities considered are series non-idealities, only voltage gain will be affected. From equation (5.48) and (5.11),

$$M_{non-ideal} = \frac{\eta}{1-2D} = \frac{1}{1 + \frac{P_{loss}}{P_0}} \times \frac{1}{1-2D} \tag{5.49}$$

$$M_{non-ideal} = \frac{1}{1+\frac{P_{loss}}{P_0}} M_{ideal} \tag{5.50}$$

In order to determine actual gain of converter, it is required to calculate all the losses for given non-ideal parameters and duty ratio. Equation (5.50) gives voltage gain of non-ideal converter.

5.4 Small-signal model and controller design

5.4.1 Small-signal model

Since the converter has six dynamic elements, it would be interesting to study small signal model of the converter. The state space averaging approach is used to obtain the small-signal model. The inductor currents and capacitor voltages are chosen as state variables, the input voltage is chosen as input variable and input current as an output variable. The small-signal state-space averaging equations are obtained from the converter equivalent circuits for switch ON and switch OFF duration as given in Fig. 5.3, and Fig. 5.4 respectively.

The state vector can be defined as

$$x(t) = \left[i_{L1}(t) \quad i_{L2}(t) \quad i_{L3}(t) \quad v_{C1}(t) \quad v_{C2}(t) \quad v_{C0}(t) \right]^T \tag{5.51}$$

The input to the converter is single voltage source so the input vector can be given as

$$u(t) = \left[v_{in}(t) \right] \tag{5.52}$$

And the output vector is

$$y(t) = \left[i_{in}(t) \right] \tag{5.53}$$

The differential equations governing the dynamics of state vector x(t) for switch ON period can be written in state space form as $K\dot{x} = A_1 x + B_1 u$

Where,

$$K=\begin{pmatrix} L_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & L_3 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_0 \end{pmatrix} \quad A_1=\begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & -\frac{1}{R} \end{pmatrix} \quad B_1=\begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

From the equivalent circuit of Fig. 5.4, the state equations for switch OFF duration can be written in state space form as $K\dot{x}=A_2x+B_2u$

Where

$$A_2=\begin{pmatrix} 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & -1 \\ 0 & 0 & 0 & 0 & -1 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -\frac{1}{R} \end{pmatrix} \quad \text{and} \quad B_2=\begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

The average matrix can be given as

$$A=dA_1+(1-d)A_2$$

And average matrix B is

$$B=dB_1+(1-d)B_2$$

The small-signal relationship among the state variables is derived by applying small signal perturbations to input voltage and duty ratio of the switch. The state equations of the small signal ac model are

$$K\frac{d\hat{x}(t)}{dt}=A\hat{x}(t)+B\hat{u}(t)+\left\{\left(A_1-A_2\right)X+\left(B_1-B_2\right)U\right\}\hat{d}(t) \qquad (5.54)$$

Equation (5.54) can be written as

$$\begin{pmatrix} L_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & L_3 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_0 \end{pmatrix} \frac{d}{dt} \begin{pmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{i}_{L3}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C2}(t) \\ \hat{v}_{C0}(t) \end{pmatrix} =$$

$$\begin{pmatrix} 0 & 0 & 0 & -D' & 0 & 0 \\ 0 & 0 & 0 & 1 & D & -D' \\ 0 & 0 & 0 & 0 & -D' & D \\ D' & -1 & 0 & 0 & 0 & 0 \\ 0 & -D & D' & 0 & 0 & 0 \\ 0 & D' & -D & 0 & 0 & -\frac{1}{R} \end{pmatrix} \begin{pmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{i}_{L3}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C2}(t) \\ \hat{v}_{C0}(t) \end{pmatrix} + \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \left[\hat{v}_{in}(t)\right] + \begin{pmatrix} V_{C1} \\ V_{C2}+V_0 \\ V_{C2}+V_0 \\ -I_{L1} \\ -(I_{L2}+I_{L3}) \\ -(I_{L2}+I_{L3}) \end{pmatrix} \hat{d}(t) \tag{5.55}$$

After Laplace transformation and rearrangement, equation (5.55) becomes

$$\begin{pmatrix} sL_1 & 0 & 0 & D' & 0 & 0 \\ 0 & sL_2 & 0 & -1 & -D & D' \\ 0 & 0 & sL_3 & 0 & D' & -D \\ -D' & 1 & 0 & sC_1 & 0 & 0 \\ 0 & D & -D' & 0 & sC_2 & 0 \\ 0 & -D' & D & 0 & 0 & sC_0+\frac{1}{R} \end{pmatrix} \begin{pmatrix} \hat{i}_{L1}(s) \\ \hat{i}_{L2}(s) \\ \hat{i}_{L3}(s) \\ \hat{v}_{C1}(s) \\ \hat{v}_{C2}(s) \\ \hat{v}_{C0}(s) \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \left[\hat{v}_{in}(s)\right] \tag{5.56}$$

$$+ \begin{pmatrix} V_{C1} \\ V_{C2}+V_0 \\ V_{C2}+V_0 \\ -I_{L1} \\ -(I_{L2}+I_{L3}) \\ -(I_{L2}+I_{L3}) \end{pmatrix} \hat{d}(s)$$

To obtain the transfer function of output voltage to input voltage, the perturbation of duty ratio is assumed to be zero and therefore

$$G_{vg} = \left.\frac{\hat{v}_{C0}(s)}{\hat{v}_{in}(s)}\right|_{\hat{d}(S)=0} = \frac{D'^2\left(s^2 L_3 C_1 - 2D + 1\right)}{Q} \tag{5.57}$$

where

$$Q = s^5 L_1 L_2 L_3 C_1 C_2 \left(sC_0 + \frac{1}{R} \right) + s^4 L_1 L_3 C_1 C_2 \left(D^2 + D'^2 \right) + s^3 \left(sC_0 + \frac{1}{R} \right)$$
$$\left\{ L_1 L_3 C_2 + D^2 L_1 L_3 C_1 + D'^2 L_1 L_2 C_1 + D'^2 L_2 L_3 C_2 \right\} +$$
$$s^2 \left(D^2 \left(L_1 C_2 + D'^2 C_2 L_2 - 2D'^2 L_1 C_1 \right) + D^4 L_1 C_1 + D'^4 \left(L_1 C_1 + L_3 C_2 \right) \right)$$
$$+ s \left(sC_0 + \frac{1}{R} \right) \left\{ D'^2 \left(D^2 L_3 + D'^2 L_2 + L_1 \right) \right\} - 2D^2 D'^4 + D^4 D'^2 + D'^6$$

To obtain transfer function of input conductance, the perturbation of duty ratio is assumed to be zero and therefore

$$G_{ig} = \left. \frac{\hat{i}_{L1}(s)}{\hat{v}_{in}(s)} \right|_{\hat{d}(S)=0} = \frac{\begin{array}{l} s^4 L_2 L_3 C_1 C_2 \left(sC_0 + \frac{1}{R} \right) + s^3 D^2 C_1 C_2 \left(L_2 + L_3 \right) + s^2 \left(sC_0 + \frac{1}{R} \right) \\ \left\{ D^2 L_3 C_1 + D'^2 L_2 C_1 + L_3 C_2 \right\} \\ + s \left(D^4 C_1 + D^2 C_2 + D'^4 C_1 - 2D^2 D'^2 C_1 \right) + \left(sC_0 + \frac{1}{R} \right) D'^2 \end{array}}{Q} \quad (5.58)$$

To obtain transfer fuction of output voltage to duty ratio, the perturbation of input voltage is assumed to be zero and therefore

$$G_{vd}(s) = \left. \frac{\hat{v}_{C0}}{\hat{d}(s)} \right|_{\hat{v}_{in}(s)=0} = \frac{\begin{array}{l} G_1 V_{C1} + G_2 \left(V_{C2} + V_0 \right) + G_3 \left(V_{C2} + V_0 \right) + G_4 \left(-I_{L1} \right) \\ + G_5 \left(-I_{L2} - I_{L3} \right) + G_6 \left(-I_{L2} - I_{L3} \right) \end{array}}{Q} \quad (5.59)$$

where G_1-G_6 details are given in appendix-C. It can be observed that the control transfer function is of sixth order. From the negative terms in numerator, it can be stated that it contains RHP zeros.

From equations (5.57) and (5.58), the transfer function of output impedance Zo(s) can be obtained as

$$Z_0(s)=\frac{D'^2\left(s^2L_3C_1-2D+1\right)}{s^4L_2L_3C_1C_2\left(sC_0+\frac{1}{R}\right)+s^3D^2C_1C_2\left(L_2+L_3\right)+s^2\left(sC_0+\frac{1}{R}\right)\left\{D^2L_3C_1+D'^2L_2C_1+L_3C_2\right\}+s\left(D^4C_1+D^2C_2+D'^4C_1-2D^2D'^2C_1\right)+\left(sC_0+\frac{1}{R}\right)D'^2} \quad (5.60)$$

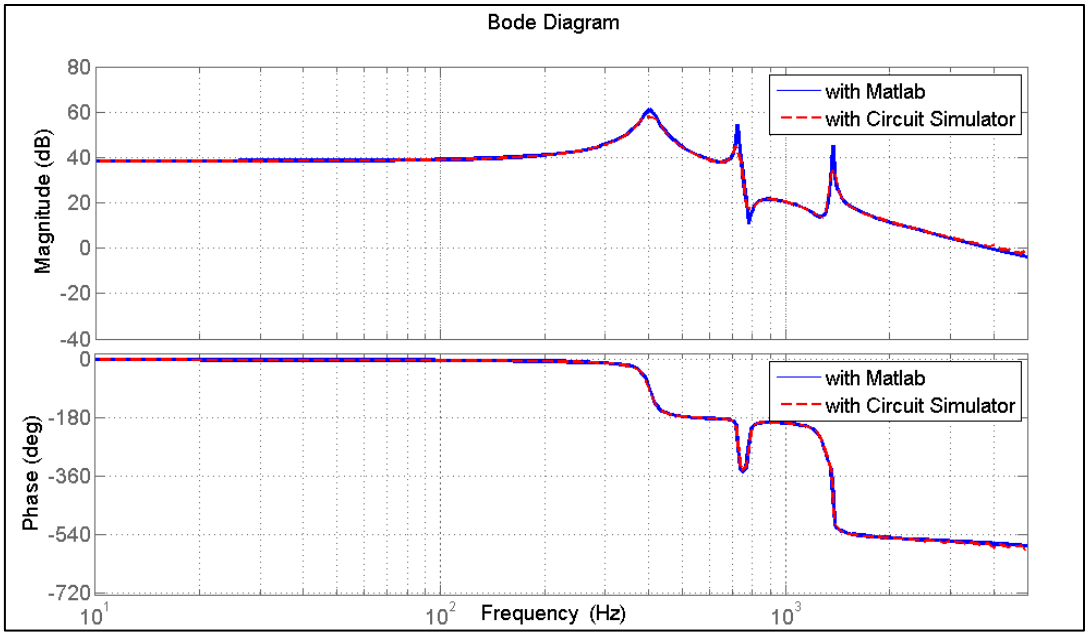


Fig. 5.8(a): Open loop control to output voltage frequency response.

5.4.2 Controller design

In Fig.5.8 (a) solid line shows theoretical open-loop frequency response bode plot obtained from equation (5.59) for control to output voltage for D=0.2 and Vin = 15V. The passive elements values used are L_1=200µH, L_2=L_3= 400µH, C_1=C_2=C_0= 90µF and load resistance of 40Ω which are closer to values used in the experiment later. For obtaining bode plot, non-idealities of inductors and capacitors have not been considered.

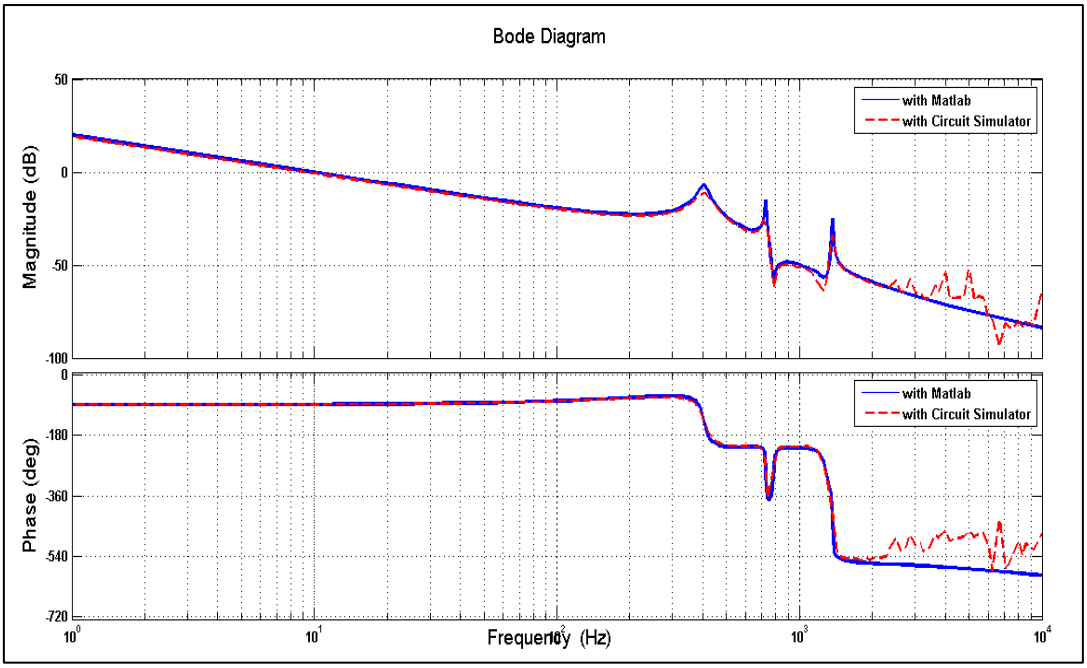


Fig. 5.8(b): Compensated frequency response.

It can be observed in Fig. 5.8(a) that bode plot obtained by using circuit simulator software PLEXIM is very well matched with theoretical bode plot obtained by using MATLAB.

With the above values of L, C, D and R and for input voltage Vin= 15 V, the transfer function (5.59) is given as

$$G_{vd}(s)=\left.\frac{\hat{v}_{C0}}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0}=\frac{(s-303\pm j8148)(s+46\pm j4903)(s-44486)}{(s+97.2\pm j2533)(s+20.4\pm j4560)(s+21.3\pm j8594)} \tag{5.61}$$

From the transfer function, it can be observed that, there three complex poles and two complex zeros and one real zero. One complex zero and one real zero lies in the right half plane (RHP) which makes this system as a non-minimum phase system.

In Fig. 5.8(b) solid line shows a theoretical bode plot of loop gain with compensation for voltage mode controller design. A PI controller structure as given in equation (5.62) is used for compensation. Feedback gain is taken as unity. Theoretical bode plot obtained by using MATLAB is verified by a closed loop bode plot obtained from circuit simulation software, and it is shown by dotted line in Fig. 5.8(b). Control design tool 'SISOTOOL' which is provided with MATLAB is used for controller design. The compensator is designed as follows. It can be observed that first peak of

$G_{vd}(s)$ occur at 403 Hz or 2533 rad/s which is a pole frequency. After this frequency, all the RHP zero frequencies, LHP zero frequency and other pole frequencies occur. Therefore it would be desirable to bring first peak well below 0 dB to reduce the effects of RHP zeros and other poles. A Gain Margin (GM) of 10dB at the frequency 2533 rad/s is chosen. The approximate Q at this frequency is 13.04 which can be obtained from equation (5.61). The 'zero' frequency of equation (5.62) 'ω_Z' is chosen to be same as first peak which is 2533 rad/s. By using MATLAB, it can be found that the dc gain of transfer function is 83.33. Therefore, with some calculations, 'ω_I' can be found as 0.737 rad/s.

$$C(s) = \frac{1 + \frac{s}{\omega_Z}}{\frac{s}{\omega_I}} \tag{5.62}$$

With this compensation design, one gets a phase margin of almost 90 degrees. However due to non-minimum phase characteristics, limitation of bandwidth with this method is severe. Hence it could be advantageous to use another control techniques like average current mode control [46], [64], or nonlinear techniques like sliding mode control [65] to get better control performance.

5.4 Simulation and Experimental Results

The laboratory prototype is implemented to verify the theoretical analysis and simulation results. The details of system specification and components used are given in table 5.1. The converter operates in open loop with 20 KHz switching frequency. The TL494 is used to generate gate signal. Fig. 5.9(a) shows the calculated and experimental values of output voltage with variation in duty ratio. Fig. 5.9(b) shows theoretical and experimental values of the converter's efficiency for different values of duty ratio or output power. The output voltage and efficiency plot shows that the result of analysis is quite closer to practical values. In Fig.5.10 and Fig.5.11 shows steady state simulation and experimental results of converter in CCM for D=0.126. It can be seen from the figure that observed waveforms matches with the simulation results.

Table 5.1: Specification of laboratory prototype.

S.No.	Parameter	Value
1	Input voltage	15 V
2	Switching frequency	20 KHz
3	Inductors L_1,L_2,L3,r_{L1},r_{L2}, r_{L3}	197.3µH,412.1µH401.4µH,0.048Ω, 0.072Ω, 0.072Ω
4	Capacitor C_1,C2,r_{C1}, r_{C2}	90.89µF, 89.83µF, 0.159Ω, 0.161Ω
5	Capacitor C_0,r_{C0}	90.17µF,0.166Ω
6	MOSFET switch, R_{DS}	IRF540N,44mΩ
7	Diodes ,V_F	MUR460, 1.05V
8	Duty Cycle D	For CCM = 0.126, 0.361
9	Load resistance	ForCCM:40Ω ,89 Ω

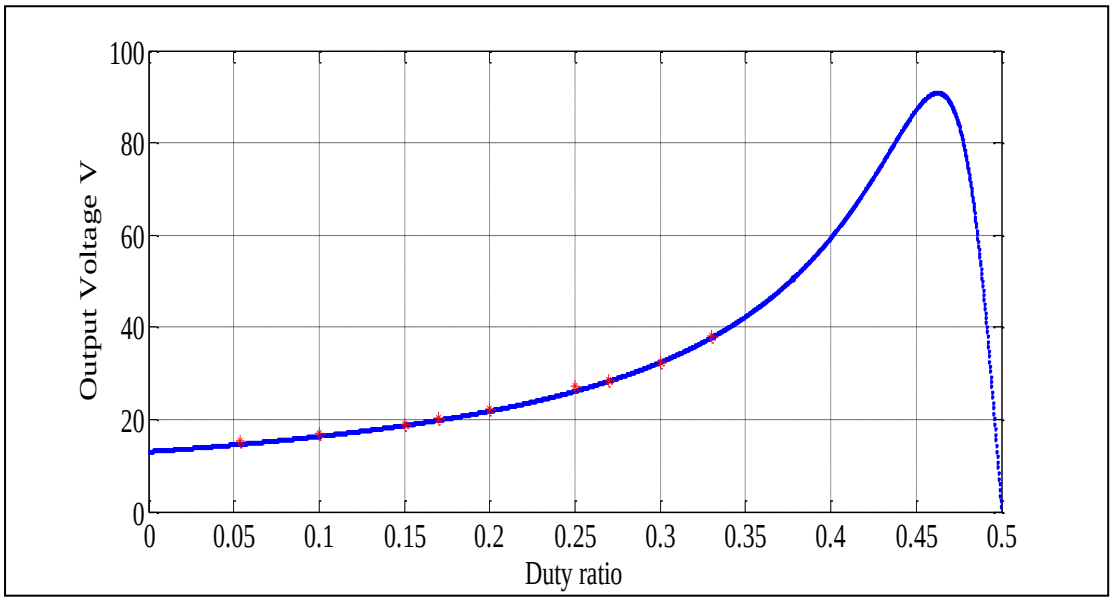


Fig. 5.9(a): Output voltage as a function of D for input voltage 15V.

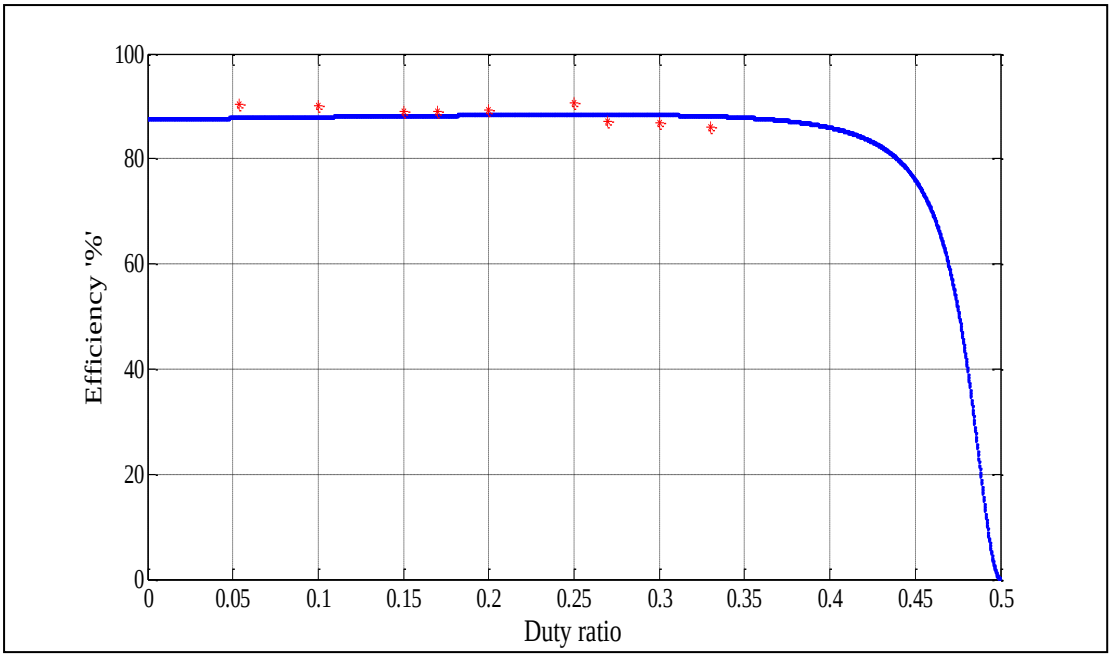
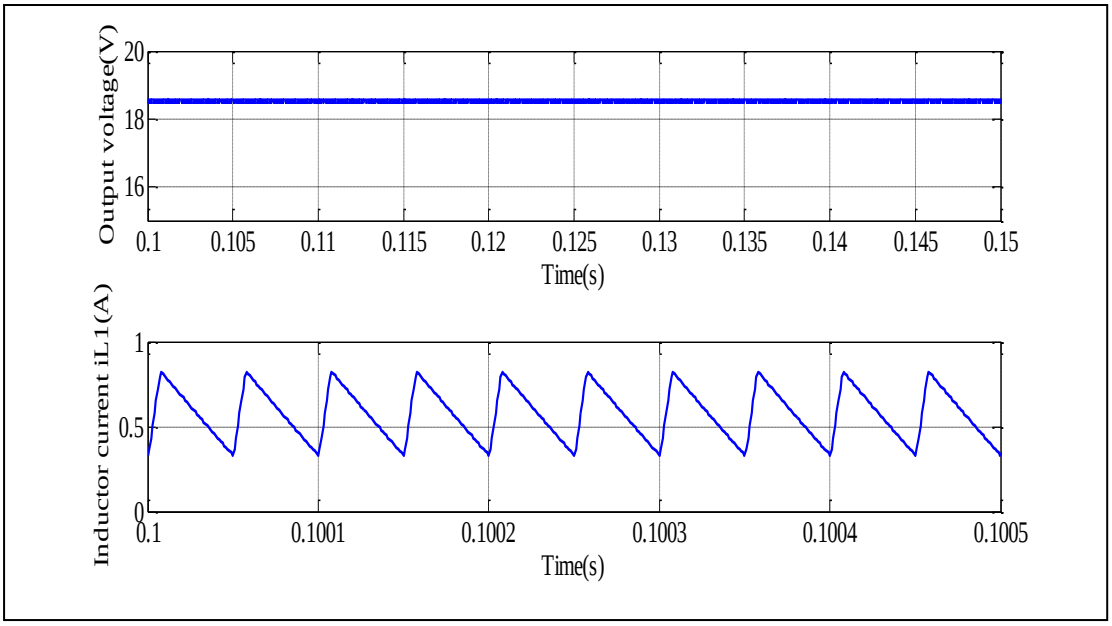


Fig. 5.9(b): Efficiency as a function of D.



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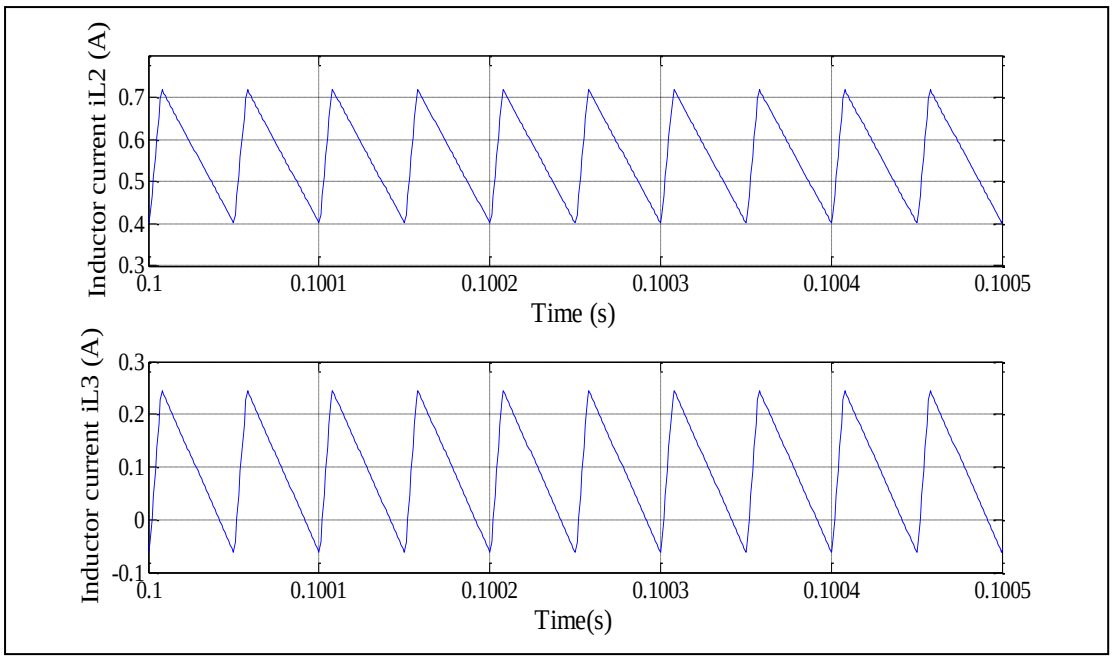

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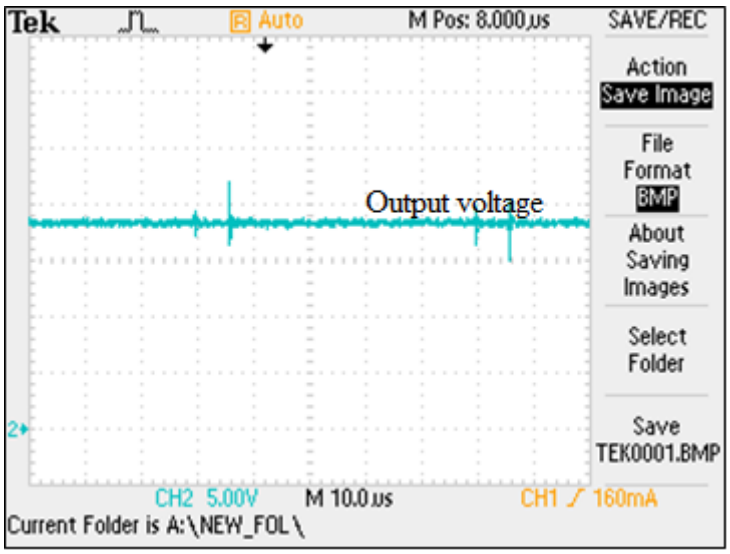
Fig. 5.10(a) Simulation results, (b) Simulation results of inductor current iL2 and iL3 for D=0.126.



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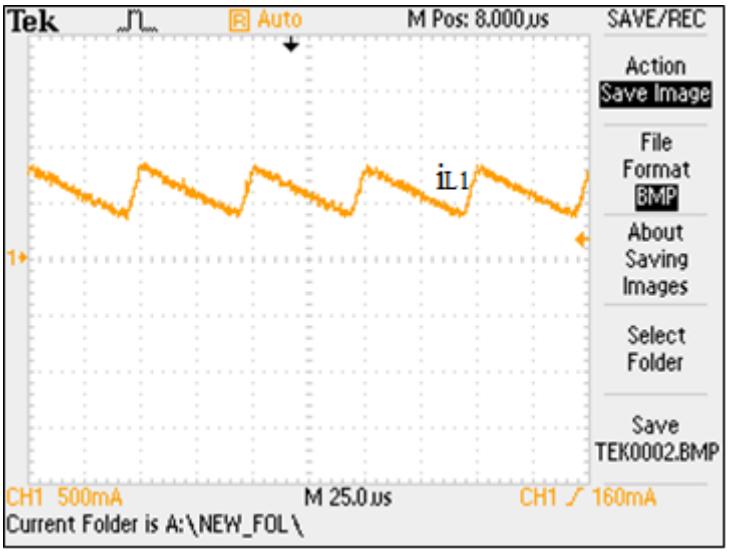
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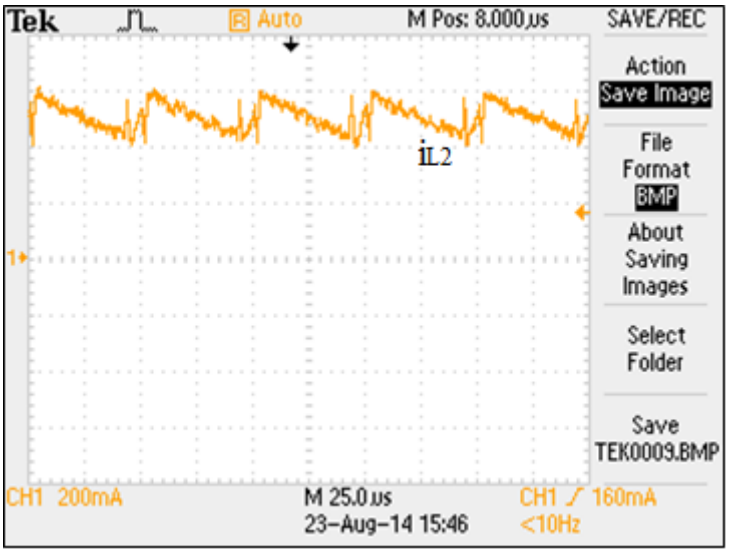
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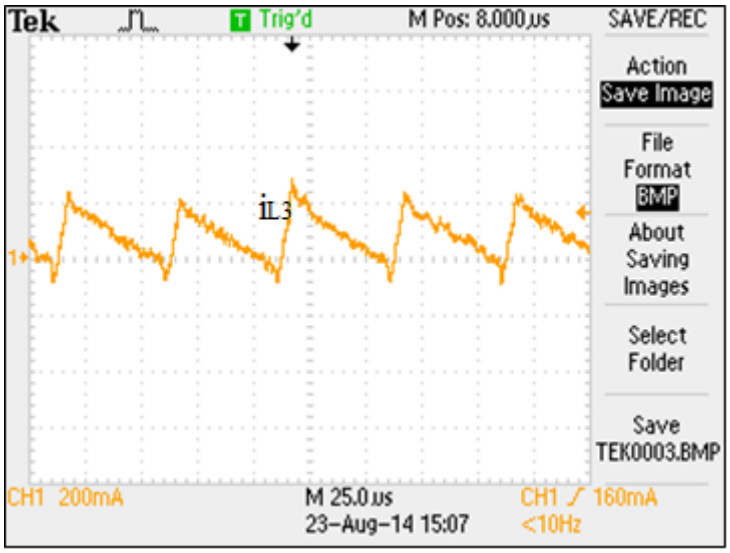
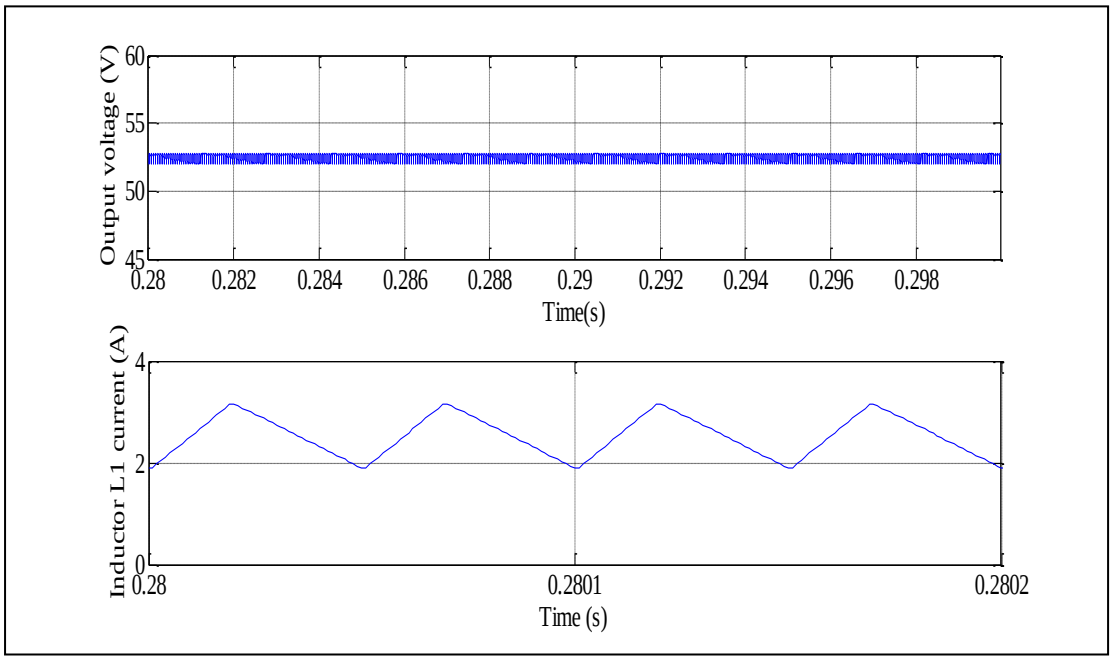


(d)

Fig. 5.11: (a) Experimental output voltage (b) Inductor current IL1, (c) Inductor current IL2, (d): Inductor current IL3 for D=0.126.

In Fig.5.12(a), (b) and (c) shows simulation and experimental results for converter operating in CCM at duty ratio D = 0.361 which also shows a considerable match between simulation and experiment



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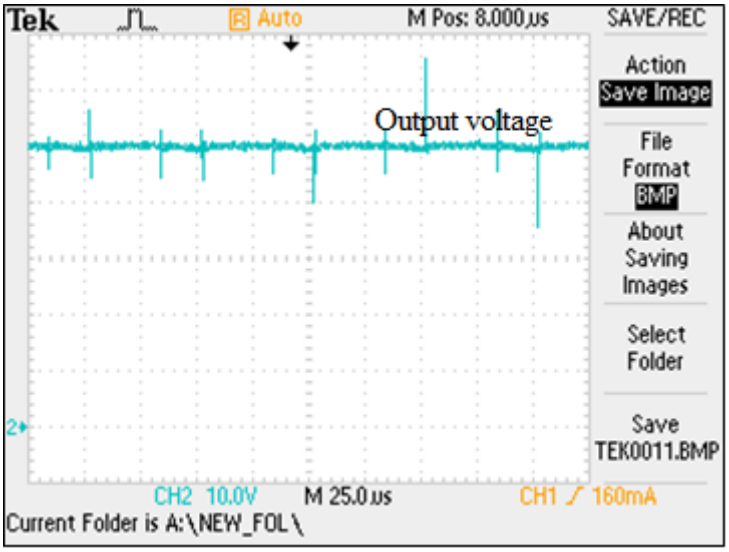

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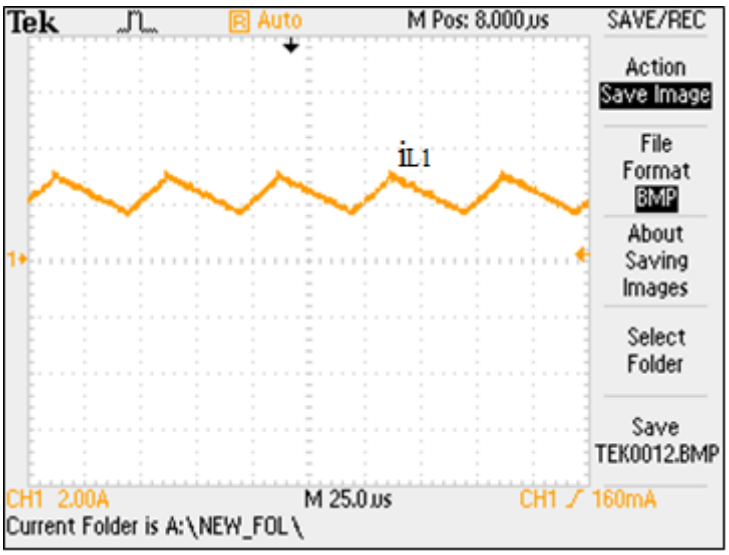
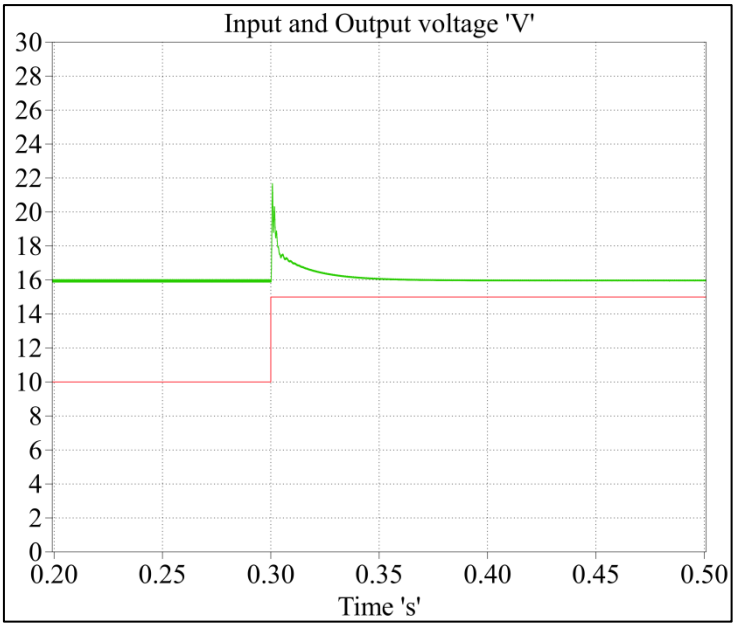


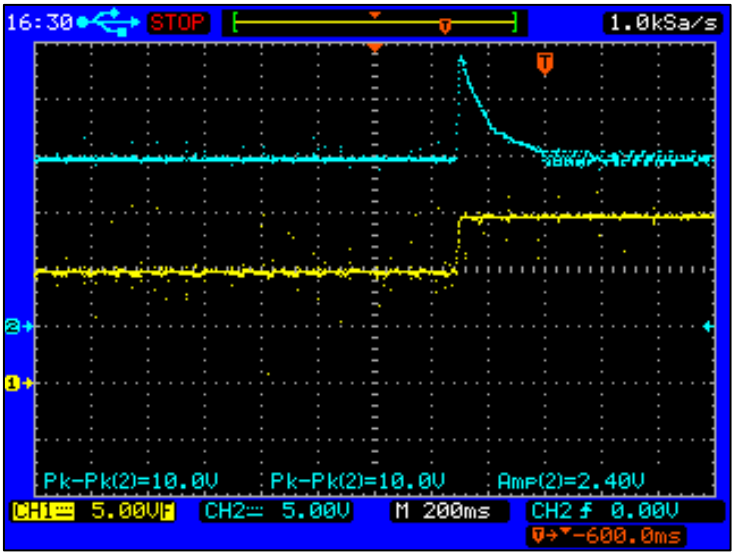
(c)

Fig. 5.12: (a) Simulation results, (b) Experimental output voltage, (c) Inductor L1 current for D=0.361.

Figure 5.13 shows response of controller for step increase in input voltage from 10V to 15V and keeping reference voltage constant. Similarly controller response for step decrease in input voltage is shown in Fig. 5.14.



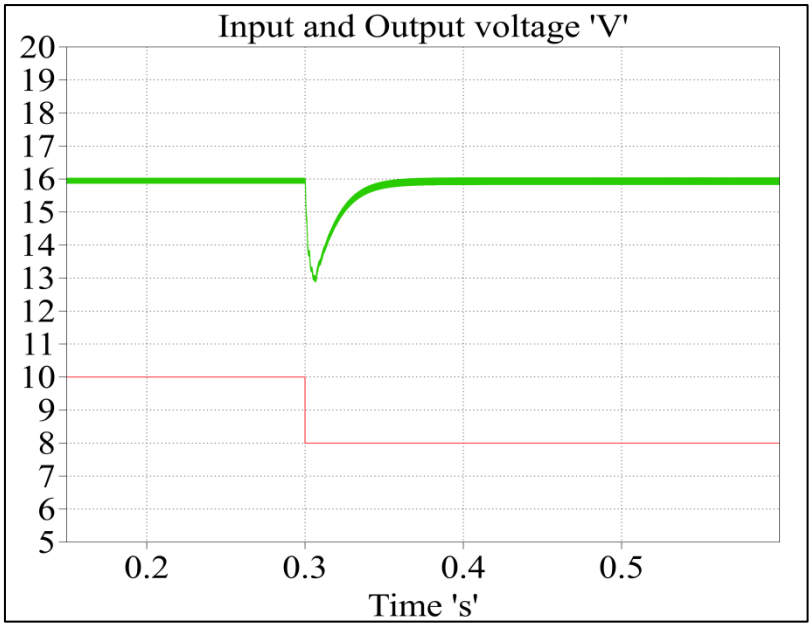
(a)



(b)

Fig. 5.13: Controller response for step increase in input voltage, (a) Simulation results, (b) Experimental results.

Figure 5.15 shows simulation and experimental result of controller response for step change in reference voltage. In Fig. 5.15 reference voltage is change from 14.3V to 16.6V and input voltage is constant. Figure 5.16 shows results for step decrease in reference voltage.



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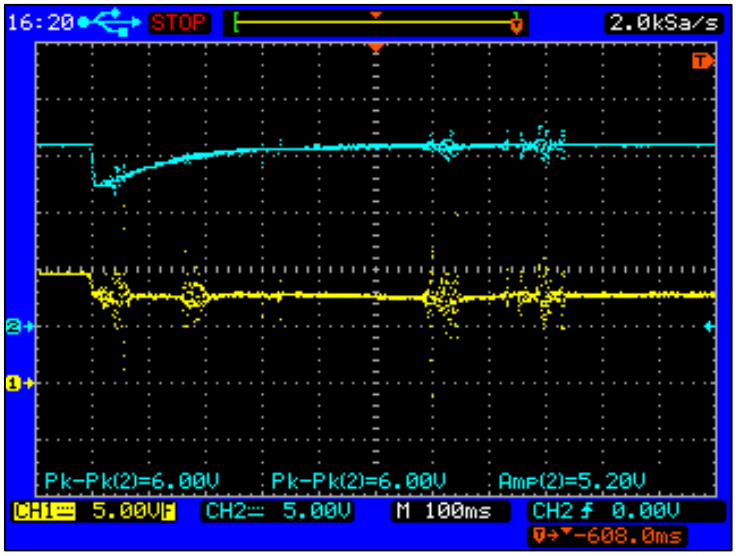

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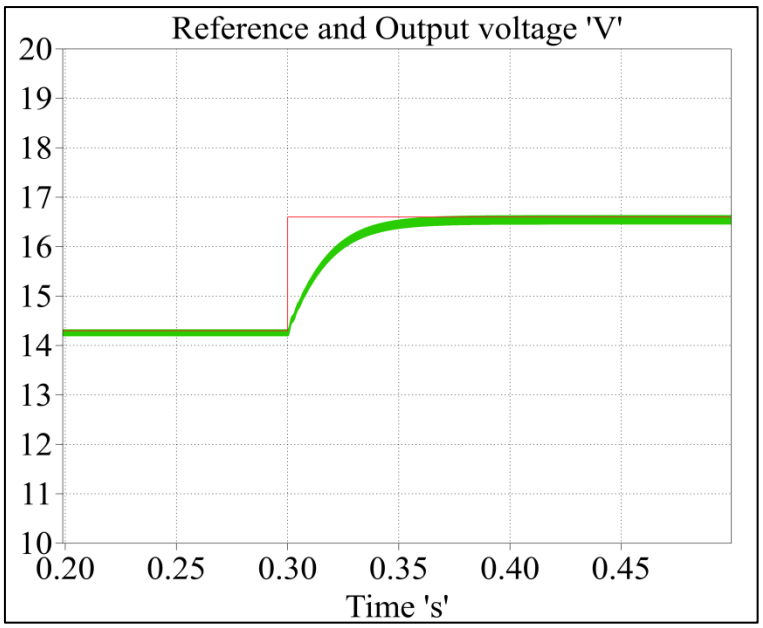
Fig. 5.14: Controller response for step decrease in input voltage, (a) Simulation results, (b) Experimental results.



(a)

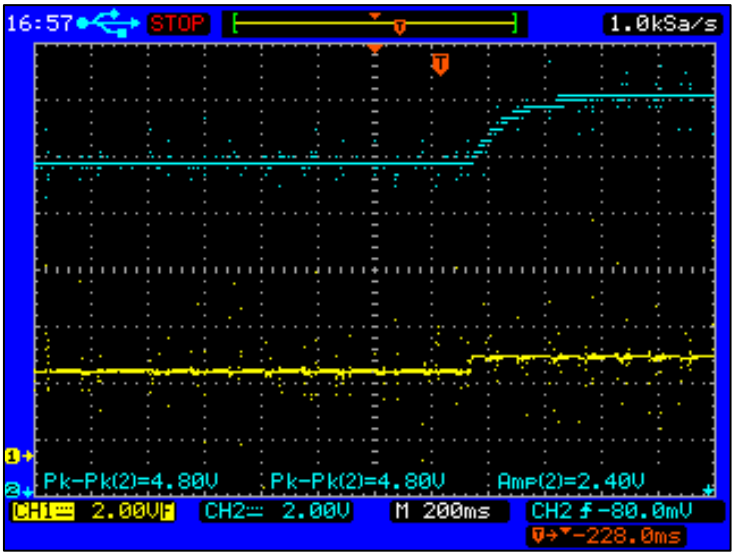


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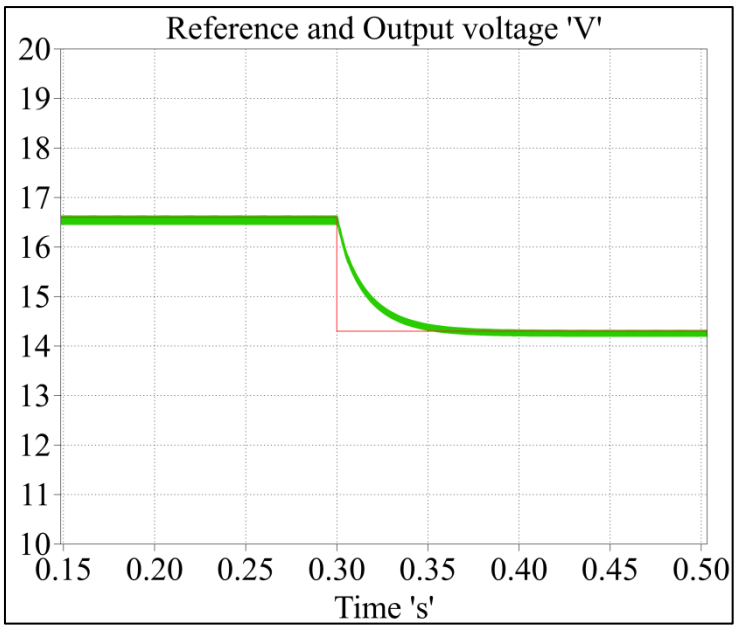
Fig. 5.15: Controller response for step increase in reference voltage, (a) Simulation results, (b) Experimental results.

A. Comparison with converter [28]

Since the proposed converter has its origin in Z-source based converter, it would be quite interesting to compare it with the previously proposed converter of similar origin. The proposed converter is compared with the PWM Z-source DC-DC converter [28] .



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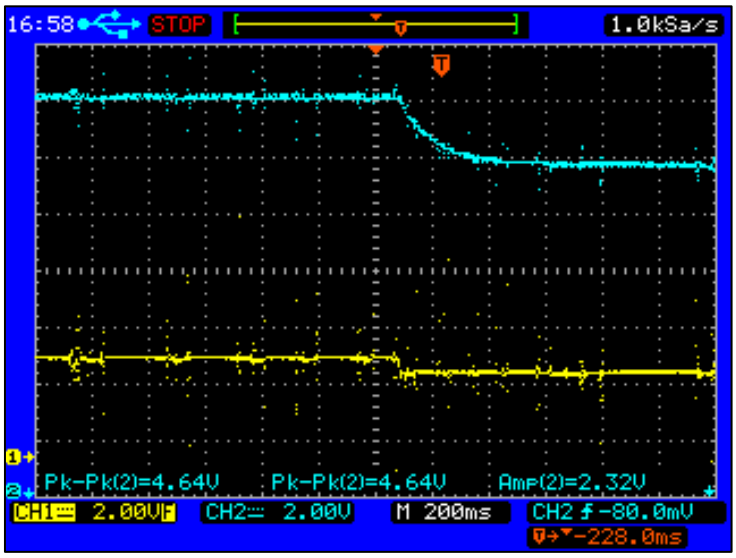


(b)

Fig. 5.16: Controller response for step decrease in reference voltage, (a) Simulation results, (b) Experimental results.

The laboratory prototype of converter [28] is built for same voltage and power level for comparison. Fig. 5.17(a) shows comparison of the variation in output voltage with duty ratio for both the converter for same operating conditions.

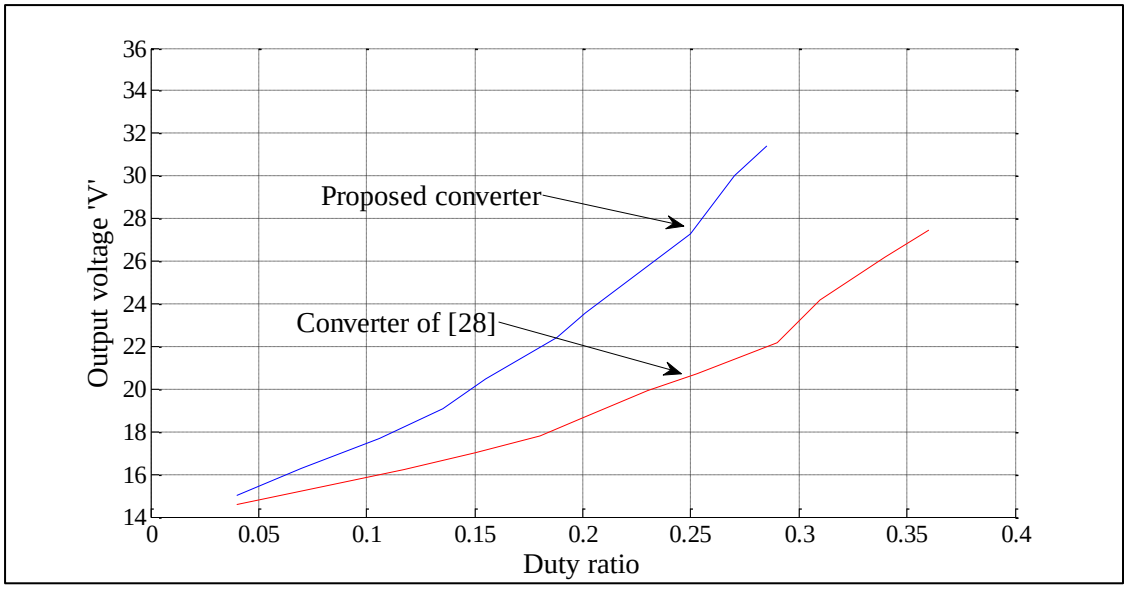


Fig. 5.17(a): Comparison of output voltage against duty ratio.

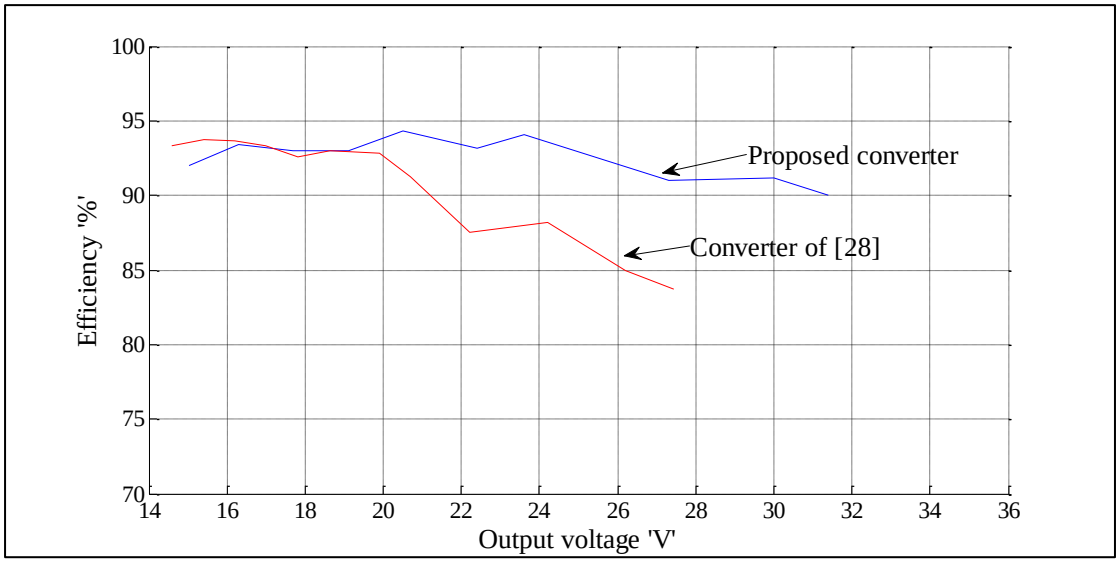


Fig. 5.17(b): Converter's efficiency comparison for different output voltage.

Fig. 5.17 (b) shows relationship of efficiency with output voltage, for input voltage 15V and load resistance 40Ω. In Fig.5.17 (b), the efficiency of converter [28] is higher for output voltage below 19V and for rest of the portion it is lower than the proposed converter.Table 5.2 gives comparison of the proposed converter with the

converter given in [28]. Figure 5.17(a) shows comparison of output voltages of both the converters. Variation in efficiency for various values of output voltage is shown in Fig. 5.17(b). The main advantages of the proposed converter in comparison with [28] are high voltage gain, continuous input current, common ground for input, load and switch, and low voltage stress on two capacitors for same output voltage. Further, it can be noted that the expressions for voltage stress on switch, diodes and capacitors can be used for component design of proposed converter.

As listed in table, the converter limitations are high stress over active switch and number of diodes.

Table 5.2: Comparison of proposed converter with converter of [28].

Converter	**Converter of** [28]	**Proposed converter**
Voltage gain	$(1-D)/(1-2D)$	$1/(1-2D)$
No. of passive components	6	6
No. of active switch	1	1
No. of diode	1	3
Continuous input current	No	Yes
Floating active switch	Yes	No
Common ground for source, load and switch	No	Yes
Voltage stress on active switch	$V_{in}/(1-2D)$	$((1+D)V_{in})/(1-2D)$
Voltage stress across diodes	$V_{in}/(1-2D)$	$V_{D1}=\frac{1}{1-D}V_{in}, V_{D2}=\frac{2D}{(1-2D)(1-D)}V_{in},$ $V_{D3}=\frac{1}{(1-2D)(1-D)}V_{in}$
Voltage stress on capacitors	$V_{C1}=V_{C2}=V_{Cf}=\frac{1-D}{1-2D}V_{in}$	$V_{C1}=\frac{1}{1-D}V_{in}$, $V_{C2}=\frac{D}{1-2D}V_{in}$, $V_{C0}=\frac{1}{1-2D}V_{in}$

6. Conclusion

This chapter proposes a new single switch non-isolated high step up converter. The converter has desirable features like continuous input current, common rail for source, load and switch, high gain for low duty ratio. The steady state analysis for CCM has been presented and boundary operating condition for CCM/DCM has been discussed. Expressions for efficiency and voltage gain for non-ideal converter are derived. The small signal model and controller design of converter has been presented. Prototypes were built to verify the practicability of converter and controller. Experimental results validate the theoretical analysis and simulation results.

Chapter 6

High step-up converters based on quadratic boost converter

6.1 Introduction

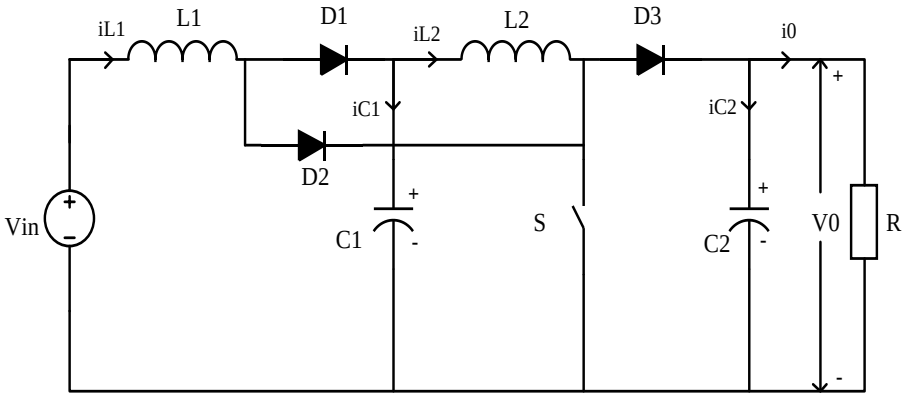
Among many techniques to achieve high step-up voltage gain, cascading of the converter is one of the alternatives. For example, cascading two boost converters can achieve high step-up voltage gain. The cascade converter requires two sets of power devices, magnetic cores and control circuits, which is complex and expensive. The system stability of the cascaded structure is another big issue, and the control circuit should be designed carefully [66]. Quadratic boost converter as shown in Fig. 6.1(a) integrates two switches of cascaded converter into one switch to reduce circuit complexity. The voltage conversion ratio is same as cascaded converter which is a quadratic expression hence named as quadratic boost converter. The circuit is simplified and instability caused by cascaded structure is avoided. The voltage conversion range is quite higher in quadratic boost converter than the conventional boost converter. Some alternative topologies like quadratic boost converter with reduced capacitor voltage stress based on Reduced Redundant Power Processing (R2P2) were also proposed in the literature [67].

Tapped-inductor based boost converter as shown in Fig. 6.1(b) is another alternative used to get high step up gain [68], [69], [70] [71], [72]. In addition to a duty cycle, another degree of freedom is a turns ratio in tapped inductor to obtain a high voltage gain. However due to the tapped-inductor structure, the converter faces the problem of highly pulsating input current especially when turns-ratio is higher or current is larger. However it is observed that switch voltage stress in tapped-boost converter is lower compared to the boost converter for the same output voltage.

If one combines a wide conversion range of quadratic boost converter and degree of freedom due to tapping of inductor in a tapped boost, it results in a two different converter topologies. Figure 6.2(a) shows a tapped-inductor quadratic boost converter which can be called as semi-tapped quadratic boost converter because only output inductor is tapped. Figure 6.3(a) is another combination of tapped-inductor and quadratic boost converter which can be called as fully tapped quadratic boost converter since both input and output inductors are tapped. To the best of author's knowledge, these converters along with its detailed performance analysis are not yet

reported in the literature. The detailed steady state performance analysis of semi-tapped and fully tapped quadratic boost is presented in this chapter.

The organization of the chapter is as follows; the section 6.2 explains the operation and carries out a steady state analysis for proposed converters. The voltage gain and efficiency analysis for non-ideal converters are presented in section 6.3. Section 6.4 shows a performance comparison of both the proposed converters considering voltage gain, efficiency and voltage stress as key features. Section 6.5 gives the experimental results which verify a theoretical analysis and simulation results. Conclusions are given in section 6.6.



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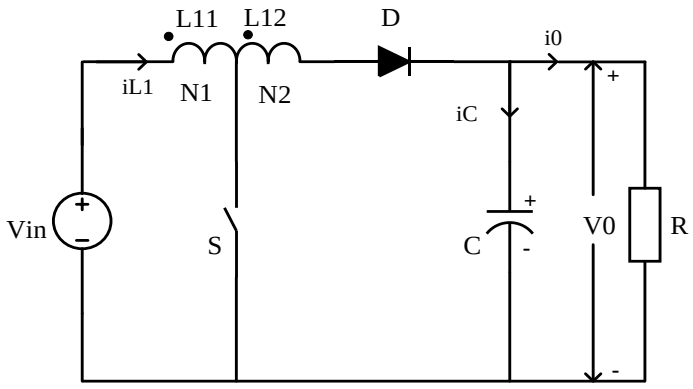


(b)

Fig. 6.1: (a) Quadratic boost converter and (b) tapped boost converter.

6.2 Principle of operation and Steady state analysis

To simplify the analysis, following assumptions are made:

1) Capacitors are large enough, thus the voltage across them can be considered as

constant in one switching period.

2) The components of the converters are ideal.

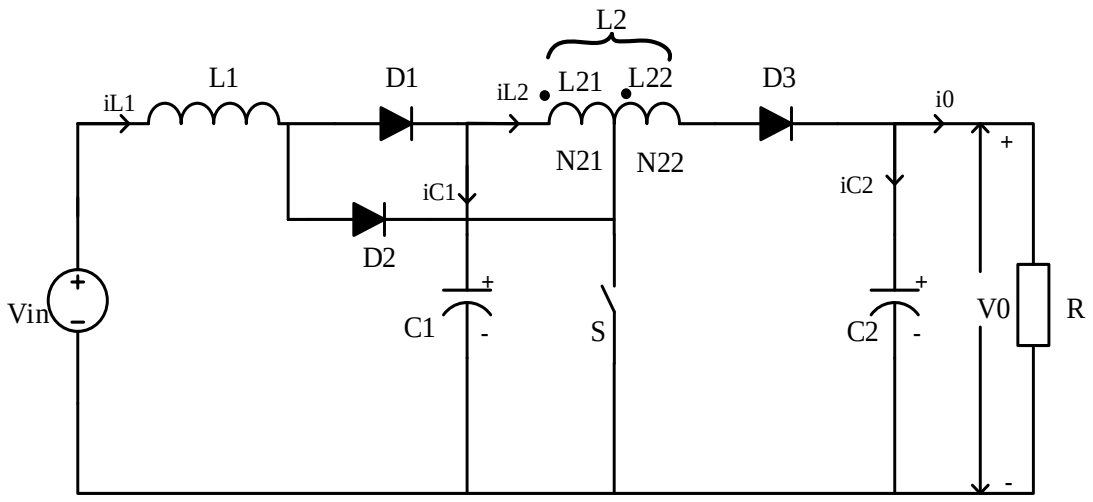
3) The coupling coefficient is equal to one.

4) Converters are operating in Continuous Conduction Mode (CCM).

6.2.1 Semi-tapped quadratic boost converter

Figure 6.2(a) shows the semi-tapped quadratic boost converter with untapped inductor L_1 and tapped-inductor L_2. Tapping divides inductor L_2 in two parts L_{21} and L_{22} with number of turns N_{21} and N_{22} respectively. Figure 6.2(b) shows the circuit when switch S is ON. Diodes D_1 and D_3 are reverse biased and diode D_2 conducts. During switch-on period, voltage across inductor L_1 is the input voltage and voltage across inductor L_{21} is same as capacitor voltage V_{C1}. Figure 6.2(c) shows the circuit when switch S is OFF. Diode D_1 and D_3 conducts and diode D_2 gets reverse biased. In this mode inductor supplies stored energy to the load and capacitors similar to quadratic boost converter.

For the analysis, inductor current i_{L1}, capacitor voltage v_{C1} and v_{C2} are chosen as state variables. For the tapped inductor, core flux φ_2 is chosen as a state variable instead of current.



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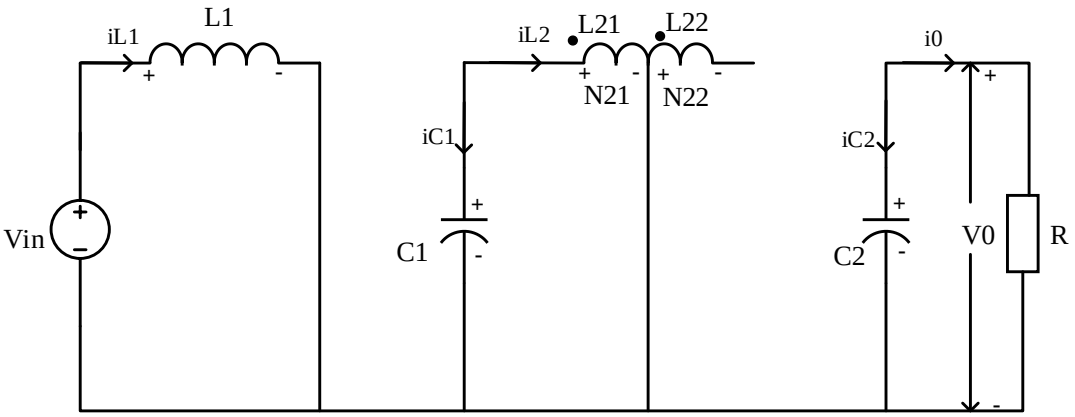

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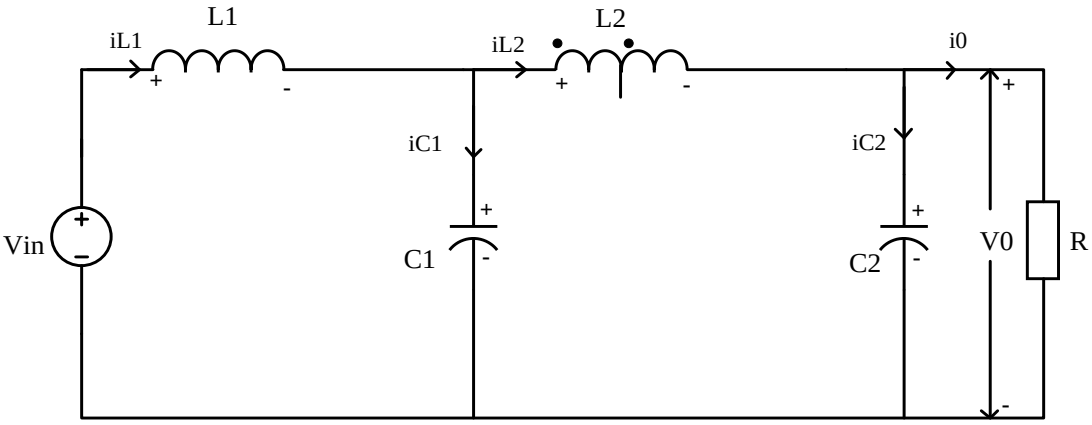


(c)

Fig. 6.2: (a) Semi-tapped quadratic boost converter and equivalent circuit (b) for switch-ON and (c) for switch-OFF.

Though the flux is not directly measurable, current measurement can confirm the analysis. The steady state expressions for semi-tapped quadratic boost converter will now be derived.

When the switch is ON, the equivalent circuit of the converter is as shown in Fig. 6.2(b). The state equations for switch-ON duration can be written as

$$L_1 \dot{i}_{L1} = V_{in} \qquad N_{21} \dot{\varphi}_2 = v_{C1} \quad C_1 \dot{v}_{C1} = \varphi_2 \frac{N_{21}}{L_{21}} \quad C_2 \dot{v}_{C2} = \frac{v_{C2}}{R} \tag{6.1}$$

For the equivalent circuit of the converter during switch-OFF state as shown in Fig. 6.2(c), the state equations can be written as

$$L_1 \dot{i}_{L1} = V_{in} - v_{C1} \quad , \quad \left(N_{21}+N_{22}\right)\dot{\varphi}_2 = v_{C1} - v_{C2}$$
$$C_1 \dot{v}_{C1} = i_{L1} - \frac{\left(N_{21}+N_{22}\right)}{L_2}\varphi_2 \, , \; C_2 \dot{v}_{C2} = \frac{\left(N_{21}+N_{22}\right)}{L_2}\varphi_2 - \frac{v_{C2}}{R} \tag{6.2}$$

The steady state expressions for flux through the core of tapped-inductor L_2, inductor current I_{L1} and capacitor voltages V_{C1}, V_{C2} can be derived by using averaging method [31]. The steady state expressions for semi-tapped quadratic boost converter are given as

$$\Phi_2 = \frac{I_0 L_2}{\left(1-D\right)\left(N_{21}+N_{22}\right)}, \quad I_{L2ON} = \frac{N_{21}\Phi_2}{L_{21}}, \quad I_{L2OFF} = \frac{(N_{21}+N_{22})\Phi_2}{L_2} \tag{6.3}$$

$$I_{L1} = I_{in} = \frac{V_{in}\left(1+n_2 D\right)^2}{R\left(1-D\right)^4} = \frac{V_0\left(1+n_2 D\right)}{R\left(1-D\right)^2} \tag{6.4}$$

$$V_{C1} = \frac{V_{in}}{\left(1-D\right)} \quad , \qquad V_0 = V_{C2} = \frac{V_{in}\left(1+n_2 D\right)}{\left(1-D\right)^2} \tag{6.5}$$

where n_2, turns ratio of tapped-inductor can be defined as $n_2=N_{22}/N_{21}$ and D is a duty ratio. It can be observed that output voltage is also a function of turns ratio n_2, which can substantially step up the output voltage. Also, one advantage of this converter is the continuous input current since the input inductor is not tapped.

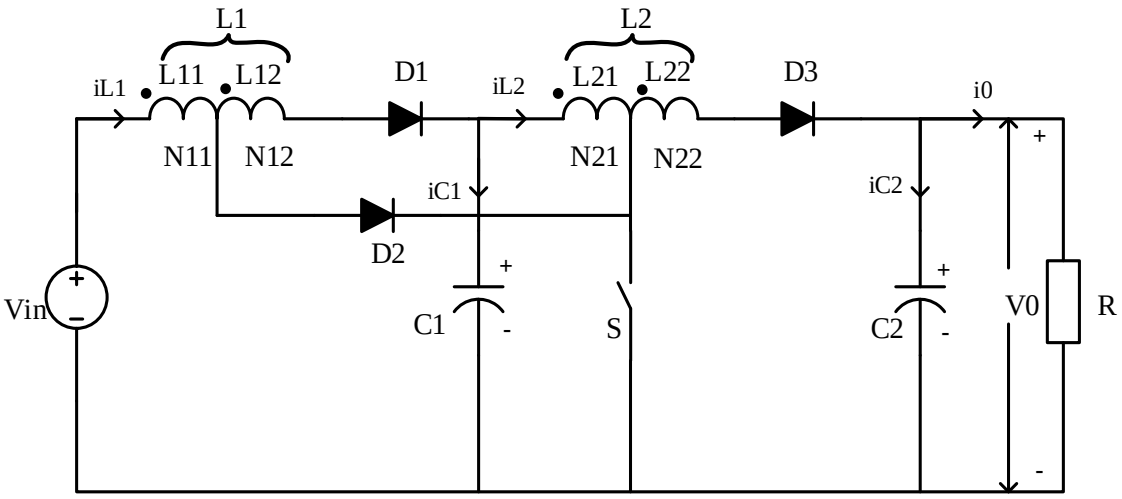
6.2.2 Fully-tapped quadratic boost converter

Figure 6.3(a) shows fully-tapped quadratic boost converter with both the inductor tapped. Inductor L_1 is divided into two parts L_{11} and L_{22} having number of turns N_{11} and N_{12} respectively. Similarly inductor L_2 is also in two parts L_{21} and L_{22}, and having number of turns $N_{21}$and N_{22} respectively. When the switch S is ON, diodes D_1 and D_3 gets reverse biased and diode D_2 conducts. During switch-ON period voltage across inductor L_{11} is equals to input voltage V_{in} and voltage across inductor L_{21} is equals to capacitor voltage V_{C1}. Due to coupling effect voltage induced across inductors L_{12} and L_{22}. When switch S is OFF, diode D_1 and D_3 conducts and diode D_2 gets reverse

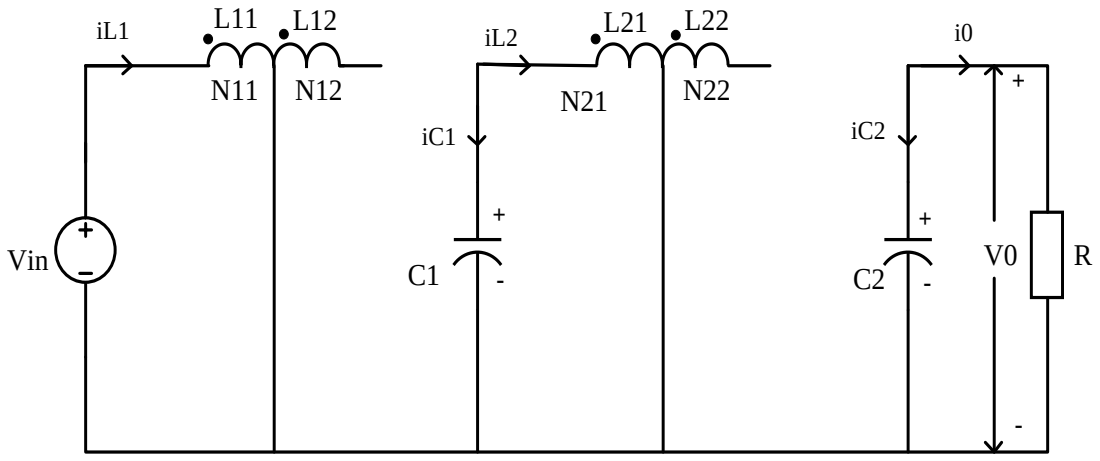
bias. In this duration, inductor stored energy supplied to load and capacitors. The steady state expressions for converter are derived as given below.

The equivalent circuit for switch-ON period of fully-tapped quadratic boost converter is as shown in Fig. 6.3(b), and the state equation for this duration can be written as

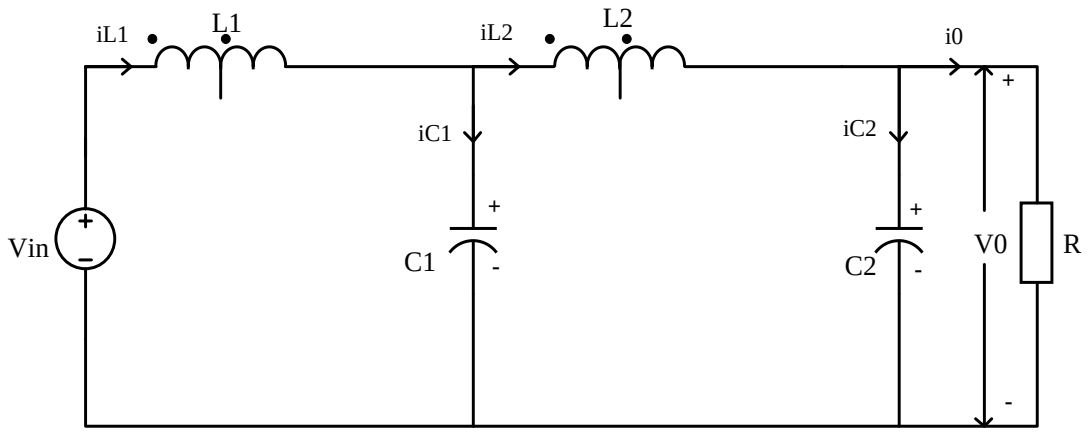
$$N_{11}\dot{\varphi} = V_{in} \qquad N_{21}\dot{\varphi}_2 = v_{C1} \qquad C_1\dot{v}_{C1} = -\varphi_2\frac{N_{21}}{L_{21}} \qquad C_2\dot{v}_{C2} = -\frac{v_{C2}}{R} \tag{6.6}$$



(a)



(b)



(c)

Fig. 6.3: (a) Fully-tapped quadratic boost converter and equivalent circuits for (b) switch-ON, and (c) switch-OFF.

For switch-OFF period equivalent circuit of the converter shown in Fig. 6.3(c), the state equations are as

$$\left(N_{11}+N_{12}\right)\dot{\varphi}_1 = V_{in} - v_{C1} \qquad \left(N_{21}+N_{22}\right)\dot{\varphi}_2 = v_{C1} - v_{C2}$$

$$C_1\dot{v}_{C1} = \frac{\varphi_1\left(N_{11}+N_{12}\right)}{L_1} - \frac{\varphi_2\left(N_{21}+N_{22}\right)}{L_2} \qquad C_2\dot{v}_{C2} = \frac{\varphi_2\left(N_{21}+N_{22}\right)}{L_2} - \frac{v_{C2}}{R} \quad (6.7)$$

By using (6.6) and (6.7), the steady state expressions [31] for flux through the core of tapped-inductors L_1, L_2 and capacitor voltages V_{C1}, V_{C2} can be found as

$$\Phi_1 = \frac{DI_0L_1}{DN_{11}\left(1+n_1\right)^2 + \left(1-D\right)\left(N_{11}+N_{12}\right)} \qquad I_{L1ON} = \frac{\Phi_1 N_{11}}{L_{11}} \qquad I_{L2OFF} = \frac{\Phi_1 N_1}{L_1} \quad (6.8)$$

$$\Phi_2 = \frac{DI_0L_2}{\left(1-D\right)\left(N_{21}+N_{22}\right)} \qquad I_{L2ON} = \frac{\Phi_2 N_{21}}{L_{21}} \qquad I_{L2OFF} = \frac{\Phi_2 N_2}{L_2} \quad (6.9)$$

$$V_{C1} = \frac{V_{in}\left(1+n_1D\right)}{\left(1-D\right)} \qquad V_0 = V_{C2} = V_{in}\left\{\frac{\left(1+n_1D\right)\left(1+n_2D\right)}{\left(1-D\right)^2}\right\} \quad (6.10)$$

Where $n_1=N_{12}/N_{11}$ and $n_2=N_{22}/N_{21}$ are turns ratio of tapped-inductors L_1 and L_2 respectively. This converter provides more flexibility in obtaining a high gain with the

help of turns ratio. Unlike semi-tapped quadratic boost converter, the input current is of pulsating nature since input inductor is also tapped. However pulsating input current can be reduced by keeping low turns ratio for the input tapped inductor.

6.3 Voltage gain and efficiency of converters

In order to evaluate the performance parameters like voltage gain and efficiency, one has to consider the non-idealities of various components. Effects of non-idealities on voltage gain and efficiency is studied in this section. The performance is evaluated for untapped, semi-tapped and fully- tapped quadratic boost converter. Inductors and capacitors are modeled with series resistance and the power MOSFET during ON-state is modeled as ideal switch with series resistance. Also diodes in conduction state can be modeled as forward voltage source in series with resistance. The circuit parameters of all three converters used for performance evaluation are listed in table 1. The circuit parameters such as inductors are selected for operating converter in continuous conduction mode for given input of 15V; operating frequency 20 KHz and maximum value of load resistance is 250Ω. The capacitors are selected to maintain voltage ripple less than 1%.

Table 6.2: Parameters of converters.

S.No.	Parameters	Value
1.	Input voltage	15V
2.	Inductor L_1, L_2	1.1mH,2.6mH
3	Inductor L_{11}, L_{12}, L_{21}, L_{22}(n_1=n_2=1)	L_{11}=278.9µH,L_{12}=284.3µH, L_{21}=666.8µH,L_{22}= 673.8µH
4	Inductor L_{11}, L_{12}, L_{21}, L_{22}(n_1=n_2=1.5)	L_{11}=180µH,L_{12}=408.6µH, L_{21}=426µH,L_{22}= 702µH
5.	Capacitor C_1,C_2	88.6µF, 180µF
6.	r_{L1}, r_{L2}	0.114Ω, 0.196Ω
7.	r_{L11}, r_{L12}, r_{L21}, r_{L22} (n_1=n_2=1)	r_{L11}= r_{L12} = 0.057Ω, r_{L21} = r_{L22} = 0.098Ω
8.	r_{L11}, r_{L12}, r_{L21}, r_{L22} (n_1=n_2=1.5)	r_{L11}=0.456 Ω, r_{L12} = 0.0684 Ω, r_{L21} =0.0784 Ω, r_{L22} = 0.1176Ω
9.	r_{C1}, r_{C2}	0.152 Ω,0.076 Ω
10.	V_{FD1},V_{FD2},V_{FD3}(maximum)	1.05V each

11.	Load resistance R	50 Ω,100 Ω,250 Ω
12.	Switch resistance rDS (maximum)	0.18Ω
13.	Measured value of coupling coefficient 'k'	0.9875

6.3.1 Voltage gain and efficiency of quadratic boost converter

Figure 6.4 shows the quadratic boost converter with parasitic elements. Averaged model of quadratic boost converter can be represented by equations (6.11)-(6.14), where inductor currents (i_{L1}, i_{L2}) and capacitor voltages (v_{C1}, v_{C2}) are the states of the converter.

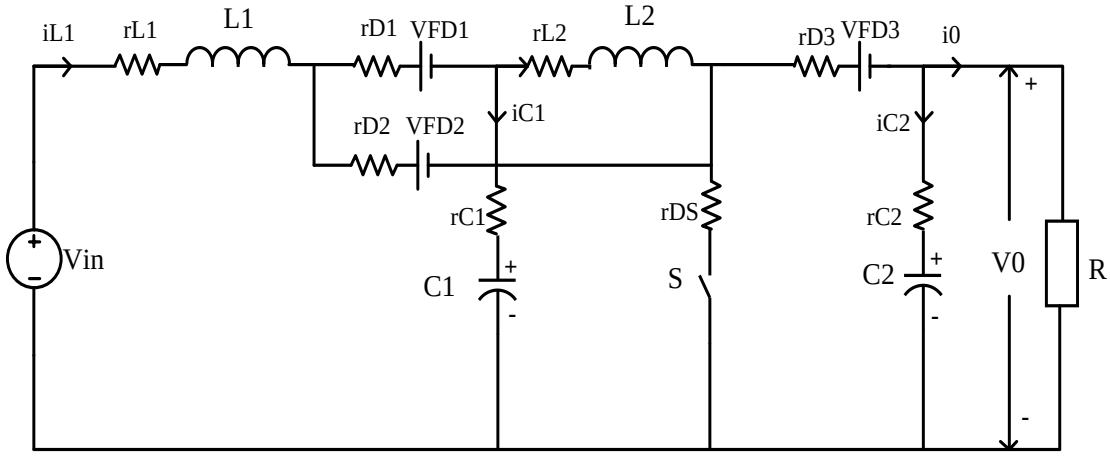


Fig. 6.4: Quadratic boost converter with parasitic parameters.

As shown in Fig. 6.4, r_{L1} and r_{L2} are the equivalent series resistance (ESR) of inductors; r_{C1} and r_{C2} are the ESR of capacitors; r_{D1},r_{D2} and r_{D3} are the on-state ESR of diodes;V_{FD1},V_{FD2} and V_{FD3} are on-state forward drop voltages of diodes D_1,D_2 and D_3 respectively; r_{DS} is the on-state resistance of MOSFET switch S; R is the load resistance; L_1,L_2 and C_1,C_2 are inductors and capacitors respectively; V_{in} is input voltage; d is averaged duty ratio.

$$\dot{i}_{L1}(t)=\frac{1}{L_1}\left\{V_{in}-d\left(V_{FD2}+i_{L1}\left(r_{L1}+r_{D2}+r_S\right)\right)-(1-d)\begin{pmatrix}V_{FD1}+i_{L1}\left(r_{L1}+r_{D1}\right)\\+r_{C1}\left(i_{L1}-i_{L2}\right)+v_{C1}\end{pmatrix}\right\} \quad (6.11)$$

$$\dot{i_{L2}}(t)=\frac{1}{L_2}\left\{v_{C1}-d\left(i_{L2}\left(r_{L2}+r_{C1}+r_S\right)\right)+(1-d)\left(\begin{array}{l}-V_{FD3}-i_{L2}\left(r_{L2}+r_{D3}\right)\\+r_{C1}\left(i_{L1}-i_{L2}\right)\\-v_{C2}\dfrac{R}{\left(R+r_{C2}\right)}\end{array}\right)\right\} \tag{6.12}$$

$$\dot{v_{C1}}(t)=\frac{1}{C_1}\left\{-d\left(i_{L2}\right)+(1-d)\left(i_{L1}-i_{L2}\right)\right\} \tag{6.13}$$

$$\dot{v_{C2}}(t)=\frac{1}{C_2}\left\{-\frac{v_{C2}}{R+r_{C2}}+\left(1-d\right)\left(i_{L2}\right)\right\} \tag{6.14}$$

In steady state, LHS of equations (6.11)-(6.14) will become zero. From these equations, non-ideal voltage gain can be derived as

$$\frac{V_0}{V_{in}}=\left\{\begin{array}{l}\dfrac{\left(1-D'V_{FD1}/V_{in}-DV_{FD2}/V_{in}\right)\left(D'^2\right)+\left(-D'V_{FD3}/V_{in}\right)\left(D'^3\right)}{\left(r_{L1}+D\left(r_{D2}+r_S\right)+D'\left(r_{D1}+r_{C1}\right)+D'^2\left(r_{C1}+r_{L2}+Dr_S+D'r_{D3}\right)\right.}\\\left.+RD'^4-2D'^2r_{C1}\right)/\left(R+r_{C2}\right)\end{array}\right\} \tag{6.15}$$

Where D′ is used for (1-D) and D is steady state duty ratio. Variation in voltage gain with variation in duty ratio at different load resistance for quadratic boost converter based on equation (6.15) is plotted in Fig. 6.5. The circuit parameters of quadratic boost converter used for performance evaluation are given in table 6.1.

Also from equations (6.11)-(6.14), the inductor L_1current can be determined as

$$I_{L1} = I_{in} = \left\{ \frac{-\left(-V_{in} + D'V_{FD1} + DV_{FD2}\right) - \left(D'^{2} V_{FD3}\right)}{r_{L1} + D\left(r_{D2} + r_S\right) + D'\left(r_{D1} + r_{C1}\right) + D'^{2}\left(r_{C1} + r_{L2} + Dr_S + D'r_{D3}\right) + RD'^{4} - 2D'^{2} r_{C1}} \right\} \tag{6.16}$$

The efficiency of the converter can be defined as

$$\eta = \frac{V_0^{\,2} / R}{V_{in} I_{in}} \tag{6.17}$$

The efficiency can be derived using equation (6.15), (6.16) and equation (6.17), and variation in efficiency with duty ratio for different load resistances are plotted in Fig. 6.6.

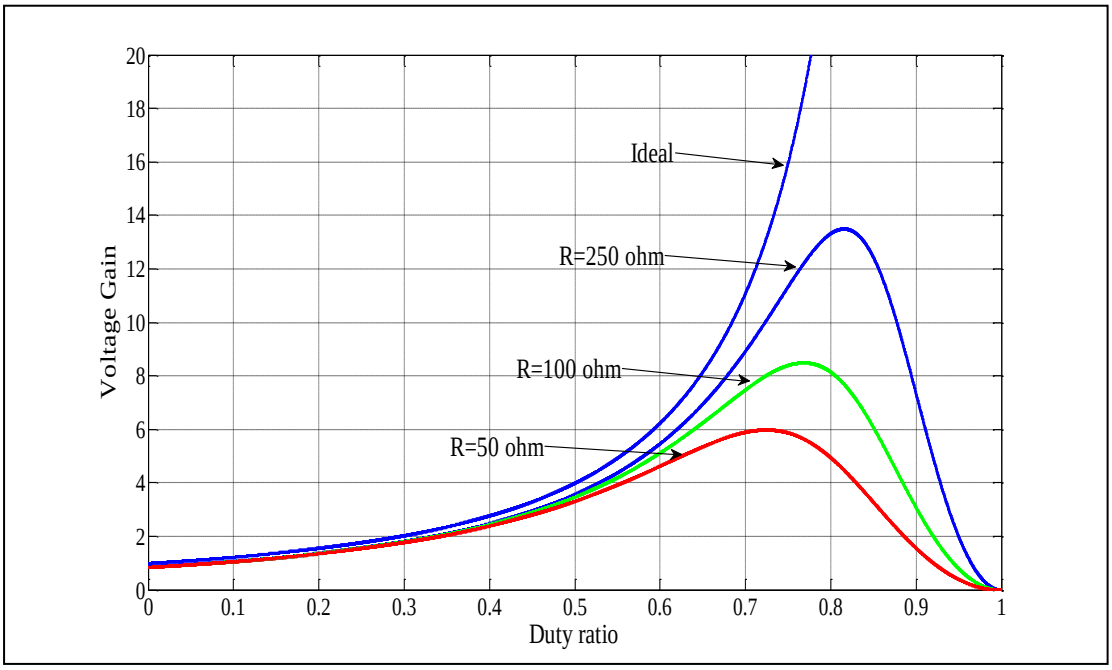


Fig. 6.5: Voltage gain of quadratic boost converter with various loads.

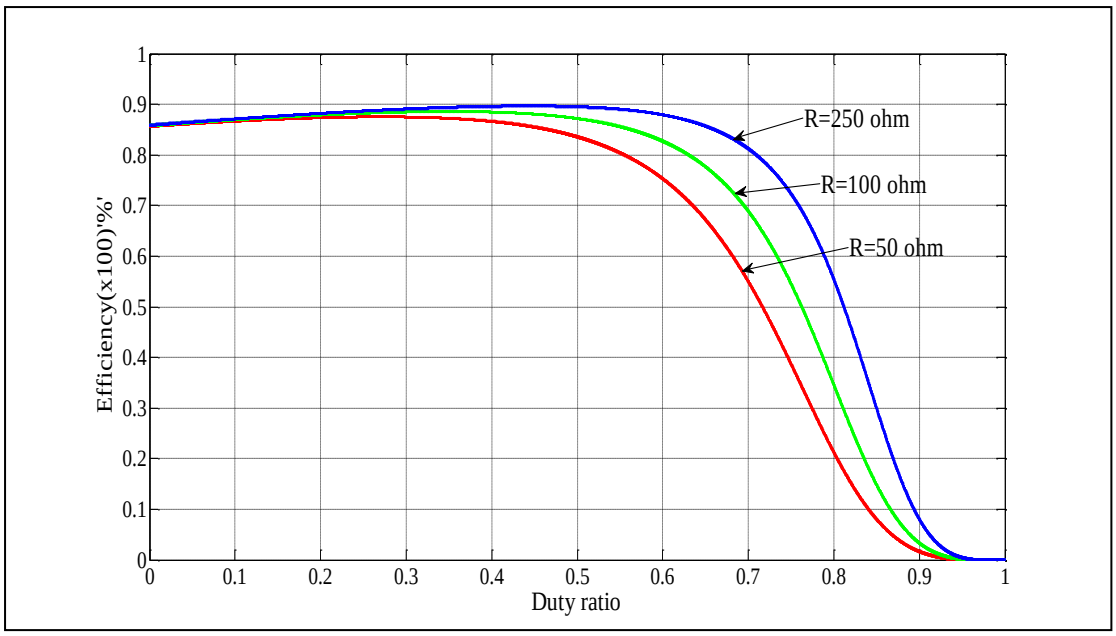


Fig. 6.6: Efficiency of quadratic boost converter with various loads.

6.3.2 Voltage gain and efficiency for semi-tapped quadratic boost converter

Figure 6.7 is the semi-tapped quadratic boost converter with non-idealities. In this figure, r_{L21} and r_{L22} are the Equivalent Series Resistance (ESR) of tapped inductor L_{21} and L_{22}. The state space averaged model of this converter is given by equations (6.18) to (6.21).

$$\dot{i}_{L1}(t)=\frac{1}{L_1}\left\{\begin{array}{l} V_{in}-d\left(V_{FD2}+i_{L1}\left(r_{L1}+r_{D2}+r_S\right)\right)- \\ (1-d)\left(V_{FD1}+i_{L1}\left(r_{L1}+r_{D1}\right)+r_{C1}\left(i_{L1}-\varphi_2\left(\frac{N_{21}+N_{22}}{L_2}\right)\right)+v_{C1}\right)\end{array}\right\} \tag{6.18}$$

$$\dot{\phi}_2(t)=\frac{d}{N_{21}}\left(v_{C1}-\left(\frac{\varphi_2 N_{21}}{L_{21}}\left(r_{L2}+r_{C1}+r_S\right)\right)\right)+\frac{(1-d)}{N_{21}+N_{22}}$$
$$\left(\begin{array}{l} v_{C1}-V_{FD3}-\frac{\varphi_2\left(N_{21}+N_{22}\right)}{L_2}\left(r_{L2}+r_{D3}\right)+r_{C1}\left(i_{L1}-\frac{\varphi_2\left(N_{21}+N_{22}\right)}{L_2}\right) \\ -v_{C2}R/\left(R+r_{C2}\right)\end{array}\right) \tag{6.19}$$

$$\dot{v_{C1}}(t) = \frac{1}{C_1}\left\{-d\,\frac{N_{21}\varphi_2}{L_{21}} + (1-d)\left(i_{L1} - \frac{\varphi_2\left(N_{21}+N_{22}\right)}{L_2}\right)\right\} \tag{6.20}$$

$$\dot{v_{C2}}(t) = \frac{1}{C_2}\left\{-\frac{v_{C2}}{R+r_{C2}} + (1-d)\,\frac{\varphi_2\left(N_{21}+N_{22}\right)}{L_2}\right\} \tag{6.21}$$

Considering the same state variables, the current through tapped inductor during switch-ON and switch-OFF duration is given by (6.3). In steady state, by taking LHS terms as zero for equations (6.18) to (6.21), the voltage gain of the semi-tapped quadratic boost converter can be derived as

$$\frac{V_0}{V_{in}} = \left\{\begin{array}{l}\left(1 - D'V_{FD1}/V_{in} - DV_{FD2}/V_{in}\right)\left(\dfrac{D'^2}{L_2}\left(\dfrac{D\left(N_{21}+N_{22}\right)}{N_{21}} + D'\right)\right) + \\ \left(-D'V_{FD3}/\left(V_{in}\left(N_{21}+N_{22}\right)\right)\right)\left(D'^3\,\dfrac{\left(N_{21}+N_{22}\right)}{L_2}\right)\end{array}\right\} / X \tag{6.22}$$

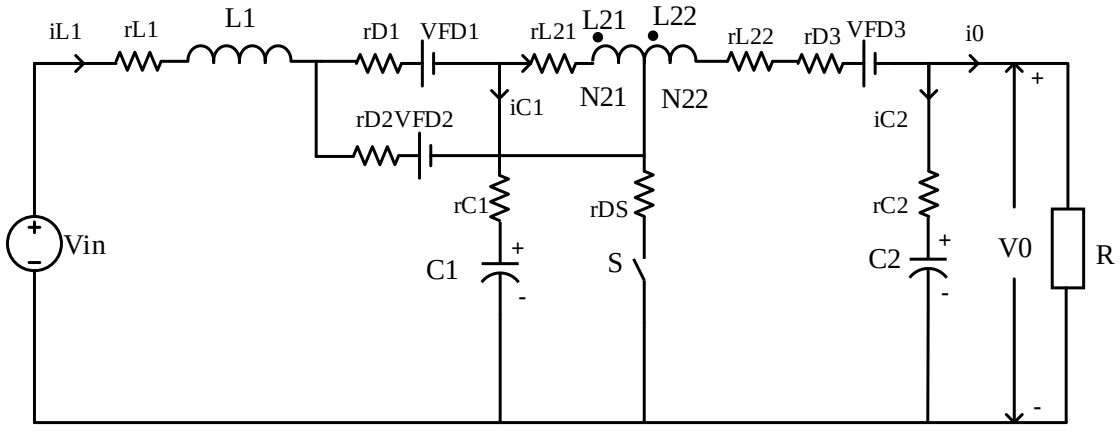


Fig. 6.7: Semi-tapped quadratic boost converter with parasitic parameters.

The current through inductor L_1 is the input current and is derived as

$$I_{L1}=I_{in}=\left\{\begin{array}{l}\left(V_{in}-D'V_{FD1}-DV_{FD2}\right)\left\{\begin{array}{l}\left(\dfrac{1}{R+r_{C2}}\right)\left(\dfrac{N_{21}D}{L_{21}}+\dfrac{\left(N_{21}+N_{22}\right)D'}{L_2}\right)\\ \left(\dfrac{D}{N_{21}}+\dfrac{D'}{\left(N_{21}+N_{22}\right)}\right)\end{array}\right\}\\ +\left(-D'V_{FD3}/\left(\left(N_{21}+N_{22}\right)\right)\right)\left\{\left(\dfrac{1}{R+r_{C2}}\right)\left(\dfrac{N_{21}D}{L_{21}}+\dfrac{\left(N_{21}+N_{22}\right)D'}{L_2}\right)\right\}\end{array}\right\}/X \qquad (6.23)$$

Where, X is

$$X=D'^2\left[\frac{-RD'^2}{\left(R+r_{C2}\right)L_2}-\frac{1}{\left(R+r_{C2}\right)}\left\{\frac{(r_{L21}+r_{C1}+r_S)D}{N_{21}}+\frac{D'r_{C1}}{L_2}+\frac{D'\left(r_{L22}+r_{L21}+r_{D3}\right)}{L_2}\right\}\right]$$

$$-\frac{1}{\left(R+r_{C2}\right)}\left[\begin{array}{l}\left\{\left(\dfrac{-N_{21}D}{L_1}-\dfrac{\left(N_{21}+N_{22}\right)D'}{L_2}\right)\left(\dfrac{D}{N_{21}}+\dfrac{D'}{N_{21}+N_{22}}\right)\left(-r_{L1}-D\left(r_{D2}+r_S\right)-D'\left(r_{D1}+r_{C1}\right)\right)\right\}\\ +\left\{\left(\dfrac{D'^2r_{C1}}{N_{21}+N_{22}}\right)\left(-\dfrac{N_{21}D}{L_1}-\dfrac{\left(N_{21}+N_{22}\right)D'}{L_2}\right)\right\}-\left\{\begin{array}{l}\left(\dfrac{D'^2r_{C1}\left(N_{21}+N_{22}\right)}{L_2}\right)\\ \left(\dfrac{D}{N_{21}}+\dfrac{D'}{\left(N_{21}+N_{22}\right)}\right)\end{array}\right\}\end{array}\right]$$

Fig. 6.8 shows the variation of voltage gain with variation in duty ratio for different load resistances using (6.22).

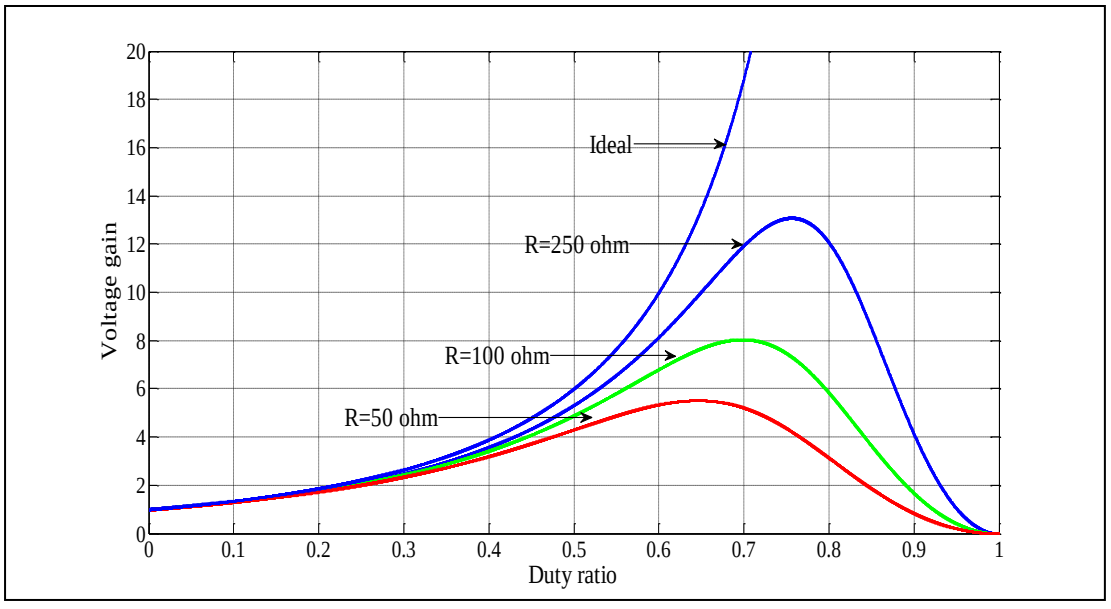


Fig. 6.8: Voltage gain of semi-tapped converter (n_2=1).

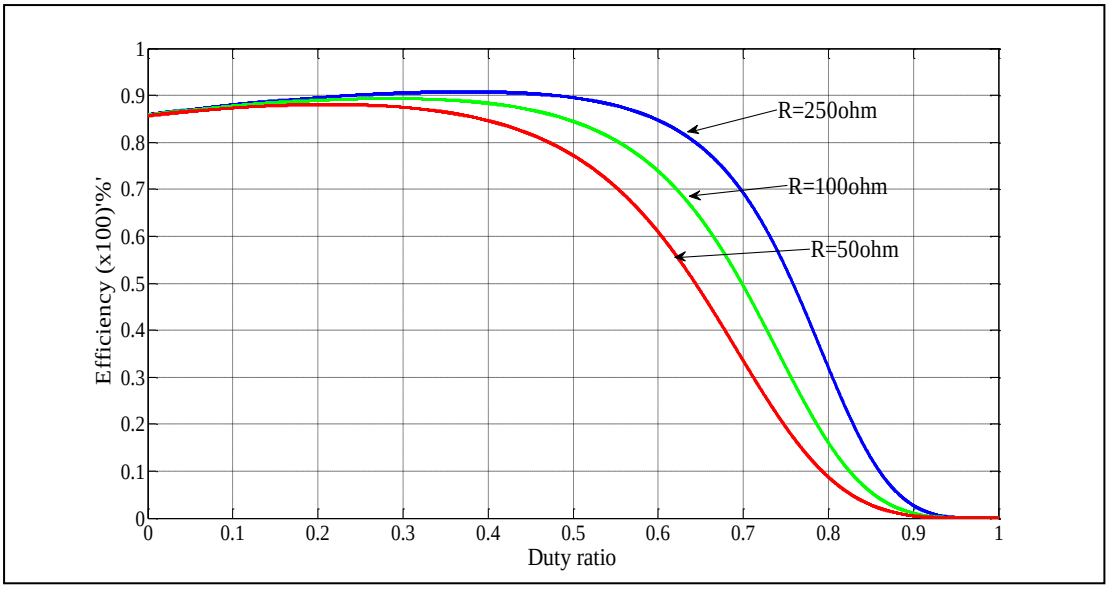


Fig. 6.9: Efficiency of semi-tapped converter (n_2=1).

The efficiency plot as shown in Fig. 6.9 can be derived using (6.22) and (6.23) for different loads. It can be observed that higher the value of load resistance, one can get higher voltage gains and efficiency for lower duty ratios. This can be explained on the fact that as load resistance decreases, current increases which increases the drop in parasitic resistances. The values taken for this analysis are given in table 6.1. The tapped inductor used for the semi-tapped converters is tightly coupled and the measured value of coupling coefficient 'k' is 0.9875 but for calculation it is assumed as k =1.

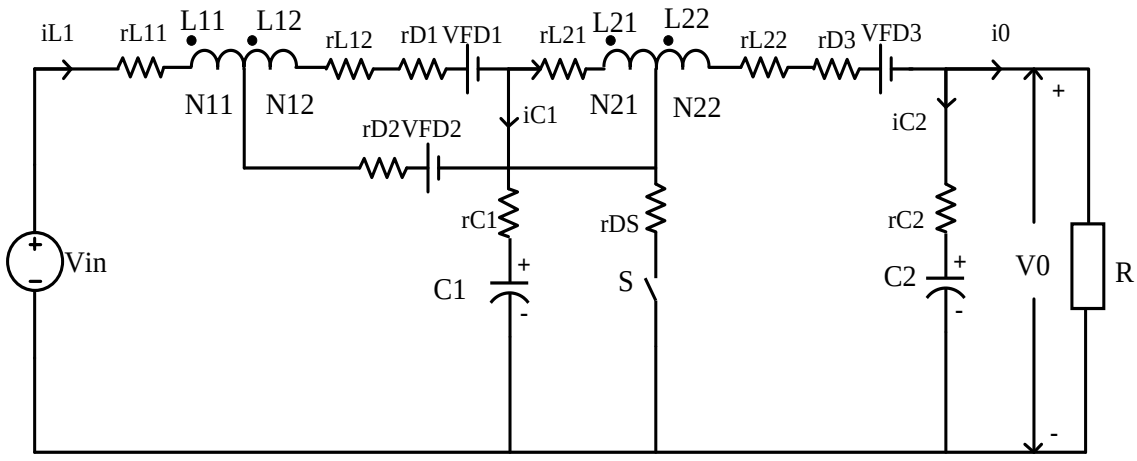


Fig. 6.10: Fully Tapped-inductor quadratic boost converter with parasitic parameters.

6.3.3 Voltage gain and efficiency of fully- tapped quadratic boost converter

Figure 6.10 shows the equivalent circuit of fully-tapped quadratic boost converter with non-idealities. The averaged model of fully-tapped inductor quadratic boost converter is given by equations (6.24) to (6.27).

$$\dot{\phi_1}(t) = \frac{d}{N_{11}}\left\{V_{in} - V_{FD2} - \left(\frac{\varphi_1 N_{11}}{L_{11}}\left(r_{L11} + r_{D2} + r_S\right)\right)\right\} + \frac{(1-d)}{N_{11}+N_{12}} \left\{\left(\begin{array}{l} V_{in} - v_{C1} - V_{FD1} - \frac{\varphi_1\left(N_{11}+N_{12}\right)}{L_1}\left(r_{L11} + r_{L12} + r_{D1}\right) - \\ r_{C1}\left(\frac{\varphi_1\left(N_{11}+N_{12}\right)}{L_1} - \frac{\varphi_2\left(N_{21}+N_{22}\right)}{L_2}\right) \end{array}\right)\right\} \quad (6.24)$$

$$\dot{\phi_2}(t) = \frac{d}{N_{21}}\left\{v_{C1} - \left(\frac{\varphi_2 N_{21}}{L_{21}}\left(r_{L21} + r_{C1} + r_S\right)\right)\right\} + \frac{(1-d)}{N_{21}+N_{22}} \left\{\left(\begin{array}{l} v_{C1} - V_{FD3} - \frac{v_{C2}R}{\left(R+r_{C2}\right)} - \frac{\varphi_2\left(N_{21}+N_{22}\right)}{L_2}\left(r_{L21} + r_{L22} + r_{D3}\right) + \\ r_{C1}\left(\frac{\varphi_1\left(N_{11}+N_{12}\right)}{L_1} - \frac{\varphi_2\left(N_{21}+N_{22}\right)}{L_2}\right) \end{array}\right)\right\} \quad (6.25)$$

$$\dot{v_{C1}}(t) = \frac{1}{C_1}\left\{-d\,\frac{N_{21}\varphi_2}{L_{21}} + (1-d)\left(\frac{\varphi_1\left(N_{11}+N_{12}\right)}{L_1} - \frac{\varphi_2\left(N_{21}+N_{22}\right)}{L_2}\right)\right\} \quad (6.26)$$

$$\dot{v_{C2}}(t) = \frac{1}{C_2}\left\{-\frac{v_{C2}}{R+r_{C2}} + (1-d)\frac{\varphi_2\left(N_{21}+N_{22}\right)}{L_2}\right\} \quad (6.27)$$

The steady state voltage gain of fully-tapped inductor quadratic boost converter can be derived by solving (6.24)-(6.27) and can be given as

$$\frac{V_0}{V_{in}}=\left\{\begin{array}{l}\left\{\left(\left(\frac{D}{N_{11}}+\frac{D'}{\left(N_{11}+N_{12}\right)}\right)-\frac{D'V_{FD1}}{V_{in}\left(N_{11}+N_{12}\right)}-\frac{DV_{FD2}}{V_{in}N_{11}}\right\}\left(-e\cdot h\cdot j\right)+\right.\\ \left.\left(-D'V_{FD3}/\left(V_{in}\left(N_{21}+N_{22}\right)\right)\right)\left(c\cdot h\cdot j\right)\end{array}\right\}/Y \qquad (6.28)$$

From (6.24)-(6.27), the steady state value of flux through the core of inductor L_1 is given as

$$\Phi_1=\left\{\begin{array}{l}\left\{\left(\left(\frac{V_{in}D}{N_{11}}+\frac{V_{in}D'}{\left(N_{11}+N_{12}\right)}\right)-\frac{D'V_{FD1}}{\left(N_{11}+N_{12}\right)}-\frac{DV_{FD2}}{N_{11}}\right\}\left(-e\cdot i\cdot m\right)+\right.\\ \left.\left(-D'V_{FD3}/\left(\left(N_{21}+N_{22}\right)\right)\right)\left(c\cdot i\cdot m\right)\end{array}\right\}/Y \qquad (6.29)$$

where details of Y and other coefficients are given in appendix-D.

The steady state value of Inductor L_1 current can be derived as

$$I_{L1}=I_{in}=\left\{\frac{DN_{11}}{L_{11}}+\frac{D'\left(N_{11}+N_{12}\right)}{L_1}\right\}\Phi_1 \qquad (6.30)$$

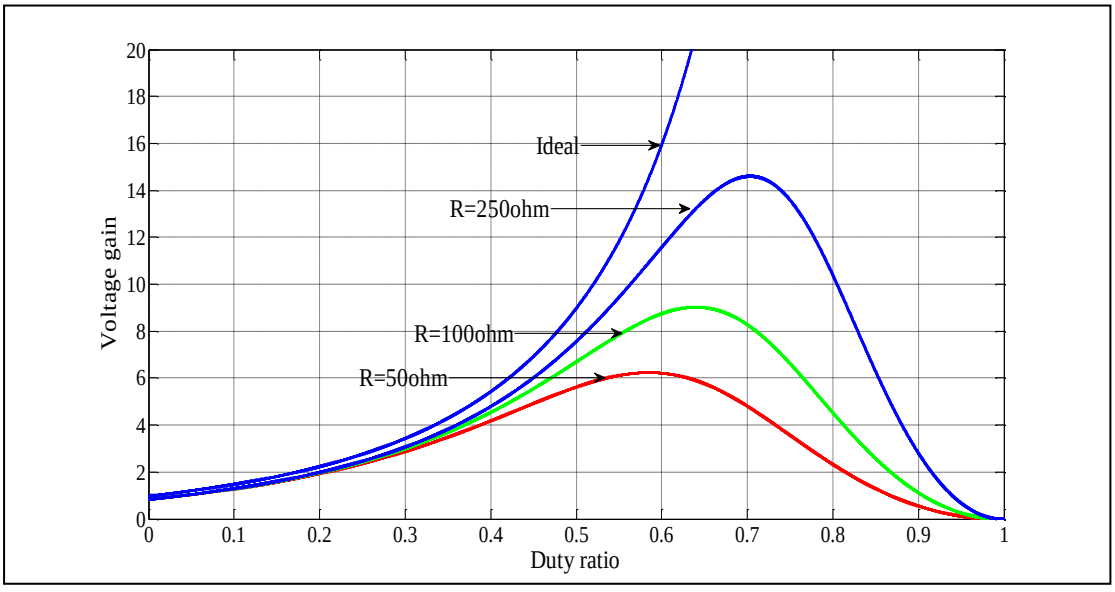


Fig. 6.11: Voltage gain of fully-tapped converter (n_1=n_2=1).

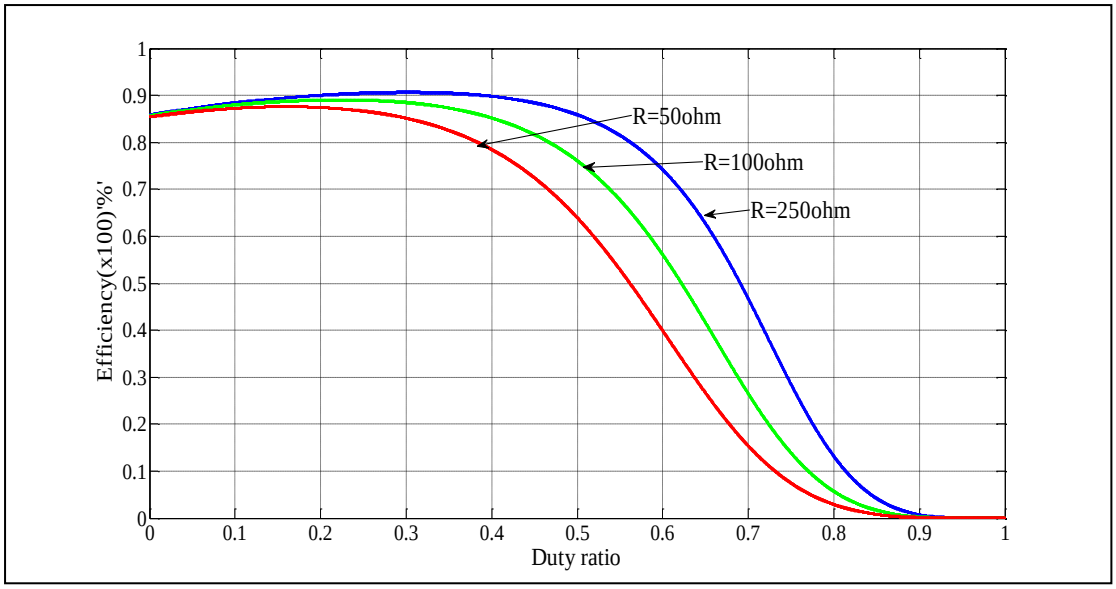


Fig. 6.12: Efficiency of fully-tapped converter (n_1=n_2=1).

Figure 6.11 shows the plot of variation in voltage gain with variation in duty ratio for different load resistance using (6.28). The plot of variation in efficiency with duty ratio is shown in Fig. 6.12 and it is derived by using (6.28), (6.29) and (6.30). It can be observed that significant voltage gain can be achieved even for lower load resistances.

6.4 Comparison between quadratic boost, semi-tapped quadratic boost and fully-tapped quadratic boost converter

6.4.1 Comparison of voltage gain and efficiency

The proposed converters are derived from quadratic boost converter which has same number of elements as proposed converter and similar quadratic conversion ratio. Hence, it would be apt to compare the proposed converters with the quadratic boost converter. The steady state performance equations for quadratic boost converter are given in [73]. Equations (6.15) and (6.17) are used to determine performance of quadratic boost converter. Similarly (6.22), (6.23) and (6.28) are used to evaluate the performance of the proposed converters. Figure 6.13 and Fig. 6.14, shows variation in efficiency and voltage gain against variation in duty ratio for converters. The load resistance and other parameters are same for comparison.

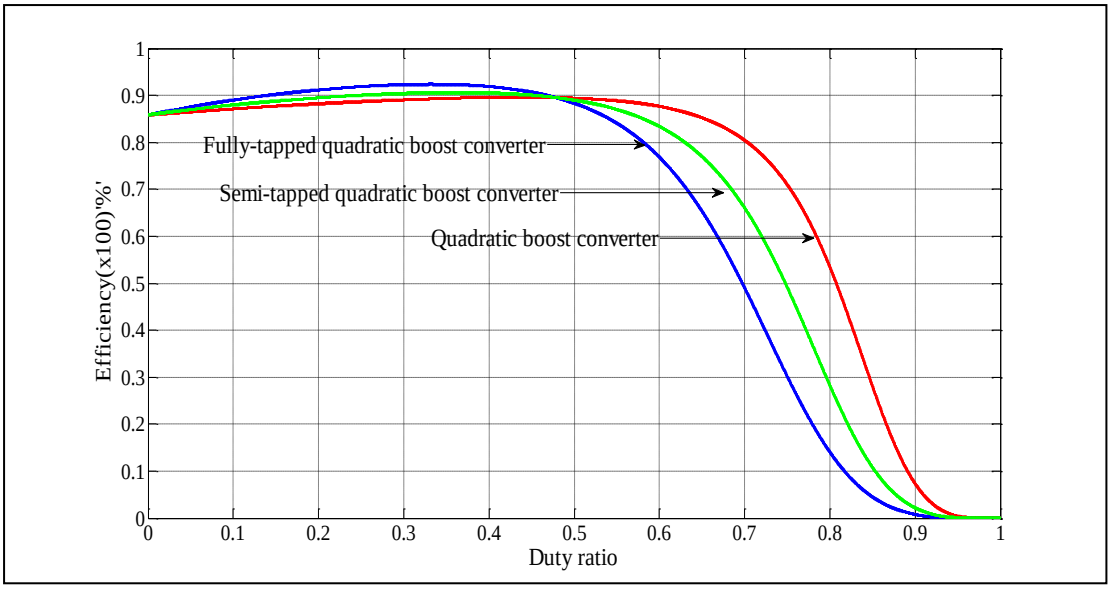


Fig. 6.13(a): Comparison of efficiency for $n_1=n_2=1$.

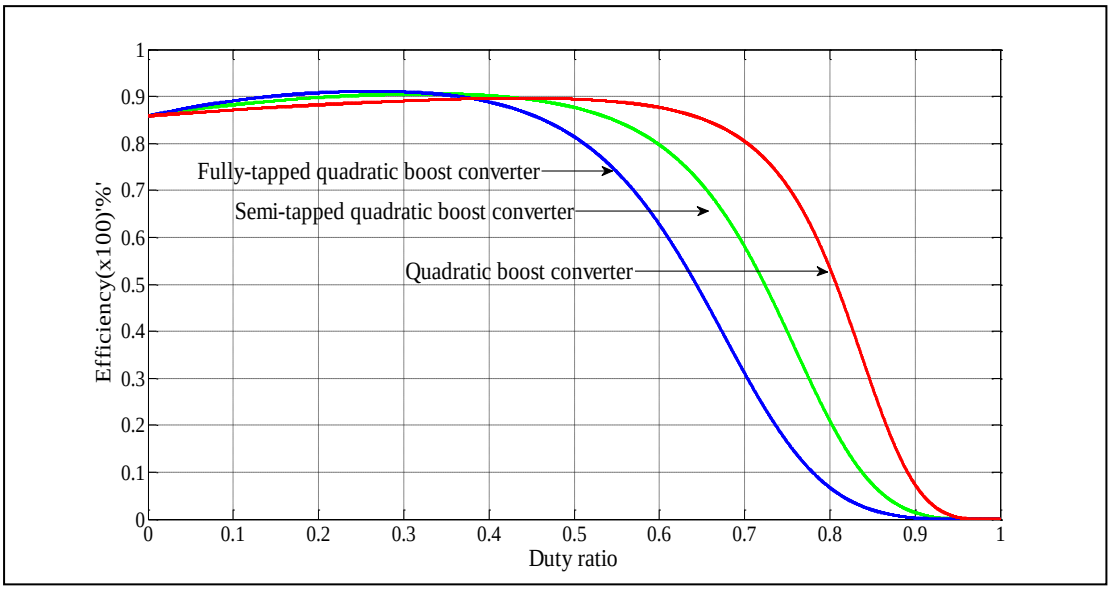


Fig. 6.13(b): Comparison of efficiency for $n_1=n_2=1.5$.

At higher duty ratios, gain reduces due to higher voltage drops. The voltage gain of fully-tapped inductor quadratic boost converter is highest and gain of semi-tapped inductor is higher than quadratic boost converter as shown in Fig. 6.14. It can be observed from Fig. 6.13 and Fig. 6.14 that for a given voltage gain, the efficiency of fully-tapped converter is higher than the other two converters.

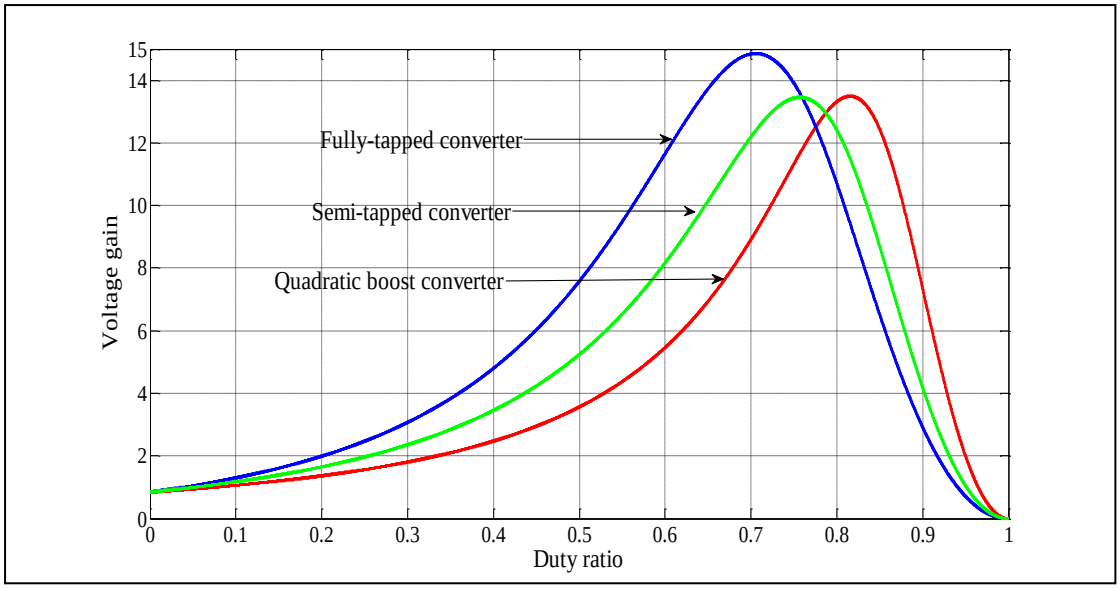


Fig. 6.14(a): Comparison of Voltage gain for $n_1=n_2=1$.

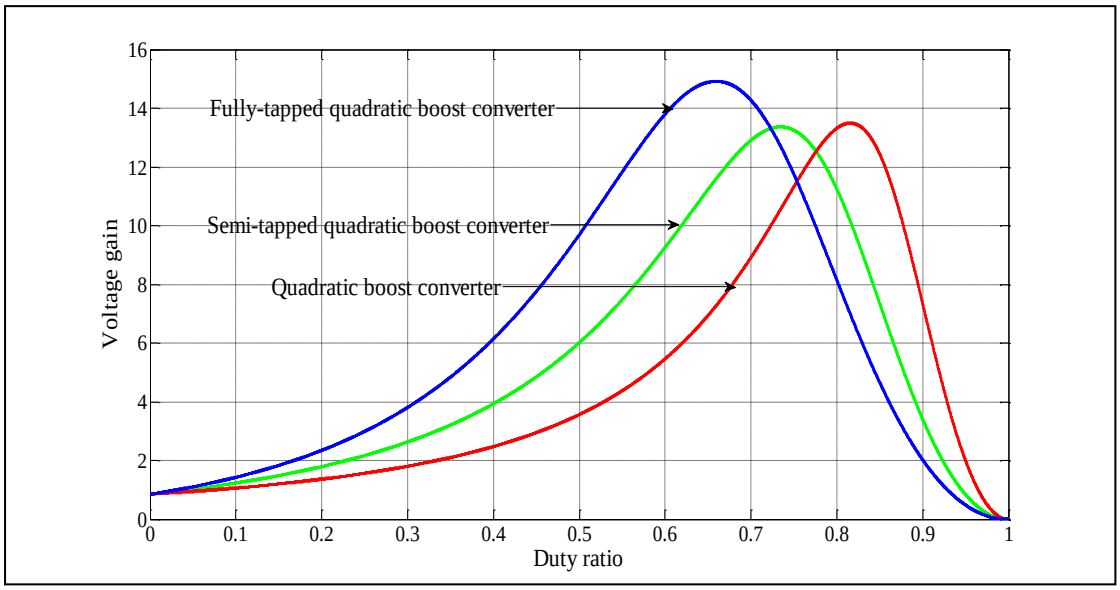


Fig. 6.14(b): Comparison of Voltage gain for $n_1=n_2=1.5$.

6.4.2. Comparison for voltage stress on active and passive switches

Comparison on the basis of voltage stress on the switch and diodes without parasitic components is given in table 6.2. From table 6.2 it can be concluded that stress over switch S is reduced in case of semi-tapped and fully-tapped quadratic boost converter for same output voltage in comparison to quadratic boost converter and it will reduce further as turn ratio increases for same output voltage. Similarly for diode D_2, voltage stress of semi-tapped quadratic boost converter is reduced as compared to quadratic boost converter and it is lowest in case of fully-tapped quadratic boost converter. For

diode D_1 voltage stress in fully-tapped quadratic boost converter is more in comparison to the rest of two converters. The voltage stress for diode D_3 is higher in case of semi-tapped and fully-tapped quadratic boost converter.

Table 6.3: Comparison of voltage stress for active and passive switches.

Component	Quadratic boost	Semi-tapped quadratic boost	Fully-tapped quadratic boost converter
Switch S	V_0	$V_0\left\{1-\frac{Dn_2}{(1+n_2D)}\right\}$	$V_0\left\{1-\frac{Dn_2}{(1+n_2D)}\right\}$
Diode D1	V_{C1}	V_{C1}	$\frac{V_{in}(1+2n_1D)}{(1-D)}$
Diode D2	V_0-V_{C1}	$V_0\left\{1-\frac{n_2D}{(1+n_2D)}\right\}-V_{C1}$	$V_0\left\{1-\frac{n_2D}{(1+n_2D)}\right\}-V_{C1}-\frac{V_{in}Dn_1}{(1-D)}$
Diode D3	V_0	$V_0\left\{1+\frac{Dn}{(1+nD)}\right\}$	$V_0\left\{1+\frac{n_2D}{(1+n_2D)}\right\}$

6.5 Simulation and experimental results

The performance of the proposed converters in terms of voltage stress, efficiency and voltage gain is tested by using the laboratory prototypes.

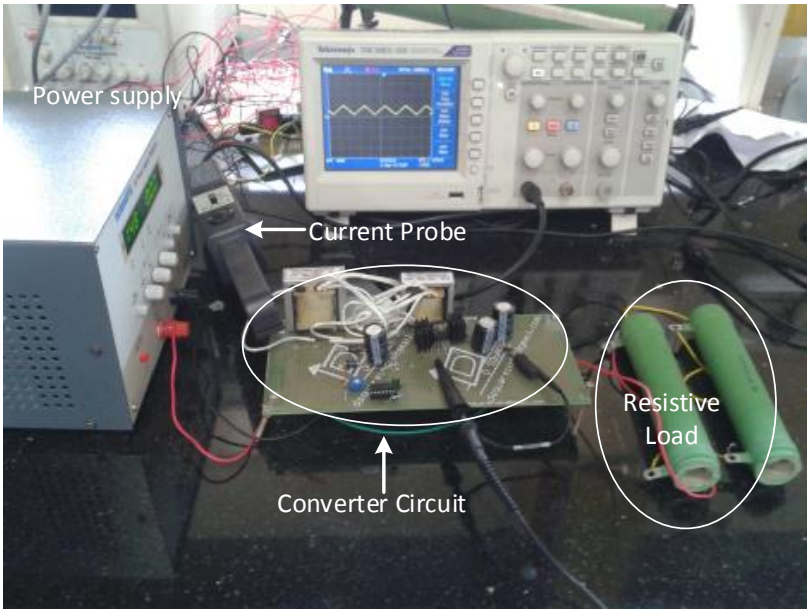
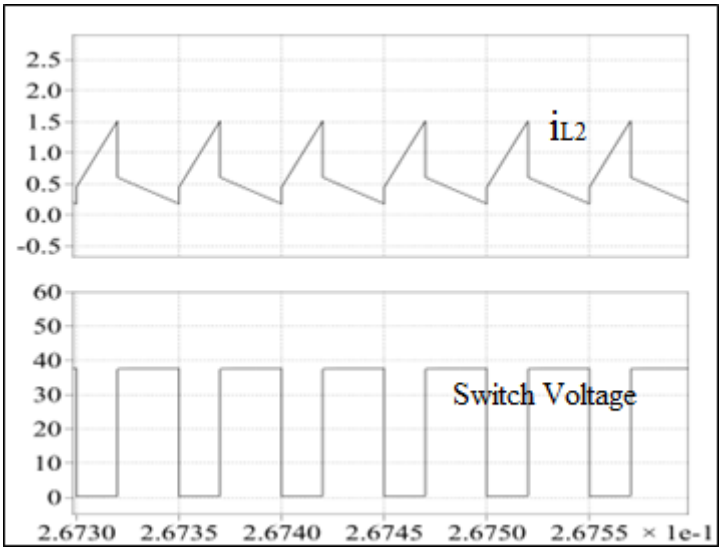
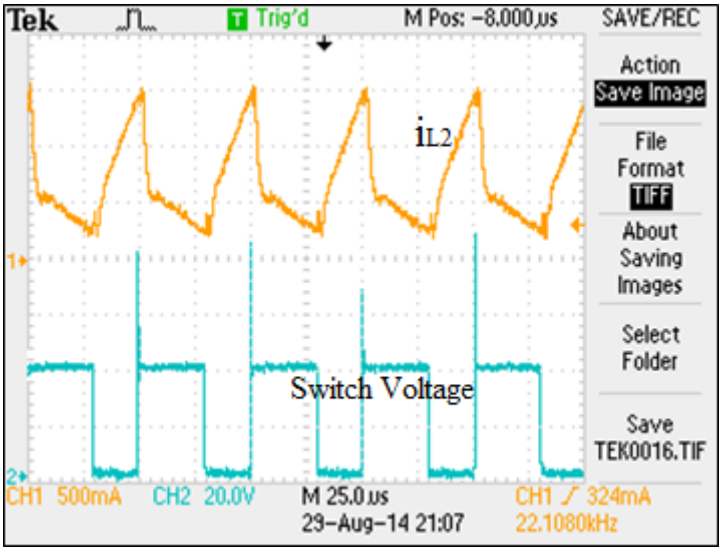


Fig. 6.15: Experimental set-up.

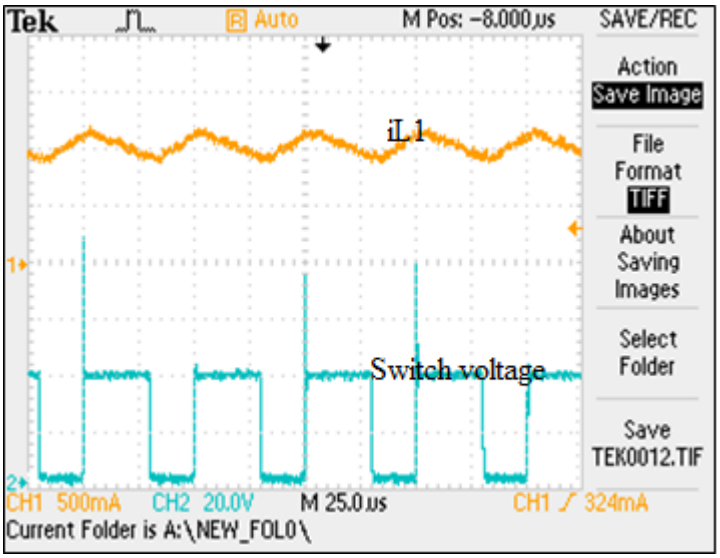
The experimental setup has the same specifications listed in table1 and TL494 is used to generate gate pulse in open loop configuration at switching frequency of 20 kHz. In a prototype circuit, MOSFET IRF640 is used as active switch and diode MUR460 is used as a passive switch. The inductor current is measured using Tektronix current probe A622. Figure 6.15 shows a picture of experimental setup. Also using the same parameters listed in table 6.1, the proposed converters are simulated in PLEXIM-PLECS simulation tool.



(a)



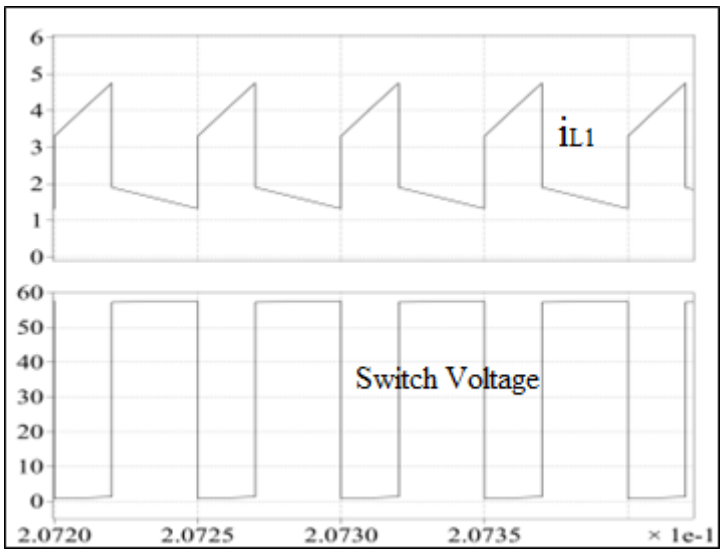
(b)



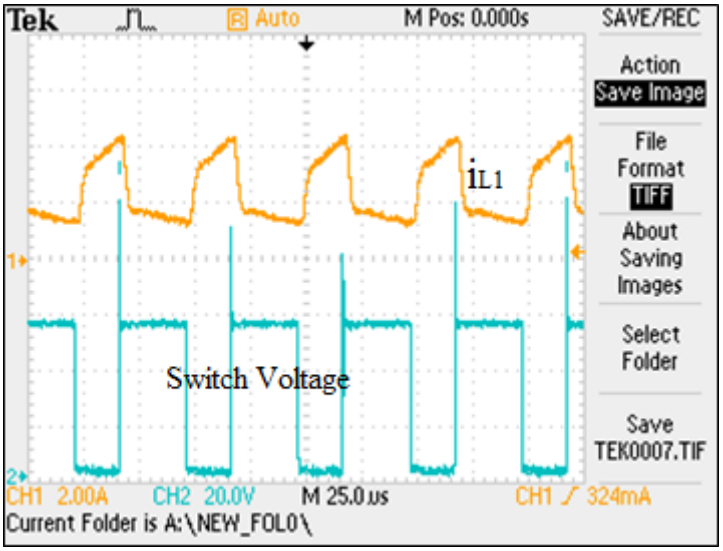
(c)

Fig. 6.16: Semi-tapped converter for D=0.4 and n_2=1.5 (a) simulation results for switch voltage and i_{L2}, (b) experimental results for switch voltage and i_{L2} , and (c) experimental results for switch voltage and $i_{L1.}$

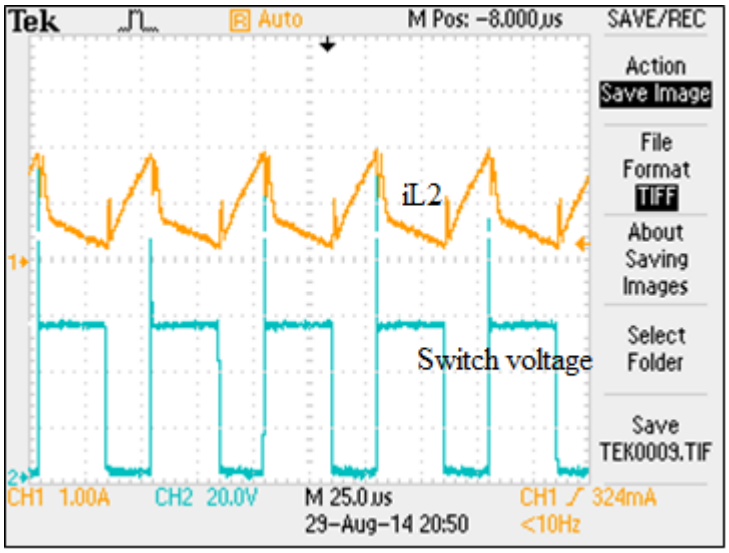
Figure 6.16 (a) shows a simulation result for semi-tapped converter for D=0.4 and R=248 Ω and turns ratio n_2=1.5. Simulation result shows switch voltage and current through tapped inductor L_2.



(a)



(b)



(c)

Fig. 6.17: Fully-tapped converter for D=0.4 and for $n_1=n_2=1.5$ (a) simulation results of switch voltage and i_{L1}, (b) experimental results of switch voltage and i_{L1}, and (c) experimental results of switch voltage and i_{L2}.

Figure 6.16(b) shows experimental results of semi-tapped quadratic boost converter's switch voltage and current through tapped inductor L_2 for the same duty ratio, Fig. 6.16(c) shows results of inductor current i_{L1} for same condition, in both results resistances and turns ratio are same as in simulation. One can observe the pulsating current in tapped inductor L_2 from the simulation as well as experimental results.

Similarly Fig. 6.17 shows simulation and experimental results for fully tapped inductor converter for D=0.4, R=248 and $n_1=n_2=1.5$. The waveform shows current of tapped inductor L_1 and switch voltage. Figure 6.17(c) shows waveform of i_{L2} for same condition of Fig. 6.17(b). It can be seen from Fig. 6.16 and 6.17 that simulation and experimental waveforms matches considerably. For example in Fig. 6.16, peak of the inductor current in both is almost equal (near 1.5 A) while switch voltage is also near 40 V in both. Further, one can observe spikes in switch voltages and inductor currents in experimental waveforms. These spikes are due to the leakage inductance (imperfect coupling) which is not considered in above performance analysis and simulation results.

Table 6.4: Measured values of voltage gain for quadratic boost converter.

Duty ratio %	Quadratic boost Measured gain
4	0.993
10	1.146
15	1.293
20	1.46
25	1.67
30	1.953
35	2.26
40	2.653
45	3.050
50	3.673
55	4.467
60	5.367
65	6.73
70	8.33

Table 6.5: Measured values for $n_1=n_2=1$.

Duty ratio %	Semi-tapped Measured gain	Fully-tapped Measured gain
4	1.033	1.093
10	1.253	1.4
15	1.473	1.673
20	1.74	2.053
25	2.053	2.533
30	2.406	3.173
35	2.966	3.906
40	3.58	4.78
45	4.346	5.846
50	5.273	7.06
55	6.193	8.07

Table 6.6: Measured values for $n_1=n_2=1.5$.

Duty ratio %	Semi-tapped Measured gain	Fully-tapped Measured gain
4	1.086	1.16
10	1.346	1.513
15	1.6	1.893
20	1.9	2.366
25	2.24	3.013
30	2.68	3.646
35	3.233	4.666
40	3.913	5.666
45	4.853	6.8
50	5.9	8.33

Figure 6.18(a) and Fig. 6.18(b), shows the measured voltage gain of quadratic boost, semi-tapped quadratic boost and fully-tapped quadratic boost converters, for tapped-inductor turn ratio is 1 and 1.5 respectively. Measured values of voltage gain for quadratic boost converter, semi-tapped and fully-tapped converters are also listed in

table 6.3, table 6.4 and table 6.5. The inductor details are same as mentioned in above performance analysis. Figure 6.18 reveals that, for same duty ratio, voltage gain of fully-tapped quadratic boost converter is highest among all the three converters and by increasing turn ratio gain can be further increased.

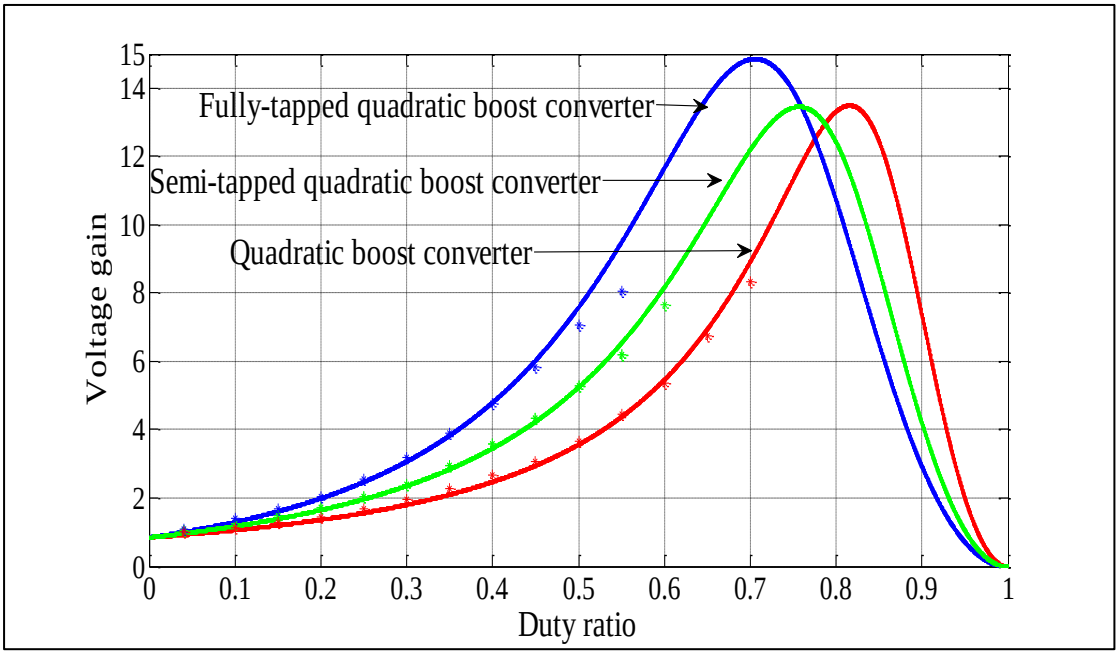


Fig. 6.18(a): Measured and calculated voltage gain for $n_1=n_2=1$.

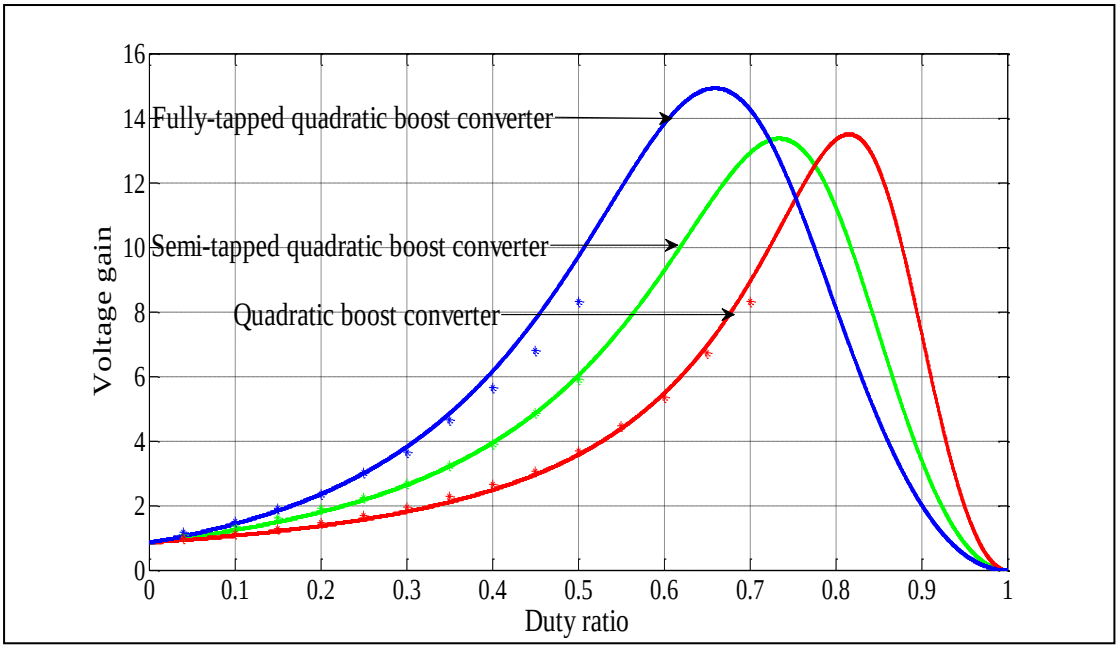


Fig. 6.18(b): Measured and calculated voltage gain for $n_1=n_2=1.5$.

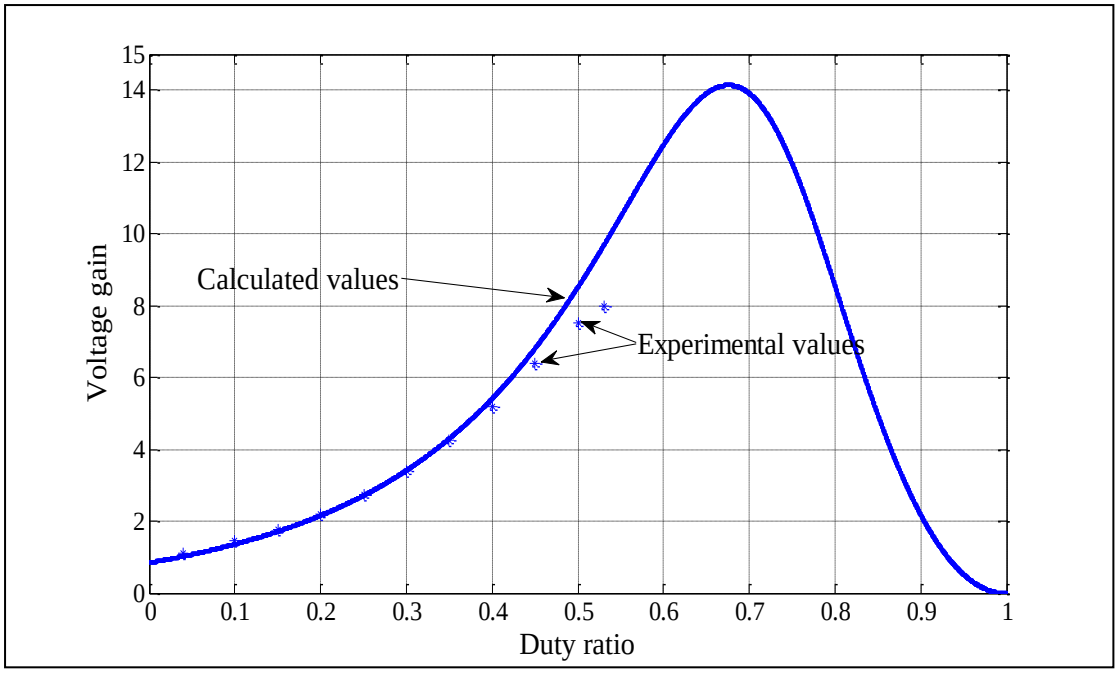


Fig. 6.19 (a): Calculated and measured voltage gain for n_1=1 and n_2=1.5.

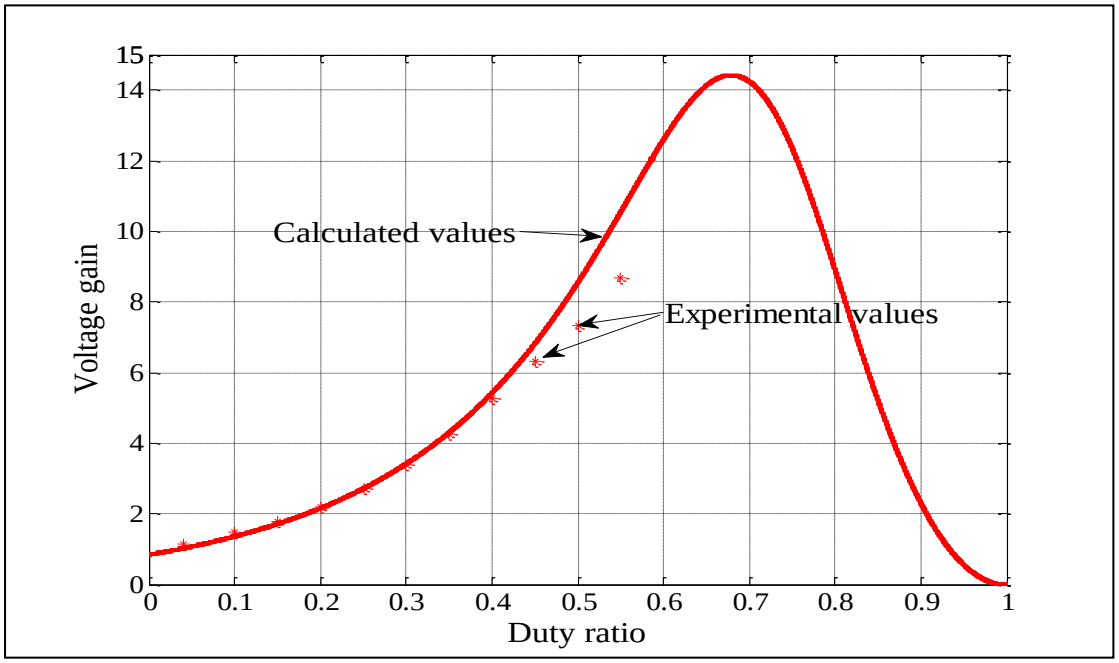


Fig. 6.19 (b): Voltage gain for n_1=1.5 and n2=1.

Experimental results of Fig. 6.18 are in good agreement with the performance analysis results of Fig. 6.14. Further, for fully tapped converter, Fig. 6.19 (a) shows the calculated and measured voltage gain plot for the turns ratio n_1=1 and n_2=1.5.

Figure 6.19 (b) shows voltage gain plot for n_1=1.5 and n_2=1. As stated above, fully tapped converter has pulsating input current which will increase as turns ratio increases. Therefore for fully tapped converter, input tapped inductor can be designed with less turns ratio to reduce the pulsating current or one has to use input filter to avoid pulsating current which is drawn from the input source.

6.6 Conclusion

The semi-tapped quadratic boost converter and the fully-tapped quadratic boost converter are proposed in this chapter to obtain a higher voltage gain at lower duty ratios. Performance of these converters and quadratic boost converter is analyzed under steady state conditions. The analysis shows that for same duty ratio, the voltage gain of fully-tapped quadratic boost converter is highest among the three converter followed by semi-tapped quadratic and quadratic boost converter. The voltage gain and voltage stress over the switch of semi-tapped and fully-tapped converters is a function of duty ratio and turns ratio of tapped inductor. The comparison of voltage stress on active and passive switches reveals that the voltage stress on the active switch is least in case of fully-tapped quadratic boost converter in comparison to other two converters for same output voltage. As the voltage stress over main switch reduces for both tapped-inductor based converters, thus low voltage rating and low on-state resistance switch can be used to decrease the power loss in switch. The proposed converters are simulated in PLEXIM-PLECS and the prototype of proposed converters and quadratic boost converter is implemented in the laboratory and the experimental results verify the theoretical analysis and simulation results of the converters.

Chapter 7
Conclusions

Step-up PWM DC-DC converters are required for wide range of applications and become a major thrust area of research. The objectives of this thesis is can be categorized in to (i) study and development of new converter configurations for high step-up applications, and (ii) on control of these converters.

The first part of the work focused on detailed study of fourth order step-up PWM DC-DC converter based on QZS converter topology. The converter studied provided same voltage gain as of Z-source DC-DC converter with reduced number of components. This converter configuration has all the features of quasi Z-source DC-DC converter. Average current mode control technique based closed loop controller was used for its output voltage control. Design procedure for controller and design expressions for converter components are presented.

In the next part of the work, same converter topology was used with tapped-inductor to enhance the voltage gain. In tapped-inductor based structure it is found that by increasing turns-ratio of tapped -inductor voltage gain can be further increased. However, due to tapped-inductor duty ratio range of converter is reduced.

Low ripple in input current of converter is desirable feature for renewable energy sources. In coupled inductor based work, a configuration of fourth order step-up converter is present to reduce the input current ripple. In this structure coupled-inductor is used to make input current ripple to zero. Due to coupled inductor weight and size of converter is also reduced. An experimental set up was built to validate and verify theoretical analysis.

A high step-up DC-DC converter is presented which gives higher gain at lower duty ratio. This converter is a combination of boost converter and fourth-order step-up DC-DC converter. The steady state analysis and small signal model of the converter is presented. Expressions are derived for calculation of losses in various components of the converter. A closed loop controller is designed and implemented for output voltage regulation.

Two new converter configurations namely semi-tapped and fully-tapped quadratic boost converters are proposed based upon quadratic boost converter and tapped inductor. It is found that voltage gain and voltage stress over the switch of semi-tapped and fully-tapped converters is a function of duty ratio and turns ratio of tapped

inductor. The comparison of voltage stress on active and passive switches reveals that the voltage stress on the active switch is least in case of fully-tapped quadratic boost converter in comparison to other two converters for same output voltage. As the voltage stress over main switch reduces for both tapped-inductor based converters, thus low voltage rating and low on-state resistance switch can be used to decrease the power loss in switch.

One cycle control technique is first time used to control Z-source based DC-DC converter and quasi Z-source based DC-DC converter. Control equation for each converter is derived. Control equation can be changed to use for controlling any capacitor voltage or DC link voltage. Further this technique is extended for fourth order step-up converter. Simulation and experimental results are presented to verify theoretical analysis. This method shows excellent dynamic performance in tracking the reference and input disturbance rejection for these converters.

Future Scope of the work

- Bidirectional operation of fourth-order step-up converter: It can be observed from the voltage conversion ratio of this converter that for duty cycle greater than 0.5, the converter gives negative voltage output. To implement this one needs four quadrant switches. Therefore, it will be interesting to study this converter for bidirectional power transfer.
- Semi-tapped and fully tapped quadratic boost converters: The current stress of the switch becomes higher for higher duty ratio and higher turns ratio. Hence using interleaving technique for current sharing would be an interesting study to improve the performance of the converter.
- To incorporate soft-switching with proposed converters: All the proposed converters are hard switching converters. The voltage and current stresses on the switches are observed to be significant. If one wants to go on higher switching frequencies, adapting soft switching for these proposed converters could be an interesting study.

APPENDIX-A

In chapter 2, transfer functions are given by equations (2.73)-(2.75) are rewritten as

$$G_{vd}(s)=\left.\frac{\hat{v}_0}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0}=\frac{G_1\left(V_{C1}+V_0\right)+G_2\left(V_{C1}+V_0\right)+G_3\left(-I_{L1}-I_{L2}\right)+G_4\left(-I_{L1}-I_{L2}\right)}{Q}$$

$$G_{i1d}\left(s\right)=\left.\frac{\hat{i}_{L1}\left(s\right)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0}=\frac{P_1\left(V_{C1}+V_0\right)+P_2\left(V_{C1}+V_0\right)+P_3\left(-I_{L1}-I_{L2}\right)+P_4\left(-I_{L1}-I_{L2}\right)}{Q}$$

$$G_{i2d}\left(s\right)=\left.\frac{\hat{i}_{L2}\left(s\right)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0}=\frac{F_1\left(V_{C1}+V_0\right)+F_2\left(V_{C1}+V_0\right)+F_3\left(-I_{L1}-I_{L2}\right)+F_4\left(-I_{L1}-I_{L2}\right)}{Q}$$

Where, details of G_1-G_4, P_1-P_4 and F_1-F_4 of equations are given below

$$G_1=D'(D'^2-D^2+s^2L_2C_1)$$

$$G_2=-D(-D'^2+D^2+s^2L_1C_1)$$

$$G_3=DD'(sL_1+sL_2)$$

$$G_4=(s^3L_1L_2C_1+sL_1D'^2+sL_2D^2)$$

$$P_1=s^3L_2C_1C_2+s^2L_2C_1/R+s\left(C_1D^2+C_2D'^2\right)+D'^2/R$$

$$P_2=DD'\left(sC_1+sC_2+1/R\right)$$

$$P_3=D\left(D^2-D'^2+sL_2\left(sC_2+1/R\right)\right)$$

$$P_4=-D'\left(D'^2-D^2+s^2L_2C_1\right)$$

$$F_1 = DD'\left(sC_1 + sC_2 + 1/R\right)$$

$$F_2 = s^3 L_1 C_1 C_2 + s^2 L_1 C_1 / R + s\left(C_2 D^2 + C_1 D'^2\right) + D^2 / R$$

$$F_3 = -D'\left(D'^2 - D^2 + sL_1\left(sC_2 + 1/R\right)\right)$$

$$F_4 = D(-D'^2 + D^2 + s^2 L_1 C_1)$$

APPENDIX-B

The voltage gain and input current in chapter 3 can be given by equations (3.1.31) and (3.1.32) as

$$\frac{V_0}{V_{in}} = \left\{ \frac{\left\{1 - \frac{D'V_{FD1}}{V_{in}}\right\}\left(g\left(i \cdot l + c \cdot j\right)\right) + \left\{-\frac{D'\left(V_{FD1} + V_{FD3}\right)}{V_{in}\left(N_1 + N_2\right)} - \frac{DV_{FD2}}{V_{in}N_1}\right\}\left(-c\left(i \cdot l + c \cdot j\right)\right)}{Y} \right\}$$

$$I_{L1} = I_{in} = \left\{ \frac{\left\{V_{in} - D'V_{FD1}\right\}\left(-g \cdot i \cdot k\right) + \left\{-\frac{D'\left(V_{FD1} + V_{FD3}\right)}{\left(N_1 + N_2\right)} - \frac{DV_{FD2}}{N_1}\right\}\left(c \cdot i \cdot k\right)}{Y} \right\}$$

Where, details of coefficient Y and other coefficients used in equations are given as

$$Y = c^2 \cdot f \cdot k - c^2 \cdot h \cdot j - b \cdot c \cdot g \cdot k + c \cdot d \cdot g \cdot j$$
$$- a \cdot g \cdot i \cdot k + c \cdot e \cdot i \cdot k - c \cdot h \cdot i \cdot l + d \cdot g \cdot i \cdot l$$

Where,

$$a = -\left\{D\left(r_{L1} + r_{C1} + r_S\right) + D'\left(r_{L1} + r_{D1} + r_{C0}\right)\right\}$$

$$b = \frac{-D'r_{D1}\left(N_1 + N_2\right)}{L_2}$$

$$c = D$$

$$e = \frac{-D'r_{D1}}{N_1 + N_2}$$

$$f = -\left\{\frac{D\left(r_{L21} + r_{D2} + r_{C0} + r_S\right)}{L_{21}} + \frac{D'\left(r_{L21} + r_{D1} + r_{D3} + r_{L22} + r_{C1}\right)}{L_2}\right\}$$

$$g = \frac{-D'}{N_1 + N_2}$$

$$h = \frac{D}{N_1}\left(1 - \frac{r_{C0}}{R + r_{C0}}\right)$$

$$i = \frac{D'\left(N_1 + N_2\right)}{L_2}$$

$$j = \frac{-DN_1}{L_{21}}$$

$$k = \frac{-1}{R + r_{C0}}$$

$$l = D'$$

$$m = -D'\left(1 + \frac{r_{C0}}{R + r_{C0}}\right)$$

APPENDIX-C

In chapter 5, the transfer function of output voltage to control can be given by equation (5.59) as

$$G_{vd}(s)=\left.\frac{\hat{v}_{C0}}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0}=\frac{G_1V_{C1}+G_2\left(V_{C2}+V_0\right)+G_3\left(V_{C2}+V_0\right)+G_4\left(-I_{L1}\right)+G_5\left(-I_{L2}-I_{L3}\right)+G_6\left(-I_{L2}-I_{L3}\right)}{Q}$$

where G_1-G_6 details are given below

$$G_1=\frac{D'^2\left(s^2L_3C_1-2D+1\right)}{Q}$$

$$G_2=\frac{D'\left(s^2C_1L_1+D'^2\right)\left(s^2L_3C_1-2D+1\right)}{Q}$$

$$G_3=\frac{-D\left(s^4C_1C_2L_1L_2+s^2\left(L_1C_2+D^2L_1C_1-D'^2L_1C_1+D'^2L_2C_2\right)+D^2D'^2-D'^4\right)}{Q}$$

$$G_4=\frac{sD'L_1\left(s^2C_2L_3-2D+1\right)}{Q}$$

$$G_5=\frac{DD'\left(s^3L_1L_2C_1+s\left(D'^2L_3+L_1+L_2D'^2\right)+s^3L_1L_3C_1\right)}{Q}$$

$$G_6=\frac{\begin{array}{l}s^5L_1L_2L_3C_1C_2+s^3\left(L_1L_3C_2+D^2L_1L_3C_1+D'^2L_1L_2C_1+D'^2L_2L_3C_2\right)+\\sD'^2\left(D^2L_3+D'^2L_2+L_1\right)\end{array}}{Q}$$

APPENDIX-D

In chapter 6, the steady state voltage gain of fully-tapped inductor quadratic boost converter can be given as

$$\frac{V_0}{V_{in}}=\left\{\begin{array}{l}\left\{\left(\left(\frac{D}{N_{11}}+\frac{D'}{\left(N_{11}+N_{12}\right)}\right)-\frac{D'V_{FD1}}{V_{in}\left(N_{11}+N_{12}\right)}-\frac{DV_{FD2}}{V_{in}N_{11}}\right\}\left(-e\cdot h\cdot j\right)+\right.\\ \left.\left(-D'V_{FD3}/\left(V_{in}\left(N_{21}+N_{22}\right)\right)\right)\left(c\cdot h\cdot j\right)\end{array}\right\}/Y$$

And the steady state value of flux through the core of inductor L_1 is given as

$$\Phi_1=\left\{\begin{array}{l}\left\{\left(\left(\frac{V_{in}D}{N_{11}}+\frac{V_{in}D'}{\left(N_{11}+N_{12}\right)}\right)-\frac{D'V_{FD1}}{\left(N_{11}+N_{12}\right)}-\frac{DV_{FD2}}{N_{11}}\right\}\left(-e\cdot i\cdot m\right)+\right.\\ \left.\left(-D'V_{FD3}/\left(\left(N_{21}+N_{22}\right)\right)\right)\left(c\cdot i\cdot m\right)\end{array}\right\}/Y$$

Where, details of Y and other coefficients are given below

$$Y=b\cdot e\cdot h\cdot m-a\cdot e\cdot i\cdot m+c\cdot l\cdot i\cdot m-c\cdot f\cdot h\cdot m+c\cdot g\cdot h\cdot j$$

Where

$$a=-\left\{\frac{D\left(r_{L11}+r_{D2}+r_S\right)}{L_{11}}+\frac{D'\left(r_{L11}+r_{D1}+r_{L12}\right)}{L_1}+\frac{D'r_{C1}}{L_1}\right\}$$

$$b=\frac{D'r_{C1}\left(N_{21}+N_{22}\right)}{L_2\left(N_{11}+N_{12}\right)}$$

$$c=\frac{-D'}{\left(N_{11}+N_{12}\right)}$$

$$e=\left\{\frac{D}{N_{21}}+\frac{D'}{\left(N_{21}+N_{22}\right)}\right\}$$

$$f = -\left\{ \frac{D\left(r_{L21} + r_{C1} + r_S\right)}{L_{21}} + \frac{D'\left(r_{L21} + r_{D3} + r_{L22}\right)}{L_2} + \frac{D' r_{C1}}{L_2} \right\}$$

$$g = \frac{-RD'}{\left(N_{21} + N_{22}\right)\left(R + r_{C2}\right)}$$

$$h = \frac{D'\left(N_{11} + N_{12}\right)}{L_1}$$

$$i = -\left\{ \frac{DN_{21}}{L_{21}} + \frac{D'\left(N_{21} + N_{22}\right)}{L_2} \right\}$$

$$j = \frac{D'\left(N_{21} + N_{22}\right)}{L_2}$$

$$l = \frac{D' r_{C1}\left(N_{11} + N_{12}\right)}{\left(N_{21} + N_{22}\right)}$$

$$m = \frac{-1}{R + r_{C2}}$$

LIST OF PUBLICATIONS

Journals:

1) Patidar K., Umarikar A.C., *"A high step-up PWM DC-DC Converter based on quasi z-source Topology,"* IET Power Electronics, 2014 (in press).

2) Keshav Patidar, Amod C. Umarikar, *"High step-up converters based on quadratic boost converter for micro-inverter,"* Electric Power Systems Research, Volume 119, Pages 168-177, February 2015, ISSN 0378-7796.

3) Keshav Patidar, Amod C. Umarikar, "*A step-up PWM DC-DC Converter for renewable energy applications*," International Journal of Circuit Theory and Applications (revision has to submit)

Conferences:

1) Patidar K., Umarikar A. *"Control of DC link voltage in quasi Z-source inverter by using one cycle control method,"* IEEE International conference Power Electronics, Drives and Energy Systems (PEDES), IIT Bombay, India, December 16-19, 2014.

2) Patidar K., Umarikar A. *"One Cycle control of Z source and Quasi Z source DC-DC Converters,"* 6th National Power Electronics Conference (NPEC), IIT Kanpur, India , December 20-23 , 2013.

3) Patidar, K., Umarikar, A.C., "*A space vector PWM signal generation for Z-source inverter using only sampled amplitudes of reference phase voltages with a unified method to implement different shoot through strategies,"* Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on, IISc. Bangalore, December 16-19, 2012.

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