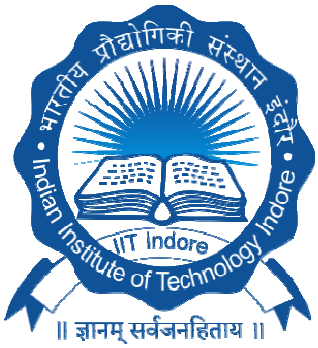
Evaluation of Nanoscale MOSFET Architectures for Low Power Analog/RF Applications

Ph.D. Thesis

by

Dipankar Ghosh



DISCIPLINE OF ELECTRICAL ENGINEERING

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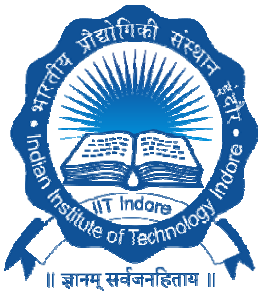
Evaluation of Nanoscale MOSFET Architectures for Low Power Analog/RF Applications

A THESIS

Submitted in partial fulfillment of the
requirements for the award of the degree
of
DOCTOR OF PHILOSOPHY

by

Dipankar Ghosh



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December 2015

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **Evaluation of Nanoscale MOSFET Architectures for Low Power Analog/RF Applications** in the partial fulfillment of the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY** and submitted in the **DISCIPLINE OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from January 2012 to December 2015 under the supervision of Dr. Abhinav Kranti, Associate Professor, Electrical Engineering, IIT Indore.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Signature of the student with date
(DIPANKAR GHOSH)

This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

Signature of Thesis Supervisor with date
(Dr. Abhinav Kranti)

DIPANKAR GHOSH has successfully given his Ph.D. Oral Examination held on **<Date of PhD Oral Examination>**.

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2. Ghosh D., Parihar M.S., Armstrong G.A., Kranti A. (2012), High performance junctionless MOSFETs for ultra low power analog/RF applications, IEEE Electron Device Letters, 33, no. 10, pp. 1477-1479.

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ABSTRACT OF THE DISSERTATION

Evaluation of Nanoscale MOSFET Architectures for Low Power
Analog/RF Applications

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Scaling dimensions for new and continuing product cycles has introduced new challenges for transistor design. As the end of the technology roadmap for semiconductors is approaching, new device structures are being investigated as possible replacements for traditional Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs). This new device technology is expected to be energy efficient, dense, and enable more device function per unit space and time. Analog/RF designers have faced difficulty to scale down the devices as aggressively as logic designers because of the severe degradation in performance which is due to intrinsic and extrinsic parameters. As a result not much attention has been devoted to miniaturization of analog/RF devices as compared to logic applications. This thesis investigates the analog/RF performance of nanoscale architectures like underlap inversion mode MOSFETs, junctionless transistors and tunnel FETs. These devices are aimed to operate at supply voltages of 0.5 V which has enabled by lower subthreshold swing, enhanced gate controllability and reduced parasitic components.

Published research work is briefly reviewed to better appreciate the research landscape regarding analog/RF performance of nanoscale MOSFET. Devices fabricated in Silicon-on-Insulator (SOI) technology are investigated as they are the most promising and foundry feasible solution for advancing to the nanoscale MOSFET design and functionality. SOI technology has been widely used for nanoscale regime due to excellent capability to overcome Short-Channel-Effects (SCE). Multi-Gate (MG) SOI MOSFETs exhibit improved short-channel effects immunity. The enhancement of the mobility of carriers in MG MOSFETs is due to volume inversion in which the entire silicon film gets inverted and offers reduced carrier scattering particularly useful for low power applications. MG SOI MOSFETs with enhanced performance still face the issue of low-power operation needed for

future generation wireless applications and get stuck in design issues related to efficient scaling scenarios where performance should not be compromised.

The thesis work starts with a discussion on the gate to source/drain region underlap in classical inversion-mode MOSFET architecture to mitigate issues related to downscaling like parasitic resistances and capacitances. The channel design through source/drain extension region engineering achieves this performance improvement in Double-Gate (DG) SOI technology due to reduction in drain electric field in classical inversion-mode MOSFETs. The design presents a trade-off between device spacer-width and lateral straggle and thus the performance optimization could be specific to the circuit application. Analog/RF performance of DG MOSFET is investigated through well calibrated device simulations at nanoscale dimensions and. Performance results for analog/RF figure-of-merits (FOM) of the DG structure is presented through optimisation around sweet spot ultra low power regime. In particular the ultra low power (ULP) performance metrics are shown to be improved due to reduction of parasitic components.

The work is then extended to evaluate the analog/RF performance metrics in junctionless transistors for low power applications. A junctionless (JL) transistor has the same type of dopants in the source, drain and channel regions. This eliminated the need for costly ultrafast annealing techniques and are easier to fabricate. As a first step, the enhanced performance metrics achieved by junctionless against classical inversion-mode MOSFETs architecture is attributed to an inherent device underlap, offered by JL devices. This opens up the opportunities available while designing junctionless transistor for optimum analog/RF performance. Design guidelines for junctionless structure is then presented with the help of simulations focusing on spacer width of source/drain extension regions and channel doping to minimize parasitic capacitance and drain electric field. The proposed design is also beneficial for operation around analog sweet spot to achieve higher gain, bandwidth and linearity metrics which overcome the conventional analog design trade-offs. The proposed improved junctionless low power transistor exhibits much lower parameter sensitivity values.

Band-to-band tunneling (BTBT) in semiconductors, often viewed as an adverse effect of short channel lengths, had been proposed as a promising current injection mechanism to allow for reduced operating voltages in nanoscale MOSFETs. The conventional lateral tunnel FET in which tunneling occurs from source to channel region due to the gate electric field has shown lower leakage current and enhanced short-channel immunity. These devices show scaling trends in

decananometer regime, if optimized with specific band-gap material in source/channel tunneling interface region along with low-κ spacer. Device simulations are used to optimize tunnel FET structures involving vertical tunneling. In a vertical tunnel FET, tunneling is expected to enhance with the alignment of gate electric field and source/channel tunnel junction. Various advantages of a vertical tunnel FET is verified through device simulations over lateral tunnel FET. This includes optimization of gate and drain overlap/underlap region and dielectric-spacer combination in lateral tunnel FET, Si_xGe_{1-x} channel thickness and Ge mole fraction in hetero-structure vertical tunnel FET.
The thesis work offers an assessment of analog/RF performance metrics in emerging MOSFET device architectures for low power applications. The research work has shown that analog trade-off in terms of gain, bandwidth and linearity can be effectively balanced using underlap channel architecture and the same topology can be effectively adapted in junctionless transistors also. Leakage current and parasitic capacitance is found to be still higher in case of both tunnel FETs. Optimised lateral and vertical tunnel FETs showcase high intrinsic gain as compared to both underalap inversion-mode and optimised junctionless MOSFETs. This work provides new perspectives into the operation of emerging MOS devices from an analog/RF domain, and will be useful for benchmarking for analog/RF applications.

Chapter 1

Introduction

1.1 Modern Analog/RF Electronic Systems

Radio frequency (RF) design in complementary metal-oxide-semiconductor (CMOS) technology has received much attention over the past 2 decades and is increasingly becoming a serious contender for RF wireless systems. While CMOS is not an obvious technology for RF millimeter wave applications in terms of performance, especially compared to SiGe and III-V technologies, it has clear advantages including low cost and potential for integration with other logic technology circuitry part of modern electronic system which makes it a natural candidate for exploration [1,2] for low power short range miniaturized wireless systems [3]. Applications that fall in this category are third and fourth generation (3G/4G) cellular communication standards, emerging wireless LAN (Local area networks) standards and short range communication standards like Bluetooth and low power sensors for wireless sensor networks (fig. 1.1) [2-4].

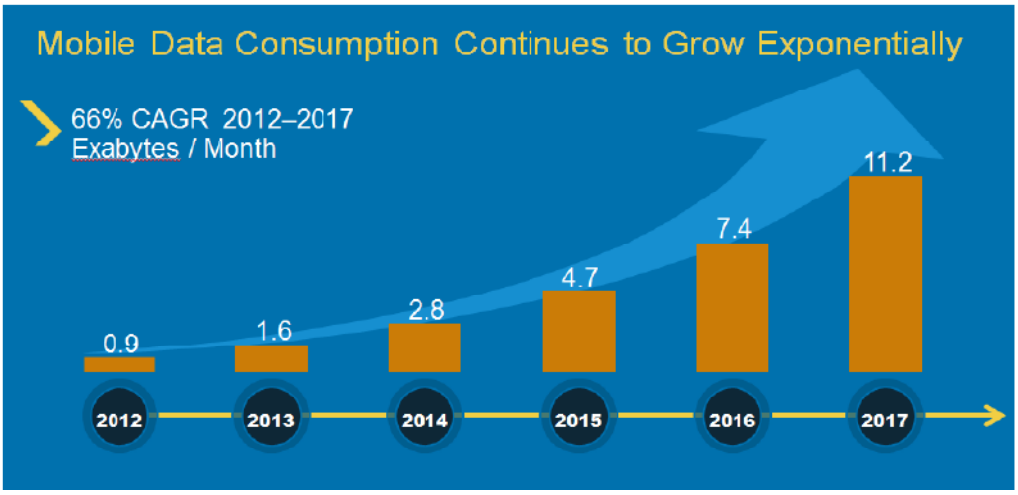

Fig.1.1 Growing demands of cellular data communication, RFMD Corporation, USA, IEEE S3S Conference 2014, California. 1 Exabyte (EB) = 10^{18} bytes = 1 billion gigabytes [4].

In particular, power minimization is crucial in emerging body implanted sensors technology [6], radio frequency identification systems (RFID) for traffic and health monitoring and unique identification of consumables, and advanced applications like evolutionary body-sensor networks, which require power consumption in microwatt range in order to enable the constituent transceiver to operate without on-chip integrated power supply along with having an extremely longer battery-life. In addition these systems may operate in the presence of large amplitude blocking signals, and, hence the linearity requirements for the transistors and the entire system become a limiting specification. Such stringent linearity requirements ensure protection from inter-modulation products and higher-order harmonics [7]. The increasing complexity of wireless communication transceivers makes the power minimization of accompanying RF front-end as one of the most important design objectives. While such systems do not have stringent sensitivity requirements, low power consumption stands as an absolute must. Due to its high integration capability and continuously scaled feature size, CMOS technologies remain a prime candidate for the future developments of Ultra-Low Power (ULP) integrated circuits [1, 3]. An extensive prior research on CMOS for ULP digital IC design has laid the foundation for design of microwatt baseband/broadband communication systems [7]. This evolution in CMOS technology is majorly motivated by decreasing price for specified performance of digital logic circuits. CMOS ensures efficient packing density for digital circuitry and to keep power consumption at an acceptable level, the dimensions of the active device should shrink more and more. This shrinkage has been supported by lowering of supply voltages through the technology generations. The pace of scaling of MOS devices in digital circuits is determined by Moore's Law [8]. While this evolution is truly very beneficial for digital applications, it has not being at the same pace for analog/RF applications.

The reasons for above are the trade-offs associated with analog/RF designs of scaled MOSFETs and shall be discussed in following chapters. The demands in contemporary Integrated Circuits (IC's) are mixed-signal, both analog and digital. The systems consisting of a large digital core includes amongst others a Central Processing Unit (CPU) or Digital Signal Processor (DSP) and memory, surrounded by several analog interface blocks such as I/O, Digital to Analog (D/A), and Analog to Digital

(A/D) converters, RF front ends including power amplifiers, RF switches, low-noise amplifiers [7]. From an ideal integrated circuit, all these functions should ideally be integrated on a single die. In this case, the analog electronics must be realized on the same die as the digital core. The evolution is dictated by the digital applications as number of MOS transistors for the digital circuits will always out number that are presents in analog/RF circuits [3, 7].

1.2 MOSFET Scaling

Several issues such as degradation of gain, bandwidth and linearity in analog/RF designs in CMOS processes and possible ways to maintain performance have been investigated in the past decade [2-7]. Silicon MOSFETs have been considered as slower devices as compared to III–V group and other compound semiconductors, which dominated as solid-state devices in Radio Frequency Integrated Circuits (RFIC) [1-3, 9]. The reason contributing is the electron mobility. Mobility, which measures how fast the free electrons can move in the semiconductor, in Si is by nature lower than in III–V group and other compound semiconductors [9]. Another reason for low mobility is that the inversion channel of a classical MOSFET is located very close to the Si/SiO_2 interface where it is subjected to the scattering effects of interface roughness, bulk crystal imperfections, and interface traps [9]. As a result, the mobility of free electrons traveling in the inversion channel is degraded [3, 4]. Besides the reasons of low-field mobility in MOSFET channel, a second reason for the inferior MOSFET RF performance has been the relatively longer channel/gate length than that had been used for logic technologies [9]. Due to the aggressive reduction in this device feature size in the past decade as a result to meet the high demands of Very Large Scale Integration (VLSI) of transistors, Si MOSFETs are better suited as RF transistors [9]. This is an outcome of tremendous research that was conducted for finding newer device designs to mitigate the performance degradation issues due to scaling [9].

The basic structure of a MOSFET consists of a gate with its dielectric, semiconductor substrate, heavily doped source and drain regions and metal electrode contacts. The device dimensions and other features have been scaled down continuously to meet the demands of higher speed and increased compactness. The gate length is the

main feature guiding the MOSFET performance [9-15]. Reducing the channel length, however, requires the scaling of other features such as the oxide thickness, drain/source junction depth, and substrate doping density. When the gate length is reduced, the oxide thickness needs to be reduced so that the gate can have a better control of the channel and provide better electrostatic controllability [3, 4, 13]. Typically, the gate is made of a heavily doped polysilicon or midgap material, and silicides are frequently deposited underneath the drain/source contacts to reduce the contact resistance [16]. Unfortunately, undesirable effects called short channel effects (SCE) are very severe in nanometer MOSFETs. To alleviate such effects, several additional features have been added to the basic MOSFET structure that will be discussed in next sections. Advanced device designs required for performance enhancement which improve gate controllability will also be discussed.

1.3 Advanced MOSFET Design

In the past, drain voltages in the range of 2 V and more were used and channel engineering has been widely used to improve the short channel performance [10]. Basically these device short-channel effects arises due to control of channel region by gate electrode gets effected by electric field lines from drain. An important phenomenon associated with the short-channel effects is the threshold voltage roll-off (i.e., threshold voltage starts to decrease when the channel length is reduced below a critical value) [3, 4]. This was found to be effectively eliminated by the use of halo or pocket-implant MOSFET [8]. Significant modification to the MOSFET has been the introduction of the Silicon On Insulator (SOI) technology, where the transistor body is separated from the semiconducting wafer by an insulating layer [9,11]. Short-channel effects can be reduced in MOSFET by using a thin buried oxide and an underlying ground plane. In a Fully Depleted SOI (FDSOI) device, the source/drain field lines propagate through the buried oxide (BOX) before reaching the channel region (Fig. 1). But FDSOI structure has the issue of increased junction capacitance and body effect [10]. A much more efficient device configuration is obtained by using the Double-Gate (DG) transistor structure. The electric field lines from source and drain terminate on the bottom gate electrode and do not reach the channel region (Fig. 1) [10].

Another device degradation mechanism in MOSFETs are the Hot-Carrier Effect (HCE) which measures device reliability [3, 13]. The hot-carrier-induced degradation in SOI devices is more complex than that of bulk devices due to the presence of two silicon-oxide interfaces. The aggressive scaling of devices further aggravates this problem because of increase in the gate electrode electric field [11]. This high electric field provides sufficient energy to the channel carriers so as to cause impact ionization. The large number of highly energetic carriers damages not only the front interface, but also the back interface, monitored as the substrate current for the NMOSFET and the gate current for the PMOSFET [11-14]. To minimize performance degradation at nanoscale integration due to hot-carrier effects [9], lightly doped drain/source regions were implemented in MOSFETs [10]. These asymmetric MOSFET structures had been introduced for bulk [3] as well as for SOI MOSFETs [3, 14] to improve the device reliability. Moreover, in recent years SOI technology got a major boost in terms of acceptance with the implementation of multiple-gate low-power designs like Double-Gate Fully-Depleted SOI (DG FDSOI MOSFET) [10], which are used across major semiconductor foundries to improve performance trends.

As mentioned before another major issue is the reduction of supply voltage. Most analog circuits can still be designed although the supply voltage has dropped from 3-5 V in the early nineties down to 1 V [7]. Although the analog transistor properties do not really get worse when comparing them at similar bias conditions, lower supply voltages require biasing at lower operating voltages which results in worse transistor properties, and hence yield circuits with lower performance [7]. This necessitates the transistor operation in the moderate inversion region, which is the range of gate-bias just at the edge of threshold voltage (voltage at which the transistor is switched on. The current levels in the moderate inversion are far less than that is required in higher power applications [9]. In order to achieve performance at nanoscale dimensions, the MOSFET devices are recently being investigated to newer design scenarios like engineering source/drain extension regions for parasitic reduction, employing transistors without junctions to ease manufacturability and novel operating mechanisms like band to band source/drain to channel tunneling. In subsequent chapters each of these designs investigated in detail for low power analog/RF performance.

1.4 Analog/RF Performance Metrics

Now in order to fully appreciate the usefulness of Si based transistors, one needs to evaluate the device performance metrics at nanoscale dimensions. Due to the exponential dependence of the drain current on both the gate and drain voltage, the weak and moderate inversion regions are generally dismissed for low-distortion analog/RF applications [5]. While the cut-off frequency, ($f_T = g_m/C_{gg}$, g_m is transconductance and C_{gg} is gate capacitance), of a transistor biased in weak inversion is too low for RF applications, there is sufficient current gain for most RF applications while biased in the moderate inversion region, especially with sub-micron devices [5]. In addition, measurements have shown a significant peak, or "sweet spot," of linearity metric in terms of the third-order intercept point, in the moderate inversion region [5]. Moreover, the peak shifts systematically to higher drain current per unit width as CMOS technology scales to smaller gate lengths [5]. This peak occurs as the mechanism for the drain current flow when biased in the weak inversion region changes from diffusion, a largely exponential behavior, to drift, a slightly less than square-law type behavior (i.e., the exponent is slightly less than two), when biased in the strong inversion region [5]. Currently, deep sub-micrometer Complementary Metal Oxide Semiconductor (CMOS) processes typically reach several tens of GHz cutoff frequency f_T making them a serious alternative to the traditional III–V compound semiconductor devices for low power operation.

An important measure of RF transistor is the cutoff frequency (f_T). This is the frequency at which the small signal current gain (h_{21}) of the transistor rolls off to unity [9]. Applying a frequently used rule of thumb that the cutoff frequency should be around 10 times the transistors operating frequency [9], one could use these devices to design integrated circuits operating up to 20 GHz, an operating frequency higher than that for the great majority of modern RF electronics. However, a high cutoff frequency is not the only requirement for a good RF transistor. Other figures of merit are low parasitic capacitance, high intrinsic gain and high maximum frequency of oscillation (f_{max}), frequency at which the transistors Unilateral power gain (U) rolls off to unity (i.e., 0 dB), is often desirable [11, 16]. Some results have been reported about the

limitation or degradation of high frequency characteristics versus the downscaling of the channel length [16]. As stated earlier, silicon MOSFETs offer the possibility to realize Systems-On-Chip (SOC) by implementing low-power and large scale integration and high reliability. But there have been challenges associated with CMOS scaling like gate controllability and mobility degradation. As channel length is reduced, higher channel doping and thinner gate-oxide (T_{ox}) is used to control short channel effects (SCEs) of conventional bulk MOSFETs [15]. The g_m for a constant drain current (I_{ds}) decreases with increasing channel doping, due to mobility degradation [15]. In the results to be discussed in subsequent chapters we demonstrate low power operation of MOSFET devices at low current levels.

1.5 Silicon-on-Insulator (SOI) Technology

In particular in deep submicron CMOS technology, the loss of gate control over channel charge and increased parasitic capacitance degraded RF performance [16]. Since Silicon-on-Insulator (SOI) devices offer improved SCE [17] than bulk devices especially for higher channel doping N_a, it requires a reduced gate-overdrive ($V_{gt} = V_{gs} - V_{th}$), where V_{th} is threshold voltage, for a given I_{ds}. Hence it provides higher surface mobility resulting in higher transconductance (g_m) and g_m/I_{ds} ratio [18-20]. For lower channel doping (N_a), mobility is roughly independent of N_a. In this regime where g_m is high, series resistance significantly affects the performance [15]. Fully depleted (FD) SOI technology emerged as promising technology [20] but has certain limitations as discussed in subsequent paragraphs. An increase in the channel doping reduces g_m and f_T of a bulk MOSFET, due to impurity carrier scattering, but improves its output resistance (R_{out}) and intrinsic gain ($g_m \times R_{out}$), resulting in a tradeoff between f_T and gain. In the case of FDSOI devices, increasing N_a increases R_{out} only slightly due to its weak dependence of the SCEs on the channel doping [15]. Thus, SOI devices show higher gain as well as higher f_T for lightly doped channels, a trend opposite to that shown by bulk MOSFETs [16]. In FDSOI devices, the silicon thickness determines the amount of source/drain charge sharing and the coupling between the back and the front gates. A thicker silicon thickness (T_{Si}) with the same channel doping increases the depletion charge [16] and hence the vertical electric field, resulting in lower mobility which causes a degradation in the g_m/I_{ds} ratio, which is metric for power efficiency of device

for low power applications [18]. This effect is stronger for higher channel doping. Thus degradation in g_m/I_{ds} for short channel, lightly doped and thick film FDSOI MOSFETs is severe due to increased source/drain charge sharing.

However, thinner T_{Si} devices have higher g_m due to reduced parasitic source/drain series resistance. The drain-body coupling decreases with thinner T_{Si}, resulting in larger R_{out} [15]. In short-channel devices for thinner T_{Si}, significant improvement in R_{out} is observed due to much suppressed DIBL as discussed in the previous sections. For a bulk MOSFET, the gain vs. f_T curves shift towards high intrinsic gain and lower f_T as the gate oxide thickness is scaled down [15]. In order to maintain the same V_{th}, thinner T_{ox} requires a higher N_a, resulting in improved intrinsic gain and a degraded f_T. This is the gain-speed trade-off of analog/RF MOSFETs. For a mid-bandgap gate FDSOI MOSFETs, the intrinsic gain vs. f_T and g_m/I_{ds} ratio vs. gain curves show significant degradation with thick T_{ox} due to reduced gate control. In the case of n^+ poly gate, N_a is high causing a decrease in mobility which counteracts the high gate-control gained by thinner T_{ox}. Thus, g_m does not improve with T_{ox} scaling [15]. Moreover, higher doping also increases gate capacitance (C_{gg}) and therefore, degrades f_T. The intrinsic gain is higher for the devices with thin T_{ox} as the R_{out} shows significant improvement. Degradation in f_T for thin T_{ox} is smaller in FDSOI technology. Consequently, aggressive T_{ox} scaling becomes more important in the FDSOI devices to improve performance [15].

1.6 Multiple Gate MOSFET

As SOI transistor is scaled, the buried oxide (BOX) thickness decreases. It has been shown that decreasing the BOX thickness has the advantage of decreasing the penetration of electric field from the source/drain regions into the body via the BOX (i.e., fringing effects), thus increasing the immunity to SCEs [19]. Decreasing the BOX thickness also has the advantage of improving the heat dissipation ability of the device. However, decreasing the BOX thickness results in increased fields, which decreases carrier mobility. Also, the coupling factor involving the channel and oxide capacitances increases, which can increase the subthreshold swing. Hence, a careful optimization of the BOX is required.

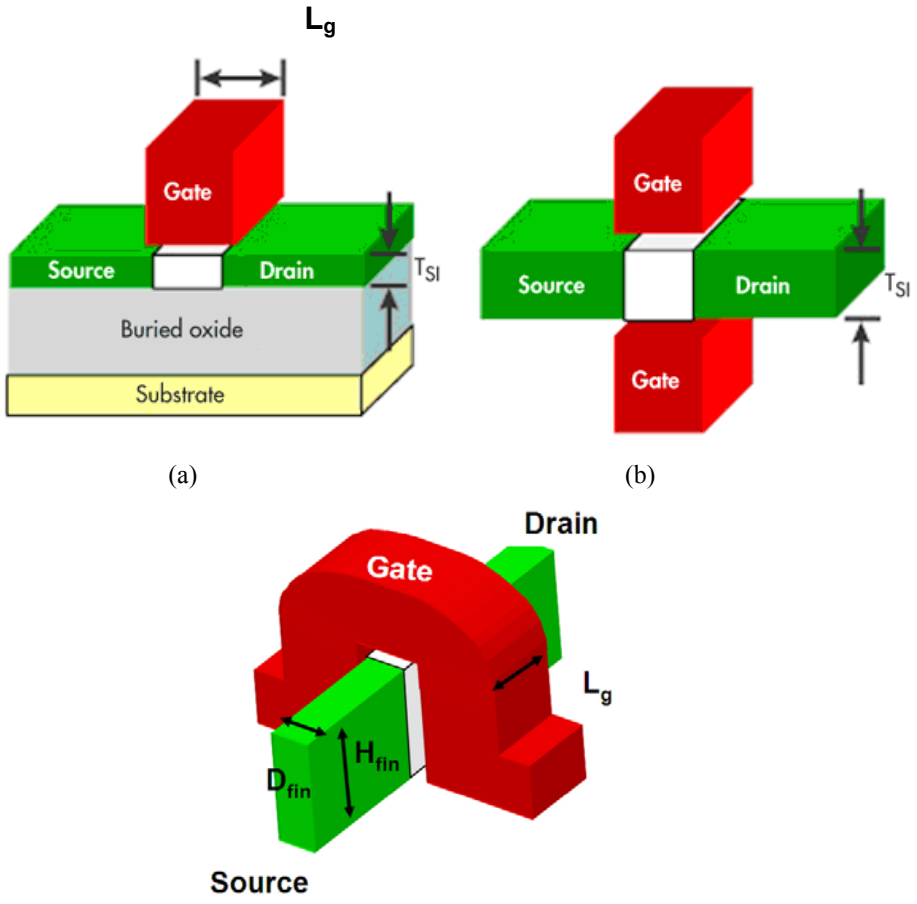

Fig. 1.2. (a) FDSOI [17] (b) Double Gate [20] (DG) MOSFET planar device schematic (L_g - gate length and T_{Si} - silicon film thickness, source/drain contacts not shown) and (c) FinFET [21] (H_{fin} and D_{fin} - Fin height and width) schematic - a 3D implementation of multi-gate MOSFETs.

The Double Gate (DG) Fully Depleted Silicon-On-Insulator (FDSOI) MOSFET has received great attention in recent years, in their 2D/3D architecture (fig. 2 a-c), owing to the inherent suppression of short channel effects (SCEs), excellent subthreshold slope (S), improved drive current (I_{ds}) and transconductance (g_m), volume inversion for symmetric devices and excellent scalability [20-21] and is considered as a possible alternative for the bulk MOSFET for low voltage applications. The above mentioned features make these multiple gate devices very attractive for analog/RF applications.

1.7 Organization of the Thesis

As discussed in previous sections, analog/RF performance of nanoscale MOSFETs for low power is yet to be investigated in detail. While considerable effort has gone into benchmarking these devices for low power logic applications, the emerging MOS devices are required to be evaluated for the suitablility and optimization for analog/RF applications. Three different MOSFET device architectures namely underlap inversion-mode, junctionless and tunnel FETs are investigated through ATLAS device simulations [22], widely accepted in leading academic universities and laboratories, to find useful insights for ultra-low power analog/RF applications.

In chapter 2, the underlap channel design in classical inversion-mode MOSFET with SOI technology is studied to understand the impact of channel engineering in the moderate inversion region around the analog sweet spot which represents a compromise between gain and bandwidth. Low power analog/RF devices in upcoming technologies are expected to operate around the analog sweet spot. Various trade–offs associated with the selection of optimal values of underlap region parameters have been indentified and guidelines for their selection established. It has also been demonstrated that underlap devices exhibit reduced parameter sensitivity in comparison to conventional abrupt S/D devices.

In chapter 3, the performance of junctionless transistor architecture for low power analog/RF applications is discussed. The specific attributes due to the absence of junctions in the MOSFET and its impact on analog/RF performance metrics for operation in subthreshold and around-threshold is investigated. The work is extended to propose an optimum design of junctionless transistor to further improve the performance metrics and lower parameter sensitivity towards analog/RF metrics. The performance of junctionless devices are also compared with classical inversion-mode MOSFET architecture which also have such optimized source/drain extensions for ultra-low power applications.

In chapter 4, the analog/RF performance metrics of tunneling based MOSFET architecture is investigated which has been proposed for steep switching logic applications as it presents a subthreshold swing significantly lower than the classical 60 mV/decade at room temperature. The analog/RF performance metrics are evaluated for

lateral and vertical tunneling FETs and performance compared with inversion-mode and junctionless transistors to establish advantages and challenges of different application scenarios.

In chapter 5, we conclude the performance outcomes of MOSFET design architectures which had been presented in previous chapters. Also, scope for further work through device architecture advancement using novel materials and circuit applications is proposed.

Chapter 2

Ultra Low Power Inversion Mode MOSFETs

2.1 Introduction

Device scaling has resulted in dramatic increase in performance over the past three decades. Source/Drain resistance had been a serious issue when operating a MOSFET in strong inversion i.e. above threshold operation, which has been the case for traditional MOS devices. This is due to the decrease in intrinsic channel resistance as the dimensions of MOS devices become smaller. However, extrinsic series resistance of these devices does not scale well. In this section, we shall discuss about parasitic resistance based optimization of MOSFET design which ultimately results of performance enhancement. These extrinsic parasitic resistances are a significant part of the total device resistance, and its impact on deep submicron device performance cannot be ignored for above threshold operation. Thus, MOSFET scaling faced the issue of high parasitic resistive components that were gate-voltage dependent (spreading and accumulation resistances) as manufacturability termed source/drain doping gradients as unavoidable. These components in a MOSFET device are inherent to the source/drain regions. The main controlling parameters of these resistance components are gate voltage and the steepness or abruptness of the doping gradient. Although the thesis work focuses on ultra low power operation where the effect of such parasitic resistances is negligible, the research on source/drain extension regions for the above threshold operation is discussed

It was found by Ng *et al.,* [23], that current conducts through the accumulation layer before spreading into the bulk region, and thus, the spreading injection resistance and the accumulation layer resistance should be considered in series with channel resistance. When the MOSFET is turned on, the accumulation layer is induced in the gate to source overlap region. The extension of this accumulation layer was determined by the point where the induced carrier concentration at the surface equals the background doping level [23]. This accumulation layer had a negligible effect on the more heavily doped source/drain region. It was pointed out in [23] that derivative of this

accumulation resistance with distance of current spreading, away from gate edge, was not found to be constant since surface mobility of the accumulation layer decreases with doping concentration. The value of spreading resistance depends heavily on the local resistivity where the current spreading takes place [23]. The farther the current spreading point is from the inversion channel, the lower is the spreading resistance. On the other hand, there is in series an additional component due to the resistance of accumulation layer [23]. As this point of current spreading shifts away from the channel end, the spreading resistance decreases, but the resistance due to the accumulation layer is increased [23]. There exists a point where the sum of the two resistances is at a minimum, and this was set as the criterion to determine the effective location of the point of current spreading into the bulk [23]. The experimental results quantifies these two complicated parasitic resistance components and emphasizes the importance of a steep junction profile to minimize the parasitic series resistance of MOSFETs [23].

Although the observations by Ng *et al.*, [23], for parasitic series resistance had shown improvement in device performance, contradictory performance resulting out of the abruptness of source/drain extension length had been reported later as the focus shifted to MOSFET devices of gate length down to nanometers [24]. It was further reported by Taur *et al.*, [24] that, to maintain adequate off-currents for a very large scale integration level of 10^8-10^9 MOSFET devices per chip, the threshold voltage must be kept at a minimum value under the worst-case conditions. For such low threshold voltage, a suitable choice of the power supply voltage is 1.0 V, as a reasonable trade-off between active power, device performance, and high gate vertical field effects. While direct 2-D scaling of MOSFETs require a gate oxide thinner than 1 nm for 25 nm MOSFETs, direct tunneling leakage in oxide/nitride gate insulators limits the equivalent gate oxide thickness to ≈1.5 nm [24]. Without scaling gate oxide and supply voltage, an optimized and non-uniform doping profile, termed as the ‘‘super-halo’’ by Taur *et al.,* is needed to control the short-channel effects [24]. The highly nonuniform profile tends to offset short channel effects, yielding device off state current (I_{off}) independent of channel length variations between 20 and 30 nm. The superior short channel effect obtained with the superhalo, shown through simulations [24] was attributed to the nearly constant V_{th} dependence on channel length, super-halo allows a nominal device to operate at a lower threshold voltage, thereby gaining significant performance benefit:

30-40% improvement over non-halo devices. It was noted that Drain Induced Barrier Lowering (DIBL), which was still present in super-halo devices, had only a minor effect on the delay/speed performance of reported MOSFET devices.

Another merit of super-halo as mentioned [24] is that it relaxes on the junction depth scaling. It was shown that the V_{th} roll-off is rather insensitive to the vertical junction depth, with only a slight change when the junction depth was doubled from 25 nm to 50 nm for the same super-halo profile. This suggests a solution for the high resistance problem associated with very shallow extensions [25]. It had been experimentally shown that scaling source/drain extension vertical depths below 30-40 nm results in insignificant performance benefit for 100 nm MOSFET devices [25]. This was explained by considering a large increase in external parasitic resistance and poorer source/drain extension to gate coupling counteracts improvement in short channel effects due to reduced charge sharing caused by vertical depth scaling.

It was reported experimentally that ultimately scaled 16 nm MOS, with a l0 nm channel length and state-of-the-art junction techniques was too sensitive to Lightly Doped Drain (LDD) diffusion under the gate I_{off} increase by 5 decades per 5 nm dispersion charge in channel length) [26]. These were experimental results clearly indicating manufacturing issues at decananometer scale length MOSFETs. While using a non-overlapped design (low channel doping), I_{off} dispersion is 1000 times lower for the same 5 nm dispersion in effective channel length/gate length (L_g). These results signify that source/drain extension region engineering was an outcome of extensive study of parasitic resistances both verified through basics device physics based simulations and experiments. It had been shown, that when the lateral abruptness of the junction is increased from 6.5 nm/dec to 1.9 nm/dec, the on-currents improve by 22.7 % while the off-currents degrade by over an order of magnitude [27]. It was reported that threshold voltage roll-off, another metric of short channel effects, is degraded by lateral source/drain junction gradients that are too gradual (6.5 nm/decade), as well as those that are too abrupt (3.3 nm/decade) [27].

This behavior was verified through simulations by two competing effects of counter-doping and charge sharing [24]. The degradation of threshold roll-off by very gradual junctions was mentioned as a result of counter doping of the channel. These source/drain donor profiles extends into the channel and counter-dopes the edge of the

channel. This in turn decreases the threshold voltage by lowering the net channel doping. The more gradual the junction gradient, the more severe counter doping is, leading to increased degradation in the threshold voltage roll-off. To explain the degradation of threshold voltage roll-off by junctions with very abrupt lateral gradients, Kwong *et al.* [27] stated the charge sharing concept which is at the heart of the origin of short channel effects. Unlike the long channel device, a significant portion of the field lines emanating from the bulk charge in a short device terminate in the source and drain regions rather than terminating at the gate. In general, it was reported [27] that increasing lateral source/drain abruptness lowers series resistance, which tends to improve the drive current. However, for very abrupt junctions, this improvement is mitigated by the degradation in leakage currents due to more severe short channel effects.

The Double Gate (DG) FET had shown to have very good electrostatic gate control [20] over the channel, enabling gate length scaling down to 10 nm. Experimental prototypes of DGFETs have been demonstrated in both planar [20] as well as fin-like geometries (FinFET) [21]. In such a multiple-gate device, short channel effects, such as threshold voltage roll-off, DIBL and degraded subthreshold swing are avoided by using thin-film which should be nearly half of gate length [28].

The ultra-thin film introduces an extrinsic parasitic resistance in series with the channel and the source/drain electrodes. The effective gate overdrive is reduced by the voltage drop across this resistance. As a result it is expected that the transconductance and performance of the device as measured by available current drive and switching delay, is degraded. This problem may be severe in DGFET since the presence of two channels implies that twice the current flows through the series resistance, leading to higher potential drop across the extrinsic resistance. The optimal lateral abruptness of the source/drain extension doping profile for a bulk MOSFET was considered [9]. It was not clear whether the same results and conclusions would hold for advanced ultrathin body DG MOSFET structures where the process constraints and tunable parameters are quite different. At a certain distance, defined as the ‘underlap’, away from the gate edge, the source/drain doping rolls off laterally into the channel with an abruptness characterized by the lateral doping gradient (fig. 2.1*a-b* [28]. The

source/drain doping profile in this ultrathin extension region can be the key component that was optimized in the study [28]. The optimization for specific I_{off} shown in [16] essentially trades off short channel effects (suboptimal underlap) for increased series resistance (underlap greater than optimal value). It was reported [28] that in both cases, drive current degrades through the reduction of effective gate overdrive.

In another simulation study [29], the fringing field induced degradation caused by high-K gate dielectrics in sub-l00 nm MOS devices was discussed quantitatively. It was found that suppressing these effects is to use a specific combination of dielectric values for the gate insulator and the sidewall. As may be the expected that the impact of spacer fringing fields on source/drain extension parasitic resistances and capacitances [29] may suggest design guidelines for basic device performance enhancement. Although such work has been carried out for DGFET and FinFET [20-21] previously, but clear intrinsic device performance improvement for ultra-low power analog/RF circuits still needed extensive study to be done.

Dependence of a bias-dependent effective channel length, i.e the channel length under the control of gate, on source/drain region doping gradients had revealed [31] a systematic approach to optimization of the SCE-parasitic resistance tradeoff, depending on fin width and lateral source/drain doping straggle, via source/drain extension region engineering. The longer effective channel length results from the underlap region and significantly relaxes the fin thickness requirement of a finFET [31] for SCE control. The approach was exemplified in [32] for a well-tempered 18 nm finFET design, showing minimal parasitic capacitance and implying reduced Gate Induced Drain Leakage (GIDL) current [3,4] and enhanced CMOS speed for the underlap design. Results by Kranti *et al.*, have demonstrated that lateral source/drain doping gradient along with spacer width can not only effectively control short channel effects, thus presenting low off-current, but can also be optimised to achieve high values of on-currents [33-34]. A careful optimization of source/drain extension region results in nearly the same as in a device with abrupt source/drain, but more importantly, a lowering of I_{off} by nearly two orders of magnitude. The ratio of spacer to doping gradient lying between 2.5 and 4.5 are the optimum values for achieving a low I_{off} along with a high I_{on} in source/drain engineered DG devices.

2.2 Analog/RF Figures Of Merit (FoM)

In previous sections, the evolution and advantages of using source/drain engineering in DG MOSFET (fig 2.1*a-b*) design at nanometer scaled dimensions were mentioned. This section comprises of fundamental attributes of analog/RF MOSFET design which are affected by basic device design changes. Previously, a significant improvement of about 50% in voltage gain and 85% in cutoff frequency was found for DGMOSFETs with optimally engineered SDE regions as compared to devices with abrupt source/drain regions [34]. The doping (N_a) of *p*-type SOI layer of 10^{15} cm^{-3}, gate oxide thickness (T_{ox}) = 1.3 nm, film thickness (T_{si}) = 10 nm and gate/channel length (L_g) = 25 nm were the parameters for the devices [34]. The spacer width at the source and drain end was varied from $0.5L_g$ to $2L_g$. The S/D extension profile, defined by its gradient (d) at the gate edge, was varied from 5 nm/decade to 9 nm/decade. Authors evaluated other important analog parameters [34], such as - transconductance-to-current ratio (g_m/I_{ds}), Early voltage (V_{EA}), transconductance and total input capacitance to analyze the reason for the improvement in A_{VO} and f_T.

The basic challenge in analog/RF design of MOSFETs lies in achieving a balance between the bandwidth and the power efficiency of a circuit [35]. This tradeoff is highly dependent upon circuit architecture, performance and power specifications; it is still directly related to physical attributes of a transistor. For a MOSFET device, that operates as a linear transconductor, the two figures of merit are cut-off frequency (f_T) and transconductance to drain current (g_m/I_{ds}) ratio. While f_T (= $_T$ /2π, where $_T$ = g_m/C_{gg}), quantifies how much total gate capacitance (C_{gg}) must be driven at the controlling node per desired transconductance, g_m/I_{ds} ratio enumerates how much current must be invested per g_m. As the quiescent-point gate overdrive (V_{gs} • V_{th}) approaches zero, the strong-inversion approximation is no more valid, and g_m/I_{ds} ratio gradually approaches an upper limit in weak inversion. Trends for f_T and g_m/I_{ds} over several generations of technology (180 nm to 45 nm) had been shown previously by Murmann *et al.*, [35]. In contrast to g_m/I_{ds}, f_T of a transistor is largest in strong inversion and generally increases with gate overdrive. As a result, there exists a tradeoff between the transconductance efficiency and the bandwidth of a transistor [35]. A key task in ultra low power design is to determine V_{gs} • V_{th} such that the bandwidth objectives are met

while operating at the corresponding maximum possible g_m/I_{ds} (lowest power). For any such ultra low power scenario where the bandwidth is flexible and part of the overall optimization, a figure of merit can be the product of g_m/I_{ds} and f_T [35]. For the transistor channel length considered in [35], $g_m f_T/I_{ds}$ product was found to exhibit a ''sweet spot'' around a gate overdrive of 100 mV, which is also a commonly found bias condition in many of moderate-to-high speed designs of integrated circuits [35].

A fundamental factor that often helps mitigate a power penalty in scaled technologies derives from the exploitation of increasing f_T. While porting an analog function with a fixed bandwidth requirement to a shorter channel process, the constituent devices can be biased at a lower $V_{gs} - V_{th}$ (and hence higher g_m/I_{ds}) to provide the required f_T [35]. While working with high g_m/I_{ds} greatly helps in lowering power for applications that do not demand an extremely high bandwidth, it comes with a penalty in terms of linearity [35]. The subsequent sections will emphasize the effectiveness of optimising source/drain extension regions to improve the device performance for the above discussed analog/RF metrics. The feasible technological option for improving the analog/RF metrics is the use of underlap Source/Drain (S/D) architecture. We will demonstrate the usefulness of underlap S/D design to enhance analog/RF metrics without degrading linearity in moderately inverted (low power) MOSFETs in next section.

The present work provides valuable design insights in the performance of nanoscale DG SOI devices with optimal source/drain engineering and serves as a tool to optimize important device and technological parameters for 65 nm technology node and below. Nanoscale underlap Multi-Gate, Surrounding-Gate MOSFETs and FinFETs have been reported recently [36-54] with performance improvement achievable through design modifications. Device performance metrics like intrinsic delay, subthreshold slope and noise margin for logic technology applications [38-47], linearity measured through harmonic distortion, cut-off frequency, intrinsic dc gain and f_{max}/f_T ratio, for analog/RF applications were found to be superior as compared to abrupt junction devices [48-54]. The present work is different in the sense that it provides valuable design insights in the performance of nanoscale DG SOI devices with optimal source/drain engineering and serves to optimize important device and technological

parameters around moderate inversion "sweet spot" for low power analog/RF applications.

2.3 ATLAS Simulations

2.3.1 Inversion Layer Mobility Models

To obtain accurate results for MOSFET simulations, one needs to account for the mobility degradation that occurs inside inversion layers. The degradation normally occurs as a result of the substantially higher surface scattering near the semiconductor to insulator interface. The inversion layer model from Lombardi [55] is best suited as it includes the transverse field, doping dependent and temperature dependent parts of the mobility and can be written by three components that are combined using Matthiessen's rule [22].

$$\mu_T^{-1} = \mu_{ac}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1}$$

The three components are total mobility (μ_T) limited by Scattering with acoustic phonons (μ_{ac}), Surface roughness factor (μ_{sr}) and Scattering with optical inter-valley phonons (μ_b) [22].

2.3.2 Device Simulation Parameters

Underlap S/D doping profile (along the channel) was defined by guassian profile $N_{SD}(x) = N_O \exp(-x^2/\sigma^2)$, where N_O is the peak S/D doping, σ is the lateral straggle parameter governing S/D roll–off [22], s is the spacer width and d is the S/D doping gradient at the gate edge.

2.4 DG MOSFET Performance

Undoped Double Gate (DG) MOSFET (fig. 2.2*a*), a promising structure for scaling at the end of ITRS roadmap [1]. While operating in the weak inversion region maximizes the speed per watt or precision per watt along with the least power consumption for a given bandwidth–SNR product, these performance gains are only realized at the expense of increased sensitivity to the transistor mismatch, power supply noise, temperature and linearity [55-56]. In addition, operating in the subthreshold

region also causes degradation in the cut-off frequency (f_T) due to increased parasitics [56]. The above trade-offs become even more severe when analog/RF devices are scaled down [57].

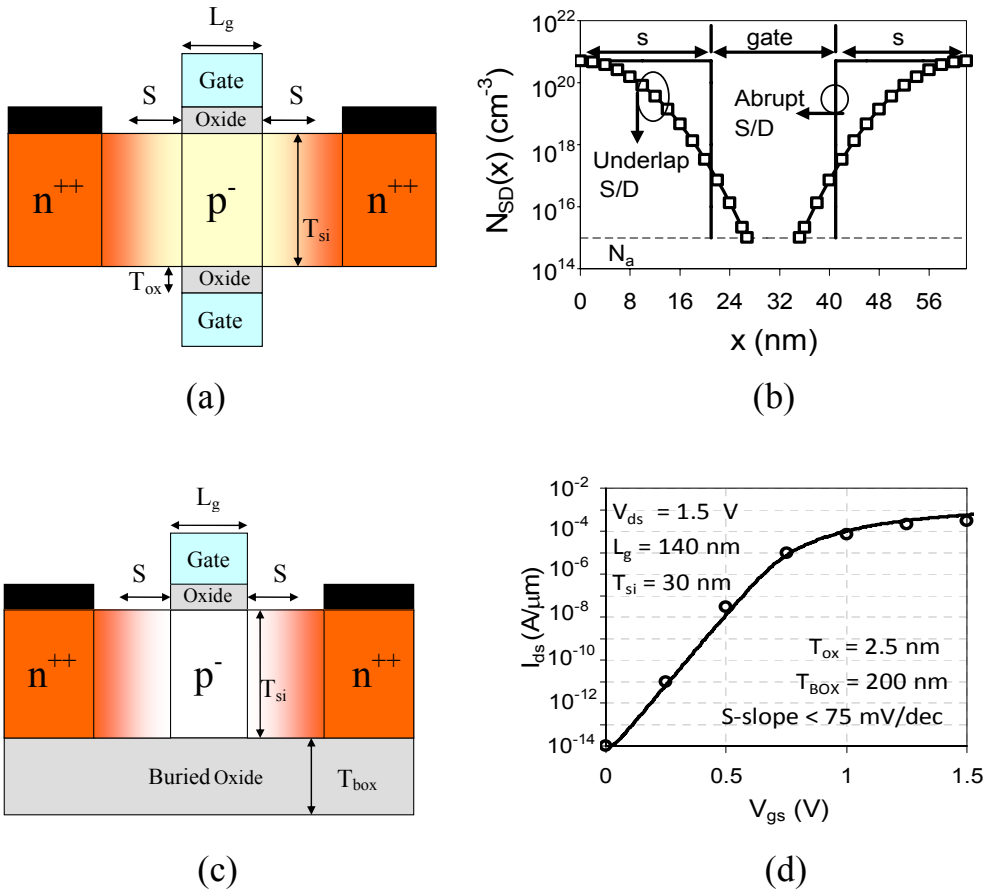

Fig. 2.1 (a) Schematic diagram of a planar Double Gate (DG) MOSFET with underlap S/D extension regions, (b) Source/Drain doping profile along the channel direction (x) and (c) Calibration of ATLAS simulations for underlap INV MOSFET with experimental data [22]. Solid line - simulation, symbols (o o o o) indicate experimental work for underlap FDSOI nMOSFET (spacer = 20 nm) [30].

The crucial questions for low power moderately inverted analog/RF MOSFETs are:

(a) Is it possible to scale down devices without degrading analog/RF performance metrics?

(b) What is optimum drive current for low power analog/RF devices?

(c) Can improved linearity be maintained at low drive currents in nanoscale devices?

The performance of low-power MOSFETs is enhanced by adopting the underlap source/drain (S/D) profile compared to the conventional abrupt S/D topology [44-45, 58-59]. A DG FinFET CMOS with gate to source/drain underlap has shown superior speed performance even with a thick Silicon fin owing to the minimized degradation of I_{on} and well controlled SCEs and suppressed parasitic fringing capacitances [60-61]. The optimal characteristic of the underlap with a gradual source/drain lateral doping gradient may eliminate the stringent need for novel annealing process and plasma doping process, which in conventional gate to source/drain overlaps is necessary to suppress SCEs with the abrupt junction in the scaled FinFET technology [60-61]. These advantages make DG technology more feasible and manufacturable for the 32-nm technology and beyond [61]. We investigate $g_m f_T/I_{ds}$, g_m^2/I_{ds} as the low power ($V_{ds} < 1$ V) performance metric [35] and *VIP*3 as the linearity metric [35] and focus on these figures of merit for moderately inverted CMOS analog/RF circuits. It is shown in the results that improved analog/RF metrics, for low-power applications, can be achieved without degrading linearity. Results also compares sensitivity of underlap and abrupt S/D MOSFETs and demonstrate that optimally designed low-power underlap MOSFETs show higher tolerance against device parameter variations.

Underlap S/D doping profile was specified by the spacer width (s) (15 and 21 nm) and the S/D doping gradient (d) (= 3 nm/decade) at the gate edge [58]. FinFETs designed with lower σ value perform worse than those with abrupt SDE regions as lower σ value with higher d value (at a given s) result in a shorter L_{eff} (enhanced SCEs) and degrade the performance [33, 58]. Please note that these larger values of σ can be obtained either by increasing d at a constant s or by increasing s for a fixed d. The first case is undesirable as it would result in shorter L_{eff} (significant SCEs). The second condition is feasible as it yields longer L_{eff} (reduced SCEs). In this paper, larger σ values refer to second condition, i.e., increasing s at a constant d to obtain the higher σ values [58]. In underlap profile, S/D doping at gate edge is lower than the peak S/D doping. As shown in fig. 2.1 *b*, spacer width is defined as the distance from the gate edge to the starting of roll–off of S/D profile. A physical effect not considered in this work is the inversion layer quantum effect, which tends to shift the peak electron concentration away from the SiO_2 interface toward the centre of the silicon film. This shift in electron

concentration is strongly dependent on how strongly the surface is inverted. Recent results by Taur [62] and Shoji [63] *et al.*, have shown that for DG devices with peak electron concentration in the range of 3×10^{19} cm^{-3}, the shift in the position of peak concentration is about 1 nm from the interface (the same as in a single gate device) and two separate channels remain even in an undoped silicon film of 5 nm thickness. This essentially indicates that the bimodal picture of electron distribution in the silicon film as depicted by classical simulations is still valid for T_{si} down to 5 nm. It has been recently reported that these quantization effects do not affect the performance of DG devices as much as traditional MOS or single gate FDSOI, due to the unique volume inversion property of the undoped DG structure [64-66].

It should be noted that the focus of our work is the moderate inversion region with current levels between 20 to 60 μA/μm. Constant current is chosen for comparison of analog/RF performance of MOSFETs, instead of the gate overdrive voltage since majority of the analog circuits are normally biased with the fixed drain currents. At these current levels, the tunneling through the gate oxide is not expected to be significant. In DG MOSFETs, the electric field near the bottom of the inversion layer is reduced. This reduces the depth of the potential well, lowers the bound state energy and broadens the inversion charge distribution, thus resulting in a lower tunneling probability [67]. Results have shown that the gate current in a DG MOSFET (non–underlap) can be reduced by four times in comparison to a bulk device at a constant inversion charge density [67]. Tunneling may occur not only in the channel region, but also in the regions where gate overlaps the S/D extension region. For long channel devices [68], the gate-to-channel current will be significant. However, in short channel devices, the gate-to-S/D overlap tunneling component will dominate. As underlap devices do not have the gate–S/D overlap, the contribution of the tunneling current is considerably reduced.

2.5 Low Power Analog/RF Performance

Considering the fundamental trade–off between the "transconductance efficiency" and the self–loaded bandwidth of a transistor, MOSFET should be operated such that bandwidth objectives are achieved while corresponding to maximum transconductance–to–current ratio (g_m/I_{ds}) [35]. This can be considered if the product of transconductance to current ratio (g_m/I_{ds}) and cut–off frequency (f_T) is plotted with drain current (I_{ds}). Figure 2.2*a–b* shows the dependence of $g_m f_T/I_{ds}$ on drain current (I_{ds}) for underlap S/D and non–underlap (abrupt) S/D MOSFETs. The device parameters used in this work correspond to RF and analog mixed-signal CMOS technology requirements for 28 nm technology node [22, 55]. The "sweet spot" corresponding to moderate inversion region [35], highlighting the range of optimum current values (I_{ds} ~ 30 – 50 μA/μm) as a compromise between bandwidth and gain, is clearly evident for all devices. Underlap S/D design results in an impressive improvement in ($g_m f_T/I_{ds}$) of ×2.8 and ×2.4 for T_{si} = 10 nm and 7 nm, respectively.

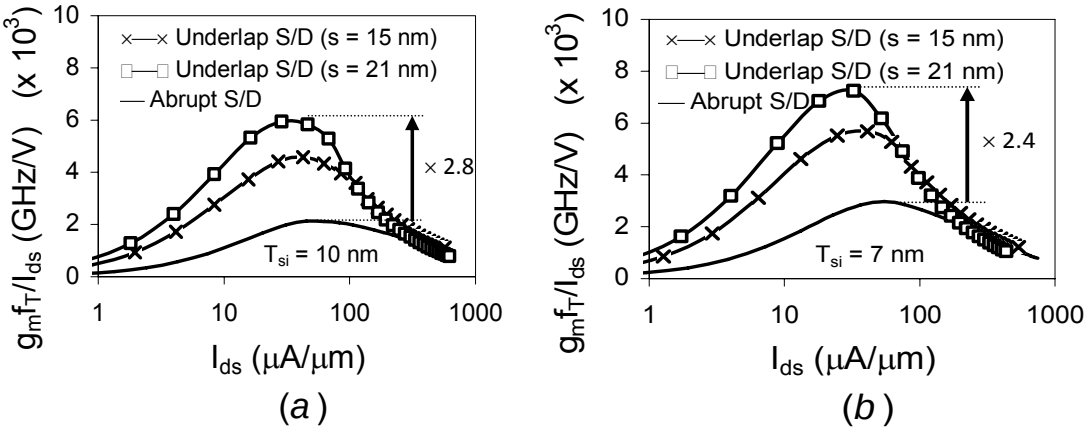

Fig. 2.2 Dependence of $g_m f_T/I_{ds}$ on I_{ds} in abrupt and underlap S/D DG MOSFETs for (a) T_{si} = 10 nm and (b) T_{si} = 7 nm. Parameters: L_g = 20 nm, T_{ox} = 1.1 nm, V_{ds} = 0.95 V.

The improvement in $g_m f_T/I_{ds}$ in underlap S/D design is due to enhanced gate controllability and reduced parasitic capacitance [33, 58]. As $g_m f_T/I_{ds}$ represents a basic challenge of achieving a good balance between bandwidth and power efficiency, higher values of $g_m f_T/I_{ds}$ indicate improved f_T at the same g_m/I_{ds} (or dc gain) or even improvement in both parameters. Comparing Fig. 2.2*a* with Fig. 2.2*b* for abrupt S/D junctions, a reduction in T_{si}/L_g from 0.5 to 0.35 lowers I_{ds} values from 30 μA/μm to 12

μA/μm to achieve $g_m f_T/I_{ds}$ = 2000 GHz/V. The underlap S/D design with T_{si}/L_g = 0.35 results in a further reduction in I_{ds} to 2 μA/μm to achieve the same $g_m f_T/I_{ds}$ value. Underlap S/D architecture with s = 21 nm (T_{si}/L_g = 0.35) achieves impressive f_T and g_m/I_{ds} values of 170 GHz and 30 V^{-1}, respectively, at I_{ds} = 10 μA/μm. These values are substantially higher than f_T = 70 GHz and g_m/I_{ds} = 24 V^{-1} achieved by abrupt S/D design for the same I_{ds}. Underlap S/D design at low I_{ds} values (~ 10 μA/μm) achieves approximately 3 times higher $g_m f_T/I_{ds}$ values. When porting an analog function with a fixed bandwidth requirement in next technology generation, MOSFETs shall be biased at lower I_{ds} to achieve the desired f_T. It is worth mentioning that in MOSFETs, peak f_T is usually obtained at I_{ds} ~ 300 μA/μm [69] whereas the peak $g_m f_T/I_{ds}$ corresponding to energy efficient and low power design is obtained at a current level nearly 5 times lower than that corresponding to peak f_T. The operation at lower I_{ds} is useful if SCEs are suppressed and parasitic capacitances reduced. As underlap S/D delivers on both these attributes it is one of the most promising technologically feasible design options for low–power RFICs [5].

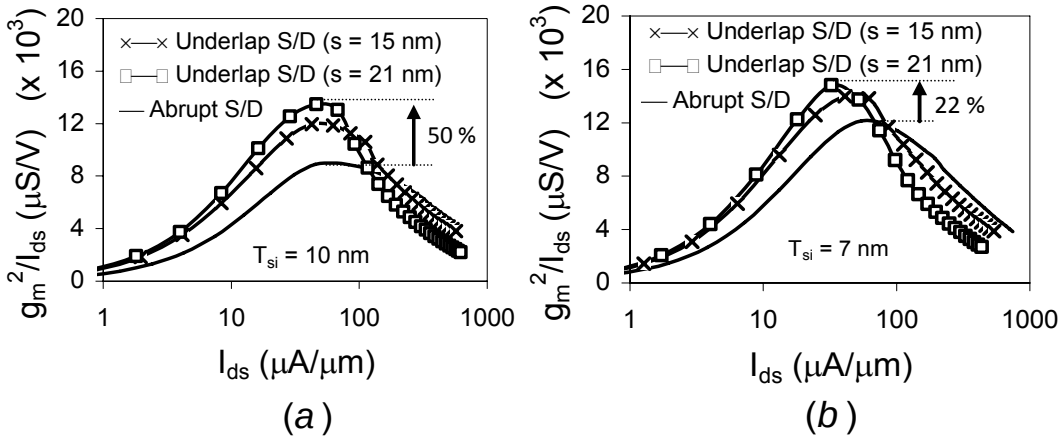

Fig. 2.3 Dependence of g_m^2/I_{ds} on I_{ds} in abrupt and underlap S/D DG MOSFETs for (a) T_{si} = 10 nm and (b) T_{si} = 7 nm. Parameters: L_g = 20 nm, T_{ox} = 1.1 nm, V_{ds} = 0.95 V. Notations are same as in figures 2.3 and 2.2.

As shown in Figure 2.3*a–b*, the product of g_m and g_m/I_{ds} i.e. g_m^2/I_{ds} also exhibits a sweet spot in the moderate inversion region for different film thickness (T_{si}) values and S/D topologies. g_m^2/I_{ds} represents a unified FoM considering signal gain, noise

figure, and power consumption of a Low Noise Amplifier [70]. Underlap S/D design with s = 21 nm results in a substantial improvement of ~ 50% for T_{si} = 10 nm and ~ 22% for T_{si} = 7 nm devices. The improvement in g_m^2/I_{ds} is due to the suppression of SCEs due to underlap S/D profile [33, 58]. A broader I_{ds} range is also available in underlap S/D MOSFETs to achieve higher g_m^2/I_{ds} as compared to abrupt S/D devices. A reduction in T_{si}/L_g in abrupt S/D devices from 0.5 (Fig. 2.3*a*) to 0.35 (Fig. 2.3*b*) lowers I_{ds} value from 60 μA/μm to 20 μA/μm to achieve g_m^2/I_{ds} = 9000 μS/V. The further reduction in I_{ds} to 10 μA/μm for the same g_m^2/I_{ds} value in underlap S/D devices (s = 21 nm) with T_{si}/L_g = 0.35 demonstrate the enormous potential of underlap S/D MOSFETs for low–power RFICs. The $(g_m^2/I_{ds})_{max}$ values are obtained at nearly the same current values corresponding to $(g_m f_T/I_{ds})_{max}$. While the trade–off between bandwidth, power efficiency, noise figure can be complex and depends on circuit architecture, it can be linked and improved by addressing the fundamental transistor attributes.

While biasing the device at peak value of–$g_m f_T/I_{ds}$ and g_m^2/I_{ds} greatly helps in lowering power for applications that do not demand an extremely high bandwidth, it may come with a penalty in terms of linearity. The metric for linearity, VIP_3 (= $\sqrt{24\, g_{m1}/g_{m3}}$ where $g_{m1} = \partial I_{ds}/\partial V_{gs}$ and $g_{m3} = \partial^3 I_{ds}/\partial V_{gs}^3$ [5]) represents the extrapolated gate voltage amplitude at which the third-order harmonic becomes equal to the fundamental tone. As shown in Fig. 2.4*a–b*, VIP_3 degrades significantly with increase in g_m/I_{ds} i.e. decreasing I_{ds}. It will be difficult to operate short channel abrupt S/D MOSFETs in the moderate inversion region as very low values of VIP_3 are obtained. The highest linearity is observed at I_{ds} = 51 μA/μm (g_m/I_{ds} = 13 V^{-1}) for T_{si} = 10 nm in abrupt S/D devices (fig. 2.4*a*). This drain current value in abrupt S/D MOSFETs can be lowered to 46 μA/μm (g_m/I_{ds} = 16 V^{-1}) by reducing the film thickness to 7 nm (fig. 2.4*b*). Using underlap S/D design s = 21 nm, the highest linearity point is observed at I_{ds} ~ 20 μA/μm (g_m/I_{ds} ~ 23 to 26 V^{-1}) for both film thickness. These current values corresponding to $(g_m f_T/I_{ds})_{max}$ and $(g_m^2/I_{ds})_{max}$ values described in fig. 2.3 and 2.4. Our analysis of improving linearity agrees well with recent published results that have also shown the benefit of moderate inversion in the reduction in the third order intermodulation product due to a singularity in the third order non–linear terms in the

I_{ds}–V_{gs} characteristics [5] and the utilization of "sweet spots" corresponding to moderate region of operation for low current squarer transconductance amplifiers [71].

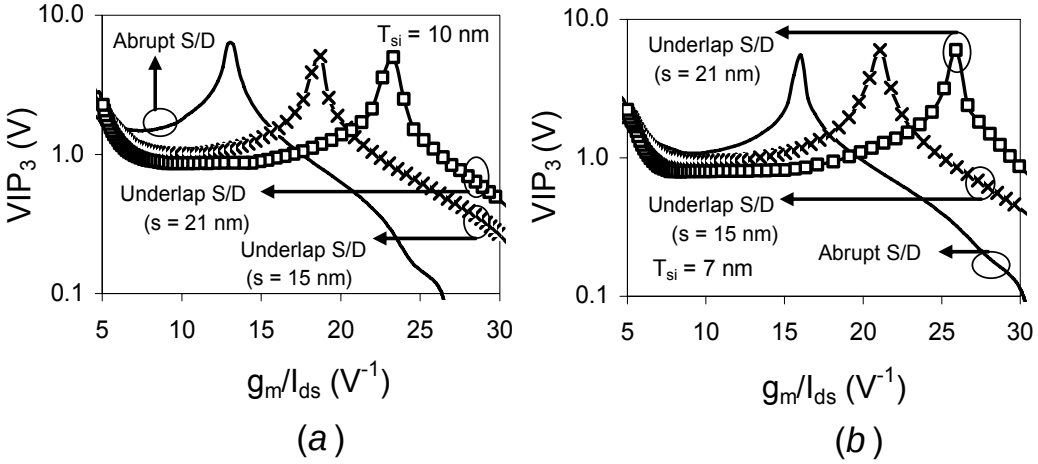

Fig. 2.4 Dependence of VIP_3 on g_m/I_{ds} in abrupt and underlap S/D DG MOSFETs for (a) T_{si} = 10 nm and (b) T_{si} = 7 nm. Notations are same as in figures 2.3 and 2.2. Parameters: L_g = 20 nm, T_{ox} = 1.1 nm, V_{ds} = 0.95 V.

Another important parameter for low power application is the current drive (I_{ds}) to achieve a particular f_T value. As shown in Table 2.1, underlap S/D devices (for both spacer widths and film thickness values) achieve f_T = 50 GHz at drive currents lower than the ITRS projection [1]. The reduction in I_{ds}, by a factor of 2, is impressive for wider spacers (s = 21 nm). Intrinsic dc gain (g_m/g_{ds}) is another crucial parameter limiting the scaling of analog devices as it degrades with gate length reduction and limits the downscaling for analog devices. To overcome this loss of gate controllability and gain, analog designers often design devices with $L_g = 5\ L_{\text{min digital}}$ [1] . Considering a longer gate length abrupt S/D device (= 55 nm) as per the ITRS ($L_{\text{minimum, digital}}$ = 11 nm) recommendation, g_m/g_{ds} values in the range of 35 to 39 dB are achieved at a gate overdrive ($V_{go} = V_{gs} - V_{th}$) of 200 mV. As underlap MOSFETs are beneficial for low power applications, nearly similar values of voltage gain can be obtained at shorter gate lengths (L_g = 20 nm), lower current drives of 2 to 4 μA/μm and lower f_T values (50 GHz). Underlap S/D achieve higher g_m/g_{ds} values (as compared to abrupt S/D devices) at lower I_{ds} values (@ f_T = 50 GHz) without having to use longer gate lengths as suggested by ITRS.

Device	s (nm)	L_g (nm)	T_{si} (nm)	I_{ds} (μA/μm) @ f_T = 50 GHz	g_m/g_{ds} (dB)	V_{ds} for g_m/g_{ds} (V)	f_T (GHz)	g_m/I_{ds} for f_T (V^{-1})
Abrupt	–	20	7	7.2	26.41	V_{dd}	50	25
			10	8.4	20.51			21
		55	7	–	39.89	$V_{dd}/2$ V_{go} = 0. 2 V	151 (I_{ds} = 250 μA/μm)	5
			10		35.45		148 (I_{ds} = 265 μA/μm)	
Underlap	15	20	7	2.9	36.30	V_{dd}	50	33
	21			1.7	39.84			34
	15		10	4.1	30.11			30
	21			2.5	34.10			31
ITRS target	–	20	–	5.0	29.50	$V_{ds} = V_{dd}$, V_{go} = 0.2 V		

Table 2.1: Comparison of current levels (I_{ds}), cut–off frequency (f_T) and intrinsic voltage gain (g_m/g_{ds}) values achieved by abrupt S/D and underlap S/D devices. Parameters: T_{ox} = 1.1 nm, V_{dd} = 0.95 V and Φ_m = 4.67 eV. ITRS target for g_m/g_{ds} is extracted at a gate overdrive V_{go} = (V_{gs} – V_{th} = 200 mV) and gate length to be 5 × minimum gate length for digital applications.

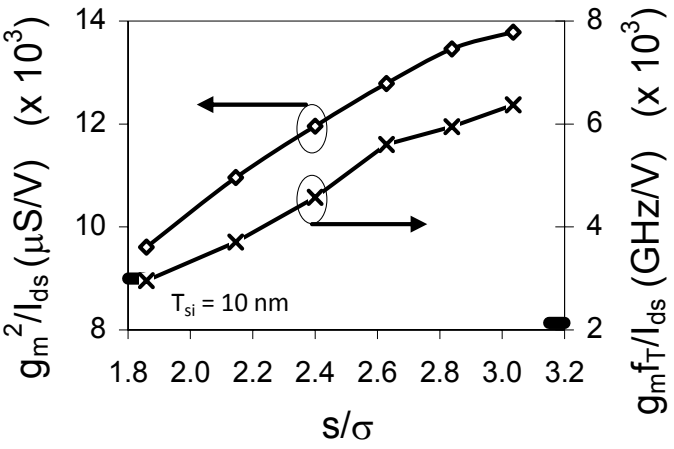

Fig. 2.5 Dependence of peak–$g_m f_T/I_{ds}$ and peak–g_m^2/I_{ds} for underlap DG MOSFETs as a function of s/σ for T_{si} = 10 nm. Parameters: L_g = 20 nm, T_{ox} = 1.1 nm, V_{ds} = 0.95 V. The markers on the y–axis indicate the values of $g_m f_T/I_{ds}$ and g_m^2/I_{ds} for abrupt S/D devices.

Figure 2.5 shows the dependence of $(g_m f_T/I_{ds})_{max}$ and $(g_m^2/I_{ds})_{max}$ on spacer–to–straggle ratio (s/σ). The optimum value of underlap region parameters in terms of maximizing both $g_m f_T/I_{ds}$ and g_m^2/I_{ds} is approximately 3. The corresponding values of abrupt S/D devices are also plotted as horizontal line on the y–axis for comparison. Nearly 50% improvement can be achieved in g_m^2/I_{ds} and 3 times higher values are observed for $g_m f_T/I_{ds}$ when compared with abrupt S/D devices. In general, low power circuits must be operated at value of f_T which is at least a factor of least five times below that of the peak–f_T (observed at 300 μA/μm [69]) in a conventional abrupt S/D MOSFET as operating too close to f_T increases amplifier input–referred noise due to current and voltage gain reductions and leads to the need to account for noise correlations in transistors via gate noise [69]. Since the current levels are relatively small in the subthreshold region, resistive drops due to parasitics that degrade g_m are minimized. Considering an abrupt S/D MOSFET (L_g = 20 nm, T_{si} = 10 nm, T_{ox} = 1.1 nm, $(f_T)_{max}$ = 300 GHz), f_T = 60 GHz (= $(f_T)_{max}/5$) is obtained at I_{ds} = 12 μA/μm. Evaluating f_T at same current in underlap devices with s/σ = 3 yields f_T = 190 GHz which is nearly 3 times higher than that achieved by abrupt device (60 GHz) in moderate inversion region.

2.6 Optimum Underlap Design and Technological Constraints

As mentioned above, underlap design with $s/\sigma = 3$ appears to be optimal in achieving an impressive improvement in $g_m f_T/I_{ds}$ and g_m^2/I_{ds} without degrading linearity (VIP_3). As the optimal s/σ value $(s/\sigma)_{optimal}$ can be achieved for various combinations spacer widths and doping gradients, the technological and performance constraints can be carefully understood and evaluated through figure 2.6 that shows dependence of s/σ on d for various spacer widths.

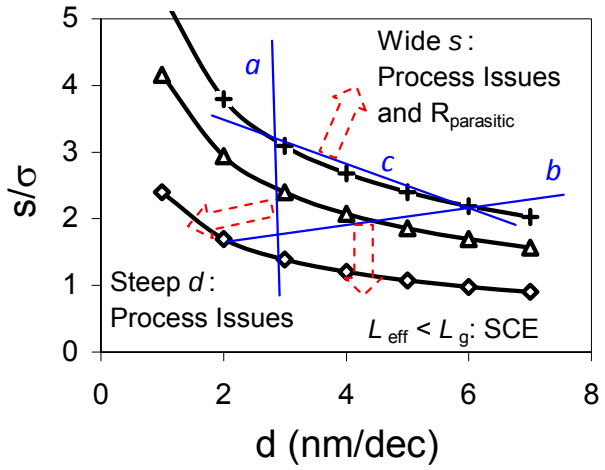

Fig. 2.6 Dependence of s/σ on doping gradient (d) for various values of spacer widths (s). Notations: +—+—+: s = 25 nm, Δ—Δ—Δ: s = 15 nm and ◊—◊—◊: s = 5 nm.

The $(s/\sigma)_{optimal}$ of 3 can be achieved (in theory) by reducing d (1 to 2 nm/decade). Physically, these d values correspond to very steep S/D doping profiles. Although ITRS [1] projected the doping gradient to be scaled in proportion to gate length (L_g) by a factor of 0.1, it will be increasing difficult to do so due to process constraints and it would require development of costly annealing techniques. Therefore, d values to the left of line a, in fig. 2.6, denote very steep doping profiles which correspond to $d < 3$ nm/decade and are very difficult to achieve. The other extreme on the doping gradient is represented by the condition of effective channel length (L_{eff}) [33-34] being comparable or shorter than L_g. Such cases, represented by s/σ values lying below the curve b, correspond to a very gradual S/D profile for shorter spacers that result in overlap gate–source/drain design (S/D doping at the gate edge is nearly same

as the peak–S/D doping) and negate the advantage of underlap S/D architecture. For a realistic S/D doping gradient of 3 to 5, wider spacer widths greater than $1.2L_g$ may also yield $s/\sigma > 3$. In such cases, wide spacer region shall contribute to the series resistance even at lower current levels and peak values of $g_m f_T/I_{ds}$ and g_m^2/I_{ds} may reduce. In addition, larger s/σ translates into $s/L_g \geq 1.5$ and fabrication of very wide spacer may add to process complexity, s/σ values above line *c* in fig. 2.6. The optimal values of s/σ for which underlap design yields improvement in low power analog/RF performance metrics is represented by the triangle enclosed by the three lines (*a*, *b* and *c*) with the best choice of s/σ and *d* lying just below the line *c*. As *d* is determined by the thermal budget and process, it is more appropriate to change *s* in the S/D design to achieve the desired s/σ ratio lying in the triangle enclosed by lines *a*, *b* and *c*.

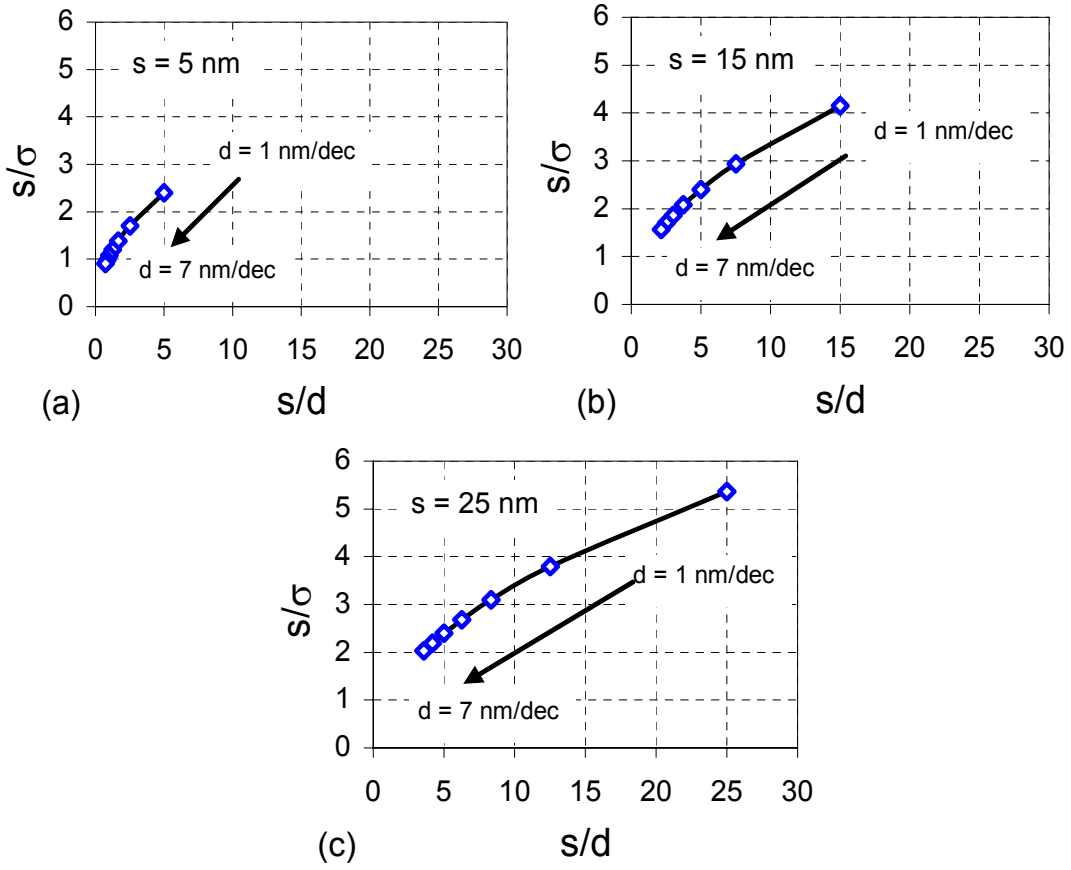

Fig. 2.7 Dependence of spacer–to–straggle ratio (s/σ) on spacer–to–gradient ratio (s/d) for (a) s = 5 nm, (b) s = 15 nm, and (c) s = 25 nm.

The optimum values of spacer widths and doing gradient, proposed in our work, is slightly different than that projected by ITRS (although not for low power analog/RF applications) [1]. ITRS suggests that the spacer width be scaled down as $0.55L_g$ and doping gradient as $0.1L_g$. The ratio of spacer width to doping gradient (s/d) as predicted by ITRS is 5.5 such that it results in a 3 decade fall of doping over the lateral extent of the junction [1]. Our projection of $s/d \cong 8$ ($s = 1.2L_g$, $d = 3$ nm/decade), specifically for low power analog/RF applications, is marginally higher that projected by ITRS and predicts 3.5 to 5 decades fall of the source/drain doping profile over the spacer and gate edge. The difference in s/d between ITRS and our underlap design is because our results are aimed to maximize $g_m f_T/I_{ds}$, g_m^2/I_{ds} and VIP_3 at lower current levels $I_{ds} \sim 30$ to 60 μA/μm, which is not the case in ITRS projections.

The optimum S/D profile can be achieved in many different ways: (i) optimizing s for a fixed d, (ii) optimizing d for a given s, and (iii) optimizing both s and d. In order to evaluate and optimize the values of s and d for optimal underlap devices, the dependence of spacer–to–straggle ratio (s/σ) on spacer–to–gradient ratio (s/d) is shown in figure 2.7*a–c*. The highest value of s/σ corresponds to underlap design with minimum value of doping gradient ($d = 1$ nm/decade) and the lowest value of s/σ for each spacer with corresponds to $d = 7$ nm/decade. The two different spacer widths analyzed in this work i.e. 15 nm and 21 nm translate into s/d of 5 and 7 and s/σ of 2.4 and 2.8, respectively, for $d = 3$ nm/decade. The relationship between s/σ and spacer to gradient (s/d) ratio was defined by Kranti *et al.* [33-34]. Hence, it will be better to fix d (generally decided by thermal budget) and optimize the spacer width. Also, S/D design with gradual doping gradients ($d = 5$ to 7 nm/decade) at shorter spacers will result in overlap architecture (S/D doping extends underneath the gate) instead of the desirable gate underlap design. Increasing the spacer width to 15 nm (fig. 2.7*b*), it is indeed possible to achieve the target s/σ of 3 but with a steep doping gradient of 2 nm/decade. All other d values (> 2 nm/decade) will either result in an underlap (3 to 5 nm/decade) or overlap ($d > 5$ nm/decade) S/D design. The underlap with $d = 3 – 4$ nm/decade at $s =$ 15 nm may give better performance as compared to abrupt S/D but it will still be below the optimal. Devices designed with $d = 5 – 7$ nm/decade with $s = 15$ nm will result in a gate overlap design as s/σ is expected to be below 2. As a steep doping profile ($d = 2$

nm/decade) is difficult to achieve, the spacer width must be increased in order to achieve the optimal s/σ. Fig. 2.7*c* shows the possible combinations in terms of s and d to achieve the optimal s/σ of 3. A doping gradient of 3 nm/decade along with spacer width of 25 nm results in the optimum combination for the desired s/σ value. Any spacer width lying between 20 and 25 nm at d = 3 nm/decade should yield a significant improvement over abrupt S/D design. Larger values of s/σ (> 3.5) tend degrade analog/RF metrics because of additional series resistance associated with very wide spacers.

2.7 Scaling

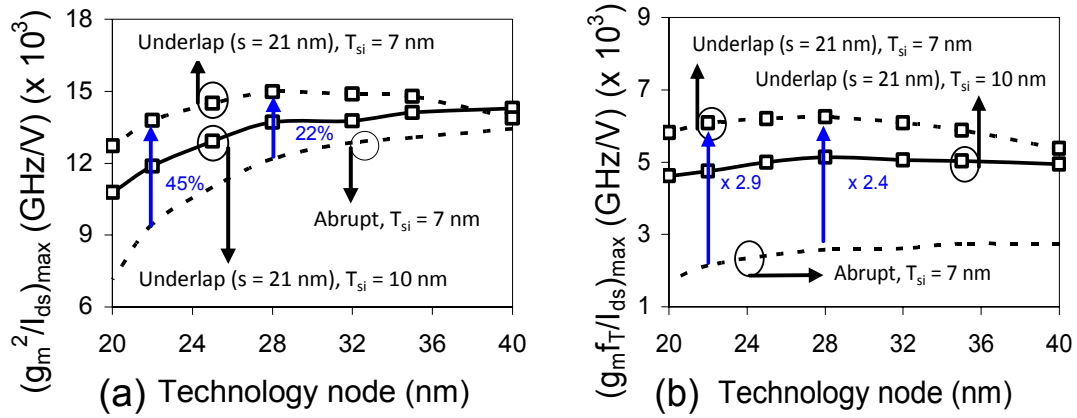

Fig. 2.8 Dependence of $(g_m^2/I_{ds})_{peak}$ and $(g_m f_T/I_{ds})_{peak}$ on technology nodes. Abrupt devices are designed with T_{si} = 7 nm to limit short channel effects whereas underlap devices with s = 21 nm ($s/L_g \sim 1$) are designed with T_{si} = 10 nm and 7 nm.

Underlap S/D design allows for the use of thicker silicon film to achieve higher values of $(g_m^2/I_{ds})_{max}$ and $(g_m f_T/I_{ds})_{max}$ as compared to abrupt S/D devices with thinner silicon films, figure 2.8*a–b*.. Even though underlap S/D design requires additional process complexity, it does ease the requirement of fabricating thin defect free silicon film for nanoscale devices. At 28 nm technology node (L_g = 20 nm, T_{ox} = 1.1 nm, V_{dd} = 0.95 V), underlap design with $s/L_g \sim 1$ results in an improvement of 22% in $(g_m^2/I_{ds})_{peak}$ and 2.4 times higher $(g_m f_T/I_{ds})_{peak}$ values as compared to abrupt S/D devices with same T_{si} value. With technology downscaling to 22 nm node (L_g = 16 nm, T_{ox} = 1.1 nm, V_{dd} =

0.8 V), the improvement in $(g_m^2/I_{ds})_{peak}$ enhances to 45% whereas $(g_m f_T/I_{ds})_{peak}$ values exhibit an increase by a factor of 2.9. At 40 nm technology node (L_g = 28 nm, T_{ox} = 1.4 nm, V_{dd} = 1 V), the peak–g_m^2/I_{ds} for underlap devices does not show appreciable change in comparison to abrupt S/D devices. However, peak–$g_m f_T/I_{ds}$ shows an improvement of 1.9 times in underlap design due to a reduction in gate capacitance.

2.8 Parameter Sensitivity

The drawback of operating in the weak/moderate inversion region (low power applications) is the increased sensitivity to device and technological parameters. The sensitivity is expected to degrade for nanoscale devices and circuits thereby limiting the use of a particular design or methodology. Underlap S/D design introduces two additional parameters i.e. spacer and doping gradient along with other already existing device parameters (L_g, T_{si}, T_{ox}) and the sensitivity to all need to be carefully evaluated. The sensitivity (S) to parameter variation can be evaluated [72] as

$$S = (\Delta Metric/Metric)/(\Delta Parameter/Parameter) \tag{2.2}$$

We investigated sensitivity to variation of structural parameters (L_g, T_{si} and T_{ox}) and underlap profile parameters (s and d) for five different performance metrics (g_m/I_{ds}, g_m, f_T, $g_m f_T/I_{ds}$ and g_m^2/I_{ds}). All devices are biased at current levels corresponding to maximum values of $g_m f_T/I_{ds}$ and g_m^2/I_{ds} (highest VIP_3) and underlap devices with T_{si} = 10 nm are designed with s = 24 nm and d = 3 nm/decade. Abrupt devices with two different film thickness values (T_{si} = 10 nm and 7 nm) are considered in the analysis. As shown in figures 2.9 and 2.10, g_m/I_{ds} appears to be the most sensitive parameter (in comparison to g_m and f_T) for all devices as the performance optimization is focussed in the moderate inversion region. Underlap devices with T_{si} = 10 nm exhibit much lower parameter sensitivity as compared to abrupt S/D MOSFETs. Even though parameter sensitivity is lowered by reducing the silicon film thickness from 10 to 7 nm, the parameter sensitivity in abrupt S/D device is still higher than underlap MOSFET.

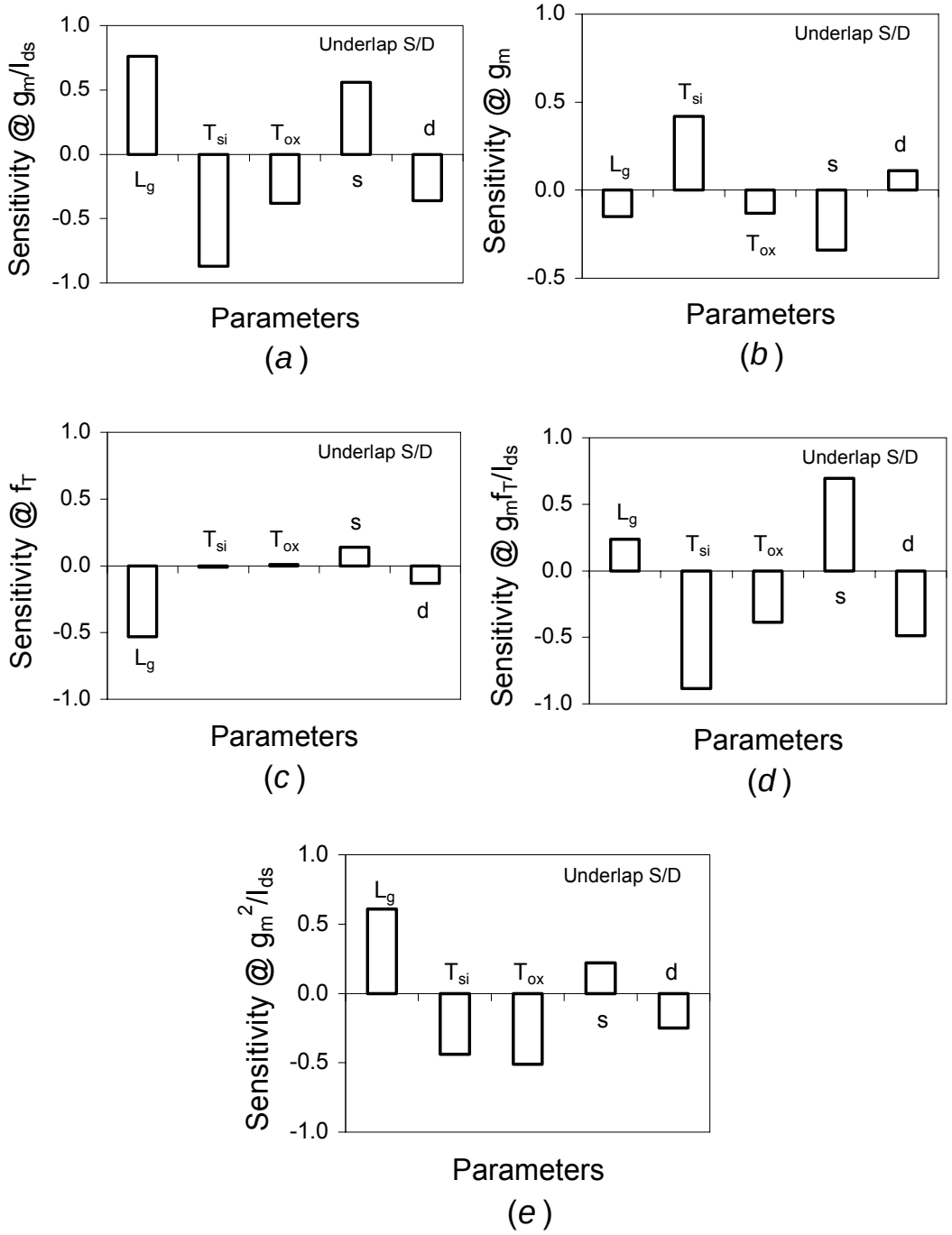

Fig. 2.9 Sensitivity analysis of underlap source/drain DG MOSFETs with T_{si} = 10 nm biased at peak–$g_m f_T/I_{ds}$ and peak–g_m^2/I_{ds} and optimum $s/\sigma = 3$ for (a) g_m/I_{ds}, (b) g_m, (c) f_T, (d) $g_m f_T/I_{ds}$ and (e) g_m^2/I_{ds}.

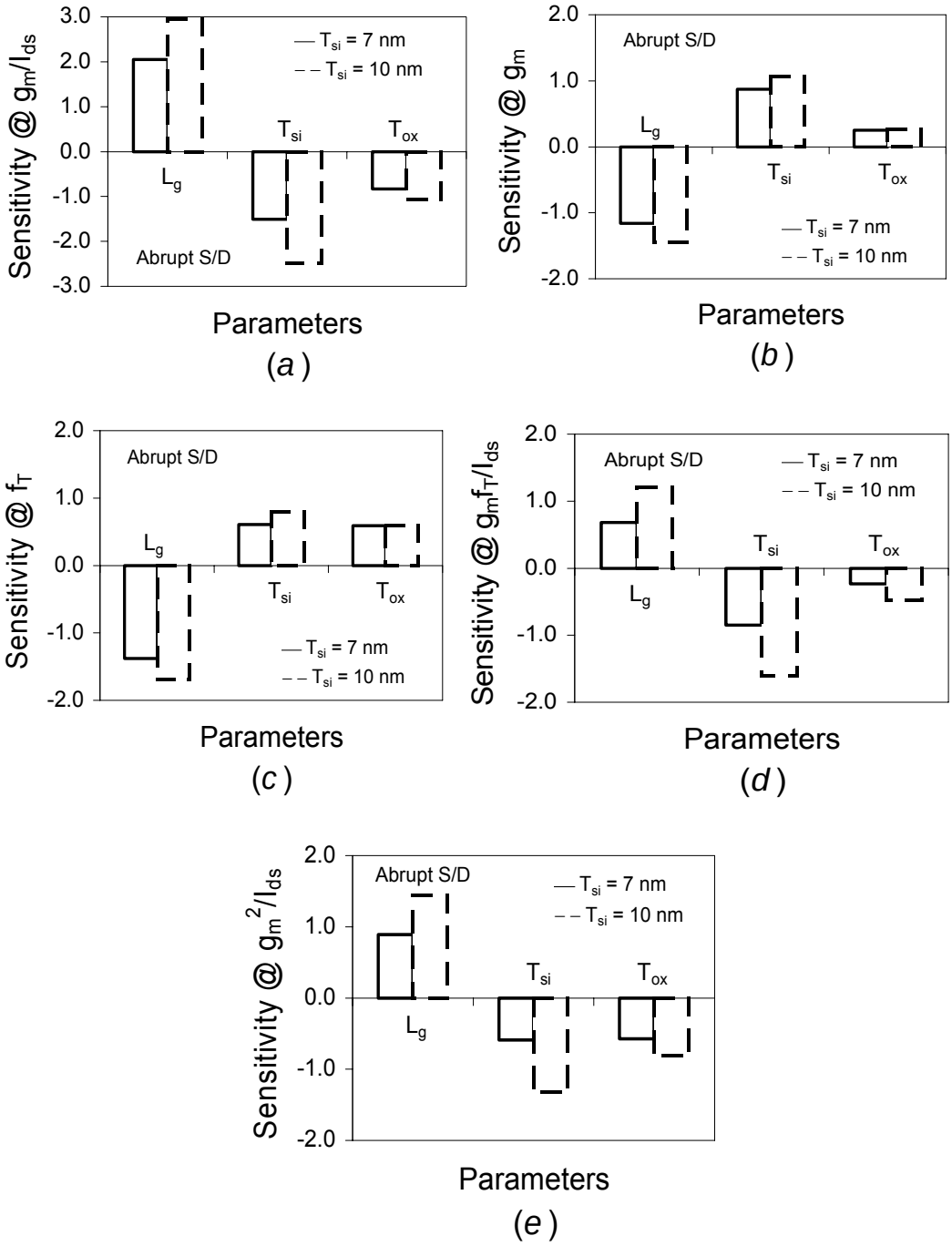

Fig. 2.10 Sensitivity analysis of two different abrupt source/drain DG MOSFETs (T_{si} = 10 and 7 nm) biased at peak–$g_m f_T/I_{ds}$ and peak–g_m^2/I_{ds} for (a) g_m/I_{ds}, (b) g_m, (c) f_T, (d) $g_m f_T/I_{ds}$ and (e) g_m^2/I_{ds}.

Increased sensitivities in $g_m f_T/I_{ds}$ and g_m^2/I_{ds} as compared to f_T and g_m are a result of higher sensitivity of g_m/I_{ds}. Abrupt S/D devices are nearly 2 times more sensitive to

parameter variation for g_m/I_{ds}. Silicon film thickness (T_{si}) is the most sensitive parameter for g_m/I_{ds}, g_m, $g_m f_T/I_{ds}$ and g_m^2/I_{ds} whereas gate length (L_g) contributes significantly to the sensitivity of g_m/I_{ds}, f_T, and g_m^2/I_{ds}. While doping gradient and spacer width contribute equal towards sensitivity of $g_m f_T/I_{ds}$ and g_m/I_{ds}. These results demonstrate that underlap S/D design does not contribute to increase in parameter sensitivity in short channel devices biased in the moderate inversion region.

2.9 Conclusions

Engineering S/D profile in nanoscale devices is expected to offer substantial benefits in the moderate inversion region, in addition to those achieved by conventional scaling methodology, for designing low–power RFICs. The advantages of underlap S/D design is presented in this chapter in significantly enhancing analog/RF FoM – g_m^2/I_{ds} and $g_m f_T/I_{ds}$ without degrading VIP_3 in moderately inverted MOSFETs. An impressive improvement of 22% in g_m^2/I_{ds} and more than twice in $g_m f_T/I_{ds}$ can be achieved by adopting optimal underlap source/drain (S/D) architecture instead of conventional abrupt S/D design. The optimal range of S/D profile parameters is identified by evaluating process and performance trade–offs associated with underlap doping profile. The length of the S/D underlap in a FDSOI and finFET device is modulated by the spacer width [30, 37]. A dual spacer process could be adopted to implement underlap channel architecture. A parameter sensitivity analysis shows that an optimally designed underlap S/D MOSFETs exhibits greater tolerance to variation of parameters as compared to conventional abrupt S/D devices.

Chapter 3

Ultra low power Junctionless MOSFETs

3.1 Introduction

Ultra Low Power (ULP) analog/RF performance of scaled MOSFETs is a major concern due to short channel effects and stringent process requirement for source/drain (S/D) regions [1]. MOSFET scaling has continued the growth of interest in finding newer and better solutions for ultra low power applications. Amongst the several challenges facing MOSFET downscaling, the loss of electrostatic integrity, increased parasitic components and abruptness of source/drain doping profile are some of the severe constraints for the development of new technologies for ultra low power RF applications [1]. The electrostatic integrity or the suppression of short channel effects (SCEs), in inversion mode devices, can be improved by the use of multiple gate devices such as Double Gate (DG) MOSFET in Silicon-on-Insulator (SOI) technology [73]. Although, DG MOSFETs can suppress SCEs and improve the electrostatic integrity, developing costly milli-second annealing techniques for nearly abrupt source/drain doping profiles and increased parasitics are unresolved technological issues hindering MOSFET scaling for ultra low power applications [1, 73]. A possible solution to the issue of abrupt steep source/drain doping profile is the use of Junctionless (JL) MOSFETs (fig. 3.1*a*) where source, channel, and drain are of the same type of doping [74]. Although JL MOSFET, require a higher gate workfunction to deplete the channel, they exhibit excellent functionality in comparison to inversion mode MOSFETs [74].

As mentioned in the previous chapter due to huge demands in microelectronic semiconductor industry for the fabrication of smaller and smaller components, transistor sizes down to the nano-scale are required for the next technology gnerations. But significant challenges in term of developing new device structures and manufacturing processes are required to continue such downscaling. An inversion-mode (INV) MOS transistor comprises two *pn* junctions called the source junction and the drain junction, the effective channel length is the distance that separates these two junctions, and the source and drain junctions are separated by a region with opposite doping type [3, 4].

The formation of such steep junctions involves extremely high doping concentration gradients, and very low thermal budget processing [74]. Flash annealing techniques are used to heat silicon for a very short time period in order to minimize diffusion, but even in total absence of diffusion, ion implantation and other doping techniques do never achieve perfectly abrupt junctions with very high concentration gradients [75]. The mobility of the carriers in a MOSFET is strongly affected by the vertical electric field [3, 4]. The universal mobility curves show that the electron mobility in the channel of a MOSFET transistor decreases as a function of the effective electric field [76]. As the dimensions of MOSFETs are scaled down, the effective oxide thickness (EOT) of the gate insulator is constantly reduced, which increases the vertical electrical field in the channel and increases carrier scattering, thereby decreasing mobility [76]. An analysis for *p*-type and *n*-type long-channel FinFET devices L_g = 10 μm reported [77] that the maximum effective mobility increases with the reduction of silicon fin-width (W_{fin}) exceeding the bulk mobility in the devices by about 9-10% [77]. This phenomenon was attributed to the reduction in the Coulomb scattering which is the dominant scattering mechanism for heavily doped junctionless devices, probably due to the occurrence of screening effect [77, 78].

The full dielectric isolation offered by the SOI structure allows one to use Accumulation-Mode (AM) devices, in which the channel region has the same doping polarity as the source and drain. N-channel accumulation-mode devices have an N^+NN^+ structure for the source, channel and drain region, respectively [75]. The junctionless devices studied by Colinge *et al.* [75] are basically accumulation mode transistors with high channel doping concentration. Accumulation mode devices made in relatively thick silicon films (thicker than 20 nm, typically) exhibit degraded short-channel effects than inversion-mode transistors because the channel is located deeper in the SOI film, and thus further from the gate electrode. This detrimental effect, however, disappears when the silicon film is very thin. In Multiple-Gate MOSFETs with a small enough cross section, there is no difference in short-channel effects between accumulation mode and inversion mode devices [75]. Since the doping type and concentration in the channel region of a junctionless transistor is equal to that in the source and drain, or at least to that in the source and drain extensions, these devices do not have any source or

drain junctions. Even though the electrical characteristics of the JL transistor are similar to those of a INV MOSFET, there is a fundamental difference between the two devices. Inversion-mode, even in their multigate design, are normally-off devices, as the drain junction is reverse biased and current flow is blocked if no channel is created between source and drain [75].

Since the electric field from the gate attracts inversion carriers, the presence of a high electric field in the channel is inherent to the operation of INV MOSFETs. In accumulation-mode transistors, an accumulation channel is formed beneath the gate insulator because the carriers are attracted by the electric field of the gate. As a result; accumulation mode transistors suffer from the same field-induced mobility degradation as inversion mode devices [75]. The junctionless transistor is basically a normally-on device where the work function difference between the gate electrode and the silicon nanowire shifts flatband voltage and threshold voltage [6]. In other words, the electric field from the gate is used to deplete the device and turn it off. When the device is on, carriers flow from source to drain in a "channel" of neutral silicon, in which there is no electric field perpendicular to current flow. In the inversion-mode device, the majority of the inversion carriers, and in particular the points of peak electron concentration, are located in high electric field regions [79]. Accumulation mode devices show results that are basically identical to those of inversion-mode devices [75]. In the junctionless transistors, on the other hand, the peak electron concentration coincides with the region of lowest electric field. This offers an obvious advantage to junctionless transistors in terms of current drive [79].

A simulation based study demonstrated that the JL bulk FinFET has a higher I_{on}/I_{off} current ratio and better short channel characteristics than that SOI JL FinFET [80]. Experiments also show that JL devices have reduced gate control and degraded short-channel characteristics relative to INV devices when benchmarked at matched I_{off} [81]. On the other hand, DG planar transistor is expected to be potential architecture for nanometer analog/RF devices due to relatively lower extrinsic parasitic capacitances than 3D finFETs [82-83]. Most of the recent research work on INV and JL devices have focused on digital applications [74-75, 81-87], and very few results are available for RF applications [88-91]. The impact of spacer length/width optimization on the low power

analog/RF performance metrics of silicon DG and nanowire inversion-mode MOSFETs have been reported earlier [89-91].

However, impact of reduced channel doping and spacer width engineering on the low power analog/RF performance metrics, analog sweet spot and parasitic capacitances have not been reported earlier for JL devices. Junctionless MOSFETs with high-κ spacers show a reduced OFF-state leakage current [92-93]. Gundapaneni *et al.* [92] demonstrated that the high-κ spacers improve the electrostatic integrity of junctionless transistors at sub-22-nm gate lengths. Electric field that fringes through the high-κ spacer to the device layer on either sides of the gate results in an effective increase in electrical gate length in the OFF-state [92]. An study comprising SOI junctionless FinFET reported device performance enhancement with high-κ spacers [93]. This necessitates the study of performance of Planar DG JL analog/RF MOSFETs with emphasis on design optimsation.

3.2 Performance of Junctionless MOSFETs

Junctionless (fig. 3.1*a*) and Inversion mode (fig. 3.1*b*) Double Gate MOSFETs, were simulated using the 2D simulator ATLAS [22] with Lombardi mobility model [55]. The doping of p-type SOI layer (N_a) of 10^{15} cm^{-3} (inversion) and n-type SOI layer (N_d) 10^{19} cm^{-3} (Junctionless), gate length (L_g) of 20 nm, gate oxide thickness (T_{ox}) = 1.7 nm and film thickness (T_{si}) of 10 nm were chosen for the analysis. The I_{ds} values (up to 30 μA/μm) correspond to weak inversion and hence quantum effects will not be significant in these devices. Fig. 3.1*c–e* shows the variation of cut–off frequency (f_T), maximum oscillation frequency (f_{MAX}) and intrinsic voltage gain (A_{VO}) with I_{ds} for JL and inversion mode devices. JL MOSFETs not only achieve improved analog/RF performance metrics but also exhibit higher values of both f_T and A_{VO}, thereby relaxing the gain–bandwidth trade–off. Junctionless MOSFETs, without the need for any channel engineering method and simpler fabrication process, achieves nearly 2 times higher values of f_T and f_{MAX} along with 65% increase in A_{VO} at I_{ds} = 10 μA/μm for low power applications.

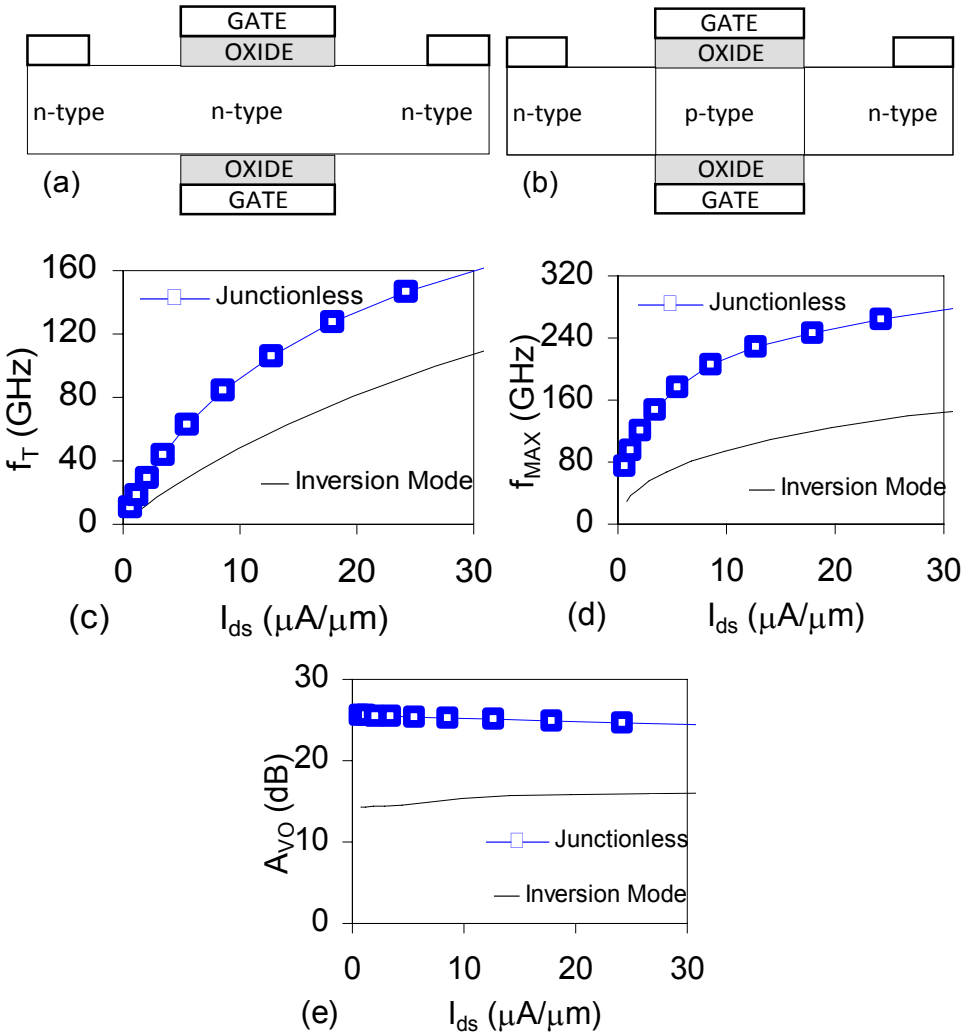

Fig. 3.1 Schematic diagram of (a) Junctionless (JL) and (b) inversion mode (non–underlap) MOSFET with abrupt S/D junctions. Dependence of (c) cut–off frequency (f_T), (d) maximum oscillation frequency (f_{MAX}) and (e) Intrinsic voltage gain (A_{VO}) on drain current (I_{ds}) in Junctionless and Inversion mode MOSFETs. Source/Drain and channel doping are same in JL devices.

In order to understand the reason for the improvement in f_T, A_{VO} and f_{MAX} for ULP JL MOSFETs, we evaluate other analog/RF metrics such as gate capacitance (C_{gg}), ratio of gate–to–source (C_{gs}) and gate–to–drain (C_{gd}) capacitances.

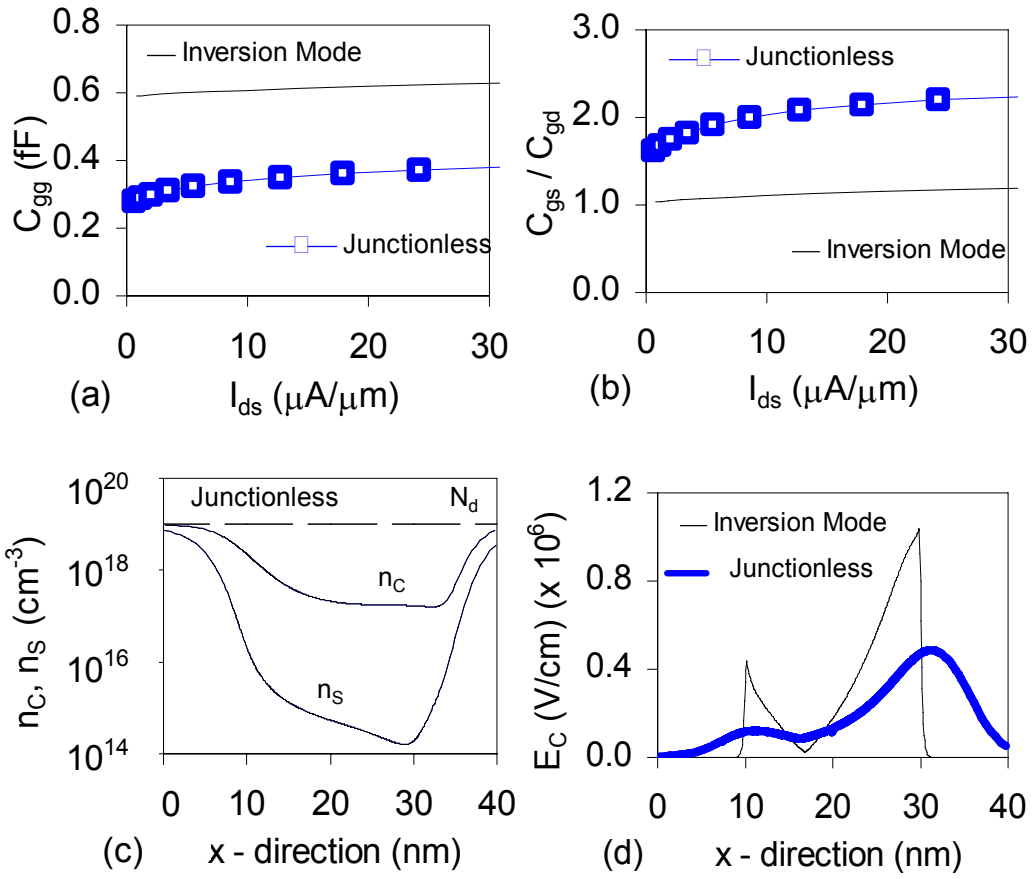

Fig. 3.2 Dependence of (a) total gate capacitance (C_{gg}), (b) the ratio of C_{gs} to C_{gd} capacitances on drain current (I_{ds}), and (c) electron concentration at surface (n_s) and centre (n_c) of the silicon on channel direction (x) and (d) Electric field at the centre of the film along the channel direction (x) at I_{ds} = 10 μA/μm. Gate is located from 10 nm to 30 nm.

The crucial challenge for weak inversion operation is the suppression of parasitics which degrade device performance. As shown in fig. 3.2*a–b*, JL MOSFET exhibits reduced C_{gg} and higher C_{gs}/C_{gd} capacitance ratio, both by a factor of ~ 2, in comparison to inversion mode devices. The ratio, C_{gs}/C_{gd}, represents the parasitic feedback capacitance and is a major limiting factor in downscaling analog/RF devices. A decrease of this ratio means a loss of channel charge control by the gate and an increase of the Miller capacitance [16]. As shown in fig. 3.2*c*, the conduction path in JL MOSFETs is located at the centre of the silicon film as the electron concentration at centre (n_c) is higher than at the surface (n_s). The electron concentration at the surface (n_s) is nearly 4 orders below the doping level (N_d = 10^{19} cm^{-3}) under the gate. In

addition, the depletion region extends beyond the gate (located from 10 nm to 30 nm) and JL devices behave as "unintentional" underlap devices. The formation of (i) conducting channel at the centre (for low drive currents) and (ii) "unintentional" underlap results in the reduction of C_{gg} and higher C_{gs}/C_{gd} ratio. The increase in A_{vo} is due to the reduction in peak electric field by 55% in comparison to inversion mode devices (fig. 3.2*d*), which reduces output conductance and increases Early voltage (V_{EA}). The electric field also extends into the depleted region beyond the gate (10 nm to 30 nm). The reduction in C_{gg} results in the improvement of f_T (= $g_m/2\pi C_{gg}$) whereas voltage gain (= $g_m/I_{ds} \times V_{EA}$) improves due to higher g_m/I_{ds} and V_{EA} values. The enhancement in f_{MAX} [16] is due to improved values of f_T, C_{gs}/C_{gd} and g_m/g_{ds}.

It had been shown in another study that, depending on gate voltage, JL devices can present both larger Early voltage and intrinsic voltage gain than inversion-mode devices of similar dimensions [94]. In addition it was shown that V_{EA} and A_{VO} are always improved in junctionless devices when the temperature is increased, whereas they present a maximum value around room temperature for inversion-mode transistors [94]. The potential to control the spacer width and lateral straggle of the doping profile can provide an additional degree of freedom alongside the aspect ratio, to design future analog devices [58]. Optimally-engineered DG MOSFETs and FinFETs have shown high tolerance to variations in gate-misalignment, spacer width and lateral straggle (roll-off of S/D profile), relaxing these crucial process control requirements in nanoscale devices [42, 58].

3.3 Comparison With Underlap Inversion Mode MOSFETs

In the previous chapter, we optimized the structure of inversion-mode MOSFETs with underlap design, while previous section has shown the enhanced performance of junctionless MOSFETs over classical inversion-mode device. In this section we compare performance between optimized underlap inversion-mode and uniformly doped junctionless device. The doping (N_d) of the *n*–type junctionless devices was taken to be 10^{19} cm^{-3} as reported earlier [83-84]. A spacer width (*s*) of 18 nm and S/D doping gradient (*d*) at the gate edge was selected to be 3 nm/decade for underlap devices. Fig. 3.3*a–d* shows the dependence of analog/RF performance metrics on drain

current. Despite high doping concentration (10^{19} cm^{-3}), JL devices at low current levels achieve transconductance (g_m) values that are nearly comparable to abrupt S/D devices (fig. 3.3 *a*). This is due the flow of conducting channel through the centre of the silicon film. g_m values are nearly same for all devices up till I_{ds} < 10 μA/μm.

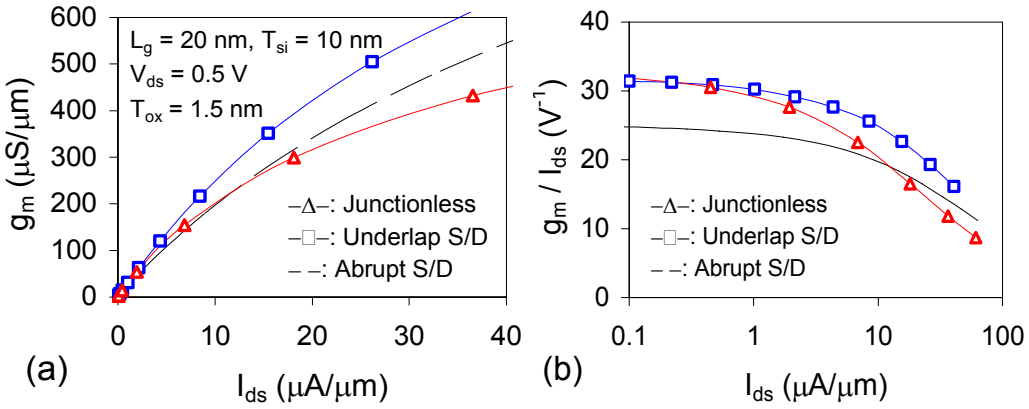

Fig. 3.3 Dependence of (a) transconductance (g_m), (b) transconductance – to – current ratio (g_m/I_{ds}), on drain current (I_{ds}) for junctionless, underlap and abrupt source/drain MOSFETs.

JL devices achieve higher transconductance–to–current (g_m/I_{ds}) ratio (30 V^{-1}) in comparison to abrupt S/D devices (25 V^{-1}) in the weak inversion region (fig. 3.3*b*). The higher peak–g_m/I_{ds} reflects on the reduction of short channel effects and a lower subthreshold slope (S = ln(10)/$(g_m/I_{ds})_{max}$) in JL MOSFETs. In moderate and strong inversion regions (g_m/I_{ds} < 10 V^{-1}), g_m/I_{ds} values degrade sharply in JL devices due the influence of source/drain resistance. As shown in fig. 3.3*c*, Early voltage (V_{EA} = I_{ds}/g_{ds}, where g_{ds} is the output conductance) is the highest for JL in comparison to abrupt S/D and underlap devices. The absence of a junction results in the reduction of the peak electric field at the drain end which reduces g_{ds} (or improves output resistance, R_{out} = $1/g_{ds}$). The combined effects of above metrics are reflected in the higher values of intrinsic voltage gain (g_m/g_{ds} = g_m/I_{ds} × V_{EA}) in JL MOSFETs. g_m/g_{ds} values in JL devices are comparable to that of underlap MOSFETs and significantly higher (≅ 60 %) than that exhibited by conventional inversion mode abrupt S/D MOSFETs (fig. 3.3*d*).

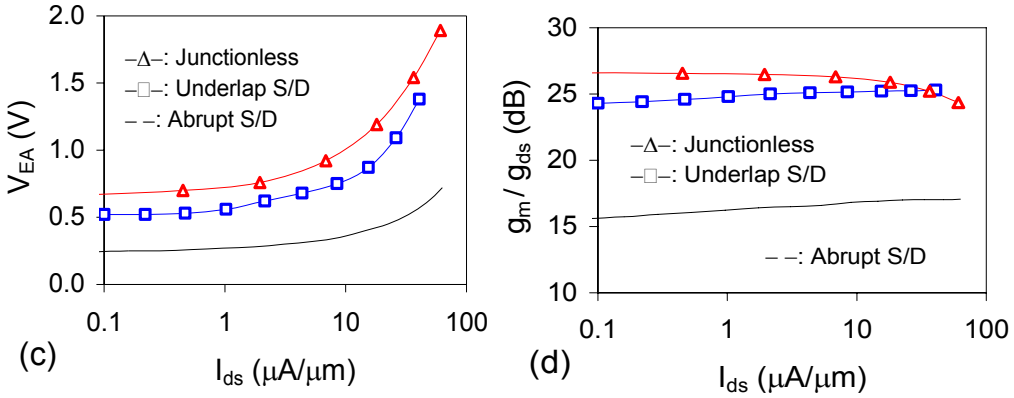

Fig. 3.3 Dependence of (c) Early voltage (V_{EA}), and (d) voltage gain (g_m/g_{ds}) on drain current (I_{ds}) for junctionless, underlap and abrupt source/drain MOSFETs.

Fig. 3.4*a–b* shows the behavior of capacitance (C_{gg}) and cut–off frequency ($f_T = g_m/2\pi C_{gg}$) for the three different device architectures. JL MOSFET exhibits the least capacitance in comparison to the other two devices. The capacitance is ~ 30 % lower than that of abrupt S/D MOSFET. The absence of *pn* junction at the gate edge allows the depletion width to extend beyond the gate (along the channel direction). This reduces the electron concentration in regions adjacent to gate edge, and lowers the inner fringing capacitance. In the subthreshold region (for low power applications), the capacitance is dominated by parasitics, and the reduction in fringing capacitance is responsible for the lower capacitance in JL devices. This reduction in fringing capacitance is comparable to that of underlap devices. The dependence of f_T on I_{ds} is shown in fig. 3.4*b*. JL MOSFETs achieve f_T values higher than abrupt S/D devices and comparable to that exhibited by underlap devices up to I_{ds} = 20 μA/μm.

As the reduction in C_{gg} dominates over the degradation in g_m (fig. 3.4*a*), JL devices exhibit higher f_T values. Beyond I_{ds} = 20 μA/μm, f_T is degraded due to series resistance effect. As JL devices have simpler fabrication process without the need for steep junctions, JL devices will be most useful for ultra–low–power applications. Another interesting aspect is that for I_{ds} < 20 μA/μm, JL devices exhibit an improvement in both voltage gain (g_m/g_{ds}) and cut–off frequency (f_T) without any need of channel engineering topology.

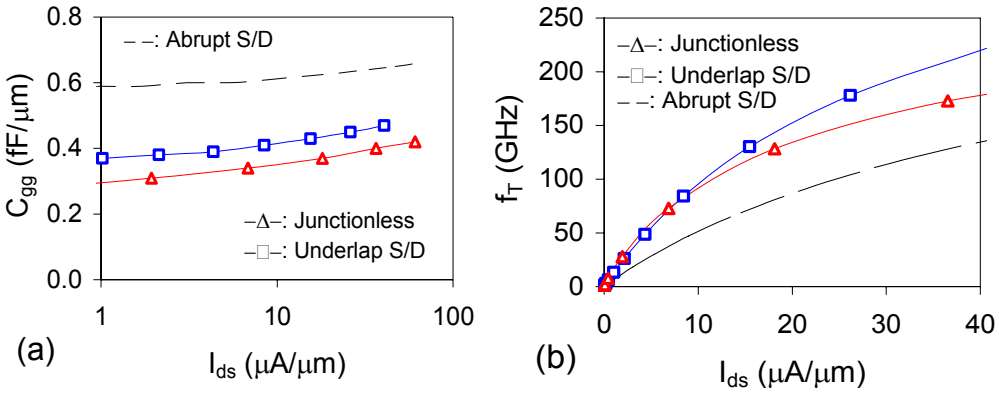

Fig. 3.4 Dependence of (a) gate capacitance (C_{gg}), and (b) cut–off frequency (f_T) on drain current (I_{ds}) for junctionless, underlap and abrupt source/drain MOSFETs.

3.4 Impact of Channel Doping on Performance

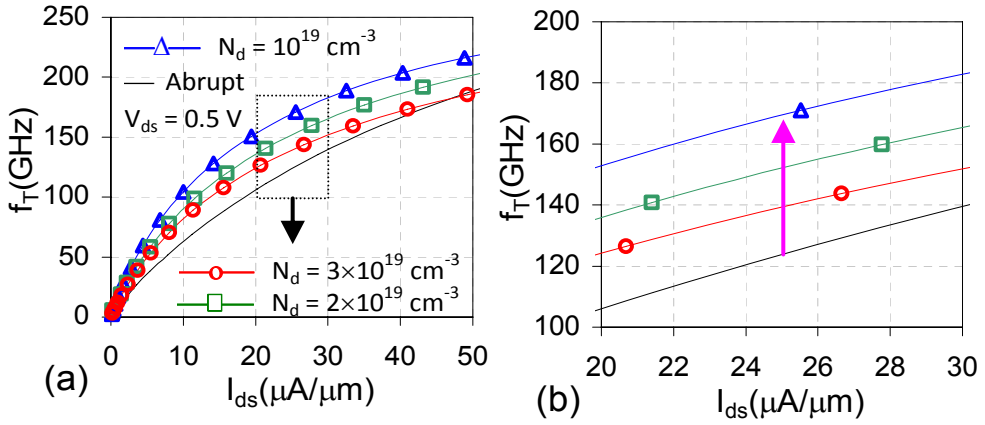

Fig. 3.5 (a) Dependence of cut-off frequency (f_T) on drain current (I_{ds}) for different devices. (b) Enlarged view of f_T corresponding to I_{ds} lying between 20 - 30 μA/μm. Notations are same as in fig. 3.5*a*.

In this section, we address the issue of channel doping in ultra low power JL MOSFETs and examine its dependence on RF performance metrics. We will also show the extracted parasitic capacitances for different doping concentrations in JL MOSFETs. Fig. 3.5*a*-*b* shows the dependence of cut-off frequency (f_T) on drain current (I_{ds}) for JL and inversion mode (INV) DG SOI MOSFETs with gate length (L_g) of 20 nm, gate oxide thickness (T_{ox}) of 1.7 nm, and film thickness (T_{si}) of 10 nm, (N_d) in the *n*–type varied from 1×10^{19} cm^{-3} to 3×10^{19} cm^{-3}. The doping of inversion mode devices (N_a) was taken to be 10^{15} cm^{-3}. As the focus of this work is for ultra low and low power

RF applications, the analysis was limited to drain current (I_{ds}) of 50 µA/µm at drain bias (V_{ds}) of 0.5 V. The values of current correspond to weak and moderate inversion regions.

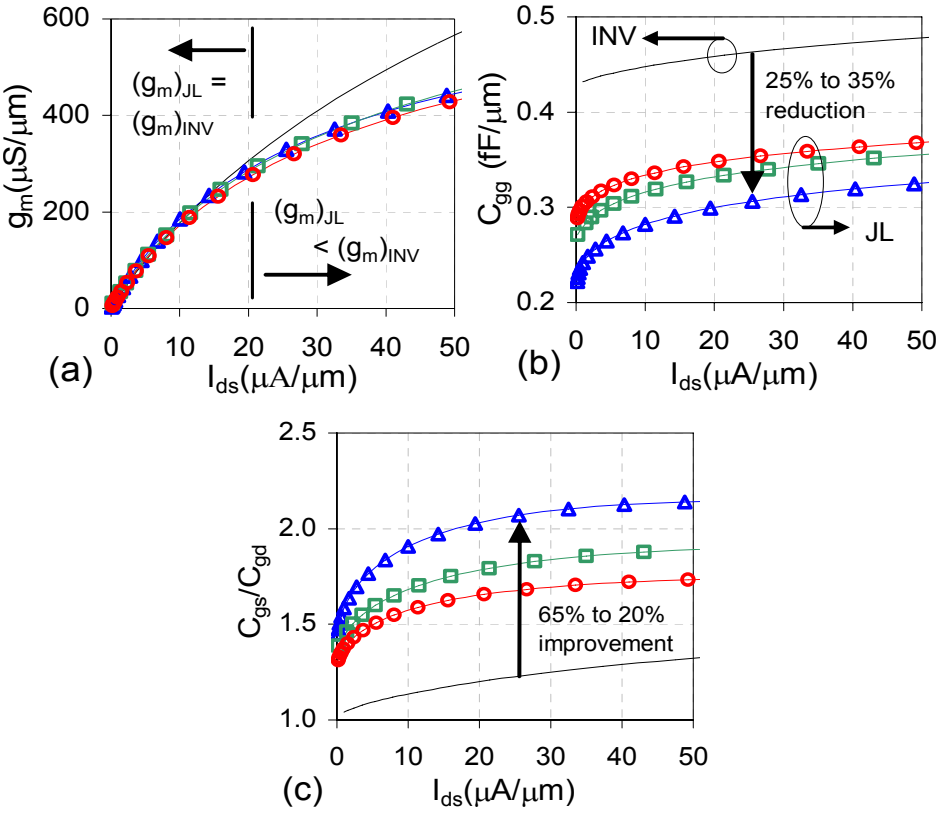

Fig. 3.6 Dependence of (a) transconductance (g_m), (b) gate capacitance (C_{gg}) and (c) ratio of gate-to-source and gate-to-drain capacitance (C_{gs}/C_{gd}) on drain current for different devices. Notations are same as in fig. 3.6 *a*.

Although, f_T reduces with increase in doping, JL transistors with different doping concentrations exhibit higher f_T values in comparison to INV devices up till I_{ds} of 50 µA/µm. This improvement in f_T at lower drain currents for JL MOSFETs is achieved even when the doping concentration (~ 10^{19} cm^{-3}) is significantly higher than that of undoped (N_a = 10^{15} cm^{-3}) INV MOSFETs. Considering the current of 25 µA/µm (fig. 3.5*b*), JL MOSFETs with N_d = 10^{19} cm^{-3} achieve nearly 40% higher f_T in comparison to INV device. The improvement is reduced to ~ 20% with an increase in doping to 3×10^{19} cm^{-3}.

The dependence of transconductance (g_m), gate capacitance (C_{gg}) and gate-to-source and gate-to-drain capacitance ratio (C_{gs}/C_{gd}) on drain current (I_{ds}) for JL and inversion mode MOSFETs is shown in fig. 3.6*a-c*. At very low current drives (≤ 20 μA/μm), JL devices achieve nearly same values of g_m as exhibited by INV MOSFETs. g_m values of JL transistors are degraded at higher current levels (> 20 μA/μm). This reduction in g_m is compensated by the reduction in the capacitance (C_{gg}) values as shown in fig. 3.6*b*. The reduction (35 %) is most significant for the JL MOSFET with $N_d = 10^{19}$ cm^{-3}. As the source/drain and channel doping is same, the depletion depth extends beyond the gate edge along the channel direction in JL devices and reduce the parasitic capacitance which is a significant portion of the total gate capacitance at lower drain currents. Junctionless transistors exhibit an increase of C_{gs}/C_{gd} ratio by 65% for $N_d = 10^{19}$ cm^{-3} (fig. 3.6*c*). The higher values reflect enhanced gate controllability i.e. suppression of SCEs due to the extension of depletion region beyond the gate edge.

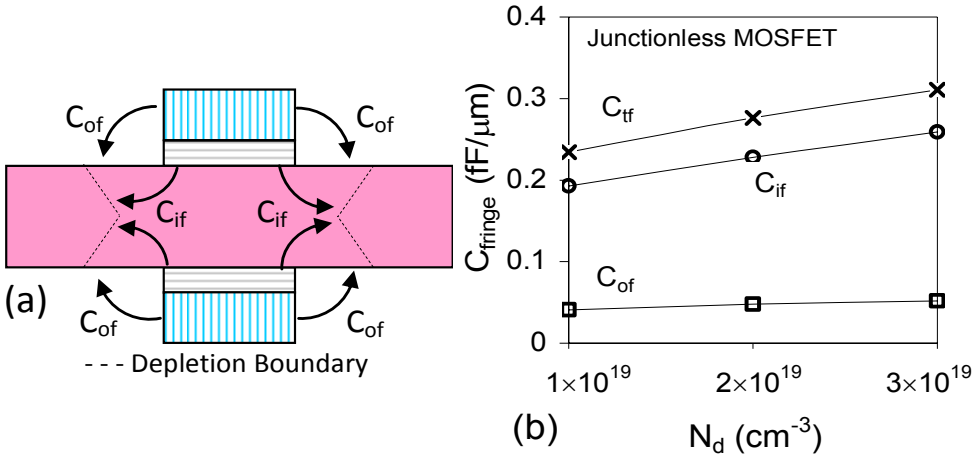

Fig. 3.7 (a) Schematic diagram showing inner (C_{if}) and outer (C_{of}) fringing capacitances in JL MOSFET. The dashed line indicates the depletion layer boundary in the off-state. (b) Dependence of fringing capacitances on doping concentration in JL MOSFETs at drain bias (V_{ds}) of 50 mV. $(C_{tf})_{INV}$ = 0.437 fF/μm.

The total gate capacitance (C_{gg}) is dominated by fringing capacitance for devices operated at low current levels [58, 59]. The extracted value of the inner (C_{if}), outer (C_{of}) and total (C_{tf}) fringing capacitance is shown in fig. 3.7*a-b*. An increase in doping concentration results in higher values of parasitic capacitance and an associated

degradation in f_T values. The dominant contribution is the inner fringing which is governed by the extension of the depletion width beyond the gate edge (fig. 3.7*a*). Compared with INV devices ($(C_{tf})_{INV}$ = 0.437 fF/μm), JL transistors achieve nearly 45% and 25% lower parasitic capacitance with N_d of 10^{19} and 3×10^{19} cm^{-3}, respectively.

3.5 Performance Optimization of Junctionless MOSFETs

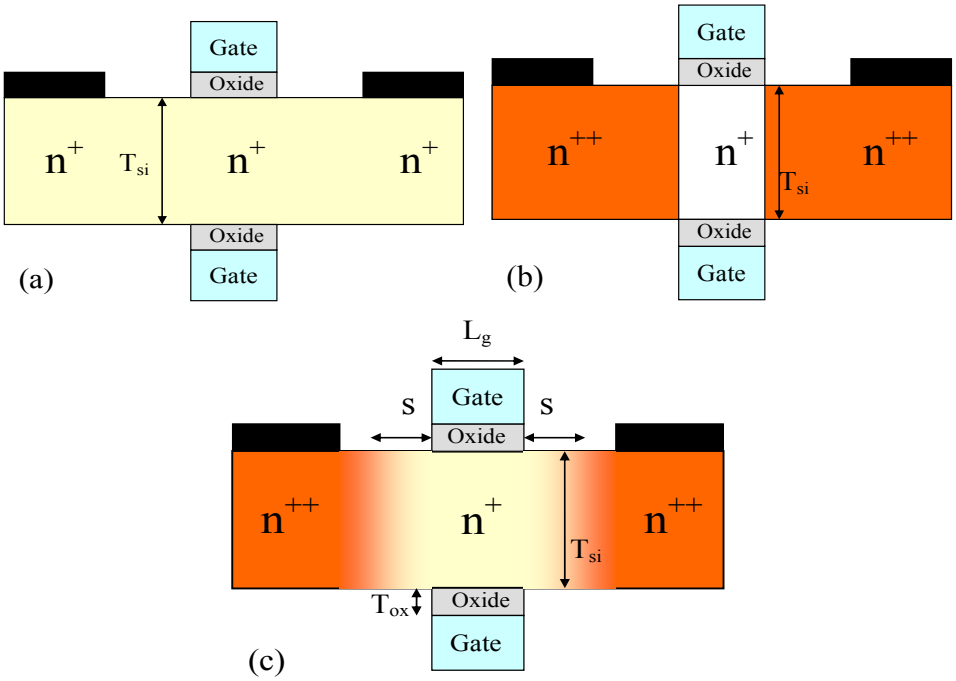

Fig. 3.8 Schematic diagram of (a) Conventional JL MOSFET (JL type-I), (b) JL transistor with highly doped S/D region (JL type-II), and (c) JL device with additional S/D doping limited from the gate edge (JL type-III).

Although a junctionless DG transistor does not have a traditional *pn* junction, it can be designed in many different topologies. The simplest being the one with same doping level in source/drain (S/D) and channel regions (fig. 3.8*a*, hereafter referred to as JL type-I topology. However, this design limits the current drive due to parasitic series resistance associated with the S/D regions. The limitation of this JL transistor topology can be overcome by using additional S/D implantation. This JL design, shown in fig. 3.8*b*, is referred to as type-II. In this structure, parasitic fringing capacitance is likely to increase as the additional S/D doping approach the gate edge. This increase in

parasitic capacitance will eventually degrade the analog/RF performance of structure. JL device can also be designed with spacer regions to restrict the peak S/D doping concentration away from the gate edge as shown in fig. 3.8*c*. This device, referred as type-III, will exhibit different performance metrics in comparison to the two previous designs (fig. 3.8*a*-*b*) as constraints related to doping and parasitic capacitance are different which govern the device performance.We evaluated the low power analog/RF performance of DG JL transistors designed in the three different topologies (fig. 3.8*a*-*c*). The performance of low power JL transistors is enhanced through the optimization of channel doping (N_d) and spacer width (s) (fig. 3.9) by applying doping gradients as design guideline. ULP Performance metrics to be evaluated are parasitic capacitances, product of transconductance efficiency and cut-off frequency ($g_m f_T/I_{ds}$) and the product of transconductance and transconductance efficiency (g_m^2/I_{ds}).

This section demonstrates the potential benefits of lowering the channel doping from 10^{19} cm^{-3} and utilizing the spacer width to improve performance and reduce parameter sensitivity. The results of optimized JL devices for low power applications are also compared with inversion mode (INV) devices. Previous studies on performance on JL MOSFETs have investigated JL devices designed with high doping concentration ($\geq 10^{19}$ cm^{-3}) [85-87]. The impact of spacer length/width optimization on the low power analog/RF performance metrics of silicon DG and nanowire inversion-mode MOSFETs have been reported earlier [89-91]. However, impact of reduced channel doping and spacer width engineering on the low power analog/RF performance metrics, analog sweet spot and parasitic capacitances have not been reported earlier for JL devices.

DG JL MOSFETs with channel doping (N_d) varying from 10^{18} cm^{-3} to 3×10^{19} cm^{-3} have been analyzed. The gate oxide thickness (T_{ox}) was fixed at 1 nm. Guassian source/drain (S/D) profile was simulated with *n*-type peak doping (N_{SD}) of 5×10^{20} cm^{-3}. Different spacer width (s) ranging from 16 nm to 30 nm with a constant doping gradient (d) of 3 nm/decade (at gate edge) was considered in the Gaussian S/D profile. The performance of JL devices has been compared with INV MOSFETs (channel doping, N_a = 10^{15} cm^{-3}) with abrupt and underlap S/D regions. Drain bias (V_{ds}) was fixed at 0.8 V for all the devices. As our focus is on low power applications, we have restricted the analysis up to a drain current (I_{ds}) of 30 μA/μm. We have included a comparison of

TCAD simulations with the experimental data (fig. 3.10) for underlap inversion mode MOSFET in previous chapter [30]. Energy quantization with gate-bias resulting from increase in sub-band energy levels and enhanced transverse electric field is expected to be an issue for DG devices designed with high doping (> 10^{18} cm^{-3}). As reported by Colinge *et al.,* [65], quantum effects are only significant for a film thickness (T_{si}) below 7 nm in a trigate MOSFET. For a device with film thickness ≥ 7 nm, subthreshold slope (*S*–*s*lope) and threshold voltage (V_{th}) remains nearly unaltered with the inclusion of quantum effects. A recent work by Duarte *et. al.* [96] confirms that the threshold voltage shift (ΔV_{th}), due to quantum confinement effects (QCEs), is not significant for film thickness greater than 7 nm in JL MOSFETs. It should be noted that QCEs are smaller in JL MOSFETs due to the electron concentration being confined to the centre of the film rather than at the surface as shown in previous section. Therefore, in our simulations we have not considered quantum effects although the impact of QCE on analog/RF performance metrics in JL transistors is studied in the last section of this work.

3.5.1 Optimised Design for Junctionless Transistor

In order to optimize JL architectures, we first compare analog/RF performance of the three different JL topologies. Most of the published results of JL transistors have suggested the use of doping of 10^{19} cm^{-3} [75, 94]. As shown in fig. 3.11*a*, cut-off frequency (f_T) of 160 GHz is achieved in JL type-I structure designed with N_d = 10^{19} cm^{-3} at a current level of 30 μA/μm. These f_T values are 20 % higher than those designed with N_d = 3x10^{19} cm^{-3} at the same current level. The increase in N_d reduces f_T due to increase in total gate capacitance C_{gg}. The increase in C_{gg} is due to reduction in unintentional underlap [75, 82, 94] effect at higher channel doping. These results clearly demonstrate that f_T increases with reduction in N_d, and further reduction in doping is necessary to improve f_T. This reduction N_d would require additional S/D implantation as the region below S/D contacts should be heavily doped in order to achieve good ohmic contacts and to reduce parasitic series resistance. Therefore, peak S/D doping (N_{SD}) and film doping (N_d) levels must be decoupled. The position of this additional S/D doping with respect to gate edge is crucial as it may result in either underlap or overlap

structure.

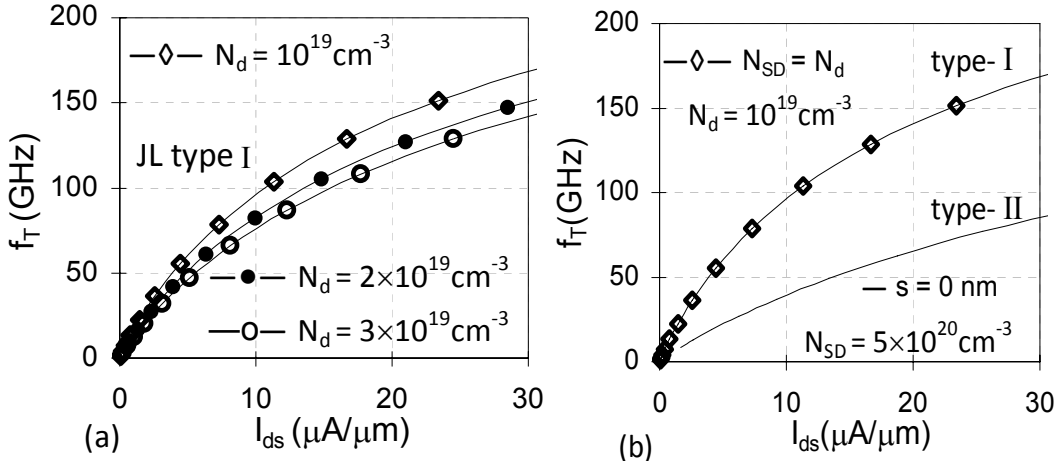

Fig. 3.9 Dependence of f_T on drain current (I_{ds}) for (a) conventional junctionless (JL) type-I device, and (b) comparison of type-I and type-II JL devices with $N_d = 10^{19}$ cm^{-3} and $N_{SD} = 5\times10^{20}$ cm^{-3}.

As shown in fig. 3.9*b*, JL type-II device with highly doped S/D region exhibits a lower f_T value in comparison to type-I JL MOSFET. Although the channel doping in this device is 10^{19} cm^{-3} but this structure exhibits high C_{gg} values due to the location of peak S/D doping (N_{SD}) being at the gate edge, resulting in a larger parasitic capacitance values which degrade the performance. In an overlap structure, the additional S/D implantation penetrates beneath the gate resulting in gate-source/drain overlap capacitance and reduced effective channel length (i.e lower than gate length), both of which result in further degradation of analog/RF performance metrics as compared to type-II topology. Hence, the overlap design is not considered in the analysis. Results in fig. 3.9*a-b* clearly indicate that JL type-II device with the same channel doping as type-I will exhibit degraded metrics. Therefore, type-II JL device will not be examined further. An "underlap" JL device (fig. 3.8 *c*) is designed such that the doping concentration at the gate edge is lower than the peak-S/D level (N_{SD}).

It should be mentioned here that in an underlap design of inversion mode (INV) devices, the doping at the gate edge is nearly 3 orders of magnitude lower than the peak S/D doping concentration as the silicon film is undoped ($N_a = 10^{15}$ cm^{-3}) [75-94]. This is not the case in JL devices as N_d varies from 10^{18} cm^{-3} to 3x10^{19} cm^{-3} and doping at the

gate edge is nearly an order or two of magnitude lower than the peak-S/D doping concentration. This shall present significant advantage of such optimized design implementation feasible in ultra low power junctionless MOSFETs. Thus manufacturability of junctionless transistor with such optimized designs will not need advanced plasma doping techniques and annealing techniques [95]. Since the value of doping gradient (*d*) depends on thermal budget and diffusivity, very small values (< 3 nm/decade) may be difficult to achieve (very small values of *d* require a nonstandard process, such as solid phase epitaxy or laser thermal annealing [95]). Therefore, it is more appropriate to increase spacer width (*s*) to achieve higher performance per device [58]. Such S/D extension region engineered devices, with wider than expected spacers, will not be useful for operation at higher current densities (> 50 μA/μm) unless the spacer is shorter than the gate length, due to the parasitic series resistance that severely degrades the device performance [58].

The variation of f_T with respect to spacer width is shown in fig. 3.10*a*. An increase in spacer width results in an increase in f_T. JL type-III device with $N_d = 10^{19}$ cm^{-3} and s = 30 nm achieves f_T values comparable to JL type-I device with $N_d = 10^{19}$ cm^{-3} (fig. 3.8*a*). In order to optimize JL device for enhanced analog/RF performance metrics, N_d is reduced to $5x10^{18}$ cm^{-3} and spacer width variation is simulated (fig. 3.10*b*) for the same spacer width variation. The reduction in doping results in a 15% higher f_T of 200 GHz at I_{ds} = 30 μA/μm s = 30 nm as compared to JL device with $N_d = 10^{19}$ cm^{-3}. As shown in fig. 3.10*c*, a further reduction of the channel doping to 10^{18} cm^{-3} yields a higher f_T of 240 GHz at a spacer width of 30 nm.

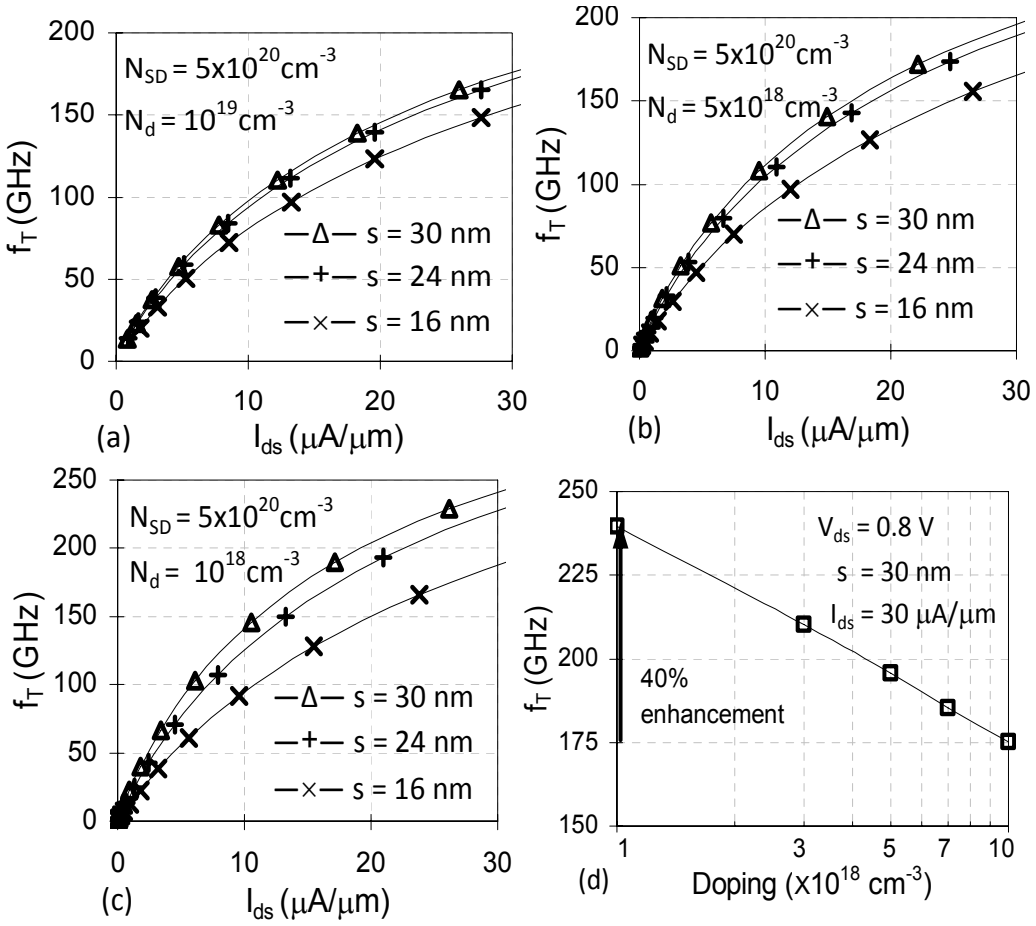

Fig. 3.10 Dependence of f_T on drain current (I_{ds}) for JL device with (a) $N_d = 10^{19}$ cm^{-3}, (b) $N_d = 5x10^{18}$ cm^{-3}.Dependence of f_T on drain current (I_{ds}) for JL device (c) $N_d = 10^{18}$ cm^{-3} for three different spacer widths (16 nm, 24 nm and 30 nm). (d) Variation of f_T on channel doping for JL type-III device with s = 30 nm.

The enhancement in f_T values from 170 GHz to 240 GHz (40%) is achieved in JL devices with reduction in doping from 10^{19} cm^{-3} to 10^{18} cm^{-3} (fig. 3.10*d*) at I_{ds} = 30 μA/μm and s = 30 nm. In order to understand the reason for this improvement, we will confine our analysis to JL type-III devices (fig. 3.8*c*) with $N_d = 10^{18}$ cm^{-3} and s = 16 nm and 30 nm and conventional JL MOSFET (JL type-I) with $N_d = 10^{19}$ cm^{-3}. The JL device with $N_d = 10^{19}$ cm^{-3} is selected as it is the most reported doping level in JL devices [75, 88].

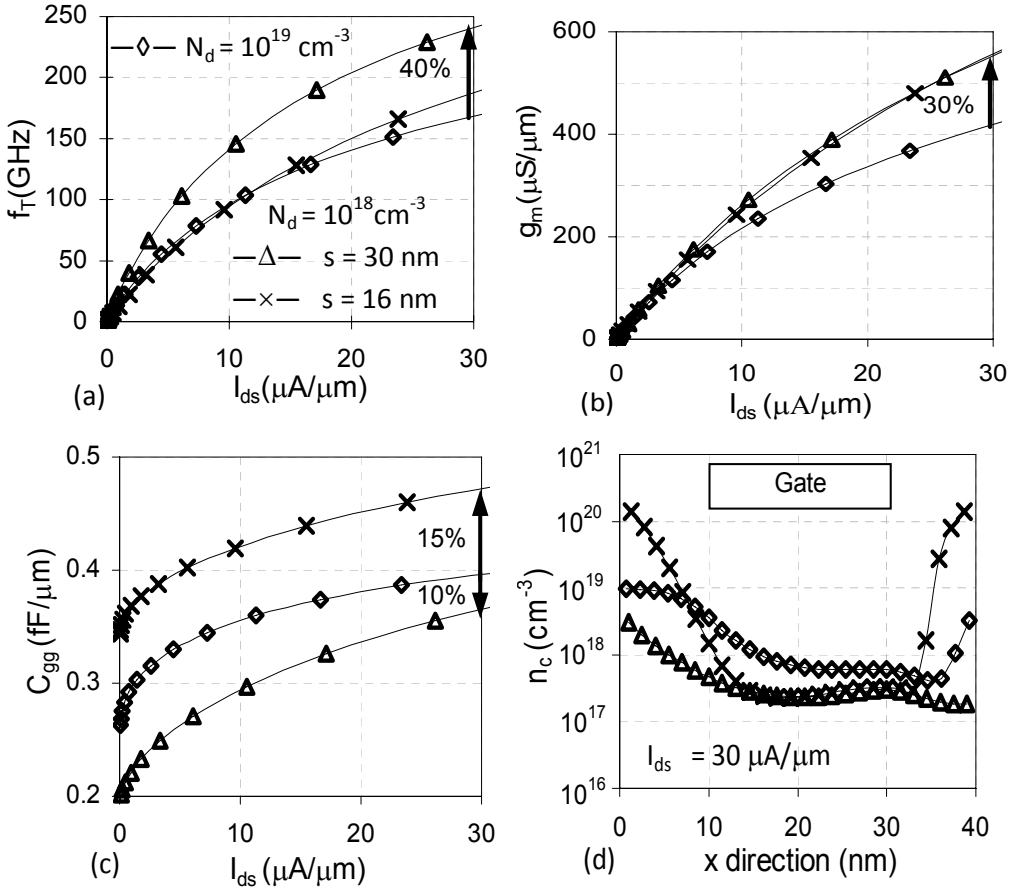

Fig. 3.11 Dependence of (a) f_T, (b) g_m, (c) C_{gg} on drain current (I_{ds}) for JL transistor with $N_d = 10^{18}$ cm^{-3} and 10^{19} cm^{-3} and (d) Variation of electron concentration (n_c) at centre of silicon film along the channel (x) direction at for JL transistor with $N_d = 10^{18}$ cm^{-3} and 10^{19} cm^{-3}. Notations are same as shown in (a). Gate is located from 10 nm to 30 nm.

The variation of cut-off frequency (f_T) with drain current for different JL architectures is compared in fig. 3.11*a*. A JL type-III device with $N_d = 10^{18}$ cm^{-3} and s =16 nm achieves f_T values similar to JL type-I with $N_d = 10^{19}$ cm^{-3}. f_T values when compared to conventional JL MOSFET with $N_d = 10^{19}$ cm^{-3} (type-I) are enhanced by 40% with the use of a wider spacer (s = 30 nm). This enhancement is due to an improvement in g_m and C_{gg} values. g_m values are nearly 30% higher for JL type-III devices with $N_d = 10^{18}$ cm^{-3} as compared to JL type-I device with $N_d = 10^{19}$ cm^{-3} (fig. 3.11*b*). Since only spacer width (s) changes for type-III JL devices ($N_d = 10^{18}$ cm^{-3}), channel doping remaining the same, not much variation can be seen in g_m for these two devices in the current range. C_{gg} values of 0.36 fF/μm and 0.47 fF/μm are achieved for

JL type-III device with N_d = 10^{18} cm^{-3} with spacer width s of 30 nm and 16 nm respectively. These values are 10% lower and 15% higher than C_{gg} value of JL type-I device with N_d = 10^{19} cm^{-3} respectively, as shown in fig. 3.11*c*. The higher C_{gg} values negate the improvement in g_m shown by type-III JL device (fig. 3.11*b*) with s = 16 nm and similar f_T values are achieved for type-III JL with s = 16 nm and N_d = 10^{18} cm^{-3} and type-I JL MOSFET (N_d = 10^{19} cm^{-3}). The electron concentration (n_c) profiles extracted at the centre of the film show that the lateral extension of the depletion width is minimum in a JL type-III device with s = 16 nm as compared with s = 30 nm. This results in higher capacitance values as shown in fig. 3.11*c*. The depletion width is unable to extend beyond the spacer width of 16 nm due to the peak S/D doping. A wider spacer (s = 30 nm) allows greater extension of depletion region as indicated by lower values of electron concentration at the gate edge and consequently lower C_{gg} values (fig. 3.11*d*).

As shown in fig. 3.12*a*, the maximum oscillation frequency (f_{MAX}), is enhanced by 50% for optimized JL type-III device at 30 μA/μm as compared to JL type-I device (N_d = 10^{19} cm^{-3}). Similarly, 15% enhanced voltage gain A_{VO} = g_m/g_{ds} , where g_{ds} represents the output conductance, is achieved for optimized JL device at same current level (fig. 3.12*b*). The dependence of the ratio of gate-to-source capacitance (C_{gs}) to gate-to-drain capacitance (C_{gd}) on drain current for different devices is shown in fig. 3.12*d*. C_{gs}/C_{gd} ratio represents the parasitic feedback capacitance and is a major limiting factor in downscaling analog/RF devices [16]. The reduction of C_{gs}/C_{gd} ratio implies the loss of gate controllability and increase of parasitic Miller capacitance. As shown in fig. 3.12*d*, C_{gs}/C_{gd} ratio is enhanced by 20% in JL type-III devices with N_d = 10^{18} cm^{-3} as compared to JL type-I device with N_d = 10^{19} cm^{-3}, since short channel effects are effectively suppressed due to the longer effective channel length [75]. The enhanced f_{MAX} value shown by optimized JL devices is due to improvement in f_T, g_m/g_{ds} and C_{gs}/C_{gd} ratio [16]. As shown in fig. 3.13*a*, JL device with wider spacer (s = 30 nm) achieves 40% enhanced Early voltage (V_{EA} = I_{ds}/g_{ds}) of 3.5 V as compared to conventional JL device with N_d = 10^{19} cm^{-3}.

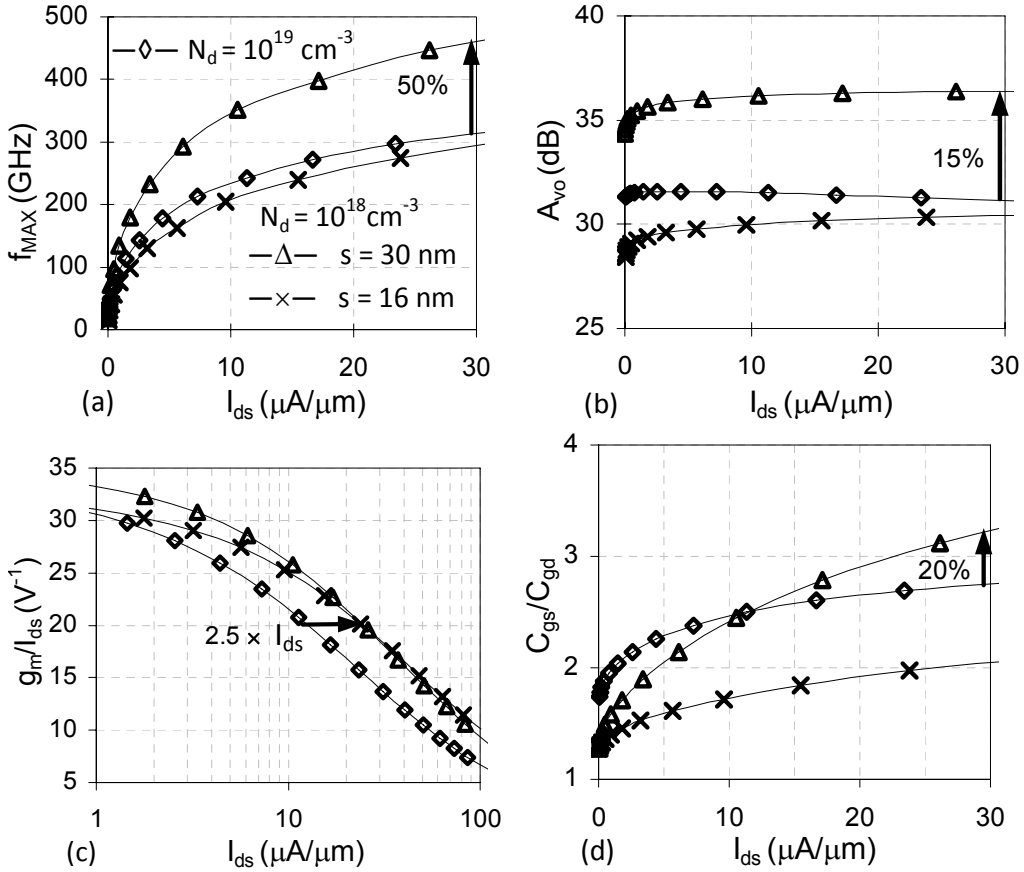

Fig. 3.12 Dependence of (a) f_{MAX}, (b) A_{VO}, (c) g_m/I_{ds}, and (d) C_{gs}/C_{gd}, at I_{ds} = 30 μA/μm for JL devices with $N_d = 10^{18}$cm^{-3} and 10^{19} cm^{-3}. Notations are same as shown in (a).

Product of Early voltage (V_{EA}) with g_m/I_{ds} ratio determines the intrinsic voltage gain (A_{VO}). The improvement in V_{EA} as shown in fig. 3.14*e* is responsible for enhanced A_{VO} for optimized JL type-III device. Results indicate that both g_m and g_{ds} are affected by reducing channel doping while spacer width variation affects g_{ds} only. Electric field distribution in the silicon film (fig. 3.13*b*) clearly demonstrates the reduction in peak electric field at the gate edge near drain for wider spacer (s = 30 nm) JL type-III device ($N_d = 10^{18}$ cm^{-3}) as compared to type-I device with $N_d = 10^{19}$ cm^{-3}. This reduction in electric field contributes to higher values of V_{EA}, A_{VO} and C_{gs}/C_{gd} for the optimized JL type-III device. The values of higher f_T, f_{MAX} and A_{VO} at lower current levels suggests the potential benefits of optimized doping ($N_d = 10^{18}$ cm^{-3}) and spacer width (s = 30 nm) in JL type-III devices for low power and high speed RF front end circuits [71].

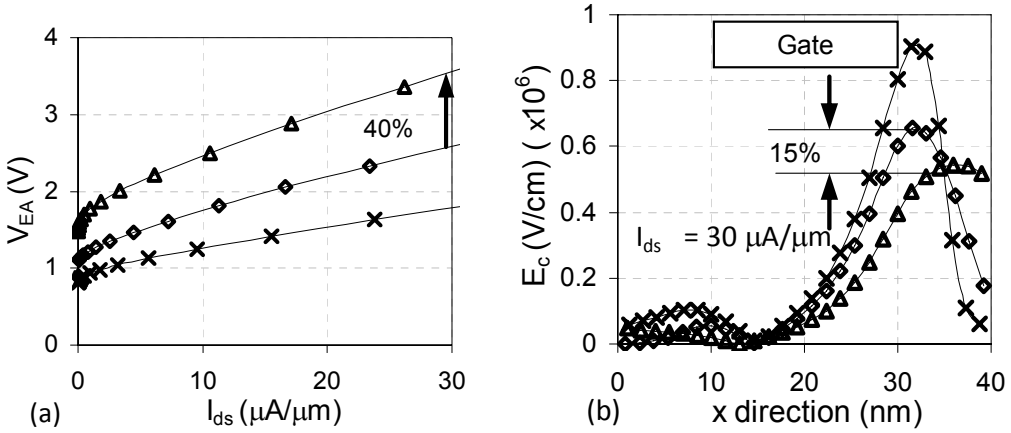

Fig. 3.13 Dependence of (a) V_{EA} on I_{ds}. (b) Electric field distribution along channel direction (x) at I_{ds} = 30 μA/μm for JL devices with $N_d = 10^{18}$cm^{-3} and 10^{19} cm^{-3}. Notations are same as shown in 3.12 (a). Gate is located from 10 nm to 30 nm.

Therefore, JL MOSFETs designed with a moderate doping of 10^{18} cm^{-3} instead of 10^{19} cm^{-3} and a spacer width of 30 nm (s/L_g = 1.5) are most appropriate for low power applications ($I_{ds} \leq$ 30 μA/μm). We have included I_d-V_{gs} characteristics (fig. 3.14*a*) for the junctionless (type-III) device for four different spacers (s = 0, 10, 20 and 30 nm). Fig. 3.14*b* below compares the variation of S-slope and $(g_m/I_{ds})_{max}$ as a function of spacer width with junctionless (type III) MOSFET.

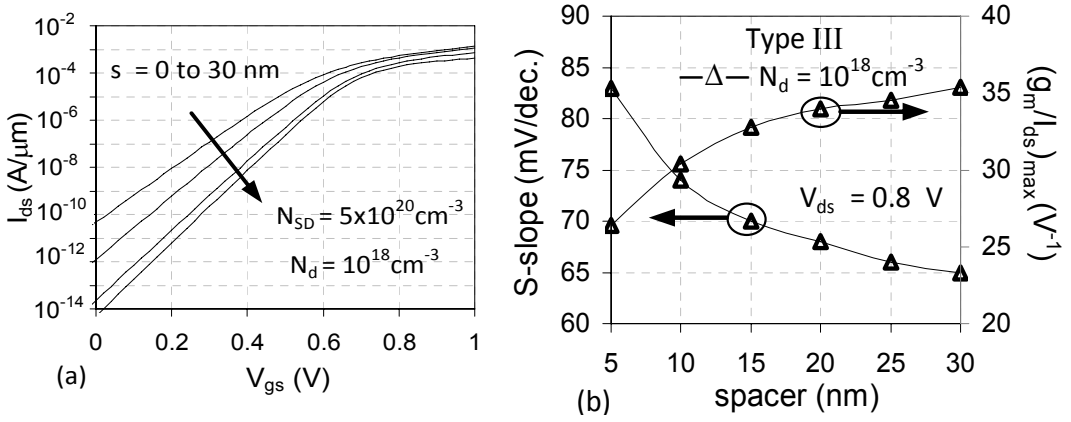

Fig. 3.14 (a) I_d - V_{gs} characteristics for junctionless MOSFETs (type-III) with spacer (s) = 0 to 30 nm and channel doping of 10^{18} cm^{-3}. (b) Dependence of S-slope and $(g_m/I_{ds})_{max}$ on spacer width (s) for JL type-III ($N_d = 10^{18}$ cm^{-3}) devices.

An increase in spacer width increases the effective channel length, and S-slope and $(g_m/I_{ds})_{max}$ both improve. For spacer (s) ≥ 15 nm, S-slope and g_m/I_{ds} max of type III device is better in comparison to type-I device. The enhancement in peak-g_m/I_{ds} can be directly correlated with a higher gain for type-III devices.

3.5.2 Analog Sweet Spot

Recently there have been several reports on analog reliability and RF linearity of JL transistors [97-101]. III–V JL gate-all-around (GAA) nanowire MOSFETs have been experimentally demonstrated [97] and reported that source/drain resistance and thermal budget are minimized by regrowth using chemical vapor deposition, instead of implantation. Simulation results reveal that a gate material engineered JL transistor shows better immunity against the influence of interface trap charges to maintain device linearization, as compared to a conventional JL cylindrical surrounding gate MOSFET [98]. A superior Bias-Temperature Instability (BTI) reliability has been demonstrated for JL pFETs compared to INV devices [99] and the low oxide electric field of these devices at the overdrive conditions results in reliability improvement [99]. The enhanced linearity of JL nanowire transistors operating in the linear regime had also been reported [100-101].

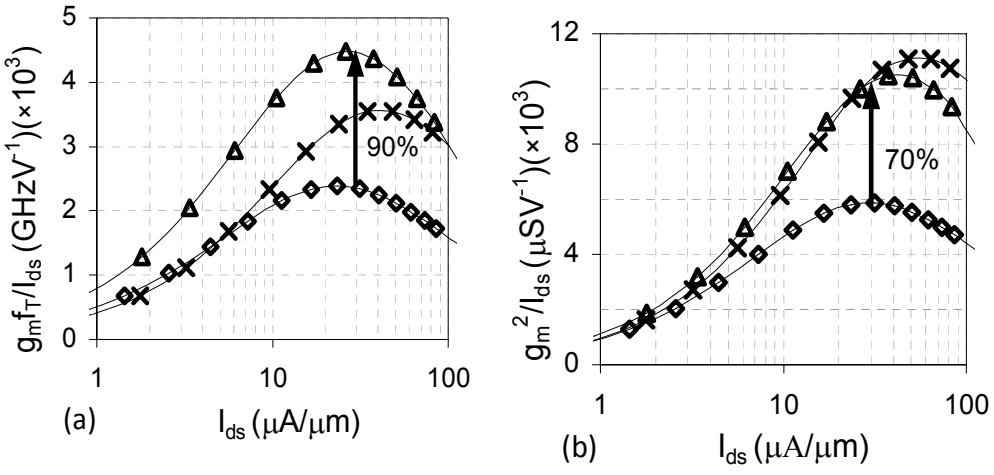

Figure 3.15 Dependence of (a) $g_m f_T/I_{ds}$, and (b) g_m^2/I_{ds} on drain current (I_{ds}) for JL transistors with N_d = 10^{18} cm^{-3} and 10^{19} cm^{-3}. Notations are same as shown in fig. 3.14 *a*.

Achieving a balance between the bandwidth and power efficiency is another crucial challenge of analog design [103-106]. This section results highlight the trade off found to be avoided in DG JL devices. This trade-off is fundamentally linked to the analog/RF metrics of the MOSFET [107]. In contrast to g_m/I_{ds}, f_T of a transistor is highest in strong inversion and increases with I_{ds} with maximum being achieved at 300 μA/μm [35, 69] for conventional inversion-mode MOSFETs. As a result, there exists a fundamental trade-off between the transconductance efficiency and the bandwidth of a transistor. Devices with shorter channel can be biased at lower current levels when bandwidth requirement is kept fixed [35]. The g_m/I_{ds} and f_T trade-off [104-105], severe at shorter gate lengths, can be evaluated and optimized by evaluating the product of g_m/I_{ds} and f_T. As shown in the fig. 3.15*a*, $g_m f_T/I_{ds}$ exhibits a "sweet-spot" around threshold ($V_{gs} - V_{th} = \pm$ 100 mV, where V_{th} is the threshold voltage), which can be utilized for minimizing the trade-off between bandwidth and transconductance efficiency [35, 71].

As $g_m f_T/I_{ds}$ represents a basic challenge of achieving a balance between bandwidth and transconductance efficiency, higher values of $g_m f_T/I_{ds}$ at lower drive currents are desirable. JL type-III device with $N_d = 10^{18}$ cm^{-3} (s = 30 nm) achieves 90% higher value of peak $g_m f_T/I_{ds}$ of 4475 GHz/V ($g_m/I_{ds} = 18$ V^{-1} and $f_T = 245$ GHz) at 30 μA/μm current level as compared to 2340 GHz/V ($g_m/I_{ds} = 13$ V^{-1} and $f_T = 160$ GHz) of JL type-I device with $N_d = 10^{19}$ cm^{-3}. Such an enhancement in $g_m f_T/I_{ds}$ is clearly due to simultaneous improvement in g_m/I_{ds} and f_T. Another important parameter for analog/RF applications is the product of g_m and g_m/I_{ds} i.e. g_m^2/I_{ds} which represents a unified figure of merit considering the signal gain, noise figure and power consumption of a low noise amplifier [70]. g_m^2/I_{ds} also exhibits a sweet spot around the threshold region. The optimized JL type-III (s = 30 nm) device achieves 70% higher value of 10200 μS/V ($g_m/I_{ds} = 18$ V^{-1} and $g_m = 560$ μS) for g_m^2/I_{ds} as compared to 5900 μS/V ($g_m/I_{ds} = 13$ V^{-1} and $g_m = 425$ μS) for JL type-I device with $N_d = 10^{19}$ cm^{-3} at specified current level of 30 μA/μm, as shown in fig. 3.15*b*. This is attributed to improvement both in g_m and g_m/I_{ds} values in JL type-III device at the specified current level. These results indicates that optimized JL type-III transistors are promising structures for vital building blocks (e.g. operational transconductance amplifiers, low noise amplifiers etc.) of low power

analog/RF circuits [70-71] at lower technology nodes. The higher values of $g_m f_T/I_{ds}$ and g_m^2/I_{ds} for type-III JL MOSFETs signify improved gate controllability and reduced short channel effects. The results for $g_m f_T/I_{ds}$ and g_m^2/I_{ds} reflect on the potential benefits of optimizing the channel doping and spacer width optimization in JL transistors to achieve enhanced performance metrics corresponding to the analog sweet spot.

3.5.3 Parasitic Fringing Capacitances

In this section, we shall evaluate the fringing capacitance components of optimized JL devices (N_d = 10^{18} cm^{-3}) against the variation in spacer width. Parasitic capacitance has several components such as gate-to-plug capacitance, inter electrode capacitance, corner capacitance [108] along with inner and outer fringe capacitance. However, change in device architecture from inversion mode to junctionless is likely to impact the fringing component of the total parasitic capacitance which is evaluated as the combination of inner fringing capacitance (C_{if}) and outer fringing capacitance (C_{of}) as shown in fig. 3.16*a*.

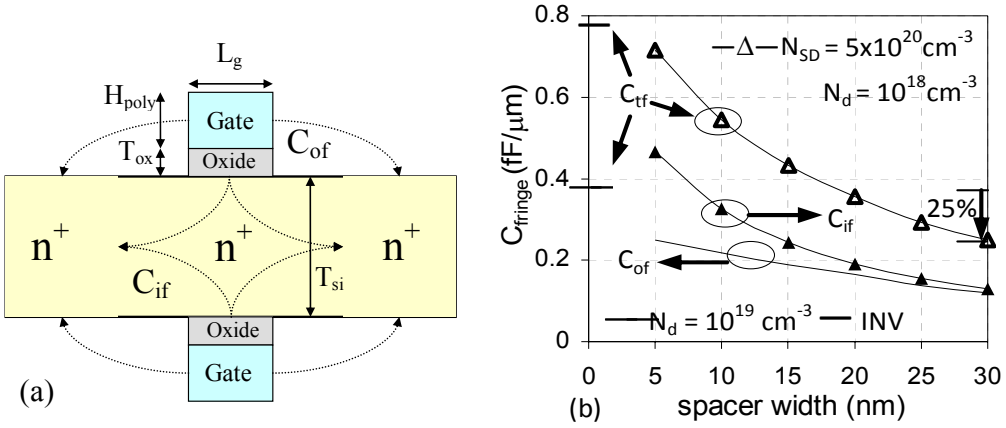

Figure 3.16 (a) Schematic diagram of JL MOSFET with parasitic fringing capacitances (inner C_{if} and outer C_{of}). (b) Dependence of fringing capacitance (C_{fringe}) on spacer width (s) for JL transistor with N_d = 10^{18} cm^{-3}. Gate height (H_{poly}) is 20 nm. The solid and dashed lines on the y-axis of (b) represents the fringing capacitance values for inversion mode and JL (N_d = 10^{19} cm^{-3}) devices respectively.

The major contribution to this change in parasitic capacitance is reduction in the inner fringing capacitance (C_{if}) due to wider depletion region caused by unintentional underlap behavior in JL MOSFETs. The outer fringing capacitance (C_{of}), dependent on gate poly height (H_{poly}), does not change appreciably with reduction in N_d. The

dependence of fringing capacitance on spacer width is shown in fig. 3.16*b*. The value of total fringing capacitance (C_{tf}) for INV devices is ~0.8 fF/μm. C_{tf} is highest for INV devices as the lateral extension of the depletion width is limited due to the additional S/D doping concentration. For optimized JL type-III devices (s = 30 nm) with doping $N_d = 10^{18}$ cm^{-3}, C_{tf} is nearly 25% lower than JL type-I device with $N_d = 10^{19}$ cm^{-3}. Lower fringing capacitance directly reflects on the lower C_{gg} and enhanced values for both f_T and f_{MAX} as discussed in the previous section. The reduction of parasitic capacitance in optimally designed JL transistors signify their usefulness in low-power analog/RF circuits demanding high bandwidth [105]. Moreover, as mentioned earlier high channel doping concentration in junctionless MOSFETs reduces carrier mobility which affects drive current and subsequently results in lower transconductance. This problem was reported, via simulations, to be eliminated using dual material gate on to the double gate JL DG transistor, i.e., two metal gates having different work functions [109]. The proposed channel doping and spacer-width engineering may help device designers to fabricate nanoscale transistors using such dual-material gates.

3.5.4 Comparison with Optimized Inversion Mode Transistors

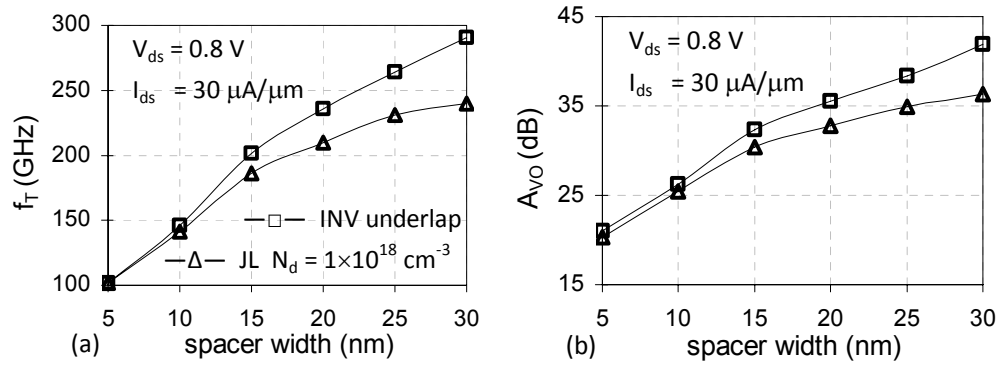

Figure 3.17 Dependence of (a) f_T, and (b) A_{VO} on spacer width (s) for INV underlap and JL type-III (N_d = 10^{18} cm^{-3}) devices at I_{ds} = 30 μA/μm.

Conventional inversion mode (INV) devices with abrupt pn junctions and underlap devices are compared in this section. An underlap design in inversion mode MOSFETs improves gate controllability and results in improved performance metrics

[103]. In order to compare optimized JL and INV devices, the dependence of f_T and A_{VO} on spacer width is analyzed and results are shown in fig. 3.17*a-b*. Performance improves for both INV and JL type-III devices with increase in spacer width as f_T and A_{VO} increase with increase in spacer width. As shown in fig. 3.17*a-b* an increase in spacer width from 10 nm to 20 nm results in an improvement in f_T for JL type-III and INV underlap devices by 50% and 60% respectively, and A_{VO} increases by ≈35% for both the devices. On further increasing s from 20 nm to 30 nm, f_T and A_{VO} values are enhanced by ≈16%-20% for both devices. If spacer width is extended beyond 30 nm to 40 nm, a marginal increase of 5% is achieved for both INV underlap and JL type-III devices. Although, C_{gg} reduces with increase in spacer width due to reduction in fringing capacitances, g_m and g_{ds} also degrade after s > 30 nm due to parasitic resistance associated with very wider spacers [103, 110]. This counteracts any enhancement of f_T and A_{VO} with increasing spacer width in both the devices. Results shows that optimized JL type-III (s =30 nm) devices achieve f_T and A_{VO} values that are somewhat lower than optimized INV underlap ($N_a = 10^{15}$ cm^{-3}) devices for s lying between 20 nm and 30 nm. In order to achieve the similar values of f_T and A_{VO}, spacer width for JL transistor should be typically 5 nm wider than that of inversion mode underlap MOSFET.

3.5.5 Parameter Sensitivity

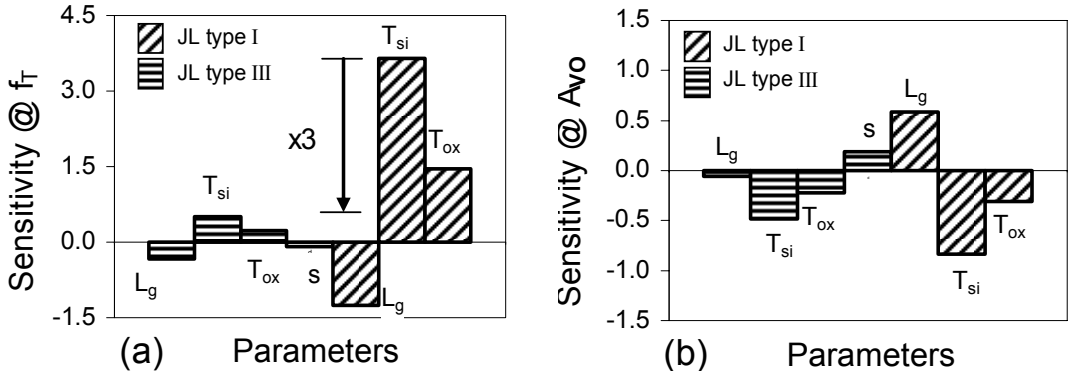

Figure 3.18 Sensitivity analysis for (a) f_T, and (b) A_{VO} for JL type- III ($N_d = 10^{18}$ cm^{-3}) and JL type- I (10^{19} cm^{-3}) devices biased at peak–$g_m/f_T/I_{ds}$.

Sensitivity to device and structural parameters is another issue while operating at lower current drives, since a minor shift in device parameters can result in significant variations in performance metrics (f_T and A_{VO}) and question the usefulness of particular device architecture. We have evaluated sensitivity (S) of analog/RF performance metrics on device parameters such as L_g, T_{si}, T_{ox} and spacer width (s) [72]. Sensitivity values evaluated for two JL devices (type-I and type-III with s = 30 nm) as shown in fig. 3.18*a-b*, biased at peak $g_m f_T/I_{ds}$ (I_{ds} = 30 μA/μm). Sensitivity against variation L_g, T_{si}, T_{ox} is reduced for JL type-III device as compared to the JL type-I device.

Due to the unintentional underlap, JL type-III devices have longer effective channel length (L_{eff}) and lower fringing capacitances than JL type-I devices. L_{eff} increases with reduction in doping concentration N_d. This results into better gate controllability and hence better tolerance against L_g variations. Threshold voltage (V_{th}) of a JL MOSFET is a function of doping concentration. When N_d, T_{si} and T_{ox} are reduced, V_{th} increases [84, 111]. This variation in threshold voltage of the device, with variations in T_{si}, T_{ox} and N_d, is suppressed with reduction in N_d [84, 111]. The tolerance of threshold voltage results in lesser variation in drain current for JL type-III devices as compared to type-I devices due to the reduced channel doping. Since transconductance (g_m) is directly related to drain current, it is observed that g_m is less effected by the variations in T_{si} and T_{ox} in JL type-III devices as compared to JL type-I devices. This translates into improved tolerance and less sensitivity of f_T and A_{VO} towards parameter variations. It can be observed from fig. 3.18*a-b* that f_T is more sensitive to parameter variations than A_{VO} for JL type-I devices. This is due to reason that change in g_m values with device parameters is cancelled by similar variations in g_{ds} values, and A_{VO} shows less sensitivity. INV underlap devices have shown reduced sensitivity as compared to conventional abrupt INV devices [112]. It was also observed in our results (not shown here) that INV underlap and JL type-III devices show comparable sensitivity of analog/RF metrics towards variation in device parameters.

3.5.6 Quantum Effects in Optimized Junctionless Devices

Quantum confinement effects (QCE) are expected to degrade MOS transistors at nanoscale dimensions due to carrier confinement and increased equivalent oxide

thickness [1]. QCE result in the increase in threshold voltage (V_{th}) [113]. This increase is negligible in devices where T_{si} > 8 nm, but is significant in the devices with the smaller cross sections [65]. Quantum simulations have been performed using density gradient model using the approach of Duarte *et al*., [96] for JL devices. Cut-off frequency (f_T) evaluated considering quantum confinement effects, does not significantly deviate from the classical simulation results for optimized JL type-III devices (fig. 3.19), in the considered current range. This is due to the reason that in JL devices electron concentration is at the centre of the film and not at the surface, and QCEs decreases with decrease in film doping in JL devices [96]. Since carrier confinement leads to increase in effective oxide thickness and this degrades g_m and f_T. However, carrier confinement also leads to reduction in C_{gg}, which may counteract any degradation in f_T. It was found in JL type-III device while considering quantum confinement effects, at lower current levels of 30 μA/μm, reduction in C_{gg} is dominant and hence f_T is found marginally higher as compared to f_T values for the device with non-quantum simulations.

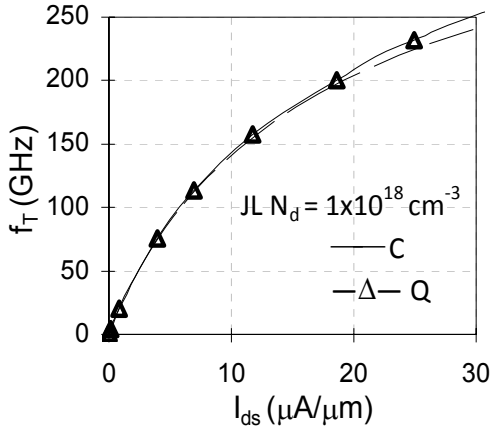

Figure 3.19 Comparison of f_T for JL type-III devices with N_d = 10^{18} cm^{-3} (s = 30 nm) using Quantum (Q) and classical (C) simulation models.

However, at higher current levels of 50 μA/μm, g_m degradation is dominant which leads to degraded f_T. Thus, JL type-III devices with reduced doping are not expected to exhibit significant quantum confinement at such lower current levels of 30 μA/μm. These results also indicate that the overall conclusions of the work will not be

significantly modified even when quantum effects are considered in JL devices designed with the device parameters of this study. As tunneling from Source/Drain to Channel region is not expected in junctionless devices without additional control gates, Band-to-band tunneling (BTBT), Trap-assisted tunneling (TAT) and interface traps models have not been included [114].

3.6 Alternate manufacturing advances in junctionless MOSFETs

Recently, a novel junctionless FinFET structure with a shell doping profile (SDP) formed by molecular monolayer doping (MLD) method and microwave annealing (MWA) at low temperature was proposed [115]. Due to the ultra thin SDP leading to an easily-depleted channel, the JL FinFET reported an ideal subthreshold slope (~ 60 mV/decade) at a high doping level [115]. Poly Si based JL FinFETs processed with MLD and MWA exhibit superior subthreshold slope ~ 67mV/dec and excellent on-off ratio ($> 10^6$) for both n and p channel devices. Such novel fabrication processes are inevitable for future generation nanoscaled MOSFETs. Barraud *et. al* had shown the performance of high-κ/metal gate nanowire transistors fabricated with a channel thickness of 9 nm and sub-15-nm gate length and and reported near-ideal subthreshold slope, extremely low leakage currents and a high on–off ratio > 10^6 [116]. Fabricated short channel (L_g = 80 nm) GaAs GAA nanowire (NW) FETs with extremely scaled nanowire width (9 nm) reported excellent g_m linearity (characterized by the high third intercept point), at biases as low as 300 mV. The high linearity was found to be insensitive to the bias conditions, favorable for low power applications [97]. Due to its degenerate doping level and junctionless structure, nonlinearities from both transconductance and output conductance had been found to be minimized [97]. JL device overall performance for the RF linearity application is much better than a modern short-channel MOSFET [101]. Deeply scaled gate length of 3 nm junctionless device had also been reported recently through simulations [117]. The formation of ultra shallow junctions is a limiting factor to scaling and puts severe constraints on the thermal budget. Furthermore, random impurity fluctuations from S/D dopants scattered in the channel region cause reproducibility problems [118]. All these advances highlight the future prospects of designing nanoscale junctionless transistors and provide useful

conclusion on their overall suitability for deca nanometer MOSFETs and nanowire FETs [118].

3.7 Conclusions

As junctionless transistors are different as compared to inversion mode devices, work was carried out in this chapter to examine the significance of device architecture on the values of voltage gain, cut-off frequency, analog sweet spot, gain-bandwidth trade-off and maximum frequency of oscillation. Junctionless transistors achieve enhanced values of both gain and bandwidth in comparison to inversion mode MOSFETs without any need for channel engineering methodology due to unintentional underlap structure which subsequently results in the following:

(a) Longer effective channel length in the subthreshold region

(b) Lower parasitic capacitance which dominates the total capacitance in the subthreshold region and limits the bandwidth,

(c) Reduced vertical electric filed at the gate edge towards the drain.

The performance of junctionless transistors can be improved further by adopting a moderate channel doping ($\cong 10^{18}$ cm^{-3}) and source/drain extension region engineering. JL devices do not show severe degradation in analog/RF performance metrics when compared with undoped inversion mode devices. Optimum design has show a significant increase in performance metrics such as intrinsic voltage gain, cut-off frequency, maximum oscillation frequency, along with reduced sensitivity, enhanced value of sweet spot thus suppressing gain-bandwidth trade-off. For operation at lower current levels (subthreshold region), these devices should be designed with wider spacers (1.5 × gate length) and lower channel doping ($N_d = 10^{18}$ cm^{-3}) which enhances gate controllability and reduces fringing capacitances. The results obtained from the work carried out in this chapter are particularly useful for designing JL transistors for moderate frequency applications.

Chapter 4

Analog/RF Performance of Tunnel FETs

4.1 Introduction

Ultra Low Power (ULP) operation is increasingly in demand for future System-on-Chip (SOC) circuits using nanoscale analog/RF transistors [56, 57] and different architectures have gained considerable interest due to their ability to suppress short channel effects (such as underlap inversion-mode [58] and junctionless MOSFETs [74]) and improved steep switching from off-to-on state (such as Lateral Tunnel FET [119-122] and Vertical Tunnel FET [123, 124]). In this chapter, we analyze the analog/RF performance metrics of ULP tunneling MOSFET architectures.

In contrast to conventional MOSFETs, where charge carriers are thermally injected over a barrier, the injection mechanism in a Tunnel FET (TFET) is interband tunneling [119-128], whereby charge carriers tunnel from one energy band to another across a heavily doped *pn* junction. In such a device band-to-band tunneling (BTBT) can be switched on and off by controlling the band bending in the channel region by means of the gate bias [119]. This function can be realized in a reverse-biased p-i-n structure [120]. In principle, the TFET is an ambipolar device [121], showing p-type behavior with dominant hole conduction and n-type behavior with dominant electron conduction. However, by designing an asymmetry in the doping level or profile, or by restricting the movement of one type of charge carrier using heterostructures, the tunneling barrier at the drain can be widened to suppress the ambipolarity [121]. The asymmetry also achieves a low off-state current. In the TFET off state, the valence band edge of the channel is located below the conduction band edge of the source, BTBT is suppressed, leading to very small off-state currents that are dictated by the reverse-biased p-i-n diode. Applying a negative gate voltage pulls the energy bands up [120].

A conductive channel is formed as the channel valence band has been lifted above the source conduction band because carriers can now tunnel into empty states of the channel. Because only carriers in an energy window $\Delta\Phi$ (fig 4.1) can tunnel into the channel, the energy distribution of carriers from the source is limited; the high-energy

part of the source Fermi distribution is effectively cut off. Thus the electronic system is effectively 'cooled down', acting as a conventional MOSFET at a lower temperature. This filtering function makes it possible to achieve an subthreshold slope (*S*) of below 60 mV/decade [120-121]. However, the channel valence band can be lifted by a small change in gate voltage, and the tunneling width can effectively be reduced by the gate voltage. As a consequence of the BTBT mechanism, *S* in a TFET is not constant, but depends on the applied gate–source bias, increasing with the gate-to-source bias. The key to the better voltage scaling of a TFET than a MOSFET is that *S* remains below 60 mV/decade over several orders of magnitude of drain current [120]. Challenge in TFETs is to realize high on currents because I_{ON} critically depends on the transmission probability, T_{WKB}, of the interband tunneling barrier. This barrier can be approximated by a triangular potential, as indicated by the grey shading in fig. 4.1, so *T* can be calculated using the Wentzel–Kramer–Brillouin (WKB) [119, 22] approximation

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar\left(E_g + \Delta\Phi\right)}\right) \tag{4.1}$$

where m^* is the effective mass and E_g is the bandgap. Here, λ is the screening tunneling length [119] and describes the spatial extent of the transition region at the source–channel interface (fig. 4.1); it depends on the specific device geometry. In a Tunnel FET, at constant drain voltage, V_{ds}, the V_{gs} increase reduces λ and increases the energetic difference between the conduction band in the source and the valence band in the channel ($\Delta\Phi$), so that in a first approximation the drain current is a super-exponential function of V_{gs}. As a result, in contrast to the MOSFET, the point subthreshold swing of the TFET is not constant [119] but strongly depends on V_{gs}. The smallest subthermal values occur at the lowest gate voltages [120]. A high on current requires a high transparency of the tunneling barrier, thus maximizing T_{WKB}, which in the best case should be unity.

4.2 Performance boosters for Tunnel FET

Previously, Choi *et al.* have demonstrated a 70-nm n-channel tunneling field-effect transistor (TFET) which has a subthreshold swing (SS) of 52.8 mV/dec at room temperature [129]. TFET optimization should simultaneously achieves the highest possible I_{on}, the lowest subthreshold slope (S_{avg}) over many orders of magnitude of drain current [129], and the lowest possible I_{off}. In order to increase the ON current further, the approaches were suggested: reduction of effective gate oxide thickness, increase in the steepness of the gradient of the source to channel doping profile, and utilization of a lower bandgap channel material [129]. To outperform CMOS transistors, the target parameters for TFETs are: I_{ON} in the range of hundreds of milliamperes; S_{avg} far below 60 mV/decade for four to five decades of current; $I_{on}/I_{off} > 10^5$; and $V_{dd} < 0.5$ V. Because S decreases with the V_{gs}, TFETs are naturally optimized for low-voltage operation. To realize a high tunneling current and a steep slope, the transmission probability of the source tunneling barrier should become close to unity [119] for a small change in V_G.

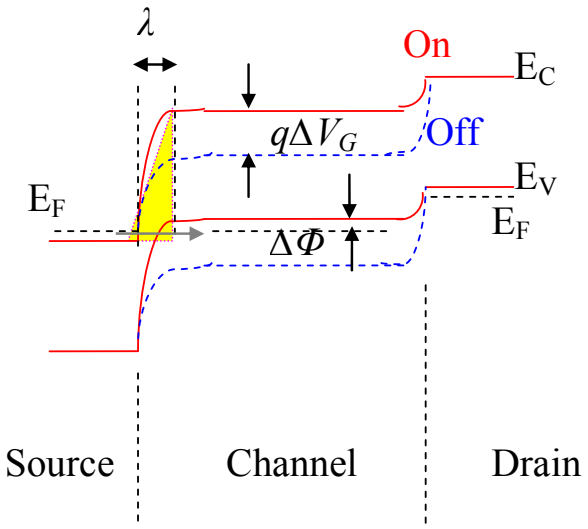

Fig. 4.1 Principle of operation of a Tunnel FET [119].

The WKB approximation, shown in equation 4.1, suggests that the bandgap (E_g), the effective carrier mass (m^*) and the tunneling length (λ) should be minimized for high barrier transparency. Whereas E_g and m^* depend solely on the material system,

λ is strongly influenced by several parameters, such as the device geometry, dimensions, doping profiles and gate capacitance [119]. A small λ results in a strong modulation of the channel bands by the gate. This requires a high-permittivity (high-κ) gate dielectric with as low an equivalent oxide thickness as possible [120-121]. Abruptness of the doping profile at the tunnel junction is also important.

To minimize the tunneling barrier, the high source doping level must fall off to the intrinsic channel in as short a tunnel width as possible [120]. This requires a change in the doping concentration of about 4–5 orders of magnitude within a distance of only a few nanometers. Increasing the source doping reduces λ and may lead to a slightly smaller energy barrier at the tunnel junction because of bandgap narrowing. However, the energy filtering effect described above becomes effective only if the Fermi energy in the source is not too large [120]. The WKB approximation works proper in direct bandgap semiconductors, such as InAs (if one single imaginary path connecting the valence band and the conduction band dominates the tunneling process), but has limited accuracy for Si and Ge structures or when quantum effects and phonon-assisted tunneling become dominant.

4.3 Simulation of Tunnel FETs

The standard band-to-band tunneling model described in ATLAS [22] calculates the recombination-generation rate at each point based solely on the field value local to that point. Hence it can be referred as local model. To model the tunneling process more accurately, one needs to take into account the spatial variation of the energy bands and whether the generation/recombination of opposite carrier types is not spatially coincident. Figure 4.2 illustrates this for a reverse biased p-n junction where it is assumed that the tunneling process is elastic. For degenerately doped p-n junctions, one can obtain tunneling current at forward bias and consequently negative differential resistance in the forward I-V curve.

4.3.1 Non-local Band-To-Band tunneling model

The ATLAS [22] non-local Band-To-Band tunneling model, specified as BBT.NONLOCAL, allows modeling of the forward and reverse tunneling currents of

degenerately doped p-n junctions. In the simulator BBT.NONLOCAL model needs defining the areas where it will be applied. These areas must each contain a single p-n junction, which may be either planar or non-planar. They should have a mesh which interpolates data from the underlying device mesh and performs the band-to-band tunneling calculations on the interpolated data. BBT.NONLOCAL thus assumes that the tunneling takes place on a series of 1D slices through the junction, each slice being locally perpendicular to the junction. The slices themselves will be approximately parallel to their neighbors. ATLAS has a method of setting up these areas of slices. This method is only applicable to planar junctions parallel to the x (horizontal) or y (vertical) axes. It allows you to set up a rectangular area using the QTX.MESH and QTY.MESH statements in respective X and Y directions. You also specify the number of tunneling slices and the number of mesh points along the slices.

It is recommended to have as fine mesh as possible in the tunneling direction, both for the physical mesh and this tunneling mesh, so that values can be accurately interpolated between the two meshes. If the tunneling direction is the x-direction, then set QTUNN.DIR to 1 on the MODELS statement. By setting the QTUNN.DIR parameter on the MODELS statement to be 0, one can define the tunneling direction to be in the y-direction.

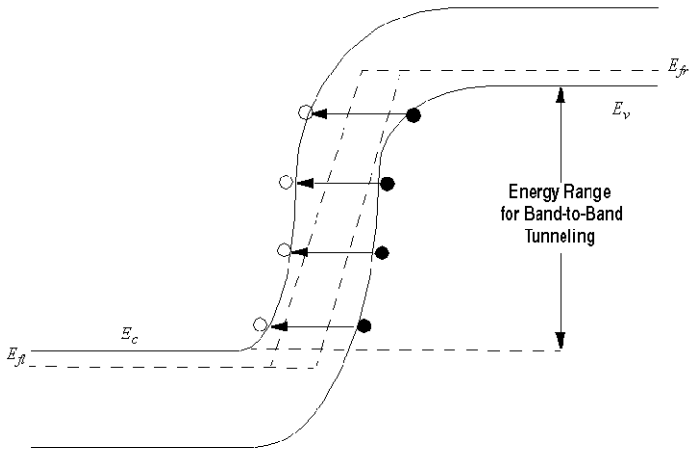

Fig.4.2 Schematic of non-local band to band tunneling in reverse bias [22]

In order to explain how the tunneling current is calculated, let us consider the energy band profile along each tunneling slice with reverse bias applied across the junction.

The range of valence band electron energies for which tunneling is permitted is shown in the schematic of the energy band profile in Figure 4.2. The highest energy at which an electron can tunnel is E_{upper} and the lowest is E_{lower}. The tunneling can be thought of being either the transfer of electrons or the transfer of holes across the junction. The rates for electrons and holes are equal and opposite because the tunneling results in the generation or recombination of electron-hole pairs. Considering the tunneling process as a transfer of an electron across the junction the net current per unit area for an electron with longitudinal energy E and transverse energy E_T is

$$J(E) = \frac{q}{\pi\hbar}\iint T(E)\left[f_l(E+E_T) - f_r(E+E_T)\right]\rho(E_T)\,dE\,dE_T \tag{4.2}$$

$$f_l = \left(1+\exp\left[\left(E+E_T-E_{Fl}\right)/KT\right]\right)^{-1} \tag{4.3}$$

$$f_r = \left(1+\exp\left[\left(E+E_T-E_{Fr}\right)/KT\right]\right)^{-1} \tag{4.4}$$

$$\rho(E_T) = \frac{\sqrt{(m_e m_h)}}{2\pi\hbar^2} \tag{4.5}$$

where $T(E)$ is the tunneling probability for an electron with longitudinal energy E. $\rho(E_T)$ is the 2-dimensional density of states corresponding to the 2 transverse wavevector components and f_l is the Fermi-Dirac function using the quasi Fermi-level on the left hand side of the junction. Similarly f_r uses the quasi-Fermi level on the right hand side of the junction. Here it is assumed that the transverse energy is conserved in the tunneling transition. Because we are using a 2-band model to give the evanescent wavevector, the transverse electron effective mass and the transverse hole effective mass are combined in the 2D density of states $\rho(E_T)$. By integrating over transverse carrier energies, one can obtain the contribution to the current from the longitudinal energy range.

The Fermi levels used in Equation are the quasi-Fermi levels belonging to the majority carrier at the relevant side of the junction. In Figure 4.2, E_{Fl} would be the Electron quasi-Fermi level and E_{Fr} would be the hole quasi-Fermi level. In equilibrium, $E_{Fl} = E_{Fr}$ and the current contributions are all zero. As also seen in Figure 4.2 the start and end points of the tunneling paths, x_{start} (filled circle) and x_{end} (unfilled circle), depend on Energy. ATLAS calculates the start and end points for each value of E and

calculates the evanescent wavevector k(x) at points between the start and end points [22]. This ensures that the energy dispersion relationship is electron-like near the conduction band and hole-like near the valence band, and approximately mixed in between. The tunneling probability, T(E), is then calculated using the WKB approximation as

$$T(E) = \exp\left(-2 \int_{x_{start}}^{x_{end}} k(x) dx \right) \tag{4.6}$$

4.3.2 Calibration of model parameters

To calibrate the BBT.NONLOCAL model, you can specify the values of effective mass used in above equations. User can set the values of effective mass used in using ME.TUNNEL and MH.TUNNEL on the MATERIAL statement respectively. Unlike the case for tunneling in a single material, it is not possible to develop a simplified closed form expression for tunneling across the hetero-interface between two semiconductors by assuming constant electric field. Depending on the extent of overlap between energy bands the tunneling path may be entirely in one material or traversing through both materials [22]. The case where the electron travels through both materials corresponds to the smallest effective energy gap ($E_{g,eff}$) and largest tunneling probability. For this case, the valance and conduction band effective mass and energy gap of both materials needs to be taken into account in the ATLAS device specification. In general, the tunneling current must be calculated non-locally by a slight modification of the WKB framework mentioned previously over the entire energy band overlap [125]. All tunneling paths, need fine meshing, each with possibly different $E_{g,eff,}$ must be considered. The I_{ds}-V_{gs} characterstics of the lighter doped source is undesirable. However, the I_{ds}-V_{gs} of the moderately doped 5×10^{19} cm^{-3} and above case is very desirable [120]. A very steep slope is observed over many decades of current. For these heavier doped segments, because the condition for overlap is larger, the electric field at the overlap condition is also larger. This results in a sudden and rapid increase in current as tunneling is permitted from the overlap of the conduction and valance band of an already “thin” tunnel barrier. In the lighter doped segments, the electric field is not very large resulting in very little jump in current. This steep swing behavior over many

decades of current is called the “sudden overlap” effect [119-120]. This results from the presence of the energy gap, which permits the tunneling process to be completely “turned off” when electrons in the valance band no longer have states to tunnel into on the receiving side [119]. When the band bending is less than the band gap the tunnel current is zero. Once bands are overlapped, the transistor swing is determined by modulation of the tunnel probability with gate voltage, which is seen not very steep.

4.4 Comparison of MOSFET Architectures

By using 2-D Quantum mechanical simulations including field-induced Quantum confinement together with semiclassical simulations including mobility models, Kao *et al.* investigated that a TFET with a TFET configuration exhibits a steeper SS and a higher ON-current than the TFET that exhibits only lateral BTBT [130]. All Si vertical TFET with (111) tunneling orientation and optimized counter-doped pockets had shown better performance than tunneling along (100) orientation [130]. The counter-doped pockets underneath the gate–source overlap decrease the quantum confinement, which is a potential source of variability, and prevent the steep subthreshold slope from lateral BTBT degradation. It was reported that this also reduces the variability associated with the gate alignment as well as the oxide thickness limitation [130]. The optimal gate–channel overlap was found to be dependent on the specific capacitance and current requirements, with an increasing overlap resulting in an enhanced ON-current in the channel-resistance-limited current regime [130].

However, homojunction embodiment using a narrow bandgap may have difficulties satisfying a low OFF-state leakage criterion [131]. As pointed out in [132], although BTB tunneling may be sufficiently suppressed, leakage current due to thermal generation, proportional to $e^{-(E_g/nKT)}$, dominates the OFF-state current and limits the on–off ratio to a few hundreds due to the small E_g used. With these considerations, staggered heterojunction were employed as the source–channel junction in our TFET design [131]. High on-current of 78 μA/μm in a TFET had been reported at 0.5 V drain voltage at room temperature [133], with TFET employing a staggered AlGaSb/InAs heterojunction with the tunneling direction oriented in-line with the gate field [133].

The structure of the n-type Si/SiGe heterojunction vertical Tunnel FET [127] is shown in Fig. 4.3c and reported earlier work [127, 122]. Prior work of using a delta doped SiGe layer was reported for enhanced tunneling [128]. The gate-stack is placed on the top of a highly doped p+ SiGe source capped with a thin intrinsic silicon pocket layer. There is no overlap of the gate with the drain since overlap result in the further depletion of channel region [134]. The source and the drain regions are separated by a nominally undoped Si channel. Under the application of the gate bias, a potential well is formed in the conduction band of the pocket, which leads to energy quantization. If the lowest sub-band in the conduction band of the pocket region aligns with the valence band of the SiGe source underneath, the tunneling of electrons starts uniformly in the entire pocket region below the gate. The magnitude of the tunneling current is determined by the position of the Fermi level in the source and the pocket which depends on the doping concentration in the source, the pocket, and the value of the gate and the drain biases. Once in the conduction band, the electrons are collected by the drain under the application of a drain bias. The salient features of this structure [123-125] can be listed as follows:

(a) boost in the tunneling efficiency attributable to the alignment of the tunneling direction to the gate electric field.

(b) steep turn ON attributable to simultaneous tunneling across the entire tunneling distance/length [127] with gate field from the source to the drain in the OFF state and to the pocket in the ON state, and a suppressed point tunneling [125] by avoiding overlap of the gate with the intrinsic region separating the source and the drain.

(c) the tunneling current is expected to be proportional to the gate length (until a certain gate length determined by the parasitic resistances [120]);

(d) the small tunneling distance attributable to the small bandgap of the SiGe source;

(e) the OFF current is independent of the gate length;

(f) the suppressed ambipolar behavior attributable to the gate underlap at the drain side.

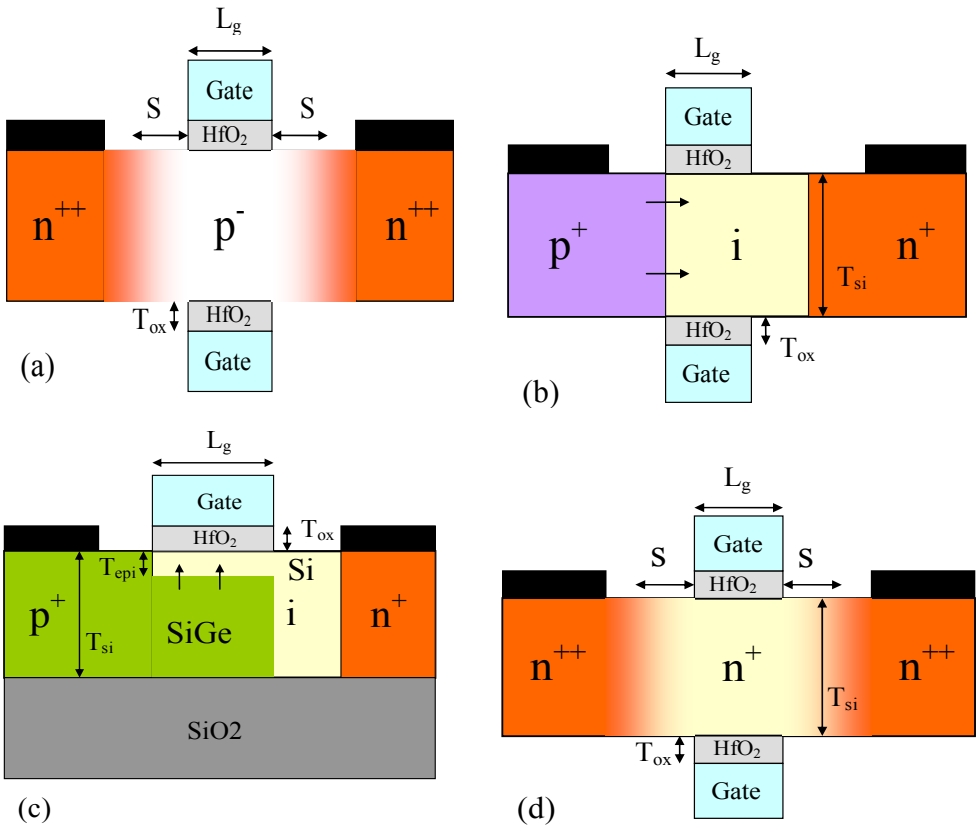

Fig. 4.3 Schematic diagram of (a) undelap inversion-mode, (b) Lateral (L)TFET, (c) Vertical (V)TFET and (d) Junctionless (JL) MOSFET. Solid arrow indicates tunneling direction for electrons (c).

Although different FET architectures such as junctionless, underlap inversion mode, Lateral TFET and Vertical TFET [119-125] (fig. 4.3 *a-d*) have shown suppressed short channel effects (SCEs) and improved switching at lower current drives, there are not many results available for their analog/RF comparison [137]. An improved g_m/I_{ds} ratio, a two-order of magnitude higher output resistance and an order of magnitude higher gain, in spite of an order of magnitude lower g_m, had been demonstrated in past for a DG lateral TFET of 10-nm-thick silicon body as compared with a DG MOSFET of similar dimensions and circuits implementations have also been reported [134-135]. MOSFETs are analyzed (fig. 4.4 *a*) with ATLAS simulator [22] using Lombardi mobility model [28] and non-local Hurkx band-to-band tunneling model (TFETs [120-121, 136]) with device parameters as given in Table 4.1. The transfer characteristics of TFETs are compared with available experimental data published in the literature for nMOS and pMOS TFETs [124-125] (fig. 4.4 *b-c*). As the focus is on ULP operation the

devices have been compared for the current ranging from 0.1 to 10 μA/μm. Low-κ spacer and high-κ gate dielectric design for Lateral TFET proposes a solution to solve the ambipolar character of TFETs [121]. The physical distance between the gate and the drain (i.e., the spacer) introduces an underlap between the gate and the drain, increasing the tunneling distance and decreasing the undesired ambipolar tunneling current.

Parameters	INV	LTFET	VTFET
L_g (nm), V_{ds} (V)	20, 0.5		
T_{ox} (nm)	3 nm HfO_2 ($\kappa = 21$)		
T_{si}, T_{epi} (nm), Ge mole (%)	10, NA		10, 2, 30
Source doping ($x10^{20}$ cm^{-3})	(N_d) 5	(N_a) 2	(N_a) 1
Channel doping ($x10^{17}cm^{-3}$)	(N_d) 0.01	(N_d) 1	
Drain doping ($x10^{20}$ cm^{-3})	(N_d) 5	(N_d) 0.2	(N_d) 1

Table 4.1 Simulation parameters. JL device has channel doping as $N_d = 10^{18}$ cm^{-3}.

For vertical TFET, if Ge concentration x is increased in $Si_{1-x}Ge_x$, its bandgap reduces, which in turn increases the carrier tunneling rate, hereby reducing the voltage to get a certain amount of carriers. A thinner epitaxial layer/pocket, for a fixed 30% Ge content, depletes completely in comparison with a thicker one [123]. In this case, a higher gate voltage is required to invert the epi layer. As epitaxial layer thickness is increased, tunnel width decreases and I_{ON} increases. Anymore increase in the thickness, however, degrades I_{ON} again, because the thicker epitaxial layer reduces gate control over tunnel junction. The conductivity of region beneath spacers is modulated by fringing field through spacer coupling after the devices turns on. At low values of dielectric constant, such as SiO_2 ($\kappa = 3.9$), higher epi resistance limits the current.

In this section a performance comparison of the optimized inversion-mode underlap device, optimized junctionless and tunnel FETs (fig. 4.3 *a-d*) for ultra low power applications is presented with the help of analog/RF metrics. Device parameters are as mentioned in Table 4.1.

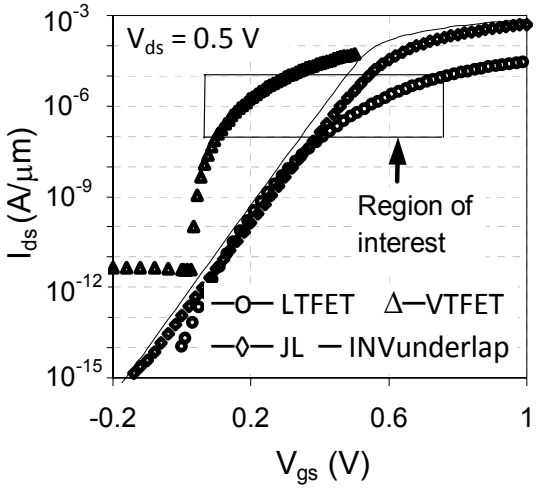

Fig. 4.4. I_{ds}-V_{gs} characterstics for INV underlap, JL, LTFET and VTFET simulated devices.

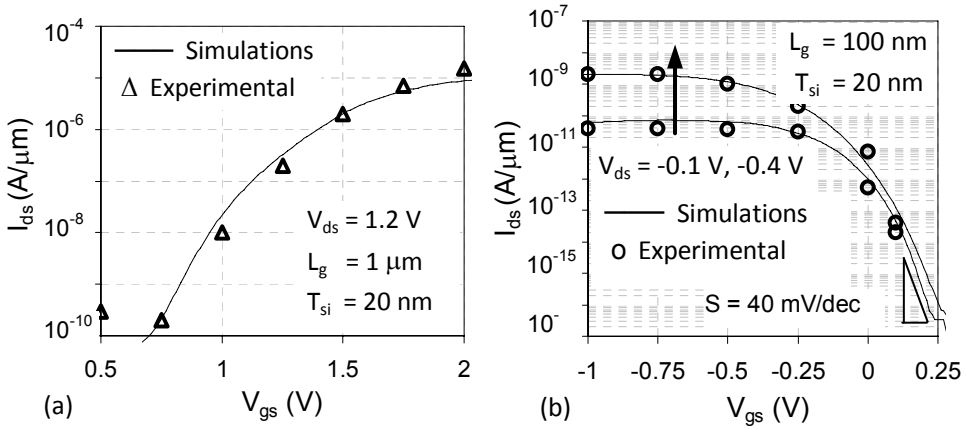

Fig. 4.5. Comparison with experimental results of (a) Vertical TFET [125], and (b) Lateral TFET [126]. Notations are same as in fig. 4.4.

Employing a high-κ material mitigates this effect until it is again limited by tunnel junction resistance. The I_{off} does not have a strong dependence on spacer κ. At I_{ds} of 10 μA/μm (fig. 4.6 *a*-*b*). junctionless and inversion-mode underlap devices exhibits f_T of 200 GHz which is 15× higher than that achieved by TFETs (7-9 GHz). A_{VO} for junctionless, inversion-mode underlap and Vertical TFET device is 35 to 45 dB which is 3 times higher than exhibited by Lateral TFET (15 dB). A lower transconductance (g_m) is expected in TFETs due to high tunneling junction resistance and lower current [119]. At the centre of channel, 5 nm below Si-oxide interface, optimized (steep

switching [120, 122]) lateral TFET and vertical TFET exhibit mobility of 20 and 5 cm^2/Vsec, respectively.

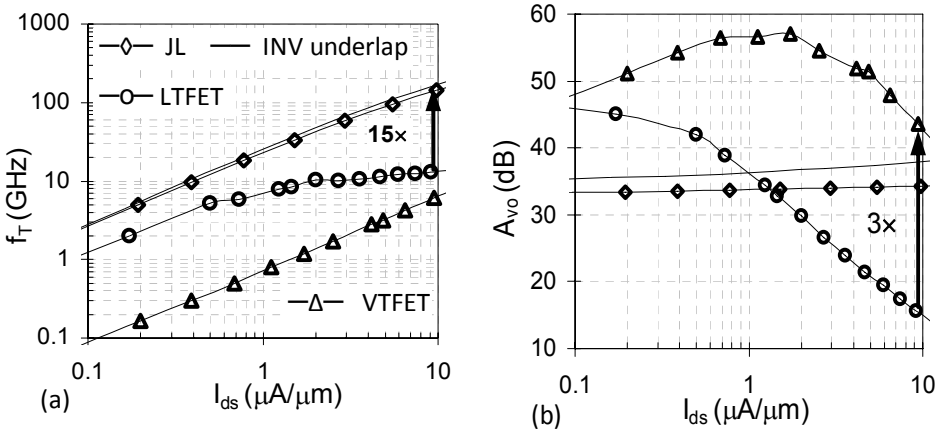

Fig. 4.6. Dependence of (a) f_T, (b) A_{VO} on drain current (I_{ds}) for the devices.

Underlap region and location of channel at the centre of film reduces SCEs and results in lower mobility (due to vertical field) in inversion-mode and junctionless devices. Reduction of SCEs results in longer effective channel length and higher mobility (≈ 230 cm^2/Vsec at the centre of film) resulting in twice and 10× higher g_m than LTFET and VTFET at I_{ds} = 10 μA/μm (fig. 4.6 *c*).

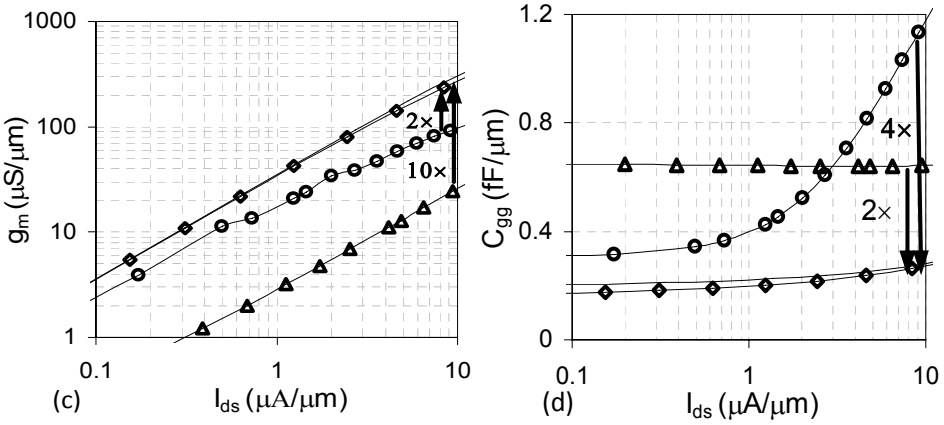

Fig. 4.6. Dependence of (c) g_m, and (d) C_{gg} on drain current (I_{ds}) for the devices. Notations are same as in fig. 4.4.

Total gate capacitance (C_{gg}) of JL and INV underlap device (≈ 0.35 fF/μm) is 4 times lower than LTFET (1.17 fF/μm) and 2 times lower than VTFET (0.7 fF/μm) (fig.

4.6 *d*). Significant proportion of charges are provided by drain in LTFET [122] and drain field influences band bending (fig. 4.7 *a*) which results in high gate-to-drain capacitance (C_{gd}) and C_{gg} values, with lower gate-to-source capacitance C_{gs}. On the contrary, VTFET exhibits higher C_{gs} due to enhanced tunneling but lower C_{gd} as channel potential is not effected by drain (fig. 4.7 *a*) [123-125]. Lower C_{gg} for JL and INV underlap devices is due to the reduction of inner fringing capacitance. Lower C_{gg} (≈ 0.35 fF/μm), off-state current (fig. 4.5 *a*) and higher f_T of 10 to 30 GHz, exhibited by LTFET, JL and INV underlap devices at even lower I_{ds} of 0.1μA/μm indicates their usefulness as ULP analog/RF transistors.

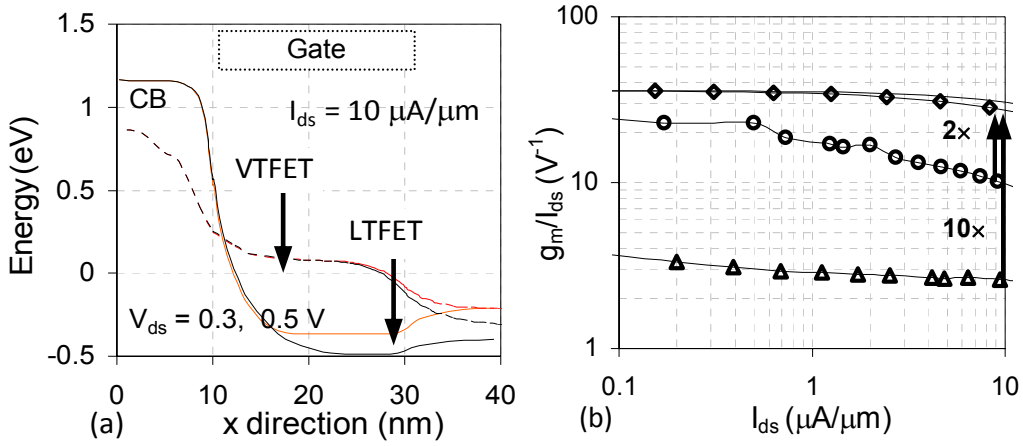

Fig. 4.7 (a) Energy band variation for TFET. CB - conduction band (b) Dependence of g_m/I_{ds} on I_{ds}. Notations are same as in fig. 4.4.

Transconductance generation efficiency (g_m/I_{ds}) (fig. 4.7 *b*) for INV underlap and JL devices is found to be 25 and 30 V^{-1} which is 10× and twice higher than VTFET (2.5 V^{-1}) and LTFET (10 V^{-1}) due to lower g_m values. Simulataneous improvement in g_m/I_{ds} and f_T for underlap INV and JL devices signifies the balance achieved between power efficiency and bandwidth useful in ULP circuits like operational transconductance amplifiers (OTAs). Although specifically ultra low power front-end analog/RF amplifiers with simpler bandwidth requirements may employ tunnel FET as basic buliding blocks and utilize the high-gain provided by such devices. Early voltage (V_{EA}) is 60 V for VTFET at I_{ds} = 10 μA/μm, 15 times higher than that for JL and INV devices (≈3 V) and "2 order" higher than LTFET (fig. 4.8 *a*), and indicating supressed SCEs. This is due to reduced influence of drain field on band bending and tunneling (fig. 4.7 *a*

and 4.8 *b*) and results in high gain (A_{VO} = g_m/I_{ds} x V_{EA}) for VTFET over the entire current range, inspite of a degraded g_m/I_{ds}. JL and INV underlap exhibit moderatly high V_{EA} and A_{VO}, due to reduced drain electric field provided by underlap effect (fig. 4.8 *b*). LTFET exhibits low V_{EA} and gain beyond I_{ds} = 1μA/μm.

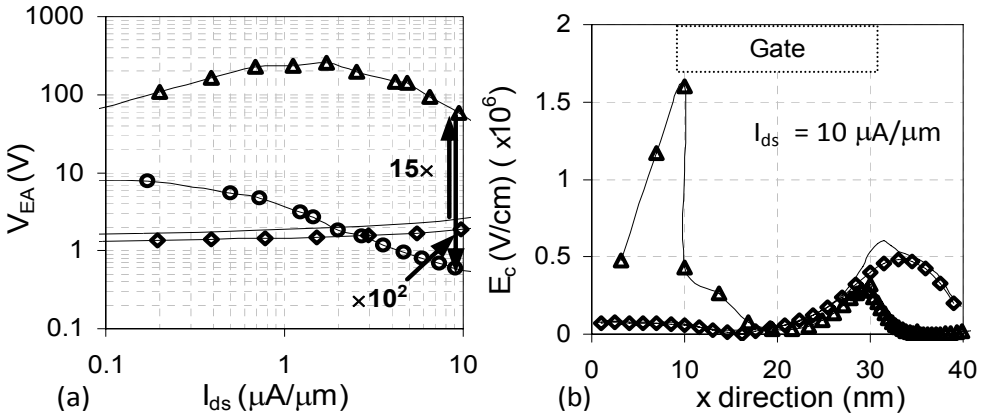

Fig. 4.8. (a) Dependence of V_{EA} on I_{ds} and (b) Electric field along the channel direction (*x*).

4.5 Conclusions

These results clearly showed that TFET structures with appropriate current levels and analog/RF performance can fulfill the requirements of high volage gain at voltages even below 0.5 V. Although the main degrading factor for analog/RF performance of TFETs is their large parasitic capacitance due to off-state tunneling of carriers which also contribute to the leakage current. TFETs will be useful in high-gain ULP circuits with limited bandwidth requirement. Carefully designed vertical tunneling transistors can potentially enable 0.1V ICs [138]. High current and low voltage operation needs small effective band gap energy which may be provided by heterojunctions of Si/Ge or compound semiconductors [132-133, 138]. In practice, the tunnel-junction bias and the junction electric field are coupled and cannot be engineered independently [138].

Chapter 5

Conclusion

While considerable effort has gone to benchmark emerging MOS devices for low power logic applications, the emerging MOSFETs are required to be evaluated for the suitability for analog/RF applications instead of adopting the "as is" structure as proposed for digital applications. Therefore, the emerging low power transistor architectures such as inversion mode MOSFETs, junctionless MOSFET and tunnel FETs are selected as focus of the research work primarily concentrated on the design and suitability of the innovative structures for analog/RF applications along with an assessment of the advantages and challenges presented by each transistor topology through well calibrated device simulations. The thesis work presents a detailed analysis of analog/RF performance metrics of different MOSFET architectures. Conclusions related to different aspects of the work are summarized below.

5.1 Summary

It has been shown in chapter 2 that Source/Drain profile engineering offers a way forward for scaling down of low power analog/RF devices. Underlap inversion-mode devices should be designed with $s/\sigma = 3$ or $s/d \cong 8$ for achieving enhanced performance metrics. Biasing the low power device within 10% of peak-$g_m f_T/I_{ds}$ not only provides substantial gain in terms of g_m/I_{ds} and f_T, but also improves linearity.

In chapter 3, it is shown that at a drain current (I_{ds}) of 10 μA/μm, junctionless (JL) devices achieve 2× higher values of cut–off frequency (f_T) and maximum oscillation frequency (f_{MAX}) along with 65% improvement in voltage gain (A_{VO}) in comparison to conventional non–underlap inversion-mode MOSFETs. It has been reported in chapter 2 that the doping dependence of RF performance metrics of junctionless transistors and compare the same with conventional undoped inversion mode MOSFETs. It is demonstrated that at low drive currents (~ m), JL transistors outperform inversion mode MOSFETs as 20% to 40% higher values of cut-off frequency is obtained for different doping concentrations (10^{19} to 3×10^{19} cm^{-3}).

This thesis reports on the significance of reducing channel doping and optimizing the spacer width to enhance analog/RF metrics. The low power analog/RF performance of junctionless transistors can be significantly enhanced by reducing the channel doping from 10^{19} cm^{-3} to 10^{18} cm^{-3} and by engineering the spacer width. Another advantage of optimized junctionless devices is the improvement in gain-bandwidth trade-off around the analog sweet spot. Despite the high doping concentration ($\cong 10^{18}$ cm^{-3}) junctionless devices do not show severe degradation in analog/RF performance metrics when compared with undoped inversion mode devices. Sensitivity of optimized junctionless devices is also found superior than conventional heavily doped ($N_d = 10^{19}$ cm^{-3}) junctionless transistors. It is shown that the junctionless device architecture is advantageous for ultra low power RF applications as parasitic capacitances are significantly reduced. Scaling trends for cut-off frequency (at lower drain currents) with respect to gate length highlights the potential of junctionless architecture for ultra low power applications.

Finally, in chapter 4, this work analyzes and compares the analog/RF performance metrics of different ULP MOSFET architectures and quantify the advantages and challenges associated with underlap inversion-mode, junctionless, lateral tunnel FET and vertical tunnel FET in terms of gain and bandwidth. TFETs will be useful in high-gain ULP circuits with limited bandwidth requirement. Underlap INV and JL devices, achieving balance between gain and bandwidth and avoiding steep junctions, are most suitable architecture for ULP analog/RF applications. For operation at lower current levels (subthreshold region), these devices should be designed with wider spacers (1.5 × gate length) and lower channel doping ($N_d = 10^{18}$ cm^{-3}) to facilitate the lateral extension of depletion depth which enhances gate controllability and reduces fringing capacitances.

5.2 Recommendations of Future work

CMOS modeling is one of the most active research areas due to its performance impact on future's high frequency ICs. Device performance at high frequencies needs to be fully understood. The intent of this thesis is to better understand the performance issues

in novel device architectures as proposed solution for decananometer analog/RF CMOS. Although the results do provide design insights, still other physical phenomena need to be addressed like trap defects present in ultra-thin SOI tunnel FETs which may affect leakage current, tunneling current and parasitic capacitances. Another study may focus on finFET/3dimensional lateral tunnel FET with the SOI implementation. CMOS modeling remains one of the most active research areas due to its performance impact on future's high frequency ICs. Device performance at high frequencies needs to be fully understood and modeled correctly [4, 106]. Compact model development of these novel MOSFET architectures with inclusion of effects like quantum confinement, carrier scattering and quasi-saturation which result in nonlinear channel resistance and loss of gate controllability, will aid RF circuit designers. However, the impact of RF performance due to the process variations is not much studied and understood. Characterizing the performance variation is equally important for mass production environment for consumer ICs.

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