INVESTIGATION OF DRAIN EXTENSION FEATURE IN A DOUBLE-GATE SILICON BASED TUNNEL FET FOR LOW POWER SoC APPLICATIONS

Ph.D. Thesis

By

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INVESTIGATION OF DRAIN EXTENSION FEATURE IN A DOUBLE-GATE SILICON BASED TUNNEL FET FOR LOW POWER SoC APPLICATIONS

A THESIS

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled "**INVESTIGATION OF DRAIN EXTENSION FEATURE IN A DOUBLE-GATE SILICON BASED TUNNEL FET FOR LOW POWER SoC APPLICATIONS"** in the partial fulfillment of the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY** and submitted in the **DISCIPLINE OF ELECTRICAL ENGINEERING, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from January 2012 to February 2016 under the supervision of Dr. Santosh Kumar Vishvakarma, Assistant Professor, Indian Institute of Technology Indore, India.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

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This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

Signature of Thesis Supervisor with date
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Dedicated to my parents

Abstract

The conventional metal oxide semiconductor field effect transistor (MOSFET) is approaching the scaling limit because of its subthreshold slope (*SS*), governed by thermionic emission-carrier diffusion over a thermal barrier being limited to 60 mV/decade at room temperature. This limitation is challenging for supply voltages below 1 V because of incremental short channel effects (*SCEs*) and leakage currents making it unsuitable for analog/RF applications. This generates a necessity for the ultralow power and energy-efficient transistor with *SS* below 60 mV/decade for future generation of integrated circuits (IC). Therefore, the tunnel field-effect transistor (TFET) is being explored as an attractive alternative to the MOSFET for low-power applications. Unlike MOSFETs, TFETs are not limited by the thermionic emission constraint since the carrier injection from source to channel in the TFET is by tunneling, which could provide SS lower than 60 mV/decade limits of the conventional MOSFETs. This enables low standby leakage currents and further scaling of supply voltage (V_{dd}) and makes it suitable for low power system on chip (SoC) applications which contains analog/RF and digital blocks. Due to different conduction concept, the sensitivity of the TFET's analog/RF characteristics to the variation in the technology parameter will be different as compared to conventional MOSFETs. Therefore, there is need to characterize the novel device for analog/RF performance before placing into the SoC design. In this way my research topic entitled "investigation of drain extension feature in a double gate Silicon tunnel FET for low power SoC applications" dedicate to investigate TFET performance for various device engineering and to unfold analog/RF behavior.

For this purpose, we present lateral asymmetric drain (*LAD*) doping effect on a double gate tunnel field-effect transistor (DG-TFET) and its influence on device RF performances. The *LAD* doping profile improves technological issues such as suppresses the ambipolar behavior, improves OFF-state current, and reduces the gate–drain capacitance. Along with that, this addition of *LAD* doping in the drain extension region also improves RF figures of merit. Further, the lateral abruptness effect for different gate lengths is also checked by ac small-signal simulation to provide more insights related to the influence of lateral abruptness on RF performance. The result demonstrates the feasibility of lateral asymmetric drain as a way to improve the RF figures of merit for low-power design application significantly.

Further we, follow the influence of *LAD* doping on RF performance, present the effect of its variation in DG-TFET reliability and its impact on analog/RF characteristics. For this, we report a quantitative understanding of the effect of drain extension with LAD doping and its variation on ambipolarity as well as also present the impact of LAD doping effect on DG-TFET performance. Apart from this, the analog/RF

figure of merit and delay analysis are also performed for drain extension length variation (L_{extd}) and compared with DG-FET behavior.

Finally, we have demonstrated the influence of gate-drain underlap (*UL*), and different dielectric material for spacer and gate oxide on DG-TFET and its analog/RF performance for low power application. Here it is found that the drive current behaviour in DG-TFET with UL feature while using a different dielectric material for spacer is different in comparison to that of DG-FET. Further, the UL based hetro gate DG-TFET with low-k spacer (LK HGDG-TFET) is more resistive for drain induced barrier lowering (DIBL) as compared to DG-TFET with low-k spacer (LK DG-TFET). Our results also suggest that LK HGDG-TFET with gate-drain UL feature can be potential candidate for RF use.

This investigation, which is made by numerical simulation, would be beneficial for a new generation of RF circuits and systems in a broad range of applications and operating frequencies covering RF spectrum. In addition, the results can be useful to other researchers for the development of robust compact models for analog/RF parameters. In a developing field where experimental results are still limited, these simulations can even be essential, since they allow the variation of a large number of parameters in a short amount of time. In this way, the work presented here can further our understanding of this emerging device, and can contribute to the progress made in future Tunnel FET fabrication and model development.

List of Patent & Publications

Patent (1)

1. Vijayvargiya V. and Vishvakarma S. K. (2016), Improved performance of DG-TFET with lateral asymmetric channel (LAC) doping profile and underlap (UL) feature, Application No. 1290/21-03/2016, filed on 18th January, 2016.

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1. Vijayvargiya V. and Vishvakarma S.K. (2014), Effect of drain doping profile on double gate tunnel field effect transistor and its influence on device RF performance, IEEE Transactions on Nanotechnology, vol. 13, no. 5, pp. 974-981. DOI:10.1109/TNANO.2014.2336812
2. Vijayvargiya V. and Vishvakarma S.K. (2016), Analog/RF Performance attributes of an underlap tunnel field effect transistor for low power applications, IET Electronics Letters, vol. 52, no. 7, pp. 559-560.
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4. Vijayvargiya V. and Vishvakarma S.K. (2016), Impact of drain parasitic in n-channel DG-TFET with LAD doping on DC and Analog/RF characteristics, International journal of electronics, Taylor & Franceis, Under Review.
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4. Singh G., Vijayvargiya V. and Vishvakarma S.K. (2015), Investigation of underlap and spacer engineering in multigate-MOSFET for improved short channel characteristics at 14 nm, Proceedings of 18th International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India.

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List of Abbreviations and Symbols

TFET	:Tunnel Field Effect Transistor
FET	: Field Effect Transistor
DG	: Double Gate
SS	: Subthreshold Swing
I_{on}	: ON-state Current
I_{amb}	: Ambipolar Current
MOSFET	: Metal Oxide Semiconductor Field Effect Transistor
MuGFET	: Multiple Gate MOSFET
SCEs	: Short Channel Effects
DIBL	: Drain Induced Barrier Lowering
RF	: Radio Frequency
SoC	: System on Chip
ε_0	: Permittivity of Vacuum
ε_{Si}	: Relative Permittivity of Silicon
ε_{ox}	: Relative permittivity of Gate Insulator
t_{ox}	: Oxide Thickness
W	: Device Width of Silicon for DG-TFET
L	: Channel Length of Silicon for DG-TFET
t_{Si}	: Silicon Thickness for DG-TFET
k	: Boltzmann Constant
T	: Temperature
q	: Electron Charge
V_{th}	: Thermal Voltage
V_{gs}	: Gate to Source Voltage
V_{ds}	: Drain to Source Voltage
C_{gs}	: Gate to Source Capacitance
C_{gd}	: Gate to Drain Capacitance
C_{gg}	: Gate to Gate Capacitance
LAD	: Lateral Asymmetric Drain

L_{extd}	: Source-Drain Extension Length
UL	: Underlap Length
HG	: Hetro-Gate
HK	: High-k Dielectric
g_m	: Transconductance
g_d	: Conductance
R_{dcr}	: Distributed Channel Resistance
f_T	:Cut-off Frequency
f_{max}	:Maximum Oscillation Frequency
GBW	: Gain Bandwidth Product

Chapter 1

Introduction

The first transistor was presented at the Bell laboratories by Willian Shockley, John Bardeen and Walter Brattain in December 1947. In 65 years, the semiconductor technology has developed with an amazing speed. The semiconductor industry's workhorse technology is silicon complementary metal oxide semiconductor (CMOS) and the building block of CMOS is the metal oxide semiconductor field effect transistor (MOSFET). Nowadays, MOSFETs are aggressively scaled down to put the MOS devices into nanometer regime. The aim of scaling is to increase the transistor density on chip and consequently increases number of functionality to perform the operation. This is the needed for today's portable device such as smart phone and electronic gadgets. Along with that, reduction in device capacitance with scaling not only increases the speed of devices but also improves analog/RF performance and radio frequency reached into gigahertz (GHz)[1–3] as well. In spite of these improvements, MOS devices face two severe problem in nanometer dimension such as short channel effects (SCEs) and power dissipation [4], [5].

1.1 MOSFET Development and Limitations for Analog/RF Performance

1.1.1 MOS Device Issues in Nanometer Dimension

As the dimensions of transistors are shrunk, the performances of transistor have been drastically improved. However, the single gate bulk MOSFET is almost at the end of the roadmap as scaling the close proximity between source and drain reduces the capability of gate electrode to control the potential distribution and the bulk-silicon transistor is facing serious issues such as SCEs that start plaguing the bulk MOSFET technology [6]. The main short channel effects are threshold voltage roll off (due to charge sharing), degradation of subthreshold swing and drain induced barrier lowering (DIBL) effects. As a result, the OFF state current increases and the ON-OFF current ratio degrades[7], [8] which also causes degradation in analog/RF characteristics. Therefore, the device performance was worsened and for all practical purposes, it seems further impossible to scale the dimensions of classical bulk MOSFETs. So, it seems to replace the bulk single gate MOSFET by changing device architecture or device engineering for nanoscale MOSFETs[9], [10].

1.1.2 Multigate MOSFETs

The multigate MOSFETs have a strong potential to extend the CMOS scaling into the sub-25nm regime[11]. They offer superior electrostatic control of channel due to multiple gates that suppress SCEs and leakage current. The lightly doped channel also helps to alleviate several other problems related to nanoscale MOSFETs, e.g. mobility degradation random dopant fluctuation, and compatibility with mid-gap material gate etc. The use of strained silicon, a metal gate and high- k dielectric as gate insulator can further enhance the current drive of the device. The natural length can be reduced by decreasing the gate oxide thickness, by using high-k gate dielectric instead of SiO_2. The circuit performance also benefits from novel gate stack material, reduced parasitic capacitance and hole mobility improvement. Therefore, the MuGFETs are strong candidates for replacing conventional single gate MOSFET in future[7], [10–12].

1.1.3 Device Engineering in MOSFET

When MOS devices are scaled down in nanometer dimension, the device engineers have also introduced device engineering concept to minimize SCEs and improve further analog/RF performances. The reported device engineering are channel engineering[13], [14], underlap (UL) architecture with Source/Drain extension length (SDE)[15], [16] and spacer engineering [16], [17].

In channel engineering, asymmetric channel doping profile[13–15], [18–22] is used in the channel region. In asymmetric doping profile, high doping concentration is near the source side in the channel region as compare to drain side. This reduces SCEs and also improves analog/RF performance due to reduction in overall gate capacitance. In nanometer dimension, SDE are used rather than schotky contact to simulate the device in order to include source/drain parasitic effects. it is also reported that parasitic capacitance is going to be dominating factor as compare channel capacitance. Therefore, in order to reduce parasitic capacitance, underlap feature has been introduced in the source/drain extension region. The UL is the length between metallurgical source-channel/drain-channel junctions to starting edge of doping segregation length in source/drain region. This architecture also improves digital performance due to reduction in parasitic capacitances. However the UL feature induces parasitic resistance causes decrease in ON-state current (*Ion*) and degrade analog/RF performance. Due to this reason, researcher have introduced trade-off between parasitic with minimum delay to get the optimum RF performance [15], [23]. Further, one of the researcher used high-k dielectric material for the spacer to increase the fringe coupling between gate electrode and UL and reduce the parasitic resistance. Despite of higher fringing capacitance, this architecture has shown its suitability for improving the analog/RF in subthreshold region [16]. In order to reduce fringing capacitance,

pal et al.[17] has also proposed dual-k spacer based architecture and have shown improvement in digital performance at 14 nm technology node for tri-gate based field effect transistor. The aim of device engineering concept is to improve device performance in terms of improvement in ON-state current (I_{on}), I_{on}/I_{off}, subthreshold swing (SS) and SCEs, and along with this improved performance parameter, the device capability for analog/RF and digital performance will also improve. Also, the optimized device will give better performance with less power consumption in circuitry. However, the power consumption is going to be the biggest issue in sub-nanometer dimension [17][4], [17], [24–26] when the device is used for system on chip (SoC) design.

1.1.4 Power Consumption Issue in MOSFET

The most important consequence of supply voltage (V_{dd}) reducing during device scaling while threshold voltage (V_T) reduces significantly less, is that the gate overdrive (V_{dd}-V_T) goes down. When gate overdrive decreases, on-current decreases, which negatively affects device performance, the I_{on}/I_{off} ratio, and dynamic speed (C_gV_{dd}/I_{on}). There are two possible solutions to this problem of needing a high gate overdrive: either V_{dd} can stay higher than it should with constant field scaling, or V_T can be scaled down more aggressively. Both of these options, and their repercussions, will be discussed.

In order to maintain acceptable levels of gate overdrive, V_{dd} scaling has slowed down drastically. When the supply voltage decreases along with device dimensions, then the power density $I_{on}V_{dd}/A$ (on-current times supply voltage divided by surface area) remains constant, which means that the energy needed to drive the chip, and the heat produced by the chip, remain constant. This assumes that when devices scale down, we don't see chip size decreasing, but rather, more complexity and functionality is added with each generation, and chip size remains more or less constant.

The power consumption in SoC design can be categorized in two parts namely dynamic power consumption and static power consumption. When V_{dd} doesn't scale down, power density increases instead. For each MOSFET, the dynamic and static power consumption can be expressed as [27].

$$P_{dynamic} = C_{total}(V_{dd})^2 f \tag{1.1}$$

where f is the frequency and C_{total} is the total switched capacitive load, and

$$P_{static} = I_{leak}V_{dd} \tag{1.2}$$

where I_{leak} is the sum of the leakage currents in the device when the MOSFET is in the off-state.

If V_{dd} does not decrease, and yet device dimensions decrease, and more devices are added to a chip such that chip size is not significantly reduced, then it can be expected that power consumption will rise considerably. The discussion up until now has not explained why static power would be increasing much faster than dynamic power, and that comes back to the second option for keeping a

high gate overdrive: scaling down V_T. Static power consumption is related with the power consumption when circuit is performing logic operation corresponding to inputs but is not in switching state and used device continuously consumes power from the supply voltage. The power consumption is also referred as leakage power consumption. The power consumption is going to be dominating factor over dynamic power consumption especially below 0.5 V of supply voltage[25]. The following factors are responsible for leakage power consumptions as shown in Fig. 1.1

- Junction Leakage (I_1)
- Subthreshold Leakage (I_2)
- Oxide tunneling and Hot carrier injection (I_3 I_4)
- Gate-Induced Drain Leakage (I_5)
- Channel Punch through current (I_6)

These leakage current components can be minimized by optimizing device through device engineering concept along with multigate structures. However, subthershold leakage is going to be limiting factor

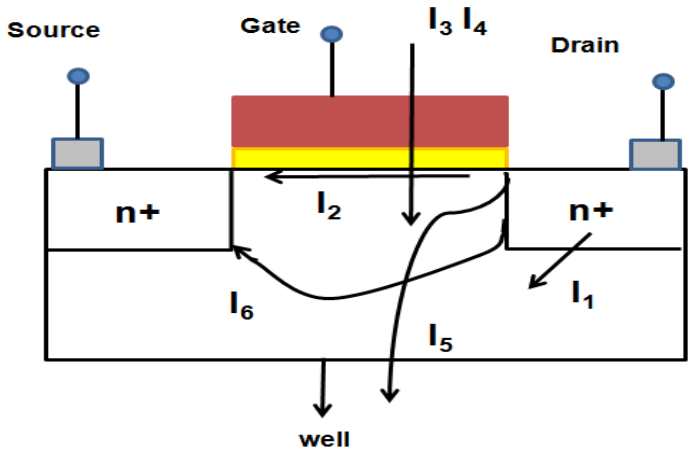


Figure. 1.1. n-channel conventional MOSFET with leakage current components [4].

for MOSFET technology below 0.5 V of supply voltage scalling due to MOS conduction concept [25] which causes subthreshold swing limitation.

1.1.5 MOSFET Limitations

Fig. 1.2 (a) shows the energy band-diagram of long channel n-MOSFET in OFF state. There is large energy barrier exist between source and channel when the device in OFF state corresponding to the I_{off} current in fig. 1.2 (b). As gate voltage increases consequently drain current increases. This is due to the energy barrier between source and channel reduces causes electrons in the source conduction band thermally injected into the channel conduction band through diffusion process reaches towards drain side. The electron concentration at the surface of channel region becomes equal to majority carrier

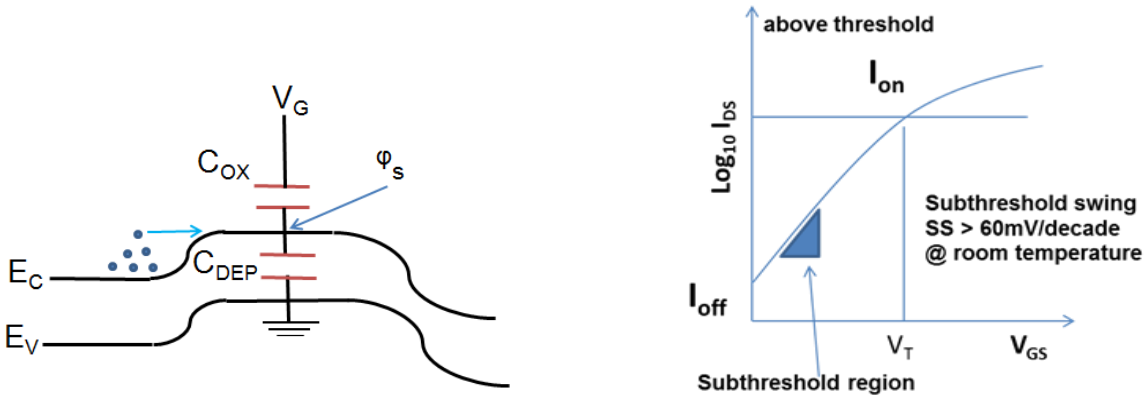


Figure 1.2. For n-channel MOSFET (a) Equivalent energy band diagram model (b) transfer characteristics[27], [28].

concentration of channel when the gate voltage reaches at threshold voltage corresponding to ON-state current as shown in fig. 1.2(b). Here, subthreshold region which exists between OFF voltage to threshold voltage, is responsible for subthreshold leakage current. This region also measures the capability of MOSFET for digital performance in terms of subthreshold swing (SS). The SS defines how effectively transistor can be turned on or turned off. It is modelled by following equation [27], [28]

$$SS = \frac{dV_g}{d\left(\log_{10} I_d\right)} \tag{1.3}$$

$$\cong \ln(10)\frac{kT}{q}\left(1+\frac{C_{dep}}{C_{ox}}+\frac{C_{ss}}{C_{ox}}\right) \tag{1.4}$$

For ideal MOSFET $C_{ox} = \infty$,

$$\rightarrow \frac{kT}{q}\ln(10) \cong 60mV/dec \tag{1.5}$$

where V_g is the gate voltage, I_d is the drain current, kT/q is the thermal voltage, and C_{dep} and C_{ox} are the depletion and the oxide capacitance respectively. SS value becomes 60 mV/decade at room temperature when C_{ox} is infinite for ideal case of MOSFET. This outcome reflects that at least 60 mV of gate voltage required to change the drain current by one order of magnitude when the transistor is operated in the subthreshold region. The Subthreshold swing limitation of MOSFETs becomes limiting factor[4], [25], [26] for further scaling of supply voltage below 0.5 V.

Another way of reducing the voltage supply without performance loss is to reduce the voltage required to turn on the device which means decreasing the average subthreshold swing defined as [25]

$$SS_{avg} = \frac{V_T - V_{G,OFF}}{\log\left(\frac{I_{on}}{I_{off}}\right)} \approx \frac{V_{dd}}{\log\left(\frac{I_{on}}{I_{off}}\right)} \tag{1.6}$$

Therefore devices with a steep SS called steep slope switches, are expected to enable V_{dd} scaling. Fig. 1.3(a) shows transfer characteristics of a MOSFET switch showing an exponential increase in OFF-state current because of an incompressible subthreshold swing (SS). Here the simultaneous scaling down of both the supply voltage (V_{dd}) and threshold voltage (V_T), maintain the same performance (ON-state) by keeping the overdrive voltage (V_{dd} -V_T) constant. It was reported that OFF-state current increases more than tenfold increase for every 60 mV scaling of V_{dd} at room temperature [5], [25], [27–29].

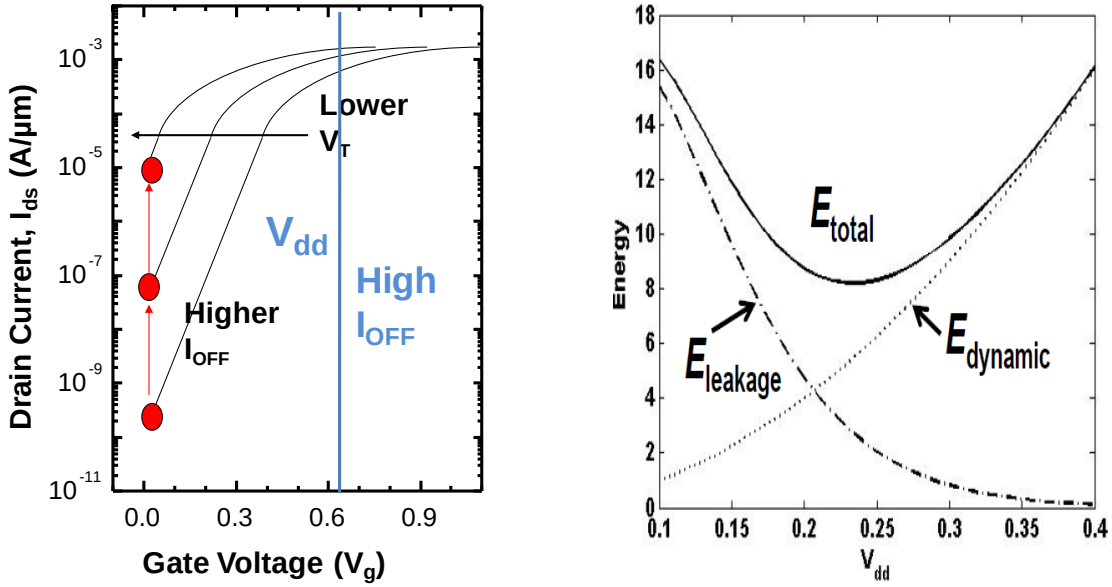


Figure 1.3. (a) Transfer characteristics of a MOSFET with V_{dd} and V_T scaling (b) Characteristics of minimum switching energy and the corresponding supply voltage for ideal MOSFET.[25]

The energy efficiency of a logic operation can be evaluated by analysing its switching energy diagram as shown in fig.1.3 (b). It shows total switching energy required per cycle with supply voltage scaling for ideal MOSFET (SS=60 mV/dec). Here, total energy consists of dynamic energy and leakage energy[25], [28]. The energy required per cycle for performing digital operation reaches its minimum value when supply voltage approaches 0.25 V to 0.3 V. After this range, required total energy per cycle increases exponentially. This is mainly due to the exponentially increases of the subthreshold leakage (OFF-state current) with V_{dd} scaling.

Therefore this analysis concludes that SS limitation of MOSFET forces to quest new energy efficient device conduction concept which do not have SS limitations and able to create new minima for total energy per cycle.

1.2 Tunnel Field Effect Transistor (TFET)

The tunnel field-effect transistor (TFET) is being explored as an attractive alternative to the MOSFET for low-power applications. Unlike MOSFETs, TFETs are not limited by the thermionic emission constraint since the carrier injection from source to channel in the TFET is by tunneling, which could provide *SS* lower than 60 mV/decade limits of the conventional MOSFETs [5], [25], [26], [28–33]. This enables low standby leakage currents and further scaling of supply voltage (V_{dd}).

1.2.1 Realization of Tunnel FET and Working

The TFET is merely a gated p-i-n diode operating under reverse bias. The drain is always biased with positive voltage to make sure the operation takes place in the reverse bias for gated p-i-n diode. In order to be steady with MOSFET technology, the names of the device terminals are chosen such that voltages are applied in a similar way for tunnel FET operation. The NMOS transistor operates when positive voltages are applied to the drain and gate. In n-type tunnel FET, n-region is referred to as its drain, and p+ region as its source.

Fig. 1.4 shows the device structure for a double gate p-i-n Tunnel FET. The structure shown is an n-type device, with a p+ source and an n+ drain. In a p-type Tunnel FET, the source would be doped n+ and the drain would be doped p+. All Tunnel FETs shown in this thesis have double gate with different device engineering.

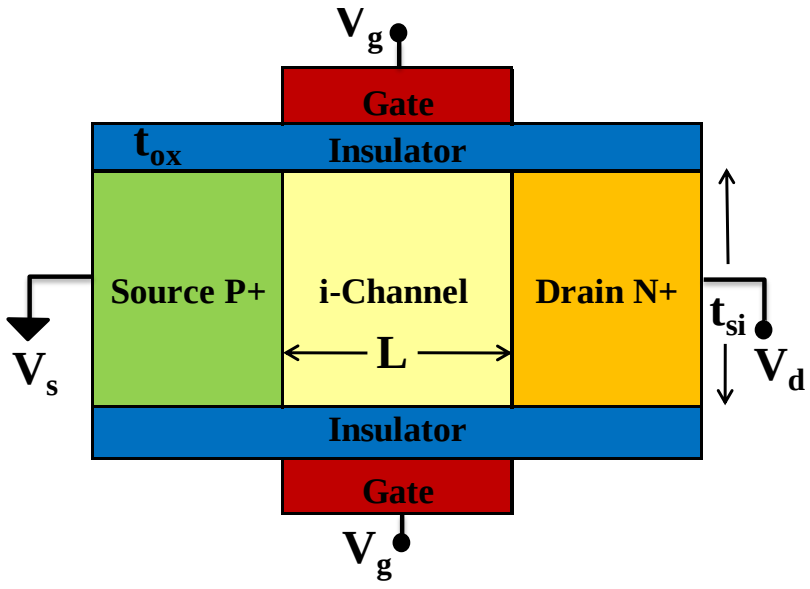


Figure 1.4. n-channel Tunnel FET device structure with double gate (DG).

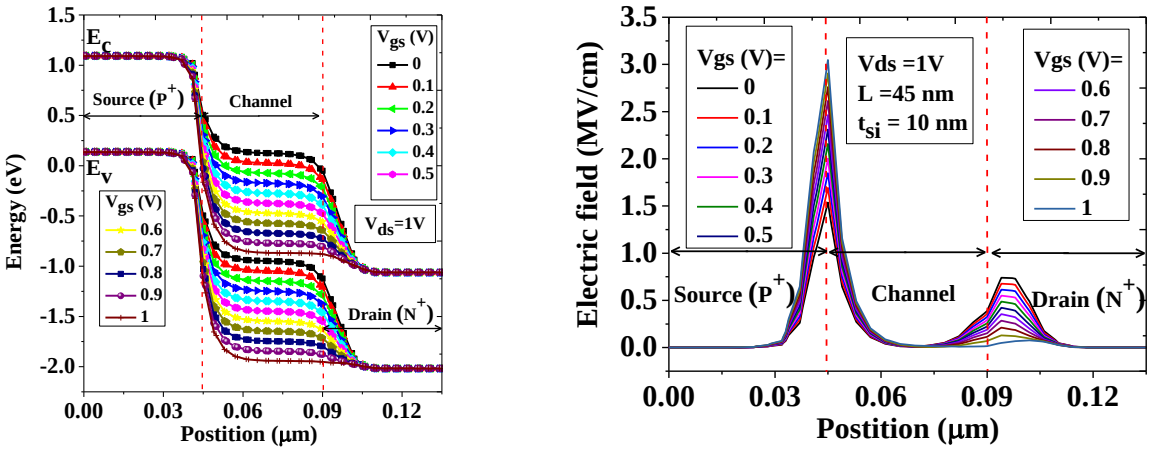


Figure 1.5. For n-channel Tunnel FET (a) Energy band diagrams with gate voltage variation. (b) Electric field with gate voltage variation.

The investigated device structure for changing doping profile at the drain side is the DG-TFET. The operation of the band-to- band TFET is based on the variation of the position of the band-gap of the channel part relative to the energy levels of the source and drain. Fig. 1.5 (a) shows the energy band diagram with gate voltage variation in step of 0.1 V for the *n*-channel DG-TFET. This figure shows both OFF and ON states of TFET device depending upon the gate voltage application. The Energy band diagrams have been taken horizontally across the *n*-channel DG-TFET at a distance of 1 nm from the surface.

In Tunnel FET OFF state, if the gate bias is low ($V_{gs} \leq 0$V), no tunneling occurs because the potential barrier between the source and the channel is large. only p-i-n diode leakage current flows between the source and drain, and this current can be extremely low (less than a fA/μm).Here, off-state voltage (V_{off}) is the minimum value of gate-to source (V_{gs}) voltage when the drain current (I_d) shows a minimum than after $V_{gs} \leq V_{off}$ V start tunneling from drain to channel.

On the other hand in the ON state, when positive voltage is applied on the gate, as the gate voltage increases pulls down the energy band of the channel region and reduces the width of the tunneling barrier. The electric field at source-channel junction increases with the variation of energy bands as shown in fig. 1.5(b). Due to the reduction in energy barrier, carriers can tunnel from the valence band of the source at the source–channel interface to the conduction band of the channel (drain) region, and thus, forming the tunneling current. The ON-current of an n-type Tunnel FET depends on the width of the energy barrier between the intrinsic and p+ regions, and the current increases exponentially with a reduction in this barrier width although the barrier width starts to saturate at high V_{gs}[32] .

1.2.2 WKB approximation for Band to band tunneling

Band to band tunneling in tunnel FET through tunneling barrier can be approximated by a triangular potential barrier as shown in fig. 1.6 with the WKB [25], [28] approximation, the band to band tunneling transmission is given by

$$T_{WKB} \approx \exp\left[-2\int_{-X_1}^{X_2} |k(x)|dx\right] \tag{1.7}$$

where k(x) is the quantum wave vector of the electron inside the barrier. Inside a triangular barrier, the wave vector is

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}(PE - E)} \tag{1.8}$$

Here, PE is the potential energy, and E is the energy of incoming electron energy at the widest part of triangle where E=0 and PE can be $E_g/2 - qE_X$ replaced by the equation for the triangle. Here E_g is the band gap of the semiconductor material at the tunnel junction and E_X is the electric field.

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}\left(\frac{E_g}{2} - qE_X\right)} \tag{1.9}$$

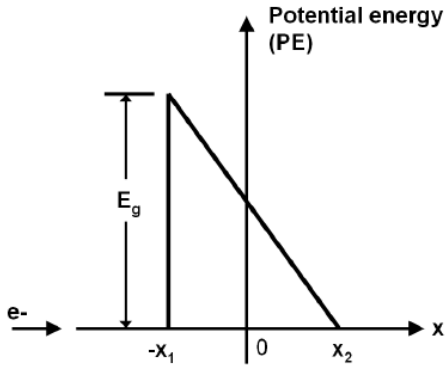


Figure 1.6. Triangular potential energy barrier approximation for band to band tunneling in Tunnel FET[32].

On putting this equation in (1.7) and give the general expression for band to band tunneling transmissions

$$T_{WKB} \approx \exp\left(\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3qh(E_g + \Delta\Phi)}\right) \tag{1.10}$$

Where m^* is the effective mass and E_g is band gap of the material, $\Delta\phi$ is the energy range over which tunneling can take place. Here λ is the screening tunneling length, it depends on device geometry. The expression for a double gate device is[8], [11], [12].

$$\lambda = \sqrt{\frac{\varepsilon_{si} t_{si} t_{ox}}{2\varepsilon_{ox}}} \tag{1.11}$$

Where ε_{si} and t_{si} are the dielectric permittivity and thickness of the silicon and ε_{ox} and t_{ox} are the dielectric permittivity and thickness of the gate dielectric.

1.2.3 Attributes and Issues of Tunnel FET

One challenge in TFET operation is to realize high ON-state current because ON-state current depends on the transmission probability of the inter-band tunneling barrier. The tunneling probability can be calculated by WKB approximation, as given in previous subsection. To realize high tunneling current, the transmission probability of the source tunneling barrier should become close to unity for small change in gate voltage. It indicates, a high transparency of the tunneling barrier is required. The WKB approximation, shown in equation (1) suggests that the band-gap (Eg), the effective carrier mass (m*) and screening tunneling length (λ) should be minimized for high barrier transparency.

The Tunnel FET is an ambipolar device[25], [32], [34–36], it also conducts for $V_{gs} \leq V_{off}$ with band to band tunneling (BTBT) occurring at metallurgical drain channel junction. Here, OFF-state voltage (V_{off}) is the minimum value of gate-to-source (V_{gs}) voltage when the drain current (I_d) shows a minimum value than after $V_{gs} \leq V_{off}$ starts tunneling from drain to channel. This ambipolar behaviour is not desirable in circuit design.

As explained earlier, that in the OFF-state, no empty states are available in the channel for tunneling from the source. When positive voltage is applied on the gate, the gate voltage pulls down the energy band of the channel region as shown in fig. 1.5(a). The inter-band tunneling starts when bottom of the conduction band in the channel aligns with top of the valance band in the source. Most importantly, this switch the device to the ON-state, only for energy window ΔΦ as explained in WKB approximation in the previous subsection. This is mainly due to the electron in the tail of the Fermi distribution cannot tunnel because no empty states are available in the channel as their energy. This filtering function makes TFET possible to achieve an SS of below 60 mV/dec. Unlike MOSFET, SS in a TFET is not linear on a logarithmic scale and highly depends on the applied gate-to-source voltage. This is mainly due to the tunneling current depends on the transmission probability through the barrier as well as on the number of available states determined by the source and channel Fermi functions. The SS of tunnel FET is modelled by following equation [36]

$$SS_{TFET} = \frac{V_{gs}^2}{5.75\left(V_{gs} + Const\right)} mV/dec \tag{1.12}$$

This model equation (1.12) suggests that the subthreshold region does not appear as a linear line when I_{ds}-V_{gs} is plotted on a log scale as shown in fig. 1.7, and the SS does not have one unique value. SS is smallest at the lowest V_{gs}, and increases as V_{gs} increases. Tunnel FET has two type of SS considered in the literature such as point swing and average swing due to nonlinear behaviour in the subthreshold region. Point swing is the smallest value of the subthreshold swing anywhere on the I_{ds}-V_{gs} curve and average swing is taken from the point where the device starts to turn on, up to threshold, often defined using the constant current technique.

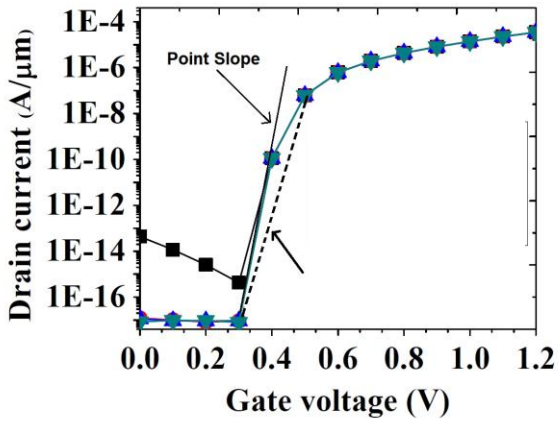


Figure 1.7. Different consideration of subthreshold swing for the Tunnel FET.

Unlike MOSFET, gate capacitance formation of TFET is different in ON-state, this is one more important feature of TFET[7]. It was reported for a MOSFET, operating in the linear region, both source/drain regions are connected to the inversion layer and gate capacitance is equally contributed by gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}). In saturation region, C_{gg} is dominated by C_{gs}. However in TFET, the drain is connected to the inversion layer. Therefore, C_{gd} constitutes a larger fraction of C_{gg} in both linear and saturation regions.

Another issue with TFET which leads to an increase of the off-current is the presence of trap states within the bandgap [33-34]. These states located at the junction impact the tunneling process. Typical kinds of traps are lattice point-defects which are caused by ion implantation damage. The relatively low activation temperature that was used does not heal all the lattice damage by crystal re-growth, so we assume there are a high number of defects in the implanted area that can act as traps. Traps in the source can be occupied by an electron due to the thermal broadening of the Fermi function. Electrons can tunnel from these traps directly into the valence band of the channel even for very low V_{ds} when no gate voltage V_{gs} is applied and the bands of source and drain are not aligned. At lower temperatures these states are not occupied and do not contribute to the off-current, thus I_{off} decreases for lower temperatures. These traps states within the exponential Fermi tail contribute to the current flow, and thus they degrade the slope.

1.3 Outline of Thesis

The tunnel field-effect transistor (TFET) is being explored as an attractive alternative to the MOSFET for low-power SoC applications. In this thesis, we have investigated drain extension feature in a double gate silicon tunnel FET for low power SoC application. The thesis is organized in seven chapters.

Chapter 2 contains the review of past works in TFET. Here, considerable effort has been given on TFET technological issues and how these issues has been solved by various TFET device engineering techniques. This chapter also contains the literature which helped in defining the objective of the thesis and perform TFET device investigation for analog/RF characteristics for low power SoC design.

In chapter 3, we have analyzed the effects of uniform and Gaussian drain doping on RF performances of the DG-TFET for ultralow-power applications. For this, the ambipolar behavior with different drain doping profiles (uniform and Gaussian) along with high density n-type impurity layer near to source end is investigated. Further, I_{on}/I_{off} ratio and *SS* as figures of merit for low standby power application have been analyzed for the same. Apart from this, RF figures of merit for the DG-TFET in terms of transconductance (g_m), unit-gain cut-off frequency (f_T), maximum frequency of oscillation (f_{max}), and gain bandwidth product (*GBW*) are analyzed with lateral asymmetric drain doping profiles along with high-density layer (*HDL*) near source end. Lateral abruptness effect for different gate lengths is further enhanced by ac small-signal simulation to provide more insights related to the influence of lateral abruptness on RF performance.

Further chapter 4 follows the influence of lateral asymmetric drain (*LAD)* doping on RF performance. Here, we have investigated drain extension feature with *LAD* doping and the effect of its variation in DG-TFET reliability and its impact on analog/RF characteristics. For this, we report a quantitative understanding of the effect of drain extension with LAD doping and its variation on ambipolarity as well as also present the impact of LAD doping effect on DG-TFET performance. Apart from this, the analog/RF figure of merit and delay analysis are also performed for drain extension length variation (L_{extd}) and compared with DG-FET behavior.

In chapter 5, explains gate-drain underlap (UL) feature of double gate tunnel field effect transistor for analog/RF characteristic. Here, it is found that parasitic resistance induced by gate drain UL is not significant as compared to DG-FET. Thus, the behavior of RF figure of merit (FoM) is different from DG-FET.

However, Chapter 6 is the extension of chapter 5, this chapter explain the influence of gate-drain underlap (UL) and different dielectric material for spacer and gate oxide on DG-TFET (double gate TFET) and its analog/RF performance for low power application. Here, we have studied the underlap condition be studied under practically matched ON-state current condition with DG-FET such that channel resistance is same. Here, the results demonstrate that the drive current behavior in DG-TFET with UL feature while using a different dielectric material for spacer is different in comparison to that of DG-FET. Further, the UL based hetero gate DG-TFET with low-k spacer (LK HGDG-TFET) is more resistive for drain induced barrier lowering (DIBL) as compared to DG-TFET with low-k spacer (LK DG-TFET). Along with that, as compare to DG-FET, this chapter also analyses the attributes of UL and dielectric material on analog/RF performance of DG-TFET. Outcome of the results also suggest that LK HGDG-TFET with gate-drain UL feature is a potential candidate for improvement the RF performance of device.

Chapter 7 contains the conclusions and discuss possible future work

Chapter 2

Review of Past Works and Problem Formulation

The conventional MOSFET is approaching the scaling limit because of its subthreshold slope (*SS*) limited to 60 mV/decade at room temperature as explained in the chapter 1. This causes limitation is challenging for supply voltages below 1 V because of increased short channel effects and leakage currents [4], [25], making it unsuitable for analog/RF applications. This generates a necessity for the low power and energy-efficient transistor with *SS* below 60 mV/decade for future generation of SoC integrated circuits.

Therefore this chapter contains the review of past works in TFET. Here, considerable effort has been given on TFET technological issues and how these issues have been solved by various TFET device engineering techniques. This chapter also contains the literature which helped in defining the objective of the thesis and perform TFET device investigation for analog/RF characteristics for low power SoC design.

2.1 Device Engineering in Tunnel FET

The tunnel field effect transistor (TFET) is being explored as an attractive alternative to the MOSFET for low-power applications. Unlike MOSFETs, TFETs are not limited by the thermionic emission constraint since the carrier injection from source to channel in the TFET is by tunneling, which could provide *SS* lower than 60 mV/decade limits of the conventional MOSFETs [4], [5], [25], [29], [30], [32], [35], [37]. This enables low standby leakage currents and allows further scaling of supply voltage (V_{dd}). The physics of the TFET conduction concept is different when compare to conventional MOSFET. It is, therefore, likely that the sensitivity of the device's characteristics to the variation in the technology parameter will differ too, which can introduce new technological challenges. Boucart *et al.* [32] predicted that the TFET performance will be much less sensitive to doping fluctuations and gate length scaling than in the conventional MOSFET. The major hurdles in the TFET operation are low I_{on} current, ambipolar behavior and high gate-drain capacitance as reported in the literature[25], [38–41]. Apart from these drawbacks, K. Boucart *et al.*, reported that drain current is strongly affected by drain voltage which causes severe drain induced barrier lowering (DIBL) to limit the application of the tunneling device for low power SoC design.

A high ON-state current (I_{on}) requires a high transparency of the tunneling barrier; WKB equation as shown in (2.1) suggests optimized TFET design approaches to boost the I_{on}.

$$T_{WKB} \approx \exp\left(\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3qh\left(E_g + \Delta\Phi\right)}\right) \tag{2.1}$$

The goal for the TFET optimization are to simultaneously achieve the highest possible I_{on}, lowest SS_{avg} over many orders of magnitude of drain current, and the lowest possible OFF current (I_{off}). The WKB approximation, suggests that the band-gap (E_g) and the effective carrier mass (m*) depend solely on the material system and screening tunneling length (λ) is strongly influenced by several parameters, such as the device geometry, dimensions, gate capacitance, and doping profiles [25], [28]. The abruptness of the doping profile at the tunnel junction is also important. To minimize the tunneling barrier, high source doping level must fall off to the intrinsic channel in as short a width as possible. Optimizing the source–channel doping as mentioned above, the ON-state current has been reported to improve dramatically with the use of double-gate architecture along with a high-k gate dielectric [32]. This is mainly due to high-k dielectric improves electric coupling between the gate electrode and tunneling junction due to the increased gate capacitance. To get further improvement in ON-state current, *C. Anghel et al.,* [38] proposed low-k spacer with high-k gate dielectric structure. In this structure ON-state current is improved due to the non-depletion of source on the gate side which causes more tunneling current flows on the surface as compared to high-k spacer. However, investigation of drain doping on the device performance is also important. Few researchers have also worked theoretically as well as experimentally, on device engineering concept such as hetro gate dielectric[40], [42] and gate engineering and have investigated to improve device performance in terms of ON-state current, ambipolar behaviour and gate-drain capacitance as compared to DG-TFET with high-k gate dielectric or low-k gate dielectric. Further, gate-drain underlap[32], [35] as well as asymmetric source/drain doping in extension region has been reported to mitigate TFET ambipolar behaviour.

It was also reported that unlike MOSFET, the gate capacitance of TFET at inversion is dominated by gate-drain capacitance (C_{gd}) than gate-source capacitance (C_{gs})[43]. Due to high C_{gd}, TFET suffers from miller effect and limit its utility for SoC design containing digital, analog and RF circuit blocks. Therefore, drain design is also important along with source doping optimization. Apart from that, very few researchers have worked on various TFET devices for analog/RF design for low power SoC design [44], [45]. However, the tunneling device should be optimized to unfold the device behavior against device engineering for getting optimum analog/RF performance before placing the device for SoC design.

2.2 Objective

The above literature on TFET was given with the motivation to work on research topic

"investigation of drain extension feature in a double gate silicon tunnel FET for low power SoC application". As stated earlier that TFET conduction is based on band to band tunneling and thus it is an alternative of MOSFETs for low voltage and low power system on chip (SoC) applications. The SoC design contains analog/RF and digital blocks. Due to different conduction concept, the sensitivity of the TFET's analog/RF characteristics to the variation in the technology parameter will be different from that of conventional MOSFETs. Therefore, there is need to characterize the novel device for analog/RF performance before placing it into the SoC design. This is why I have dedicated my research to investigate TFET performance to unfold it analog/RF behaviour for application in device engineering.

2.3 Methodology

2.3.1 TCAD for Novel Devices

Technology computer aided design (TCAD) tool uses process and device simulators. It appies numerical derivations based on complex equations such as partial differential equations to predict the behavior of the device. ATHENA is a process simulator which predicts the structures generated from specified process sequences (oxidation, diffusion and ion implantation) based on the physics and chemistry of the semiconductor processes.

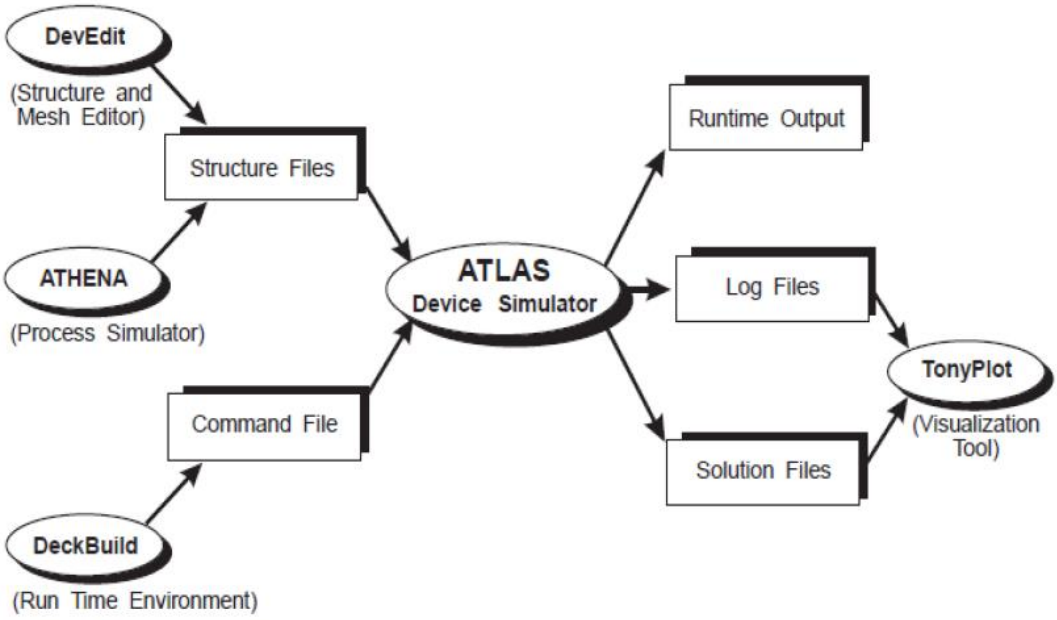


Figure 2.1: ATLAS device simulator input and output flow.

In this work, we have used 2D ATLAS [46] as a TCAD for device simulation and verification. ATLAS is a numerical device simulator. It predicts the electrical characteristics that are associated

with specified physical structures and bias conditions. This normally involves an iterative solution of Poisson's equation combined with a transport model for a given set of boundary conditions. A common way to accomplish this is by discretizing the 2D surface or 3D volume in a grid and then applying a partial differential equation solver to find solutions at the grid points in an iterative manner. The convergence and accuracy depend on the size and layout of the grid and the complexity of the applied physical models. ATLAS has wide range of models for transport, carrier statistics, material properties etc. These can be combined with the simulation of a wide range of customized 2D and 3D device geometries.

Fig. 2.1 shows the types of information that flow in and out of ATLAS. ATLAS is normally used through the DECKBUILD run-time environment, which supports both interactive and batch mode operation. Most ATLAS simulations use two inputs: a text file that contains commands for ATLAS to execute and a structure file that defines the structure to be simulated. ATLAS produces three types of outputs: The run-time output shows the execution of each ATLAS command and includes error messages, warnings, extracted parameters and other important outputs for evaluating each ATLAS run. When ATLAS is run interactively, run time output is sent to the output section of the DECKBUILD application window and can be saved as required. Log files store all terminal voltages and currents from the device analysis and the solution files store two and three dimensional data relating to the values of solution variables within the device for a single bias point.

2.3.2 Simulation Model for Tunnel FET Device

To accomplish the objective of the thesis, n-channel DG-TFET is used for investigation. The device simulations are carried out using ATLAS 2-D[46] device simulation software. In this analysis, a nonlocal model for the BTBT is employed, which is available in ATLAS[46], and also explained in the appendix part. Further, taking in account the high doping concentration in the source and the drain regions, a band-gap narrowing model is also included with other physical models such as concentration, field dependent, mobility, Shockley–Read–Hall (SRH), recombination model, and Fermi–Dirac statistics.

2.3.3 Analog/RF parameter measurement for Tunnel FET

For logic applications, maximizing the I_{on}/I_{off} ratio and minimization of gate delay is the main concern, whereas for analog/RF applications, we need to maximize transconductance generation factor (TGF), cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}). A high value of gain is always desirable, which is an indication of efficiency of the device to convert DC power and can be defined as the ratio of transconductance g_m with drain-to-source conductance g_{ds}. f_T and f_{max} can be calculated

in the conventional way, when short circuit current gain and unilateral power gain drop to unity. For that, the analog/RF figures of merit have been extracted from the *Y* parameter matrix generated by performing the small-signal ac analysis.

Using normal equivalent circuit approach, we can explore f_T and f_{max} as [1], [13], [18], [47]

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{2.2}$$

$$f_{\max} = \frac{g_m}{2\pi C_{gs}\sqrt{4\left(R_G + R_S + R_i\right)\left(g_{ds} + g_m \frac{C_{gd}}{C_{gs}}\right)}} \tag{2.3}$$

C_{gs} and C_{gd} are equal to gate-to-source and gate-to-drain capacitances, g_m and g_{ds} are equal to gate transconductance and drain-to-source conductance, and R_G, R_S and R_i are gate resistance, source and channel resistances, respectively. As shown in equation (2.2) and (2.3), f_T is dependent on the ratio of transconductance g_m and total gate capacitance C_{gg}, while f_{max} also depends on the source/drain and gate parasitic resistances.

The gate-to-drain capacitance C_{gd}, total gate capacitance C_{gg}, transconductance g_m and drain-to-source conductance g_{ds} on which gain, f_T and f_{max} strongly depend can be evaluated from imaginary and real part of admittance parameters y_{12}, y_{11}, y_{21} and y_{22}, respectively.

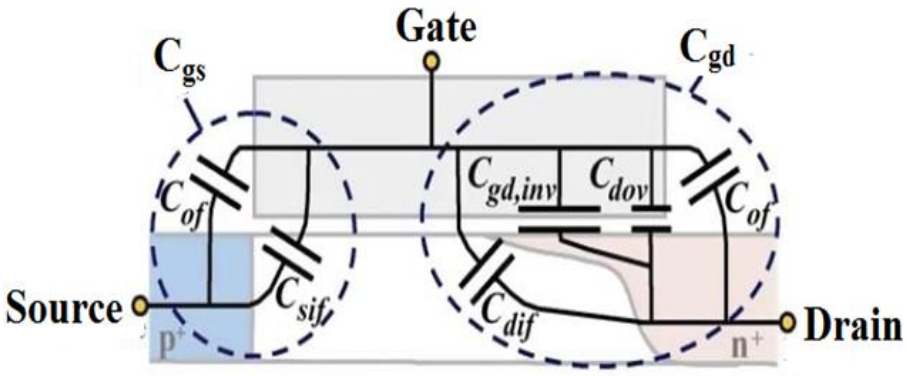


Figure 2.2: Equivalent circuit of tunnel FET with gate capacitance components [43]

Fig. 2.2 shows equivalent circuit of tunnel FET with gate capacitance components. Based on understanding of device physics and capacitance components from numerical simulation, the total capacitance (intrinsic + extrinsic) of a Tunnel FET, gate-source (C_{gs}) and gate-drain (C_{gd}) capacitance without considering overlap capacitances are calculated as

$$C_{gd} = C_{of} + C_{dif} + C_{GD,inv} \tag{2.4}$$

$$C_{gs} = C_{of} + C_{sif} \tag{2.5}$$

where C_{of} is the outer fringing capacitance, and C_{dif} and C_{sif} are the inner fringing capacitances at drain and source side, respectively, they are related to the source doping abruptness. The two fringing capacitance calculation is performed by adjusting expression reported in[13], [47], and are approximated by total input capacitance ($C_{gg} = C_{gs} + C_{gd}$), can be extracted from ac simulation as

$$C_{gg} = \left|\mathrm{Im}\left(Y_{11}+Y_{12}\right)/\omega\right| \tag{2.6}$$

where $\omega = 2\pi f0$.

We can define C_{gg} in the first order as $C_{IN} + C_{frin}$ (total fringing capacitance including external and internal fringing components). The C_{frin} can simply be identified by limiting C_{gg} at zero or negative V_{gs}.

2.4 Research Contributions

This thesis contributes to identify the analog/RF behaviour of Tunnel FET for low power applications. The research work focuses on n-channel TFET to investigate the effect of various technological parameter variations on DC and Analog/RF behaviour. The work contains the number of contributions in field of future tunnel FET for low power SoC applications. The main contributions are summarized as follows:

- We have investigated the effect of drain doping profile on a double-gate tunnel field-effect transistor (DG-TFET). It is found that lateral asymmetric drain (LAD) doping profile suppresses the ambipolar behavior, improves OFF-state current (I_{off}), and reduces the gate–drain capacitance.
- Placing the high-density layer in the channel near the source–channel junction, a reduction in the width of depletion region, improvement in ON-state current (I_{on}), and subthreshold slope are analyzed for this asymmetric drain doping.
- The LAD doping profile also improves various RF figures of merit (FoM) such as transconductance (g_m), unit-gain cut-off frequency (f_T), maximum frequency of oscillation (f_{max}), and gain bandwidth product. LAD doping effects on RF performances are also checked for the various channel length.
- We have also investigated drain extension feature with LAD doping and the effect of its variation (L_{extd}) on DG-TFET for DC and analog/RF characteristics. For this, we report a quantitative understanding of the effect of drain extension with LAD doping and its variation on ambipolarity as well as we also present the impact of LAD doping effect on DG-TFET

performance. Apart from this, the analog/RF figure of merit and delay analysis are performed for drain extension length (L_{extd}) variation and compared with DG-FET behavior.

- Further, we have also presented the influence of gate-drain UL, and different dielectric material for spacer and gate oxide on DG-TFET and its analog/RF performance for low power SoC application. Here, it is found that the drive current behavior (I_{on}) in DG-TFET with UL feature while using a different dielectric material for spacer is different in comparison to that of DG-FET.
- Finally, the UL based hetro gate DG-TFET with low-k spacer (LK HGDG-TFET) is more resistive for drain induced barrier lowering (DIBL) as compared to DG-TFET with low-k spacer (LK DG-TFET). Along with that, as compare to DG-FET, we have also studied the attributes of UL and different dielectric materials on analog/RF performance of DG-TFET. Our results also suggest that LK HGDG-TFET with gate-drain UL feature can be potential candidate for RF use.

Chapter 3

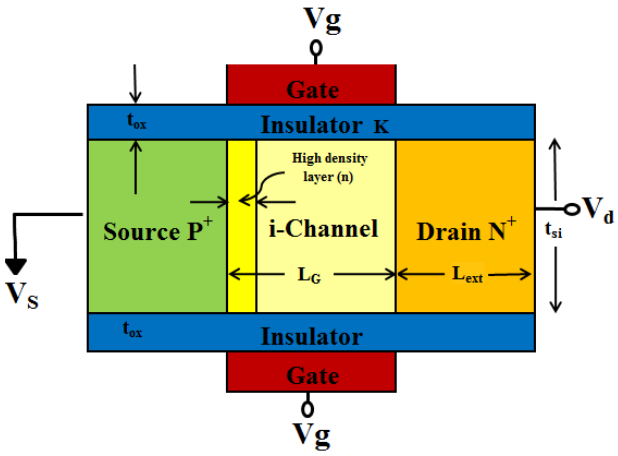
Tunnel FET with LAD Doping and its RF Performance

Asymmetric source/drain doping or lightly doped drain (LDD) engineering in TFET supress ambipolar conduction and also pocket doping in the channel region near source improves tunneling phenomena. However, Tunnel FET suffers from high gate-drain capacitance [43] due to different conduction concept as compare to conventional MOSFET. This causes degradation in RF performance consequently limit TFET device's utility for low power SoC design. It was also reported that parasitic capacitance is a dominating factor over channel capacitance in nanometer dimension. So drain design optimization is also important for improving the device performance and its RF figures of merit.

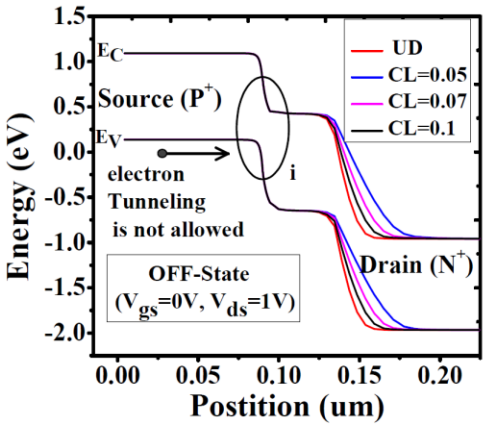
Therefore, in this chapter, the effect of drain doping profile on a double-gate tunnel field-effect transistor (DGTFET) and its radio-frequency (RF) performances are studied. It is demonstrated that the lateral asymmetric drain (LAD) doping profile suppresses the ambipolar behavior, improves OFF-state current, reduces the gate–drain capacitance, and improves the RF performance. Further, placing the high-density layer in the channel near the source–channel junction, a reduction in the width of depletion region, improvement in ON-state current (I_{on}), and subthreshold slope are analyzed for this asymmetric drain doping. However, it also improves many RF figures of merit for the DG-TFET. Furthermore, lateral asymmetric doping effects on RF performances are also checked for the various channel length. Therefore, this work would be beneficial for a new generation of RF circuits and systems in a broad range of applications and operating frequencies covering RF spectrum. So, the RF figures of merit for the DG-TFET are analyzed in terms of transconductance (g_m), unit-gain cut-off frequency (f_T), maximum frequency of oscillation (f_{max}), and gain bandwidth product.

3.1 Device Structure, Operation, and Simulation Setup

The double-gate TFET (DG-TFET) is merely a gated p-i-n diode operating under a reverse bias as shown in Fig. 3.1(a). The double-gate device under study has following parameters; slightly boron doped intrinsic channel region = $10^{17}/cm^3$, p-type source doping = $10^{20}/cm^3$, n-type drain doping = $5\times10^{18}/cm^3$. An ultrathin fully depleted n^+ pocket layer (HDL doping = $5\times10^{18}/cm^3$) inserted between the source and channel region is used to decrease the tunneling barrier width and increase the lateral electric field. This reduces the potential drop across the tunneling junction, thereby improving device performance. The source–channel junction is kept perfectly abrupt for improving the performance of the device. Silicon thickness (t_{si}) = 10nm, oxide thickness (t_{ox}) = 3nm with permittivity of high-k gate oxide insulator (K) = 21ε0, channel length (L_G) = 45nm, gate and source–drain extension length (L_{ext})



(a)



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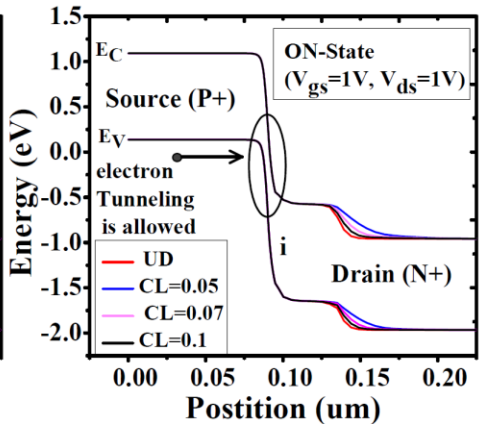

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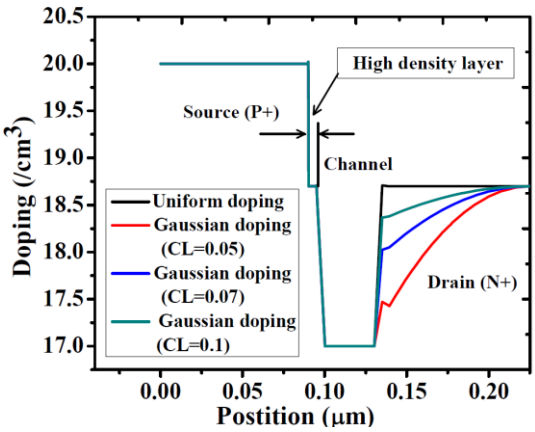

(d)

Figure 3.1. (a) Device schematic (b) Energy-band diagram of the OFF-state (c) Energy-band diagram of ON-State of n-channel DG- TFET with high density layer (d) Uniform and gaussian doping profile with different CL (Y-axis doping concentration is on $\log_{10}$ scale)

= 90nm. The device simulations are carried out using ATLAS 2-D [46] device simulation software. In this analysis, a nonlocal model for the BTBT is employed, which is available in ATLAS [46], and validated using[36]. Further, taking in account the high doping concentration in the source and the drain regions, a band gap narrowing model is also included with other physical models such as

concentration, field dependent, mobility, Shockley–Read–Hall recombination model, and Fermi–Dirac statistics. Furthermore, the analog/RF figures of merit have been extracted from the Y parameter matrix generated by performing the small-signal ac analysis.

The drain is always biased with positive voltage to make sure the operation take place in the reverse bias for gated p-i-n diode. The investigated device structure for changing doping profile at the drain side is the DG-TFET. The operation of the band-to-band TFET is based on the variation of the position of the band gap of the channel part relative to the energy levels of the source and drain. Fig. 3.1(b) and (c) shows the band diagram of the n-channel DG-TFET in OFF and ON states, respectively. Energy band diagrams have been taken horizontally across the n-channel TFET at a distance of 1 nm from the surface. In its OFF state, if the gate bias is low ($V_{gs} \leq 0V$), no tunneling occurs because the potential barrier between the source and the channel is large. Here, off-state voltage (V_{off}) is the minimum value of gate-to source (V_{gs}) voltage when the drain current (I_d) shows a minimum than after $V_{gs} \leq V_{off}$ start tunneling from drain to channel. On the other hand in the ON-state, when positive voltage is applied on the gate, the gate voltage pulls down the energy band of the channel region and reduces the width of the tunneling barrier. Due to the reduction in energy barrier, carriers can tunnel from the valence band of the source at the source–channel interface to the conduction band of the channel (drain) region, and thus, forming the tunneling current. In the following discussion, the doping profile of the drain extension regions is assumed to be Gaussian-like[46],which is expressed as

$$N(Y) = Peak.\exp\left[-\left(Y - Y_{Peak}/Y.CHAR\right)^2\right] \tag{3.1}$$

where Y.CHAR specifies the principle characteristic length (CL) of the implant. The CL is equal to the square root of twice the standard deviation. Here, the CL is taken in micro meter. Peak specifies the peak doping concentration (5×10^{18} /cm^3) at the beginning of drain extension region and then the doping concentration decreases towards the channel with CL. The TFET is an ambipolar device; it also conducts with negative gate voltage with band-to-band tunneling (BTBT) occurring at the metallurgical drain–channel junction. This ambipolar behavior is not desirable in the circuit design. In this case, the TFET for different doping profiles toward drain such as uniform doping (UD) and Gaussian doping (GD) profile with different CL is checked as shown in Fig. 1(d).

3.2 LAD Doping Effect on the DG-TFET

Fig. 3.1(d) shows UD and GD profile with different CL. Here, source doping is kept uniform throughout the source extension region as required for increasing the tunneling. Effects of UD and GD profiles in the drain extension region are checked for the TFET performance. The UD is a useful basis for comparison to explain the effects of variation in doping gradient on the TFET. In a TFET device,

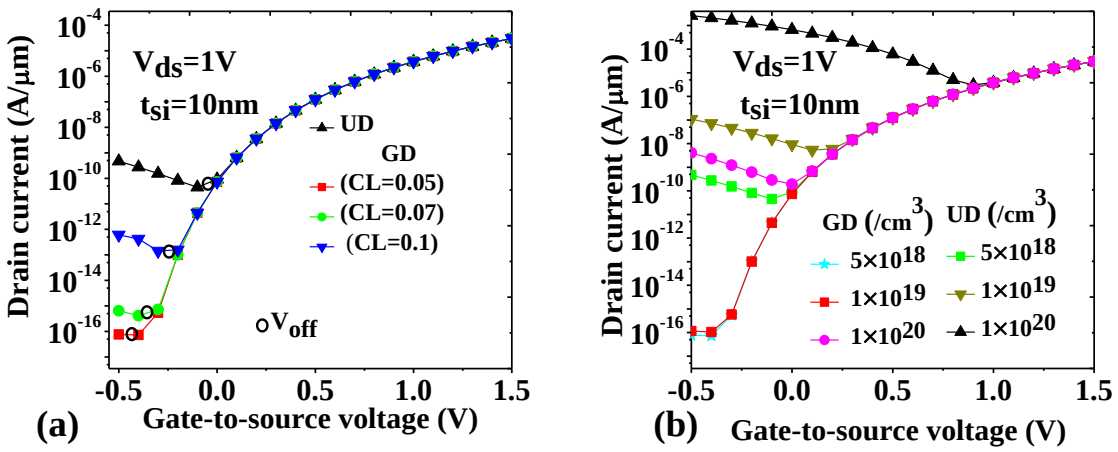

Figure 3.2. Effect of Uniform and gaussian doping profile in drain extension region (a) Shows the I_{ds}-V_{gs} characteristics for drain doping (5×10^{18} /cm^3) (b) Shows the I_{ds}-V_{gs} characteristics for varying drain doping for (CL=0.05).

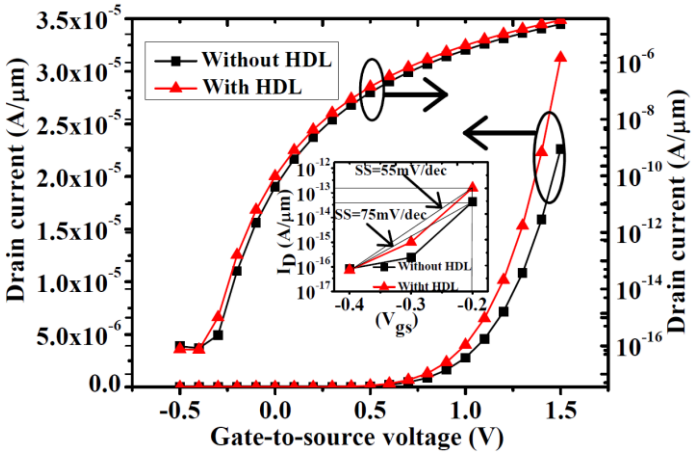

Figure 3.3. I_{ds}-V_{gs} characteristics of a double gate TFET with and without HDL.

the series resistance is distributed to tunneling barrier resistance and channel resistance. The channel resistance has a negligible influence on I_{on} since the series resistance is mostly dominated by the tunneling barrier between source and channel region [35]. In the case of the TFET with L = 45nm and GD coefficient (CL) changes from 0.1 to 0.05 has no influence on the I_{ON}, and consequently, I_{on} remains constant as shown in Fig. 3.2(a). From energy-band diagram of the OFF-state as shown in Fig. 3.1(b), it is observed that depletion width between channel and drain junction decreases with an increase in CL of doping profile, since heavily doped drain region come closer to gate edge resulting in an increase in OFF-state current as shown in Fig. 3.2(a).

The I_{ds}–V_{gs} characteristics has also been studied in the negative gate bias as shown in Fig. 3.2(b) for various drain doping and for UD and GD profile. It is shown that the tunneling of charge carriers from drain-to-channel is quite suppressed in GD profile (CL = 0.05) because of the depletion width increased at the drain junction. Ambipolar conduction is the main hurdle to use a TFET in the circuit design. The suppression of ambipolarity should be determined at the time of dc characterization

otherwise it will constitute leakage power consumption. The suppression of this back conduction (ambipolar conduction) up to some negative voltage is helpful for low-power analog /RF circuit design.

Fig. 3.3 shows the transfer characteristic of the DG-TFET with and without HDL with t_{si} = 10 nm, channel length (L_G) = 45 nm, and drain GD of CL = 0.05. From the curve, it is observed that for without HDL, SS of 75 mV/decade is achieved for three decades of drain current and drain current 4.8×10^{-8} A/μm is obtained at 0.5 V of gate voltage. However, for the TFET with HDL, SS improves 55 mV/decade for approximately four decades of drain current and drain current 1.2×10^{-7} A/μm is obtained at 0.5 V of gate voltage. Enhancement of this current and SS of the DG-TFET with HDL are due to reduction of depletion width at source–channel junction resulting in the enhancement of lateral electric field, consequently, improving the tunneling probability.

3.3 LAD Doping and HDL Effect on Analog/RF Performances

In this section, RF performances are investigated with the use of different CLs and its impact on down scaling of the channel length. The main figures of merit to evaluate RF performance are the cut-off frequency (f_T), maximum frequency of oscillation (f_{max}), and GBW. The main goal of this variation is to maximize the RF figures of merit.

3.3.1 Capacitance Characteristics with Channel Length Variation

Based on understanding of device physics and capacitance components from numerical simulation, the total capacitance (intrinsic + extrinsic) of a DG-TFET, gate–source (C_{gs}) and gate–drain (C_{gd}) capacitance without considering overlap capacitances are calculated as $C_{gd} = C_{of} + C_{dif} + C_{GD,inv}$ and $C_{gs} = C_{of} + C_{sif}$, where C_{of} is the outer fringing capacitance, and C_{dif} and C_{sif} are the inner fringing capacitances at drain and source side, respectively, they are related to the source doping abruptness. The two fringing capacitance calculation is performed by adjusting expression reported in , and are approximated by total input capacitance ($C_{gg} = C_{gs} + C_{gd}$), can be extracted from ac simulation as

$$C_{gg} = \left| \frac{|\mathrm{Im}(Y_{11} + Y_{12})|}{\omega} \right| \quad \text{Where} \quad \omega = 2\pi f_0$$

We can define C_{gg} in the first order as $C_{IN} + C_{frin}$ (total fringing capacitance including external and internal fringing components). The C_{frin} can simply be identified by limiting C_{gg} at zero or negative V_{gs}.

Fig. 3.4(a) and (b) shows the comparison of gate-to-drain capacitance (C_{gd}) and gate-to source capacitance (C_{gs}) for different V_{ds} (0.1, 0.6, and 1 V) as a function of gate-to-source voltage obtained for technology computer-aided design (TCAD) simulation for different values

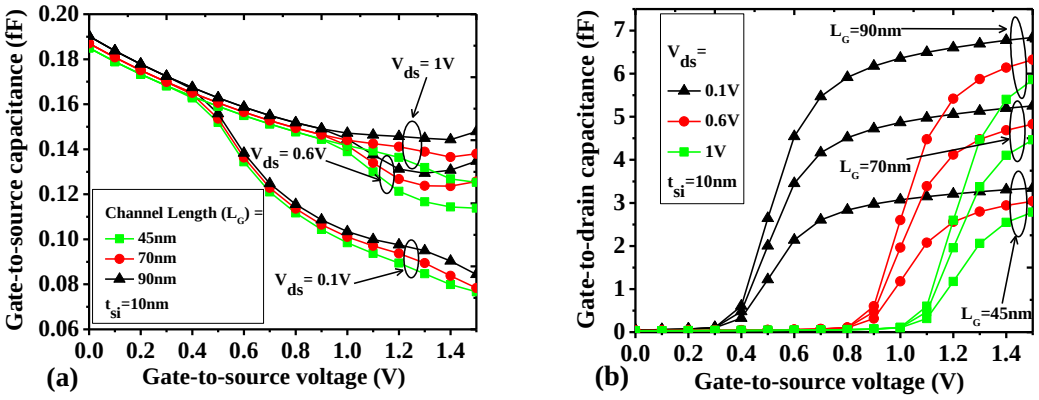

Figure 3.4. (a) Gate-to-source capacitance (C_{gs}) and (b) Gate-to-Drain capacitance (C_{gd}) as a function of gate-to-source voltage (V_{gs}) for different channel length.

of gate lengths and CL = 0.05. Before inversion occurs, gate capacitance consists of parasitic capacitance for low gate voltage. As gate-to-source (V_{gs}) voltage increases, formation of inversion takes place and it increases from inversion layer forms drain toward source below the gate dielectric for fixed drain voltage[43]. Thus, C_{gd} constitutes larger fraction of total capacitance. This is also clear from C_{gd} curve. It is also observed that with scaling of channel length C_{gd} greatly decreases. On the other hand C_{gs} consists of parasitic capacitance and it is smaller than C_{gd} and it is less dependent on gate voltage. C_{gs} drops slightly with increasing gate voltage due to screening of gate-to-source capacitance coupling of the inversion layer.

3.3.2 Transconductance

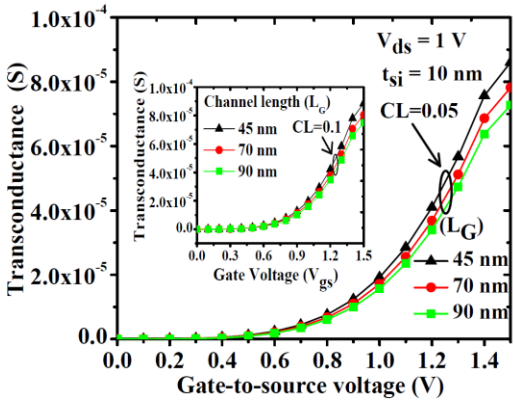

Figure 3.5. Transconductance (g_m) of Tunnel-FET as a function of gate voltage with Gaussian doping profile (different characteristics length).

Fig. 3.5 shows transconductance (g_m) as function of V_{gs}. It is observed that the transconductance of the DG-TFET does not change significantly with the variation of the channel length (from 90 to 45 nm) and drain doping profile CL change (from 0.05 to 0.1). This is because of current conduction in the TFET occurs by tunneling between source and intrinsic channel and also effective width and area for tunneling will not change by variation of the channel length [36].

3.3.3 RF Characteristics with LAD Doping

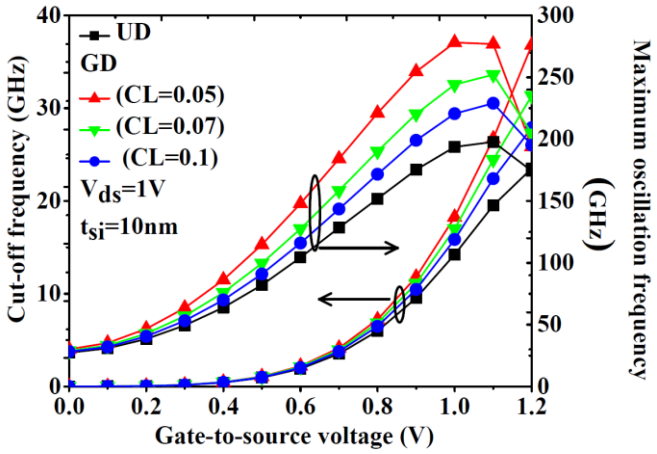

Figure 3.6. f_T and f_{max} characteristics of Tunnel-FET as a function of gate voltage with uniform and Gaussian doping profile with different characteristics length.

Fig. 3.6 shows f_T and f_{max} characteristics of the DG-TFET as a function of gate voltage with UD and GD profile (different CLs) for channel length 45 nm, extracted from the two-port Y-parameter based on the ac device simulation with the TCAD tool. Here, f_T is extracted when current gain drops to unity ($Y_{21}/Y_{11} = 1$), and f_{max} is extracted when Mason's unilateral gain drops to unity. As V_{GS} increases, transconductance increases since number of electrons injected from source by band to band tunneling is increased, therefore, frequencies start increasing with gate bias until it reaches its maximum value at a specific gate bias. The initial increment of the RF figures of merit are driven by the increasing on current level due to increasing gate bias than it falls with gate bias due to the combined effect of the accelerating increasing of the total gate-to-drain/source capacitance and limiting of g_m due to mobility reduction by the gate field. The peak point of RF figures of merit corresponds to the point between the minimum gate–drain/source capacitance and peak of transconductance. For calculating the effect of doping profile in drain extension region, we have to look on to Fig. 3.1. From the doping curve, it is found that the doping concentrations at the gate edge changes from 5×10^{17} to 5×10^{18} /cm^3 as doping profile change from GD to UD for fixed drain extension length (90 nm). This variation affects the drain parasitic capacitance as a result; gate-to-drain capacitance (C_{GD}) reduces with decreasing doping at the gate edge. This variation will affect RF figures of merit as it is conformed from Fig. 3.6. Based on this, curve shows the impact of CL of GD profile in drain region on f_T and f_{max} as function of gate voltage. When CL = 0.1, the f_T and f_{max} obtained are 25 and 225 GHz, respectively. While if CL = 0.05, f_T and f_{max} obtained are 37 and 275 GHz, respectively. The reason for this enhancement is the reduction of C_{GD} parasitic capacitance.

3.3.4 RF Characteristic with L_G and LAD Variation

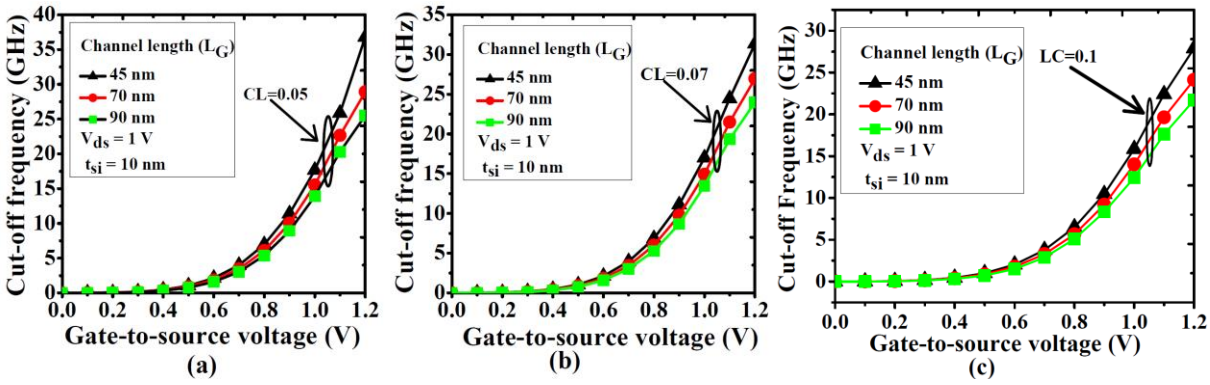

Figure 3.7. [(a), (b), (c)] f_T as a function of the gate voltage for various characteristic length (CL) of Gaussian doping.

Fig. 3.7(a), (b), and (c) shows the variation of cut-off frequency (f_T) as a function of gate-to-source voltage for different channel lengths with different CLs. For that, in conventional MOSFETs, cut-off frequency depends upon g_m and total gate capacitance (C_{gg}) [13], [18], [20], [47]. In the MOSFET, with the downscaling of the channel length, g_m increases and C_{gg} significantly reduces and both device parameters are responsible for significant improvement of cut-off frequency. While in the case of a DG-TFET, g_m does not change considerably and C_{gd} reduces with downscaling of the channel length and also by varying the position of the drain body junction with respect to the gate edge by controlling the drain doping profile [According to Fig. 3.1(b)] reduces the parasitic capacitance, consequently, C_{GD}. The curve indicates that f_T improves with downscaling of the length and reducing CL. The maximum value of cut-off frequency of the DG-TFETs with the channel length (L_G) = 45, 70, and 90 nm with CL = 0.1 are 27, 24, and 21 GHz, respectively, and it improves to 37, 28, and 25 GHz, respectively, when CL = 0.05. The f_T improved by 33%, 16%, and 20% with the variation of channel length when CL changes from 0.1 to 0.05. These values are calculated at V_{gs} = 1.2 V.

Another parameter for RF performance f_{max} is the frequency where power gain is unity. For conventional MOSFETs, it can be expressed in [1], [12] as

$$f_{\max} = \frac{g_m}{2\pi C_{gs}\sqrt{4(R_G + R_S + R_i)(g_{ds} + g_m \frac{C_{gd}}{C_{gs}})}} \tag{3.2}$$

where R_g , R_s , and R_i are the gate, source, and channel resistances, respectively. For determining the value of fmax, the gate resistance plays a major role, therefore, metal gates are used to reduce gate resistance. Molybdenum is considered to be a potential for future metal gate technology, therefore, in our simulation study, we have used molybdenum for gate material.

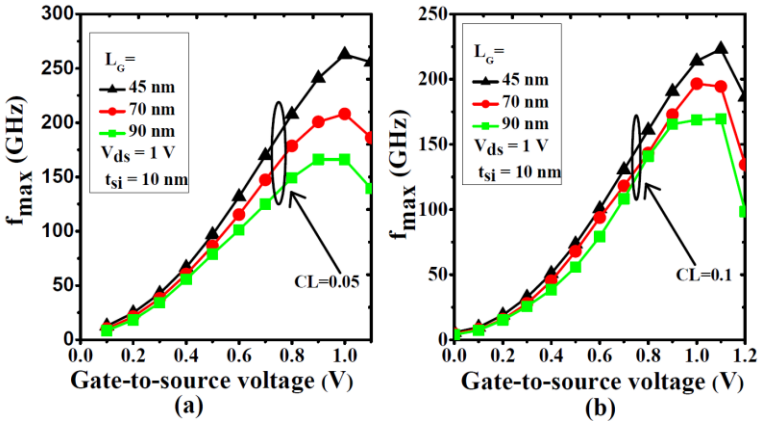

Figure 3.8. [(a), (b)] Maximum oscillation frequency (f_{max}) of Tunnel-FET as a function of gate voltage with Gaussian doping profile (different characteristics length).

Fig. 3.8 (a) and (b) shows the comparisons of f_{max} as a function of gate-to-source voltage for different values of the channel length (L_G) with different CL. In the DG-TFET, it is observed that fmax increases with downscaling of L due to reduction in the CGD/CGS ratio and distributed channel resistance, rather than improving gm. The f_{max} of DG-TFETs with channel length (L_G) = 45, 70, and 90 nm with CL = 0.1 are 223, 194, and 169 GHz, respectively, and it improves to 255, 186, and 139 GHz, respectively, when CL = 0.05. Here, f_{max} increment is limited by the dominant effect of increasing of parasitic resistances.

Further, one more important parameter for evaluating RF performance is the GBW for a certain dc gain. In case of conventional MOSFETs, GBW is expressed by [2]

$$f_A = \frac{g_m}{2\pi 10 C_{gd}} \tag{3.3}$$

as channel length (L_G) is scaled down, transconductance (g_m) is increased, and the gate capacitance values are decreased, therefore, f_A α (g_m/C_{GD}).On the other hand, g_m of a TFET does not change significantly with down scaling of the channel length L_G and the gate capacitance values are

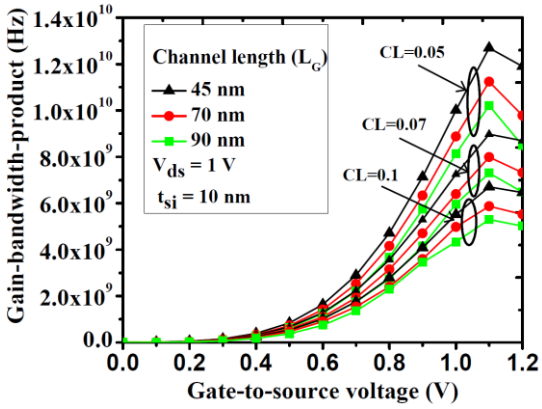

Figure 3.9. Comparison of GBW product for TFET for different channel length with different CL of Gaussian doping.

decreased with L_G. Fig. 3.9 shows GBW product versus V_{gs}, which indicates that channel length scaling results in larger GBW product when the gate-to-source voltage approaches the supply voltage. From curve, it is also evident that the TFET exhibits higher GBW as the CL changes from 0.1 to 0.05 for the channel length 45 nm.

Now it is concluded that RF figures of merit improves with downscaling of the length and also improve with decreasing the CL due to reduction of parasitic capacitance. Table 3.1 shows the comparisons of RF figures of merit with variation of channel lengths for UD and GD at drain region. The results are calculated at drain current value of 10^{-5} A/μm. It is observed that f_T, f_{max}, and GBW are improved by 96%, 40% and 140%, respectively, in GD of CL = 0.05 at 45 nm in comparison to UD.

Table 3.1. Comparison of RF figures of merit of double gate with HDL TFET for different channel length with uniform and Gaussian doping of different CL

RF Parameter	Channel Length (L_G)=45nm				Channel Length (L_G)=70nm				Channel Length (L_G)=90nm			
	GD			UD	GD			UD	GD			UD
	CL=0.05	CL=0.07	CL=0.1	UD	CL=0.05	CL=0.07	CL=0.1	UD	CL=0.05	CL=0.07	CL=0.1	UD
f_T(GHz)	37	26	22	19	28.5	23	20	17	25.5	21	18.5	16
f_{max} (GHz)	260	240	215	185	190	200	185	170	140	170	160	160
GBW(GHz)	12.75	8	6	5	11.25	7.5	5.5	4.5	10	7	5	4

3.3.5 LAD doping with HDL

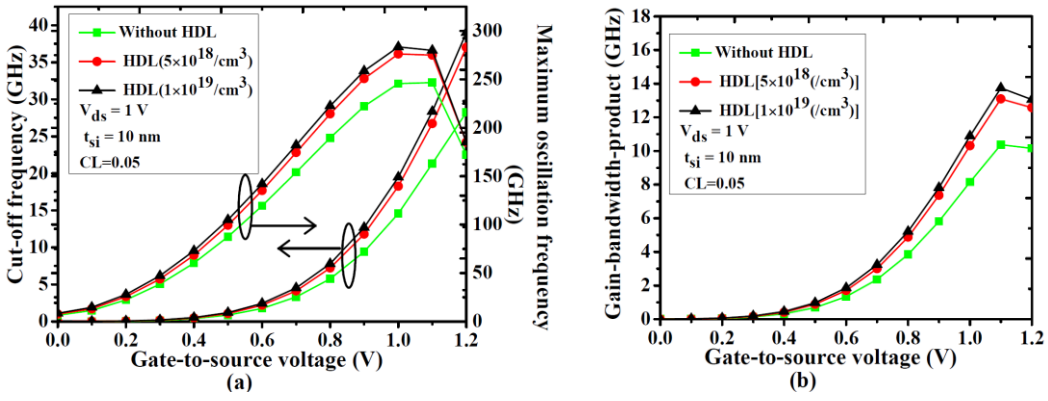

Figure 3.10. RF figures of merit for HDL and without HDL double gate TFET (a) f_T and f_{max} as a function of the gate voltage (b) GBW product as a function of the gate voltage.

The variation of RF figures of merit such as cut-off frequency (f_T), maximum oscillation of frequency (f_{max}), GBW with gate voltage for without HDL and with different HDL concentration is shown in Fig. 3.10. The thin HDL n^+ layer reduces the tunneling and increases the tunneling carriers, consequently, improving the transconductance. The device parameter g_m also increases with increasing HDL

concentration resulting in the improvement of RF figures of merit. Thus, for comparison, all figures of merit are extracted at a particular drain voltage of V_{ds} =1 V while drain doping is taken Gaussian with CL = 0.05. RF figures of merit like cut-off frequency, maximum oscillation frequency, and GBW are compared for UD and GD with HDL ($10^{19}/cm^3$) and without HDL in Table 3.2. It is observed that these parameters show improvement in GD as compared to UD. This is due to the reduction of gate–drain parasitic capacitance. These figures of merit improve, if GD parameter CL changes from 0.09 to 0.05 in drain region, as it is observed in Table 3.2.

Table 3.2. Comparisons of RF figures of merit for HDL and without HDL double gate TFET with uniform and Gaussian doping at drain region

RF Parameter	Gaussian doping				Uniform doping	
	CL=0.05		CL=0.09			
	Without HDL	With HDL	Without HDL	With HDL	Without HDL	With HDL
f_T (GHz)	25	39	22	30	17.5	25
f_{max} (GHz)	210	280	180	230	145	190
GBW (GHz)	10	13	5	7.25	37.5	4.75

Therefore, it can be concluded that the use of lateral asymmetric doping (LAD) in the drain suppresses the ambipolar conduction, improves subthreshold swing and also with this LAD addition, enhances the performances of the TFET for RF applications.

Chapter 4

Impact of Drain Parasitic on TFET Reliability and its Analog/RF Characteristics

Tunnel FET is considered as alternative of MOSFET for low voltage and low power SoC applications. In previous chapter demonstrated the feasibility of lateral asymmetric drain doping in TFET as a way to improve device performances and RF figure of merit. However, in MOSFET, the lateral asymmetric doping profile improves SCEs but this profile induces parasitic resistance consequently reduces MOS device reliability and degrades analog/RF characteristics. On the other hand, in Tunnel FET, the sensitivity of device characteristics to the variation in technological parameter will be different due to different conduction concept as compare to MOSFETs. A complete understanding of transistor parasitic in TFET on device reliability and its impact on analog/RF performance for asymmetric doping is also required for device optimization for SoC applications.

Therefore in this chapter, the effects of lateral asymmetric drain (LAD) doping profile and drain extension length (L_{extd}) variation of double gate tunnel field effect transistor (DG-TFET) are discussed on device reliability and its analog/RF performance. For that, some of the important parameters of DG-TFET and DG-FET such as driving current, transconductance (g_m), and device efficiency (g_m/I_d) are compared for uniform doping (UD) and gaussian doping (GD) profile. The results indicate that resistance induced by source-drain extension length region and drain doping variation are not significant in TFET as compared to MOSFETs. This makes TFET more reliable against parasitic resistance of doping fluctuation variation than MOSFETs. This chapter also reports a quantitative understanding of the LAD doping and its variation on DC performance of DG-TFET. Further, the L_{extd} variations of the DG-TFET are also investigated for RF performance and delay. The results show that the behavior of RF FoM is different from DG-FET.

4.1 Device Structure and Simulation Setup

The device structure for a n-channel DG-TFET used in this paper is shown in Fig. 4.1 (a). The device parameters of DG-TFET used in the simulation are shown in Table I. High-k gate insulator is placed over the whole device and the gate electrode which is placed over insulator, covers the channel region. The device structure was widely presented in the literature [36] and represents an excellent device for simulation calibration. The DG-TFET is investigated for varying drain doping profile and its extension region on device performance. In the following discussion, the doping profile of the drain extension region is assumed to be Gaussian like which is expressed as [46].

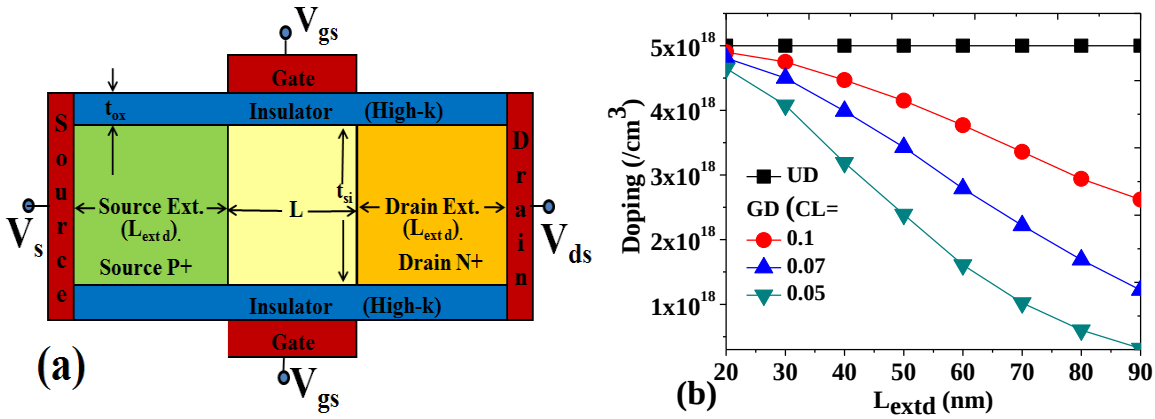

Figure 4.1: (a) Device schematic of the n-channel DG-TFET (b) Doping concentration at drain-channel junction in drain region with L_{extd} variation.

$$N(Y) = Peak.\exp\left[-(Y - Y_{Peak}/Y.CHAR)^2\right] \tag{4.1}$$

CHAR specifies the principle characteristic length (CL) of the implant. Characteristic length (CL) is equal to the square root of twice the standard deviation. Here, CL is taken in micron. Peak specifies the peak doping concentration (5×10^{18} /cm^3) at the beginning of drain extension region and then the doping concentration decreases towards the channel with CL and length of L_{extd} as two variables. As explained in the previous chapter, Fig. 3.1(b) shows the doping profile of n-channel DG-TFET with L_{extd} = 90 nm for UD and different CL of GD profile. It is observed that the doping concentration decreases at gate edge in the drain region when decreasing CL (0.1 to 0.05). Here, Fig. 4.1(b) shows doping concentration at drain-channel junction in drain region with L_{extd} variations for UD and different CL of GD profile. It is observed that the higher doping level come closer to gate edge in the drain region for different CL when decreasing L_{extd} from 90 nm to 20 nm and doping concentration reaches towards the UD profile. Drain-channel junction is changing abruptly for UD and different CL of GD profile. Source-channel junction is also kept perfectly abrupt for improving the performance of the device [15].This is also same for high tunneling effect in ETFET [21], which needs a sharp and high drain doping profile.

The device has been simulated using the nonlocal band-to-band tunneling (BTBT) model available in Silvaco Atlas[46] validated using[32], [36]. This model requires a special mesh to be applied around area where the tunneling can take place. To calibrate the nonlocal BTBT model, the electron mass (m_e) and hole mass (m_h) are changed the values m_e = 0.22 and m_h = 0.34.The value of other parameters for the nonlocal model are kept unchanged and taken default value as projected for silicon (Si). Although,

Table 4.1: Parameter used for the DG-TFET simulation

Device parameters	**Value**
Channel length (L)	45 nm
Silicon thickness (t_{si})	10 nm
Gate dielectric thickness (t_{ox})	3 nm
Width of the device (W)	1 µm
Drain doping concentration	5×10^{18} cm^{-3}, n-type
Channel doping concentration	1×10^{17} cm^{-3}, p-type
Source doping concentration	1×10^{20} cm^{-3}, p-type
Gate material work function	4.1 eV
Drain voltage (V_{ds})	1 V
Source voltage (V_s)	0 V
Gate voltage (V_{gs})	0 V to 1V
High-k dielectric material permittivity	21
Source/Drain extension length	90 nm-20 nm

an alternation of electron and hole mass in nonlocal model for BTBT device or abrupt doping profile in the device results in some variation in simulated current levels. But, this does not have much impact on the outcome of the investigation. Device current components in off state region are ambipolar current, SRH (Shockley-Read-Hall) and TAT (trap assisted tunneling). In this study, SRH recombination model is included with default parameters [46]. Further, taking into account the high doping concentration in the source and drain region, band gap narrowing model is also included with other physical model such as concentration, field dependent mobility and Fermi-Dirac statistics. Furthermore, the analog/RF figures of merit have been extracted from the Y-parameter matrix generated by performing the small-signal ac analysis. Whenever, work function of gate electrode is not mentioned it is considered to be 4.1eV.

4.2 Comparison Between DG-TFET and DG-FET

Fig. 4.2 shows LAD doping effect on asymmetrical DG-FET with asymmetric DG-TFET. Here, asymmetric means doping concentration of source and drain are different. Which is 1×10^{20} /cm^3 and 5×10^{18} /cm^3 respectively. Except the type of doping of the source, the two devices have the same dimensions for dielectric thickness, channel length, silicon thickness; same gate work function equal to 4.4 eV and source and drain extension length. Fig 4.1 (b) shows the UD and GD profile with different CL. Here, the source doping is kept uniform throughout the source extension region. Effect of UD and GD profile in the drain extension region are analyzed for both devices. The UD is one of the useful basis for comparison to explain the effects of variation in doping gradient on the DG-TFET and DG-FET. In case of DG-FET, graded doping profile in extension region reduces SCEs. However, this profile induces parasitic resistance which degrades analog/RF characteristics. More gradient doping profile in SDE region and Lightly-doped drain (LDD) may lead to large parasitic resistance.

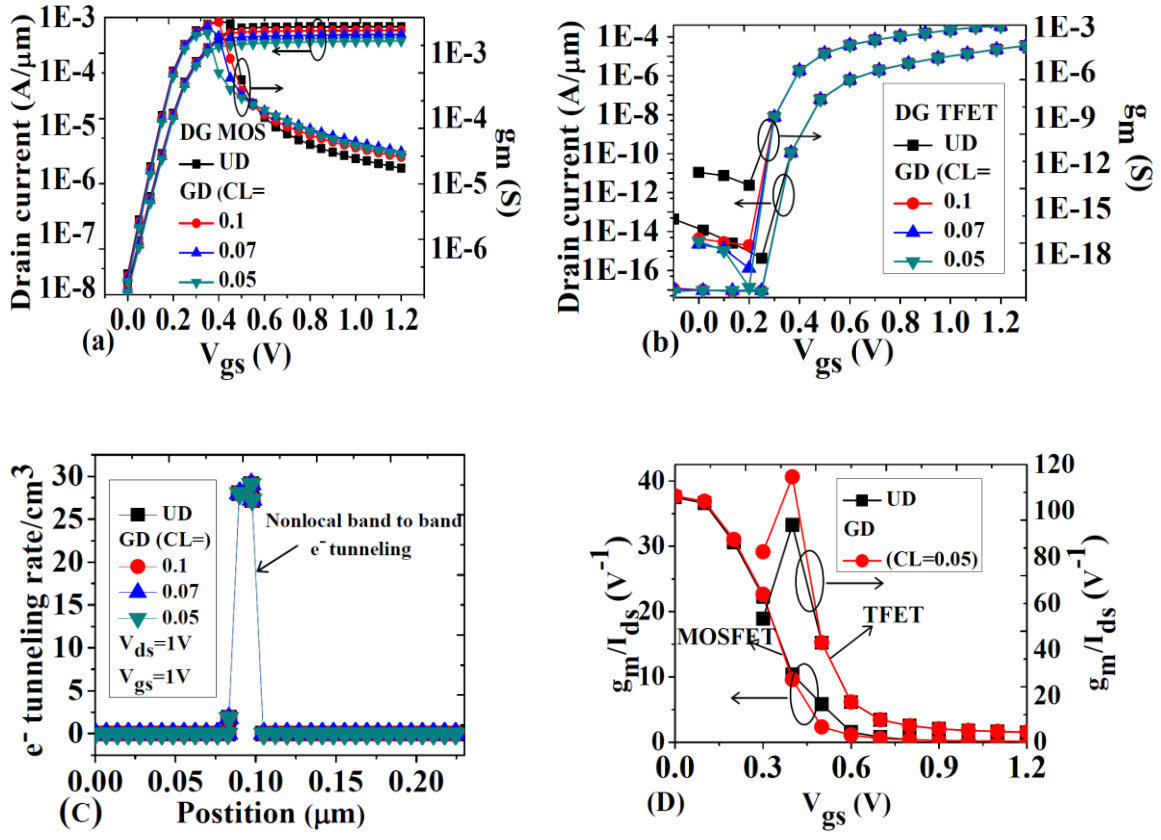

Figure 4.2: Comparison of DG-TFET characteristics with optimized asymmetric DG-MOSFET for UD and GD profile for different *CL* and gate material work function = 4.4 eV (a) Transfer characteristics and g_m behaviour for DG FET (b) Transfer characteristics and g_m behaviour for DG TFET (c) Nonlocal BBT e- tunneling ((Y-axis is on log10 scale) (d) g_m/I_d with V_{gs} variation.

Fig. 4.2(a) shows the corresponding device transfer characteristics for UD and GD profile, the curve clearly indicates that driving current obtained in the DG-FET for CL =0.05 decreases due to increase in parasitic resistance. On the other hand for DG-TFET, LDD is used to reduce the ambipolar effect and moreover graded doping profile in the drain extension region reduces ambipolar conduction up to large V_{gs} (explanation is given in the next section). DG-TFET does not show the variation in driving current with doping variation from UD to GD. Such behavior is expected when we consider that series resistance in TFET comprises of channel resistance and tunneling barrier resistance. Changing in length or doping concentration affects the channel resistance whereas changing the cross section area affects the tunneling barrier resistance. For the variation in doping profile (from UD to GD), ON-state current is observed to be nearly constant as seen in Fig. 4.2 (b). Although, the magnitude of current in DG-FET is higher than that of DG-TFET, it depicts that the current in DG-FET is more sensitive to varying parasitic resistance compared to DG-TFET. However, increment in channel resistance, due to decrease in doping concentration at drain-gate junction of DG-TFET does not vary the overall series resistance [3]. Thus, sensitivity of driving current against parasitic resistance affects RF FoM of DG-TFET in a different manner when compared to DG-FET.

Fig. 4.2(a) and Fig. 4.2(b) also show the transconductance (g_m) for DG-FET and DG-TFET as a function of gate voltage for UD and GD profile. Transconductance represents the amplification delivered by the device. It is an important parameter of device for analog/RF performance. It is clear from the fig. 4.2(a) that g_m of DG-FET degradation is induced by incremental parasitic resistance when drain doping profile change from UD to GD. Degradation is more severe for CL=0.05 than for CL= 0.1. This is probably due to the increased parasitic resistance, whereas the gm of DG-TFET does not alter with doping profile from UD to GD as shown in fig. 4.2(b). It is due to the reason, as explained earlier, that changing doping profile or length does not change the overall series resistance significantly and tunneling carrier at source-channel junction remains same as shown in fig. 4.2 (c).

Fig. 4.2(d) shows the LAD doping effects on transconductance generation efficiency, g_m/I_{ds} (TGF) for both DG-FET and TFET as a function of gate voltage. If the value of TGF is high, then it shows the strong capability to deliver ac gain and this high value is required for analog/RF application. With increasing gate voltage, TGF of both the devices degrade. It indicates that power consumption also increases. It is also clear from the TGF curve for DG-FET that its value is higher between V_{gs} = 0.4V to V_{gs} = 0.7V for UD as compared to GD for CL=0.05. The lower value of TGF for GD profile is due to more degradation in gm between 0.4 V to 0.7 V. So, TGF is more efficient for UD profile (or low gradient profile). Whereas in TFET, the conduction concept is based on band to band tunneling, therefore it does not have SS limitation. So, its value is large initially as compared to DG-FET. It is also observed from the curve that value of TGF, initially (as V_{gs} equal to 0.4 V), for DG-TFET is 93.92 V^{-1} and 114.64 V^{-1} for UD and GD (CL = 0.05) profile respectively. The higher value of TGF for GD profile is due to lower OFF-state current (10^{-17}A/µm) as compared to OFF-state current (10^{-14} A/µm) of UD profile. TGF value becomes equal for UD and GD profile at gate voltage equal to 0.6 because after this drain current as well as gm does not change. So, this analysis for DG-TFET concludes that GD profile is more efficient for TGF initially.

4.3 L_{extd} Variation Effect on DC Performance

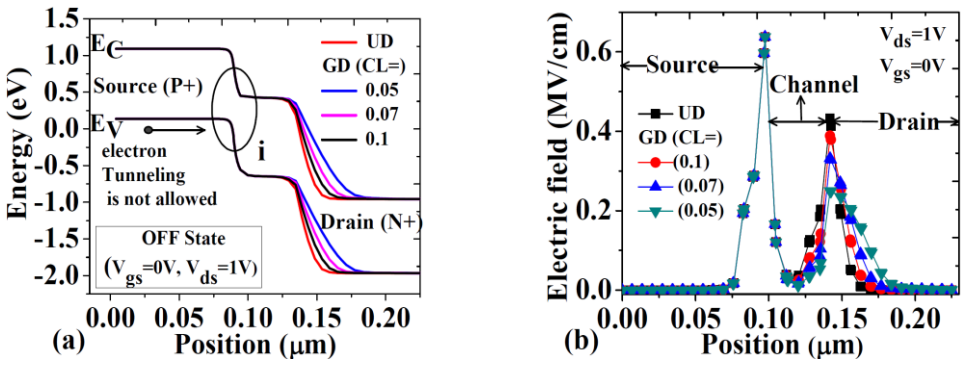

Figure 4.3: (a) Energy band diagram of the OFF-state and (b) Lateral electric field as a function of device position for n-channel DG-TFET

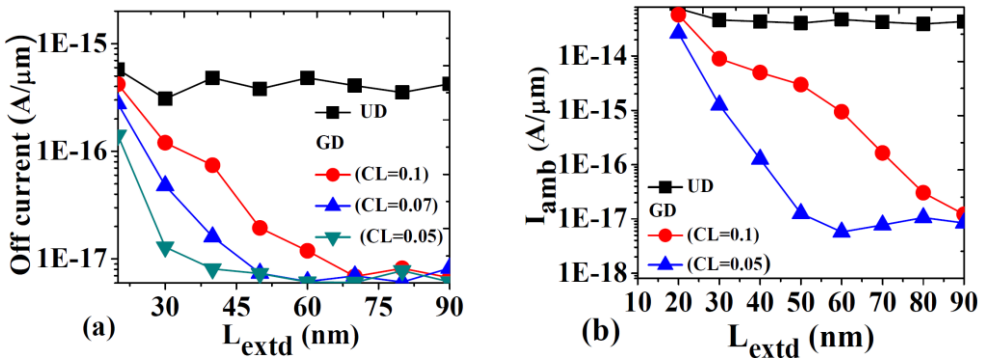

Figure 4.4:(a) Off-state current behaviour and (b) I_{on}/I_{off} behaviour with drain extention length variation for UD and GD profile with different CL

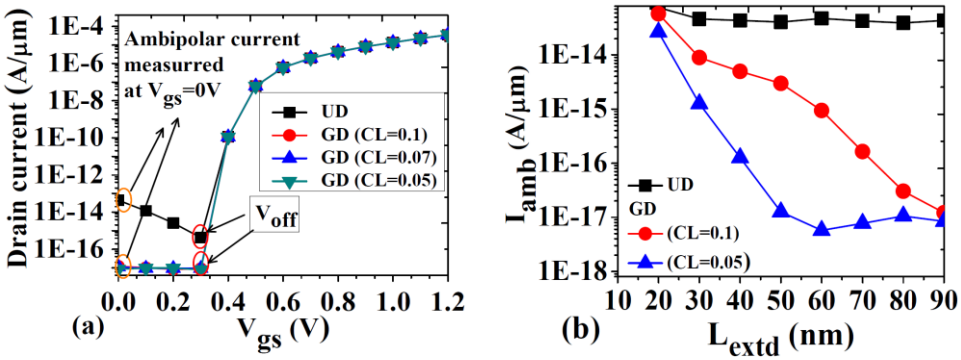

Figure 4.5:(a) Transfer characterstic of n-channel DG-TFET for I_{amb} measurement (b) I_{amb} behaviour with L_{extd} variation for UD and GD profile.

Fig. 4.3(a) shows the band diagram of the n-channel DG-TFET in OFF-state with UD and GD profile with different CL. Energy band diagram has been taken horizontally across the n-channel DG-TFET at a distance 1 nm from the surface. In the OFF-state, no tunneling occurs because the potential barrier between the source and channel is large. Here, OFF-state (V_{off}) is the minimum value of gate-to-source (V_{gs}) voltage at drain voltage (V_{ds}) of 1V when the drain current (I_d) shows a minimum value but for $V_{gs} \leq V_{off}$, it either starts tunneling from drain-to-channel (ambipolar conduction) or remain in OFF-state depending upon drain-channel barrier. Also ON- state current is defined (extracted) when gate-to-source voltage (V_{gs}) is equal to 1V and drain-to-source (V_{ds}) voltage is 1V. From the energy band curve, it is observed that the depletion width at drain-channel junction increases with decrease in CL of doping profile, since doping concentration in the drain region close to gate edge decreases resulting in decrease in OFF-state current. It is clear from fig. 4.4(a), representing OFF-state current (OFF-state current measured at V_{gs} = 0V and gate work function = 4.1eV) with drain extension length variation, that OFF-current value is 10^{-17}A/μm at drain extension length of 90 nm for gaussian CL=0.05 as compared to 1E-15 for UD profile for same drain extension length. When L_{extd} decreases and reaches within the range of 60 nm-50 nm, OFF-state current remain constant for CL=0.05 thereafter, OFF-state current starts increasing and reaches towards the OFF-state current for UD doping profile. The

OFF-state current increment is more for larger value of CL such as 0.07, 0.1 and UD, because of higher doping in the region comes closer to gate edge in the drain region and reduces the potential barrier of drain-channel junction. Fig. 4.4 (b) shows the drain extension length variation with I_{on}/I_{off}. The variation in the drain extension length from 90 nm to 50 nm, the value of I_{on}/I_{off} is almost constant with a value of 10^{13}A/µm for CL=0.05 and then starts decreasing and reaches towards the UD doping profile. It is clear from the curve that I_{on}/I_{off} degradation is more for higher value of CL.

The TFET is an ambipolar device and conducts when $V_{gs} \leq V_{off}$, with band to band tunneling (BTBT) occurring at the metallurgical drain-channel junction. Fig. 4.3(b) shows the lateral electric field as a function of device position for UD and GD profile for different CL at V_{gs} as 0V and V_{ds} as 1V. The electric field has been taken 1 nm below the oxide-silicon interface. As CL of GD profile changes from 0.1 to 0.05 electric field source-channel junction remains constant for aforementioned variation of doping profile. This ambipolar behaviour is not desirable in the circuit design. Fig. 4.5(a) shows the drain current with gate voltage variation for ambipolar current measurement for different CL against UD profile. The gate work function has been changed to 4.4eV; due to which OFF-state voltage shifted to 0.3V from 0V and ambipolar current is measured at 0V. Fig. 4.5(b) shows ambipolar current measurement with different drain extension length variations. It is clear from the curve that drain current remains in OFF-state value of 10^{-17}A/µm up to 50 nm drain extension length for CL equal to 0.05 as compare to UD for ambipolar current of value 10^{-13}A/µm. The ambipolar current starts increasing below 50 nm of L_{extd} for CL = 0.05 and increases towards the ambipolar current for UD profile.

4.4 Device Capacitance with L_{extd} Variations

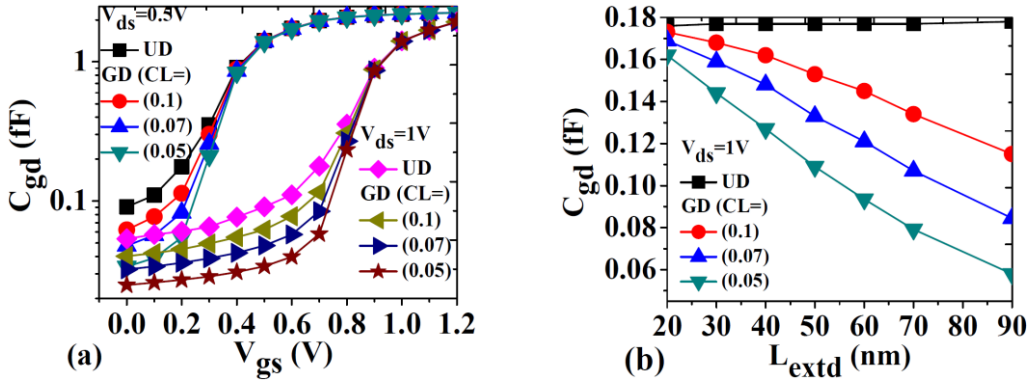

Figure 4.6: (a) C_{gd} as a function of V_{gs} for UD and GD profile with different CL for L_{extd} = 90 nm. (b) C_{gd} with L_{extd} variation for UD and GD profile.

The schematic shown in fig. 4.1(a), depicts the total parasitic (extrinsic) gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitance (not taking overlap capacitance into consideration as source-channel and drain-channel junction abruptly change) are expressed as Cgs (parasitic) = $C_{outer,fring}$ + $C_{Sinner,fring}$ and

C_{gd} (parasitic) = $C_{outer,fring}$ + $C_{Dinner,fring}$. Where, $C_{outer,fring}$ is the external electric field which is bias dependent and comprises of the capacitance between the gate and the SDE (source drain extension) region. $C_{Sinner,fring}$ and $C_{Dinner,fring}$ are internal fringing electric fields respectively which depend on source and drain doping profile. The intrinsic capacitance formation of DG-TFET is different from the MOSFET as explained in the literature [43].it was shown that C_{gd} of TFET constitutes larger fraction of total gate capacitance (C_{gg}).

Fig. 4.6(a) shows, (C_{gd}) capacitance as a function of gate voltage for n-channel DG-TFET. In the same curve, the effect of LAD and uniform drain doping profile are also shown. The characteristics shows that the capacitance C_{gd} of LAD doping profile is initially lower than that of UD doping profile. This is because, in LAD device, inner-fringing capacitance is less as compared to UD doping when the transistor is switched off. It can be screened by the inversion layer which is supported by the tunneling carrier. From the curve, it is found that the fringing capacitance is screened when the gate voltage is 1 V and drain voltage is 1V. The inner fringing capacitance is also reduced when gaussian coefficient CL changes from 0.1 to 0.05.This reduction of the C_{gd} capacitance reduces OFF-state current as well as ambipolar conduction. This will also greatly enhance the RF FoM. Fig. 4.6(b) shows the L_{extd} variation effect on gate to drain capacitance. From the curve, it is observed that C_{gd} increases when drain extension length varies from 90 nm to 20 nm for various GD profile coefficient (CL=0.1 to CL=0.05) and drain doping concentration of value 5×10^{18} /cm^3 and this capacitance (C_{gd}) reached towards the capacitance (C_{gd}) for UD profile. This is because lower L_{extd} encroaches more doping concentration at drain-gate edge. Which is not suitable for DG-TFET performance in terms of OFF-state current and ambipolar behaviour as explained earlier in DC performance calculation. On other side for MOSFET, same trend will increase SCEs [1], [47] in the device for the advance technology node. Total input capacitance (extrinsic + intrinsic) can be extracted from numerical ac simulation of DG-TFET as

$$C_{gg} = \left|\mathrm{Im}\left(Y_{11}+Y_{12}\right)/\omega\right| \tag{4.2}$$

where $\omega=2\pi f$, Here C_{gg} can be defined as = C_{in} + C_{frin} (fringing capacitance including external and internal fringing components). The C_{frin} can simply be identified by limiting C_{gg} at zero or negative V_{gg}.

4.5 L_{extd} Variation Effect on RF and Delay Performance

Fig. 4.7(a) shows, the transconductance and source-drain conductance characteristics as the function of gate-to-source voltage. From the curve, it is clear that both characteristic behaviour do not change with change in the doping profile from UD to GD profile for different CL for 90 nm of L_{extd}. Furthermore, their value remains constant with variation of L_{extd} from 90 nm to 20 nm as shown in fig. 4.7(b). The reason behind such rigid behaviour is that tunneling area as well as number of tunneling

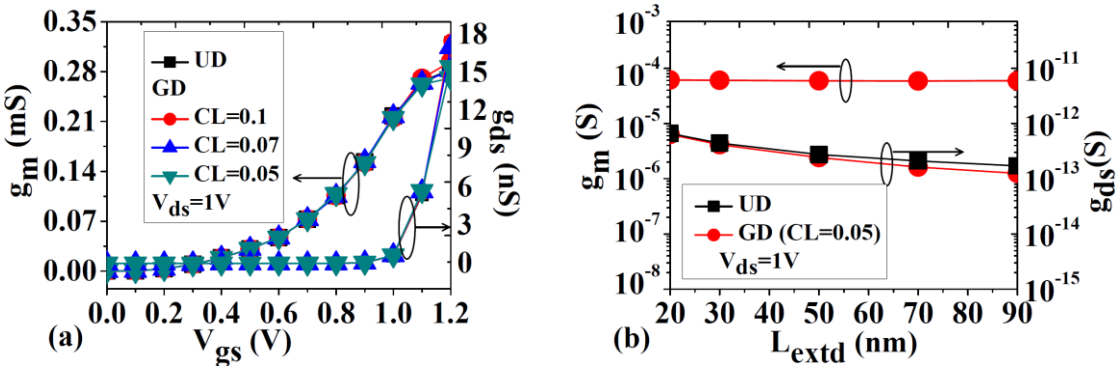

Figure 4.7: (a) g_m and g_{ds} characteristics of DG-TFET as a function of V_{gs} (b) behaviour of g_m and g_{ds} as a function of L_{extd} variation for UD and GD profile with different CL (g_m and g_{ds} values are extracted at 0.7 V of V_{gs})

carrier do not change at source-channel junction with variation of both doping profile and L_{extd}. The invariable behaviour of g_m and g_{ds} will affect RF FoM differently as compare to MOSFET. So, it is necessary to study the effect of drain extension features on RF FoMs.

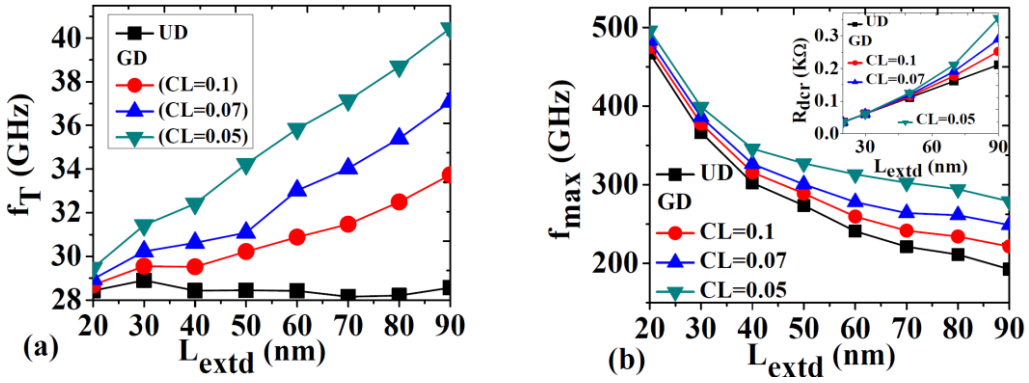

Figure 4.8: Behaviour of (a) f_T and (b) f_{max} as a function of L_{extd} variation. (f_T and f_{max} values are extracted at V_{gs} =0.7 V and V_{gs} =0.6 V respectively)

Fig. 4.8(a) and (b) shows the f_T and f_{max} behaviour with variation of L_{extd} for UD and GD profile. Here, f_T is extracted when current gain drops to unity and f_{max} is extracted when masons's gain drops to unity. As we have explained in the previous chapter, from the curve, it is clear that the f_T reduces linearly with reduction of L_{extd} for different CL of GD profile and reaches towards the value of f_T for UD profile. The reason behind such behaviour is that the f_T depends on g_m and total gate capacitance as given in equation (3). But g_m of TFET does not change with variation in L_{extd} and doping concentration as explained earlier. The doping concentration increases at drain-gate junction for various CL of GD profile when drain extension length varies from 90 nm to 20 nm. This variation causes the increment in gate-drain parasitic capacitance and consequently reduces f_T. The values of f_T are 33.74, 37.09 and 40.45 GHz for GD profile coefficient of CL equal to 0.1, 0.07, and 0.05

respectively at L_{extd} of 90 nm and the values of f_T become 28.69, 28.96, and 29.47 GHz respectively at 20 nm.

The f_{max} behaviour is opposite as in f_T with L_{extd} variation. From the curve fig. 8(b), it is observed that fmax increases with reduction of L_{extd} from 90 nm to 20 nm. However, the increment is not linear because f_{max} depends on R_g, g_{ds} and f_T behaviour with L_{extd} variations. f_{max} increases with increase in f_T and decrease in R_g. f_T is more effective on fmax for above 50nm of drain extension length as compared to R_g. Therefore, f_{max} increases very slowly from 90 nm to 40 nm of L_{extd}. After that (below 40 nm of L_{extd}), f_{max} starts increasing rapidly due to the distributed channel resistance becomes more dominant over f_T reduction. The values of fmax are 221.47, 248.76 and 278.69 GHz for GD profile coefficient of CL equal to 0.1, 0.07 and 0.05 respectively at 90 nm of L_{extd} and the values of f_{max} become 475, 483, and 496 GHz respectively at 20 nm of L_{extd}.

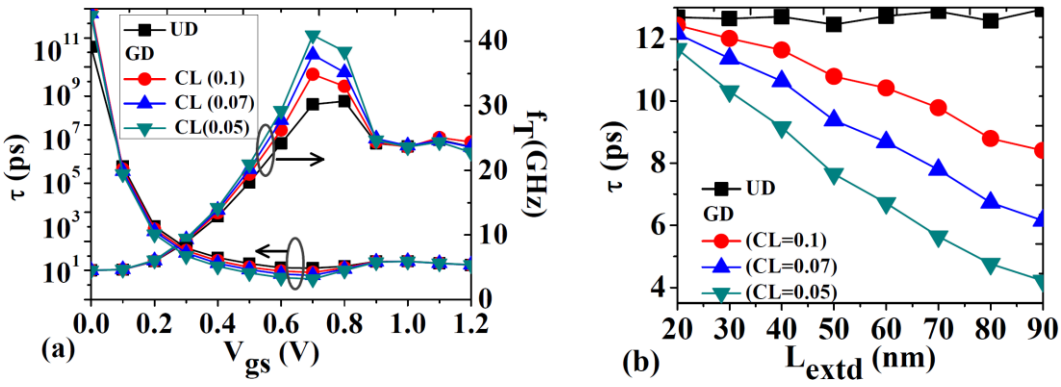

Figure 4.9: Behaviour of (a) Intrinsic dealy and f_T as a function of V_{gs} and (b) delay as a function of L_{extd} variation for UD and GD profile with different CL. (intrinsic device dealy value is extracted at V_{gs} =0.7 V.)

Fig. 4.9(a) shows the intrinsic delay time of the DG-TFET as a function of gate-to-source voltage for UD and GD profile. Intrinsic delay time is defined by[48]

$$\tau = \left(C_{gg} \times V_{dd}\right) / I_{on} \tag{4.3}$$

where V_{dd} is the supply voltage equal to 1 V. Since, DG-TFET has high cut-off-frequency and low C_{gd} for GD profile (CL = 0.05) and consequently an improved Intrinsic delay time (τ) can be obtained as confirmed from Fig. 10(a). It is found that improved τ is 207 times lower for GD profile of CL=0.05 as compared to UD profile for 90 nm of Lextd at 0.7 V of V_{gs}. Furthermore, delay behaviour is also checked for L_{extd} variation as shown in fig. 10 (b). It is found that delay is proportional to 1/ f_T when L_{extd} varies from 90 nm to 20 nm.

4.6 Drain Parasitic Dependency for Tunnel FET and DG-FET

RF FoM of DG-FET for UD and GD profile (CL = 0.05) are compared for various L_{extd} length in Table-II. From the values, it is clear that g_{ds}, C_{gd}, and gm are affected significantly for aforementioned variation of L_{extd}. With graded doping (for CL = 0.05) in the drain extension region as compare to uniform doping, C_{gd} are reduced due to reduction in fringing capacitance and gds is also degraded due to reducing gate control in extension region. However, g_m drops

Table 4.2. RF FoM of DG-FET for UD and GD (CL = 0.05) profile and different drain extension lengths. RF values are extracted at their peak value and V_{ds} = 1 V

RF Parameter	L_{extd} = 30 nm		L_{extd} = 50 nm		L_{extd} = 70 nm		L_{extd} = 90 nm	
	UD	GD	UD	GD	UD	GD	UD	GD
I_{on}/I_{off}	1.23E+05	1.25 E5	0.84 E5	0.80 E5	0.70 E5	0.61 E5	0.71 E5	0.45 E5
C_{gd} (F)	4.65E-17	4.47 E-17	4.66 E-17	3.63 E-17	4.76 E-17	2.87 E-17	4.72 E-17	2.18 E-17
g_m (S)	4.78E-03	4.57 E-3	4.13 E-3	3.51 E-3	3.49 E-3	2.85 E-3	3.25 E-3	2.01E-03
g_{ds} (S)	5.74 E-4	5.63 E-4	2.90E-04	2.45E-04	2.93 E-4	1.79 E-4	3.49 E-4	1.27 E-4
f_T (GHz)	412	408	385	362	367	309	349	242
f_{max} (GHz)	645	647	500	550	420	480	366	433

continuously due to increasing value of series resistance, as reported in the literature[1], [23], [47]. On the other hand, increase in doping concentration makes gm higher and C_{gd} also increases. The nature of the variation of g_{ds}, C_{gd} and gm with L_{extd} variation accounts for the trend in f_T and fmax. Therefore, investigations have been reported on doping optimization in the SDE region and have also shown the trade-off between resistance and capacitance to enhance the RF performance.

Table 4.3 Comparison of device performance parameter and RF figure of merit of DG-TFET for different source-drain extension lengths (I_{on} and I_{off} are measured at V_{gs} =1V and V_{gs} = 0V respectively for V_{ds} = 1V

Device Performance Parameter	L_{extd} = 90nm			L_{extd} = 50nm		
	CL=0.05	CL=0.1	UD	CL=0.05	CL=0.1	UD
I_{on}/I_{off}	8.6E+12	7.90E+12	1.26E+11	7.30E+12	6.70E+11	7.10E+10
I_{amb}	8.38E-18	1.21E-17	4.34E-14	1.26E-17	2.97E-15	4.05E-14
C_{gd} (F)	5.80E-17	1.15E-16	1.78E-16	1.09E-16	1.53E-16	1.78E-16
C_{gs}/C_{gd}	3.9	1.98	1.28	2.09	1.49	1.28
f_T (GHz)	40.45	33.74	28.56	34.33	30.22	28.45
f_{max}(GHz)	278.67	221.47	192.34	327.05	288.88	273.49
GBW(GHz)	19.8	9.9	6.4	10.5	7.5	6.4
Delay (ps)	4.22	8.41	12.95	7.65	10.79	12.46

Device performance parameters and RF figure of merit of DG-TFET for UD and GD profile are compared for L_{extd} equal to 90 nm and 50 nm in Table III. The values are extracted for V_{gs} = 0.7 V. The I_{on}/I_{off} and ambipolar current are almost same when Lextd switches from 90 nm to 50 nm for

CL =0.05. However, I_{on}/I_{off} and ambipolar current are 100 and 1000 times higher respectively as compared to UD profile at 50 nm of L_{extd}. Further, high C_{gs}/C_{gd} is required to avoid Miller effect. When the L_{extd} switched from 90 nm to 50 nm, the ratio decreased due to increment in gate-drain parasitic capacitance. However, C_{gs}/C_{gd} for 0.05 value of CL is 1.63 times higher and delay for same value of CL is 63% lower as compared to UD profile at 50 nm of L_{extd}. The f_T and f_{max} behavior are opposite when L_{extd} is switched from 90 nm to 50 nm, as explained earlier. However, f_T, GBW and fmax for CL of 0.05 are 17.12%, 39% and 16.5% respectively as compare to UD profile at 50 nm of L_{extd}. So, it depicts that there is need of optimization for gate-drain parasitic capacitance rather than parasitic resistance for optimum value of DC and RF performance.

This work on TFET describes the optimizations required for applying TFETs in low power applications. This research will act as base to future work on TFET devices with drain extension feature in the context of RF and analog/RF performance

Chapter 5

Analog/RF Performance of Tunnel FET without Gate-drain Overlap

In MOSFET technology, source/drain extension (SDE) concept was devised to overcome short channel effects (SCEs) and leakage current [47], [49], [50]. Further, investigation was done on doping optimization in SDE region which suggest trade-off between parasitic components and enhanced performance in RF region [47], [49], [50]. The work related with MOSFETs SDE engineering for analog/RF improvement motivates to work towards gate-drain underlap engineering in tunnel FET for analog/RF characteristics. Since, the conduction concept of TFET differs from MOSFET, it suffers from low on-state current, ambipolar behavior and high gate-drain capacitance [25], [43] but it does not suffer from doping fluctuations. Therefore, the sensitivity of analog/RF characteristic to the variation in technology parameters for device engineering will differ too. Gate-drain underlap as well as asymmetric source drain doping engineering in extension [32], [35]region has been reported to mitigate TFET ambipolar behavior. Few researchers have worked on various TFET devices for analog/RF design for low power SoC applications. In previous chapters 3 and 4 have presented the lateral asymmetric drain doping engineering effect on n-channel DG-TFET device performance and its influence on RF characteristics. This chapter explains gate-drain underlap (UL) feature of double gate tunnel field effect transistor for analog/RF characteristic. Here, it is found that parasitic resistance induced by gate drain UL is not significant as compared to DG-FET. Thus, the behavior of RF figure of merit (FoM) is different from DG-FET.

5.1 Device Structure and Simulation Setup

The device structure for an n-channel DG tunnel field effect transistor (DG-FET) with gate-drain UL used in this chapter is shown in Fig. 5.1. High-k gate insulator is placed over the whole device and the gate electrode which is placed over insulator, covers the channel region. The DG-TFET is investigated for varying gate-drain UL region on device analog/RF characteristics. The device parameters of DG-TFET used in the simulation are shown in figure caption of fig. 5.1.The device has been simulated using the nonlocal BTBT model available in Silvaco Atlas[46] and validated simulation model using [32]. Since the tunnelling process is nonlocal therefore this model requires a special fine mesh to be applied around area where the tunnelling can take place. To calibrate the nonlocal BTBT model, the

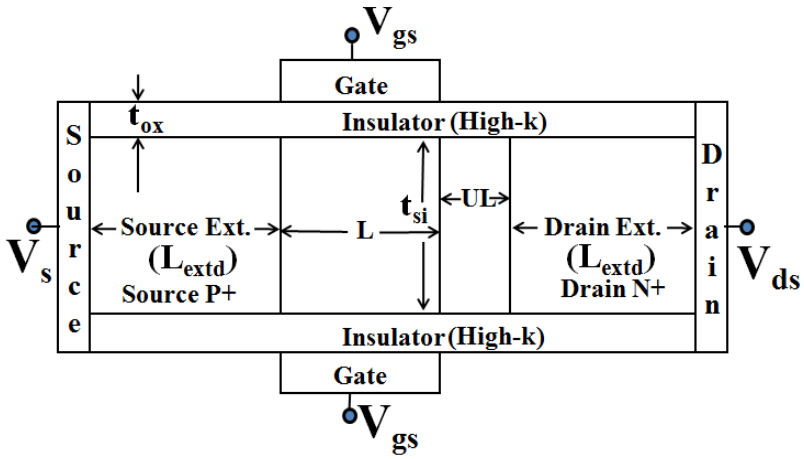

Figure 5.1: Device schematic of the n-channel DG-TFET with channel length (L) = 45nm, silicon thickness (t_{si})=10 nm, gate dielectric thickness (t_{ox})=3nm, width (W)=1µm, gate material work function = 4.3 eV, high-k dielectric material permittivity=21, L_{extd}=45 nm, UL length=0 to 24 nm, source/drain doping concentration=$1\times10^{20}/cm^3$, while for DG-FET, source P+ is replaced with n+ and channel is doped by P type to minimize SCEs. UL is measured in nm.

electron mass (m_e) and hole mass (m_h) for Silicon are tuned the values of m_e = 0.22 and m_h = 0.36. The values of other parameters for the nonlocal model are kept to their default value as projected for Silicon. The calibrated current level is slightly higher than the experimental data as indicated by reference[32]. However, there is negligibly small impact on the outcome of our investigation. Further, taking into account the high doping concentration in the source and drain region, band gap narrowing model is also included with other physical model such as SRH, concentration, field dependent mobility and Fermi-Dirac statistics. Furthermore, the analog/RF figures of merit have been extracted from the Y-parameter matrix generated by performing the small-signal ac analysis.

5.2 UL Variation Effect on DG-TFET Characteristics

5.2.1 DC Characteristics

Fig. 5.2 shows gate-drain UL variation effect on DG-TFET transfer characteristics. In DG- TFET, gate-drain UL is used to reduce the ambipolar effect and improve the OFF-state current. Inset of fig. 5.2, shows the lateral electric field as a function of device position for different UL at V_{gs} and V_{ds} at 0V and 1V respectively. Electric field at drain channel junction reduces when UL varies from 0 nm to 24 nm, causes ambipolar reduction and electric field at source- channel junction remains constant for aforementioned variation of UL. On the other hand, DG-TFET does not show the variation in driving current (ON-state) with UL variation from 0 nm to 24 nm. Such behavior is expected when we consider that series resistance in TFET comprises of channel resistance and tunnelling barrier resistance.

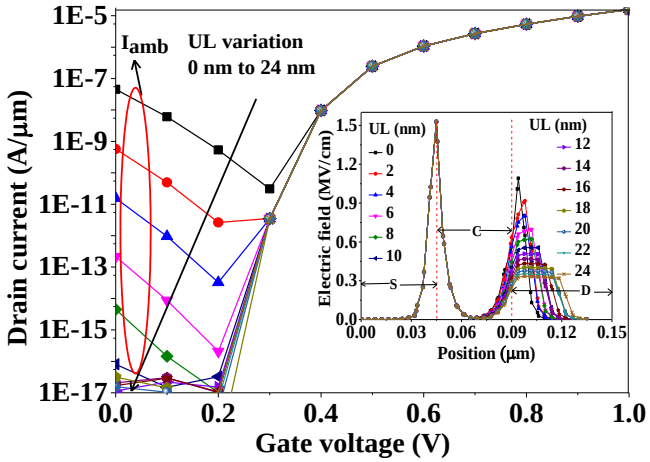

Figure 5.2: Transfer characteristics of DG-TFET for different UL

Changing in length or doping concentration affects the channel resistance whereas changing the cross section area affects the tunnelling barrier resistance. Although, the magnitude of ON-state current in DG-FET (as shown in Table 5.1) is higher than that of DG-TFET, it depicts that the current in DG-FET is more sensitive to varying parasitic resistance compared to DG-TFET. However, increment in channel resistance, due to increasing in UL length of DG-TFET does not vary the overall series resistance. Thus, sensitivity of driving current against parasitic resistance affects RF FoM of DG-TFET in a different manner when compared to DG-FET (Explanation is given in subsequent paragraph).

Table 5.1: Comparison of RF figure of merit for DG-TFET and DG-FET with different UL. I_{on} is Measured at V_{gs} =1V and V_{ds} = 1V.

Analog/RF parameters	DG-TFET			DG-FET		
	UL=0	UL=10	UL=24	UL=0	UL=10	UL=24
I_{on} (A/μm)	1.60E-05	1.60E-05	1.60E-05	1.58E-03	1.19E-03	6.17E-04
g_m (S)	5.26E-05	5.25E-05	5.24E-05	1.89E-03	1.85E-03	1.65E-03
g_{ds} (S)	5.38E-06	5.37E-06	5.37E-06	1.74E-03	1.38E-03	5.53E-04
C_{gd} (F)	1.12E-16	6.16E-17	3.81E-17	1.04E-16	5.65E-17	3.84E-17
C_{gs} (F)	1.39E-16	1.39E-16	1.39E-16	6.42E-16	6.96E-16	7.99E-16
C_{gs}/C_{gd}	1.24	2.24	3.65	6.17	12.31	20.8
f_t (GHz)	31.18	39.53	44.21	405	392	325
f_{max} (GHz)	139	193	207	402	407	266
GBW (GHz)	6.4	11.3	16.4	291	528	681

5.2.2 Analog Characteristics

Fig. 5.3(a) shows the UL variation effects on transconductance generation efficiency, g_m/I_{ds} (TGF) for both DG-FET and DG-TFET as a function of gate voltage. If the value of TGF is high, then it shows the strong capability to deliver ac gain and this high value is required for analog/RF application. With

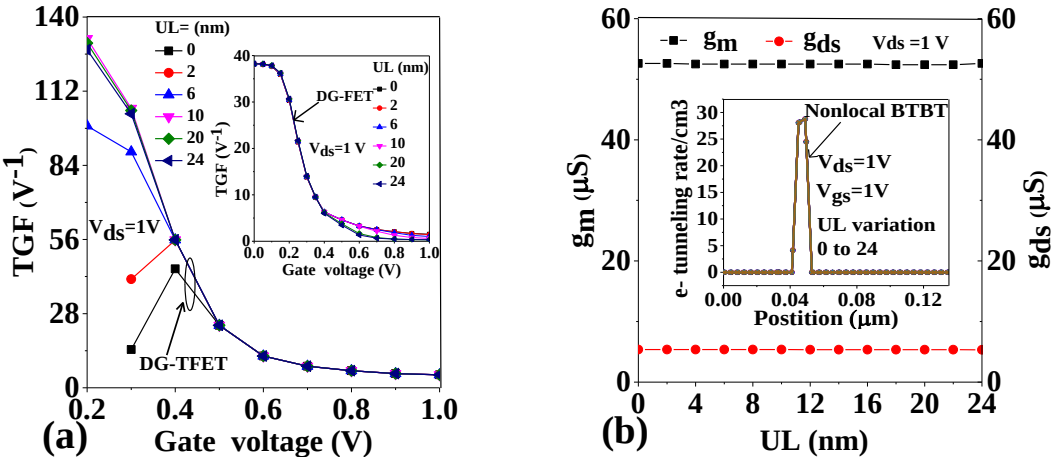

Figure 5.3: (a) TGF (g_m/I_{ds}) with V_{gs} variation for different UL (b) Behaviour of g_m and g_{ds} of DG-TFET as a function of UL variation (g_m and g_{ds} values are extracted at 0.8 V of V_{gs})

increasing gate voltage, TGF of both the devices degrade. It indicates that power consumption also increases. It is also clear from the TGF curve for DG-FET that its value is higher between V_{gs} = 0.4V to 1V for UL=0 nm as compared to UL=24nm. The lower value of TGF for higher value of UL is due to more degradation in g_m between 0.4 V to 0.7 V. So, TGF is more efficient for lower value of UL. Whereas in TFET, the conduction concept is based on band to band tunnelling, therefore it does not have SS limitation. So, its value is large initially as compared to DG-FET. It is also observed from the curve that value of TGF, initially (peak value), for DG-TFET is 44.92 V^{-1} and 128 V^{-1} for UL=0 nm and UL=24 nm respectively. The higher value of TGF for higher gate-drain UL is due to lower OFF-state current as compared to OFF-state current without UL.TGF value becomes equal for various UL at gate voltage equal to 0.5 V because after this drain current as well as gm does not change. So, this analysis for DG-TFET concludes that higher value of UL is more efficient for TGF initially.

Fig. 5.3(b) shows, the transconductance (g_m) and source-drain conductance (g_{ds}) characteristics as the function of UL length variation. g_m represents the amplification delivered by the device. It is an important parameter of device for analog/RF performance. It is clear from the Table 5.1, that g_m and g_{ds} of DG-FET degradation is induced by incremental parasitic resistance when UL changes from 0 nm to 24 nm. However, g_m and g_{ds} of DG-TFET doesn't change with UL varying from 0 nm to 24 nm. It is due to the reason, as explained earlier, that changing gate-drain UL or length does not change the overall series resistance significantly and tunnelling carrier at source-channel junction remains same as shown in inset of fig. 5.3(b). The invariable behaviour of g_m and g_{ds} affect RF FoMs differently as compared to MOSFET. So, it is necessary to study the effect of gate-drain UL features.

5.2.3 RF Characteristics

The intrinsic capacitance formation of DG-TFET is different from the MOSFET as explained in the literature[43]. It is shown that C_{gd} of TFET constitutes larger fraction of total gate capacitance (C_{gg}).

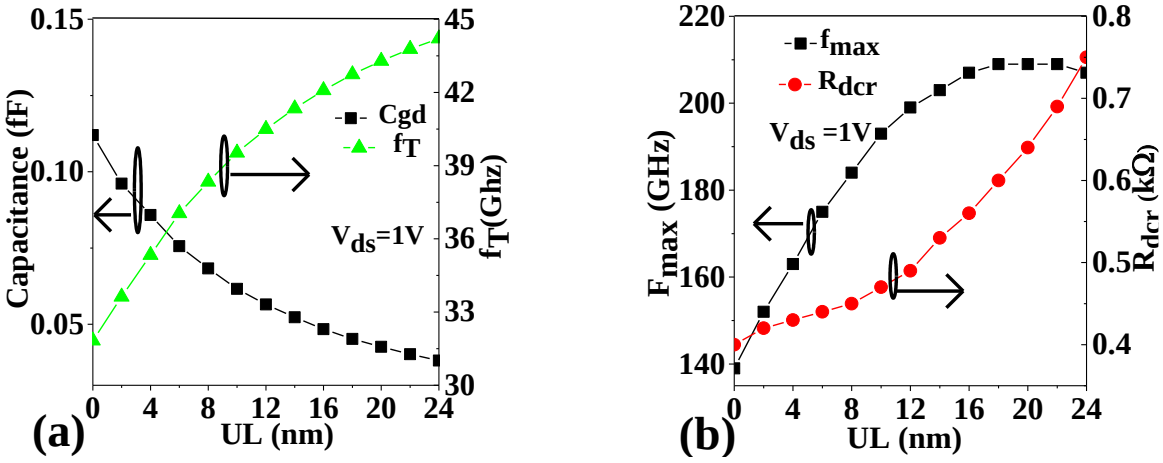

Figure 5.4: (a) Behaviour of C_{gd} and f_T characteristics with UL (b) Behaviour of F_{max} and R_{dcr} characteristics with UL (f_T and f_{max} values are extracted at 0.8 V of V_{gs})

Therefore, it suffers from Miller effect. Fig. 5.4(a) shows the UL variation effect on gate to drain capacitance. From the curve, it is observed that C_{gd} decreases when UL varies from 0 nm to 24 nm. This is because lower value of UL encroaches more doping concentration at drain-gate edge which is not suitable for DG-TFET performance in terms of OFF-state current and ambipolar behaviour as explained earlier. On other side for MOSFET, same trend will increase SCE [47], [50] in the device for the advance technology node. Total input capacitance (extrinsic + intrinsic) can be extracted from numerical ac simulation of DG-TFET as $C_{gg}=|\mathrm{Im}(Y_{11}+Y_{12})/\omega|$ where $\omega=2\pi f$, Here C_{gg} can be defined as C_{in} + C_{frin} (fringing capacitance including external and internal fringing components). The C_{frin} can simply be identified by limiting C_{gg} at zero or negative V_{gg}.

Fig. 5.4 (a) and Fig. 5.4 (b) also show f_T and f_{max} characteristics of the DG-TFET as a function UL extracted from the two port Y-parameter based on the ac device simulation with TCAD tool. Here, f_T is extracted when current gain drops to unity and fmax is extracted when masons's gain drops to unity. From the curve, it is clear that the increment in f_T is directly proportional to decrement of C_{gd} when UL changes from the 0 nm to 24 nm. However, it must be noted that as the UL is increased beyond 24 nm the increment in f_T as well as decrement in C_{gd} start saturating. Although, f_T depends on g_m and total gate capacitance but g_m of TFET does not change with variation in UL as happened in MOSFETs and also, shown in Table 5.1. On other hand, f_{max} behavior of DG-FET is described by g_m, g_{ds}, f_T, C_{gs}/C_{gd} and R_g where, R_g is the gate resistance which is sum of gate electrode resistance and distributed channel resistance (R_{dcr}). Here metal gate electrode is used in the simulation therefore gate electrode resistance is negligible. Unlike DG-FET, g_m and g_{ds} of DG-TFET are not altered significantly with gate-drain UL variation, therefore invariance of g_m and g_{ds} with UL will also not account for the variation in f_{max}. From fig 5.4(b), it is also evidence that f_{max} linearly increases with UL variation from 0 nm to 10 nm. The increment in fmax becomes sluggish when UL is between 12 nm to 18 nm because

increment in f_T and R_{dcr} affects f_{max} characteristic oppositely. Beyond 18 nm, f_{max} starts saturating and further it also starts decreasing due to dominance of R_{dcr}.

In this chapter we have presented Analog/RF performance attributes of gate-drain UL TFET for low power applications. We have demonstrated, parasitic resistance induced by gate-drain UL is not significant for DG-TFET, since the conduction concept differs from that of MOSFET. Further, device efficiency is also improved by gate-drain UL due to improvement in OFF-state current. Unlike DG-FET, g_m and g_{ds} are significantly unaffected by gate-drain UL variation, therefore the invariance variation of g_m and g_{ds} with UL variation will not account for the variation in f_T and f_{max}. Overall we concluded that, to improve the analog/RF efficiency of DG-TFET we only need to improve C_{gd} rather than the parasitic resistance as was in DG-FET.

Chapter 6

Attributes of Underlap and Dielectric Material for Tunnel FET Device Characteristics

The tunneling field effect transistor (TFET) and its analog/RF performance is being aggressively studied at device architecture level for low power SoC design. The UL and hetro-gate (HG) dielectric engineering in TFET technology improve the technological issues [35],[40].In previous chapter, Analog/RF performance attributes of gate-drain UL TFET for low power applications presented. The chapter demonstrated parasitic resistance induced by gate-drain UL is not significant for DG-TFET. Since, TFET suffers from low ON-state current and its ON-state current lower by two order as compared to conventional MOSFETs. Therefore the sensitivity of DG-TFET for induced parasitic resistance is less as compared to DG-FET. Therefore, it is necessary the underlap condition be studied under practically matched ON-state current condition such that channel resistance is same.

In MOSFET technology, UL architecture has been proposed to reduce SCEs and severe parasitic capacitances and consequently improve digital performance [17] as explained in the chapter 1. In order to achieve optimum analog/RF performance, trade-off between parasitic have been created for this UL structure. Further, in advanced MOS technology, UL architecture with high-k [16] and dual-k spacer [17] had been reported to improve the MOS device performance so that optimum performance for SoC design can be obtained. Unlike MOSFET, tunnel FET technology based on band to band tunneling conduction concept. So it is necessary to investigate the behavior for analog/RF performance of these structural variations.

Therefore, this chapter explain the influence of gate-drain underlap (UL) and different dielectric material for spacer and gate oxide on DG-TFET (double gate TFET) and its analog/RF performance for low power application. Here, the results demonstrate that the drive current behavior in DG-TFET with UL feature while using a different dielectric material for spacer is different in comparison to that of DG-FET. Further, the UL based hetero gate DG-TFET with low-k spacer (LK HGDG-TFET) is more resistive for drain induced barrier lowering (DIBL) as compared to DG-TFET with low-k spacer (LK DG-TFET). Along with that, as compared to DG-FET, this chapter also analyses the attributes of UL and dielectric material on analog/RF performance of DG-TFET in terms of transconductance (g_m), transconductance generation factor (TGF), capacitance, intrinsic resistance (R_{dcr}), cut-off frequency (f_T), and maximum oscillation frequency (f_{max}). Outcome of the results also suggest that LK HGDG-

TFET with gate-drain UL feature is a potential candidate for improvement the RF performance of device.

6.1 Device Structure and Simulation Setup

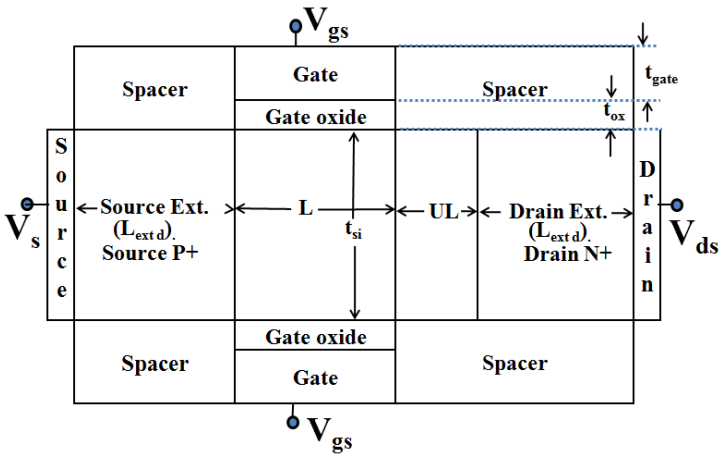

Figure 6.1 Device schematic of the n-channel gate-drain UL DG-TFET with spacer while for DG-FET, source P+ is replaced with n+ and device is optimized to minimize SCEs. UL is measured in nm.

The schematic cross sectional view of a planner n-channel DG-TFET is shown in fig. 6.1. In this device structure, gate-drain underlap (UL) has been considered only at drain side. Simulations are carried out with varying UL from 0 nm to 24 nm to get the device electrical behaviour. The gate-drain UL for 0 nm corresponds to without any UL for which the gate is exactly aligned with the metallurgical drain-channel junction. Here, L_{extd} is the source/drain extension length. Further, width of the spacer is computed from gate edges to source/drain end edges and metal contacts vertically placed at their end. Here, different dielectric insulator materials are used as spacer to investigate device behaviour. The gate drain UL structure has a gate dielectric length of L and dielectric may be of high-k or hetero gate dielectric (HG). In HG DG-TFET, gate dielectric length of L is the sum of high-k gate dielectric length (L_{hk}) and low-k gate dielectric length (L_{lk}). The gate dielectric of length L_{hk} and L_{lk} are placed at the source side and drain side respectively. Whenever HGDG-TFET is not mentioned, it is considered that gate oxide of length L has high-k dielectric material of permittivity 21.The source and drain are heavily doped p type and n type respectively for n-channel DG-TFET. The channel and UL region are intentionally undoped. Source-channel junction is also kept perfectly abrupt for improving the performance of the device [28].This is also same for high tunneling effect in ETFET [51], which needs a sharp and high drain doping. Drain doping uses Gaussian doping profile and followed by a doping gradient (σ_L) of 3 nm/decade. The device parameters of DG-TFET used in the simulation are shown in Table 6.1.

According to the study in [53], band to band tunneling probability (P_T) in tunnel FET through

Table 6.1. Parameter used for the DG-TFET simulation

Device Parameter	**Value**
Channel length (L)	45 nm
Silicon thickness (t_{si})	10 nm
Gate dielectric thickness (t_{ox})	3 nm
Width of the device (W)	1 µm
Drain doping concentration	1×10^{20} cm^{-3}, n-type
Channel and UL doping concentration	1×10^{17} cm^{-3}, p-type
Source doping concentration	1×10^{20} cm^{-3}, p-type
Drain voltage (V_{ds})	1 V
Source voltage (V_s)	0 V
Gate voltage (V_{gs})	0 V to 1V
SiO_2 material permittivity	3.9
Si_3N_4 material permittivity	7
HfO_2 material permittivity	21
L_{hk} (High-k length in HG)	12 nm
L_{lk} (Low-k length in HG)	33 nm
Source/Drain extension length	60 nm
Underlap (UL)	0 nm to 24 nm

tunneling barrier can be analytically calculated by considering a triangular potential barrier with the WKB [28] approximation. With the above approximation, tunneling probability (P_T) and tunneling current I_{BBT} have been estimated by equation (6.1) where m^* is the effective mass and E_g is band gap of the material, $\Delta\phi$ is the

$$I_{BBT} \alpha P_T \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3qh\left(E_g + \Delta\Phi\right)} \right) \tag{6.1}$$

energy range over which tunneling can take place. In order for band-to-band tunneling to take place in materials with an indirect band gap such as silicon, crystal phonons are necessary in order to conserve momentum [54] therefore the model is modified, and energy gap of semiconductor (E_g) is replaced by E_g-E_p, where E_p is the phonon energy. The effective mass must then change to reduced effective mass in the tunneling direction [55]. Here λ is the screening tunneling length of the electrical potential, consisting of two contributions: $\lambda = \lambda_{doping} + \lambda_{geo.}$ λ_{doping} reflects the steepness of the doping profile at the tunneling junction and λ_{geo} is determined by the device geometry and technological device parameters such as dielectric material for both gate oxide and spacer. The high-k gate dielectric material increases the electrostatic coupling between gate electrodes and tunneling junction which causes improvement in λ [56]. However, high-k dielectric for spacer depletes the source region near the gate due to fringing field with application of gate voltage which causes tunneling current to reduce. This is mainly due to the increased value of λ for high-k spacer as compared to low-k spacer [56].

The device has been simulated using the nonlocal hurkx band-to-band tunneling (BTBT) model available in Silvaco Atlas [46]. Since the tunneling process is nonlocal therefore this model requires a

special fine mesh to be applied around the area where the tunneling can take place. The model parameters were calibrated against experimental Zener diode characteristics published by Fair and Wivell [57].The effective mass parameters, electron mass (relative effective mass of electron, m_e) and hole mass (relative effective mass of hole, m_h) have been taken 0.24 and 0.36 respectively to calibrate the nonlocal model as shown in fig. 6.2(a). The calibrated nonlocal model with a careful WKB method is applied in our design device. Device current components in OFF state region are ambipolar current, SRH (Shockley-Read-Hall) and TAT (trap assisted tunneling). Here, OFF-state voltage (V_{off}) is the minimum value of V_{gs} at V_{ds} of 1V when drain current shows a minimum value. For $V_{gs} \leq V_{off}$, we have the following two definition depending upon drain-channel barrier in TFET device: 1) V_{off} is the value of V_{gs} when current changes from p-i-n leakage to ambipolar conduction 2) V_{off} is the value of V_{gs} when the drain current I_d shows a minimum, where ambipolarity is present for relatively low value of V_{gs} as shown in fig. 6.2(b). SRH recombination model is included with default parameters. Gate leakage current was neglected in these simulations. Although OFF-state current is limited by TAT at high temperature [60] therefore, TAT is not considered for this study. Further, taking into account the high doping concentration in the source and drain region, band gap narrowing model is also included with other physical model such as concentration, field dependent mobility and Fermi-Dirac statistics. Further, the spacer dielectric constant changes threshold voltage as explained in [38]. Therefore, for fair comparisons between LK spacer based DG-TFET (LK DG-TFET) and HK spacer based DG-TFET (HK DG-TFET), the gate work function is adjusted so that turn-on point ($\geq V_{off}$) becomes 0.2 V. After that it is found that ON-state current 2.23 times larger for LK DG-TFET as compared to high-k spacer with permittivity 21 based HK DG-TFET. Fig. 6.2(b) shows the transfer characteristics with UL=12 nm at V_{ds}=1V for the spacer with k=3.9 (SiO_2), k=7 (Si_3N_4) and k=21 (HfO_2). SOI MOSFETs are also considered in this paper, which have the same structure as the TFET as shown in fig. 1. Furthermore, the analog/RF figures of merit have been extracted from the Y-parameter matrix generated by performing the small-signal ac analysis.

6.2 Attributes of UL and Dielectric Material

6.2.1 Ambipolar Characteristics

Fig 6.2 (c) shows, the I_{amb} current behaviour of DG-TFET with gate-drain UL variation for different dielectric material of spacer. Without an UL, The TFET is an ambipolar device [35] and conducts when $V_{gs} \leq V_{off}$ with band to band tunneling (BTBT) occurring at the metallurgical drain-channel junction. In TFET, gate-drain UL is used to reduce the ambipolar effect [35] and improves the OFF state current. Inset of fig. 6.2(c) shows the lateral electric field as a function of UL and different dielectric material of spacer such as, SiO_2 is used for LK and HfO_2 is used for HK. The peak value of

lateral electric field (E) has been taken 1 nm below the oxide-silicon interface towards the drain-channel junction at V_{gs}=0V and V_{ds}=1V. The value of electric field reduces when UL varies from 0 nm to 24 nm thus, it causes ambipolar reduction and the reduction in E is more sensitive for LK spacer based DG-TFET. It is observed, after 12 nm of UL, the reduction in E get sluggish and ambipolar current achieves its minimum value for LK spacer based DG-TFET. However, peak electric field at source-channel junction remain constant for aforementioned variation of UL.

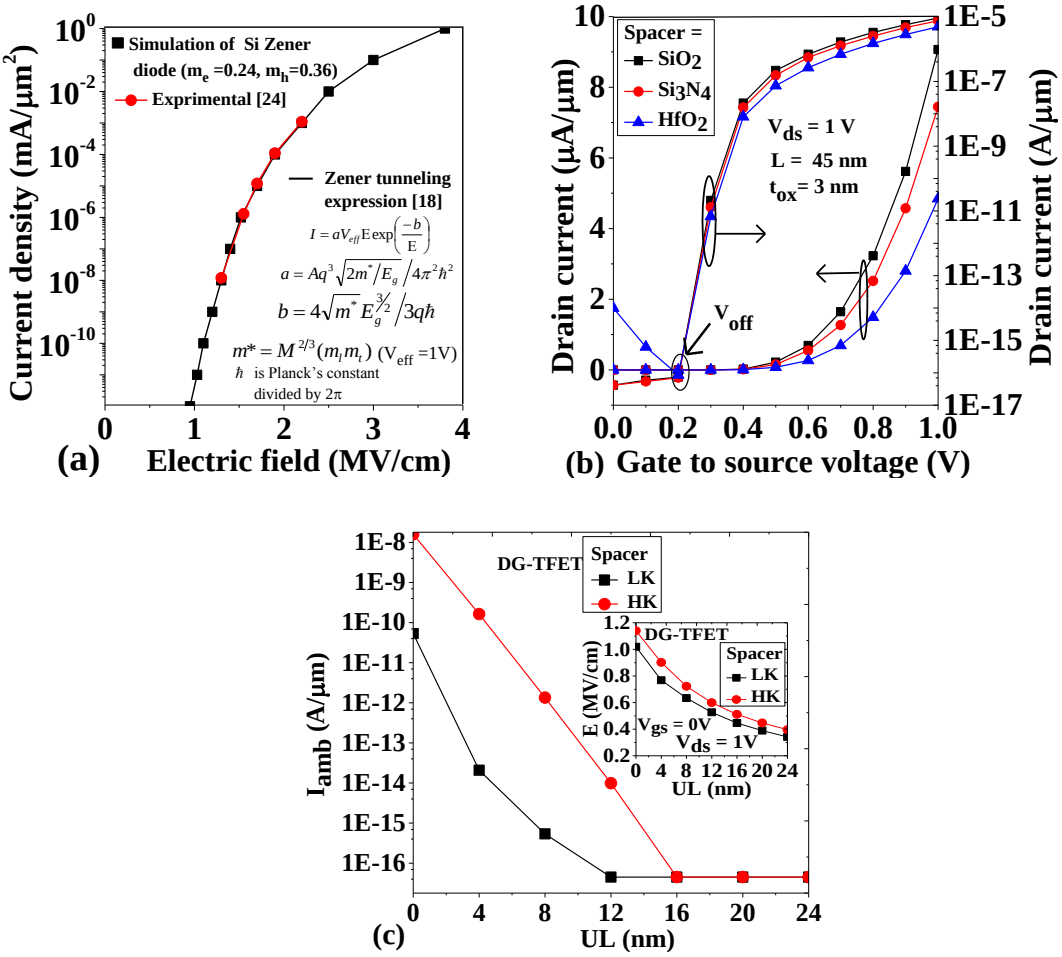

Figure 6.2. (a) Simulation of Si Zener diode with a reverse junction bias of 1V fitted to solid line given by Zener tunneling expression [28] using the experimental data of Fair & Wivell [57]. The drain current flows across a degenerated doped p^+-n^+ tunnel junction (b) Transfer characteristics of DG-TFET with different spacer dielectric (c) behaviour of ambipolar current (I_{amb}) with UL variation for DG-TFET with LK and HK spacer

6.2.2 ON-state Current Characteristics

Fig. 6.3(a) shows the behaviour of transfer characteristics with UL variation for LK DG-TFET. Here, for fair comparisons between DG-TFET and DG-FET, the gate voltage is varied up to 3 V to achieve approximately same current level as in DG-FET in fig. 6.3(b). It is observed that LK DG-TFET does not show the variation in driving current (ON-state current) with UL variation from 0

nm to 24 nm. Such behaviour is expected when we consider that the series resistance in TFET consists of channel resistance and tunneling barrier resistance. Change in length or doping concentration affects the channel resistance whereas changing the cross section area affects the tunneling barrier resistance.

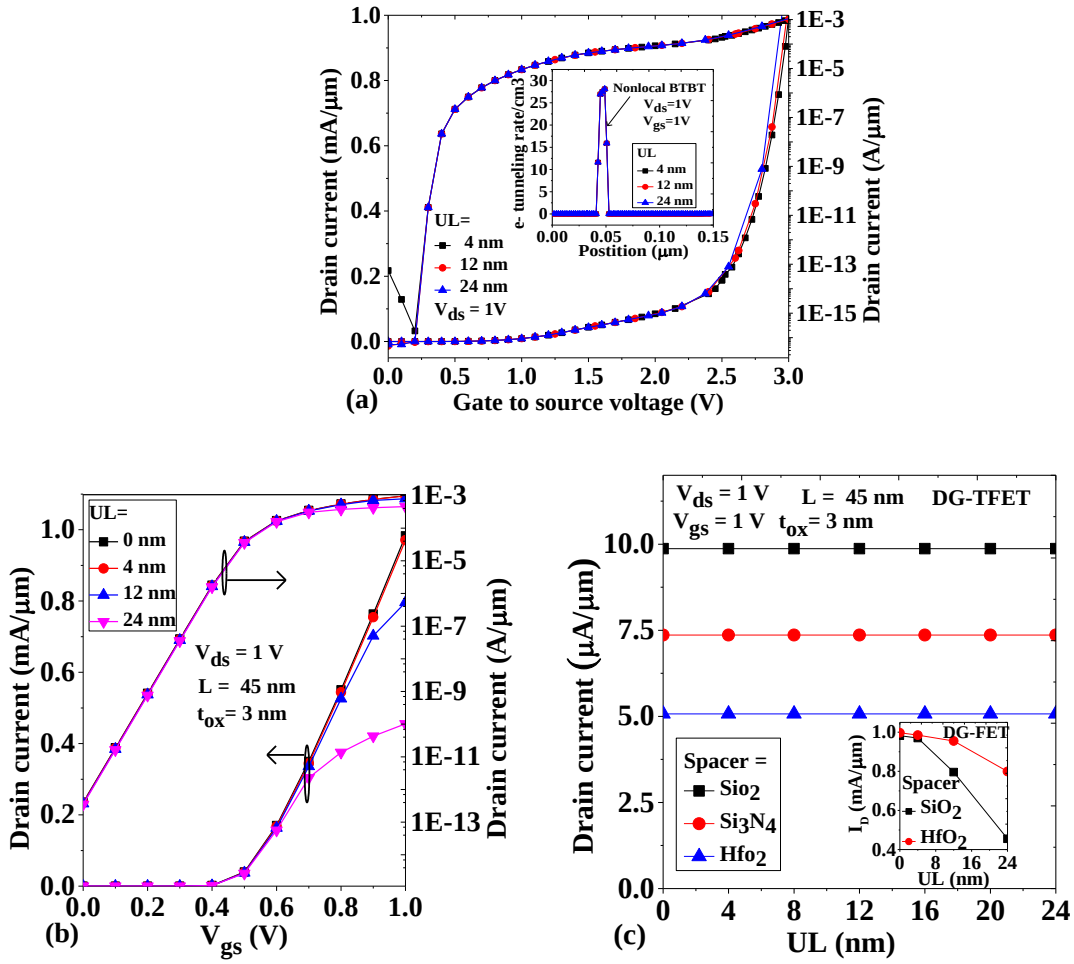

Figure 6.3. (a) Behaviour of transfer characteristics with UL variation of DG-TFET with LK spacer dielectric_(b) Behaviour of transfer characteristics with UL variation of DG-FET with LK spacer dielectric (c) Behaviour of ON-state current (I_{on}) with UL variation of DG-TFET with different spacer dielectric.

However, the TFET conduction concept is based on band to band tunneling and from the inset of fig. 6.3(a), the tunneling carrier at source-channel junction remains same for UL variation. Therefore, it can be concluded that increment in channel resistance due to increase in UL length of DG-TFET does not vary the overall series resistance and consequently the driving current remains same. On the other hand MOSFET conduction concept is based on thermal injection of charge carrier from source to channel. Fig. 6.3(b) shows the behaviour of transfer characteristic with UL variation for LK spacer based DG-FET. The curve indicates that driving current obtained in the DG-FET decreases with variation of UL from 0 nm to 24 nm due to increase in parasitic resistance. The behaviour of DG-FET indicates that the current in it is more sensitive to varying parasitic resistance when compared to DG-

TFET also in DG-FET, UL feature in Source/Drain region reduces SCEs. However, this profile induces parasitic resistance which degrades analog/RF characteristics [47], [49], [50], [52]. Further, the effect of different dielectric spacer material as a function of gate-drain UL is also analyzed for DG-TFET and the behavior is compared with DG-FET. Fig. 6.3 (c) shows variations in driving current with varying gate-drain UL at V_{ds}=1 V and V_{gs}=1V for different spacer with k=3.9 (SiO_2), k=7 (Si_3N_4) and k=21 (HfO_2). As compared to HK DG-TFET, ON-state current is higher LK DG-TFET due to the non-depletion of source on the gate side which causes more tunneling current flow on the surface. Here again, driving current is not sensitive to variation in parasitic resistance due to UL variation with different dielectric material for spacer, the reason behind which is stated earlier. On the contrary, in DG-FET high-k spacer improves the coupling between gate electrode and UL region when compared to low-k spacer causes improvement in ON-state current due to fringe induced barrier lowering. Therefore, the gate fringe induced barrier lower is responsible for reducing the series parasitic resistance. This analysis concludes that the behaviour of ON-state current in DG-FET is different as compared to DG-TFET with UL as well as spacer variations. Thus, the sensitivity of driving current against parasitic resistance affects analog/RF FoM of DG-TFET in a different manner when compared to DG-FET.

6.2.3 DIBL Characteristics

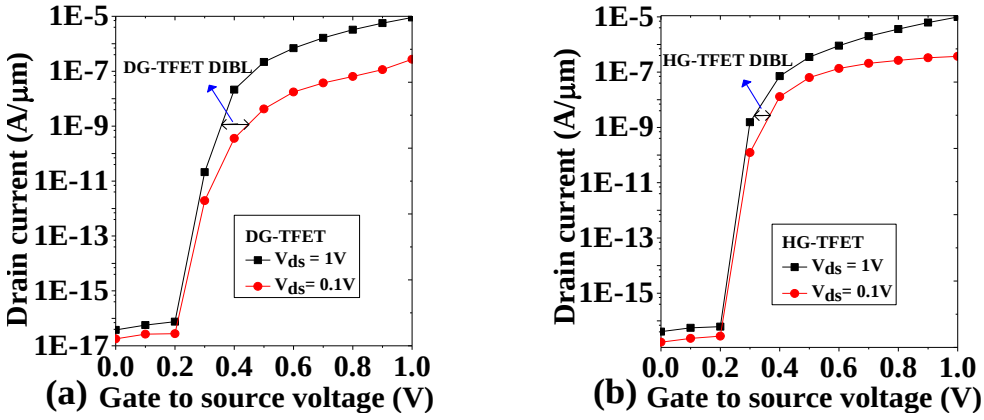

Figure 6.4. DIBL effect in (a) DG-TFET with LK-spacer dielectric (b) HG DG-TFET with LK-spacer dielectric.

Fig. 6.4 shows the DIBL effect in DG-TFET and HG-TFET for 12 nm of UL with low-k spacer. HG-TFET is optimized according to ref [40]. Here in DG-TFET, DIBL is a measurement of gate voltage shift at a constant drain current (10^{-8} A/μm) for the transfer characteristics of V_{ds}=1 V and V_{ds} =0.1 V. The shift in V_{gs} (marked in fig. 6.4) is found to be 177 mV for the LK DG-TFET and 52 mV for the HG DG-TFET. Therefore, the lower value of DIBL for LK HGDG-TFET indicates the device is more suitable for SoC design.

6.3 Impact of Dielectric and UL on Analog/RF Characteristics

6.3.1 Analog Characteristics

Fig. 6.5 shows, the transconductance (g_m) and conductance (g_{ds}) characteristics as the function of UL and dielectric spacer material. From the curve, it is clear that g_m and g_{ds} value are higher for the low-k spacer based HG DG-TFET as compared to other considered TFET structures due to improved SS and higher I_{on} [40]. However, the behaviour of characteristics does not change with UL variation from 0 nm to 24 nm. The reason behind such rigid behaviour is that tunneling areas as well as number of tunneling carrier do not change at source-channel junction with UL variation as explained earlier. On the other hand, the degradation in g_m and g_{ds} of DG-FET are due to incremental parasitic resistance and gate losing its control in the extension region for aforementioned variation of UL [1],[23],[47].The degradation is more severe for LK spacer. This is due to the higher parasitic resistance as compare to HK spacer, the reason is stated earlier.

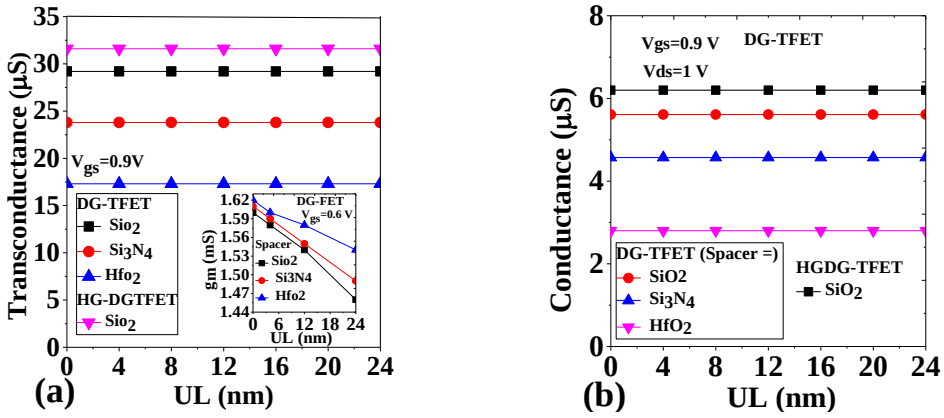

Figure 6.5. Behaviour of DG-TFET for (a) g_m and (b) g_{ds} characteristics as a function of UL variation and different dielectric material for spacer

Fig. 6.6(a) shows the UL variation effects on transconductance generation efficiency, g_m/I_{ds} (TGF) for DG-TFET as a function of gate voltage. If the value of TGF is higher, then it indicates that the capability to deliver ac gain is stronger which is requirement for analog/RF application. In TFET, the conduction concept is based on band to band tunneling, therefore it does not have SS limitation. So, initially its value is large as compared to DG-FET whose ideal value is equal to 36 V^{-1}.With increasing gate voltage, TGF of DG-TFET degrades; it indicates that power consumption also increases. It is observed that the initial value of TGF for DG- TFET is 44.92 V^{-1} and 128 V^{-1} for UL=0 nm and UL=12 nm respectively. The higher value of TGF for UL= 12 nm is due to lower OFF-state current as compared to UL= 0 nm. The TGF value becomes equal for various UL at gate voltage equal to 0.4 V because after this available gain (g_m) per unit value of power dissipation become equal. This is due to

induced parasitic resistance with UL as explained earlier. So, this analysis for DG-TFET concludes that higher value of UL is more efficient for TGF initially. Fig. 6.6(b) shows g_m/I_{ds} as a function of V_{gs} for different spacer material of DG-TFET and HGDG-TFET. It is observed that initially TGF value is higher for HGDG-TFET among the other spacer based DG-TFET structures. This is due to higher

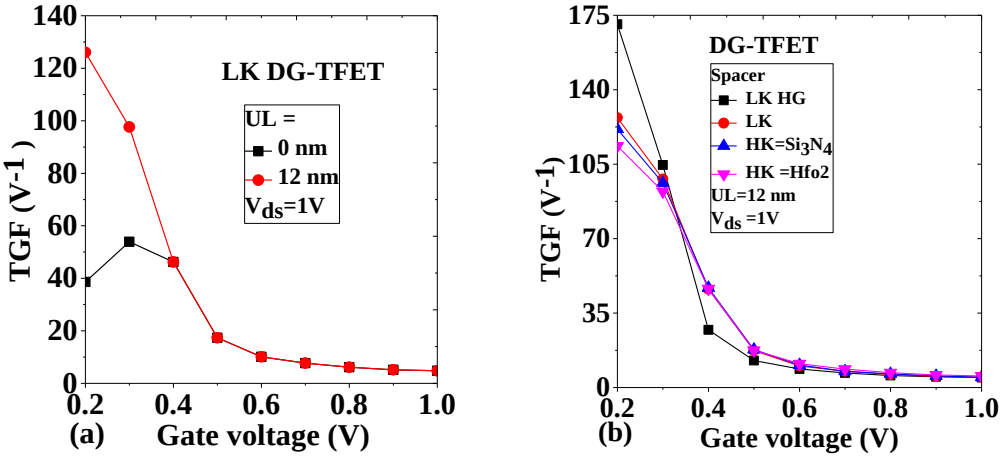

Figure 6.6. Behaviour of TGF (g_m/I_{ds}) of DG-TFET with gate voltage variations (a) as a function of UL variation for low-k spacer (b) as a function of different dielectric material for spacer and gate dielectric.

value of g_m and SS value for HGDG-TFET between 0.2 V to 0.35 V of gate voltage. After this voltage range, TGF value of HGDG-TFET has lower value as compared to the other structures. This is mainly due to lesser available gain for per unit value of power dissipation. On the other side for DG-FET, HK spacer improves g_m as compare to LK spacer based DG-FET as explain earlier and consequently g_m/I_{ds} improves significantly [16].

6.3.2 RF Characteristics

Fig. 6.7(a) shows the C_{gd} capacitance value of DG-TFET and HGDG-TFET with different dielectric spacer material. The intrinsic capacitance formation of TFET is different from the MOSFET as explained in the literature [22]. It was shown that C_{gd} of TFET constitutes larger fraction of total gate capacitance (C_{gg}) in both linear and saturation region therefore it suffers from Miller effect. Initially, C_{gs} consists of only parasitic capacitance and this value decreases slightly as inversion layer form [22]. The C_{gd} in LK HGDG-TFET has low value as compared to HK DG-TFET and LK DG-TFET. This is because of the low value of fringing capacitance as compare to HK DG-TFET and also high-k dielectric in HGDG-TFET is placed only for a source side gate dielectric therefore total C_{gg} capacitance is also lower than LK DG-TFET.

The schematic shown in fig. 6.1(a), the total parasitic (extrinsic) gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitance (not taking overlap capacitance into consideration as source-channel and drain-channel junction abruptly change) are expressed as C_{gse} (parasitic) = $C_{outer,fring}$ + $C_{Sinner,fring}$ and C_{gde}

(parasitic) = $C_{outer,fring}$ + $C_{Dinner,fring}$., where,$C_{outer,fring}$ is the external electric field which is bias dependent and comprises of the capacitance between the gate and the SDE(source drain extension) region. $C_{Sinner,fring}$ and $C_{Dinner,fring}$ are internal fringing electric fields respectively which depend on source and drain doping profile. Fig. 6.7(b) shows the UL variation effect on gate-drain parasitic

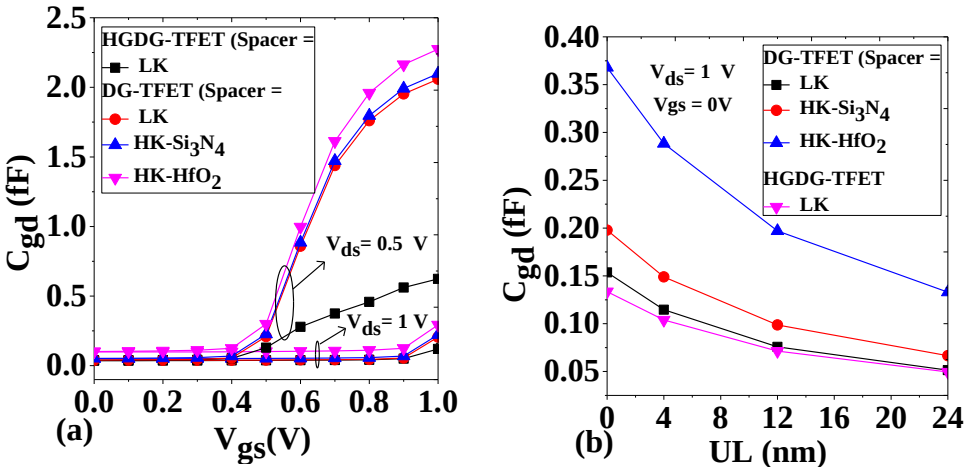

Figure 6.7 (a) C_{gd} characteristics of DG-TFET (UL=12 nm) as a function of gate voltage and different dielectric material of spacer (b) C_{gde} (gate-drain parasitic capacitance) characteristics of DG-TFET as a function of UL and different dielectric material of spacer

capacitance (C_{gde}). From the curve, it is observed that C_{gd} decreases when UL varies from 0 nm to 24 nm. This is because higher value of UL reduces doping concentration at drain gate edge causes reduction in fringing capacitance which is suitable for DG-TFET performance in terms of reduction in C_{gd} and ambipolar conduction. From the curve it is also clear that after 12 nm of UL, reduction in C_{gd} sluggish and ambipolar behaviour almost saturate as it has been established earlier. Here, LK DG-TFET has the lowest parasitic (C_{gde}) value as compare to HK DG-TFET due to reduced value of fringing field between gate electrode and UL. Total input capacitance (C_{gg} = C_{gs}+C_{gd}), C_{gs} and C_{gd} have been extracted from Y-parameter matrix generated by numerical ac simulation of DG-TFET as

$$C_{gg} = \frac{\mathrm{Im}(Y11)}{\omega}, \quad \text{if the definition of } C_{gg} \text{ is: } C_{gg} = \frac{dQ_g}{dV_g} \tag{6.2}$$

$$C_{gd} = -\frac{\mathrm{Im}(Y12)}{\omega} \quad \text{if the definition of } C_{gd} \text{ is: } C_{gg} = \frac{dQ_g}{dV_d} \tag{6.3}$$

where $\omega=2\pi f$, Here C_{gg} can be defined as = C_{in} + C_{frin} (fringing capacitance including external and internal fringing components). The C_{frin} can simply be identified by limiting C_{gg} at zero or negative V_{gg}.

Fig. 8 shows f_T and f_{max} characteristics as a function of V_{gs} with implementing different dielectric material for spacer, extracted from two ports Y-parameter based on the ac device simulation with TCAD tool. Hence f_T is extracted when current gain drop to unity (Y_{21}/Y_{11}=1). From the curve it is

observed that f_T increases first and then decreases after reaching the peak value due to increase in the total gate capacitance and limiting to g_m. It is also found from the capacitance curve that HK DG-TFET has higher fringing capacitance and lower transconductance as compare to LK DG-TFET. Therefore, f_T of LK DG-TFET is improved by 250% as compared to HK DG-TFET. Further, HGDG-

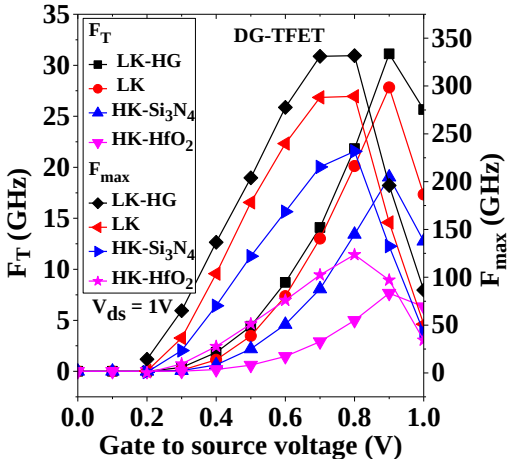

Fig. 8. f_T and f_{max} characteristics of DG-TFET as a function of gate voltage for different dielectric material of spacer (UL=12 nm)

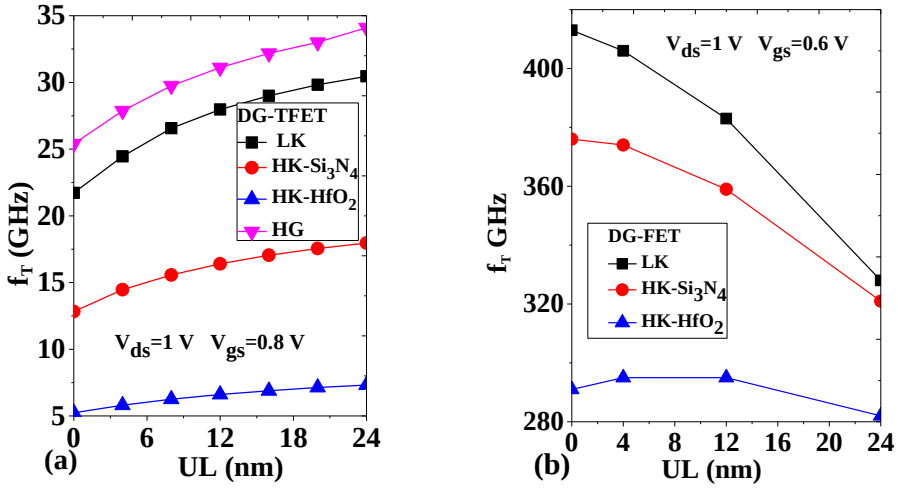

Figure 6.9. f_T characteristics of (a) DG-TFET and (b) DG-FET as a function of UL variation and different dielectric material of spacer

TFET improves f_T by 15% as compared to LK DG-TFET. This is due to lower intrinsic capacitance and higher value of g_m. Further, f_T behaviour is also discussed with UL variation for different dielectric spacer material and same is compared with DG-FET in fig. 6.9. From the curve it is clear that the increment in f_T is directly proportional to decrement of C_{gd} when UL changes from 0 nm to 24 nm. However, it must be noted that as the UL is increased beyond 12 nm, the increment in f_T as well as decrement in C_{gd} start saturating. Although, f_T depends on g_m and total gate capacitance but g_m of TFET does not change with variation in UL as explained earlier, hence the frequency performance sensitive to change in value C_{gg}. It is found that f_T of HGDG-TFET improves by 28% when UL changes

from 0 nm to 12 nm. In DG-FET, as observed earlier g_m is highly sensitive and decreases for LK DG-FET as compare to HK DG-FET with gate-drain UL variation from 0 nm to 24 nm. Therefore degradation in f_T is higher in LK DG-FET as conformed from fig. 6.9 (b).

Using normal equivalent circuit approach, f_{max} of a conventional MOSFET can be expressed as [13], [47], [50], and [52]

$$f_{\max} = \frac{f_T}{\sqrt{4R_g.\left(g_{ds} + 2\pi f_T C_{gd}\right)}} \tag{6.4}$$

The f_{max} behaviour of DG-FET is described by g_m, g_{ds}, f_T, C_{gd} and R_g. where R_g is the gate resistance which is sum of gate electrode resistance and distributed channel resistance (R_{dcr}). Here, metal gate electrode is used in the simulation therefore gate electrode resistance is negligible. Fig. 6.10 (c) shows, f_{max} characteristics of DG-FET as a function of UL variation and different dielectric material of spacer.

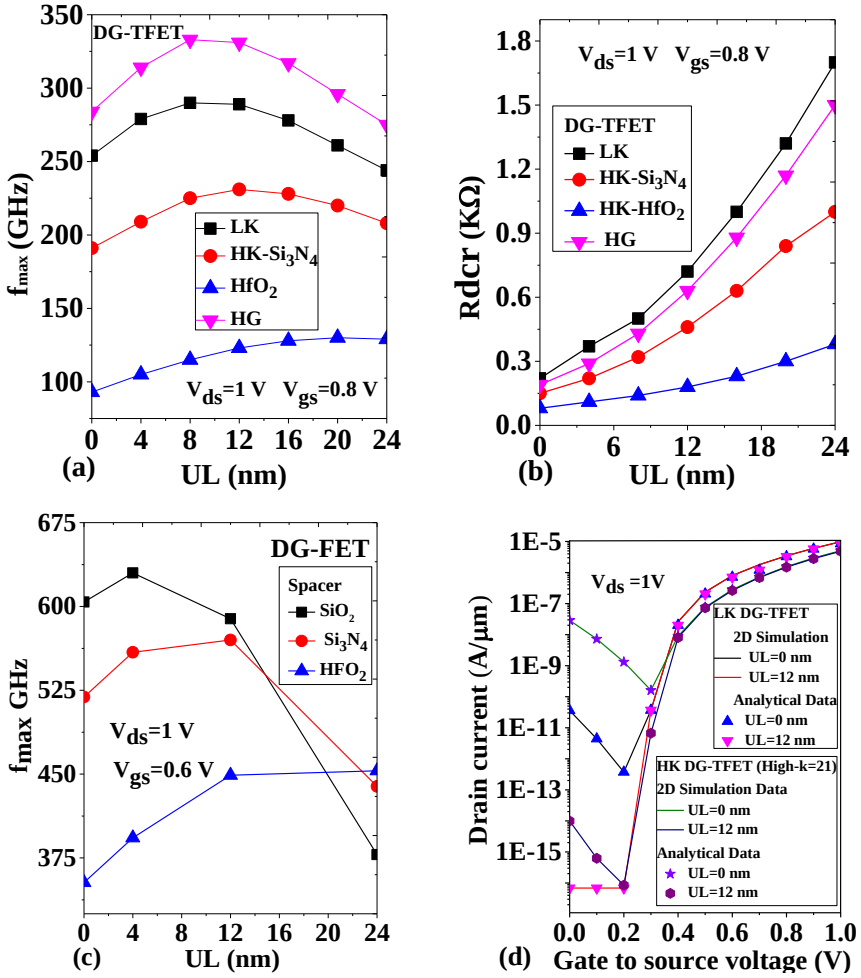

Figure 6.10. Characteristics of DG-TFET (a) f_{max} (b) Rdcr as a function of UL variation and different dielectric material of spacer (c) characteristics of DG-FET as a function of UL variation and different dielectric material of spacer (d) calibration of our simulated I_d-V_{gs} characteristics for LK/HK DG-TFET (device parameter used as given in Table I)

However in DG-TFET, the g_m and g_{ds} are not altered significantly with gate-drain UL variation as it is explained earlier. Therefore invariance of g_m and g_{ds} with UL will also not account for the variation in f_{max}. From fig. 6.10 (a), it evidences that, for LK DG-TFET, f_{max} increases with UL variation from 0 nm to 10 nm and increment get sluggish when UL is between 10 nm to12 nm. The trend of f_{max} is due to dominance of the f_T behaviour between the UL ranges. After 12 nm, f_{max} decreases due to control of Rdcr become effective over f_T. As compared to LK DG-TFET, f_{max} in HK DG-TFET has low value and increment in f_{max} also sluggish when UL changes from 0 nm to 24 nm. This behaviour is mainly due to increment in f_T and Rdcr also get sluggish as conformed from Fig. 6.10 (a) and (b)

In Table 6.2, analog/RF parameters are extracted for UL variation with different dielectric material for spacer and gate oxide at V_{gs} =0.5 V which is the targeted Tunnel FET bias range. The results clearly show that the LK HGDG-TFET with gate-drain UL feature has improved value for RF performance due to reduce value of gate-drain capacitance. Overall we conclude that, to improve the analog/RF efficiency of TFET technology, need to improve C_{gd} rather than the parasitic resistance as was in DG-FET.

Table 6.2. Comparison of Analog/RF Figure of Merit of DG-TFET with UL Variation while using dielectric Material for Spacer. (Here, LKHG means Hetero Gate Dielectric with LK Spacer. HK means HK Spacer for DG-TFET. LK means LK Spacer for DG-TFET.)

Analog/RF parameter	DG-TFET UL= 0 nm, V_{gs}=0.5 V			DG-TFET UL= 12 nm, V_{gs}=0.5 V		
	LK HG	LK	HK	LK HG	LK	HK
C_{gd} (fF)	0.07	0.08	0.2	0.04	0.05	0.1
g_m (µS)	4.44	3.61	1.39	4.44	3.61	1.39
g_{ds} (µS)	0.35	0.22	0.08	0.35	0.22	0.08
TGF (V^{-1})	13	17.4	17.6	13	17.4	17.6
f_T (GHz)	3.91	2.85	0.5	5	3.5	0.61
f_{max} (GHz)	171	143	40	206	177	60
GBW (GHz)	1.03	0.71	0.11	1.8	1.3	0.22

6.4 Analytical Verification

Mobile charge have a negligible effect on the electrostatics of the device in the transition from ON-state to OFF-state. The Poisson equation can, therefore, be written as [2]

$$\frac{\partial^2 \phi(x,y)}{\partial\, \phi x^2} + \frac{\partial^2 \phi(x,y)}{\partial\, \phi y^2} = -\frac{-qN_j}{\varepsilon_{Si}} \tag{6.5}$$

Where $\phi(x,y)$ is the electrostatic potential in the region of consideration, N_j is the film doping where j=1,2,3…, N_1 is the P+ source doping , $\pm N_2$ is the lightly doped channel, $-N_3$ is the n+ drain doping

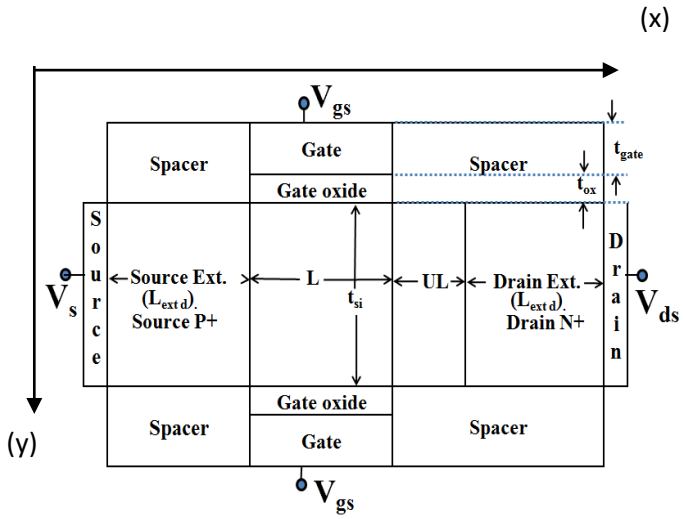

Fig. 6.11 Device schematic of the n-channel gate-drain UL DG-TFET with LK/HK spacer

The potential along the y-direction can be approximated by the second order polynomial for double gate device

$$\phi(x,y) = c_0(x) + c_1(x)y + c_2(x)y^2 \tag{6.6}$$

Imposing the boundary condition of continuity of surface potential and electric field in the y-direction at Y=0 and Y=t_{si} and resulting resultant equations [58], we can get a 1-D differential equation in the front gate surface potential ϕ_s

$$\frac{\partial^2 \phi_s(x)}{\partial x^2} - k^2 \phi_s(x) = -k^2 \phi_c \tag{6.7}$$

With $k = \sqrt{2\eta / t_{Si}^2}$ and $\phi_c = -\frac{t_{Si}^2}{2\eta}\left[\frac{qN_j}{\varepsilon_s} - \frac{2\eta}{t_{Si}^2}\phi_g\right]$ (6.8)

ϕ_g = gate potential, η = capacitance ratio of gate oxide and silicon film = C_{ox}/C_{Si} , C_{ox} is the gate oxide capacitance (for the intrinsic channel region) = ε_{ox}/t_{ox} ,the fringing field effect due to gate voltage in the source and drain region causes depletion is taken into account by conformal mapping techniques , giving the oxide capacitance as $C_{ox} = 2/\pi \times \varepsilon_{ox}/t_{ox}$. The silicon film capacitance is $C_{Si} = \varepsilon_{Si}/t_{Si}$.

The parameters k and ϕ_c have particular values in the three different regions, i.e. the source, the channel and the drain.

Equation (4) is solved individually for each region (source, channel and drain). The solution for the each region is

$$\phi_{s,j}(x) = a_j e^{-k j (x - x j)} + b_j e^{-k j (x - x j)} + \phi_{cj} \tag{6.9}$$

Where k_j and ϕ_{cj} are the parameters defined in (5). The coefficient a_j and b_j are defined according to [58] and solution for surface potential along the y-direction can be obtained using (3) and (6). The electric field can be calculated using the partial derivatives of the potential in the x and y direction respectively

$$E_{x,j}(x,y) = k_j(a_j e^{-k(x-xj)} - b_j e^{-k(x-xj)})(1 + \eta y/t_{si} - \eta y^2/t_{si}^2) \tag{6.10}$$

$$E_{y,j}(x,y) = -c_1(x) - 2c_2(x)y \tag{6.11}$$

Numerical integration of the band to band generation rate G_{btb} gives the drain current I_d:

$$I_d = q\int G_{btb} dV \tag{6.12}$$

The generation rate is given by Kane's model [46] as

$$G_{btb} = A\frac{|E^2|}{\sqrt{E_G}}\exp[-B\frac{E_G^{3/2}}{|E|}] \tag{6.13}$$

where E_G is the silicon band gap and $|E| = \sqrt{E_x^2 + E_y^2}$ is the electric field at the given point. The electric field is calculated analytically according to work given by reference [58] for LK DG-TFET and HK DG-TFET in which considering the junctions depletion region inside the source and the drain. The Kane's parameter A and B are given by the expression $A = \frac{q^2\sqrt{2m_{tunnel}}}{h^2}$, $B = \frac{\pi^2\sqrt{m_{tunnel}/2}}{qh}$ using $\left(\frac{1}{m_{tunnel}}\right) = \left(\frac{1}{m_{ee}}\right) + \left(\frac{1}{m_{eh}}\right)$ $m_{eh} = m_h m_0$, $m_{ee} = m_e m_0$, m_e and m_h are the electron and hole effective masses respectively and the masses are taken to be equal to the masses obtained by ATLAS model calibration with experimental data. *h* being Planck's constant, and q being the electronic charge. The accuracy of the analytical calculation for LK DG-TFET and HK DG-TFET are verified by comparing the results with 2D numerical simulation as shown in fig. 6.10 (d). In a HK/LK DG-TFET, the length of depletion inside source/drain can be calculated from the potential drop across the junction [28].The curve also confirms that LK DG-TFET has higher current as compared to HK DG-TFET. This is mainly due to lower value of fringing capacitance for a low value of k of the spacer, result in improved value of screening tunneling length (λ) and electric field [56], [57-59].

Chapter 7

Conclusions and Scope for Future Work

In this thesis, drain extension feature for tunnel FET and its analog/RF performance for various device engineering such as symmetric and asymmetric source/drain doping profile, gate-drain UL feature and spacer engineering have been presented for future low power SoC applications.

The effect of UD and GD profile within the drain extension region on the DG-TFET performance is presented. It is shown that asymmetric drain doping profile (GD) improves the TFET performance in terms of SS slope and suppression of ambipolar conduction, which makes a TFET suitable for the low-power circuit design. Further, the gradual variation of doping in the drain extension region is also responsible for improving the RF figures of merit due to a reduction of gate-to-drain parasitic capacitance. Furthermore, the effect of the CL of Gaussian drain doping profile on the TFET for RF application is also discussed under the variation of the channel length. The result demonstrates the feasibility of lateral asymmetric drain as a way to improve the RF figures of merit for low-power design application significantly.

Further, LAD doping and L_{extd} variation on DG-TFET for device and its analog/RF performance are discussed, including the impact of the parasitic on DG-TFET performance with respect to DG-FET. Due to the different conduction concept as compared to MOSFET, the impact of parasitic is different in DG-TFET. Parasitic resistance induced by the SDE region and lateral graded doping profile in drain extension region are not significant to the total series resistance which does not influence the ON-state current of DG-TFET. Further, study on variation of L_{extd} shows ambipolar behavior, gate-drain capacitance, delay and f_{max} are increased whereas f_T is reduced continuously with increasing doping concentration in drain-channel junction at the drain side for asymmetric DG-TFET. Thus, in case of DG-TFET variation in f_T and f_{max} are mainly dependent on the change in C_{gd} and does not vary significantly with g_m and g_{ds} as it happens in case of a DG-FET.

Finally, we have demonstrated attributes of gate-drain UL and dielectric material for DG-TFET. The result shows that On-state current of DG-TFET is not sensitive for induced parasitic resistance due to UL with different dielectric material of spacer unlike DG-FET where UL reduces On-state current and the degradation is improved by HK spacer. It has been also presented that LK HGDG-TFET has improved DIBL as compared to LK DG-TFET. Further, we have also presented its impact on analog/RF performance and same compared with DG-FET behaviour. For analog performances, TGF is improved by gate-drain UL and initially its value is higher for UL based LK HGDG-TFET as compare to UL based LK DG-TFET and HK DG-TFET structures. However in UL based DG-FET,

TGF has improved with HK spacer. Unlike DG-FET, g_m and g_{ds} of DG-TFET are significantly unaffected by gate-drain UL variation. Therefore for RF performance, the invariance variation of g_m and g_{ds} with UL variation will not account for the variation in f_T and f_{max}. The result shows that with UL feature, f_T and f_{max} in LK HGDG-TFET improved by 28% and 17% respectively when UL changed from 0 nm to 12 nm. Also f_T and f_{max} are improved by 370% and 170% respectively as compare to HK DG-TFET for UL=12 nm. Further analog/RF parameter in Table 5 clearly shows that the LK HGDG-TFET with gate-drain UL feature has potential for RF performance. Overall we concluded that, to improve the analog/RF efficiency of TFET we need to improve C_{gd} rather than the parasitic resistance as was in DG-FET.

This investigation, which is made by numerical simulation, would be beneficial for a new generation of RF circuits and systems in a broad range of applications and operating frequencies covering RF spectrum. In addition, the results can be useful to other researchers for the development of robust compact models for analog/RF parameters. In a developing field where experimental results are still limited, these simulations can even be essential, since they allow the variation of a large number of parameters in a short amount of time. In this way, the work presented here can further our understanding of this emerging device, and can contribute to the progress made in future Tunnel FET fabrication and model development.

Noise is an important parameter for analog/RF performance. From a microscopic point of view, carrier transport in electronic devices is a stochastic process. The stochastic nature of carrier movement gives rise to a time dependent fluctuation in the current. This phenomenon is described by noise models. Noise components include thermal noise associated with the channel, the source, and the drain. In our work we have investigated analog/RF behaviour of TFET for various device engineering such as LAD doping effect, gate-drain UL based design and dielectric effect for spacer and gate oxide. Since LAD/UL based TFET design induces parasitic resistance so it will effect device noise at RF frequency. Therefore, my future work is to investigate noise spectral density for aforementioned device engineering and also to develop compact models for low power analog/RF circuit design

Appendix A

Band-to-Band Tunneling Models

A.1 Nonlocal Band to Band Tunneling Model

All band to band tunneling was simulated in this thesis using the non-local BTB tunneling model available in Silvaco Atlas. This model require special fine mesh to be applied around the area where the tunneling occurs. In order to explain how the tunneling current is calculated, let us consider the energy band profile along each tunneling slice with reverse bias applied across the junction. The range of valence band electron energies for which tunneling is permitted is shown in the schematic of the energy band profile in Fig. A. The highest energy at which an electron can tunnel is E_{upper} and the lowest is E_{lower}. The tunneling can be thought of being either the transfer of electrons or the transfer of holes across the junction. The rates for electrons and holes are equal and opposite because the tunneling results in the generation or recombination of electron-hole pairs. For an electron that has an energy between E-ΔE/2 and E+ΔE/2 (Where ΔE is a small energy increment), the contribution to the BTBT current is

$$J(E)\Delta E = \frac{qkTm^*}{2\pi^2\hbar^3}T(E)\log\left(\frac{\left(1+\exp\left[\left(E_{Fr}-E\right)/KT\right]\right)\left(1+\exp\left[\left(E_{Fl}-E-E_{\max}\right)/KT\right]\right)}{\left(1+\exp\left[\left(E_{Fl}-E\right)/KT\right]\right)\left(1+\exp\left[\left(E_{Fr}-E-E_{\max}\right)/KT\right]\right)}\right)\Delta E \quad \text{A.1}$$

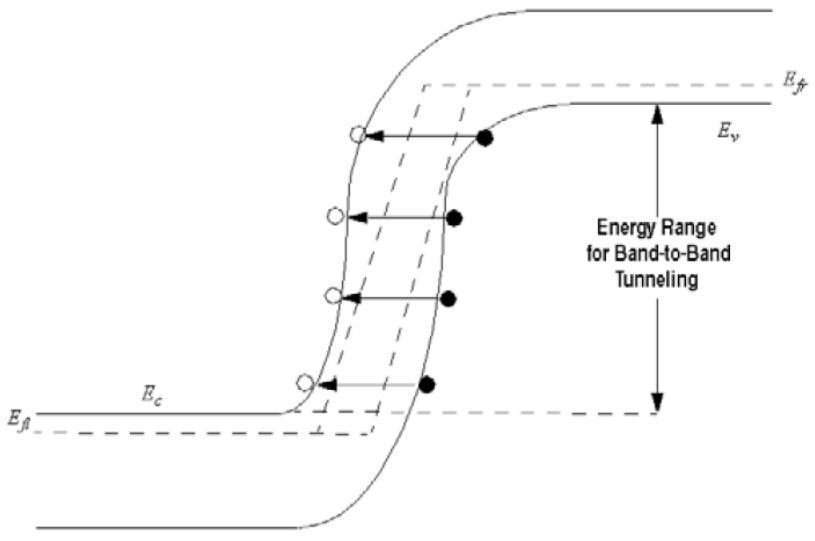

Figure A.1: Schematic of non-local band to band tunneling in reverse bias[46].

Here, T (E) is the tunneling probability, E_{fl} and E_{fr} are the Fermi levels as shown in fig. The tunneling probability T(E) is calculated with a two-band approximation for the evanescent wave vector, given by

$$k(x) = \frac{k_e k_h}{\sqrt{k_e^2 + k_h^2}} \qquad \text{A.2}$$

Where

$$k_e(x) = \frac{1}{i\hbar}\sqrt{2m_o m_e(x)(E - E_c(x))} \qquad \text{A.3}$$

and

$$k_h(x) = \frac{1}{i\hbar}\sqrt{2m_o m_h(x)(E - E_c(x))} \qquad \text{A.4}$$

This ensures that the energy dispersion relationship is electron-like near the conduction band and hole-like near the valence band, and approximately mixed in between. The tunneling probability, *T (E)*, is then calculated using the WKB approximation

$$T(E) = \exp\left(-2\int_{x_{start}}^{x_{end}} k(x)dx\right) \qquad \text{A.5}$$

This value is put into A.1 to give the tunneling current density at a given perpendicular energy, *E*, and the resulting current is injected into the simulation at x_{start} and x_{end}. This is repeated for all values of *E* between E_{lower} and E_{upper} and is done for every tunneling slice in the tunneling regions.

Effective electron and hole effective masses are adjusted to calibrate the nonlocal model when attempting to fit experimental data. The tunneling current is most sensitive to the effective masses used in Equations A.3 and A.4 because the tunneling probability depends exponentially on them.

A.2 Local Band to Band Tunneling

In local band-to-band tunneling models calculate a recombination generation rate at each point based solely on the field value local to that point. For this reason, we refer to them as local models. Local band to band tunneling models are not the best choice for simulations, since band-to band tunneling is fundamentally a non-local process which depends upon the tunneling battier width and the availability of energy states across the barrier. The general equation, used by the local models, is

$$G_{BBT} = DBB.A \times E^{BB.GAMMA} \times \exp\left(-\frac{BB.B}{E}\right) \qquad \text{A.6}$$

where *E* is the magnitude of the electric field, *D* is a statistical factor, and BB.A, BB.B, and BB.GAMMA are user-definable parameters. In Atlas, there are different sets of values that may be applied to the local model parameters.

The model parameters can be set to the standard model, BBT.STD, the parameter defaults for the standard model are as follows:

BB.A = 9.6615e18 cm^{-1} V^{-2} s^{-1} BB.B= 3.0e7 V/cm BB.GAMMA= 2.0

The model parameters may also be set to the Klaassen model by specifying BBT.KL on the MODELS statement. The parameter defaults for the Klaassen model are as follows:

BB.A = 4.00e14 $cm^{-1/2}$ V-$^{5/2}$ s^{-1} BB.B = 1.9e7 V/cm BB.GAMMA= 2.5

In application, use the standard model with direct band gap while using the Klaassen model with indirect band gap.

Another local tunneling model is based on the work of Kane. In this model, the tunneling generation rate is given by

$$G_{BBT} = \frac{DBBT.A\_KANE}{\sqrt{E_g}} F^{BBT.GAMMA} \exp\left(- BBT.B\_KANE \frac{E_g^{\frac{3}{2}}}{F} \right) \qquad \text{A.7}$$

This model automatically includes variation of band position that is why, the model differ from the standard model.

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