A Novel Micro-electronic Strain device Fabrication & 2D Materials Characterization

M.Tech Thesis

By

Sarthak Acharya
DAAD IIT Master Sandwich Scholar- 2016

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Sarthak Acharya

DISCIPLINE OF METALLURGY ENGINEERING AND MATERIAL SCIENCE

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **A Novel Micro-electronic Strain device fabrication & 2D Materials Characterization** in the partial fulfilment of the requirements for the award of the degree of **Master of Technology** and submitted in the **Discipline of Metallurgy Engineering and Material Science, Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from July 2015 to July 2017. Thesis submission under the supervision of **Dr. Parasharam M. Shirage**, Associate Professor, Discipline of Metallurgy Engineering and Material Science.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

Signature of the student with date
Mr. Sarthak Acharya

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Signature of the Supervisor
Date:
Dr. Parasharam M. Shirage

Signature of the Supervisor
Date:
Dr. Joachim Knoch

Sarthak Acharya has successfully given his M.Tech. Oral Examination held on **27 June 2017**.

Signature of Supervisor of M.Tech. Thesis
Date:

Convener, DPGC
Date:

Signature of PSPC Member 1
Date:

Signature of PSPC Member 2
Date:

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Sarthak Acharya

Dedicated

To

My Parents

&

My Guide

ABSTRACT

So far strain engineering has proved to be an efficient way to induce and tune the band gap in 2D materials. While mechanical strain device have already been demonstrated, they rely on bending a flexible substrate. However, bending the substrate induces also strain underneath the contacts leading to ambiguities in the interpretation the electrical behaviour of the 2D material and eventually to a complete failure of the contacts. A novel micro-electronic device has therefore been fabricated on thin (200 micron) Si Substrates with silicon dioxide on top of it using optical lithography and deep silicon reactive ion etching, which can create strain in the 2D material (flakes) mounted on it. The idea is to etch a deep trench into the substrate such that the remaining silicon becomes thin enough to act like a hinge. The benefit of this novel device is that there is a rigid substrate underneath the contacts so that strain is only applied in between the contacts. As a result, higher strain levels should be applicable since contact failure due to mechanical strain is avoided. Furthermore, the substrate can be used to get the 2D material within the contact are suppressing the impact of the metal-2D material interface on the measurements. The device was fabricated using microelectronic steps. During the initial phase of fabrication of the device faced few difficulties including the adhesion of thin Photo Resists (AZMIR 701), Silicon Oxide depth, Deep Reactive Etch etc. A new honey Photo-resist was used instead of the thin one and a standard recipe for the new resist was designed. All the ambiguities were overcome successfully and a final fabricated device was tested by giving external strain. The fabrication of the final strain devices provide a flexible strain variation of at least 10-12%. The device can be utilise further to induce strain in two-dimensional layered materials such as TMDCs, which may change the electrical, photonic, phononic and optical properties of those materials by altering the number of layers and changing the band gap.

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LIST OF ABBREVIATIONs

2D - Two Dimensional

3D - Three Dimensional

ALD - Atomic Layer Deposition

BOE - Buffer Oxide Etching

DC - Direct Current

DRIE - Deep Reactive Ion Etching

FETs - Field Effect Transistors

HAR - High Aspect Ratio

HDP - High Density Plasma

HMDS - Hexamethyl Disilazane

IPA - Isopropyl Alcohol

LED - Light Emitting Diode

MOSFET- Metal Oxide Semiconductor FET

PR - Photo Resist

RCA- Radio Corporation of America

RTP - Rapid Thermal Processing

SEM - Scanning Electron Microscopy

TFETs - Tunnelling FETs

Chapter 1

1. Introduction

1.1. Introduction

Strain is a description of dislocation, deformation (or) slip mechanism of the lattice arrangement in a body. Mostly it occupies our mind as a bulk-mechanical phenomenon, while strain physics in semiconductor is an old concept. The idea of introducing strain in Si/Ge has started since 1950s. Induced strain, results in enhancement of opto-electronic properties in different materials incorporated via lattice mismatch. In 2002, an induced strain was introduced into a planar Si MOSFET transistor by Intel which heralded a new age of feature scaling in transistors. Since then, Strain engineering is used as a trend to boost device calibre and performance.

In the early 1980s (Manasevit et al., 1982; R. People et al., 1984) Strained Si was introduced in MOSFETs that enhanced the mobility of electrons in n-type <100> $Si/Si_{1-x}Ge_x$ multilayer structure [1]. With rapidly changing technology, Strain has its tangible effects on band structures, carrier transport and lattice orders.

Thin layered materials are quite useful for their integration into a wide variety of technologies, especially in opto-electronic devices. For the optimisation of these possible technologies can be handled by gaining control over different properties of materials. By applying Strain, it is possible to alter the electronic structures of two-dimensional crystals, such as Graphene, Transition Metal Dichalcogenides (TMDC) etc. [2,3]. Alteration in electronic structures moulds the behaviour of the materials.

While straining phenomena is fundamental but the sources of strain is purely dependent on the technology, device and methods. For Instance, Strain can be introduced by intrinsic stress in deposited thin films, from Lattice mismatch of epitaxial growth films, by phonon induced lattice vibration (or) by external stress. Sometimes Force summing devices such as cantilever, transducers are also good means of straining. Therefore, it is purely dependent on the kind of geometrical scaling we require for our application.

Molybdenum Disulphide, a layered two-dimensional material, has been observed to show a change in behaviour in the material by straining it to ~3% [6]. Decrease in the photoluminescence intensity of MoS_2, is the indication of direct to indirect band gap

transition at an applied strain of 1-3%. Therefore, it can also be inferred that transitions such as direct to indirect and Metal to Semiconductor can also happen by straining layer structured materials.

2-Dimensional materials such as Graphene, has exceptional carrier mobility, high mechanical strength & elasticity, optical transparency. However, despite of such outstanding properties, it lacks band gap [2]. Not only graphene but there are certain 2D materials, which either lacking band gap (or) possesses poor lower band gap. This property can be tuneable by giving strain to these materials. So far, it has been observed that strain values over 10% are sufficient to open a significant band gap in these materials. But the concerning area related to straining mechanism is the poor Strain transfer between the 2D materials & the supporting substrate.

In this Thesis, we have introduced a novel methodology to create stain in Micro/nano (2D materials) Flakes. A novel micro- electronic device has been fabricated on thin (200-500 micron) Si substrates with SiO_2 on top of it using optical lithography and deep Si reactive ion etching. Further, the device has been tested by straining up to breakage and an optimal strain variation of 10-12% was obtained. In Chapter 2, theories related to strain & motivation towards the fabrication of this device were discussed. In Chapter 3, 4 & 5 the process flow, fabrication steps, fabrication difficulties & its solution, final device fabrication steps were discussed. Various tools & techniques used during the thesis work are mentioned briefly. In Chapter 6, summary of the fabrication work is mentioned and the future scope of this work has been discussed. The important steps involved in the fabrication are sequenced in order. The extended work possible by using this device is outlined in the last section of the chapter.

Chapter 2

2. Theory

2.1. Strain Engineering

Strain can be defined as "Extension/ Compression per unit length". It has no unit as it is a ratio of lengths. If the strain caused by tensile force it is named as Tensile Strain, If by Compressive force, then Compressive Strain.

$$Strain(\in) = \frac{e}{l} \ ;$$

Where e = Extension;

l = Original Length;

In general, Strain is a tensor quantity, can be decomposed into normal and shear components. The amount of deformation along the material line element is defined as "Normal Strain". The amount of deformation associated with the sliding of plane layers over each other is defined as "Shear Strain".

Normal strain can again be classified as Tensile Strain, if there is an increase in length due to strain & as Compressive strain, if there is a reduction in length due to strain.

Engineering Strain:

It can be expressed as "the ratio of total deformation to the initial dimension of the material body in which forces are being applied".

$$\propto = \frac{\Delta l}{l} \ ;$$

Where $\propto$ = engineering Strain;

Δl = Change in length;

l = Original length;

It is also known as "Cauchy Strain".

According to literature, engineering strain are subjected to very small deformations [1]. Strain, on a greater scale can be categorised as Stretch, Logarithmic strain, Green strain, Almansi strain etc.

Strain can be analysed on Macro-scale as well in Micro/ Nano level. On Macro-scale strain is associated with stress and can be explained by Hooke's Law.

$$\sigma = E.\epsilon \ ;$$

Where E = elasticity of modulus

$$\sigma = Stress\ applied$$

$$\epsilon = Strain$$

On Micro/Nano scale, it can be explained by Williamson-Hall equation which is subjected to Lattice Strain, which can be analysed and calculated from X-ray Diffraction data.

The mathematical equation can be given as

$$\epsilon = \frac{\beta}{4.tan\theta} \ ;$$

Where β = FWHM (from XRD peak)

θ = Angle in the XRD data

2.2. Strain in Micro-electronics Devices

In this Modern era, integrated circuits were invented and evolved exponentially in density and performance. Along the path portended by Moore's law through improvements in lithography and micro-electronics fabrication technologies until various obstacles began to loom.

Finally, continual geometric scaling of MOSFET channel length, gate–dielectric thickness and junction depth led to various short channel effects. Performance improvement by simple geometrical scaling became more problematic and costly. The reason for the end of simple scaling for a solid-state device technology are Power density limits, base widths and voltage. In order to meet growing needs of global market for a continuation of Moore's law, Feature enhancement is recognized instead of simple geometric scaling [1].

For the micro-electronics industry, key features include induced-Strain, metal gate, non-planar geometrics, heterogeneous integration etc. The first key feature to enhance 90, 65 & 45nm technology needs uniaxial induced stress [1]. The development of first

commercial strain feature-enhanced Si technology is reviewed in 2006 [1]. In the 90s, two process induced Strain sources were investigated, high stress capping layers deposited on MOSFETs and embedded Si-Ge source.

2.3. Two-Dimensional Materials

Two dimensional materials are substances with a thickness of few nanometres (or) less, in which movement of electrons are free in 2-dimensional plane. These materials consisting of a single layer of atoms, hence sometimes known as single layered material [7]. The first 2D material discovered was Graphene, which exhibits excellent electrical and optical properties. Graphene is another 2D carbon allotrope with similar structure as graphene. Some of the 2D materials exhibits multiple layered structure, generally known as Van der Waals heterostructure. New family of 2D materials are Transition Metal Dichalcogenides (TMDCs) [3,4]. Which exhibits layered structure and the mono-layered TMDCs are atomically thin semiconductors. Some of the well-known TMDC materials are MoS_2, $MoSe_2$, $MoTe_2$, WS_2, and WSe_2. These materials combined with other 2D materials like Graphene, Boron Nitride etc. forms heterostructure. Such structures are used in Solar cells application, LEDs, photo detectors, fuel cells and sensing devices. TMDC materials possess indirect band-gap while its monolayers exhibit direct band-gap. The electrical. Photonic and optical properties of these materials depend on the number of layers present, size of Dichalcogenides, band gap etc. [5]. The other major applications of these 2D materials are in photovoltaic, in energy storage devices etc. [8]. Currently, it is one of the focused area for researchers with a lot of future scopes.

2.4. Motivation towards the work

Straining mechanism in nano-materials are one of the interesting topic for the researchers. There are many mechanical sources of inducing strain but the drawback of these sources is it cause damages to the surface of the materials which may induce defects in the material [3]. There are other methods to induce strain such as nano-patterning, chemical treatment etc. but again they will cause the surface damage. Therefore, there should be a device which can induce strain in nano-materials without causing surface distortion. Few of the motivations towards this work are stated below

Motivation 1:

Graphene, a well-known 2D material has zero band gap [2]. But a strain of 20-30% opens the band gap in graphene. Similarly, TMDC materials which are layered materials and already possess band gap can also be tuned inducing strain [3,4]. As they already have the band gap, the amount of strain, require to alter the properties will be lesser than in graphene. A strain percentage more ~3% can make differences. If the multi-layered structure can be tuned to monolayer, there can be two major transitions. First indirect to direct band gap transitions and second will be semiconductor to metal transition. Hence, this ideology motivated me to think about such a device that can induce strain in TMDC nano-materials.

Motivation 2:

For future nano-electronics circuits, the primary requirement is low power dissipation. Probably the reason TFETs are preferred over conventional FETs. In case of Conventional FETs, the charge carriers are thermally injected into the channel, where as in TFETs it is done by quantum mechanical band to band tunnelling. For TFETs fabrication, monolayers are preferred due to its direct band gap property [4]. Therefore, if straining can reduce the number of layers then it could be feasible to fabricate low power electronic device.

Motivation 3:

In a Transistor, whether it is FET (or) TFET, the most important parameter is Current, which decides the fate of the device. In case of TFETs, the tunnelling current is dependent on few parameters, given by WKB approximation below.

$$I_{on} \propto \exp\left(-\frac{4\sqrt{2m_t^*}E_G^{3/2}}{3q\hbar E}\right)$$

Where m^*_t = tunnelling effective mass;

E_G = Band Gap;

E = electric field at source- channel junction;

I_{on} = Tunnelling Current;

If we analyse the above equation properly, then we can see that the tunnelling current is purely dependent on two parameters, they are 'm^*_t' & 'E_G' [4]. Lower the value of these two parameters, higher will be the current. But if we take the radicals into consideration the former parameter has 0.5, and the later has 1.5. Hence, it will be better if the later will be focused. Lower band gap can change the tunnelling current effectively. Lowering the band gap will also results in Small sub-threshold swing (SS) and in high I_{on}/ I_{off} ratio.

Work done so far:

This can also be considered as one of the motivation towards fabrication of this device. The first trail to induce strain in flakes is experimented by taking a plastic substrate with a dielectric material on top of it. MoS_2 flake was mounted on top of it by using metallic contacts. The setup is shown in figure 1(a). The difficulty with the setup was, when it was given a strain, the metallic contacts ripped off. Due to the ripping off of the contacts the flake didn't find a fixed position. The strained set up is also shown in figure 1(b). Other ambiguities with the setup was the plastic substrate, which unable to produce a greater strain. Hence, there should be a device with flexible substrate that can cause strain.

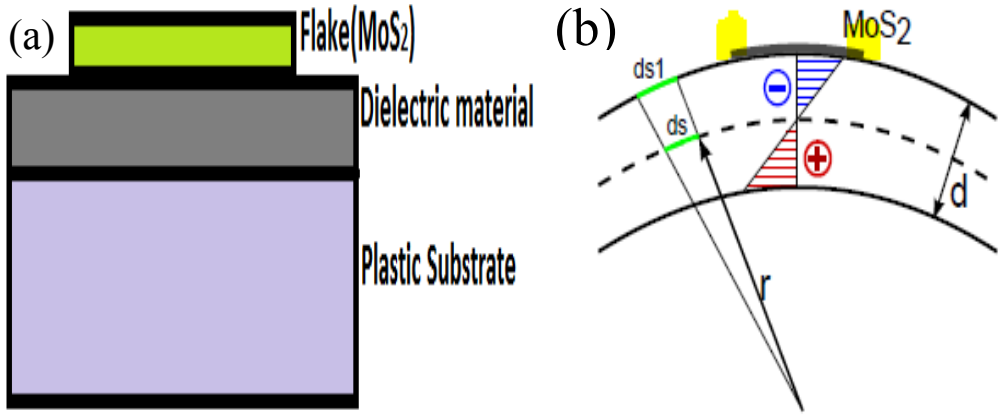


Figure 1. (a) A strain setup using plastic substrate. (b) Strained substrate.

These are few theoretical aspects that motivated me to think about a device fabrication that can be a source of straining 2D flakes. Fabrication of such device requires various tool knowledge and hand on experience on the tools. Hence, the first step is to make a process flow. According to the process demand, the requirement of the tools will be decided. In chapter 3, the lists of the tools, their working principle and their

specification are discussed. During the course of my thesis work, I have given training on those tools which helped me to carry out the fabrication work easily.

CHAPTER – 3

3. Tool Methodology & Process Development

3.1. Overview

In the following sections, the different methods employed in this work are outlined and explained. Subsequently, it is presented how they were applied in the development of the fabrication process. Challenges and solutions are discussed and the optimised processes are presented. In this Chapter, we will discuss all the tools and their working principle that are used during the dissertation work. These tools were used for the fabrication of the final device. The instruments that are used are Wet benches, fume hood, HMDS substrate dryer, Spin Coater, Optical Lithography tool (MA6/MA4), Optical 3D Laser microscopy, Reactive ion etching tool (RIE-51), Raman Spectroscopy, Rapid Thermal Process tool, Scanning electron microscopy, Current-voltage measurement set up etc.

3.2. Wet Benches & Wet Chemistry

Generally Wet benches are placed in a clean room to carry out pure and contamination-free fabrication. Working on wet benches needs special training. Typically, a wet bench is a fully automated tool which is used for Standard RCA cleaning and etching operations in semiconductor fabrication. They are used for acids, bases, and solvent processing. Benches includes several modules or baths, which contains cleaning, etching solution, development solvents and deionized (DI) water. Nitrogen gun is fixed to each section to make the sample dry and particle free.

In the Clean room and at the benches each sample are processed with different contamination level and comply with the colour code of tool sets such as tweezers, beakers, carrier wafers, substrate holders etc. in order to minimize cross-contamination. Generally, samples like 6 inches & 4 inches Si wafers, diced Si pieces are processed. There are Three Contamination categories classified namely A, B, C. Category-A is the cleanest one tagged with White labels includes Si, SiO_2, SiN, Al_2O_3, Photoresist,

PMMA. Category-B tagged with Green labels is the same as Al, Ti, Ni, Co, W. Category-C is the least clean category tagged with Red labels and includes metals such as Au, Ag, Cu, Fe, Na, K and III-V semiconductors. Few applications of Wet benches include Cleaning & Surface Preparation, Etching, Stripping, Texturing, Plating etc.

Wet Chemistry

Wet chemistry is the form of analytical chemistry that is used for element analysis using laboratory beakers and flasks to manipulate a sample. It can also be name as Wet Chemical Analysis that generally refers to chemistry performed on samples in the liquid phase. H_2O_2, H_2SO_4, HF, BOE, HCl, NH_3.

3.3. Optical Lithography

.

Lithography is combination of several processes. Starting from the photo-resist coating, followed by masking and then resist development. In this work, the Si substrate after HMDS substrate drying, is a given a resist coating by a spin coater. The lithography can be done by MA6 tool (or) MA4 tool. But in this work, we have used MA6 tool.

MA6 tool has certain sequence of steps to be followed. The first step is to change the mask and an appropriate chuck. There can be two choices in mask and chuck: 4 inch and 6 inch. Vacuum as well as a mechanical support is used to fix the mask. The next is to load a sample and alignment of the sample. The sample automatically be fixed by vacuum. The sample can be aligned by using top, bottom, left and right navigations and monitored as well. After the sample alignment, proper parameters must be set according to the recipe of the process. The parameters such as exposure time, type of contacts, channel wavelength etc. can be manipulate using the option “set parameters”. After setting all the parameters, final work is to do “Exposure”. After the process done, sample and the mask must be unloaded. The Nitrogen and vacuum flow must not off soon after the process, it must be off after 20 minutes. This will cool down the lamp properly and will protect the tool from damage. After this, the sample will be developed using developer solution for an adequate amount of time. The developer solution used in this work is AZ-726 MIF.

3.4. Rapid Thermal Processing

Rapid Thermal Processing (RTP) is a collective term for various high temperature processes in semiconductor manufacturing technology. The mechanism of the process is "wafers (or) samples are heated to a high temperature (up to 1000◦C and more) within a very short duration of time (usually on the order of a few seconds). The semiconductor industry uses RTP methods for dopant activation, annealing, oxidation, nitration, hydrogenation etc. For this work, an AnnealSys AS-One 150 Rapid Thermal Processor (AS-One 150) is employed to grow ultrathin silicon dioxide layers. The AS-One 150 features a high vacuum chamber which is equipped with 18 halogen lamps (with a combined power of 34kW) [9]. This allows for process temperatures of up to 1200℃. Two pyrometers are used in the chamber to control the inside heat and surrounded by barium fluoride windows. To provide a pure ambient atmosphere, the chamber used to evacuate up to a pressure of 8×10^{-6} mbar [10]. This is very crucial for silicon nitride, since the Oxygen traces left inside the chamber may form an oxy nitride and hamper the film's properties. Pyrometers gives accurate measurement only above 300^{0}C, hence a constant power is applied till the PID allows proper control. After reaching to the desired temperature, various atmospheric gas mixtures, with pressures up to 1bar flows into the chamber, gases such as argon, hydrogen, oxygen or ammonium. A mixture of oxygen and hydrogen is not possible, because the resulting water could damage the machine and react with the barium fluoride, forming hydrofluoric acid. A basic schematic of RTP chamber is shown in figure 2.

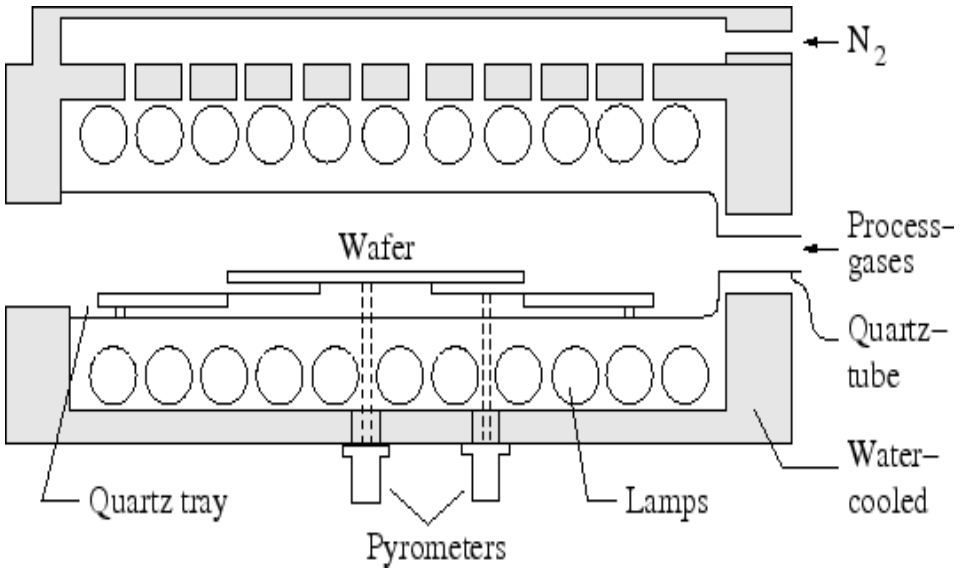


Figure 2.A schematic set-up of a Rapid Thermal Processing reactor

Features & Caution

1. While placing the carrier wafer inside the chamber, make sure that the wafer must not touch the 3 quartz bars. Reason being as the bars are conducting in nature, there will be heat/ temperature loss. Because of which inside temperature may not reach the required process temperature.
2. There are two pyrometers inside the chamber. While placing the sample leave central pyrometer uncovered. The samples must be placed in the side areas. Reason being the temperature at the centre and in the side areas are different. If the both the sample and wafer will be placed in the centre, then a double layer will reduce the temperature sensing. To compensate the effect, system will try to increase heat up the system, which may result in damaging of the tool.

Process Parameters

Oxidation step

T = 1100 ℃

T- Ramp = 40 ℃*/sec*

$P = 1 X 10^{3} mbar$

O_2 *Flow = 2000 sccm*

Time = 60 sec.

3.5. Etching

Etching is the process of removing materials from the selected areas of a surface of the wafer. In semiconductor manufacturing, mostly two types of etching are used. “Dry” (plasma) etching is used for circuit-defining steps, while “wet” etching (using chemical baths) is used mainly to clean wafers. During any fabrication, before etching step begins, a wafer is coated with PR (or) a hard mask and exposed to a circuit pattern during lithography. Etching removes material only from the pattern. This sequence of patterning and etching is repeated multiple times during the chip making process.

Etch processes can further be classified, on the basis of the types of films that are removed from the wafers, into conductor etch, dielectric etch, polysilicon etch. Dielectric etch is involved when an oxide layer is etched. Dielectric etch is also employed to etch via holes and trenches for metal conductive paths. Polysilicon etch is used to create the gate in a transistor. And metal etch removes aluminium, tungsten, or copper layers to reveal the pattern of circuitry at progressively higher levels of the device structure.

Plasma etching is performed by applying electromagnetic energy to a gas containing a chemically reactive element, such as fluorine or chlorine [11]. The plasma releases positively charged ions that bombard the wafer to remove materials and chemically reactive free radicals that react with the etched material to form volatile or non-volatile by-products.

In this work, two type of etching is used. First one Deep reactive ion etching using COBRA tool. Second one is BOE using buffer solution.

3.5.1. Deep Reactive Ion Etching

The tool for patterning silicon (Si) which is used to fabricate the final device is inductively coupled plasma (ICP) deep reactive-ion etching (DRIE), a special type of reactive-ion etching (RIE). RIE is considered to be one of the most basic dry etching methods and is also well established in the semiconductor industry. One of the major reason of choosing dry etching over wet etching is the fact that it offers the possibility to produce anisotropic structures such as trenches or holes.

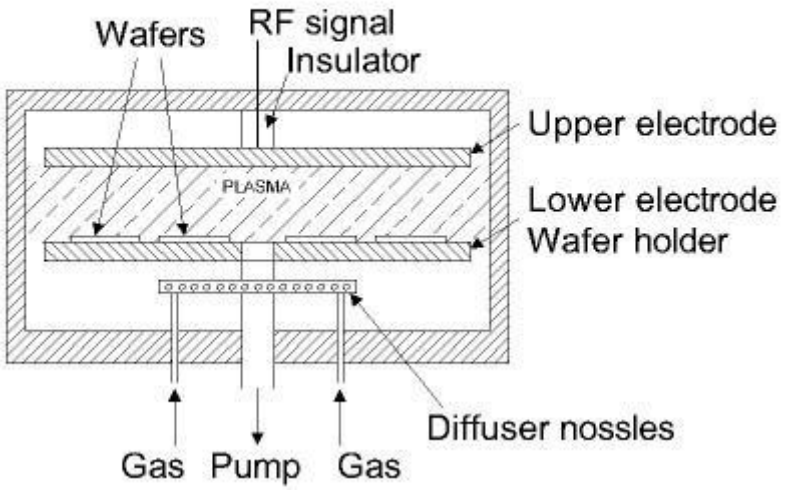


Figure 3. A basic RIE setup.

The general setup of a reactive-ion etching chamber is shown in Fig. 3. Process gases can flow into the chamber through an inlet and a plasma gets ignited with the help of electromagnetic fields. Movement of the electron in the chamber fasten due to the presence of an alternating voltage. The electrons hit the upper electrode (or) the chamber walls and accumulates on the isolated lower electrode upon contact. Thus, an average DC voltage builds up [11]. As a consequence, the ions from the plasma are directed onto the wafer where they react with the substrate and remove material. The reaction is always partly chemical which introduces an isotropic etching component but there are also ions which simply sputter material by transferring kinetic energy. Since most ions reach the substrate in a vertical path, RIE is able to generate anisotropic etching patterns.

In 1994, Robert Bosch has developed the phenomena of Deep RIE in order to generate very high aspect ratio structure. DRIE processes broadly classified into HAR-Bosch etching and cryogenic etching. In this work, HAR-Bosch process is preferred over the cryogenic etching. The reason for preferring the former over the latter is explained in chapter 4.

3.5.2. BOSCH Etching Process

The Bosch process uses a fluorine based plasma chemistry to etch the silicon. The sidewall passivation and selectivity to masking is taken care by the fluorocarbon plasma. It relies on the source gases being broken down in a high-density plasma region before reaching the wafer, which has a small but controlled voltage drop from the plasma. This technique cannot be performed in reactive ion etch systems (RIE), as these have the wrong balance of ions to free radical species. This balance can be achieved in high-density plasma systems (HDP). The most widely used form of HDP uses inductive coupling to generate the high-density plasma region so is known as 'inductively coupled plasma' (ICP). Sulphur hexafluoride (SF_6) is the source gas used to provide the fluorine for silicon etching. This molecule will readily break up in high-density plasma to release free radical fluorine. The sidewall passivation and mask protection is provided by Octofluorocyclobutane (c-C_4F_8), a cyclic fluorocarbon that breaks open to produce CF_2 and longer chain radicals in the high-density plasma. These readily deposit as fluorocarbon polymer on the samples being etched. The advantage of the process is, it is relatively insensitive to the exact nature of the photoresist [12]. In fact, it is best to avoid high temperature bakes of resist, as this causes variation in the resist profile. An etching profile is shown in figure 4. Which was achieved during the fabrication process. All the process parameters used are mentioned in chapter 4.

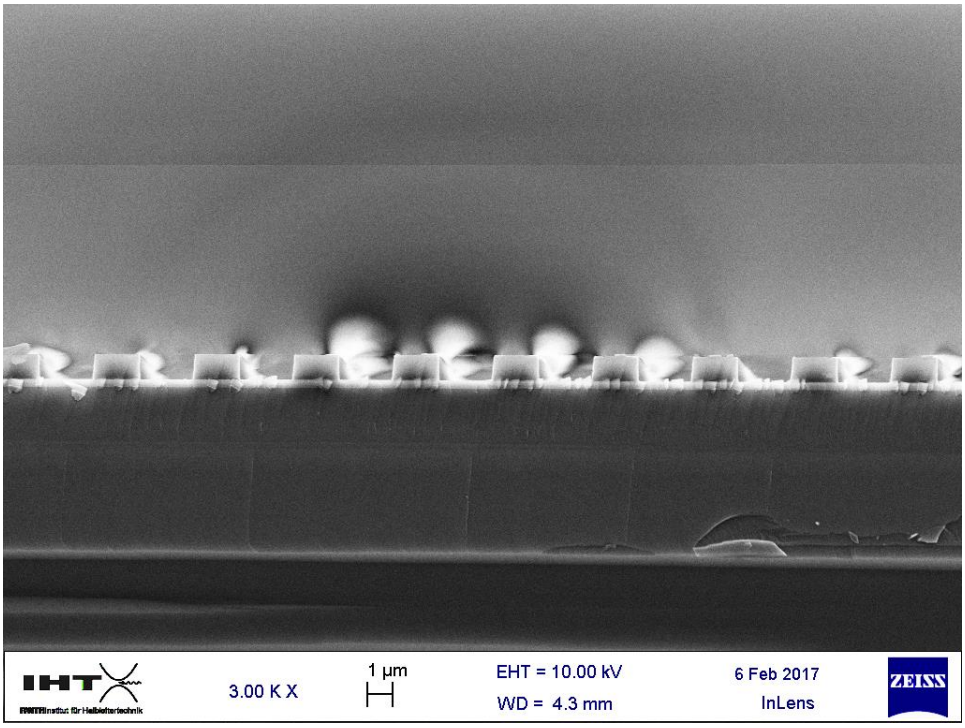


Figure 4. SEM Image of etching profile using Bosch process

3.5.3. Buffered Oxide Etching (BOE)

BOE is also known as buffered HF, which is a wet etchant used for micro fabrication. It is used to etch thin films of oxide (or) polysilicate glass. It is a buffered mixture of HF that slow downs the attack of HF on oxide layers. In this work, it is used to etch Silicon dioxide layer. BOE can be prepared by mixing Ammonium fluoride (NH_4F), Hydrofluoric acid (HF), DI water. But the one used in this work was already a prepared solution. The action BOE is shown in the figure 5.

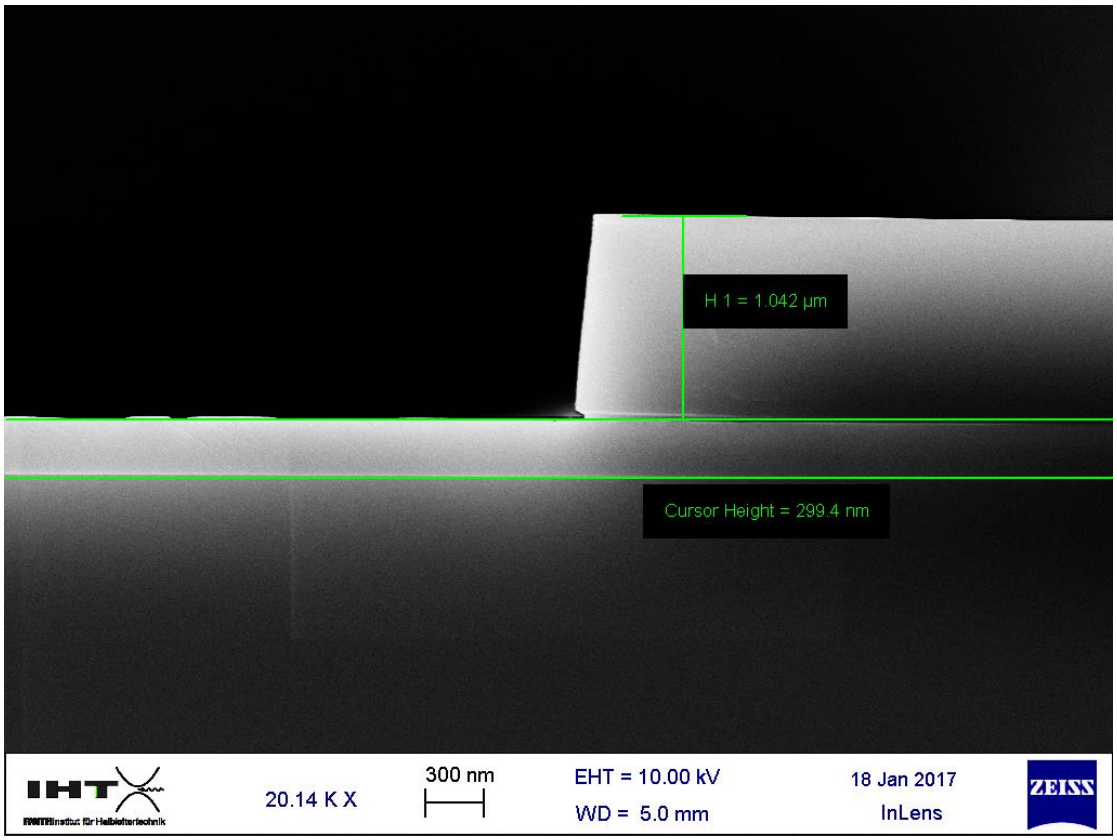


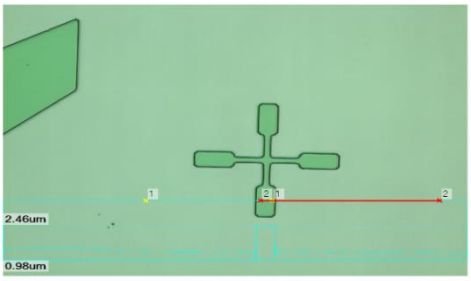
Figure 5. Etch profile of Alumina layer after Buffered Oxide Etching.

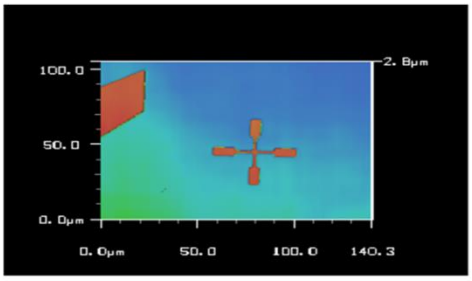
3.6. Optical 3D Laser Microscopy

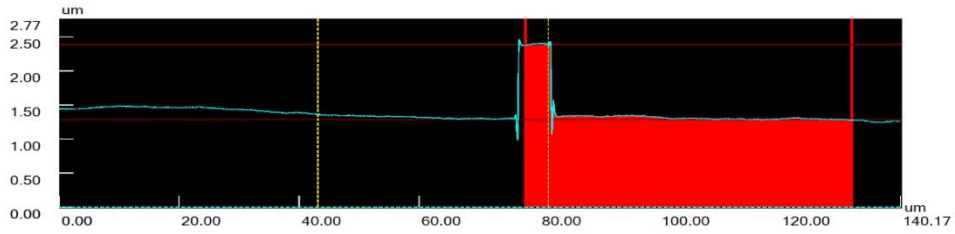
In this form of optical microscopy, the focused beam of a laser is scanned over the sample and the reflected intensity is displayed as a function of position to create a digital reflected light image of the sample. Scanning a focused laser beam allows the acquisition of digital images with very high resolution since the resolution is

determined by the position of the beam rather than the pixel size of the detector. These measurements include topography mapping, extended depth of focus, and 3D visualization (red/blue).

In this work, the software used to visualise the images is VK Viewer. It has four magnification lenses with resolution 10X, 20X, 50X, 100X. The facilities that can be avail from this tool are: HDR capture, Measurements of etching profile, 3D display of the structure etc. In figure 6, an etched marker structure and its etching profile is shown. This tool is quite helpful in viewing 3D structure and structure analysis.







Profile1	Horz. dist.	Hght. diff.	Hght. ave.	Angle	C.S. length	C.S. area	R	Comment
All	140.17um	0.18um	1.39um	0.08°	143.46um	195.41um2		
Seg.1	38.32um	1.04um	1.45um	1.55°	39.89um	55.77um2		
Seg.2	54.25um	1.09um	1.40um	1.16°	55.92um	76.23um2		
Seg.3								
Seg.4								
Seg.5								
Seg.6								
Seg.7								
Seg.8								
Seg.9								
Seg.10								
Total	92.56um	2.13um	2.85um	2.71°	95.81um	132.00um2		
Max.	54.25um	1.09um	1.45um	1.55°	55.92um	76.23um2		
Min.	38.32um	1.04um	1.40um	1.16°	39.89um	55.77um2		
Ave.	46.28um	1.07um	1.43um	1.35°	47.91um	66.00um2		
Std. DV	7.97um	0.03um	0.03um	0.20°	8.01um	10.23um2		
3sigma	23.90um	0.09um	0.08um	0.59°	24.04um	30.70um2		

Profile1
Line type : Horz.
Ave: None
Correction : Smooth intensity None, DCL/BCL None, Smooth height None, Correct tilt None
Ref. value1 : 2.77um
Ref. value2 : 0.00um
Step : 2.77um

Figure 6. Etching Profile Measurement using Optical Laser Microscopy

3.7. Scanning Electron Microscopy

A **scanning electron microscope** (**SEM**) is a type of electron microscope that produces images of a sample by scanning the surface with a focused beam of electrons. The electron cloud interact with atoms in the sample and produces various signals that contain information about the sample's surface topography and composition. This is the most used tool in this work. After each fabrication step, the results were observed and analysed by SEM.

The software used in this work is "Smart SEM". There are two options available to scan a sample: Cross-sectional Scan and Top view scan. The chamber always stays in vacuum in order to avoid any outer disturbances and contaminations. To load a sample, the chamber needs to be vented first. It has two modes of view: In Lens and BSE. In Lens is used in total fabrication process. To scan a sample EHT must put on. After proper focus on different magnifications, an image can be captured. To save an image, we must FREEZE the image and then choose the directory to give desired location. If no directory is chosen, by default it will store in the previous directory used. After taking an image, different measurements are also possible using Smart SEM software.

CHAPTER- 4

4. DEVICE FABRICATION

In this chapter we will get insight to the fabrication steps of the device. With the knowledge of the above tools, mentioned in chapter 3, a Process flow for the Fabrication is prepared. Later on, various fabrication difficulties and overcome to those ambiguities are discussed.

4.1. Design of Mask

The first and foremost requirement in the fabrication step is a Mask. The complete device structure depends on mask designing. The mask for this device is designed using AutoCAD software. There are four different sections of the Mask, designed as three column of small marker structure on either of a trench line. If we take the macro view the middle portion will look like a line but in actual it is a vertical rectangle. All the four sections having same number of marker structure with different dimensional width of 1/2/3/5 micron (10^{-6} m) and with a fixed length of 12362 micron. The purpose behind the variation of length is to get different openings of the final strain device so that variation in the strain can be observed. The Mask shown in figure 7.the hard copy of the mask and the one shown in figure 8 is the software layout. In figure 7, the four sections used in the fabrication are not clearly visible due to the transparency of that region. The Mask is shown in the figure 8. Part (a) shows the complete mask, in which only four sections with red marker structure and trench line were used in the device fabrication. Part (b) shows a large view of one of the four section of the Mask used. Part (c) shows a large view of the marker structure. Part (d) shows a clear and macro view of the trench line which in actual is a vertical rectangle with a width of 5 micron. Similarly there are three other sections with different width of the rectangular trench.

Figure 7.The Hard copy of the Mask showing four transparent region used for the device fabrication.

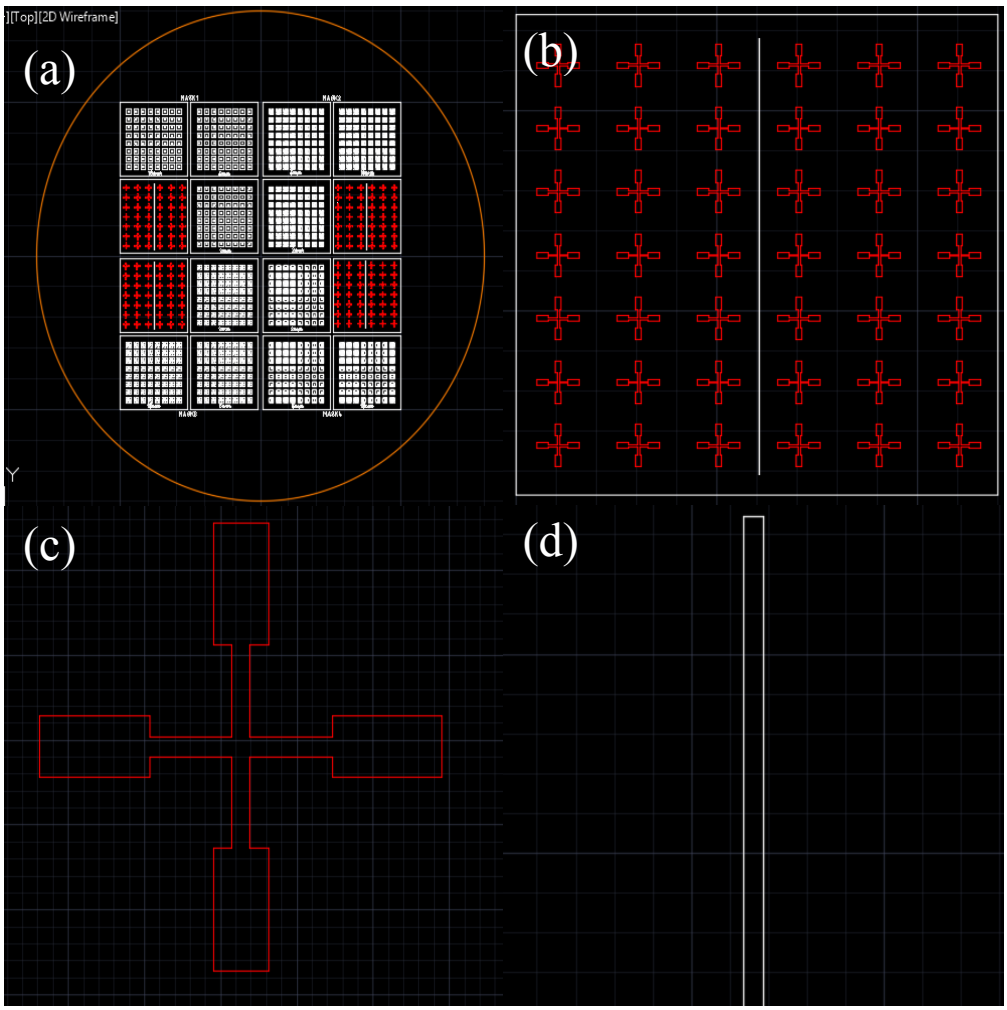
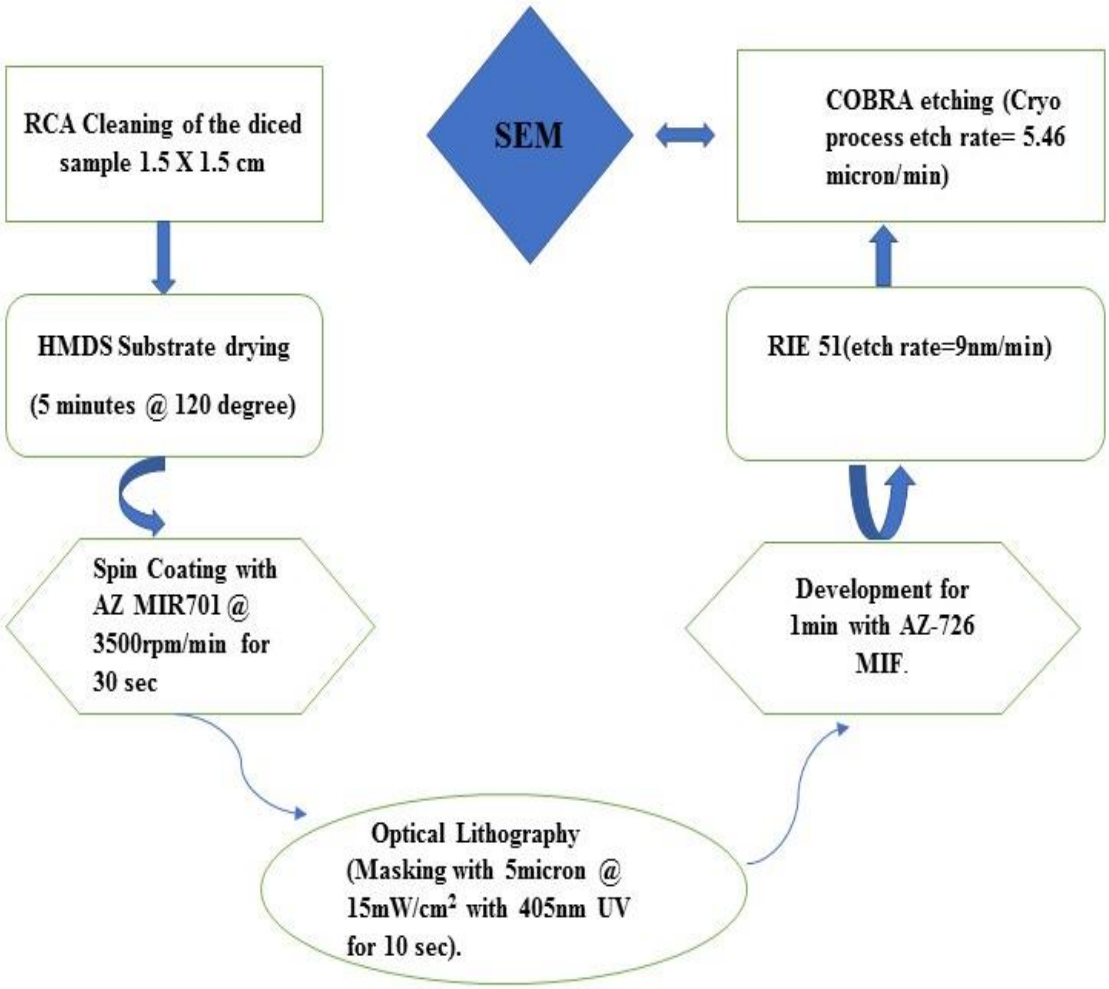


Figure 8. . a) Overall Mask view. b) Trench line in the middle with Marker structure on either side. c) A Marker structure in a large view. d) Trench line in large view

4.2. Sample preparation

The device will be fabricate, using the Silicon substrate <100>. This work used two kind of wafers, a thin one of thickness 275 micron and a thick one of thickness 575 micron. The four inch Wafer used for the device fabrication is oxidised using RTP on the both side. The thickness of the oxide layer is 275nm. The wafer then given a resist layer on top and diced into small pieces of dimension 1.5 X 1.5 cm. These small pieces will be cleaned using Acetone at 130 degree followed by IPA at 130 degree for 10 minutes each. This will remove the resist layer from the small pieces of substrate. The cleaned substrate, then will follow the steps of the process flow in order to fabricate the device.

4.2.1. Initial Process Flow



RCA Cleaning

Radio Corporation of America (RCA) has developed a set of standard steps for wafers, which need to be performed before any semiconductor fabrication process. It removes the organic contaminants, thin oxide layers, ionic contaminants etc. It has a standard recipe of few steps. Treatment of acids, solvents and bases make the surface of the wafer free from dirt, which is quite necessary for device fabrication. Hence, the diced samples were treated with full RCA clean before getting into fabrication steps.

HMDS Substrate Drying

The diced sample of dimension 1.5 X 1.5 cm were treated with RCA cleaning. The standard recipe of the RCA cleaning was followed (see Appendix I). Now the samples are free from oxide layers, coarse organic contaminations and dirt on the surface. Hexamethyl disilizane (HMDS) /$C_6H_{19}NSi_2$ used as an adhesion promoter for the photoresist used for microlithography. Use of this is preferred because of several reasons such as 1) It reduces the chemical consumption and water contamination on substrate surface. 2) Increases adhesion Longevity even in high relative humidity atmosphere. Here, HMDS applied in gas form called Vapor Prime. It promotes a good adhesion of resist layer to the wafer surface by making the surface hydrophobic. The samples were treated at 120 degree for 5 minutes.

Spin Coat

After HMDS substrate drying, the samples were processed with spin coating. Spin Coating process involves depositing a small puddle of fluid resin (photo resist) onto the centre of the substrate and then spinning it at high speed. The substrate is fixed by vacuum and centripetal acceleration spreads the fluid in a uniform order on the substrate. The photo resist used for this work is AZMIR 701, which is a thin positive resist. The process parameters used are spin speed at 3500 rpm, time is 30 seconds. After spin coating a post bake is required for 60 seconds at 90 degree hot plate. A general spin coat method and the uniform deposition of the PR on the substrate is shown in figure 9.

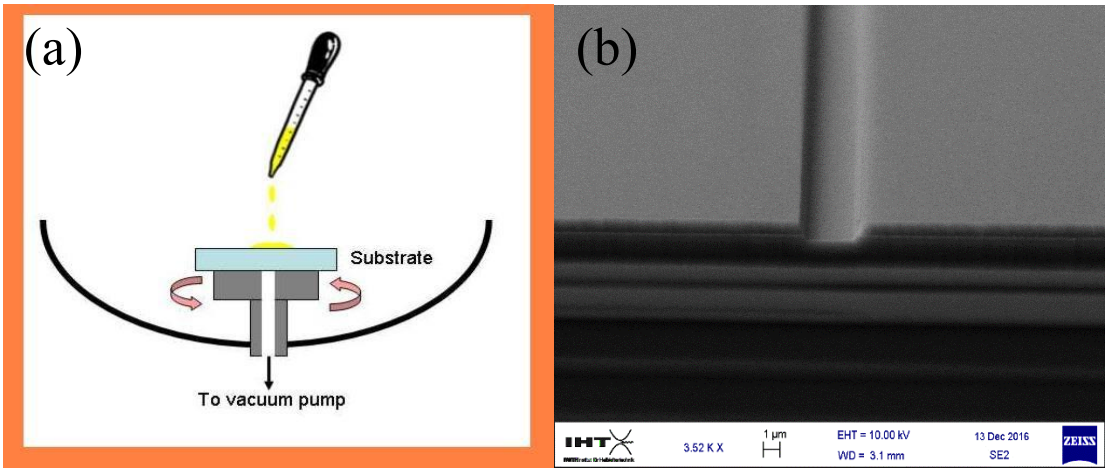


Figure 9. (a)Spin coating mechanism. (b) SEM image of uniform PR layer on Si Substrate

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Optical Lithography

After the post bake of the resist layer, the samples were treated with Optical lithography. MA6 tool is used for the process. The Mask shown in figure 2 is fitted on the tool for the exposure. The samples were exposed to Constant Intensity (CI) channel 2 with a wavelength of 405 nm. The exposure time was 10 seconds and the power used is 15 mW/cm^2. After the exposure, the samples were kept in AZ-726 MIF for 60 seconds for the development of PR layers. The samples were then kept under DI water for 5-10 minutes to pacify the action of development solvent. To investigate the surface of the samples, SEM images were taken which is shown in figure 10. The line with marker structure on both the side is clearly visible.

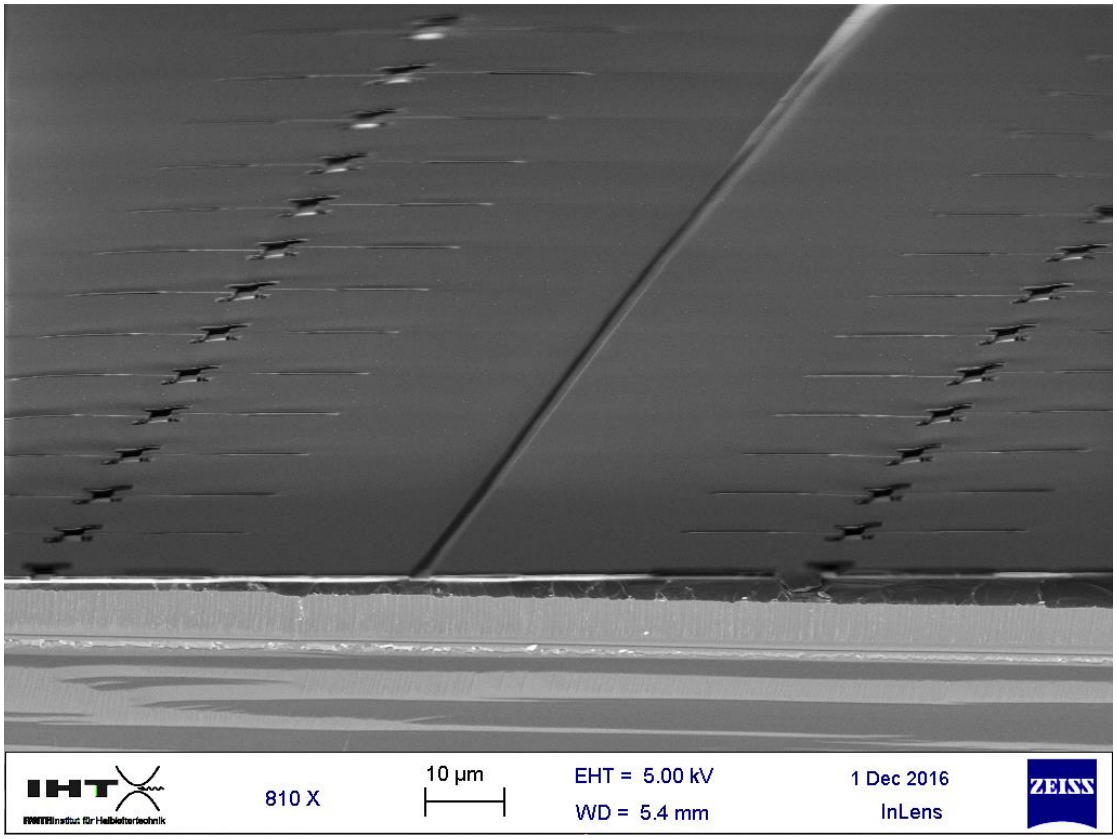

Figure 10. SEM image of the sample after optical lithography and development

Reactive Ion Etching (RIE)

After the patterning of the PR layer in the previous step, the next step is to remove the Oxide layer (SiO_2) [13]. RIE-51 tool is used to remove the SiO_2, which is about 275 nm in thickness. The etch rate of tool, determined by dummy samples is about 9 nm/min. Hence, the samples were processed for 32 minutes in order to etch through the oxide layer completely. The samples were observed under SEM after the process, which showed the target was almost achieved. The images are shown in figure 11, where the thickness of PR, an interface of PR and SiO_2 and the Oxide layer is shown.

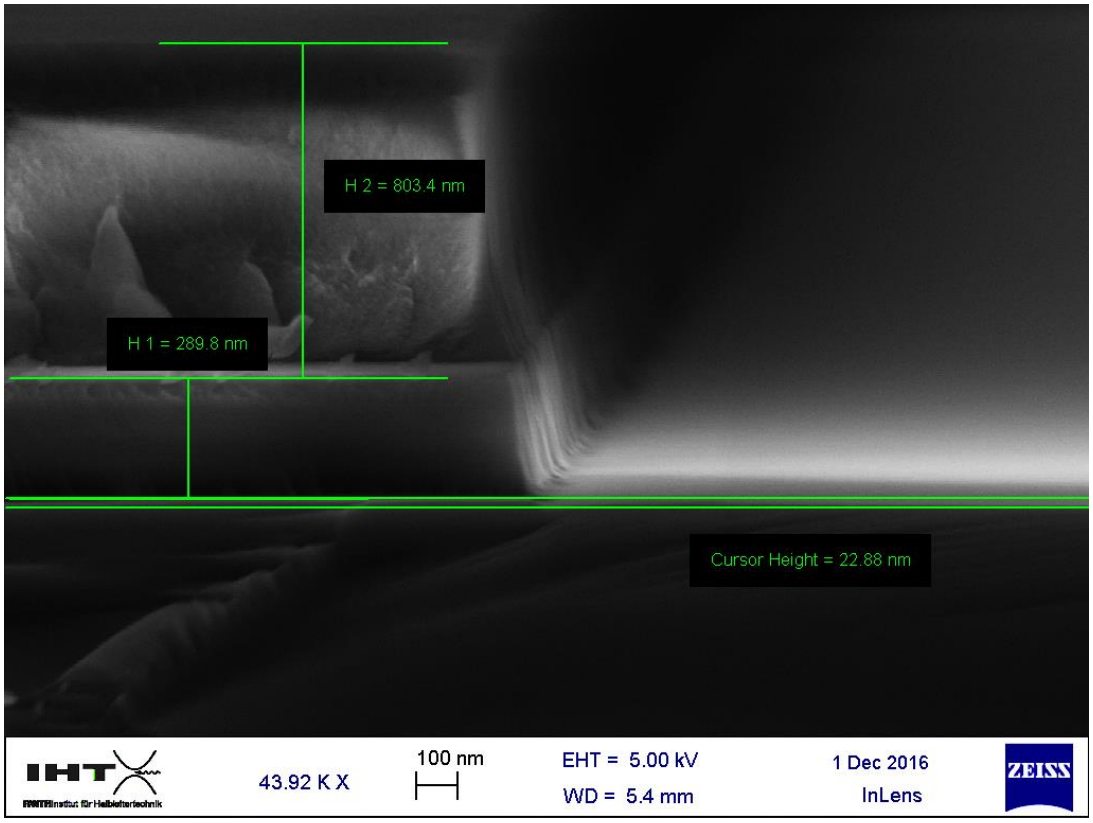

Figure 11. SEM image of the sample processed for 32 minutes in RIE 51

Deep Reactive Ion Etching

After patterning the PR and Oxide layer, the last step is to structure Si layer. There are two kind of samples, one with the thickness of 575 micron and other with 275 micron. Both are used for the device fabrication. The Si layer can be structured by deep reacting ion etching. The tool used for this process is COBRA etching tool, in which we can follow either Cryogenic process or High Aspect Ratio (HAR) - Bosch process. Here, the former one is used. The etch rate of the Cryo process is about 5.46 micron/min. The sample with the thickness of 275 micron is processed for 50 minutes. Considering the safety of sample and the carrier wafer, the whole process was divided into two half of 25 minutes each with O_2 clean of 2 minutes in between. After the completion of the process, the sample was observed in SEM. The result was surprising, the PR was scattered all over the surface. The SEM image of surface of the Sample is shown in figure 12 (a) and (b). The reason for this ambiguity is discussed in the next section.

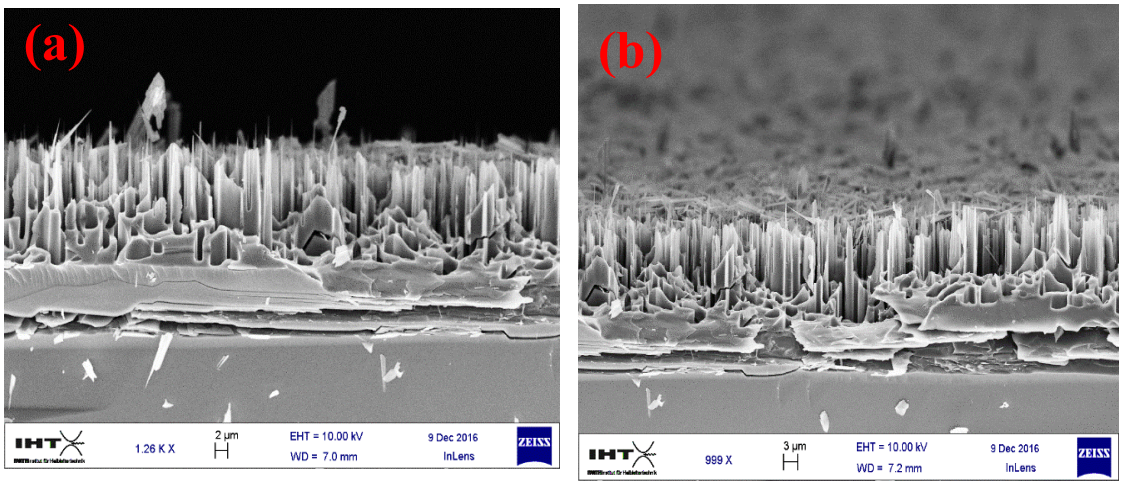

Figure 12. (a) & (b) Showing the sample's surface after Cryogenic etch for 50 minutes

4.2.2. Fabrication Ambiguities & Solutions

In Section 4.2.1, a process flow for the device fabrication was created. The results up to Oxide layer etch was satisfactory but in the final step during Si etching, there was scattering of PR over the substrate. After a careful observation, it is noticed that the problem might cause because of Poor Selectivity of Oxide layer or the Instability of PR layer [13]. The tool specification sheet provided by the company clearly is shown in figure 13.

Parameter	High Rate DSE	High Aspect DSE	Smooth DSE 1	Smooth DSE 2	SOI DSE [1]
Process Chemistry	Bosch SF_6-C_4F_8	Bosch SF_6-C_4F_8	Bosch SF_6-C_4F_8	Cryogenic SF_6-O_2	Bosch SF_6-C_4F_8
Feature Size µm (Trench)	50	2	5	10	10
Exposed Area /%	< 5	< 5	< 10	< 5	< 10
Etch rate /µm/min	> 10	> 1	> 1	> 2	> 2
PR Selectivity	> 125	> 25	> 25	> 50	> 50
SiO_2 Selectivity	> 300	> 50	> 50	> 100	> 100
Profile control	90° ±1°	90° ±1°	90° ±1°	90° ±1°	90° ±1°
Bosch scallop / cryo roughness /nm	< 330	< 150	< 50	< 5 rms	< 120
Notch [1] /nm	-	-	-	-	< 250
Uniformity (in-wafer) /%	< ± 5%	< ± 5%	< ± 5%	< ± 5%	< ± 5%
Reproducibility (run-run) /%	< ± 3%	< ± 3%	< ± 3%	< ± 3%	< ± 3%
Aspect Ratio	< 1	< 30	< 5	< 3	< 3

Figure 13. Specification Sheet of OXFORD COBRA etching tool

Solution to Selectivity of Oxide Layer

Assuming that the problem was with the thickness of Oxide layer i.e. SiO_2. A solution was decided. The SiO_2 layer was then replaced by Alumina layer (Al_2O_3). Al_2O_3 offers an exceptional selectivity compared to SiO_2. Now, few of the same samples, which were coated with SiO_2 layer on both the side are removed from one side using BOE. After the removal of SiO_2, a layer of Al_2O_3 of about 300nm was deposited by ALD, shown in figure 14(a). Again the same process flow was repeated. But this time, to etch Alumina layer, BOE is used. The rate of BOE for Alumina etch 23.2 nm/min. But again the issue was Instability of PR because of BOE, which is shown in figure 14(b).

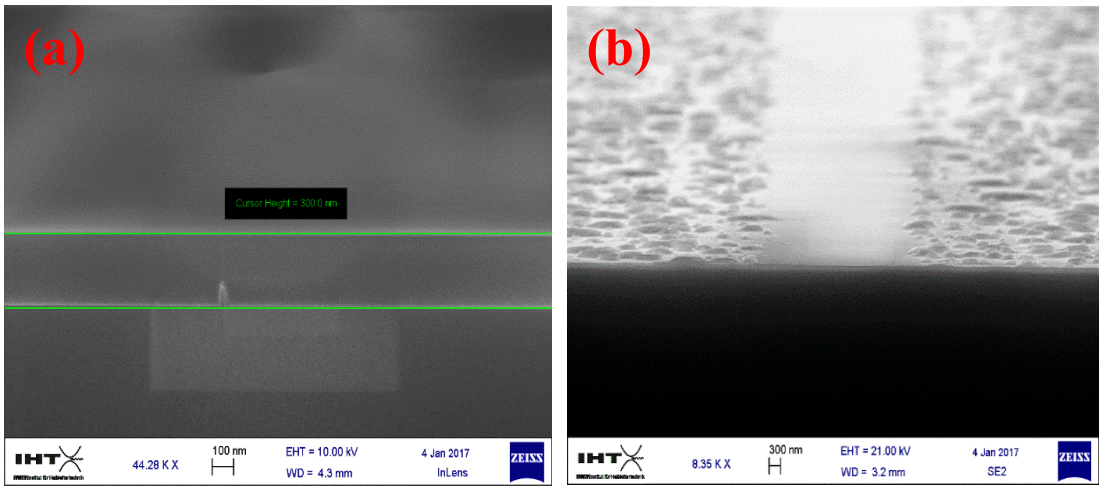

Figure 14. (a) Thickness of alumina layer deposited. (b) Instability of PR due to BOE

Solution to the Instability of PR layer

The resist used for the fabrication is AZMIR 701, which is a thin resist and showed instability to BOE [13]. In order to stabilize the resist layer, two different methods were adopted. First, few samples are post baked at 115 degree for 30 minutes. Second, few samples are post baked at 120 degree for 30 minutes. Two methods are illustrated below in figure 15 & 16.

Figure 15. Method 1

Figure 16. Method 2

Few Samples were treated by each of the above two methods and then result was observed in SEM. In figure 17, the images related to Method 1 are shown. In figure 18, results of Method 2 are shown. Both of the methods produced almost the same result, which are not satisfactory at all. The PR still remained unstable and does not produce the desired outcome.

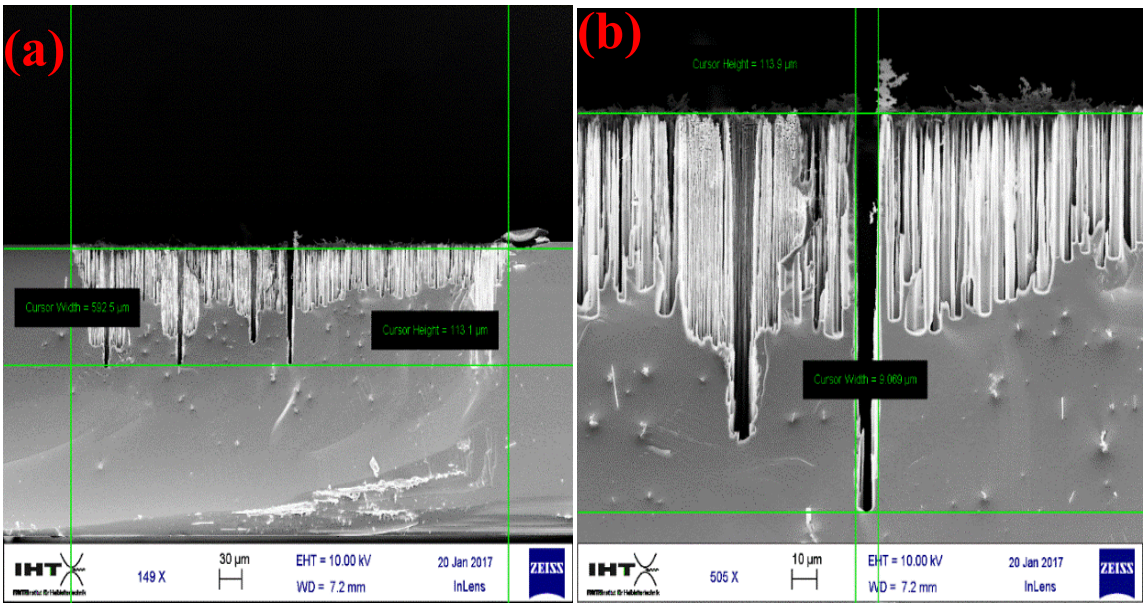

Figure 17. (a) & (b) showing the SEM image of sample with Method 1 after final etching.

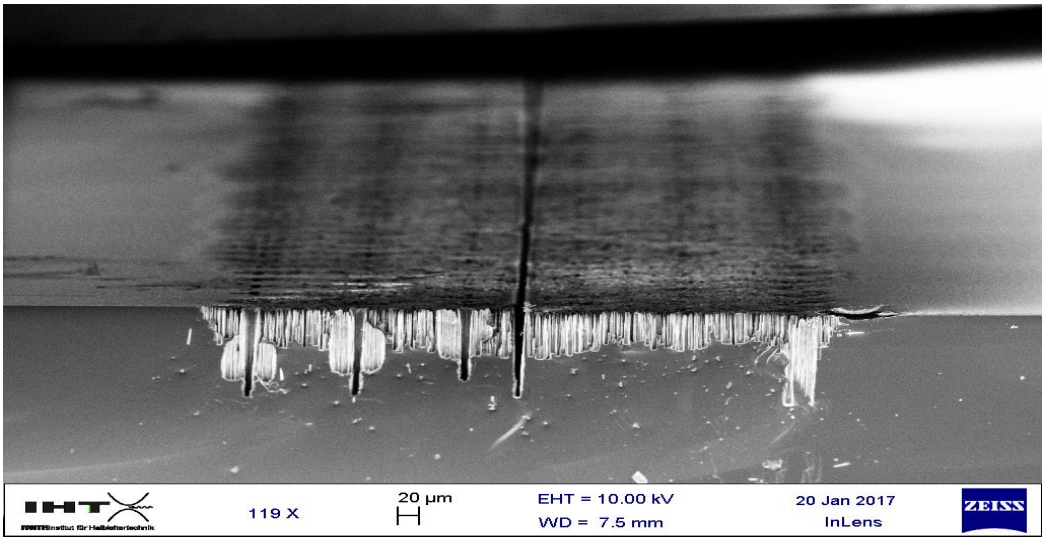

Figure 18. SEM image of the device fabricated using Method 2

4.2.3. New Work Plan

After analysing the ambiguity of the previous work, it can be concluded that the problem was not with the thickness of the Oxide layer but it is the thin PR layer, which is unstable to the processes. In order to solve the problem, the thin resist should be replaced by a thicker one. Previous resist was AZMIR 701 which will now be replaced by AZ9260, a honey resist. The standard recipe for AZMIR-701 was available but so is not with AZ9260.

New Photo Resist: AZ9260

Several experiments needs to be performed with different samples, in order to formulate a standard recipe for the new resist. It is not an easy task to handle such a thick resist. To determine the optimum parameters such as: spin rate, acceleration time, exposure time, development time etc. different values were tested and the results were observed in SEM. After several tests a final standard recipe for the thick resist AZ9260 was formulated. Few experimental data which were trailed to finalise the recipe of the new resist are listed in Table 1. The favourable set of parameters, which will be used further in fabrication of the final device is highlighted in bottom most of the table 1. The SEM

images of the device fabricated with few best possible set of parameters are shown in figure 19.

Table 1. Experimental data for Final Recipe of AZ9260

Sl. No.	Spin speed (rpm/min)	Acceleration	Spinning Time(sec)	Exposure time (sec)	Development time (min)	Channel WL(nm) @15mWcm^{-2}
1.	2500	250	70	40	4	405
2.	2500	500	65	40	4	405
3.	2500	1000	62.5	40	5	405
4.	3000	250	70	40	6	405
5.	3000	500	65	60	6	405
6.	3000	1000	62.5	70	6	405
7.	**3000**	**1000**	**62.5**	**90**	**6**	**405**

A lot variation in these parameters were tested. The above-mentioned set of parameters are the best among all the trailed parameters.

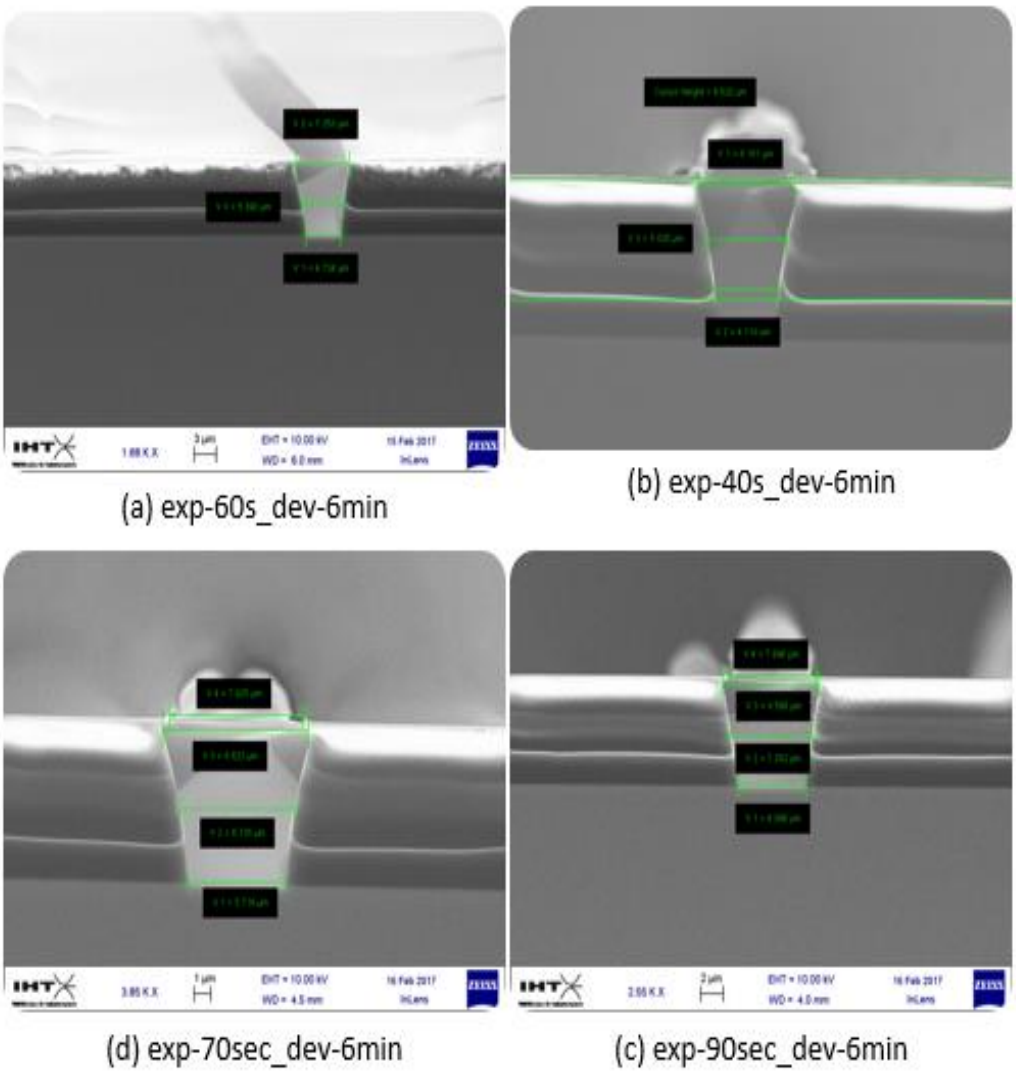

Figure 19. (a), (b), (c), & (d) showing results by altering the parameters for AZ9260 recipe

Comparison of Photo-resist Recipe

There are many differences between the old and new resist in terms of processing. A brief comparison between AZMIR 701 and AZ9260 is shown in table 2. AZ9260 is a thick resist**,** which needs a longer processing time compared to thinner one. AZ9260 resist layer can be developed using both AZ726 MIF and AZ400K, but the former one preferred. The reason was AZ400K contains metal ion and it requires dilution before its use. In order to avoid the cross contamination in the clean room AZ726 MIF has been used. Although both the developer solution has almost the same effect on the resist layer and also the development duration is almost equal.

Table 2. Comparison between Thick and Thin Photo resist.

AZ9260	AZMIR-701
• Positive Thick resist	• Positive Thin resist
• Lower Optical absorption	• Higher Optical absorption
• High Spin rotation time(62.5sec)	• Low spin rotation time(30 sec)
• Higher Post bake(165sec@110^0 C)	• Lesser Post bake(60sec@90^0 C)
• Higher exposure time(90 sec)	• Lesser exposure time(10 sec)
• Higher Development time(6 min)	• Lesser Development time(60 sec)
• AZ 726 MIF/AZ 400K: dev. solution	• AZ 726 MIF : dev. Solution

4.3. Fabrication With AZ9260

After the finalisation of the standard recipe of the new PR, the fabrication work again started using the same initial process flow. The only changes made in the process flow is the new resist and its corresponding recipe. In the previous case, everything was perfect up to the Oxide layer etching. The problem was with the etching of Si. As discussed in chapter 3, for deep etching into Si substrate deep reactive ion etching is required. This can be done by either Cryogenic process (or) HAR- Bosch process [12]. In previous process Cryogenic etching was used. But after considering the specification sheet of the new resist layer, Bosch process is preferred than the former one [14]. The reason was the Operating temperature. A brief comparison between Cryo and Bosch process is shown in table 3. Although the etching rate of the Bosch process is slower than the Cryo process but the operating temperature makes the survival of resist layer for long. The fabrication process continued with process flow and the Si etching has been done by Bosch process. This time the results are quite satisfactory. The SEM images of the result is shown in figure 20.

Table 3. Comparison between Cryogenic etching process and Bosch etching process

CRYOGENIC ETCH	BOSCH ETCH
Etch rate **= 5.46 micron/min**	Etch rate = **2.9 micron/min**
Operating Temp. : -**100**^{0} **C**	Operating Temp. : -**5**^{0} **C**
Sidewall passivation relies on Oxygen(O_2)	Sidewall passivation given by CF_6
Aspect ratio Independent etching	Aspect ratio dependent etching

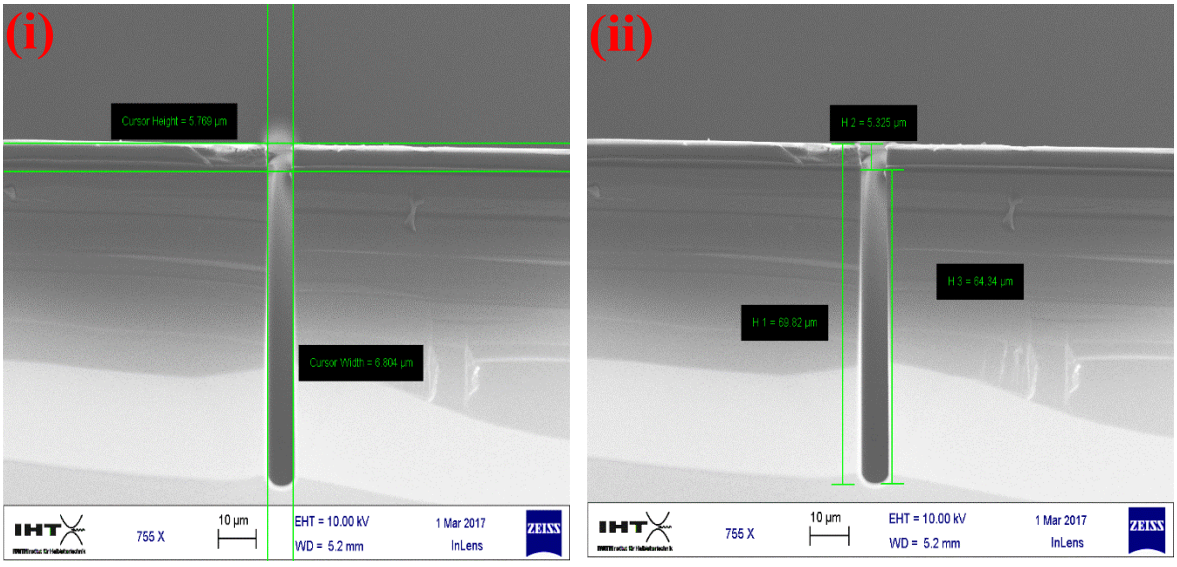

Figure 20. (i) & (ii) SEM image of Si etch into the substrate by HAR Bosch etching process

This time the etching into the Si is perfect. The above depth of etching was achieved by Bosch process for 30 minutes. The depth is 64.34 micron. Deeper depth can also be achieved by increasing the duration of the process. This time the surface of the device looks perfect with the clear visibility of the marker structure. The SEM images of the surface and trench line is shown in figure 21.

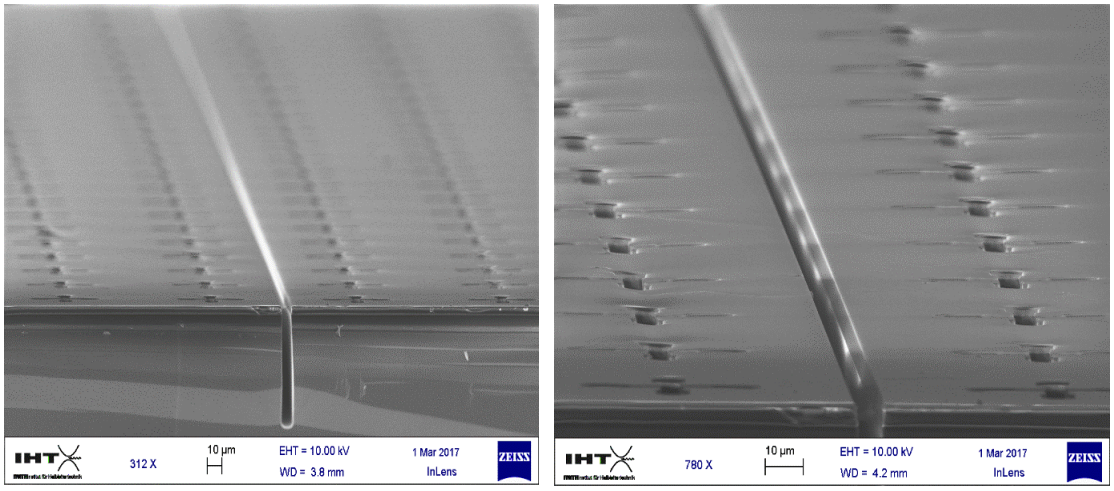

Figure 21. SEM image of the Surface of the device after Bosch etching for 30 minutes

4.3.1. BOSCH Etching Process Parameters

HAR- Bosch process was used to achieve the above result. The steps followed in the process and the process parameters used for the final device fabrication is shown in table 4. In the table the first step was Descum process. It is necessary to run this step in order to remove the remaining photo-resist in the target area of etching. The duration of each step and other parameters are shown.

Table 4 Process Parameter followed for deep Si etch using COBRA tool.

Material to be Etch	Process	Temp (degree Celsius)	SF6 (sccm)	O2 (sccm)	C_4F_8 (sccm)	Pressure (mTorr)	ICP (W)	HF (W)	Time (min)
PR	Descum	-5	-	20	-	2	-	10	1:00
Si	HAR-Bosch	-5	200	-	10	40	1600	5/40	15:00
-	SF6 / O2 Clean	-5	10	50	-	30	1500	-	2:00
Si	HAR-Bosch	-5	200	-	10	40	1600	5/40	10:00
-	O2 Clean	-5	-	50	-	30	1500	-	2:00

4.3.2. Isotropic Etching

The etched structure into the Si shown in figure 20 & 21 are perfect but the aim of fabricating this device is to obtain maximum amount of strain. Straining with such opening is possible but it can be further improvised by making the etched structure laterally deep. The benefit of laterally deep structure will be its flexibility towards bending in comparison with the previous one. The propagation of the strain will be from curve path which will enhance the resistance of the device towards break down. In simple words, the device's sustainability will increase towards external applied strain. Such lateral deep etching can be achieved by Isotropic etching. The device processed with Isotropic etching is shown in figure 22 (a) & (b). It is clearly visible that the now the etching profile is isotropic.

Process parameter for Isotropic etching:

It is similar to Bosch process with little modification in process parameters. The process parameters are shown in table 5.

Table 5. Process Parameters for Isotropic etching

Process	Isotropic etching
Material to be etched	Si
Temperature(degree Celsius)	-5
SF6 (sccm)	200
O2 (sccm)	-
C_4F_8 (sccm)	10
Pressure (mTorr)	40
ICP (W)	2000
HF (W)	55
Time (min)	10:00

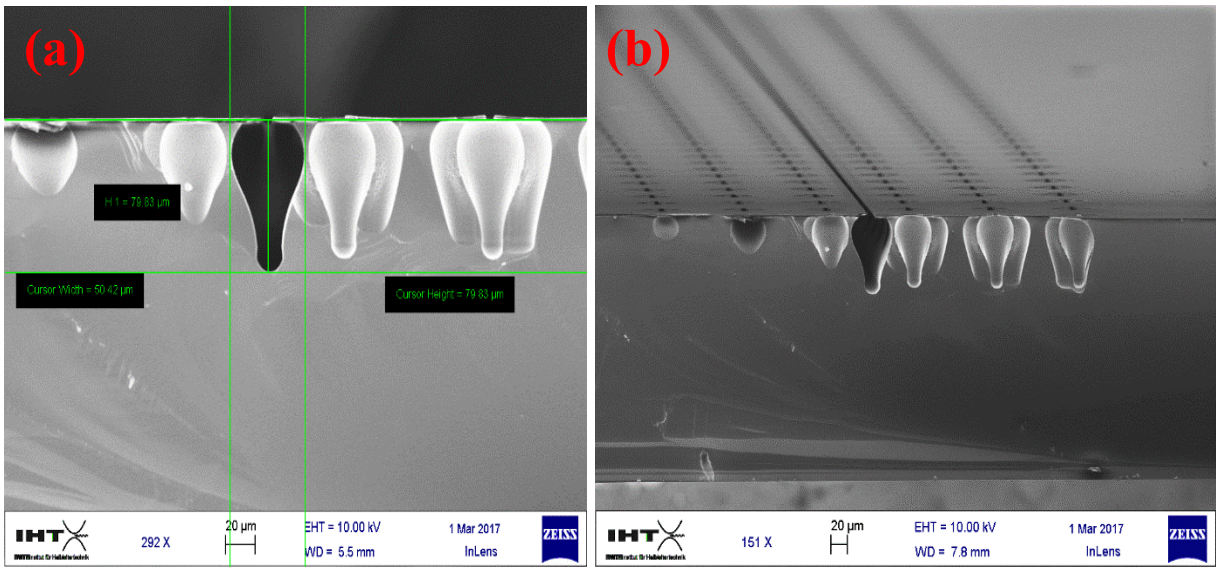

Figure 22. (a) & (b) SEM of the Isotropic etching for 10 minutes

4.4. Final Process flow

After a long hit and trail method, the final structure of the device was obtained. The desired structure of the device is shown in figure 22. There must be a process flow chart in which steps of fabrication should be clearly mentioned from starting to end. A complete final process flow is shown in the flow chart below in figure 23.

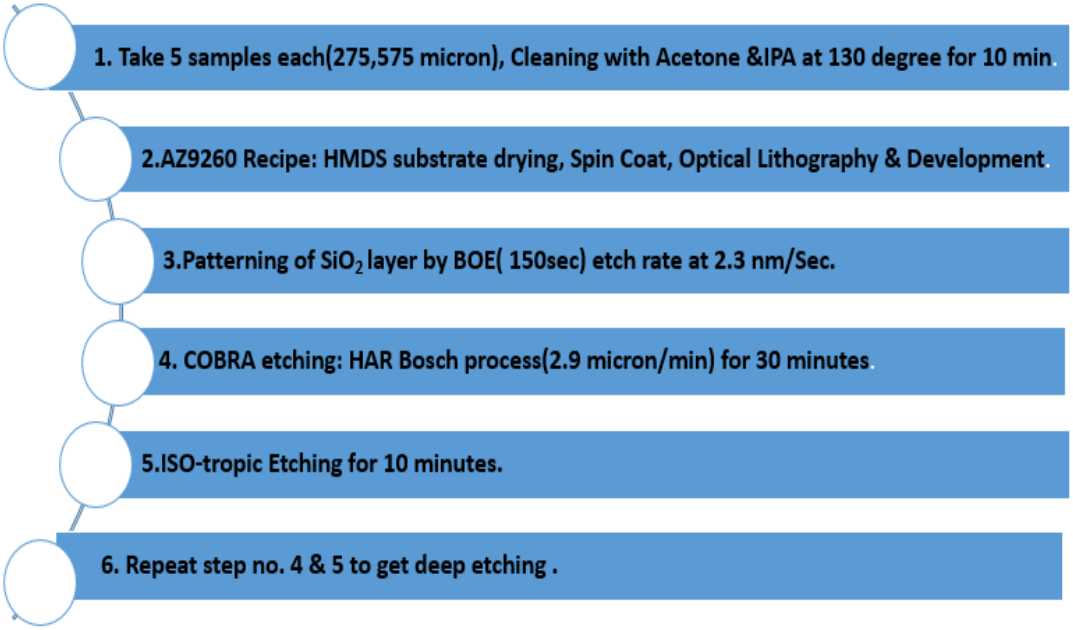

Figure 23. Final Process flow for the device fabrication.

4.4.1. Deep Etching

Using the above process flow, a device can be fabricate which will use in inducing strain in micro/ nano flakes. The last step in the process flow shown in figure 23 will play a vital role when it comes to amount of strain. Deeper the trench structure, better will be the device in terms of flexibility. And that can be achieved by repeating the Bosch etching process and isotropic process. By altering the duration of these two processes different depth of etching were obtained. They are shown in figure 24, 25 and 26.

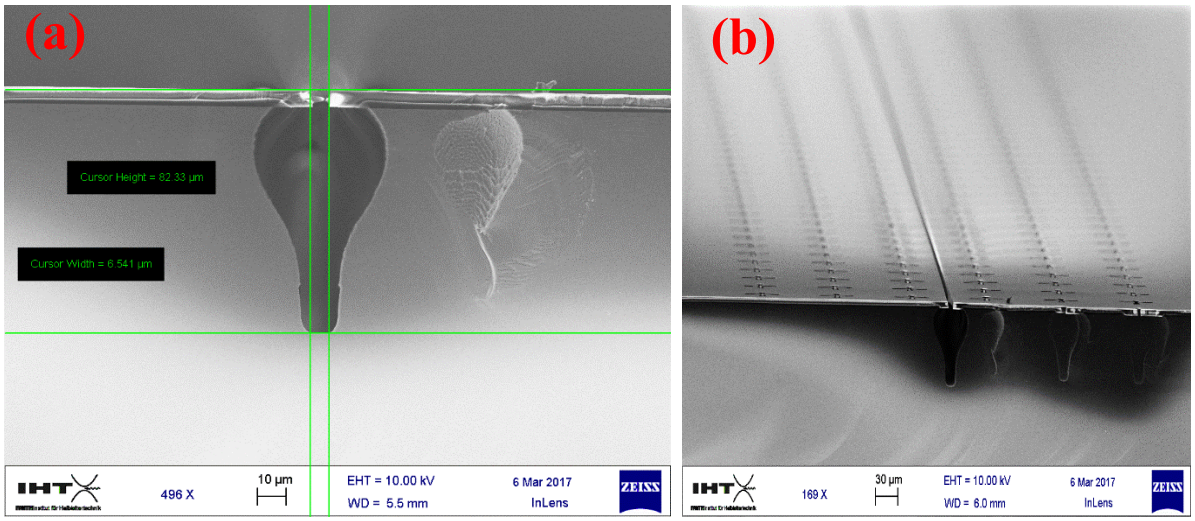

Figure 24. (a) & (b) Etching depth of 82.33 micron after 1 time Bosch + 2 times Isotropic etch.

In figure 24, the depth of Si etched is 82.33 micron, which is resulted from 1 time Bosch etch and 2 times Isotropic etch. Similarly, in figure 25, the etching depth achieved is 103.8 micron which is resulted after 2 times Bosch etching (30 min) and once Isotropic etching (10 min). In figure 26, the depth reaches to 142 micron after 3 times Bosch etching (45 min) and once isotropic etching. Hence, the variation in the etching depth can be manipulate by repeating the HAR-bosch and Isotropic etching process. The alteration in etching time and the depth profile are noted in Table 6.

Table 6. Etching depth variations corresponding to etching time

Bosch Etch(15 min each)	Isotropic Etch(10 min)	Depth of Etching(micron)
1	1	79.83
1	2	82.33
2	1	103.8
3	1	142.0

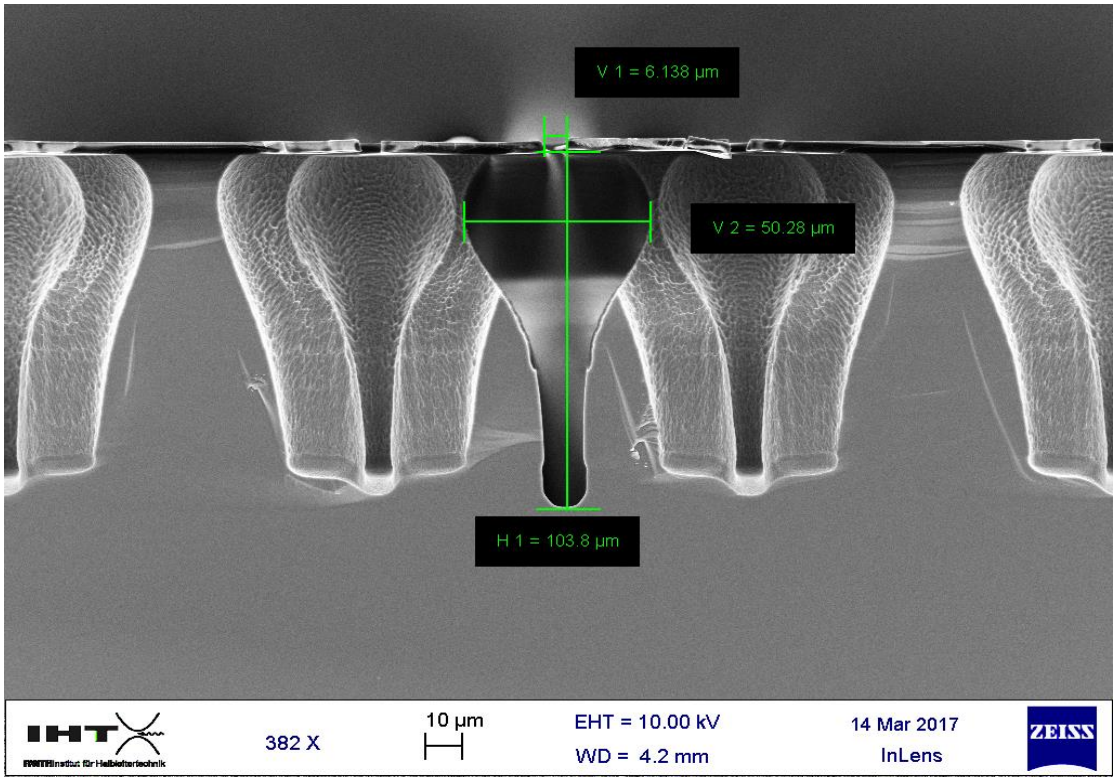

Figure 25. SEM image of etching profile after 30min Bosch + 10min Isotropic etch

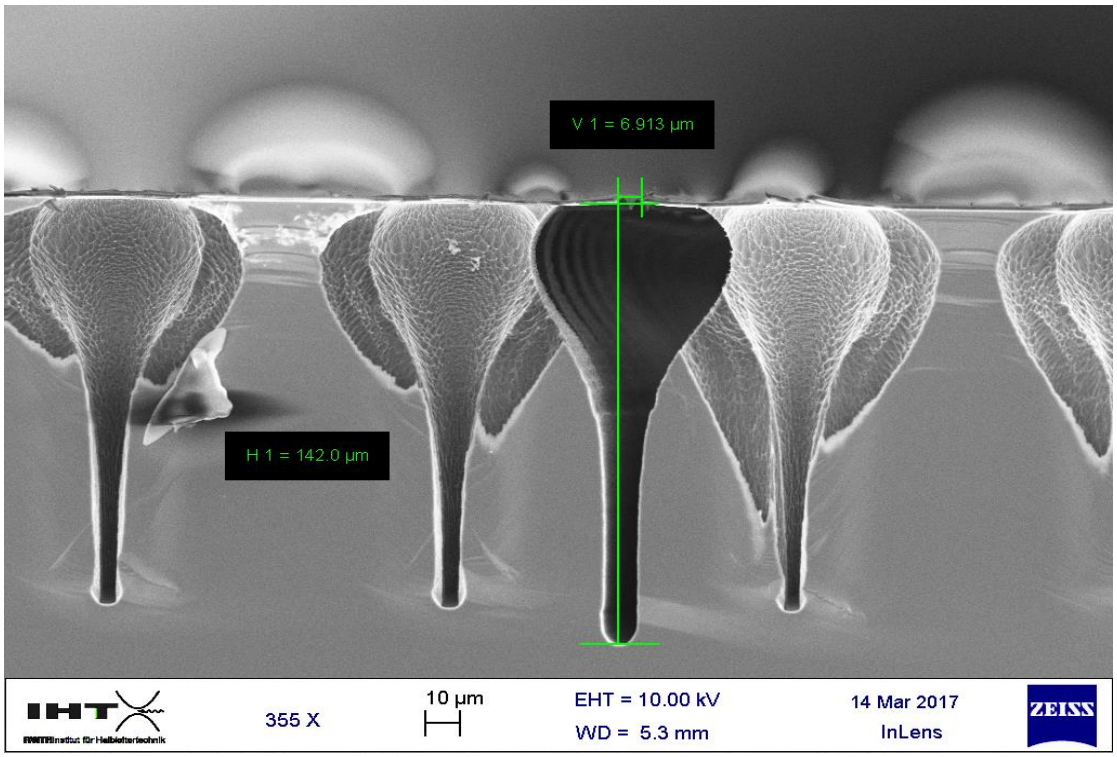

Figure 26. SEM image of etching profile after 45min Bosch + 10min Isotropic etch.

4.5. Final Device Look

From the beginning of this chapter, an initial process flow was made. Working with that process flow various fabrication difficulties were faced. The ambiguities were solved by hit and trail method. Due to instability of the thin resist, a new thicker resist is used. After all these steps, we finally came up with a complete process flow chart which indicates all the steps in sequence to fabricate the strain device. In order to achieve the variation in etching depth into Si substrate, few steps need to be repeat. Overcoming with all the fabrication issues, the device finally fabricated. The final look of the device is shown in figure 27. The trench line is in the middle of the device and marker structures are in either side of the deep etch structure. The device then treated in Plasma ashing tool in order to remove the remaining photo resist layer from the device. The final device has only a thin layer of Silicon dioxide on the top of Si substrate. In the next chapter we will investigate the usefulness of the device by straining it and calculate the optimum percentage of the strain it can bear before break down.

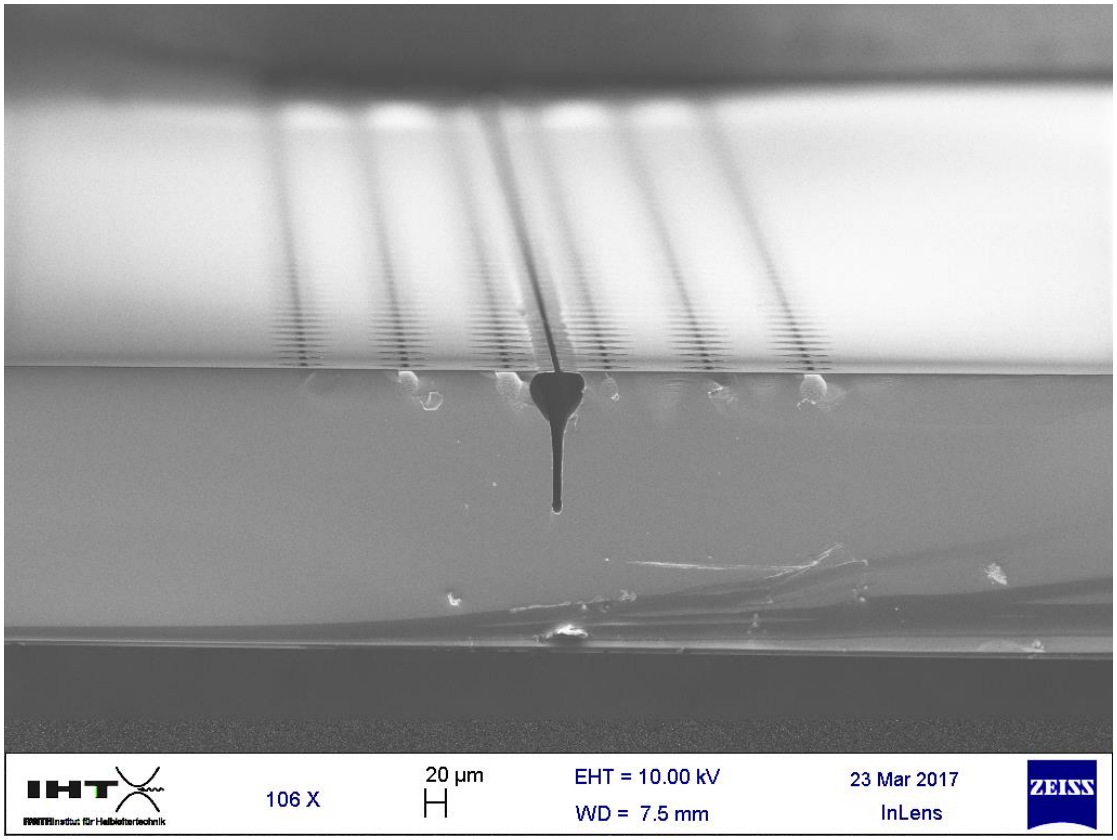

Figure 27. SEM image of the Final device fabricated using micro-electronic step

Chapter-5

5. Measurements

In Chapter 4, The Process flow of the fabrication was discussed and a final straining device has been fabricated using different micro-electronics steps. In this section we will perform the tests and measurements in order to check the flexibility of the device towards strain and calculate the maximum possible amount of strain (in percentage) before its breakdown. Strain measurement with such micro structure is not an easy task. Although we can induce strain by some means but the important factor is how to quantify the amount of strain applied? A setup shown in figure 28 can create strain in the device but the drawback with it is its Size. The setup is large enough to place inside a SEM or in an Optical Laser Microscope. So, the visibility and measurement of Straining effect will be an issue. A better solution to the measure the strain is discussed in section 5.1.

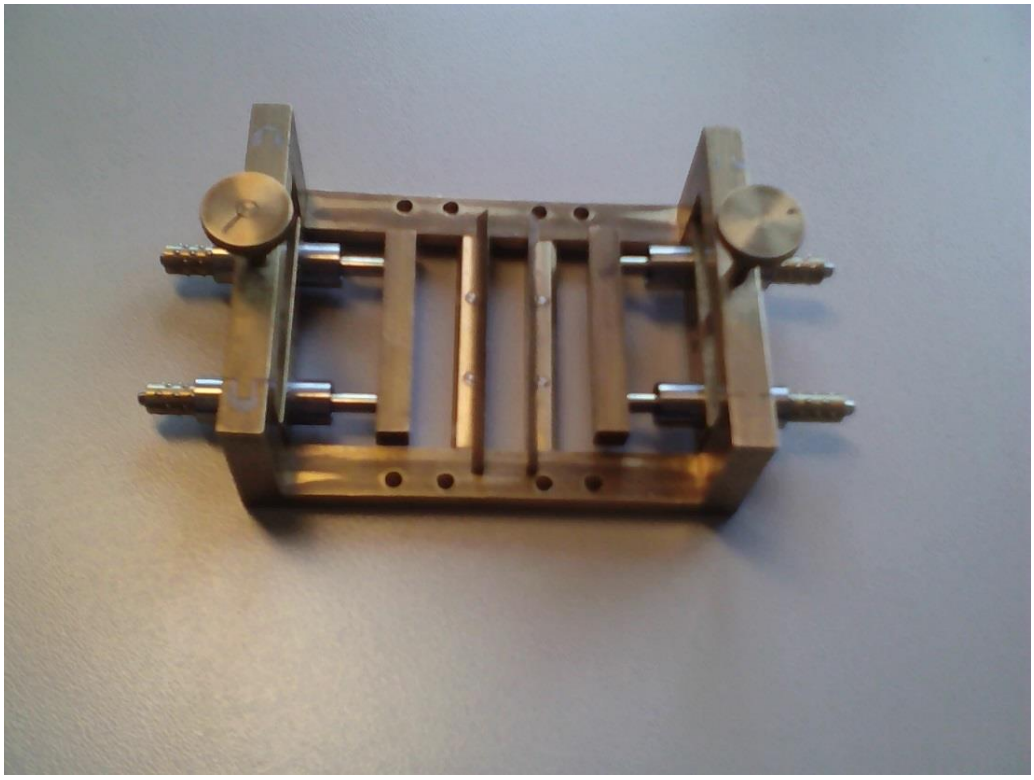

Figure 28. A Setup with top & side screw to Create Strain in Sheets/Wafer type material.

5.1. Strain Measurement

The device can be strained with various external sources but the key idea is to have a visual evidence to the strain happening to the micro structure and calculate the strain percentage. One of the finest method to do so, is to observe the width of the opening of trench structure. If the width of the trench can be measured before and after straining, then the percentage of strain can be calculated easily by using the following equation.

$$Strain(\%) = \frac{Original\ Width\ of\ the\ opening - Width\ of\ the\ opening\ after\ Strain}{Original\ Width\ of\ the\ opening}\ X\ 100 \quad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Strain Tests

The method used in this work in order to induce the strain in the device and calculate it, is a manual one. Several tests were performed and the amount of strain has been calculated. In this work, the source of induced strain in the device is a SEM cross-sectional sample holder with a Screw on it. One part of the device is clipped and placed on the sample holder, which is supported by two other small piece of Si wafer sticked on the sample holder surface using black tape, which results in a hinge like of structure. At the same time, the clipped device will be placed such that the screw will be in direct contact with the middle portion of the device and can be strained by tightening the screw of the holder. On each successive test, the screw will be tighten gradually, until the device reaches its break down. The variation in bending of the device will vary the width of the opening of the trench as well and can be observed clearly in SEM. The image of the hinge type structure is shown in figure 29 (a) & (b). In figure 30, the original width of the opening i.e. before straining is shown. The device has an initial width of the opening is 6.665 micron.

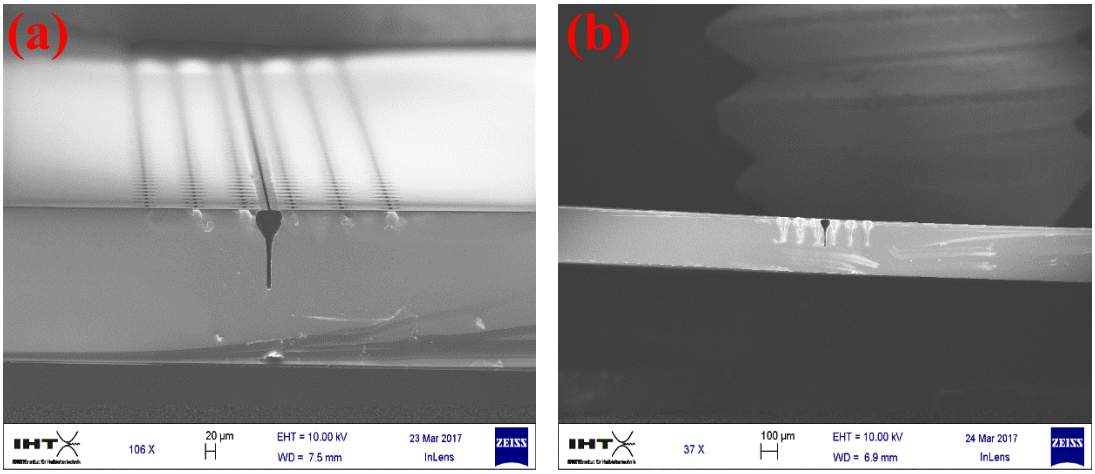

Figure 29. . a) device on setup with compressive strain. b) Hinge like structure

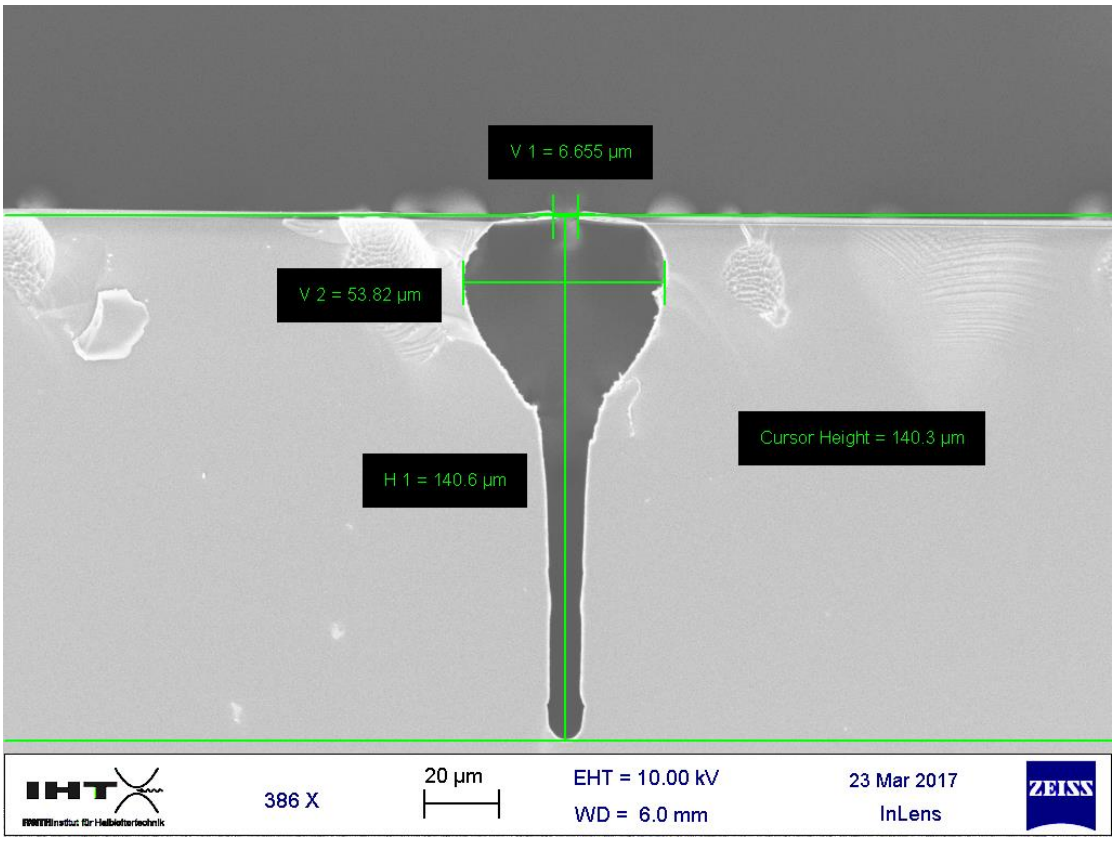

Figure 30. SEM image of the device showing the width of the opening before applying Strain

TEST 1

Tests will determine the flexibility of the device. Therefore, the device was tested a number of times by varying the strain amount. In Test 1, the screw of the sample holder was tighten little bit such it will create a strain in the device. The result of the strain is shown in figure 31 and 32. The opening width of the trench is clearly visible and it widen to 7.368 micron.

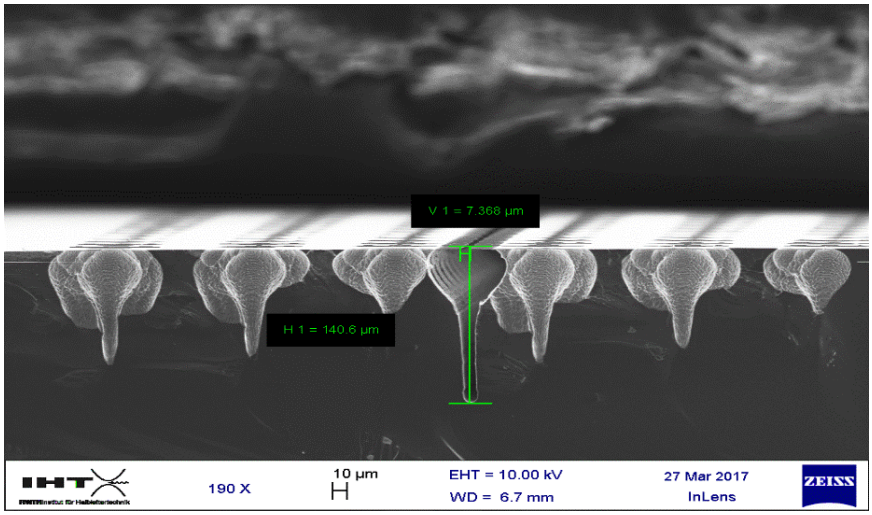

Figure 31. SEM image of the device after TEST 1.

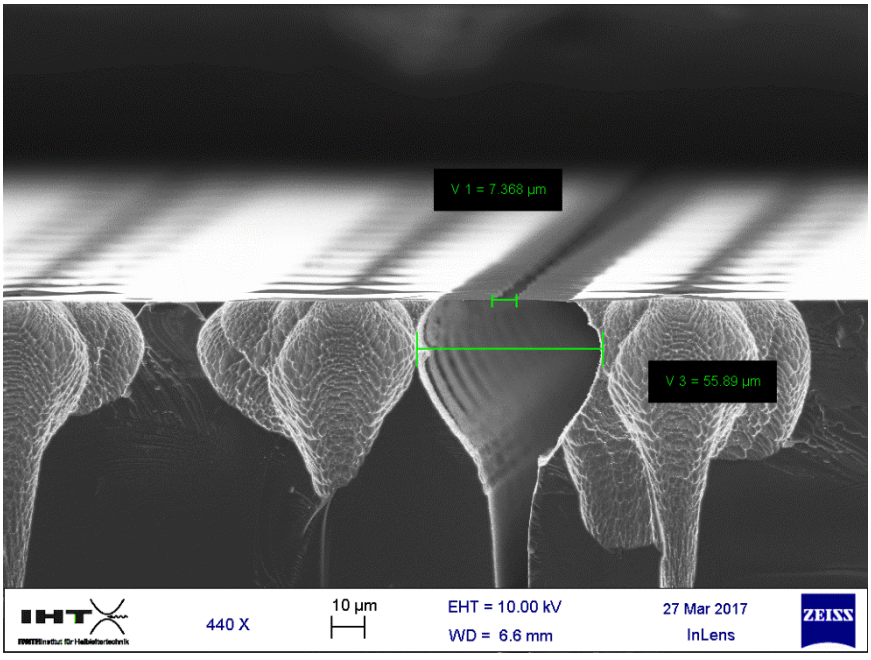

Figure 32. Straining effect on the opening of the trench after TEST 1.

TEST 2

After Test 1, a gradual increase in strain level has been done in order to check the optimum strain capacity of the device. The screw is tighten further to investigate the width of the opening. The observation was satisfactory as the device survived with the strain and the opening further widen to 7.392 micron. The image of Test 2 is shown in figure 33 & 34.

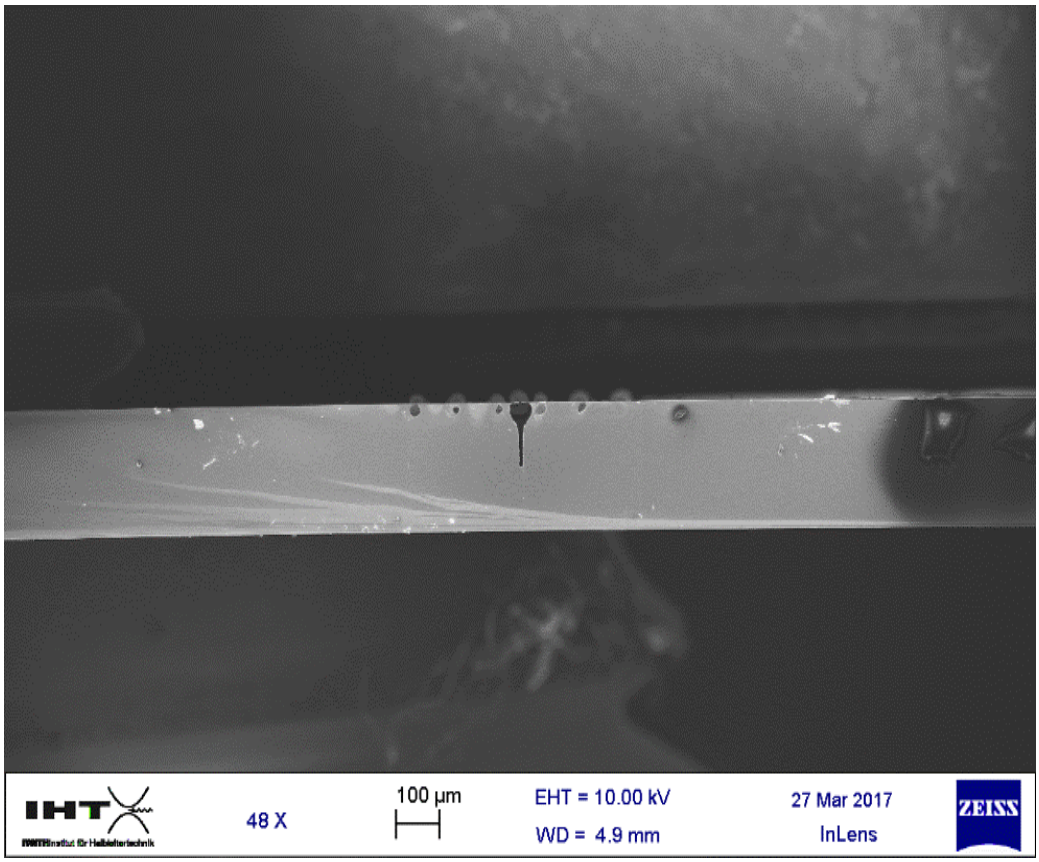

Figure 33. SEM image of the strained device after Test 2

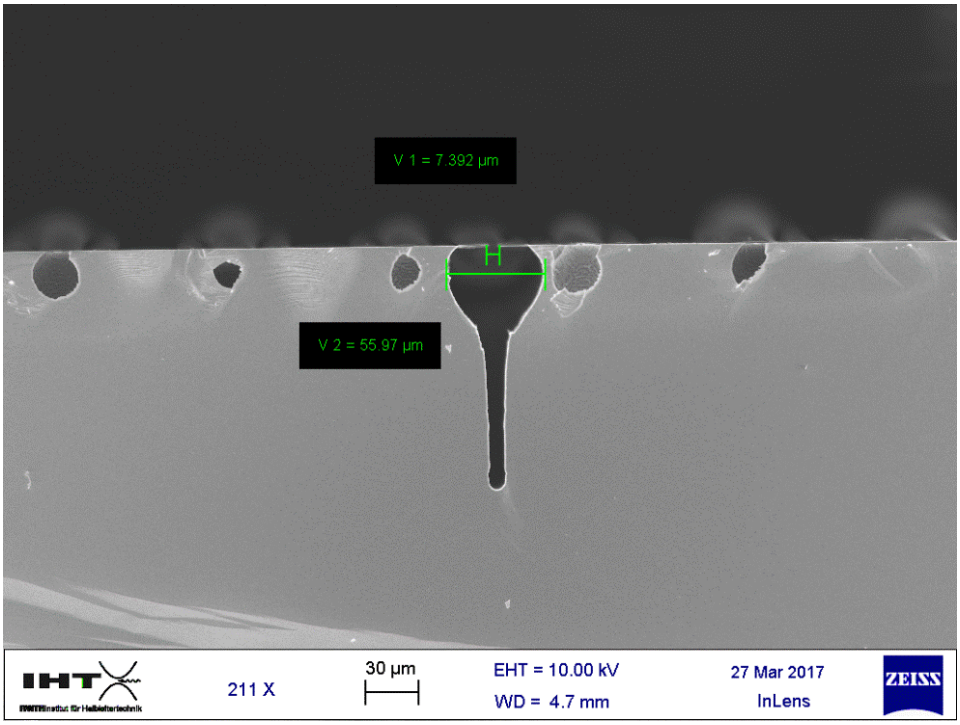

Figure 34. SEM image of the Opening of the trench after Strain Test 2

TEST 3

Sustained with Test 2, the device is strained further to check its maximum strain bearing limit. The Screw is tighten further and the result was seen in SEM. Now, the width of the opening reached to 7.457 micron. The device still looks fine without any crack on the opening. The image of Test 3 is shown in figure 35.

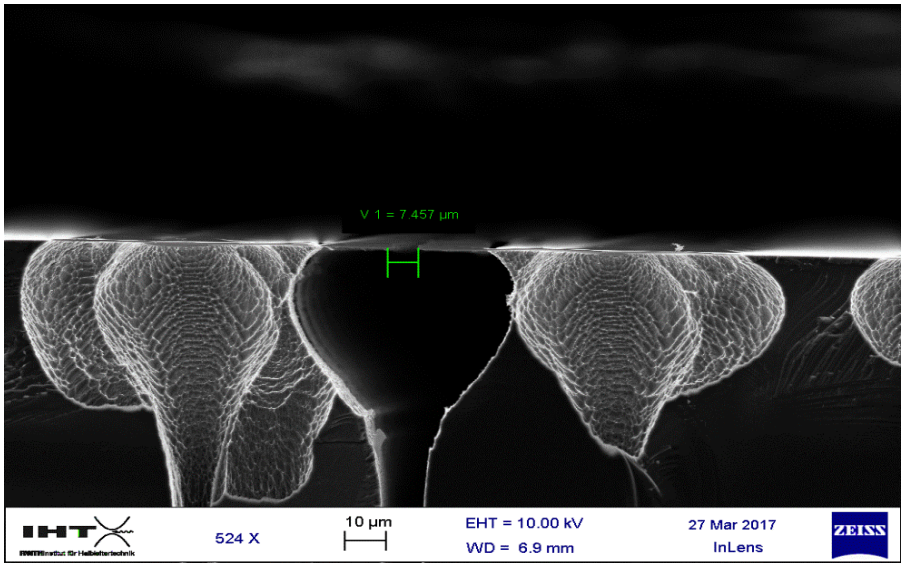

Figure 35. Width of opening of trench after strain Test 3

TEST 4 (Break down)

With the success of Test 3, the device is strained further to check its limit. This time the device reached its maximum limit and broke down from the middle. The images of Test 4 is shown in figure 36. Hence, it can be concluded that the optimum withstand strain for the device was achieved in Test 3.

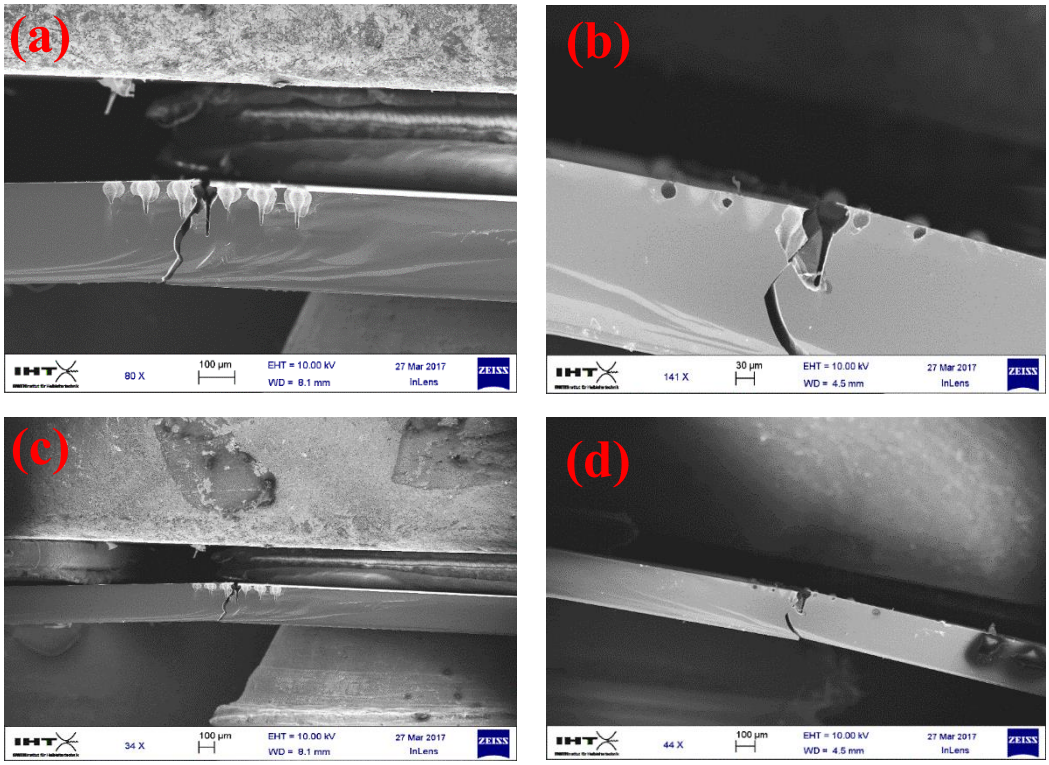

Figure 36. (a), (b), (c), (d) showing the breakdown of the device due to over strain in Test 4

The above four tests were done in order to check the usefulness of the device. It has been shown clearly that, the width of the opening is varying with variation in external strain. Before applying strain the width of the opening was 6.665 micron, which has been successfully altered to 7.368 micron, 7.392 micron and 7.457 micron in Test 1, Test 2 and Test 3 respectively. Using these information, The Strain percentage is calculated in section 5.2.

5.2. Calculation

In this Section, the amount of strain can be quantify using the information from the SEM image. The ratio of the differential width of the opening to the original width of the opening will give the amount of strain. Using the equation (4), the calculation can be done as follow

For Test 1:

$$Strain(\%) = \frac{Differential\ width\ of\ the\ Opening}{original\ width\ of\ the\ Opening}\ X\ 100\ ;$$

$$= \frac{7.368 - 6.665}{6.665}\ \text{X}\ 100 = \mathbf{10.547\ \%}$$

For Test 2:

$$Strain(\%) = \frac{Differential\ width\ of\ the\ Opening}{original\ width\ of\ the\ Opening}\ X\ 100\ ;$$

$$= \frac{7.392 - 6.665}{6.665}\ \text{X}\ 100 = \mathbf{10.907\ \%}$$

For Test 3:

$$Strain(\%) = \frac{Differential\ width\ of\ the\ Opening}{original\ width\ of\ the\ Opening}\ X\ 100\ ;$$

$$= \frac{7.457 - 6.665}{6.665}\ \text{X}\ 100 = \mathbf{11.883\ \%}$$

Strain percentage for all the three tests were calculated. In test 1, the achievable strain is 10.547% and then increased to 10.907% and 11.883 % in Test 2 and 3 respectively. The maximum strain obtained is 11.883%, which is a very high value for the two-dimensional material. In Test 4, the device reached the break point which can be seen from the figure 36.

Chapter-6

6. Conclusion & Outlook

6.1. Conclusion

The intension behind the fabrication of such a novel device is to develop a source of strain for two dimensional materials, especially layered materials. The thickness of these materials are very low. So, mechanical way of straining results in damaging of surface and induce dis-orders. The key idea was to fabricate such a trench like structure on which flakes can be mounted easily and can be strained atleast above than 5-10 %. The summary of this work can be given as below:

- The complete fabrication of the device was done by micro-electronics steps. The initial process flow has encountered various ambiguous conditions, which were solved and a final process flow was made.
- The most crucial step in the process flow was etching. There were 3 different materials to be etched namely Photo-resist, Oxide layer and Silicon. PR was patterned by developer solution and can be removed by using acetone followed by propanol.
- Oxide layer was etched by using BOE. The difficulty in this process is its vetch rate variation.
- Si can be etched (or) structured using deep reactive ion etching. Which can be done by either Cryogenic process or HAR Bosch process. In the final process flow the later one is preferred over the former one.

- Isotropic etching was just the modification of few parameters of Bosch process. But this etching made the device more flexible, thus became a mandatory step in the process flow.
- The etching depth variation was done by using the Bosch and Isotropic etch in repetitive loop.
- The final device was tested by applying external strain up to its break down. And a maximum of 11.88% of feasible strain was noted.

The future aspects of this device is discussed briefly in the next section.

6.2. Outlook

In this section, all the future prospective related to the device were discussed and how this device will be useful in 2D material characterization. The fabricated device will be a vital straining source for the 2-Dimensional materials. Layered materials can be mechanically exfoliated by using blue scotch-tape method. The exfoliated flakes can then be transferred by 2D material transfer technique and those flakes will be mounted in the middle of trench structure. The location of the flakes can be monitored by Optical 3D laser microscopy. After observing the correct position, flake will be fixed by making metallic contacts. Then the flake can be strained and the strained flake can be observed under Raman microscopy to investigate the modification in band gap. Further, the electrical and optical property can also be checked by doing different characterizations.

PROCESS PARAMETERs

Standard-Clean - wafer -

Preparation:

• fill the basins with the desired acid/base carefully • turn on heating system (80°C)

1) ***piranha-acid (removes coarse organic contaminations)***

a) **10 min @ 80°C: H_2O_2: H_2SO_4** (1.25l: 3.75l)

(*Attention: In this case you first have to fill in the* ***H_2SO_4*** *and then* ***H_2O_2****!! Fill in slowly because of strong exothermic reaction*)

b) **10 min: di-water rinse with quick dump rinse**

2) HF-Dip (1%tig) :(removes oxide)

a) **20 sec: H_2O** : **HF** (50%) (7.35l: 0.15l)

b**) 5 min: di-water rinse with quick dump rinse**

3) SC- 1 :(removes remaining organic and some metallic contaminations)

a) **10 min @ 80°C: H_2O: H_2O_2: NH_3** (6.0l: 0.75l: 0.75l)

b) **10 min: di-water rinse with quick dump rinse**

4) HF-Dip (1%tig) :(removes oxide)

a**) 20 sec: HF** or **BOE**

b) **5 min: di-water rinse with quick dump rinse**

5) SC- 2: (removes metallic and some ionic contaminations)

a) **10 min @ 80°C: H_2O: H_2O_2: HCl** (6.0l: 0.75l: 0.75l)

b) **10 min: di-water rinse with quick dump rinse**

6) HF-Dip / BOE-Dip: (prior to deposition for instance)

a**) 20 sec: HF** (or) **BOE**

b) **5 min: di-water rinse with quick dump rinse**

H_2O_2: hydrogen peroxide; **H_2SO_4**: sulphuric acid; NH_4F: ammonium fluoride

HF: hydrofluoric acid; **NH_4OH**: ammonium hydroxide

HCl: hydrochloric acid.

Standard Recipe of AZ 9260

Application: positive process

Recipe:

- Substrate drying: 5’00“ @120 °C (hot plate)
- Adhesion-Promoter **HMDS:**
  - Recipe: HMDS_01
- Resist **AZ 9260**:
  - Spin Coating: 0’03“ @ 1000 min^{-1}
0’60“@ 3000 min^{-1}
  - Rest time: 2:00 min
  - Soft-Bake: 2:45 min @ 110 °C (Hot Plate)
  - Rest Time: 35:00 min
- Exposure: 1:30 min @ 15 mW/cm^2, 405 nm (Cl2)
- Development: 6’00“ with **AZ 726 MIF**

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