# B. TECH. PROJECT REPORT

# On Study of High Step-Up DC-DC Converters for PV Applications

BY Apoorva Kushwaha Shraddha Mehra Kartika Meena



DISCIPLINE OF ELECTRICAL ENGINEERING INDIAN INSTITUTE OF TECHNOLOGY INDORE November 2016

# Study of High Step-Up DC-DC Converters for PV Applications

## A PROJECT REPORT

Submitted in partial fulfillment of the requirements for the award of the degrees

of BACHELOR OF TECHNOLOGY in ELECTRICAL ENGINEERING

Submitted by:

Apoorva Kushwaha Shraddha Mehra Kartika Meena

Guided by:

Dr. Amod C. Umarikar Associate Professor Discipline of Electrical Engineering



INDIAN INSTITUTE OF TECHNOLOGY INDORE November 2016

## **CANDIDATES' DECLARATION**

We hereby declare that the project entitled **"Study of High Step Up DC-DC Converter for PV Applications"** submitted in partial fulfillment for the award of the degree of Bachelor of Technology in **'Electrical Engineering'** completed under the supervision of **Dr. Amod C Umarikar, Associate Professor, Electrical Engineering, IIT Indore** is an authentic work.

Further, we declare that we have not submitted this work for the award of any other degree elsewhere.

Shraddha Mehra

B.Tech. IV YearDiscipline of Electrical EngineeringIIT Indore

#### Apoorva Kushwaha

B.Tech. IV YearDiscipline of Electrical EngineeringIIT Indore

Kartika Meena B.Tech. IV Year Discipline of Electrical Engineering IIT Indore

## **CERTIFICATE by BTP Guide**

It is certified that the above statement made by the students is correct to the best of my knowledge and belief.

Dr. Amod C Umarikar, Associate Professor, Discipline of Electrical Engineering, Indian Institute of Technology Indore (Project Guide)

## **PREFACE**

This report on **"Study of High Step Up DC-DC Converter for PV Applications**" is prepared under the supervision of **Dr. Amod C Umarikar**, Associate Professor, Electrical Engineering, IIT Indore.

In this report, we have studied different topologies of DC-DC converter to step up the output voltage of PV Module, which is DC in nature. This DC output is then fed to an inverter which converts it to AC.

We have tried our best in explaining the content in a lucid manner constrained by our abilities and knowledge. We have also added graphs, flowcharts and diagrams where possible/applicable to make it more illuminating.

Shraddha Mehra Apoorva Kushwaha Kartika Meena B.Tech. IV Year Discipline of Electrical Engineering IIT Indore

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Shraddha Mehra (130002036) Apoorva Kushwaha (130002003) Kartika Meena (130003020) B.Tech. IV Year Discipline of Electrical Engineering Indian Institute of Technology Indore

#### **ABSTRACT**

With electricity demand escalating, and supply depending largely on non-renewable sources, we need to transit towards renewable resources. One such source of abundant renewable energy is the Sun. Solar energy is converted to electrical energy by PV module. This motivates us to use PV cells to the zenith of its capacity. Rural household applications generally involve AC power driven appliances while output power of PV cell is DC in nature. So, we feed output DC voltage of PV into the inverter which converts it to AC voltage. Output power of PV modules vary widely with changes in solar irradiation and temperature. Unfortunately, the power range of a single PV module usually ranges from 100 Watts to 300 Watts, and the maximum power point (MPP) voltage for inverters. In cases with lower input voltage, it is difficult for the inverter to reach high efficiency. Employing a high step-up DC–DC converter in front of the inverter. So, step up DC-DC converter is usually used in PV applications, in order to cope up with the range of the PV voltage, reduce inverter ratings and produce a desired voltage for the load or connection to the utility.

Therefore, in this context, it is necessary to utilize a high step-up DC-DC converter as an intermediate stage between the Solar PV and the inverter. Thus, we intend to study various different topologies of high step-up DC/DC converters through theoretical analysis and simulation, using PLECS software.

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#### **Chapter 1**

#### Quasi Z-Source DC-DC Converter with Switched Capacitor

#### **1.1. Introduction**

Quasi Z-source converter is a single stage soft switched power converter derived from Zsource converter topology, employing an impedance network coupling the source with the converter. Along with the advantages of Z-source network topology, quasi Z-source converter has some advantages, such as continuous input current and output current and lower voltage stress on impedance network capacitor and across switch. The proposed converter provides higher voltage gain. The current flow is bidirectional. The duty cycle of the switch can be adjusted to maintain constant voltage during load change. This converter is very suitable to boost low DC voltage from solar and fuel cells.



Fig.1. 1 Circuit topology of Quasi Z-Source DC-DC Converter with Switched Capacitor The above figure shows a circuit topology of Quasi Z-source dc-dc converter with cascaded switched capacitor. The proposed converter has a dc input voltage source  $V_E$ , Z- network, switch S, Switched Capacitors, a low-pass filter formed by  $L_f$  and  $C_f$  and the resistive load  $R_f$ . The Z-source network composed of the two inductors  $L_1$ ,  $L_2$ , and the two capacitors  $C_1$ ,  $C_2$  connected to the primary side of switched capacitors.

The switched capacitor network composed of two diodes  $D_1$ ,  $D_2$  and the two capacitors  $C_3$ ,  $C_4$  is connected to the primary side of the low-pass filter  $L_f - C_f$ . Value of capacitor  $C_3$  and  $C_4$  is equal. The switched capacitor enhances the boost factor range without any additional active switches. The  $L_f - C_f$  output filter is used to smoothen the output current and load voltage respectively

## **1.2. Circuit Operation**

The quasi Z- source dc-dc converter with switched capacitor has two operation modes, state 0 and state 1.

D —duty ratio  $T_s$ —total time period.  $DT_s$ —switch ON period.  $(1 - D)T_s$ —switch OFF period

#### 1.2.1. State 0 operation: when switch is ON

During the term of state 0, the switch S is ON and the diode  $D_0$  is off. During this mode inductor  $L_1$  is charged by capacitor  $C_2$  and voltage source  $V_E$ , inductor  $L_2$  is charged by capacitor  $C_1$ . The inductor  $L_f$  is charged through two capacitors  $C_3$ ,  $C_4$ . During this time switch voltage  $v_D$  is zero.



Fig.1. 2 Equivalent Circuit during state 0

As shown in fig, the following equations are derived in state 0:

$$L_{1} \frac{di_{L_{1}}(t)}{dt} = v_{L_{1}} = V_{E} + v_{C_{2}}$$

$$L_{2} \frac{di_{L_{2}}(t)}{dt} = v_{L_{2}} = v_{C_{1}}$$

$$L_{f} \frac{di_{L_{f}}(t)}{dt} = v_{L_{f}} = 2v_{C_{s}} - v_{o}$$

$$v_{C_{f}} = v_{o}$$

$$v_{D} = 0$$

$$v_{C_{3}} = v_{C_{4}} = v_{C_{s}}$$

#### 1.2.2. State 1 Operation: when switch is OFF

During the term of state 1, the switch S is OFF and the diode  $D_0$  is ON. During this mode, the capacitors  $C_3$ ,  $C_4$  and load R are charged by the voltage source  $V_E$ ,  $L_2$ ,  $L_f$  and  $L_1$ . Simultaneously capacitors  $C_1$  is charged from voltage source  $V_E$  and inductor  $L_1$ , and the capacitor  $C_2$  is charged by the inductor  $L_2$ .



Fig.1. 3 Equivalent Circuit during State 1

As shown in fig, the following equations are derived in state 1:

$$L_{1} \frac{di_{L_{1}}(t)}{dt} = v_{L_{1}} = V_{E} - v_{C_{1}}$$

$$L_{2} \frac{di_{L_{2}}(t)}{dt} = v_{L_{2}} = v_{C_{1}} - v_{C_{s}} = -v_{C_{2}}$$

$$L_{f} \frac{di_{L_{f}}(t)}{dt} = v_{L_{f}} = v_{C_{s}} - v_{o}$$

$$v_{D} = v_{C_{s}}$$

#### 1.3. Inductor (Volt-sec) balance: -

As all the inductor currents are periodic, no net flux variation can occur in any inductor over a switching period i.e. Average inductor voltage over a switching interval is zero.

$$V_{L_1} = \frac{1}{T_s} \int_0^{DT_s} (V_E + v_{C_2}) dt + \frac{1}{T_s} \int_{DT_s}^{T_s} (V_E - v_{C_1}) dt = 0 \quad \dots (1)$$

$$V_{L_{2}} = \frac{1}{T_{s}} \int_{0}^{DT_{s}} (v_{c_{1}}) dt + \frac{1}{T_{s}} \int_{DT_{s}}^{T_{s}} (v_{c_{1}} - v_{c_{s}}) dt = 0$$

$$V_{c_{1}} = (1 - D) V_{c_{s}} \qquad \dots (2)$$

$$V_{L_{2}} = \frac{1}{T_{s}} \int_{0}^{DT_{s}} (v_{c_{1}}) dt + \frac{1}{T_{s}} \int_{DT_{s}}^{T_{s}} (-v_{c_{2}}) dt = 0$$

$$DV_{c_{1}} = (1 - D) V_{c_{2}} \qquad \dots (3)$$

$$V_{L_{f}} = \frac{1}{T_{s}} \int_{0}^{DT_{s}} (2v_{c_{s}} - v_{o}) dt + \frac{1}{T_{s}} \int_{DT_{s}}^{T_{s}} (v_{c_{s}} - v_{o}) dt = 0$$

$$V_{o} = (1 + D) V_{c_{s}} \qquad \dots (4)$$

In steady state, the averaged capacitor voltages for  $T_s$  are constant. So,

$$V_{C} = \frac{1}{DT_{s}} \int_{0}^{DT_{s}} (v_{C}) dt = \frac{1}{(1-D)T_{s}} \int_{DT_{s}}^{T_{s}} (v_{C}) dt$$

Apply this in eqn (1),

$$V_E + DV_{C_2} - (1 - D)V_{C_1} = 0 \qquad \dots (5)$$

from eqn (2), (3) and (5),

$$V_E = (1 - 2D) V_{C_S} \qquad \dots \dots (6)$$

From eqn (4) and (6),

$$V_o = \frac{(1+D)}{(1-2D)} V_E$$

# **1.4.** Voltage gain $\left(\frac{V_o}{V_E}\right)$ versus the Duty Cycle D Curve.

Figure shows the voltage  $gain\left(\frac{V_o}{V_E}\right)$  versus the duty cycle D. It clearly shows that there are two operating regions. When the duty cycle is greater than 0.5, the converter enters negative gain region, i.e. the polarity of the output voltage is reversed. When the duty cycle is less than 0.5, the output voltage is inphase with the input voltage.

#### **1.5. Steady Space expressions:**

When converter is in equilibrium, the capacitor voltages  $V_{C_1}, V_{C_2}, V_{C_s}$  and inductor currents  $I_{L_1}, I_{L_2}, I_{L_f}$  can be expressed as follows: -



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Fig.1. 4 Voltage Gain vs. Duty Cycle

$$V_{C_1} = \frac{(1-D)}{(1-2D)} V_E \quad ; \quad V_{C_2} = \frac{D}{(1-2D)} V_E$$
$$V_{C_s} = \frac{V_E}{(1-2D)} \left[ 1 - \frac{D(1+D)}{(1-D)} \frac{R}{R_o} \right]$$
$$I_{L_1} = I_{L_2} = \frac{(1+D)}{(1-2D)} \frac{V_0}{R_o} \quad ; \quad I_{L_f} = \frac{V_0}{R_o}$$

Software requirement: -

Plecs

#### 1.6. Simulation:

Modelling and simulation of converters are described here. Inductance, capacitances and resistances values, plots are shown in the results. Simulation model of the proposed converter is built with PLECS simulator. The values of the circuit elements are as follows: -

$$\begin{split} C_1 &= C_2 = 1mF \;,\; C_3 = C_4 = 0.1\text{mF},\; C_f = 660\text{uF},\; L_1 = L_2 = L_f = 1mH \\ r_{L_1} &= r_{L_2} = r_{C_3} = r_{C_4} = r_{C_f} = R = 0.01ohms \;,\; R_o = 36ohms \;, V_E = 36volts \\ \text{Switching frequency},\; f_C &= 30\;KHZ. \end{split}$$

An ideal Mosfet switch was used as switch S. The three diodes  $D_0$ ,  $D_1$  and  $D_2$  were ideal i.e. forward voltage drop of the diodes was zero.



Fig.1. 5 Simulation Model of the proposed converter

The calculated waveform of the output voltage is as shown when the duty ratio D= 0.20 was given. The theoretical value of output voltage 72.00volts.



Fig.1. 6 Waveforms of output voltage, switched capacitor voltage, inductor 1 current and capacitor 1 voltage

## **1.7.** Conclusion:

Input current of proposed converter is continuous and the current flow is bidirectional. The proposed quasi Z- source dc-dc converter with switched capacitor provide higher voltage gain

$$V_o = \frac{(1+D)}{(1-2D)} V_E$$

compared to the conventional quasi Z- source dc-dc converter for same duty ratio D, whose voltage gain is,

$$V_o = \frac{(1-D)}{(1-2D)} V_E$$

Thus, this converter is very suitable to boost low DC voltage from solar and fuel cells.

## **Chapter 2**

#### Stacked Coupled-Inductor Boost Converter

#### **2.1. Introduction**

This group of the high-step-up coupled-inductor boost converters can be viewed as the boost converter combined with the flyback converter. The major advantage of the converter lies in the relatively simple and compact structure, where the leakage energy can be directly recycled to the output. Topological improvements in this group based on this basic converter mainly focus on applying soft-switching techniques to reduce switching loss and employing voltage multipliers to further raise the voltage gain. A few of these topologies have been discussed below.

# 2.2. High Boost Converter using Voltage Multiplier

#### 2.2.1. Features



Fig.2. 1 Circuit Diagram of High boost converter with voltage multiplier

- A pair of inductors is coupled magnetically and a secondary side of coupled inductors is rectified using a voltage multiplier.
- The multiplier can consist of various types. In this case, a voltage doubler is used.
- The number of multiplier can be adjusted to get a needed duty ratio.
- The main features of this converter are high conversion ratio, high efficiency, single low voltage switch and simple topology.

#### 2.2.2. Circuit Operation

The CCM (continuous conduction mode) is now considered to simplify the analysis of operational principles. There are four modes of operations:

*Mode 1*: After Switch S1 is turned on, the inductor current of L1 is increased linearly. The voltage of L2 is rectified through the multiplier, which is connected with capacitor voltage Vc3. Energy is stored in Inductor L1 and transferred to load by L2.

*Mode 2:* Switch S1 is turned off at this time. The stored inductor energy is transferred to capacitor C3 via input voltage and D. The voltage of C3 is charged up to the boost voltage of (1). The voltage of L2 as shown in (2) is also rectified through the multiplier.

*Mode 3:* After the current of primary winding of inductor reaches to zero, the current of secondary winding flows through the capacitor C1.







*Mode 4:* This mode exists in a discontinuous current mode. If inductor current is continuous, mode 1 to 3 will be repeated in sequence. In this mode, inductor current is discontinuous during turn-off state of the switch. Also, the capacitor at load side supplies a load current.



#### 2.2.3. Steady State Analysis

To analyze the steady state characteristics of the proposed converter in CCM, the leakage inductance, winding resistance, and transient characteristics of switch are neglected. If the inductor current is continuous, the capacitor voltage  $V_{c3}$  can be expressed as follows:

$$V_{c3} = \frac{Vin}{(1-D)}, D = T_{on}/T_s$$
(1)

where, D is the duty ratio, Ton is the pulse width, Ts is the switching period. Also, the capacitor voltage  $V_{c1}$  and  $V_{c2}$  can be expressed as follows:

$$V_{c1} = V_{in} \frac{nD}{1-D}, V_{c2} = nV_s$$
 (2)

where, n is turn ratio of L2/L1. Using (1) and (2), the output voltage can be expressed as follows:

$$V_{out} = V_{c1} + V_{c2} + V_{c3} = V_{in} \frac{2}{1 - D}$$
(3)

where, n is assumed to 1. If the voltage multiplier is increased, the output voltage can be expressed as the sum of voltages of output capacitors as follows:

$$V_{out} = V_{in} \frac{1 + nk}{1 - D}$$
(4)

where, k is the number of voltage doubler and n is the turns ratio.

With very low duty cycle,  $V_{C2}$  cannot be the product of turn ratio and input voltage because C2 cannot be charged fully due to very short duty cycle. If the turn-on time ends prior to the charging of capacitor C2 to nVs, output voltage will be decreased in proportional to the charging voltage of C2. In this case, it is assumed that the duty cycle is enough to guarantee the charging time of C2.

#### 2.2.4. Simulation



The PLECS schematic of the above -mentioned circuit is shown below:

Fig.2. 2 Magnetic Circuit Representation of high boost converter with voltage multiplier In this schematic, we have used the magnetic circuit representation of coupled inductor, with a turns ratio of 1, duty ratio of 0.5, frequency of 10kHz and input voltage of 30V. The waveforms for  $V_{c1}$ ,  $V_{c2}$ ,  $V_{c3}$  and  $V_{out}$  are shown below, which are in accordance with the theoretical values calculated using equations (1), (2) and (4).



Fig.2. 3 Waveforms of Vc1, Vc2, Vc3 and Vout

## 2.3. Ultra-Large Gain Step-Up Switched Capacitor DC-DC Converter 2.3.1. Features



Fig.2. 4 Ultra-large Gain Step-Up Switched Capacitor DC-DC Converter

- The connections of the two cells, the coupled inductor and the switched capacitor circuit give a large step-up voltage conversion ratio.
- The source energy is transferred through the coupled inductor to either the load or switched capacitors during the entire switching period.
- The leakage inductor energy of the coupled inductor can be recycled, increasing the efficiency.
- This also has the benefit of reducing the voltage stress on the active switch.

#### 2.3.2. Steady State Analysis

The energy is transferred from  $V_{in}$  during modes I–IV. As the duration of the modes I and III are very short, these modes are neglected in the calculation of the dc voltage conversion gain. To simplify the steady-state analysis, the leakage inductances at secondary and primary sides are neglected. The following equations are obtained:

$$V_{c3} = V_{in} \frac{n(1+D)}{1-D}, D = T_{on}/T_s$$
 (5)

$$V_{c4} = \frac{Vin}{1-D}$$
(6)

The output voltage results as the sum of  $V_{c3}$  and  $V_{c4}$ , giving the dc voltage gain:

$$V_{out} = V_{in} \frac{1 + (1 + D)n}{1 - D}$$

#### 2.3.3. Simulation

The PLECS schematic of the above-mentioned circuit is shown below:

(7)



Fig.2. 5 Magnetic Circuit Representation of Ultra-Large Gain Step-up Switched Capacitor DC-DC Converter

In the above schematic, we have used the magnetic circuit representation of coupled inductor, with a turns ratio of 1, duty ratio of 0.5, frequency of 10kHz and voltage input of 30V. The waveforms for  $V_{c3}$ ,  $V_{c4}$  and  $V_{out}$  are shown below, which are in accordance with the theoretical values calculated using equations (5), (6) and (7).



Fig.2. 6 Waveforms for Vc3, Vc4 and Vout

#### 2.3.4. Conclusion

There are two sections which cover two topologies of stacked coupled-inductor boost converters. In the first section, the novel high boost converter using the multiplier is presented and the operation and features have been described. The proposed method eliminates the problems of extreme duty ratio or complexity of circuits in the conventional topology. Also, the proposed circuit has the following various advantages compared to the conventional boost converters: low voltage stress, higher boost rate, higher efficiency, and several modified circuits for other applications. Therefore, the proposed converter can be applied to various high boost applications, such as a battery back-up system, fuel cells, military applications, etc.

In the next section, a switched-capacitor step-up dc-dc converter with coupled inductor is presented. It achieves a high step-up voltage gain. Since the energy of the leakage inductor of the coupled inductor can be recycled, the voltage stress across the main switch is constrained, allowing for the selection of a switch with a lower ON-state resistance. The inrush current problem of the switched-capacitor circuit has been well restrained by the leakage inductance of the coupled inductor. These merits contribute to the good efficiency of the proposed converter.

#### Chapter 3

#### Interleaved boost converter

#### **3.1**. Interleaving Technique

In high power applications, the stress on the power switches and the rectifiers can be so high that it is impossible to obtain the required power using a single converter. Hence, parallel operation of converters is necessary. The main advantage comes from the fact that sharing the input current among paralleled converters improves important aspects such as maintenance, repairing, loss-heat dissipation, reliability and fault tolerance.

An interesting solution, which has both of the features of paralleling operation, and increasing frequency is interleaving technique or multiphase operation of converters. In multiphase operation, converters are connected in parallel and they are controlled by interleaved switching signals, which have the same switching frequency and the same phase shifting. The switching instants are sequentially phase shifted by equal fractions of a switching period. This arrangement lowers the net ripple amplitude and raises the effective ripple frequency of the overall converter without increasing switching losses or device stresses. The resulting cancellation of low-frequency harmonics allows eventually the reduction of size and losses of the filtering stages. The obvious benefit is an increase in the power density without the penalty of reduced power conversion efficiency. There is still a penalty of increased circuit complexity (greater number of power handling components, their drives, protection and synchronized control etc.).

#### **3.2. Interleaving Technique in Boost Converter**

Generally, a multi-phase interleaved boost converter is for high power conversion applications. A basic boost converter converts a DC voltage to a higher DC voltage. Interleaving add additional benefits such as reduced ripple currents in both the input and output circuits. Higher efficiency is realized by splitting the output current into two paths, substantially reducing I<sup>2</sup>R losses and inductor AC losses. This technique has advantages such as reduce the inductor size, reduce the current ripple and for same rated value of components the rated of the output converter can be increased. However, this technique requires more number of components here considering two phase interleaved boost converter. The interleaved boost converter can be developed by some pair of the single-boost converters that be arranged in parallel connection with the switching frequency of each pairs are shifted over the switching period. With the help of interleaving technique, the inductor current of interleaved boost converter can be reduced. To analyse the stability and large signal time-domain transient analysis or small signal frequency-domain analysis of the converter, the average modelling has become employed.

#### **3.3.** Analysis of two phase Interleaved Boost Converter

It was seen in previous section that by paralleling the converters, input current is shared among the phases resulting in better efficiency and reliability. Moreover, number of paralleled stages results in lower current ripple at the input and lower voltage ripple at the output. But with more phases, analysing of the converter becomes tedious and it will be difficult to investigate and determine both steady and transient state. The two-phase boost converter is shown in Figure. 3.1 Each converter operates in continuous current mode (CCM) and these converters are controlled in current control mode. Further the converters are clocked with a series of synchronizing pulses, which are equally phase shifted in time.



Fig.3. 1 Two phase Interleaved Boost Converter

#### 3.3.1. Circuit Operation

The two-phase interleaved boost converter has four mode of operation in one switching cycle.

Mode1: When both switches S1, S2 are on.

Both diode D1, D2 are off, the current of Inductor L1 and L2 starts to rise while capacitor is discharging through load.



Fig.3. 2 Mode 1 operation

As shown in fig, the following equations are derived in mode 1:

$$\frac{dil1}{dt} = \frac{dil2}{dt} = \frac{V_{IN}}{L}.$$

Mode 2: when switch s1 is on and s2 is off

In this case inductor 11 current is discharging through capacitor and load and 12 is charging.



Fig.3. 3 Mode 2 Operation

As shown in fig, the following equations are derived in mode 2:

$$\frac{dil1}{dt} = \frac{V_{IN}}{L}$$
$$\frac{dil2}{dt} = \frac{V_{IN} - V_O}{L}.$$

Mode 3: when switch S1 is on and S2 is off. It is same as mode 1



Fig.3. 4 Mode 3 Operation

As shown in fig, the following equations are derived in mode 3:

$$\frac{dil1}{dt} = \frac{dil2}{dt} = \frac{V_{IN}}{L}$$

Mode 4: when switch S1 is off and S2 is on.

In this case 12 is discharging through capacitor and resistor and 11 is charging.



Fig.3. 5 Mode 4 Operation

As shown in fig, the following equations are derived in mode 3:

$$\frac{dil2}{dt} = \frac{V_{IN}}{L}$$
$$\frac{dil1}{dt} = \frac{V_{IN} - V_O}{L}$$

Steady state expression,

$$\frac{V_O}{V_{IN}} = \frac{1}{1 - D}$$

#### 3.4. Simulation

Modelling and simulation of converters are described here. Inductance, capacitances and resistances values, plots are shown in the results.

Simulation model of the proposed converter is built with PLECS simulator. The values of the circuit elements are as follows: -

$$C_1 = 680 \mu \text{F}, \ L_1 = L_2 = \text{L} = 400 \mu H$$

R = 1ohms ,  $V_{in} = 12$ volts

Switching frequency,  $f_c = 25 \ KHZ$ . An ideal Mosfet switch was used as switch S. The two diodes  $D_1 and D_2$  are ideal i.e. forward voltage drop of the diodes is zero.

The calculated waveform of inductor current and output voltage is as shown:



Fig.3. 6 Schematic of the Proposed Converter

**Case 1**: when D= 0.5, in this case ripple will be zero in final inductor current.



Fig.3. 7 waveforms of  $I_{11}$ ,  $I_{12}$ ,  $I_{out}$  when D=0.5

Case 2: when duty cycle is D=0.3

Here in this case, ripple in total inductor current is less due to interleaving



Fig.3. 8 waveforms of  $I_{11}$ ,  $I_{12}$ ,  $I_{out}$  when D=0.3

#### **3.5.** Conclusion

The input inductor makes the source current smooth and hence these converters provide very good EMI performance. In high power applications, the stress on the power switches and the rectifiers can be so high that it is impossible to obtain the required power using a single converter. Hence, parallel operation of converters is necessary. The main advantage comes from the fact that sharing the input current among paralleled converters improves important aspects such as maintenance, repairing, loss-heat dissipation, reliability and fault tolerance.

#### Chapter 4

#### **Photovoltaic Module**

#### **4.1. Introduction**

Photovoltaic system is an apparatus for converting solar energy to DC electric power. Photovoltaics cells or Solar cells consist of a p-n junction fabricated in a thin wafer or layer of semiconductor.

In the dark, the I-V output characteristic of a solar cell has an exponential characteristic similar to that of a diode. When exposed to light, photons with energy greater than the bandgap energy of the semiconductor are absorbed and create an electron-hole pair. These carriers are swept apart under the influence of the internal electric fields of the p-n junction and create a current proportional to the incident radiation. When the cell is short circuited, this current flows in the external circuit; when open circuited, this current is shunted internally by the intrinsic p-n junction diode. The characteristics of this diode therefore sets the open circuit voltage characteristics of the cell.

Solar cells are the basic building block of photovoltaics modules, otherwise known as Solar panels. A number of solar cells are arranged in series and parallel combinations to form a solar PV module. A PV panel is a non-linear power source, i.e., its output power/current depends on the terminal operating voltage and the maximum power generated by the system changes with temperature and solar radiation.

#### 4.2. Modelling the PV module

The simplest equivalent circuit of a solar cell is a current source in parallel with a diode. The output of the current source is directly proportional to the light falling on the cell. The diode determines the I-V characteristics of the cell. For this research work, a model of moderate complexity was used. The model included temperature dependence of the photocurrent I<sub>1</sub> and the saturation current of the diode I<sub>0</sub>. A series resistance  $R_s$  is included, but



Fig.4. 1 Circuit diagram of a PV module

not a shunt resistance. A single shunt diode is used with the diode quality factor set to achieve the best curve match.

# 4.3. Specifications of a PV module

Electrical Characteristics	PV Module
Maximum power ( <i>P<sub>max</sub></i> )	65W
Voltage at $P_{max}(V_{MPP})$	17.6V
Current at $P_{max}(I_{MPP})$	3.69A
Short-circuit current $(I_{sc})$	3.99A
Open-circuit voltage (V <sub>oc</sub> )	22.1V
Temperature coefficient of $I_{Sc}$	(0.065±0.015) %/ °C
Temperature coefficient of Voc	(80±10) mV/°C
Temperature coefficient of power	(0.5±0.05) %/ °C
NOCT (Air 20°C; Sun 0.8kW/m2; wind 1m/s)	47±2°C
Maximum series fuse rating	20A
Maximum system voltage	600V (U.S. NEC & IEC 61215 rating) 1000V (TÜV Rheinland rating)

#### Table 1: Specifications of a PV module

For our research work, following are some additional specifications of the PV panel:

Number of PV modules in String	2
Number of Strings in parallel	3

Maximum Power (P <sub>max</sub> )	390 W
Voltage at maximum power (V <sub>mpp</sub> )	35.2 V
Current at maximum power (I <sub>mpp</sub> )	11.07 A

#### 4.4. Maximum Power Point Trackers

The output characteristics of PV module depends on the solar insolation, the cell temperature and output voltage of PV module. Since PV module has nonlinear characteristics, it is necessary to model it for the design and simulation of maximum power point tracking (MPPT) for PV system applications. A maximum power point tracker (MPPT) is used for extracting the maximum power from the solar PV module and transferring that power to the load. The peak power is reached with the help of a DC-DC converter by adjusting its duty cycle such that the resistance corresponding to the peak power is obtained.

Maximum Power Point Tracking (MPPT) is an electronic system which operates PV to gain a maximum power. The problem considered by MPPT techniques is to automatically find the voltage ( $V_{MPP}$ ) and current ( $I_{MPP}$ ) at which a PV array should operate to obtain the maximum power output ( $P_{MPP}$ ) under a given temperature and irradiance. Maximal Power Point (MPP) does not lie at a particular point but it moves around P-V curve depends on light intensity and temperature. As the power supplied by the solar array depends on the insolation, temperature and array voltage, an important consideration in the design of an efficient solar array system is to track the maximum power point correctly. The purpose of the MPPT is to move the array operating voltage close to the MPP under changing atmospheric conditions. By using an intelligent algorithm, it ensures the PV module always operates at its maximum power point as the temperature, light intensity and load vary. Maximum power point trackers may implement different algorithms, such as perturb and observe. We have implemented the incremental conductance algorithm

#### 4.5. Incremental Conductance Method

Incremental Conductance was designed based on an observation of P-V characteristic curve. IC method tries to improve the tracking time and to produce more energy on a vast irradiation changes environment. This method shows a better performance and also has a lower oscillation.

$$P = VI$$

$$\frac{dP}{dV} = \frac{d(V.I)}{dV} = I + V \frac{dI}{dV}$$
MPP is reached when,  $\frac{dP}{dV} = 0$ 
*i.e.*

$$I + V \frac{dI}{dV} = 0$$
*or*



$$\frac{dI}{dV} = -\frac{I}{V}$$

FIG shows that the slope of the PV array power curve is zero at the MPP, increasing on the left of the MPP and decreasing on the right-hand side of the MPP

$$\frac{dP}{dV} > 0$$
 then  $\frac{dI}{dV} > -\frac{I}{V}$  at left of MPP

$$\frac{dP}{dV} = 0 \ then \ \frac{dI}{dV} = -\frac{I}{V} \qquad at \ MPP$$

$$\frac{dP}{dV} < 0 \text{ then } \frac{dI}{dV} < -\frac{I}{V} \qquad \text{ at right of MPP}$$

Where I and V are the PV array output current and voltage, respectively. The left-hand side of the equations represents the Incremental Conductance of the PV module, and the right-hand side represents the instantaneous conductance. From above equations, it is obvious that when the ratio of change in the output conductance is equal to the negative output conductance, the solar array will operate at the MPP. In other words, by comparing the conductance at each

sampling time, the MPPT will track the maximum power of the PV module by adjusting the duty cycle.

## Flowchart of Incremental Conductance method



Fig. 4. 2 Flowchart of the Incremental conductance method with direct control

SPECIFICATION	INCREMENTAL CONDUCTANCE		
Efficiency	High about 98%		
Complexity	Difficulty		
Realization	More complex		
Cost	High cost		
Reliability	accurate		
Rapidly changing atmosphere	Good and automatically adjusts modules operating voltage		

 Table 2: Advantages and Disadvantages of Incremental conductance MPPT method

#### 4.6. Conclusion

The circuit model of the PV module has been shown and the specifications of a PV module have been mentioned in Table 1. We use maximum power point tracker to ensure that we achieve max power even if light intensity and temperature varies. Out of various algorithms of MPPT we have implemented **Incremental conductance** method. Because IC method improves the tracking time and produces more energy on a vast irradiation changes environment. This method shows a better performance and also has a lower oscillation.

## **Chapter 5**

#### Inverters

#### **5.1. Introduction**

Inverter is basically an interface between DC source like photovoltaic cell and AC networks. The SPWM (Sinusoidal Pulse Width Modulation) technique of bipolar inverter is presented and the models are simulated in Plecs. The H-Bridge inverter topologies are made up of power electronic switches and are fed with constant amplitude pulses with varying duty cycle for each period. The SPWM pulses are generated by comparison of two waves- a carrier wave, which is triangular in this case and a modulating reference wave whose frequency is the desired frequency, which is sinusoidal in this case. This pulse width modulation inverter is characterized by simple circuitry and rugged control scheme that is SPWM technique to obtain inverter output voltage control and to reduce its harmonic content.

The basic inverter circuits perform the task of converting DC input power to AC output power. Inverter can be widely classified based on many parameters but considering one of them based on the arrangement of the power electronic switches are – Half Bridge Inverter and Full bridge inverter. A Full bridge inverter has two legs consisting of two semiconductor switches in each of them with the load connected at the centre points of the two legs.



Fig.5. 1 Full bridge Inverter

#### 5.2. Bipolar PWM Inverter

The basic idea to produce PWM Bipolar voltage switching signal is shown in Fig.6.2. It comprises of a comparator used to compare between the reference voltage waveform  $V_r$  with the triangular carrier signal  $V_c$  and produces the bipolar switching signal. If this scheme is applied to the full bridge single phase inverter as shown in Fig., all the switch  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$  are turned on and off at the same time. The output of leg A is equal and opposite to the output of leg B.

The output voltage is determined by comparing the reference signal,  $V_r$  and the triangular carrier signal,  $V_c$  and  $S_3$ ,  $S_4$  are turned on or turned off at the same time. The output of leg A is equal and opposite to the output of leg B. The output voltage is determined by comparing the control signal,  $V_r$  and the triangular signal,  $V_c$  as shown in Fig. 5 to get the switching pulses for the devices, and the switching pattern and output waveform is as follows.



Fig.5. 2 Bipolar Generator

#### **5.3. Simulation**

The Plecs model of bipolar inverter is as shown in Figure. A triangular generator and a sine wave generator are used for generating the carrier wave and the modulating wave respectively. The carrier frequency is Hz and the reference wave frequency is Hz. The modulation index can be varied by changing the amplitude of sinusoidal modulating wave.



Fig.5. 4 Waveforms of gating pulses and output voltage

## **5.4.** Conclusion

Inverter converts DC input to AC output. Sinusoidal Pulse Width Modulation technique is used to obtain inverter output voltage control and to reduce its harmonic content.

### **Chapter 6**

#### Filters

A filter is often used to interconnect an inverter to the utility grid in order to filter the harmonics produced by the inverter

#### 6.1. L-Filter

This type of filter is also called choke filter. It consists of an inductor L which is inserted between the rectifier and the load resistance  $R_L$ . The rectifiers contain AC components as well as DC components. When the output passes through the inductor, it offers a huge resistance to the AC components and no resistance to DC components. Therefore, AC component of rectified output is blocked and only DC component reached the load. It is the first order filter with attenuation 20 DB/decade over the whole frequency range. Therefore, the application of this type of filter is suitable for converters with high switching frequency, where the attenuation is succinct. On the other side inductance greatly decreases dynamics of the whole system converter filter.



Fig.6. 1 L Filter

#### 6.2. LCL-Filter

Their purpose is to filter the inverter's switching frequencies. The attenuation of the LCLfilter is 60 dB/decade for frequencies above resonant frequency, therefore lower switching frequency for the converter can be used. It also provides better decoupling between the filter and the grid impedance and lower current ripple across the grid inductor. Therefore LCL-filter fits to our application. The LCL filter has good current ripple attenuation even with small inductance values. However, it can bring also resonances and unstable states into the system. Therefore, the filter must be designed precisely according to the parameters of the specific converter.



Fig.6. 2 LCL Filter

## **6.3.** Conclusion:

A L- filter or LCL- filter is usually placed between the inverter and the grid to attenuate the switching frequency harmonics produced by inverter. Compared with L-filter, LCL-filter has better attenuation capacity of high order harmonics and better dynamics characteristics. However, an LCL filter can cause stability problems due to undesired resonance caused by zero impedance at certain frequencies.

## **Chapter 7**

## **Results**

## 7.1. PV Module

The Plecs schematic of a PV module is shown below. This schematic has been used as a subsystem in the final schematic.





## 7.2. Incremental Conductance MPPT method

The following code is used to implement the algorithm in the final Plecs schematic.

#define V Input(0) #define I Input(1) #define P\_old DiscState(0) #define Vref DiscState(1) #define inc DiscState(2) #define V\_MAX 36 #define V\_MIN 0 #define DeltaV 0.01 //Global variable static double P;  $P_old = 0;$ Vref = 35;inc=-1; P = V\*I;if(P<P\_old) ł

```
inc=-inc;
}
Vref=Vref+inc*DeltaV;
if (Vref>V_MAX)
{
Vref=V_MAX;
}
if (Vref<V_MIN)
{
Vref=V_MIN;
}</pre>
```

Output(0) = Vref;

 $P_old = P;$ 

## 7.3. Full Bridge Inverter

The Plecs schematic of inverter, as a subsystem, is shown below:



Fig.7. 2. Inverter subsystem

## 7.4. Filters

The Plecs schematic of L and LCL filters are shown below:



Fig.7. 3. L filter subsystem



Fig.7 4. LCL filter subsystem

## 7.5. Closed loop control of Converter output

## 7.5.1. Voltage Controller

The Plecs schematic of voltage controller is shown below. This schematic has been used as a subsystem in the final schematic.



Fig.7. 5.1. Voltage Controller subsystem

## 7.5.2. Current Controller

The Plecs schematic of current controller is shown below. This schematic has been used as a subsystem in the final schematic.

#### Proportional-resonant controller



Fig.7.5.2. Current Controller subsystem

## 7.5.3. Unipolar Modulator

The Plecs schematic of unipolar modulator is shown below. This schematic has been used as a subsystem in the final schematic.



Fig.7.5.3. Unipolar Modulator subsystem

## 7.6. High Boost Converter with Multiplier



Fig.7.6. 1 Final schematic of high boost converter with voltage multiplier



#### 7.6.1. Waveforms

Fig.7.6. 2 Waveforms of  $V_{pv}$ , Duty ratio and  $V_{conv}$  for High Boost Converter with Voltage Multiplier

## 7.6.2. Output with L filter



Fig.7.6. 3 Inverter output with 1 filter for high boost converter

## 7.6.3. Output with LCL filter



Fig.7.6. 4 Inverter output with lcl filter for high boost converter



7.7. Ultra Large Gain Step-up Switched Capacitor DC-DC Converter





## 7.7.1. Waveforms



## 7.7.2. Output with L filter



Fig.7.7. 3 Output with 1 filter for Ultra Large Gain Step-Up Switched Capacitor Converter



## 7.7.3. Output with LCL filter

Fig.7.7. 4 Output with lcl filter for Ultra Large Gain Step-Up Switched Capacitor Converter

## 7.8. Quasi Z- Source DC-DC Converter with Switched Capacitor



Fig.7.8. 1 Final Schematic of Quasi Z- Source DC-DC Converter with Switched Capacitor



## 7.8.1. Waveforms

Fig.7.8. 2 Waveforms of V<sub>pv</sub>, I<sub>pv</sub>, V<sub>conv</sub> and Duty ratio

## 7.8.2. Output with L filter



Fig.7.8. 3 Output with 1 filter for Quasi Z-Source Converter with switched capacitor

# 7.8.3. Output with LCL filter



Fig.7.8. 4 Output with lcl filter for Quasi Z-Source Converter with switched capacitor

## 7.9. Interleaved boost converter



Fig.7.9. 1 Final Schematic of Two Phase Interleaved Boost Converter





Fig.7.9. 2 Waveforms of  $V_{pv}$ , Duty Ratio and  $V_{conv}$  for Two Phase Interleaved Boost Converter

## 7.9.2. Output with L filter



Fig.7.9. 3 Output with l filter for Two Phase Interleaved Boost Converter

## 7.9.4 Output with LCL filter



Fig.7.9. 4 Output with lcl filter for Two Phase Interleaved Boost Converter

## 7.10. Conclusion

The simulation results of the final assembled circuits of the four different topologies discussed in the early chapters, have been presented in this chapter.

# Chapter 8

# **Conclusion and Future Work**:

# **Comparison of the proposed Converters:**

## Table 3: Comparison of the proposed converters

Topology		Component count (switch/cap acitor/ diode/magn etic core)	Voltage Gain	Switch Voltage Stress	Advantages
Stacked coupled- inductor	High boost with voltage multiplier	1/3/3/1	$\frac{1+n}{1+D}$	$\frac{Vout}{1+n}$	<ul> <li>Improve Step-up gain and utilization of magnetic core</li> <li>Low switch walkage stragg</li> </ul>
boost converter	Ultra Large Gain Step up with switched capacitor	1/4/4/1	$\frac{1+n+Dn}{1-D}$	$\frac{Vout}{1+n+nD}$	Alleviate reverse recovery problem and parasitic oscillations
Quasi Z- Converter Capacitor	Source DC-DC with Switched	1/5/3/0	$\frac{1+D}{1+2D}$	$\frac{1+D}{1-D}$	<ul> <li>high voltage gain</li> <li>continuous input and output current</li> <li>low voltage stress on capacitors</li> </ul>
Interleaved Converter	d Boost	2/1/2/0	$\frac{1}{1-D}$		<ul> <li>Due to current sharing ripple reduces</li> <li>low voltage stress on switches</li> </ul>

The task of this project is to study different topologies of DC-DC converters for developing an intermediate between the PV Module and the Inverter. From the above chapters and the results of the simulation and experimental studies, it can be observed that the proposed configurations have the ability to operate successfully under different operating conditions.

The respective topologies have the ability to operate the PV at MPP, using the Incremental Conductance MPPT method. It can be observed that the IC method successfully suppresses the oscillation around MPP. The drawback of this method is its low tracking time. The tracking time can be improved by adjusting the increment/decrement step of duty cycle. The increment/decrement step also could be adaptively changed to achieve a better time response. Each of these converters are then connected to an inverter, which in turn is connected to a grid. This is an efficient way of utilizing the renewable energy resources for domestic appliances or

for remote places, where the transmission of power is not possible.

For future work, hardware implementation of the proposed configurations can be carried out. Inclusion of some of the non-idealities, that have been ignored in this project, can be taken up as the next few steps for this project.

#### Chapter 9

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